# Shielded Passive Devices for Silicon-Based Monolithic Microwave and Millimeter-Wave Integrated Circuits

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***Abstract*—This paper introduces floating shields for on-chip transmission lines, inductors, and transformers implemented in production silicon CMOS or BiCMOS technologies. The shield minimizes losses without requiring an explicit on-chip ground connection. Experimental measurements demonstrate $Q$-factor ranging from 25 to 35 between 15 and 40 GHz for shielded coplanar waveguide fabricated on 10 Ω·cm silicon. This is more than a factor of 2 improvement over conventional on-chip transmission lines (e.g., microstrip, CPW). A floating-shielded, differentially driven 7.4-nH inductor demonstrates a peak $Q$ of 32, which is 35% higher than an unshielded example. Similar results are realizable for on-chip transformers. Floating-shielded bondpads with 15% less parasitic capacitance and over 60% higher shunt equivalent resistance compared to conventional shielded bondpads are also described. Implementation of floating shields is compatible with current and projected design constraints for production deep-submicron silicon technologies without process modifications. Application examples of floating-shielded passives implemented in a 0.18-$\mu$m SiGe-BiCMOS are presented, including a 21–26-GHz power amplifier with 23-dBm output at 20% PAE (at 22 GHz), and a 17-GHz WLAN image-reject receiver MMIC which dissipates less than 65 mW from a 2-V supply.**

***Index Terms*—Bondpads, coplanar transmission lines, floating shield, inductors, millimeter-wave integrated circuits, MMICs, on-chip interconnects, patterned ground shield, silicon, slow-wave transmission lines, substrate loss, transformers.**

## I. Introduction

SILICON system-on-a-chip (SoC) or system-in-a-package (SiP) are enabling technologies for the next generation of low-cost portable multimedia wireless devices. These fourth generation systems will evolve from current wireless data networks, but their economic viability depends upon low-cost realizations with a rapid time to market. This favors highly integrated silicon SoC/SiP realizations with reproducible radio frequency (RF) performance [1].

As transistor $f_T$ progresses beyond 100 GHz, silicon transistors are enabling circuit applications above 10 GHz (i.e., into the millimeter-wave or mm-wave frequency band, where the wavelength on-chip is $<$10 mm). With gain-bandwidth products approaching 300 GHz projected for silicon transistors in the near future, many circuit techniques that are commonly used at lower frequencies may become practical to implement in the low-GHz range. For example, negative feedback loops to set gain, input/output impedances and optimize the dynamic range of an RF amplifier without compromising stability could become practical [2]–[4]. However, linear passive devices with stable, reproducible characteristics are needed to implement such feedback networks so that designers can capitalize on the traditional benefits of feedback in RF circuits. Reactive components (e.g., inductors, transformers and capacitors) do not contribute thermal noise, and may therefore be used to realize circuits with the widest possible dynamic range. Linear on-chip magnetic components, such as inductors and interstage coupling transformers have also been proven as a basis for RF circuit topologies that operate below 1 V, which is desirable for integration of analog RF functions using deep-submicron CMOS technologies [5]–[9].

Passives with low parasitic losses that can be isolated from other circuit sub-blocks are required to complement the gain-bandwidth of silicon transistors for microwave and mm-wave applications. Unfortunately, the parasitics of RF on-chip passive components are not scaling as readily as the parasitics which accompany active devices such as transistors. Until these components are developed, well-known circuits that could capitalize on advances from Moore's Law will continue to be constrained by the (under-performing) interconnections and passive components surrounding the active devices.

Semiconducting silicon substrates with 1–20 Ω·cm resistivity are typically used to manufacture mixed-signal RF ICs, and the conductive substrate is a well-known cause of signal loss in passives [10], [11]. Shielding methods for inductors and transmission lines, such as the patterned ground shields [12]–[14] have been developed to minimize the RF energy coupled into the substrate. By placing a ground plane between an inductor and the silicon substrate, the electric field leaking into the silicon may be reduced almost to zero. However, in practice it is difficult to implement an on-chip ground reference that does not suffer some voltage variation due to parasitics from circuit and package interconnections. When an AC voltage is present on the shield (which is positioned close to the substrate to reduce parasitic capacitance), energy is again lost to the silicon rendering the shield ineffective. Due to the aforementioned scaling difficulties, this

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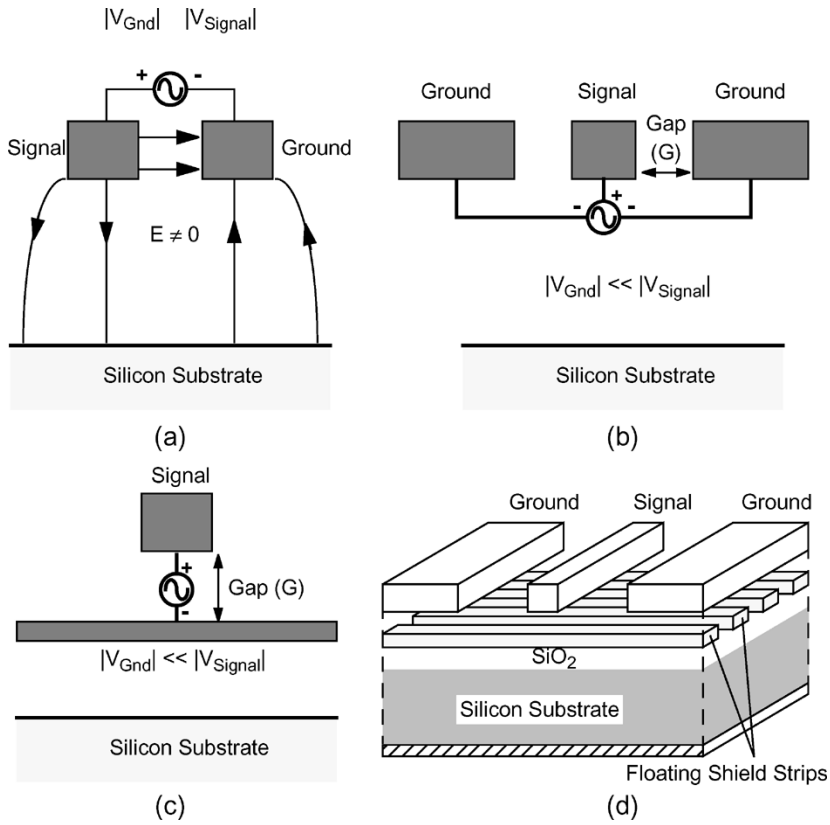


Fig. 1. Cross section highlighting ground path voltages of commonly used transmission lines. (a) Balanced. (b) Coplanar waveguide. (c) Microstrip. (d) S-CPW.

problem is exacerbated as operating frequencies advance into the mm-wave range.

In this paper, a floating shield technique that is suited to differential RF topologies is proposed to minimize substrate loss. Section II is devoted to the discussion of an ideal ground and what is required to implement a good approximation of an ideal ground on an MMIC, and the concept of a floating shield introduced. Section III describes slow-wave coplanar waveguide (S-CPW) on-chip interconnects. Together with a floating shield, S-CPW attains below 0.5-dB/mm loss at 40 GHz, high quality factor ($Q$), and adjustable wavelength. These characteristics cannot be matched using conventional transmission line designs such as microstrip and CPW [15]. Section IV discusses adaptation of the floating shield concept to monolithic inductors and transformers [16], and includes a detailed discussion of experiments and development of an equivalent circuit model and model parameter extraction technique. Section V demonstrates uses for the floating shield in other RF circuit components, including on-chip capacitors and input/output bondpads. Circuits that benefit from the use of floating-shielded passive components in typical RF IC applications are presented as examples throughout.

## II. Design Challenges of MMIC Passives in Silicon Technology

Ohmic loss, parasitic inductance, and parasitic capacitance of interconnect metals in silicon IC technologies are common impairments in monolithic microwave integrated circuits (MMICs) operating at a large fraction of the transistor $f_T$. The effects of these factors on typical circuit interconnections are discussed in the following subsections.

### A. Ground Plane Requirement for an MMIC

On-chip active and passive components typically use a ground plane to complete a current loop. An ideal ground plane is a near-zero impedance pathway, so it serves well as a current return and voltage reference (e.g., 0 V) for single-ended circuits. However, neither a true 0 V reference nor zero impedance paths exist on-chip in practice. Instead, the current-return path approximates an ideal ground only when it is intentionally designed for near-zero voltage swing. For example, when a coaxial transmission line is excited by an AC source (such as a transistor), the outer ground conductor remains at 0 V as predicted by Gauss's and Ampere's Laws (i.e., $\mathrm{V_{Gnd}} = 0$).[1] As a result, leakage of the electromagnetic field (EM-field) beyond the ground is minimized.

However, a ground path undergoes some voltage swing if it forms an incomplete coaxial shield around the (center) signal conductor. If the outer shield of a coaxial interconnect [as shown in Fig. 1(a)] is reduced to an identical cross-sectional area as the signal, the ground path (i.e., the shield) carries a voltage identical in magnitude to the signal path: $|\mathrm{V_{Gnd}}| = |\mathrm{V_{Signal}}|$, due to symmetry. Commonly used on-chip (planar) transmission lines, such as coplanar waveguide [CPW in Fig. 1(b)] and microstrip [Fig. 1(c)], lie in between the extreme cases where $\mathrm{V_{Gnd}} = 0$ or $|\mathrm{V_{Gnd}}| = |\mathrm{V_{Signal}}|$ because of the layered (i.e., metal–insulator–metal) structure. In order to compensate for this limitation,

[1]Assuming that the frequency is low enough and a TEM mode dominates.

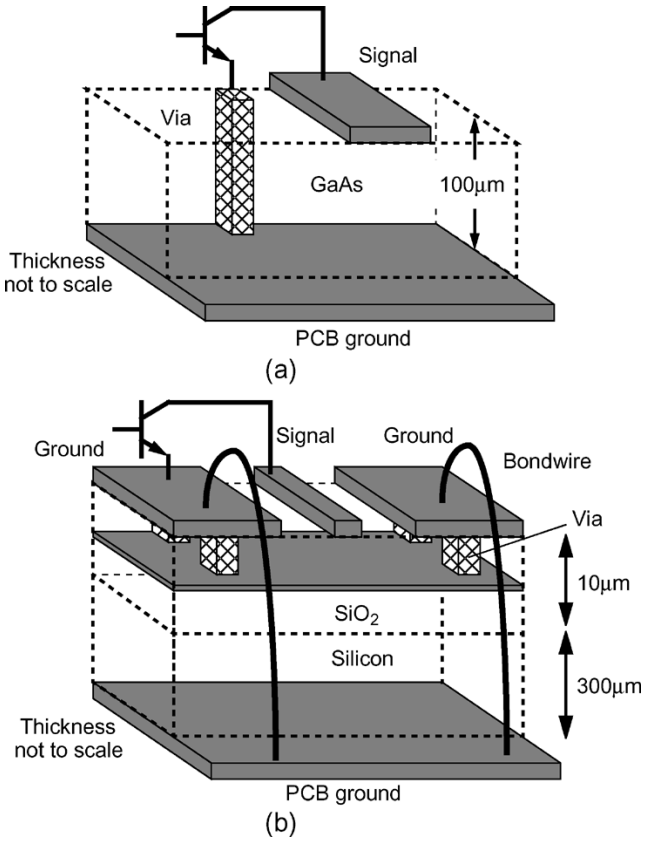


Fig. 2. Comparison of metal interconnect schemes typically used in production III-V (e.g., GaAs) and silicon technologies. (a) III-V GaAs technology. (b) Silicon-based technology.

the ground path is typically made much wider than the signal path (e.g., >5 times wider) to minimize AC voltage swing.

Fig. 1(d) illustrates a slow-wave coplanar waveguide (S-CPW). It uses floating metals to shield against substrate loss without relying on an explicit ground connection. This shielding structure also slows down signal propagation, resulting in wavelength reduction that is adjustable in the physical design of a circuit. S-CPW will be described in more detail in Section III.

### B. Ground on Silicon MMIC

Implementation of a true ground reference for circuits fabricated on a silicon substrate is hindered by the inability to make through-wafer ground connections between devices on top of a chip and a backside ground plane via the substrate [as in Fig. 2(a)]. Unlike III-V MMIC technologies, where the off-chip ground directly serves as a common voltage reference and return current path for on-chip components, ground paths on a silicon IC must be explicitly defined using on-chip metals [see Fig. 2(b)]. These on-chip metal layers are relatively thin (e.g., 0.3–1 $\mu$m per metal level, except for the top metal), and their area is limited because holes or slots are added to prevent stress-induced intermetal dielectric cracking. Furthermore, the on-chip ground is connected to the off-chip circuit ground at the periphery of the IC, often using bondwires. The parasitic inductance and resistance contributed by relatively thin on-chip metals used to implement a ground combine with the bondwire parasitics to isolate the on-chip and off-chip grounds from each other. Consequently, the ground on a silicon MMIC has some AC voltage swing.

### C. Narrow Transmission Lines on Lossy Substrate

When the signal and ground are both implemented on a silicon MMIC, the signal paths are typically a fraction of those in other microwave circuit technologies (e.g., one-sixth for microstrip [17]). The signal and ground of a microstrip line fabricated on an insulating or semi-insulating (i.e., III-V semiconductor) substrate are separated by the full substrate thickness (e.g., 100 $\mu$m). Since the line parasitic capacitance is relatively small, a microstrip line with a 50-$\Omega$ characteristic impedance may have a wide signal path (e.g., $\sim$ 70 $\mu$m on an insulating substrate) [19], [20]. Substrate vias connect the ground on the chip to a metal die attach plate in the IC package through low inductance vias. By contrast, the signal and ground for microstrip on a silicon MMIC are separated by only a few microns of intermetal dielectric, resulting in a relatively large capacitance between signal and ground. Consequently, 50-$\Omega$ microstrip has a relatively narrow signal path (e.g., 6 $\mu$m in width for a 4-$\mu$m-thick dielectric). Ohmic resistance of microstrip-on-silicon is about an order of magnitude greater than for an insulating substrate as on a typical GaAs MMIC, because of the narrow signal conductor and thin ground plane on the chip.

The relatively small signal-to-ground gap of microstrips on a silicon MMIC also constrains the reactive energy storage and the quality factor figure of merit ($Q$, [17]). The $Q$-factor of a transmission line is defined as

$$Q = \frac{\beta}{2\alpha} \tag{1}$$

where $\beta$ is the phase delay along the line (in radians/m) and $\alpha$ is the attenuation per unit length (in Nepers/m). A higher $Q$-factor indicates lower loss per radian (or degree) of phase-shift and also lower loss per wavelength in a delay line or a quarter-wavelength transmission line transformer.

Coplanar waveguide (CPW) has the inherent advantage that it allows a wider signal path to be used, because the physical gap between signal and ground of CPW (as shown in Fig. 1) is not set by the dielectric thickness. Increasing this gap lowers the signal to ground capacitance, allowing a wider signal path to be used. For example, a 50-$\Omega$ CPW with 5-$\mu$m gap can have a 15-$\mu$m-wide signal path. If the gap is increased to 20 $\mu$m, the signal can be increased to 50 $\mu$m wide while maintaining a 50-$\Omega$ characteristic impedance. However, the ground conductors of a CPW do not shield the signal conductor from the underlying the substrate. Therefore, if the gap is not smaller than the dielectric thickness to confine the EM-field, there is a significant loss of energy to the substrate. Relatively wide signal paths and their accompanying large gaps suffer from attenuation and low $Q$-factor due to such losses on a silicon MMIC. In the next section, a CPW with a floating shield is described (S-CPW) which can realize a $Q$-factor at mm-wave frequencies comparable to transmission lines fabricated on insulating and semi-insulating substrates.

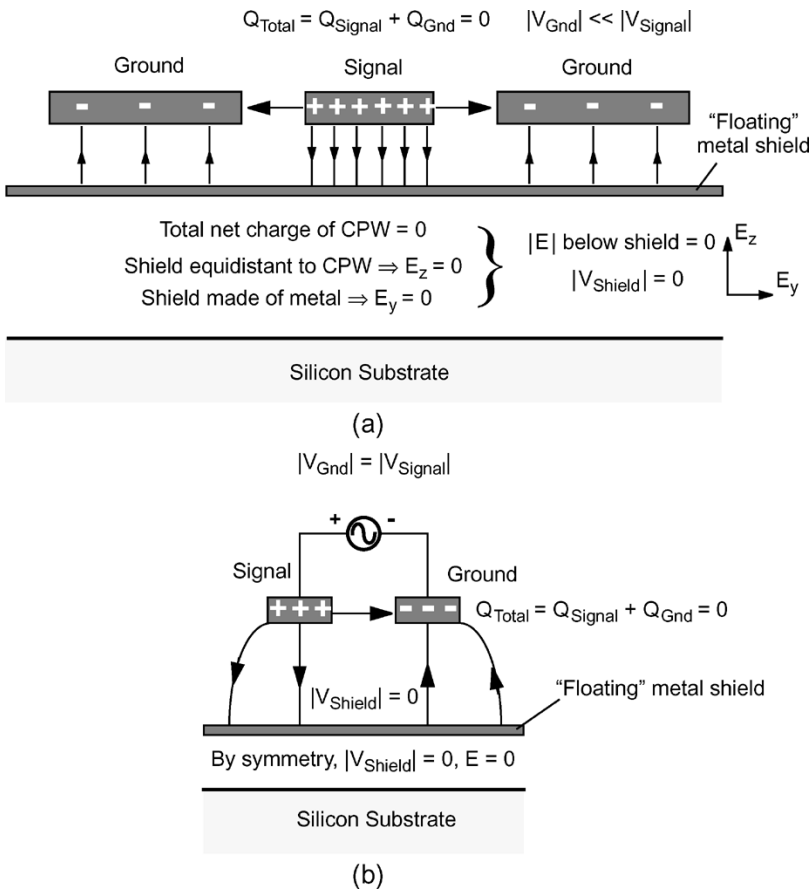


Fig. 3. Transmission lines with floating shield. (a) Coplanar waveguide. (b) Differential.

## III. Slow-Wave CPW With Floating Shields

The difficulty of designing a truly 0 V ground path is that the ground itself is directly connected to, and driven by, the AC source. This causes the polarity of the ground plane potential to alternate between positive and negative over each RF cycle. The voltage swing on the ground plane couples energy to the conductive substrate causing losses. A floating shield technique that reduces the electric field coupling to the substrate is described in this section. Application of a shielded transmission line is used to illustrate the design concept.

Fig. 3(a) shows a ground–signal–ground cross section of a CPW where metal strips (i.e., metal not connected to any circuit nodes) are placed underneath the CPW as a floating shield. Since the shield is a good conductor, there is no electric field tangential to the strips. For a component of the electric field from the CPW to enter the substrate vertically, the shield must be subject to a net electric flux from the CPW (i.e., net electric field summed over the area of the shield). However, this is not the case because there is no net charge on the CPW. Thus, the voltage on the shield is at 0 V with respect to the CPW, and the floating strips can act as an effective electric shield between the CPW line and the substrate. Moreover, unlike an explicitly grounded substrate shield that is susceptible to circuit parasitics (such as parasitic inductance), the floating shield remains close to 0 V regardless of the selection of signal and ground conductor widths. Similarly, a floating shield stays at 0 V when applied to a pair of coplanar differential transmission lines [Fig. 3(b)].

### A. Slow-Wave Coplanar Waveguide

Transmission lines one-quarter of a wavelength long are commonly used in microwave circuits [17]. For conventional transmission lines such as CPW and microstrip, the speed of the signal propagation is a constant that is solely governed by effective dielectric constant of the surrounding media. Therefore, the wavelength (which is the ratio of speed and frequency) cannot be adjusted by the circuit designer.

The slow-wave coplanar waveguide (S-CPW) was first proposed by Seki and Hasegawa for reducing the signal speed and the dimension of transmission lines on semi-insulating (e.g., GaAs) substrates [21]. Since wavelength is proportional to the signal speed, a more compact quarter wavelength long transmission line can be made using an S-CPW with a periodic structure that slows down the wave velocity.

The slow-wave phenomenon can be explained from the circuit perspective. If the alternating high and low impedance sections are short in length compared to the wavelength (i.e., finely distributed), each section can be approximated by an $L$-$C$ lumped element model, where $L$ and $C$ are the line inductance and capacitance of the section, respectively. In this example, the transmission line is assumed to be in a uniform dielectric media. The high-impedance section is designed to have line inductance $nL$ and line capacitance $C/n$, so that its characteristic impedance is higher by a factor of $n^2$ than the low-impedance section with line inductance $L/n$, and line capacitance $nC$. Notice that designing the section to achieve

a higher inductance (by a factor $n$) requires a proportionally smaller line capacitance (also by a factor $1/n$) because the wave velocity is fixed by the dielectric constant. In the physical layout of the transmission line, higher inductance requires more distance between the signal and ground paths which reduces the line capacitance, as desired. However, when the two sections are cascaded together, the series inductance is dominated by the high impedance section, while the capacitance is dominated by the low-impedance section. This causes a simultaneous increase of the both the $L$ and $C$, resulting in an increased delay of the signal, which is proportional to the square root of the $LC$ product. The wave velocity and wavelength are reduced by a factor of $n/2$ (for $n \gg 1$) and give rise to the slow-wave phenomenon.

### B. S-CPW on Silicon MMIC

In silicon technologies, the floating shield can be added to a conventional CPW to form the slow-wave coplanar waveguide (S-CPW) [15]. In additional to an adjustable wavelength, S-CPWs on silicon MMICs have several advantages over conventional microstrip and CPW. Conventional microstrip lines will have a narrower signal path and thin ground plane compared to an S-CPW line with the same characteristic impedance. Conventional CPW lines do not have a substrate shield, and hence have higher attenuation. Fig. 1(d) shows the design of the S-CPW on a silicon substrate. It consists of a conventional CPW, and an array of closely spaced floating shield strips which spans the width of the CPW and is placed beneath it. A wide gap between signal and ground can be used to achieve a relatively high inductance, while the floating shield minimizes the substrate loss. If the shield strips are short (i.e., order of microns in the direction of the current flow), the current induced onto the shield strips by signal current is negligible. Therefore, the line inductance is not affected by the shield. However, the shield strips add parasitic capacitance between the signal and the ground paths. As a result, the line inductance and capacitance of the original CPW are increased simultaneously by the addition of the floating shield strips.

### C. Transmission Line Experiments

Fig. 4 illustrates the wiring schemes used for the experiments. The first is a four-level metal version of IBM's SiGe-7HP BiCMOS technology interconnect, which uses aluminum top metals [i.e., top two metals as shown in Fig. 4(a)] and copper for the lower wiring levels. The second is a single damascene copper process, with wiring thicknesses as shown in Fig. 4(b). Tungsten vias connect all aluminum metal layers and copper vias are used between copper wiring levels. The test wafers did not have a final nitride passivation layer normally used for scratch protection. Without this passivation layer, the transmission line characteristic impedance is slightly higher than when passivation is used. The following transmission line experiments were fabricated using the aluminum-copper metallization scheme [Fig. 4(a)] on 10 Ω·cm resistivity substrate.

Four types of transmissions line are compared in this paper, including CPW, MS (i.e., microstrip), and S-CPW. The fourth type is S-CPWG, which is similar to the S-CPW, but with the lower shield strips connected to the top ground paths using vias

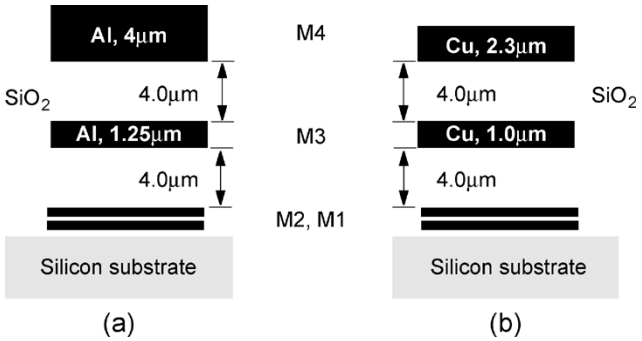


Fig. 4. Wiring schemes used for the experiments. (a) Aluminum-copper process; (b) all-copper process.

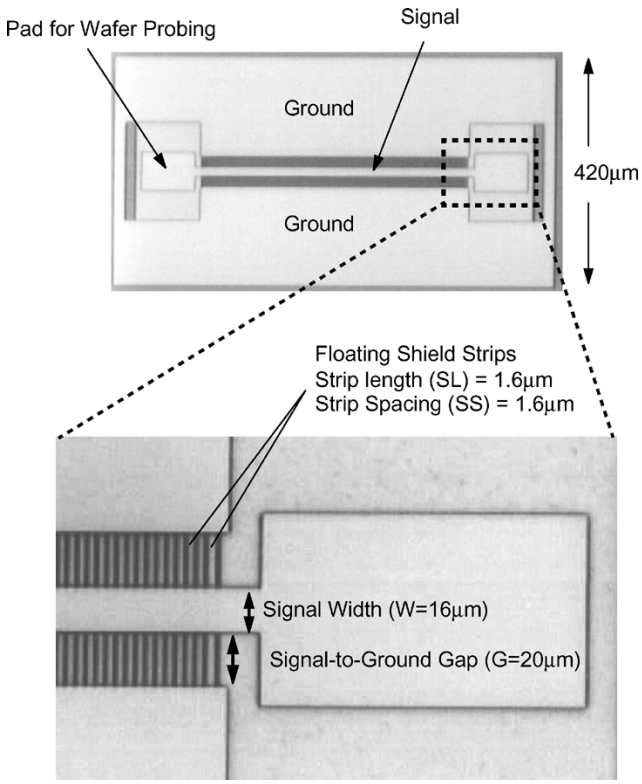


Fig. 5. Micrograph of an example S-CPW test line, 500 $\mu$m long.

(i.e., a grounded shield). Fig. 5 shows a micrograph of one of the S-CPW lines fabricated for testing. It has a 16-$\mu$m signal path and 20-$\mu$m signal-to-ground gap. The floating shield strips on the second-highest level metal (i.e., M3) are 1.6 $\mu$m in length and spaced 1.6 $\mu$m apart.

Specifications of the transmission lines characterized in this work are listed in Table I. To ensure a fair comparison between different designs, all of the transmission lines are designed with the same characteristic impedance. A $Z_o$ of 50 Ω was chosen in order to simplify measurement with a 50-Ω vector network analyzer. All the test structures have a total width of 420 $\mu$m to ensure that they consume the same amount of silicon area per unit length. Also included in Table I are the signal path width (W) and the signal-to-ground gap (G) for each of the transmission line types. For each type, two test lines with different gaps were tested (e.g., CPW1 and CPW2 in Table I). Conventional

TABLE I
TRANSMISSION LINES ($Z_o \approx 50\ \Omega$) TESTED FROM 1 TO 40 GHZ

| Transmission Line | Signal Width (W) | Signal-to-Ground Gap (G) | Shield Strip Length (SL) | Shield Strip Spacing (SS) |
|---|---|---|---|---|
| CPW1 | 15μm | 5 μm | No shield strips | |
| CPW2 | 50μm | 20μm | | |
| MS1 | 6μm | 4μm (between M4 signal on M3 ground plane) | | |
| MS2 | 15μm | 9.25μm (between M4 signal on M2 and M1 ground plane) | | |
| CPW_REF (on alumina) | 55μm | 20μm | | |
| S-CPW1 | 16μm | 20μm | 1.6μm | 1.6μm |
| S-CPW2 | 34μm | 120μm | 1.6μm | 1.6μm |
| S-CPW3 | 16μm | 20μm | 10μm | 2μm |
| S-CPW4 | 34μm | 120μm | 4μm | 5μm |
| S-CPWG1 (grounded shield) | 26μm | 120μm | 1.6μm | 1.6μm |

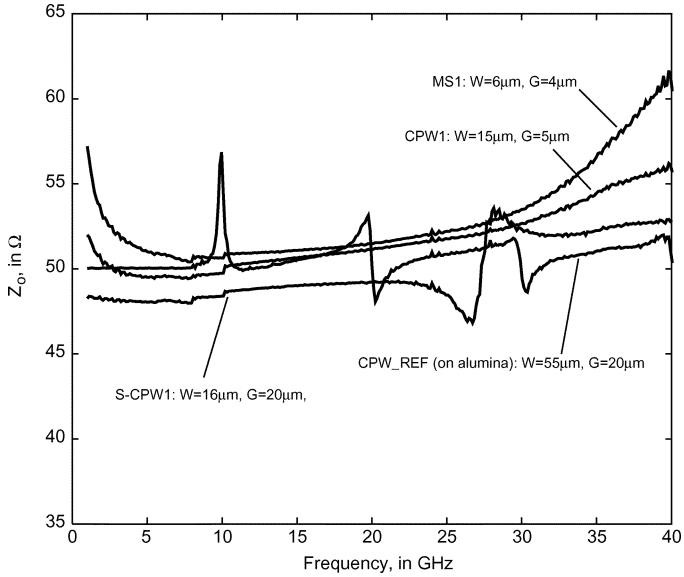


Fig. 6. Characteristic impedance of microstrip, CPW and S-CPW on silicon substrate.

coplanar waveguides CPW1 and CPW 2 are fabricated using the top (M4) metal. Microstrip line MS2 is fabricated with M4 as the signal path on a ground plane that consists of first and second metals M1 and M2 in parallel. Microstrip line MS1, and all of the S-CPWs and S-CPWG1 are designed in metals M4 and M3 for the signal and shield/ground, respectively. Finally, the CPW_REF is a low-loss 50-Ω CPW fabricated using thin film gold metal on an insulating alumina substrate (GGB CS-5). For S-CPWs with floating shields, the shield strip length (SL) and spacing (SS) are also shown in Table I.

A vector network analyzer (VNA) was used for on-wafer S-parameter measurement of the test lines. It was calibrated using the through-reflect-line (TRL) calibration method on an alumina calibration standard substrate (GGB CS-5). A TRL procedure using CPWs of two different lengths calibrates the VNA over a frequency ratio of 1:9 between the highest and lowest frequency in the calibration range. In order to cover a frequency range from 1 to 40 GHz (i.e., 1:40 ratio), the TRL calibration is split into two bands. The first band from 1 to 10 GHz was calibrated using 500-$\mu$m and 6550-$\mu$m long lines, and from 10 to 40 GHz 500-$\mu$m and 1450-$\mu$m line lengths were used. For the purpose of verification, the calibration was repeated using the short-open-load-through calibration method and standards (SOLT), which is suitable for measurement from very low frequencies (e.g., 40 MHz) up to about 15 GHz. Measured s-parameters of the transmission lines using TRL and SOLT calibrations are virtually identical from 1 to 15 GHz. Picoprobes Model 67A which are suitable for on-wafer measurement from DC up to 67 GHz were used for transmission lines characterization.

### *D. Measured Results of Conventional Microstrip, CPW Versus S-CPW*

Fig. 6 shows the $Z_o$ of selected microstrips, CPW, and S-CPWs in the experiment. To extract $Z_o$ of the test-lines on silicon, the effects of the probe-pad parasitics were first measured and removed from the s-parameters of 2000-$\mu$m-long test-lines [22], and then $Z_o$ was extracted from the de-embedded s-parameters [23]. For the CPW_REF line on an alumina substrate, the $Z_o$ was extracted from s-parameters of a 6550-$\mu$m-long CPW. The extraction method for $Z_o$ is inaccurate for frequencies at which the physical line length is close to multiples of a half-wavelength. However, the purpose of showing these results is to verify that the transmissions lines under test have a $Z_o$ near 50 Ω for fair comparison.

The performance of the transmission lines is characterized by the attenuation per millimeter length ($\alpha$, in dB/mm), relative dielectric constant ($\varepsilon_r$), and $Q$-factor. For each transmission line design, two lines of 500 $\mu$m and 2000 $\mu$m in length were measured, and the parameters $\alpha$, $\varepsilon_r$, and $Q$ were extracted from these two sets of s-parameters using a method similar to the TRL calibration procedure [24]. One advantage of this de-embedding method is that the parasitics of the probes and probe-pads do not need to be known or approximated by a lumped-element network. The accuracy of the de-embedding is only affected by the repeatability of the measurement. The measurement for the entire set of experimental transmission lines was repeated at least three times (i.e., with the VNA recalibrated) to ensure that there were no significant differences between the three sets of measurement. Only a representative set from these data is reproduced here.

Fig. 7 compares the relative dielectric constant ($\varepsilon_r$) of conventional transmission lines MS1, MS2, CPW1, and CPW2 against S-CPW1 and S-CPW2. The $\varepsilon_r$ of these conventional transmission lines is approximately 3 regardless of design (i.e., microstrip or CPW), or the use of a wider or narrower signal-to-ground gap. This is expected, because the surrounding media is silicon oxide ($\varepsilon_r = 4$) and air ($\varepsilon_r = 1$). Similarly, $\varepsilon_r$ of the CPW_REF on alumina is about 5.5, which is between the $\varepsilon_r$ of alumina (9.9) and air. Therefore, the effective $\varepsilon_r$ and wavelength of conventional transmission lines are determined by the surrounding dielectric media and it is not possible to alter it by making changes to the physical layout. By contrast,

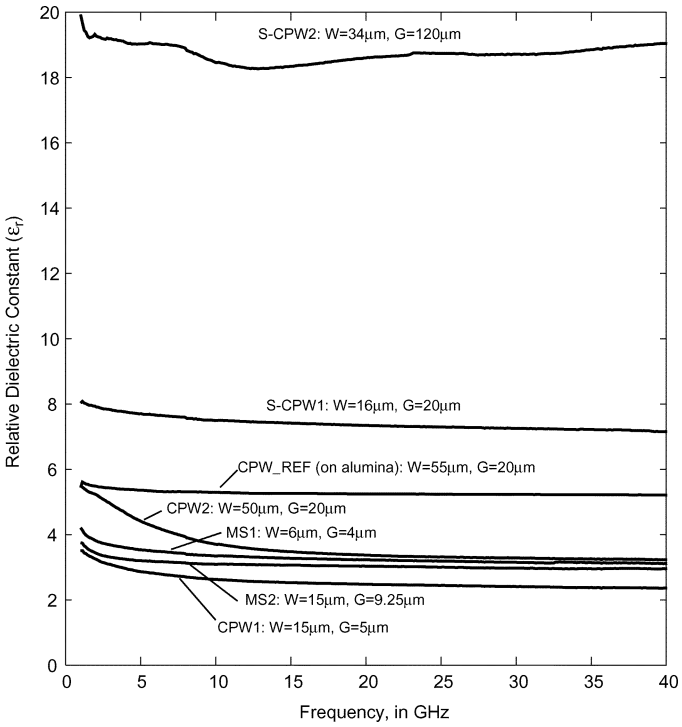


Fig. 7. Relative dielectric constants of microstrip, CPW, and S-CPW.

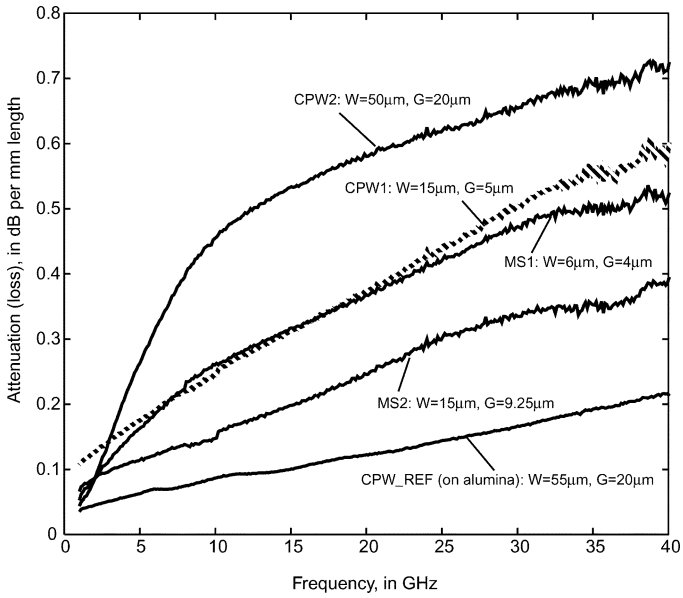


Fig. 8. Attenuation per unit length of CPW_REF on alumina, CPW and microstrip on silicon.

the $\varepsilon_r$ and wavelength of S-CPW are adjustable by changing the gap. With G $= 20$ $\mu$m, S-CPW1 has an $\varepsilon_r = 7.5$. When G is increased to 120 $\mu$m, S-CPW2 achieves $\varepsilon_r = 19$, which is about 6 times that of a conventional CPW transmission line on silicon. There is less than 5% variation in the measured $\varepsilon_r$ from 2 to 40 GHz. Since wavelength is inversely proportional to the $\sqrt{\varepsilon_r}$, the wavelength of S-CPW2 is reduced by a factor of 2.4 compared to conventional on-chip transmission lines. This reduction in wavelength allows a more compact implementation of transmission lines for impedance transformation and phase shifting applications. Furthermore, the adjustable wavelength gives some additional freedom to the circuit designer. For example, two S-CPWs of the same physical length can be designed with different phase shifts by adjusting the $\varepsilon_r$.

Fig. 8 compares the attenuation per unit length (in dB/mm) of CPW_REF on alumina and conventional microstrips and CPWs on silicon. CPW1 with a relatively narrow 5-$\mu$m signal-to-ground gap and 15-$\mu$m-wide signal trace has a loss of 0.4 dB/mm at 20 GHz. Increasing the gap to 20 $\mu$m allows the use of a wider signal path (W $= 50$ $\mu$m), giving one-third of the DC resistance. However, the loss at 20 GHz rises to 0.6 dB/mm because a wider gap permits more of the EM-field to leak into the substrate. Microstrip MS1 with a 4-$\mu$m gap and 6-$\mu$m signal width has similar performance as CPW1 with 5-$\mu$m gap. However, MS2 with a 9.25-$\mu$m gap allows a wider signal path of 15 $\mu$m, and it has only 0.25-dB/mm loss at 20 GHz. In general, CPW has higher loss than microstrip, because the gap surfaces where current crowding (due to skin effect) occurs are much narrower in CPW than in microstrip [18]. The reference line CPW_REF on alumina, which represents the best case performance, has an attenuation of only 0.12 dB/mm at 20 GHz.

Fig. 9 compares the quality factors of CPW_REF and conventional transmission lines. Conventional CPW1 with a narrow gap of 5 $\mu$m has about 40% higher quality factor compared to CPW2 with a (wider) gap of 20 $\mu$m (i.e., $Q = 7.8$ versus 5.5 at 20 GHz). This is expected because in the absence of an effective shield, wider gap CPW has more attenuation due to EM-field leakage. The opposite is observed for microstrips. MS2 with a 9.25-$\mu$m-thick dielectric has a $Q$ of 13 at 20 GHz, compared to a $Q$ of 9 for MS1 (4-$\mu$m-thick dielectric). Maximizing the oxide thickness by using the lowest metal level results in a ground plane with submicron thickness. In this experiment, the microstrip ground consists of a solid (i.e., unslotted) metal plane. It should be noted that slots are normally added to prevent dielectric stress cracks from forming.

Fig. 10 compares the attenuation per unit length (in dB/mm) of CPW_REF on alumina, S-CPWs and S-CPWG on silicon. S-CPW1 and S-CPW2 with 20-$\mu$m and 120-$\mu$m signal–ground gaps demonstrate attenuations of 0.25 and 0.2 dB/mm, respectively, at about 20 GHz. Therefore, not only does S-CPW have lower loss per unit length than conventional CPW, shielding results in a S-CPW with a 120-$\mu$m gap having attenuation comparable to a (narrower) 20-$\mu$m gap S-CPW. Consequently, circuit designers can freely adjust the gap of S-CPWs to select the proper wavelength.

Fig. 11 compares the quality factors of CPW_REF, S-CPW, and S-CPWG lines. At 20 GHz, S-CPW1 with a 20-$\mu$m gap has a $Q$ of 17. Increasing the gap to 120 $\mu$m permits higher energy storage per unit length (as indicted by its relative high $\varepsilon_r$ of 19 for S-CPW2 in Fig. 7) without an increased loss per unit length (refer to Fig. 10). As a result, S-CPW2 achieves a $Q$ of 33 at 20 GHz, which is comparable to the quality factor of the CPW_REF line on an insulating alumina substrate. The attenuation per degree of phase-shift and the loss per wavelength are inversely proportional to the quality factor of the transmission line. This implies that S-CPW delay lines (e.g., for

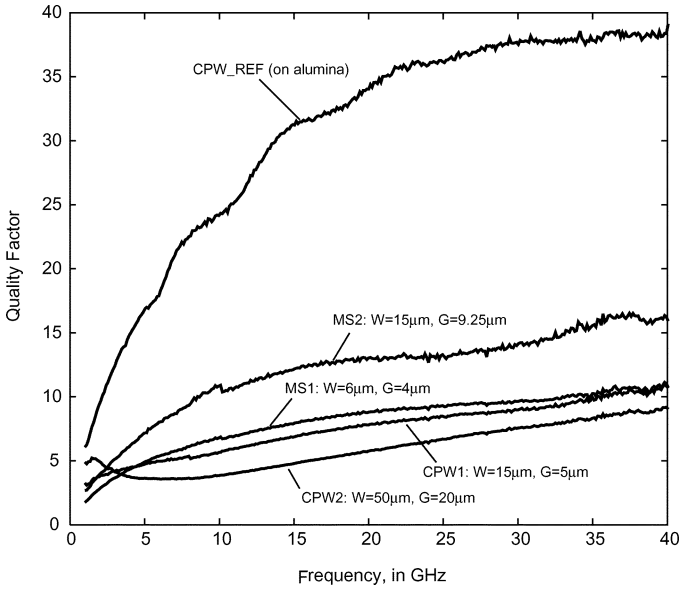


Fig. 9. Quality factors of CPW_REF on alumina, CPW, and microstrip on silicon.

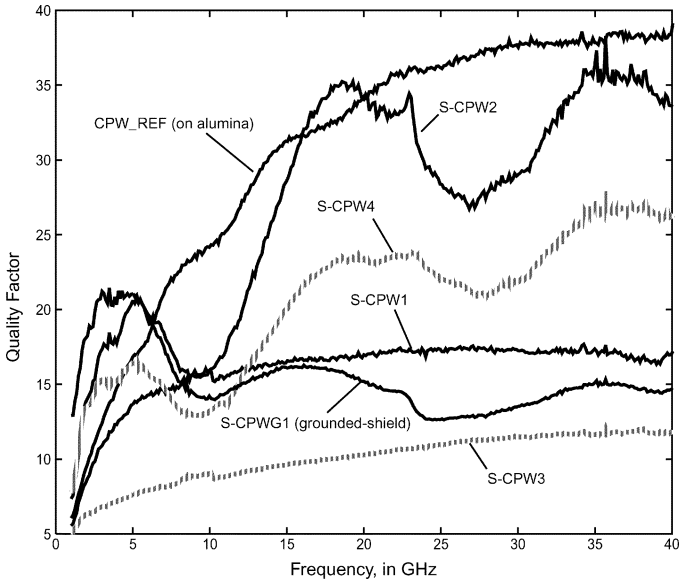


Fig. 11. Quality factors of CPW_REF on alumina, S-CPW, and S-CPWG on silicon.

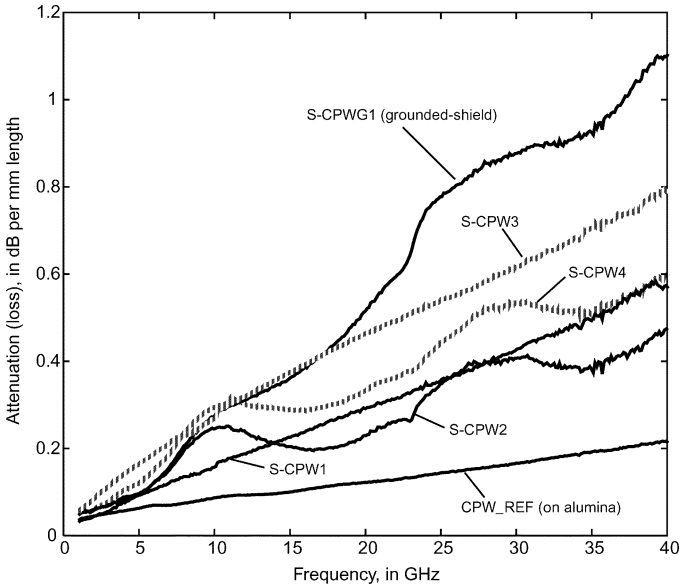


Fig. 10. Attenuation per unit length of CPW_REF on alumina, S-CPW, and S-CPWG on silicon.

phase-shifting), or an S-CPW quarter-wavelength impedance transformer will have less loss than the equivalent component designed using either conventional CPW or microstrip transmission lines on-chip by a factor of 2.5 to 6. Furthermore, the signal path width of the 50-$\Omega$ S-CPW2 (34 $\mu$m) has one-quarter to one-half the DC resistance of the 50-$\Omega$ microstrip lines (6-$\mu$m-wide MS1 and 15-$\mu$m-wide MS2). Interconnects with lower DC resistance are useful in high-current applications, such as power amplifiers.

### *E. Effect of Shield Length and Shield Spacing*

The floating shield strips for the S-CPW lines described in the previous section are designed using the minimal length and minimal spacing of 1.6 $\mu$m allowed by the technology. First, a minimal strip length (SL) suppresses induced current flow. This minimizes ohmic loss and the reduction of line inductance, thereby maximizing the reactive energy storage per unit length. Also, using the smallest shield strip spacing allowable minimizes the exposure of the overlying CPW to the conductive substrate.

Fig. 10 also compares the attenuation of S-CPWs having fine and coarse arrays of shield strips. For a 20-$\mu$m gap, S-CPW3 with a coarse shield length (SL) of 10 $\mu$m and shield spacing (SS) of 2 $\mu$m has 0.17 dB/mm higher loss above 20 GHz than S-CPW1, which has a fine array of closely spaced, short shield strips ($\mathrm{SL} = \mathrm{SS} = 1.6\ \mu\mathrm{m}$). Similarly, for a 120-$\mu$m gap, S-CPW4 with a relatively coarse shield ($\mathrm{SL} = 4\ \mu\mathrm{m}$, $\mathrm{SS} = 5\ \mu\mathrm{m}$) has 0.12 dB/mm higher loss above 20 GHz than S-CPW2, which has a fine shield strip array ($\mathrm{SL} = \mathrm{SS} = 1.6\ \mu\mathrm{m}$). As seen from Fig. 11, the coarse shield of S-CPW3 reduces its quality factor by almost a factor of two compared to S-CPW1, and the quality factor of S-CPW4 is over 30% lower than the finely shielded S-CPW2. Therefore, a floating shield made of narrow and finely spaced ($< 2\ \mu\mathrm{m}$) metal strips is required to maximize the performance of the transmission line up to 40 GHz.

### *F. S-CPW (Floating Shield) Versus S-CPWG (Grounded Shield)*

For the transmission line experiments reported here, the oxide thickness separating the CPW and the floating shield strips is 4 $\mu$m. Electric field from the signal path couples to the floating shield, and then from the shield back to the coplanar ground conductors on top. Therefore, the floating shield is a conduit for the electric field between signal and ground conductors that doubles the effective dielectric thickness between them (i.e., effectively 8 $\mu$m). When the shield strips are grounded (i.e., shield strips directly connected to the ground path using vias), the path for the electric field between signal and ground is reduced to 4 $\mu$m, which increases the line capacitance compared to S-CPW with a floating shield.

Furthermore, grounding the shield causes the voltage on the shield itself to fluctuate, as it is a part of the signal return path in a circuit. To quantify the benefit of floating versus grounded shield, S-CPWG1, a grounded shield version of S-CPW2, was fabricated. Both S-CPW2 and S-CPWG1 have signal-to-ground gaps of 120 $\mu$m, and minimum shield strip length and spacing of 1.6 $\mu$m. To accommodate the increase in line capacitance caused by grounding the shield, the signal width for S-CPWG1 is 26 $\mu$m for a $Z_o$ of 50 $\Omega$. Thus, both the floating and ground shielded S-CPWs in this experiment have equal characteristic impedances for comparison. The measured attenuation per unit length for S-CPW2 and S-CPWG1 are shown in Fig. 10. Below 10 GHz, there is no difference in attenuation between the transmission line with a floating shield and the grounded shield. However, loss of the ground-shielded S-CPWG1 is 0.3 dB/mm higher (at 20 GHz) and 0.6 dB/mm higher (at 40 GHz) than S-CPW2 with the floating shield. The results of Fig. 11 show that for frequencies above 15 GHz, S-CPW2 with a floating shield has more than double the quality factor of S-CPWG1.

### *G. Application Examples: S-CPW in Millimeter-Wave Silicon Power Amplifiers*

Broadband wireless networks in mm-wave frequencies such as the 24-GHz ISM band will reduce congestion in lower frequency bands, and supports data services up to hundreds of Mb/s, enabling 4G wireless access and connectivity. In mm-wave power amplifiers fabricated on semi-insulating GaAs substrates, quarter-wavelength transmission line transformers are often used for impedance matching. Although high quality microstrip and CPW lines are not available in silicon technologies, S-CPW offers a compact solution for this purpose. An example application of S-CPW is a low-loss impedance transformation to realize optimum loads (i.e., $R_{\rm opt}$) for maximum output power in an RF amplifier. A 24-GHz 14-dBm CMOS power amplifier uses (ground-shielded) S-CPWG as transmission line transformers for input, interstage, and output impedance matching [25]. However, the use of floating-shielded S-CPW is preferred to realize higher quality factor, lower loss, and a wider signal path for lowest DC resistance and reliability (e.g., failure caused by electromigration of metal).

Fig. 12 shows a linear integrated 21–26-GHz power amplifier (PA) with 125 mW (+21 dBm) output power using 1.8-V breakdown $(V_{\rm CEO})$, 100-GHz $f_T$ SiGe bipolar transistors [26]. Three stages of amplification (approximately 6-dB small-signal gain/stage) provide 15-dB gain at 1-dB gain compression per stage (i.e., large signal). The amplifier produces full power with a 6-dBm RF input. Interstage step-down transformers and on-chip input/output baluns optimize the gain in each stage. Slow-wave differentially shielded transmission lines connect the signals from the input balun to the first stage of differential amplifiers. The balanced excitation from the differential transmission lines preserves signal swing with minimal loss to the medium resistivity (10–15 $\Omega$·cm) substrate even at 24 GHz. This allows the use of a relatively wide gap (40 $\mu$m) between the differential pair to increase $\varepsilon_r$ (i.e., more compact length) and signal width, as discussed previously. Therefore, not only is substrate loss reduced, the wider path also increases the interconnect DC conductance and current rating, which is desirable for power amplifier reliability.

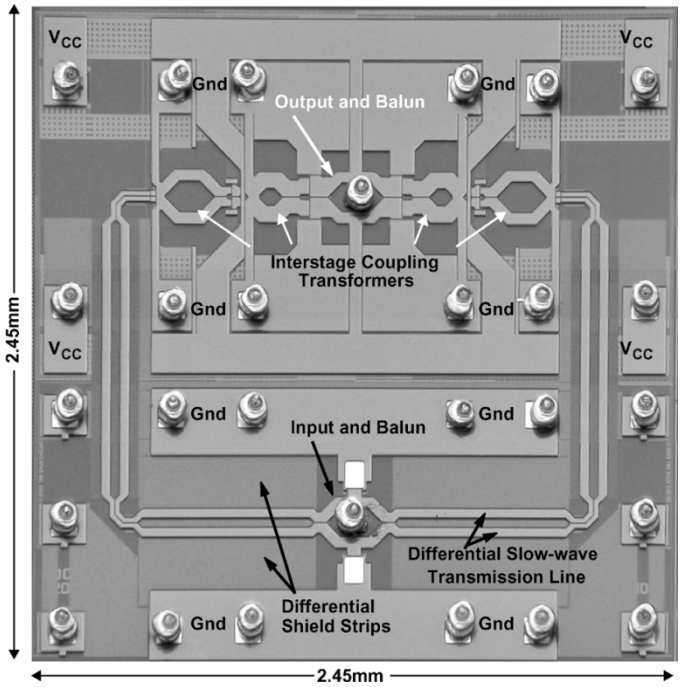


Fig. 12. A 24-GHz SiGe power amplifier with floating-shielded differential slow-wave transmission lines.

The application of floating shields in the magnetic components such as interstage transformers, baluns, and inductors will be discussed in the next section.

## IV. Differential Inductors and Transformers With Floating Shields

In the implementation of transceivers, voltage-controlled oscillators (VCOs) with low phase noise are needed for the generation of the carrier signal. For an $L$-$C$ type VCO which uses an inductor in parallel with a shunt capacitor to form a resonant tank, a high $Q$ of the tank circuit is crucial to minimize the phase noise of the VCO output [27]. Therefore, it is desirable to maximize the $Q$-factor of on-chip inductors and capacitors.

The $Q$-factor of inductors in mixed-signal VLSI technologies is primarily limited by losses in the silicon substrate and not in the conductor metals [28]. In general, dissipation is minimized when the passive component is constructed using a perfect dielectric material (i.e., an insulator with infinite resistivity) to allow fields to propagate without attenuation, and using perfect conductors (i.e., conductors with zero resistivity) to guide the EM-waves. A component made from imperfect dielectric materials can be improved by modifying the silicon substrate in some way [29], [30], or using a lower-$k$ intermetal dielectric [31], [32]. However, it is desirable to use a standard process flow to minimize costs, and these methods require processing steps, or materials which are atypical of production silicon technologies.

An alternative solution is the patterned ground shield placed between the inductor and the substrate [12], [33], [34]. The shield is constructed from metal, silicided polysilicon, or low-resistivity buried layers close to the silicon surface [35], [36]. An

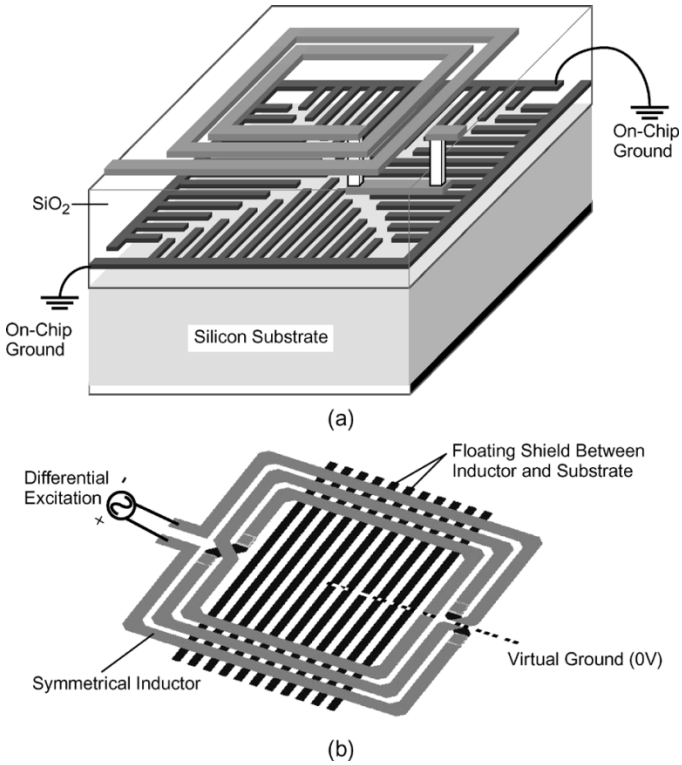


Fig. 13. Two substrate shielding methods for inductors. (a) Ground-shielded inductor. (b) Floating-shielded differential inductor.

illustration of an inductor with patterned ground shield is shown in Fig. 13(a). Shield fingers connected to the on-chip ground plane lie directly underneath the inductor winding to block the electric field from entering the silicon substrate. Since induced currents on the shield decrease the overall magnetic field, inductance and the inductor $Q$-factor, the shield fingers are designed and placed to minimize current flow caused by magnetic induction. However, due to parasitic inductance, there is no 0 V reference on a silicon chip where the shield can be grounded, as outlined in Section II. In addition, the ground plane may be affected by other circuit activity on the chip, which can couple interference to the inductor. Connecting the shields of many passive components together is also a source of unwanted signal coupling between circuits (e.g., between a VCO tank and the degeneration inductor of a low-noise amplifier).

Many of these implementation difficulties are avoided when a floating shield is used. Fig. 13(b) shows a symmetric inductor with a floating shield [16]. A differential voltage applied to the inductor winding (shaded) induces no net voltage onto the shield metal. This blocks capacitively coupled currents from entering the silicon substrate, thereby reducing substrate dissipation and improving the inductor $Q$-factor. It should be noted that an effective floating shield must be under equal and opposite electric field excitation from the passive component and its current-return path.

The floating shield has several advantages over the traditional ground shield. First, the floating shield does not need an explicit 0 V ground reference as discussed previously. Second, the floating shield is not connected to, and directly driven by, AC sources such as transistors. It shields a passive device by electric induction, and can even maintain 0 V on the shield at mm-wave frequencies. This is because the interconnect inductance between the shield and its 0 V reference is now minimized (i.e., virtual ground is at the center of the inductor). Moreover, the floating shields of different passive devices are not connected together, so isolation between devices is improved over grounded shields which are connected to a common on-chip ground. A floating shield which minimizes energy leaking from the differential inductor to the substrate will also block differential noise from the substrate coupling into the same inductor. Finally, the floating shield can be used to satisfy metal density requirements for fabrication. In advanced damascene interconnect processes, local regions of very high and very low metal pattern density are difficult to yield in manufacture. Therefore, metal is added to fill-in areas where there are a low density of metallization (e.g., inductor center). Prior research has shown that the metal fill lowers the inductor $Q$-factor because it adds parasitic capacitance as well as paths where currents induced by the magnetic field can flow, which dissipates energy [37]. However, this work shows that the metal fill can be arranged as floating shields to both aid circuit performance and satisfy stringent rules for manufacturability at the same time.

The floating shield is most effective when the shield strips have much lower inductance than the device being shielded (e.g., as in a multi-turn top-metal inductor winding). A floating shield (especially with submicron thickness) is more effective to block electric field by reflection like a mirror if it is made of metal (e.g., aluminum or copper) instead of a more resistive material (e.g., polysilicon). For example, prior research has studied the prospect of using a high-resistivity, floating polysilicon layer to mimic a high-resistivity substrate. However, the shielded 2-nH inductor yields a poorer $Q$-factor than its unshielded counterpart above 8 GHz [38]. Floating p/n junctions with isolation trenches to suppress eddy currents in the silicon substrate [39] have also been proposed. However, our simulations and subsequent measurements have shown that such currents are very small on medium resistivity (i.e., 10–20 $\Omega$·cm) silicon substrates. In addition, floating diffusions do not reduce EM-field induced losses, which depend upon the conductivity of the silicon substrate. Substrate losses may actually increase when isolation junctions are added, depending upon the dopant concentration of the diffusion.

### A. Floating-Shielded Differential Inductor Experiment

Differential inductors with three floating shielding patterns were fabricated and are illustrated in Fig. 14. The horseshoe pattern consists of U-shaped metal rings placed beneath each turn, with additional shielding strips adjacent to the outer and innermost turns. Note that there are no closed loops where magnetically induced currents may flow. Thus, the addition of the shield metal does not affect the inductance. The outer-most turn of the inductor has the highest voltage swing and requires maximum shielding. Therefore, a relatively fine shield strip spacing of 1 $\mu$m is used near the outer-most turn, and the spacing gradually increases to 8 $\mu$m at the inner-most turn. The mesh pattern of Fig. 14(b) is comprised of horizontal and vertical strips that span the length and width of the inductor. Induced current is inhibited by placing the strips orthogonal

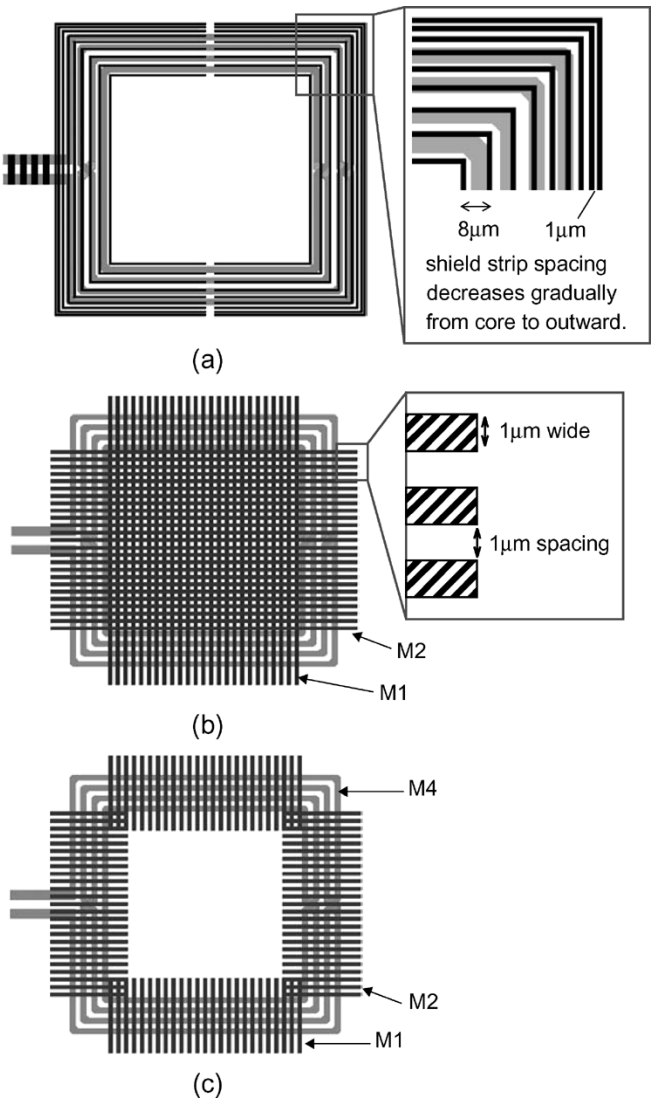


Fig. 14. Floating shield patterns for differential inductors (bottom view). (a) Horseshoe. (b) Mesh. (c) Ladder.

to the inductor winding. The third metal pattern is the ladder shield of Fig. 14(c). Here, short horizontal and vertical metal strips shield the electric field from the substrate. The strips are placed directly beneath each group of conductors on each side of the winding. As there is a phase shift along the coil length, the net potential induced onto each shield strip is not zero, but it diminishes as the number of top metal turns for the inductor increases. A constant spacing of 1 $\mu$m between shield strips is used for the mesh and ladder patterned shields. The width of the shield strips for all the shielded inductors is 1 $\mu$m, which is near the minimum width allowed by the technology to suppress induced current flowing on the shield. For the purposes of comparison, an inductor without any shielding was also fabricated. All four inductors (i.e., three shielded and the unshielded baseline) have the same square winding with a conductor width of 6 $\mu$m and spacing of 5 $\mu$m. Each inductor has four turns and an outer dimension of 275 $\times$ 275 $\mu$m. The inputs are connected to test-pads for on-wafer probing in the ground–signal–ground configuration over a copper ground plane.

All of the inductors were fabricated using the aluminum-copper [Fig. 4(a)] and all-copper processes [Fig. 4(b)]. Both 10 $\Omega$·cm and 500 $\Omega$·cm resistivity substrates were used to fabricate test inductors with each interconnect metal scheme. The two upper-level metals (i.e., M4 and M3) form the coil winding and underpass layers, respectively. The bottom two (copper) layers implement the metal shielding patterns for all inductors.

### *B. $Q$-Factor and Self-Resonant Frequency Extraction*

The $Q$-factor is determined from a differential one-port impedance measurement of the $L$-$C$ resonant tank. The impedance of the tank reaches its maximum value $(\mathrm{Z_{max}})$ at resonant frequency, $f_o$. The tank $Q$-factor at $f_o$ is defined by the ratio of $f_o$ to the $-3$-dB bandwidth $f_{-3\mathrm{dB}}$ [40], where $f_{-3\mathrm{dB}}$ bounds the impedance above $0.707 \cdot \mathrm{Z_{max}}$. Parasitic effects from the probe pads and pad-to-inductor interconnect may be removed from the measurement using a well-known de-embedding procedure [22]. In this work, only the shunt parasitics are removed by y-parameter de-embedding from the measured s-parameters of the inductor. The series parasitics (due to probe contact and a short section of interconnect metal) are dominated by a parastic resistance (a fraction of an Ohm) and inductance (100–200 pH) that is small compared to the 7.5-nH test inductors. These parasitics were not de-embedded from the measured data. Consequently, the de-embedded $Q$-factors are slightly pessimistic, however, over-estimation of the $Q$-factor due to z-parameter de-embedding is avoided.

The de-embedded two-port s-parameters were then used to compute the one-port differential impedance of the inductor. An ideal capacitor $(C_{\mathrm{tank}})$ added in parallel with this impedance defines a resonant tank. Parameters $\mathrm{Z_{max}}$, $f_o$, $f_{-3\ \mathrm{dB}}$, and the $Q$-factor at $f_o$ are then calculated. By sweeping over a range of values for $C_{\mathrm{tank}}$, a plot of the $Q$-factor versus frequency is obtained.

With no capacitor added in parallel, $f_o$ reaches its largest value called the inductor's self-resonant frequency (SRF). For frequencies above the SRF, the inductor becomes capacitive and it is not usable in a tank. Therefore, a high SRF for an inductor is desirable to maximize the tunable frequency range of the resonator for VCO applications. Picoprobe Model 40A and a Wiltron 360B network analyzer calibrated to the probe tips using the SOLT method were used for measurement.

### *C. Inductor Measurement and Simulation Results*

In order to compare the consistency and quality of the probe contact for each measurement, the real part of differential one-port impedance (i.e., $\mathrm{Re}[\mathrm{differential} - Z_{11}]$) for the unshielded and three floating-shielded inductors on a 10 $\Omega$·cm substrate is plotted in Fig. 15. At frequencies below a few hundreds of megahertz, $\mathrm{Re}[\mathrm{diff} - Z_{11}]$ is dominated by the conductor resistance of the inductor and the probe contact resistance. The z-parameters plotted in Fig. 15 are derived directly from raw s-parameter data measured on a vector network analyzer (i.e., no de-embedding). At frequencies near 100 MHz, the measured resistances (i.e., real part of $\mathrm{Z_{11}}$) for all four copper inductors are 6.05 $\pm$ 0.15 $\Omega$ (i.e., $\pm$2.5%), verifying a consistent and repeatable RF probe contact (which is estimated at about

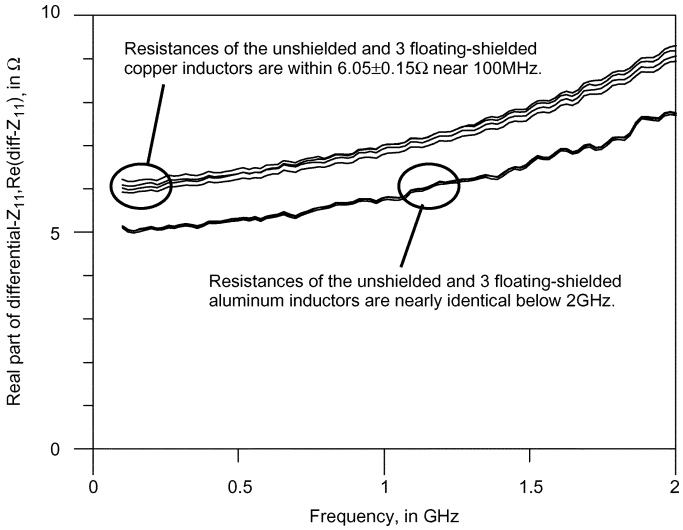


Fig. 15. Measured differential $Z_{11}$ of of the experimental inductors on a 10 Ω·cm substrate (before y-parameter de-embedding).

TABLE II
INDUCTOR MEASUREMENT SUMMARY, Cu AND (Al)

| Measurement (10Ω·cm substrate) | Unshielded | Horseshoe | Mesh | Ladder |
|---|---|---|---|---|
| Inductance, in nH | 7.72 (7.45) | 7.78 (7.40) | 7.78 (7.35) | 7.79 (7.36) |
| Self-resonant frequency (SRF), in GHz | 8.43 (9.45) | 8.21 (9.26) | 8.23 (9.31) | 8.33 (9.42) |
| Peak impedance, in kΩ | 6.6 (7.9) | 9.7 (11.6) | 9.3 (11.7) | 7.7 (9.4) |

0.2–0.3 Ω/contact) between measurements of the different devices. Results for the aluminum inductors also showed a very consistent probe contact.

Parameters extracted from the de-embedded measurement for the unshielded and the 3 floating-shielded inductors (10 Ω·cm substrate) fabricated in all-copper and aluminum/copper technologies (as in Fig. 4) are compared in Table II. The inductance value is 7.5 nH (designed), which agrees well with the measured low frequency inductances of 7.8 and 7.4 nH for the copper and aluminum inductors, respectively. The difference is due to thicker aluminum top metal in the mixed Al/Cu process. The parasitics of the floating differential shield lower the self-resonant frequency of the inductor by less than 3% (e.g., 8.21 GHz versus 8.43 GHz for horseshoe and unshielded all-copper inductors). There is less than 2% difference in the inductance between shielded and unshielded inductors, indicating that the effect of current induced in the shielding strips from the coil's magnetic field is negligible. The data show that the addition of a floating differential shield does not diminish the useful frequency range or the inductance value.

The $Q$-factors determined from s-parameter measurement and de-embedding are illustrated in Fig. 16 and Fig. 17 for both copper and aluminum inductors on 10 and 500 Ω·cm wafers. Fig. 16 shows that on a 10 Ω·cm substrate, floating differential shielding improves the $Q$-factor by 30% for the copper and 35% for aluminum inductors. The horseshoe and mesh shields are more effective than the ladder pattern, despite the longer

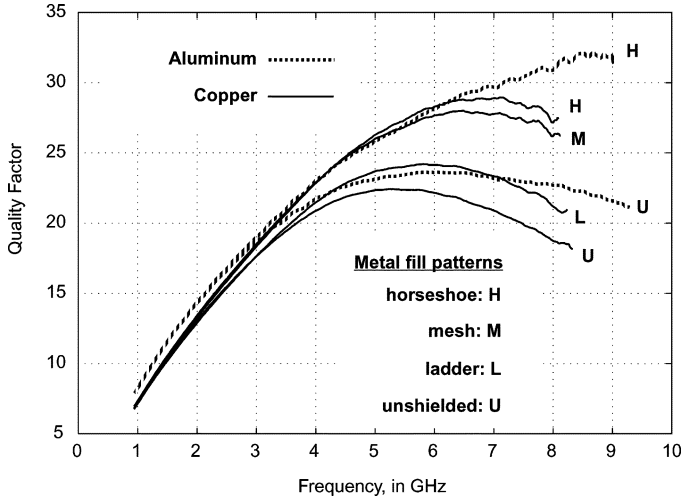


Fig. 16. Measured $Q$-factors of floating-shielded inductors on a 10 Ω·cm substrate.

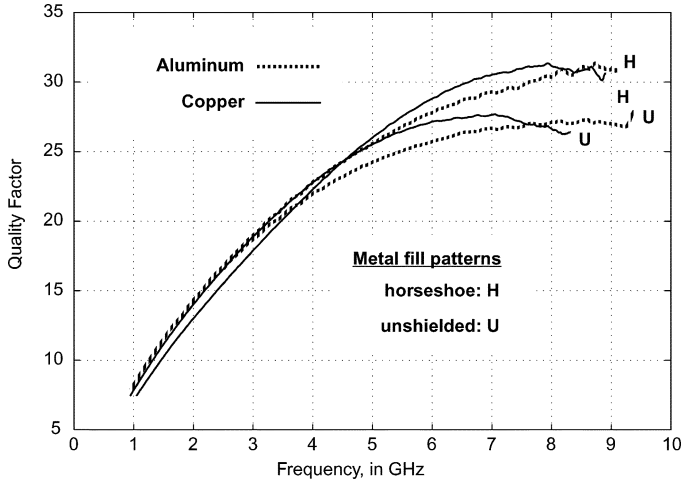


Fig. 17. Measured $Q$-factors of floating-shielded inductors on a 500 Ω·cm substrate.

metal strips used (i.e., for H and M patterns). This suggests that effective floating shielding requires that the metal strips link both sides of the coil winding (i.e., where the potentials are identical in magnitude but opposite in phase) as in the horseshoe and mesh shielded designs. On 500 Ω·cm material (Fig. 17), floating differential shielding also improves the inductor $Q$ by 13% compared to the unshielded design. The experiment also shows that floating shielded inductors (with the horseshoe or mesh patterns) on a 10 Ω·cm substrate have slightly higher $Q$-factors than the unshielded inductor on a 500 Ω·cm substrate (i.e., with 50 times higher resistivity).

Table III compares the performance of the floating-shielded inductor (this work) to the patterned ground-shielded inductor published in a previous study [12]. Both inductors have 7.4-nH inductance and they are fabricated on silicon substrate of about 10 Ω·cm resistivity. The technology used in this work has about twice the dielectric thickness (9.25 $\mu$m versus 5.6 $\mu$m) and metal thickness (4 $\mu$m versus 2 $\mu$m) of the technology for the ground-shielded inductor. The ground-shielded inductor was designed for single-ended usage, whereas the floating-shielded

TABLE III
COMPARISON OF GROUNDED SHIELD AND FLOATING-SHIELDED INDUCTORS

| Parameter | Patterned Ground Shield Single-ended Inductor [12] | Floating-Shielded Differential Inductor (This Work) |
|---|---|---|
| Substrate | 11Ω·cm silicon | 10Ω·cm silicon |
| Metallization | 2μm thick aluminum | 4μm thick aluminum |
| $SiO_2$ thickness | 5.6μm | 11μm |
| Shield to top metal | 5.2μm | 9.25μm |
| Inductance | 7.4nH | 7.4nH |
| Quality factor (bandpass definition) | 10.2 | 30 |
| Self-resonant frequency (unshielded) | 3.6GHz (6.8GHz) | 9.26GHz (9.45GHz) |
| Impedance at resonance | 1.5 kΩ | 11.6 kΩ |

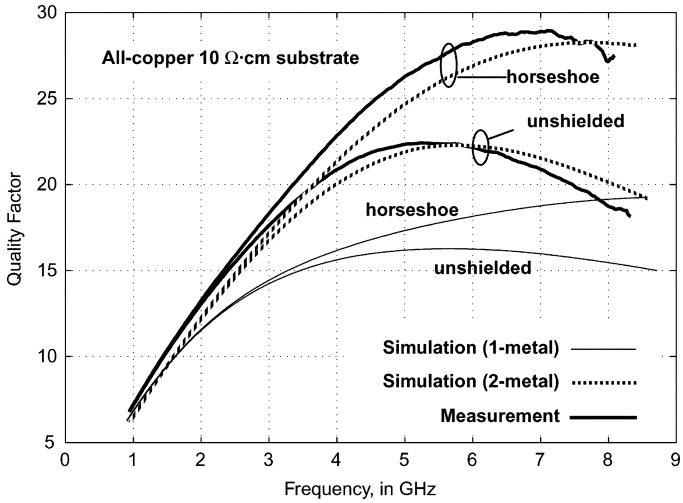


Fig. 18. Numerical simulation versus measurement.

inductor was driven differentially. Differentially driven unshielded symmetric inductors have demonstrated 50% higher $Q$-factor over single-ended unshielded inductors [41]. Given these differences, the floating-shielded inductor has a $Q$-factor that is about 3 times of the ground-shielded inductor (i.e., $Q$-factors of 10.2 versus 32, compared using the same $Q$-factor definition). Furthermore, the grounded shield lowers the SRF by 47% (i.e., from 6.8 to 3.6 GHz), and therefore significantly reduces the usable frequency range of the inductor. By contrast, the floating shield causes less than 3% reduction in the SRF. At resonance, the peak impedance of the floating-shielded inductor is over 7 times of the ground-shielded inductor (i.e., 11.6 kΩ versus 1.5 kΩ).

To verify the benefits of the floating shields, the inductors were also simulated using Agilent's Momentum, a commercially available 2.5D method-of-moments simulator. The simulated $Q$-factors of the unshielded copper inductor and the horseshoe-shielded copper inductor on a 10 Ω·cm substrate are compared with the measurement in Fig. 18. Normally only one metal layer would be used to represent the 2.3-$\mu$m first metal in the simulation. However, as seen in Fig. 18, there is a large discrepancy between simulation and the measurement. This is because the simulator assumes the metal layer to be infinitely thin, but in reality the inductors have 2.3-$\mu$m-thick metals that are closely coupled (5-$\mu$m spacing), so the line-to-line capacitance is underestimated. The simulation agrees with measurement (within 10% error) when two layers are used in simulation to represent the top and bottom surfaces of the 2.3-$\mu$m first metal.

### D. Inductor Compact Circuit Model

Inductors have a broad range of applications in RF circuits, ranging from oscillator tanks to amplifier load and matching networks. The circuit model for time-domain circuit simulation consists of time-invariant lumped elements that capture the inductor's electrical behavior over the usable frequency range (i.e, from DC up to the self-resonant frequency) with sufficient accuracy. Accurate use of the inductor in a matching network (typically low-$Q$) requires an accurate inductance value. Using the inductor in parallel with a capacitor as the resonant tank of a VCO requires the model to reflect the quality-factor, resonant-frequency and tank impedance in order to predict the frequency range, output amplitude, and phase noise from simulation.

Fig. 19(a) shows an inductor circuit model which is based on the physical layout of the inductor. When the inductor is driven differentially, the windings between adjacent turns have opposing voltage polarity, causing electric field leakage into the substrate. To account for this distributed loss, substrate loss networks "Si" are included in the compact model of Fig. 19(a). The substrate loss networks represent the parasitics coupling between adjacent metal traces in each turn of a symmetric inductor layout. Fig. 19(b) shows the equivalent circuit of each substrate loss network, which consists of four capacitors and two resistors: $C_{\rm ox}$, $C_{\rm c}$, $C_{\rm si}$, $R_{\rm si}$, $R_{\rm cm}$ and $C_{\rm cm}$. Although either the T [Fig. 19(b)] or $\pi$-model [Fig. 19(c)] can be used, the T-model has advantages over the $\pi$-model when extracting the element parameters from a numerical simulation or measurement. Since the inductor is driven differentially, fitting accuracy of the model parameters to simulation or measured data for differential excitation takes precedence over common-mode excitation. In the T-model, the lumped elements are divided into differential-mode elements $C_{\rm si}$, $R_{\rm si}$, $C_{\rm ox}$, $C_{\rm c}$, and common-mode elements $R_{\rm cm}$ and $C_{\rm cm}$. By contrast, all six lumped elements are involved for differential-mode excitation in the $\pi$-model, making it more difficult to isolate and extract each parameter accurately.

Parameter extraction for the T-model can be divided into four steps. First, the low-frequency series inductance $L$ and series resistance $R$ (in Fig. 19) are estimated from the measured s-parameters at relatively low frequency (e.g., below 2 GHz). Next, $C_{\rm si}$, $R_{\rm si}$, $C_{\rm ox}$, and $C_{\rm c}$ are fit to the differential s-parameters data (i.e., $\rm S_{11} - S_{21}$), because these parameters are largely unaffected by the common-mode elements. Common-mode parameters $R_{\rm cm}$ and $C_{\rm cm}$ can then be determined from the common-mode s-parameters (i.e., $\rm S_{11} + S_{21}$), with all other elements fixed. Finally, all elements are fine-tuned to fit the measured s-parameters. Fitting the differential parameters first, followed by the common-mode parameters, results in a parameter set that

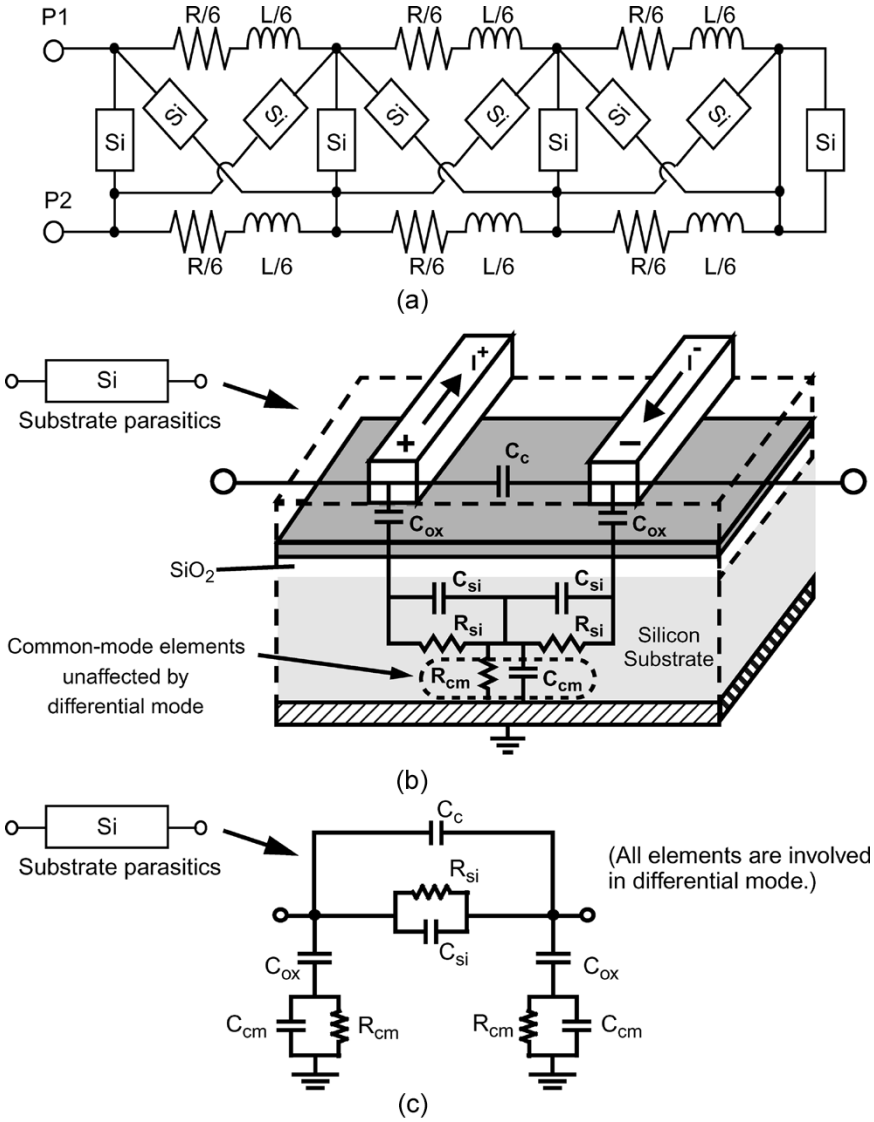


Fig. 19. Inductor compact model. (a) Inductor model schematic. (b) T-model for substrate parasitics. (c) $\pi$-model for substrate parasitics.

is most accurate for differential operation. The model parameters in this work were extracted using Agilent's Advanced Design System (ADS) software.

Fig. 20 compares s-parameters from a simulation of the compact model with parameters determined according to this parameter extraction procedure, and the measurement data of copper inductor shielded with horse-shoe pattern. The simulated and measured $S_{11}$, $S_{21}$ are in good agreement from 0 to 10 GHz, which is the entire usable frequency range. Fig. 21(a) shows that inductance and differential impedance $Z_{11}$ of the model accurately fit the measured data from 0 to 6 GHz. Fig. 21(b) shows that from 0 to 10 GHz the differential $Z_{11}$ increases rapidly up to a peak of 10 k$\Omega$ at resonance, and its value is accurately captured by the compact model.

It should be noted that at gigahertz frequencies, current crowding due to the skin-effect increases the resistance of the conductors, and (in general) this loss should be included in the models of passive components. However, in the inductor compact model (i.e., Fig. 19), no lumped-elements are dedicated to the modeling of skin effect, yet the compact model remains an accurate description of the inductor's measured electrical characteristics.

The loss of a high impedance transmission line inductor is more susceptible to loss due to shunt capacitance and resistance of the silicon substrate than the parasitic series resistance. Accuracy of the model increases as more lumped element sections are added, however, this also increases simulation time when the model is used in a circuit simulation. Therefore, the model should have enough sections to capture the most important and rapidly changing characteristics of the component. Six L-C sections are used to model the distributed (e.g., transmission line) effects. Each section models approximately 8.3% of a wavelength (i.e., half-wavelength divided by six sections) and the associated substrate loss. In practice, more sections can be added if a more accurate fit to the data is required. A six-section inductor compact model (Fig. 19) simultaneously captures the s-parameters, inductance, differential input impedance $Z_{11}$, self-resonant frequency (where $|Z_{11}|$ is at maximum), and $Q$-factor with ex-

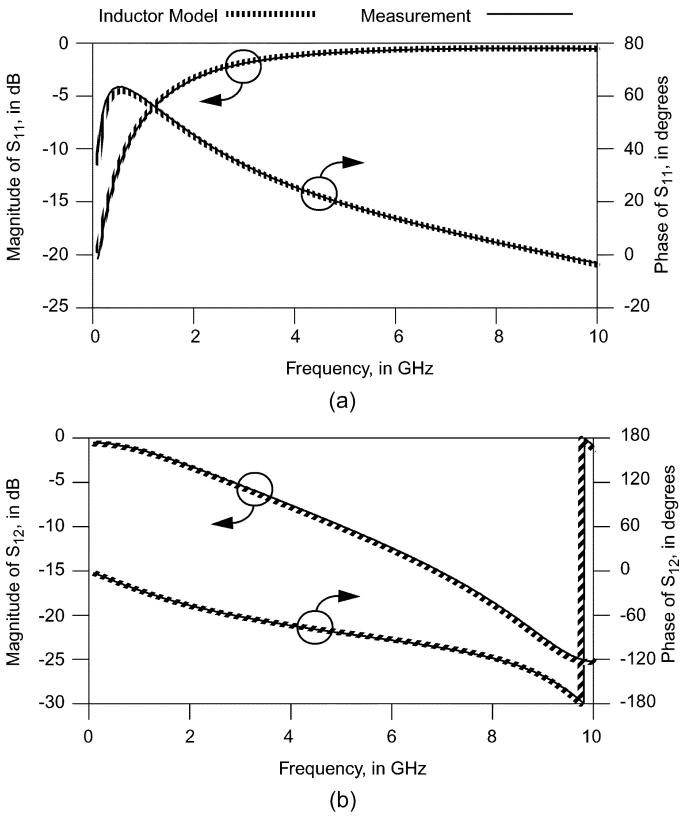


Fig. 20. S-parameters of horseshoe-shielded inductor compact model and measurement. (a) $S_{11}$ (same as $S_{22}$). (b) $S_{12}$ (same as $S_{21}$).

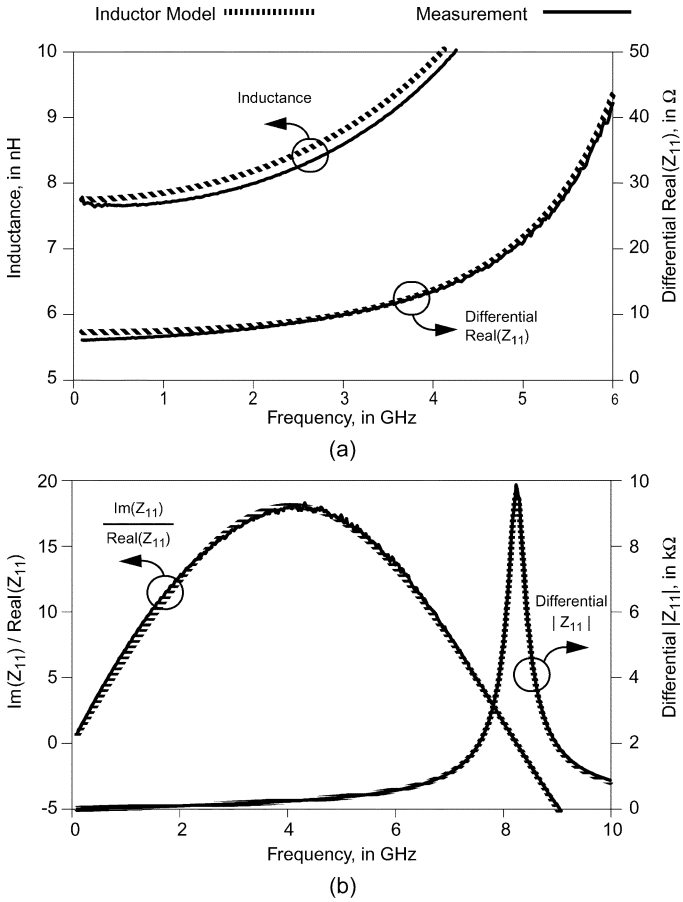


Fig. 21. Inductance and $Z_{11}$ of horseshoe-shielded inductor compact model and measurement. (a) Inductance and differential $\mathrm{Real}(Z_{11})$ from 0 to 6 GHz; (b) differential $|Z_{11}|$ and $\mathrm{Im}(Z_{11})/\mathrm{Real}(Z_{11})$ from 0 to 10 GHz.

cellent accuracy (maximum 8% error, from 1 to 9 GHz). Note that all of these parameters are important to circuit simulation accuracy, and that they are also very sensitive to minor variations in the s-parameters.

The model parameters for the unshielded baseline copper inductor and the horseshoe-shielded copper inductor on 10 Ω·cm wafers are compared in Table IV. Although the floating shield does not reduce the extracted resistances, it doubles capacitance $C_{\mathrm{si}}$, which shunts current away from resistor $R_{\mathrm{si}}$. This lowers the substrate loss as the frequency increases. As confirmed by experiment, the $Q$-factor of the shielded inductor is higher than the unshielded inductor, and it also reaches its maximum value at a higher frequency.

TABLE IV
UNSHIELDED AND HORSESHOE PATTERN FLOATING-SHIELDED INDUCTOR MODEL PARAMETERS

| Shield Pattern | L (nH) | R (Ω) | $C_c$ (fF) | $C_{ox}$ (fF) | $R_{si}$ (kΩ) | $C_{si}$ (fF) | $R_{cm}$ (Ω) | $C_{cm}$ (fF) |
|---|---|---|---|---|---|---|---|---|
| Unshielded | 7.75 | 7.3 | 3.92 | 9 | 0.55 | 35 | 2k | 9 |
| Horseshoe | 7.75 | 7.3 | 4.5 | 9 | 0.6 | 70 | 2k | 9 |

### *E. Floating-Shielded Transformer*

Similarly, a floating shield can also be applied to a monolithic transformer. As an example, Fig. 22 shows a floating-shielded transformer balun that combines the output from two pairs of differential amplifiers to drive a single-ended 50-Ω output. At 24 GHz, it achieves a measured 1.5-dB insertion loss (including loss of the probe-pad contact and 290-$\mu$m-long differential interconnect at each of the differential input, but without tuning capacitors) [42]. This transformer balun is similar to the output power-combining balun used in the 24-GHz SiGe power amplifier shown in Fig. 12.

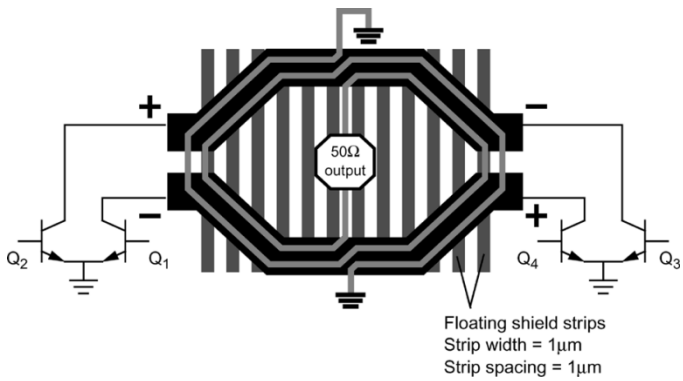


Fig. 22. Floating-shielded power combining balun.

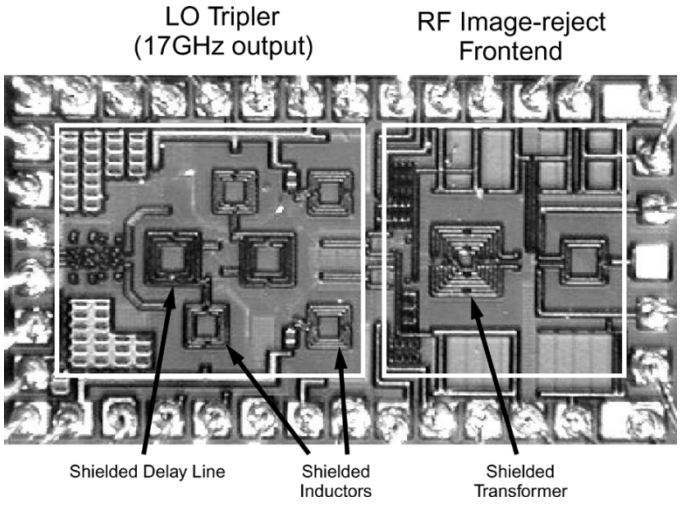


Fig. 23. A 17-GHz image-reject WLAN receiver front-end with floating-shielded transformer, inductors and delay lines [43].

### *F. Application Examples of Floating-Shielded Magnetic Components*

Fig. 23 shows a 17-GHz receiver which uses floating-shielded passive devices extensively [43]. It includes a low-noise amplifier (LNA) and two mixers coupled by a step-down transformer. A quadrature local oscillator (LO) generator allows the image rejection of the downconverter to be optimized by adjusting the phase of the LOs generated by a subharmonically injection-locked oscillator incorporating on-chip passive delay lines. Differential inductors are used as loads for gain stages in the LO and also as degeneration for the LNA. All of the delay lines, inductors and the transformer on the 17-GHz receiver MMIC are shielded using the ladder patterned floating shield, which enables improved RF performance without requiring higher power consumption. Over 50 dB of image-rejection at 70-MHz IF, 15-dB power gain from RF-IF, 6.5-dB single-sideband noise figure (50 $\Omega$) and $-5.1$-dBm $\text{IIP}_3$ were demonstrated in a production 100 GHz $f_T$ SiGe BiCMOS technology. The testchip consumes a total of 62.5 mW from a 2.2-V supply.

## V. Capacitors and I/O Bondpads With a Floating Shield

The floating shield can also be applied to other passives, such as on-chip metal–insulator–metal (MIM) capacitors, and input/output bondpads. Fig. 24 shows floating-shielded capacitors in series and parallel arrangements. For the series design [Fig. 24(a)], the capacitor top plate is divided into two parts which are connected to the transmission lines, and a single bottom plate can be used as a floating shield. Effectively, the capacitor is divided into two parts in series, and the symmetry of the capacitor ensures that the floating bottom plate is near 0 V to act as a shield when it is driven by a balanced (differential) signal. For applications that do not permit a floating capacitor plate, two capacitors connected in parallel to a differential signal line [as in Fig. 24(b)] implement a capacitor with balanced parasitics. A floating shield (using a lower level metal) added underneath the MIM capacitors will then minimize loss

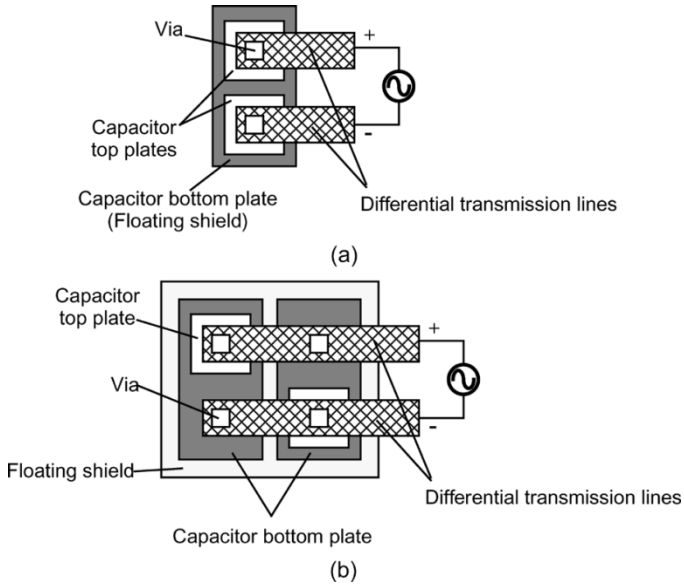


Fig. 24. Floating-shielded differentially driven capacitors. (a) Floating-shielded capacitors in series arrangement. (b) Floating-shielded capacitors in parallel arrangement.

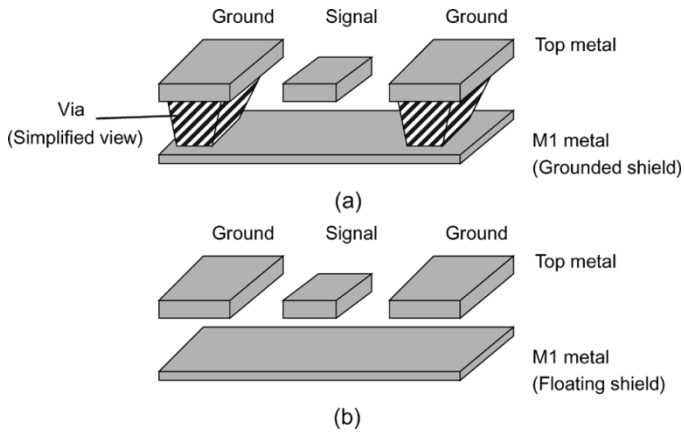


Fig. 25. Ground-shielded and floating-shielded bondpads. (a) Ground-shielded bondpads. (b) Floating-shielded bondpads.

caused by electric field coupling from the capacitor to the substrate.

Traditionally, input and output bondpads are shielded by placing a ground plane beneath them [Fig. 25(a)] [44]–[46], but there are several advantages to use the floating shield instead [as shown in Fig. 25(b)]. The shunt parasitic capacitance of a bondpad and the series bondwire inductance together form an $L$-$C$ low-pass network to the circuit. The floating shield effectively doubles the dielectric thickness between the ground and the signal path to reduce the pad capacitance. Simple ground–signal–ground (GSG) pads with grounded shield and floating shield were fabricated for experimental comparison. Both bondpads were made with top metal (M4), the shield in the form of a solid metal plane was made using the lowest level metal (M1). The size of the signal pad is 50 $\mu$m $\times$ 70 $\mu$m, and each ground pad is 120 $\mu$m $\times$ 160 $\mu$m. The distance between the centers of the adjacent pads is 150 $\mu$m. Cascade Infinity Probes (40-GHz version) and Wiltron 360B network analyzer

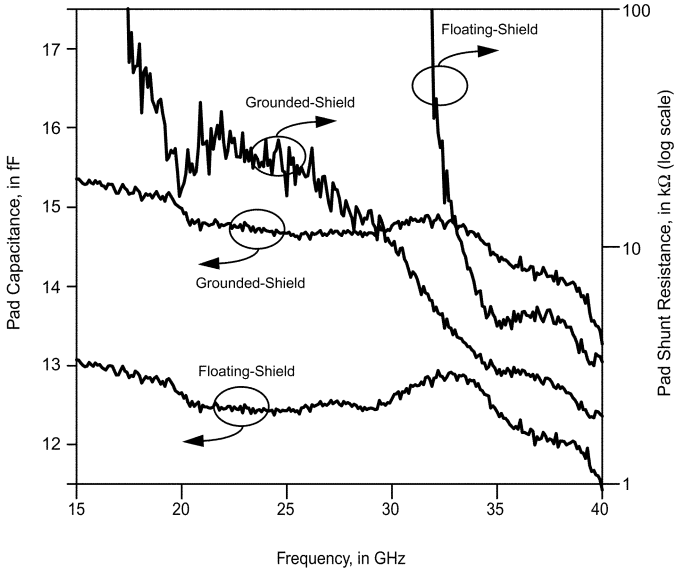


Fig. 26. Capacitance and resistance of ground–signal–ground pads with floating shield and grounded shield.

calibrated with the TRL method were used for measurement. Fig. 26 shows that the bondpad with grounded shield has 15-fF shunt capacitance, which is about 17% higher than the 12.8-fF capacitance of the bondpad with floating shield. The loss of the bondpad is measured by extracting the equivalent shunt resistance, which is also shown in Fig. 26. The shunt resistance of the pad with floating shield is nonmeasurable below 30 GHz, and from 30 to 40 GHz, it is at least 60% higher than the shunt resistance of the ground-shielded bondpad.

## VI. Conclusion

Successful demonstration of SiGe and CMOS implementations at mm-wave frequencies is opening up new product avenues, such as wireless personal-area networking. Recent development of 100–200-GHz technologies requires low-loss passive components to bring high-performance microwave and mm-wave applications within reach. This paper presented the floating shield technique that minimizes the loss of passives on the silicon substrate. By using floating metals to link equally opposing electric field emitting from the passive component and its current-return path, the floating shield stays at 0 V without an explicit ground reference. This overcomes the difficulty of designing a 0 V (explicitly) grounded shield on silicon MMIC. Floating shields for passive devices are physically separated and thereby also minimize unwanted coupling between devices. The floating shield technique is applicable to a broad range of commonly used passive components. Experiments on 10 $\Omega$·cm silicon substrate show that from 15 to 40 GHz, a 50-$\Omega$ S-CPW with floating shield and 120-$\mu$m signal-to-ground gap achieves $Q$-factors ranging 25 to 35, which is over 2 times the $Q$-factors of conventional 50-$\Omega$ microstrips, CPW, and ground-shielded S-CPWG. The S-CPW has 34-$\mu$m-wide signal and 50% lower DC resistance compared to 15-$\mu$m-wide CPW and microstrip. Unlike conventional transmission lines with a fixed on-chip wavelength, the wavelength of S-CPW is adjustable by circuit designers. Applying the floating shield to a 7.4-nH differential inductor improves the resonant $Q$-factor from 23.5 for the unshielded to 32 (i.e., >35% improvement) with negligible reduction in the self-resonant frequency. Floating-shielded ground–signal–ground bondpads have unmeasurable loss below 30 GHz, and 15% lower capacitance than its ground-shielded version. Selected application examples of floating-shielded passives in 24-GHz power amplifiers and a 17-GHz receiver fabricated in silicon-based technologies were summarized in the paper.

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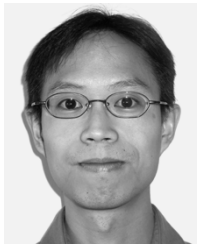

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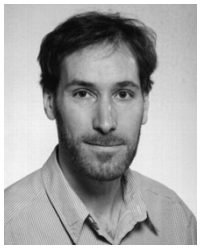

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