A Single–Chip 10-Band WCDMA/HSDPA 4-Band GSM/EDGE SAW-less CMOS Receiver With DigRF 3G Interface and +90 dBm IIP2

Daniel Kaczman, *Member, IEEE*, Manish Shah, *Member, IEEE*, Mohammed Alam, *Member, IEEE*, Mohammed Rachedine, *Member, IEEE*, David Cashen, *Member, IEEE*, Lu Han, *Member, IEEE*, and Anand Raghavan, *Member, IEEE*

***Abstract*—This paper describes the design and performance of a 90 nm CMOS SAW-less receiver with DigRF interface that supports 10 WCDMA bands (I, II, III, IV, V, VI, VIII, IX, X, XI) and 4 GSM bands (GSM850, EGSM900, DCS1800, PCS1900). The receiver is part of a single-chip SAW-less transceiver reference platform IC for mass-market smartphones, which has been designed to meet Category 10 HSDPA (High Speed Downlink Packet Access) requirements. The novel receiver core consists of a single-stage transconductance amplifier (TCA) with large gain control range, a current commutating passive mixer enhanced for automatic on chip IIP2 calibration with 25% duty-cycle LO injection and threshold adjust, and current-input complex Direct Coupled Filter (DCF). The low noise TCAs are designed without inductive loads to save area. A self-contained on chip automatic IIP2 calibration system with algorithm routine, implemented in firmware, is used to optimize IIP2 performance. This topology eliminates the external LNA, inter-stage SAW filter and transimpedance amplifier (TZA) in conventional WCDMA designs and results in current drain and die area savings as well as improved noise. The 25% duty-cycle LO injection, with threshold adjustment, into a current driven passive double-balanced mixer results in 3 dB additional gain, lower noise figure and lower intermodulation distortion. Large signal blocking and 1/f noise performance are improved significantly by eliminating the 0 and 180° LO signal crossover at the mixer. The full receiver achieves 2.2 dB/2.39 dB simplex/duplex NF (with −24.5 dBm TX leakage), >90 dBm complex two-tone IIP2, 60 dB gain and −1/+5 dBm half/full-duplex image IIP3. The receiver core consumes only 15.1 mA from a 1.5 V supply.**

***Index Terms*—25% duty-cycle, 3G, complex IIP2, DCOC, digital RF interface (DigRF), digitally assisted calibration, direct coupled filter (DCF), direct conversion, duplex noise figure, EDGE, EGPRS, EVM, GSM, high-speed downlink packet access (HSDPA), high-speed packet access (HSPA), IIP2, multi-band, multi-mode, SAW-less, smartphone, surface acoustic wave (SAW) filters, transceiver, wideband CDMA (WCDMA).**

I. Introduction

CELLULAR handset semiconductor revenue is forecast to reach $32.2 billion dollars worldwide by 2012 [1]. In 2007 WCDMA was reported to have had the largest share of this market revenue by cellular technology, and it was estimated that it would maintain this lead through 2012; with EDGE and HSPA (High-Speed Packet Access: HSDPA downlink, HSUPA uplink) occupying the second and third spots respectively [1]. ICs in 3G HSPA enabled smart phones, which also support GPRS/EDGE, are projected to have the fastest revenue growth, at a compounded annual growth rate of 130.5.2% (2006–2012), and are projected to command the highest aggregate average selling price [1]. To capitalize on the high revenue, high growth, high margin segment of this worldwide market opportunity, a small, low-cost, single-chip multi-band HSPA/WCDMA/GSM/EDGE transceiver solution is needed that supports all radio bands in North America, Latin America (AMER), Europe, Middle East, and Africa (EMEA), Asia/Pacific and Japan. Designing the transceiver with a standard digital RF (DigRF) interface offers further advantages as it typically allows fast time-to-market and enables the IC to more easily be integrated into multiple platforms with different basebands (which are typically a process shrink ahead of the transceiver part).

In order to reduce size, cost and complexity of multi-band 3G/2.5G handsets it is necessary to eliminate the inter-stage surface acoustic wave (SAW) filter, between the LNA and mixer, used in commercially available WCDMA transceivers [2], [3]. Achieving this goal with best-in-class performance, die size and current drain can be a key product differentiator. There have been several attempts to eliminate the WCDMA inter-stage SAW filter [4]–[9]. The earliest paper on the subject was that of Tamura [4], who in 2005 reported results of a single band WCDMA direct conversion receiver without SAW filter. In the receiver described by Tamura, an LNA (with inductive load) was followed by a Gilbert cell mixer, without transconductor for improved linearity. The mixer load resistors were made as thick as possible to avoid mismatch. A SAW filter and isolator were used in the transmitter path, to reduce receive band noise and PA reverse IM; which relaxes half-duplex linearity requirements. The receiver IC achieved 4.9 dB simplex NF, +38 dBm two-tone IIP2, and <−109.5 dBm duplex reference sensitivity; with very relaxed TX leakage of −29 dBm. This IC performance would not be sufficient to meet WCDMA multi-mode co-banded inter-stage SAW-less radio requirements with up to 4 dB front end loss and TX leakage up to −25 dBm.

Yanduru [5] later published a paper which describes a single-band dual-mode WCDMA/GSM/EDGE receiver without inter-

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D. Kaczman was with Freescale Semiconductors. He is now with Texas Instruments, Dallas, TX 75243 USA (e-mail: dkaczman@ieee.org).

M. Shah, M. Alam, M. Rachedine, D. Cashen, L. Han, and A. Raghavan are with Freescale Semiconductors, Lake Zurich, IL 60047 USA.

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stage SAW filter that consisted of a single-ended LNA with tuned LC load, followed by an amplifier, passive mixer with 50% duty-cycle LO and differential amplifier. High Q bond wire inductors were used to resonate with a capacitor to provide some attenuation to the TX signal. The simplex noise figure data was shown for only one channel, and no duplex noise figure data with large modulated TX leakage signal was reported. Two-tone IIP2 of +49.3 dBm, before a 13.7 dB correction factor was added, was achieved for one part and one channel. With this method, bond wire variation could affect manufacturability.

Expanding on the principle developed by Yanduru, Tenbroek [6] described a WCDMA single-mode tri-band inter-stage SAW-less transceiver with tuned LC load but added a tuned Q-enhancement circuit (with inductor and capacitor) at the intermediate node of the LNA to reduce the TX signal. The optimum IIP2 was achieved by tuning both the LNA choke as well as the Q-enhancement circuit, which could be quite complicated. There were numerous inductors on the die that consumed considerable area. Data was shown for only one part and no calibration approach was mentioned in the paper. It was not clear if the performance was hand optimized and repeatability is to be determined.

Brandolini [7] described a single-band mixer with +78 dBm IIP2 and 16 dB gain. The noise figure was reported to be 4 nV/$\sqrt{}$Hz, which is equivalent to 19 dB noise figure referred to a 50 Ohm source [$F = (Vin^2/R)/kT + 1$, where Vin is the input-referred RMS voltage per square root Hertz, $k = 1.38 \times 10^{-23}$, $T = 290$ and $R = 50$]. An external 50 Ohm LNA with 0.2 dB NF and 18 dB gain would be required in front of this mixer to achieve 3.6 dB simplex NF (0.5 nV$\sqrt{}$Hz referred to 50 Ohms), which would also degrade input-referred IIP2 and IIP3 and add parts count. The parasitic capacitances at the mixer switched pair common sources are tuned out with a 5.5 nH inductor and a 15 pF capacitor to enhance IIP2. For multi-band radios with up to three mixers this would consume considerable area. A similar approach was used for GSM, with the addition of a pseudo-differential transconductor and common-mode feedback compensation, which achieved simplex noise figure, gain and IIP2 of 3.5 dB, 31.5 dB and 51 dBm, respectively [8]. For both approaches no duplex noise figure data, at sensitivity, with a large modulated TX blocker was provided, which is necessary to verify SAW-less performance.

In 2007 Darabi [9] published a blocker filtering technique for SAW-less wireless receivers. The approach used a translational loop that wraps around the receiver LNA. Using this application for WCDMA in a direct conversion mode would require routing the transmitter signal to the receiver which would likely be problematic given the very high TX to RX LO isolation requirement. Also, for WCDMA, the image-rejection requirements for the up-conversion mixer could become challenging. For multi-band radio implementation this approach would require additional circuitry on each LNA input, affecting die size, current drain and noise figure. It is not clear that this approach is feasible for WCDMA and no data was presented.

These reference papers provide little evidence that repeatable SAW-less transceiver performance, with 1 dB worst case margin to standard, for W-CDMA/GSM/EDGE co-banded multi-band radios can be met with current techniques. Furthermore many of the approaches require inductive chokes, additional inductors, high Q bond wires or additional circuitry that can increase die size. Also, IIP2 and noise figure data appear to be reported from a single channel measurement and many include only simplex data (without TX leakage). Meeting multi-band multi-mode (GSM/EDGE + WCDMA) inter-stage SAW-less requirements for all bands with up to 4 dB front-end loss, very low power consumption, small die size and repeatable IIP2 performance introduces an additional level of complexity and difficulty. The experimental work reported here in combination with simple theoretical treatment, will provide an alternative approach to solve the key problems of designing a multi-band multi-mode inter-stage SAW-less receiver.

This paper describes a compressed-mode inter-stage SAW-less receiver with DigRF interface, which is part of a single-chip inter-stage SAW-less transceiver, targeted for use in the reconfigurable reference platform shown in Fig. 1. This approach significantly lowers bill-of-materials, shrinks board space, and reduces cost and radio complexity over previous generation non-compressed mode applications, with inter-stage SAW filters, where the GSM and WCDMA baseband paths are separate and have a separate interface to the baseband IC [3]. The receiver has seven input ports and supports 10 WCDMA bands (I, II, III, IV, V, VI, VIII, IX, X, XI) and four EGPRS bands (GSM850, EGSM900, DCS1800, PCS1900) for markets in Europe, Asia, North America and Japan as illustrated in Table I and Fig. 2.

The receiver supports EGPRS Class 34 and WCDMA FDD HSDPA category 10 operations. No external LNAs or inter-stage SAW filters are needed and the LNA choke inductors have been eliminated. This paper derives the IC requirements for multi-band multi-mode SAW-less WCDMA operation and focuses on the design and principle of operation of the core receiver section of the transceiver design which has been implemented in 90 nm CMOS. The core receiver consists of single stage low noise transconductance amplifier with large gain control range, a current commutating passive mixer enhanced for automatic on chip IIP2 calibration with 25% duty-cycle LO, including threshold adjust, and a current-input direct coupled filter. The low noise TCAs are designed without inductive loads to save area. A self-contained on-chip automatic IIP2 calibration system with algorithm routine, implemented in firmware, is used to optimize IIP2 performance. The 25% duty-cycle LO injection, with threshold adjustment, into a current driven passive double-balanced mixer with low impedance load, results in 3 dB additional gain; as well as lower noise figure, intermodulation distortion and 1/f noise. The full receiver measured at the output of the DigRF interface achieves 2.2/2.39 dB simplex/duplex (−24.5 dBm TX leakage) noise figure, 49 dB gain, >90 dBm complex two-tone IIP2, −1 dBm half-duplex image IIP3, +5 dBm duplex image IIP3. The core receiver consumes 22.6 mW.

II. Multi-Band Multi-Mode Saw-Less Requirements

WCDMA receivers have conventionally employed an external inter-stage SAW filter to suppress the transmitter leakage and thus relax the linearity requirements of the mixer. An additional

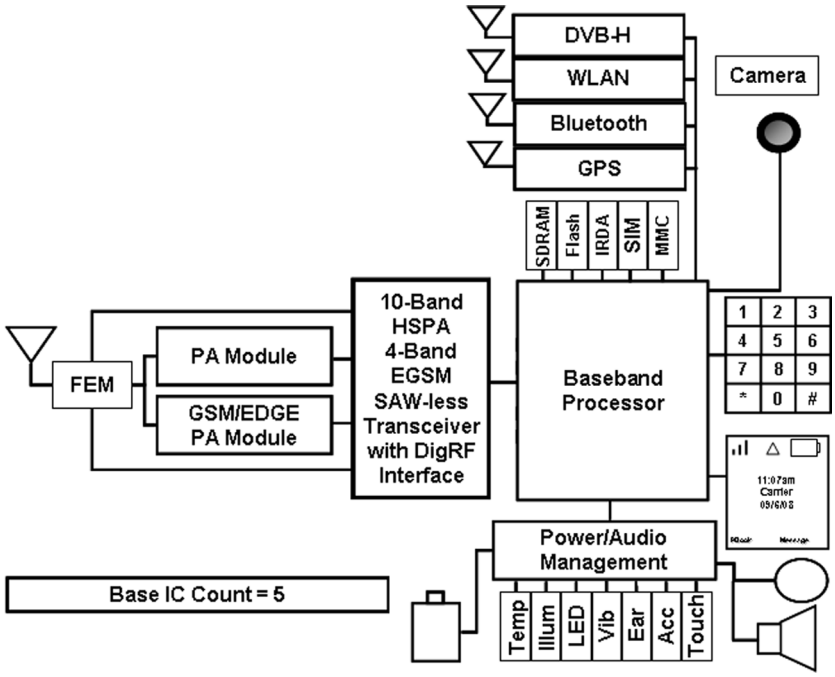

Fig. 1. Reference platform with single-chip 10-band WCDMA/HSPA, 4-band GSM/EDGE compressed-mode transceiver with DigRF Interface.

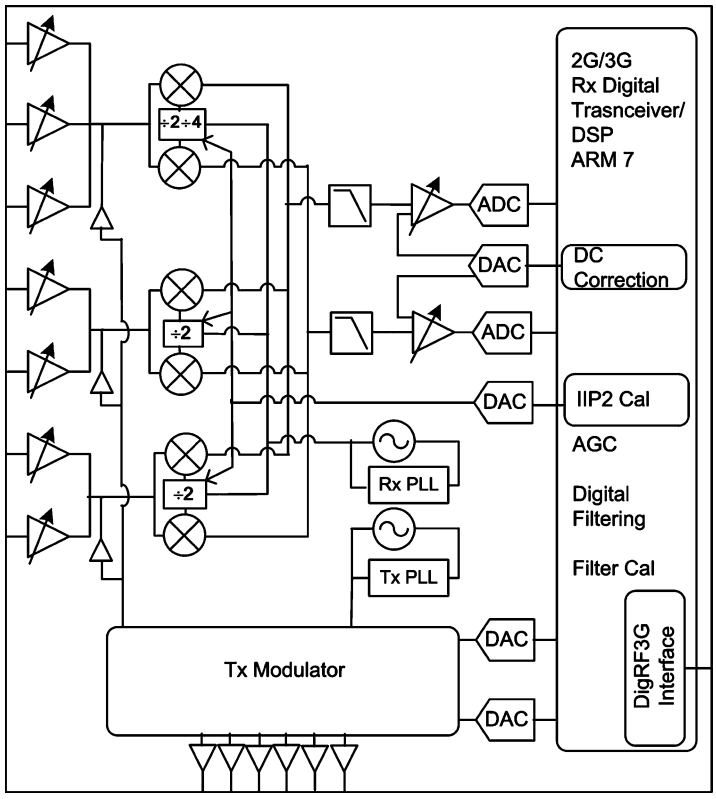

Fig. 2. Transceiver IC block diagram showing receiver with IIP2 calibration.

LNA is also used to reduce the filter noise contribution. This adds expense and size to the radio, especially for multi-band configurations. With the elimination of inter-stage SAW filter, the receiver needs to meet noise figure and linearity requirements with very high TX leakage power. For a Power Class 3 radio, the maximum output power could be +25 dBm (+24 dBm with tolerance of $+1/-3$) at the antenna. With 2 dB of loss between the PA output to the antenna, and 52 dB of duplexer isolation at the TX frequency, the receiver will see TX leakage of −25 dBm (25 dBm+2 dB −52 dB). 3GPP specification requires meeting sensitivity at max TX power, while linearity and blocking are specified at 5 dB below max power.

TABLE I
3GPP BANDS COVERED IN TRANSCEIVER IC

Operating Band	RX Frequencies (MHz)		TX Frequencies (MHz)		TX-RX Frequency Separation (MHz)
	Min	Max	Min	Max	
WCDMA I	2110	2170	1920	1980	190
WCDMA II	1930	1990	1850	1910	80
WCDMA III	1805	1880	1710	1785	95
WCDMA IV	2110	2155	1710	1755	400
WCDMA V	869	894	824	849	45
WCDMA VI	875	885	830	840	45
WCDMA VIII	925	960	880	915	45
WCDMA IX	1840	1880	1745	1785	95
WCDMA X	2110	2170	1710	1770	400
WCDMA XI	1476	1496	1428	1448	48
GSM/EDGE-GSM850	869	894	824	849	45
GSM/EDGE-GSM900	925	960	880	915	55
GSM/EDGE-DCS1800	1805	1880	1710	1785	95
GSM/EDGE-PCS1900	1930	1990	1850	1910	80

A. Simplex and Duplex Noise Figure Requirements

The NF requirements of the receiver for each operating band can derived from the 3GPP test parameters for reference sensitivity. The strictest sensitivity requirement of -106.7 dBm is specified for operating Bands I, IV, VI and X. For this sensitivity, the maximum allowable noise power within the channel bandwidth, referred to the antenna, is equal to -99 dBm [10]. To meet the 1 dB worst case margin to the specification, this becomes -100 dBm. For radios requiring multi-band, multi-mode WCDMA/GSM co-banded operation the front-end insertion loss, which includes the RF switch, duplexer and transmission lines to route multiple bands on the radio board, can be as high as 4.0 dB for Band I. With 4.0 dB front-end loss, the maximum acceptable noise plus intermodulation distortion (IMD) power within the channel bandwidth, referred to transceiver input, is calculated to be -104.0 dBm.

The actual noise plus IMD power at the input of the receiver IC can be represented by modeling the receiver as an ideal (noiseless) receiver, preceded by a summing junction where one input is the input noise (thermal noise) and the others referred to the IC input are; noise generated within the real receiver without large signal affects, noise of transmitter in receive band, noise due to reciprocal mixing of leaked transmit signal with receive LO phase noise, and effective noise due to second-order nonlinearity of the receiver. Since the actual total noise plus intermodulation distortion power $(PNtotal)$ referred to the IC input must be less than or equal to acceptable noise power, the following equations can be written (with noise contributors expressed in dBm):

$$\begin{aligned} PNtotal = 10\log_{10}\Big(&10^{PNth/10} + 10^{PNa/10} \\ &+ 10^{PNrpmix/10} \\ &+ 10^{PNtx/10} \\ &+ 10^{PNimd2/10}\Big) \\ \leq\, &104\,\text{dBm} \end{aligned} \tag{1}$$

$$\begin{aligned} PNth &= 10\cdot\log_{10}\left[\kappa\cdot T\cdot B\cdot 10^{3}\right] \\ &= -108.1\,\text{dBm} \end{aligned} \tag{2}$$

where $PNth$ is the thermal noise power, or noise power at the input of the receiver, κ is Boltzmann's constant, T is absolute temperature, B is signal bandwidth (3.84 MHz for WCDMA), PNa is the total input-referred noise power added by the receiver circuits without large signal affects, $PNrpmix$ is noise power due to reciprocal mixing, $PNtx$ is transmitter noise power in receive band, and $PNimd2$ is the input-referred second-order intermodulation distortion power generated by a modulated signal after DC offset and digital channel filtering.

The receiver simplex noise figure requirement and other circuit specifications are budgeted based on iterative tradeoffs between achievable circuit performance and overall noise requirements using (1). For example, for Band I, with worst case sensitivity requirements, simplex noise figure can be calculated using a two-tone IIP2 of 58 dBm (as derived in the linearity section), transmitter noise in receive band at the receiver IC input of -180 dBm/Hz (specified based on 47 dB duplexer isolation in receive band) and LO phase noise at the TX offset of -162 dBc/Hz, which is specified to add approximately 0.1 dB to the total noise plus intermodulation power. Rewriting (1) in terms of simplex noise figure and $PNrpmix$, $PNtx$, and $PNimd2$ in terms of circuit parameters, we find

$$\begin{aligned} PNtotal = 10\log_{10}\Big(&10^{(PNth+NFsimplex)/10} \\ &+ 10^{PNrpmix/10} \\ &+ 10^{PNtx/10} \\ &+ 10^{PNimd2/10}\Big) \\ \leq\, &104\,\text{dBm} \end{aligned} \tag{3}$$

$$\begin{aligned} PNrpmix &= Ptx - 162 + 10\log(3.84e6) \\ &= -25 - 162 + 65.84 \\ &= -121.16\,\text{dBm} \end{aligned} \tag{4}$$

$$PNimd2 = 2Ptx - 6 - IIP2$$
$$= 2(-25) - 6 - 58$$
$$= -114\,\text{dBm} \quad (5)$$
$$PNtx = -180 + 10\log(3.84e6)$$
$$= -114.16\,\text{dBm} \quad (6)$$

Substituting the results of (2), (4), (5) and (6) into (3) and solving

$$NFsimplex(dB) = 3.0\ \text{dB}. \quad (7)$$

From this example, it can be seen that of the maximum allowable noise plus intermodulaton power referred to the receiver input of -104 dBm is distributed/budgeted as follows: worst case simplex noise power (-108.1 dBm + 3.0 dB $=$ -105.09 dBm) is 78% of total power (-1.09 dB); TX noise power in receiver band (-114.16 dBm) is 10% of the total power (-10 dB); second-order intermodulation power (-114 dBm) is 10% of the total power (-10 dB); and reciprocal mixing noise power (-121.16 dBm) is 1.9% of the total power (-17.16 dB).

The simplex noise figure is very useful when designing and testing the receiver IC to determine the performance before a large TX signal is applied. However, meeting simplex noise figure and two-tone IIP2 requirements alone is not adequate to prove SAW-less operation since large signal affects such as bias noise up-conversion and 1/f noise rise with a large TX blocker leakage signal (-25 dBm) present can be significant. It is necessary to meet duplex reference sensitivity, or duplex noise figure specifications with a max TX modulated leakage signal present.

The worst case duplex sensitivity test specification for each band referred to the receiver IC input, with TX receive band noise contribution subtracted, as typically measured, can be calculated from

$$Sensitivity_{IC} = Sensitivity_{ANT} - FEIL - 1\,\text{dB} - 0.44\,\text{dB} \quad (8)$$

where $Sensitivity_{IC}$ is the duplex sensitivity specification, as measured, referred to the input with receive band noise contribution removed, $Sensitivity_{ANT}$ is the sensitivity required at the antenna ($\hat{REFI}_{\text{or}}$), *FEIL* is the front-end loss for the particular band, 1 dB is subtracted for margin and 0.44 dB is subtracted to remove the receive band noise (-180 dBm/Hz) contribution. $\hat{REFI}_{\text{or}}$ is the received reference power spectral density (integrated in a bandwidth of $1+\alpha$ times the chip rate and normalized to the chip rate) of the downlink signal as measured at the UE antenna connector which the Bit Error Ratio (BER) shall not exceed 0.001. For Band I, $Sensitivity_{IC}$ is -112.14 dBm (-106.7 dBm -4 dB -1 dB -0.44 dB). The sensitivity requirement, with TX noise in receiver band contribution included, as it is typically used to derive circuit specifications is -111.7 dBm.

The IC duplex noise figure requirement for all bands can be derived from the above equation by subtracting the required SNR (-7.7 dB) from the sensitivity specification of the IC (to get the noise level at the IC) and subtracting κTB (-108 dBm) from this. For Band I this would be 3.6 dB (-112.14 dBm + 7.7 dB + 108 dBm) and 4.6 dB without 1 dB margin. Or more intuitively from

$$NFduplex_{IC}(\text{dB}) = NFreq_{ANT} - 1\,\text{dB} - FEIL - 0.44\,\text{dB} \quad (9)$$

where $NFduplex_{IC}$ is the required duplex noise figure of the IC for the particular band (before TX noise in receiver band contribution), *FEIL* is the front-end insertion loss for the particular band, $NFreq_{ANT}$ is the noise figure required at the antenna for the particular operating band. $NFreq_{ANT}$ is the noise figure required at the antenna which can be calculated for each band using

$$NFreq_{ANT} = Sensitivity_{ANT} - (-7.7\,\text{dB}) + 108.1\,\text{dBm}. \quad (10)$$

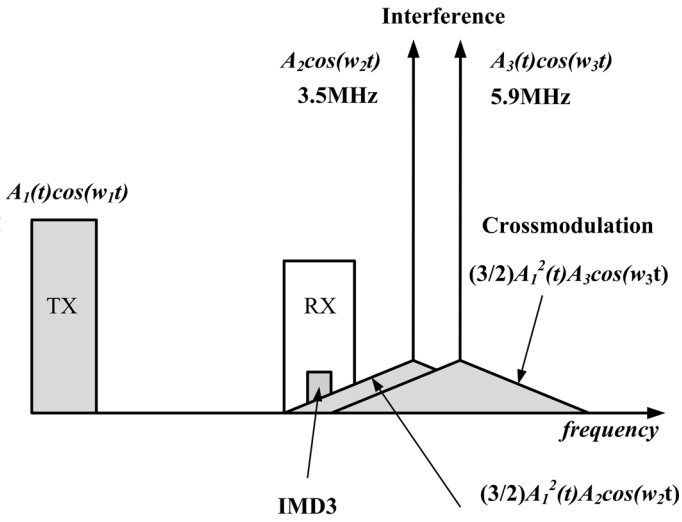

Fig. 3. Cross-modulation.

B. Linearity Requirements

The worst case linearity requirements for an inter-stage SAW-less 3G receiver, with large TX leakage, can be derived from the 3GPP minimum requirements for out-of-band blocking, at half-duplex and full-duplex image conditions and from the minimum requirements for narrowband intermodulation characteristics due to cross-modulation. The out-of-band blocking requirements apply to all bands; however, worst case narrowband IM requirements related to cross-modulation conditions apply only to Bands II, III, IV, V, VIII and X. For both out-of-band blocking and narrowband IM requirements, the UE transmitted mean power is 20 dBm (for Power Class 3).

1) Cross-Modulation: The cross-modulation requirement applies to a full duplex system where modulation of the leaked TX signal gets transferred onto a CW blocker close to the desired signal. Cross-modulation is a third-order phenomenon. Fig. 3 depicts a scenario for the narrowband IM condition, with a CW Interfering signal at 3.5 MHz and a GMSK interfering signal at 5.9 MHz away from the desired signal. From this figure it can be seen that the TX cross-modulation energy spread is twice the bandwidth and some of the energy falls

within desired signal bandwidth. The distortion product generated in the receiver can be estimated using

$$Pcm\,(\mathrm{dBm}) = 2Ptx + Pi - 2IIPcm. \tag{11}$$

Here, Pcm is total energy that falls within the desired bandwidth referred to the IC input, Ptx is transmit leakage power at the receiver IC input, Pi is CW interferer power at receiver IC input (at 3.5 or 3.6 MHz offset) and $IIPcm$ is input third-order intercept point of the modulated TX leakage signal and the CW blocker.

The specification for $IIPcm$ can be calculated from the 3GPP minimum intermodulation requirements for narrow band blocking. Requirements at the antenna input are specified with a UE transmitted mean power of 20 dBm, CW interfering signal power of −44 dBm at 3.5 MHz offset for Bands II, IV, V and X (−43 dBm at 3.6 MHz offset for Bands III and VIII) and desired signal power 10 dB above reference sensitivity. This corresponds to TX leakage power (Ptx), interferer power (Pi) and desired signal power of −30 dBm, −46 dBm and −98.7 dBm (using $\hat{REFI}_{\mathrm{or}} = -106.7$) respectively at receiver IC input, with 2 dB minimum front-end loss. With −98.7 dBm desired power, total noise plus distortion power can not exceed −91 dBm at the transceiver input (to achieve −7.7 dB SNR). Noise power at the transceiver input is −104 dBm, which is 13 dB below noise plus distortion requirements. Ignoring the noise contribution in the noise plus distortion power, the $IIPcm$ requirement can be calculated as follows:

$$IIPcm = \frac{2Ptx + Pi - Pcm}{2} \tag{12}$$

$$IIPcm(required) = \frac{(2\,(-30) - 46 - (-91))}{2} = -7.5\,\mathrm{dBm}. \tag{13}$$

Since one tone is modulated, a two-tone IM simulation is not enough to predict $IIPcm$. To verify circuit performance, under cross-modulation conditions, an envelope simulation is needed to calculate total energy that falls within the desired bandwidth at the baseband output. Results of such a simulation are shown in Fig. 4 where the total energy that falls within the desired bandwidth (0.1 to 1.92 MHz), referred to the output of the IC, is $(Pcm + G)$.

The specification compliance requirements for the IC related to cross-modulation, as derived from the 3GPP narrowband intermodulation characteristics, are typically expressed in terms of noise figure when verifying measured results. This requirement can be calculated for all 3G bands using

$$NFcm_{REQ} \cong NFreq_{ANT} + 10\ \mathrm{dB} - FEIL \tag{14}$$

where $NFcm_{REQ}$ is the required IC noise figure under cross-modulation test conditions (i.e., $Ptx = -30$ dBm and $Pi = -44$ dBm $- FEIL$), $NFreq_{ANT}$ is the noise figure requirement at the antenna for the operating band as in (10), 10 dB is added since the test requirement is specified 10 dB above reference sensitivity, and $FEIL$ is the front end loss for the operating band. For example, using a worst case sensitivity of −106.7 dBm and a front end insertion loss of 4 dB, the noise figure requirement under cross-modulation conditions would be approximately 15 dB.

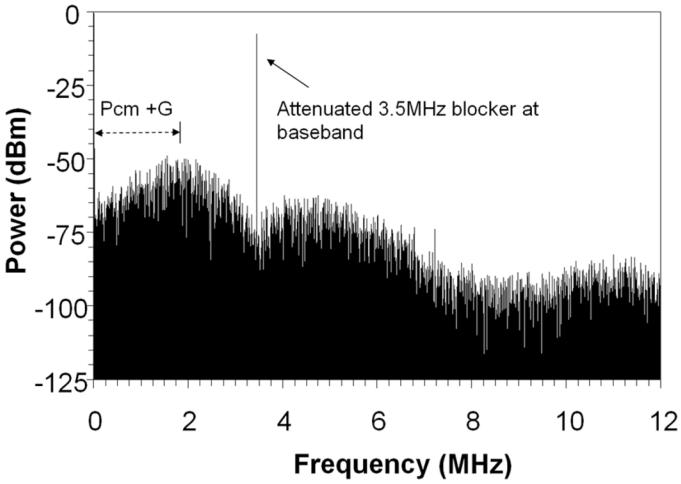

Fig. 4. Envelope simulation results at baseband for cross-modulation condition. $Pcm + G$ (Gain) is the RX output referred noise plus IM power integrated across the channel bandwidth from 0.1 to 1.92 MHz.

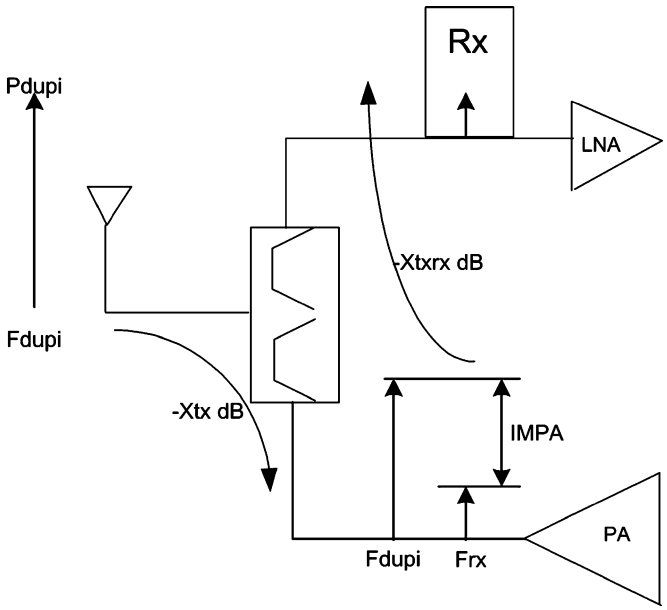

Fig. 5. PA reverse IM concept.

2) Full-Duplex Image and Half-Duplex Image Linearity: The duplex image and half-duplex image IIP3 requirements are derived from the out-of-band blocking requirements using a CW interfering signal at 2 or 0.5 times the duplex spacing from the receive band, respectively, and the modulated TX leakage signal. Linearity requirements of the receiver are dependent on the duplex filter rejection as well as the power amplifier linearity. For Band I, the duplexer provides 37 dB rejection at duplex frequency from antenna to receive port and 26 dB from antenna to TX port. PA nonlinearity is specified in terms of PA reverse IM ($IMPA$). The PA reverse IM phenomenon is shown in Fig. 5.

Out-of-band blockers that fall at duplex image frequencies (Band I: Frx −380 MHz) come in through antenna at level $Pdupi$ dBm. The TX filter attenuates the signal by Xtx dB. The

signal entering the output stage of the PA is $(Pdupi - Xtx)$ dBm. Nonlinearities in the PA generate intermodulation products that fall at RX frequencies, at level $IMPA$ dB below the signal entering the PA output. This signal is attenuated by the duplexer's TX-RX selectivity, $Xtxrx$. The following equation can be used to estimate total intermodulation power generated by the PA at the receiver IC input:

$$PIMDPA = Pdupi - Xtx - IMPA - Xtxrx \quad (15)$$

where $PIMDPA$ (in dBm) is the intermodulation power generated by the PA in the presence of the duplex blocker at the receiver IC input, $Pdupi$ is duplex blocker power at the antenna, Xtx is the TX filter attenuation from antenna to TX port at duplex frequency, $IMPA$ is the PA reverse IM in dB, and $Xtxrx$ is duplexer TX to RX isolation at RX frequency. For Band I, $PIMDPA$ can be estimated using (15) with the values: $Pdupi = -15$ dBm, $Xtx = 26$ dB, $IMPA = 20$ dB, and $Xtxrx = 47$ dB, to obtain

$$\begin{aligned} PIMDPA\,(\mathrm{dBm}) &= (-15 - 26 - 20 - 47)\ \mathrm{dBm} \\ &= -108\,\mathrm{dBm}. \end{aligned} \quad (16)$$

The desired signal power for the out-of-band blocker case is -103.7 dBm (3 dB below reference sensitivity) at the antenna or -105.7 dBm at the transceiver input for minimum front-end loss. With -105.7 dBm desired signal power, noise plus distortion power cannot exceed -98 dBm to achieve -7.7 dB SNR. Total noise plus distortion power referred to receiver IC input can be estimated as follows:

$$\begin{aligned} PIMDtotal &= 10\log_{10}\left(10^{PIMDPA/10} + 10^{PIMDrx/10} + 10^{PNtotal/10}\right) \\ &\le -98.88\,\mathrm{dBm} \end{aligned} \quad (17)$$

where $PIMDtotal$ is total noise plus distortion power, $PIMDPA$ is intermodulation power generated by PA, $PIMDrx$ is intermodulation power generated by receiver circuit and $PNtotal$ is total noise power of the receiver referred to receiver IC input. Solving for $PIMDrx$ in (17) gives

$$\begin{aligned} PIMDrx &= 10\log(10^{-98/10} - 10^{-108/10} - 10^{-104/10}) \\ &= -99.88\,\mathrm{dBm}. \end{aligned} \quad (18)$$

At the receiver IC (LNA) input, TX signal power and interferer power are -30 dBm and -52 dBm $(-15-37$ dB$)$, respectively. From this information the IIP3 of the receiver can be calculated to be -6 dBm using the standard two-tone IIP3 equation. The half-duplex image IIP3 requirement for the receiver can also be calculated to be -6 dBm using the same method.

The specification compliance requirement for the duplex image intermodulation case, as measured in the lab, is determined from the 3GPP wideband blocking test and is specified in terms of noise figure. This requirement can be calculated for all bands as follows:

$$\begin{aligned} NFduplex_{image} = NFreq_{ANT} \\ +3\,\mathrm{dB} - FEIL - PA_{RIM} \end{aligned} \quad (19)$$

where $NFduplex_{image}$ is the required IC noise figure under duplex-image blocking conditions, $NFreq_{ANT}$ is the noise figure requirement at the antenna for the operating band as derived in (10), 3 dB is added since the out-of-band blocking test requirement is specified at 3 dB above reference sensitivity, $FEIL$ is the front-end loss for the operating band, and PA_{RIM} is the degradation due to PA reverse isolation. For example, for Band I since $PIMDPA$ $(-108$ dBm$)$ contributes 0.4 dB to the total noise plus IMD power of $PIMDtotal$ $(-98$ dBm$)$, PA_{RIM} is equal to 0.4 dB. From (19), $NFduplex_{image}$ can be calculated to be approximately 7.6 dB $(9$ dB$+3$ dB-4 dB-0.4 dB$)$. The TX noise in receive band will have a small contribution but is ignored in this equation since the test is performed at 3 dB above reference sensitivity and the TX power is 5 dB lower than the sensitivity case.

The input tone levels for this test at the IC for each operating band can be calculated as follows based on out-of-band blocking requirements and front-end selectivity. For example, for Band I,

$$\begin{aligned} &Pdupi(Ftx - DuplexSpacing) \\ &\quad = -15\,\mathrm{dBm} - FEselectivity \end{aligned} \quad (20)$$

$$Ptx = -30\,\mathrm{dBm} \quad (21)$$

where $Pdupi$ is the power level of the duplex-image blocker ($Ftx = 190$ MHz for Band I) at input of the IC, -15 dBm is the level of the duplex-image blocker at the antenna for Band I, $FEselectivity$ is the front-end attenuation of the duplex-image blocker for the particular band, Ptx is the power of the modulated TX leakage at the input of the IC based on a UE transmitted mean power specification of 20 dBm (5 dB less than the -25 dB max leakage power used in the sensitivity case).

3) Second-Order Intermodulation Requirements: Second-order intermodulation distortion is generated when a non-ideal receiver is exposed to a two-tone CW or AM modulated signal. In the case where the interfering modulated signal is very large, very high IIP2 performance can be required to minimize SNR degradation. Non-idealities that can degrade IIP2 performance include device mismatch (without mismatch and ideal differential stages IIP approaches infinity) and layout asymmetry. Part-to-part IIP2 performance can also change due to process variation and temperature. For each part, IIP2 performance can potentially vary with interferer offset, modulation BW and two-tone spacing. Because of this it is important to design the receiver with sufficient IIP2 margin to specification. Digitally assisted calibration techniques can be employed for improved manufacturability.

The requirement for out-of-band IIP2 is determined from system sensitivity tradeoffs using the following equation:

$$PNimd2 = 2Ptx - IIP2 + C(N) \quad (22)$$

where $PNimd2$ is the input-referred IMD2 power generated by a modulated signal after DC offset and digital channel filtering,

Ptx is the modulated uplink (UL) TX leakage power level at the receiver IC input, $IIP2$ is the required continuous wave (CW) two-tone complex IIP2, and $C(N)$ is an adjustment factor which is dependent on the number of data channels (N). The correction factor takes into account the difference in second-order distortion created by two-tone test signals relative to that resulting from a modulated signal (spread to approximately 2 times the signal bandwidth) with the DC and out-of-band frequencies filtered out.

A closed-form approximation for the correction factor, based on theory and MATLAB simulations [11], is given by

$$C(N) \cong 10\log 10\left(\frac{3}{8} - \frac{7}{(24N)}\right) \tag{23}$$

where it can be seen that the correction factor has less of an effect (a smaller negative number) as the number of channels increases, which results in higher two-tone IIP2 requirements. For 1, 6, and 16 data channels the correction factor is approximately -10.8 dB, -5 dB, and -4.3 dB, respectively.

To determine the correction factor for the actual circuit, schematic level envelope simulations were first performed using a two-tone signal (with each tone 3 dB lower than the modulated signal power) followed by simulations using a TX uplink modulated signal generated from test equipment (1 data and 1 control channel). The intermodulaton distortion power was 5.4 dB lower (after DC offset removal and using a sinc filter approximation for the low-pass filtering) for the TX modulated case. This equates to a correction factor of -11.4 dB (6 dB lower since the two tones are 3 dB lower in power than Ptx) using Ptx as in (22), which agrees fairly well with the -10.8 dB correction factor from (23) and other publications [11]–[13].

For the calculations in this paper, a correction factor (C) of -6 dB was used to calculate the two-tone IIP2 requirement with Ptx of -25 dBm. This correction factor was selected to allow 5.4 dB margin from envelope simulations and is the same correction factor, after margin, as used in [12]. Sufficient margin was allocated for IIP2 to account for part to part, process and temperature variation. The two-tone IIP2 requirement can be reduced or increased based on the correction factor used and number of data channels assumed. The ability to meet two-tone IIP2 requirements with increased number of data channels offers a product advantage/differentiator over systems designed for a single data channel limited to 12.2 kbps uplink speeds. Achieving very high IIP2 offers the additional advantage that lower cost duplexers with less TX to RX attenuation can be used.

By inserting (22) into (3) and subtracting the required SNR $(-7.7$ dB$)$ the duplex sensitivity to achieve -7.7 dB SNR can be plotted versus two-tone IIP2 required with allocated NF, TX noise power and reciprocal mixing noise power. For example for Band I,

$$\begin{aligned} Sensitivity_{IC} &= 10\log_{10}\left[10^{[2(-25)-IIP2-6]/10} \right. \\ &\quad + 10^{(-108.1+NF)/10} + 10^{-114.16/10} \\ &\quad \left. + 10^{-121.15/10}\right] - 7.7. \end{aligned} \tag{24}$$

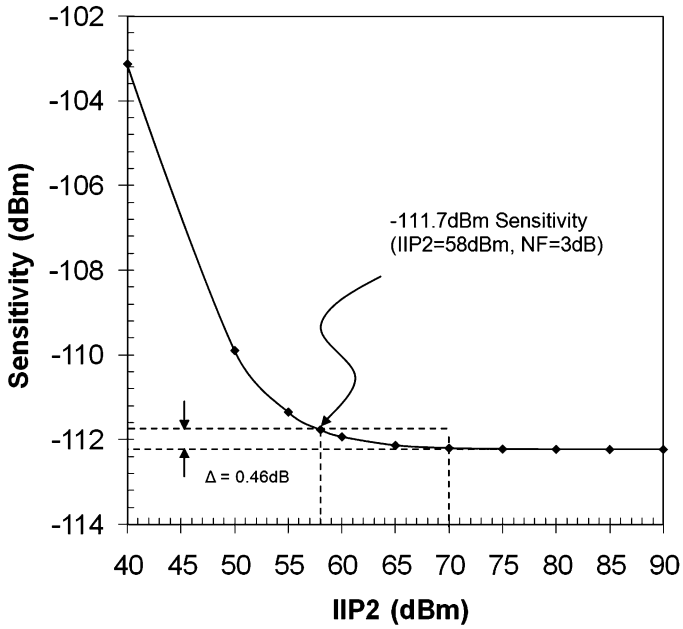

Fig. 6. Receiver sensitivity referred to the IC input versus IIP2 at TX offset with simplex $\mathrm{NF} = 3$ dB and uplink modulated $Ptx = -25$ dBm.

This equation is plotted in Fig. 6, where it can be seen that a two-tone IIP2 of $+58$ dBm is required to meet a reference sensitivity of -111.7 dBm at the receiver IC input (including TX noise contribution), to achieve an SNR of -7.7 dB, with a 3 dB simplex noise figure and -25 dBm TX UE leakage power. The value of IIP2 was selected such that the estimated second-order intermodulation power after baseband filtering and DC offset removal (based on correction factor) contributes approximately 0.46 dB degradation to the overall IC noise figure or 10% of the total noise plus IMD power $(-114$ dBm$)$ at sensitivity. Also, by inserting this IMD2 power $(PNimd2)$ into (22) and reworking, using a correction factor of 6 and a TX leakage power of -25 dBm, we find the required minimum two-tone complex IIP2 to be

$$\begin{aligned} IIP2(required) &\geq 2(-25\ \mathrm{dBm}) - (-114\ \mathrm{dBm}) - 6\ \mathrm{dB} \\ &= 58\ \mathrm{dBm}. \end{aligned} \tag{25}$$

Worst case simplex noise figure of 3 dB used in this analysis may seem aggressive, however from the plot it can be seen if the simplex noise figure specification were relaxed an additional 0.46 dB the worst case complex two-tone IIP2 required for the receiver IC (not just the mixer) would be $+70$ dBm. This also assumes -162 dBc/Hz LO phase noise at the TX offset and -180 dBm/Hz TX noise in receiver band. From this it can also be seen that there is also not much room to relax the phase noise since the only variable left is the TX noise in receive band, which is very aggressive for a SAW-less transmitter.

The equation for calculating the actual complex two-tone IIP2 from measurements can be represented as follows:

$$\begin{aligned} IIP2_{2T\_complex} &= 2P_{1\_TX} \\ &\quad - \left[10\log_{10}\left(10^{P_{IM2I}/10} + 10^{P_{IM2Q}/10}\right) - G_{complex}\right] \end{aligned} \tag{26}$$

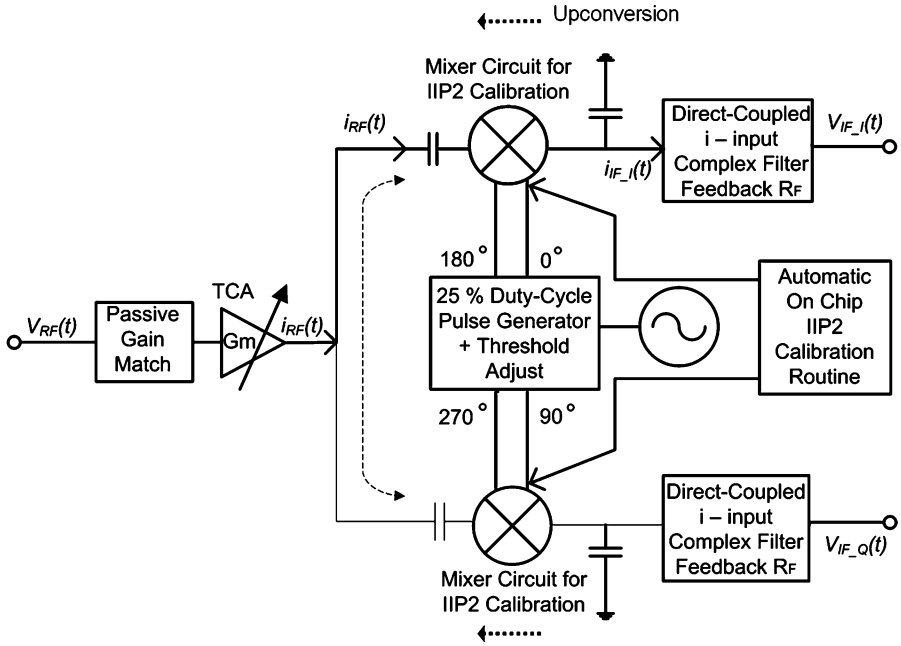

Fig. 7. Simplified block diagram of inter-stage SAW-less receiver core, along with the quadratue generator and IIP2 Calibration (patent pending).

where P_{IM2I} and P_{IM2Q} are the IMD2 power for the I and Q channels (generated from a two-tone signal), respectively, at the output of the IC. $G_{complex}$ represents the complex gain, which is 3 dB higher than the gain of one channel if the gain of each channel is equal. If we assume the IMD2 power of one channel is much better than the other then the composite IIP2 becomes approximately equal to the IIP2 of the worst channel plus 3 dB. Because the IIP2 between channels can be significantly different it is important that the IIP2 of both channels be high [15]. Also, since the correction factor was used in the derivation of the two-tone IIP2 requirement, the correction factor should not be subtracted from the measured IIP2 data when comparing to specifications. Two-tone measurements should be done close to the modulation bandwidth for best correlation.

III. Multi-Band Multi-Mode SAW-Less Receiver Design

The receiver is based on a direct conversion architecture for WCDMA and a very low IF (VLIF) architecture (with direct conversion option) for GSM/EDGE. This enables high-integration, low power and simplifies frequency planning for multi-band applications. Seven transconductance amplifiers (TCAs) and three mixer pairs are used to convert combinations of 10 possible WCDMA bands and 4 EGSM bands to in-phase (I) and quadrature (Q) signals as shown in Fig. 2. A single baseband path is shared for all 3G and 2.5G bands to minimize die size. This consists of I and Q paths each containing a direct coupled filter (DCF), baseband amplifier (BBA), and analog to digital converter. The receiver and transmitter each contain a fractional-N synthesizer and digitally tuned on chip VCO. A digital transceiver provides digital filtering, gain and phase imbalance correction, digital AGC and DigRF 3G interface. Also provided is DC offset, I/Q and IIP2 calibration. The TCA and BBA have quasi-continuous gain adjusted as part of the AGC system.

A simplified block diagram of the receiver core is shown in Fig. 7, along with the quadrature generator and IIP2 calibration control. Here it can be seen the signal is first converted to a current, using a single low noise transconductance stage with large gain control range and passive gain match. The passive mixer commutates the AC current signal with 25% duty-cycle LO which allows the current to be directed to either the I or the Q mixer as a function of the LO 25% duty-cycle waveform. A direct coupled current input filter (DCF) provides a low impedance virtual ground to the mixer output nodes such that the current flows to the feedback resistor of the DCF. The gain of the receiver is a function of the passive gain, TCA Gm, mixer conversion efficiency and DCF feedback resistor (R_F). A capacitor at the output of the mixer provides a low-impedance to ground to stop high frequency signals from passing though the DCF. This topology results in 3 dB more gain, lower noise figure, lower 1/f noise and improved uncalibrated IIP2 over conventional approaches. The 25% duty-cycle LO eliminates crossover of the non-ideal 0° and 180° LO pulses and the threshold adjust is used to optimize performance. An automatic on chip IIP2 calibration routine is used with a novel mixer circuit for IIP2 calibration to enhance IIP2 while accounting for interaction between the I and Q mixers. This overcomes the problem where up-converted DC offsets, due to calibration at one mixer, can affect the optimization of the other mixer [16] as shown in Fig. 7. A more detailed description of the receiver circuit blocks, principle for operation and on chip calibration is given in Sections III-A–F.

A. Variable Gain Transconductance Amplifier (TCA) With Inductor-Less Choke

The low noise TCA converts the input signal voltage $V_{RF}(t)$ into an AC current $i_{RF}(t)$ and provides the desired parallel real part of the input impedance (800 ohm typically) for passive gain and desired Q (no greater that 5) for ease of matching. The AC current signal $i_{RF}(t)$ is not to be confused with a DC current as it can pass through a blocking capacitor which is a short at RF

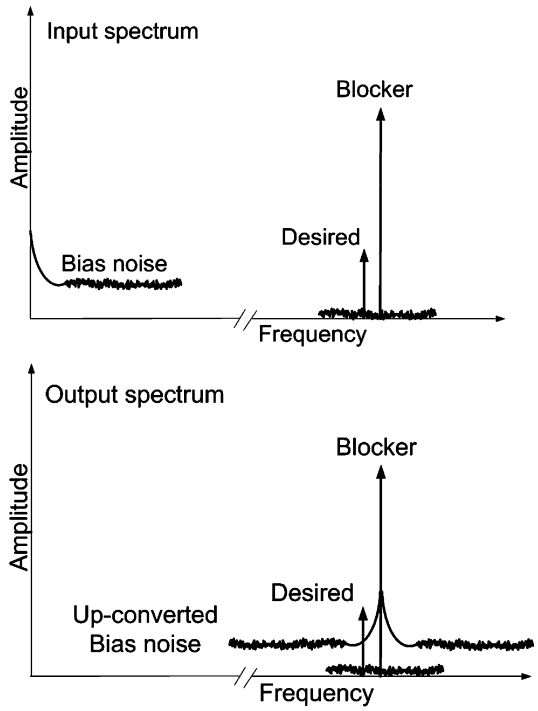

Fig. 8. Receiver desense due to bias noise (input and output spectrum).

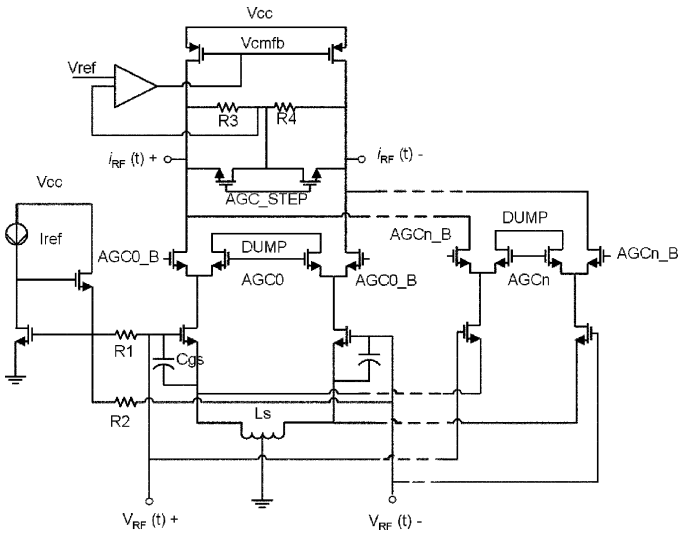

Fig. 9. Simplified schematic of transconductance amplifier (TCA) with large gain control range (patent pending).

frequencies. Only one low noise amplification stage is used prior to mixing, as shown in Fig. 7, to minimize LO feedback/leakage coupling points, which can degrade IIP2. A single stage also results in reduced current drain. Since there is only one LNA in this design it absorbs the full 40 dB gain control range specification used in conventional WCDMA receivers with two LNAs where RF gain control range was typically split between the two stages. Conventional binary-weighted gain control topologies alone are not able to meet this range since adding additional gain control bits increases die area, noise and parasitics, which limits the maximal achievable range. The TCA contains circuit enhancements to provide the required 40 dB of gain control range in one stage with minimal effect on input impedance as will be explained further in this section. Another critical requirement for the TCA, to achieve SAW-less operation, is that it be insensitive to bias noise up-conversion since the maximum leaked TX signal is present during sensitivity testing. The mechanism of receiver desense caused by low frequency noise up-conversion with a large amplitude interferer is shown in Fig. 8 and is described in the literature [17], [18]. To minimize die size for multi-band multi-mode receivers, the large bulky choke inductors conventionally used in low noise amplifiers have been eliminated.

The simplified schematic of one of the seven transconductance amplifiers used in the receiver is shown in Fig. 9. Each of the seven transconductance amplifiers consists of a differential low noise common source NMOS g_m-stage with source degeneration to introduce a real part to the input impedance without adding significant noise. A differential input to the TCA is used to minimize RF, LO and noise coupling and to achieve high impedance with optimal noise match for more passive gain. In order to implement fine gain control each transconductor is divided into five binary-weighted sections with digitally-controlled current steering via cascoded devices. This allows 31 different gain settings and the total dynamic range is roughly 30 dB. Each transconductance unit has its current either directed to the load or directed to a dummy bus by digitally steering all of the current in the cascode device, thus keeping the input impedance constant. In the maximum gain stage, all of the current is directed to the load. In the minimum gain stage, all of the current is directed in to the dummy bus. The attenuation for each binary step of the five bit gain control is determined by the following equation:

$$Attenuation\,(\mathrm{dB}) = 20\log\left(1 - \frac{agc\_in\_decimal}{31}\right). \quad (27)$$

A coarse step was added to provide a total gain control range of 40.5 dB. The step gain control was achieved by reducing load resistance with the addition of a smaller shunt load, which results in little change in input impedance. Simulation results of the receiver gain versus fine and stepped AGC settings, is shown in Fig. 10.

The AC voltage at the output of the transconductor is mainly a product of the AC current and the impedance between the output of the transconductance stage and the input of the direct coupled filter stage. This impedance is determined by the on resistance of the passive mixer switching core and the size of the blocking capacitors used to AC couple the two stages together. It is important to limit the magnitude of the AC voltage swing on the output of the transconductor by making sure this impedance is suitably low for the transconductance used and the highest anticipated signal level on the input device. The load to the transconductance amplifier is implemented as an active load with common mode feedback or as a resistive load to reduce die area instead of using large bulky inductors. The transconductance amplifier current can be adjusted with a 3-bit digital bus. The bias circuit contains high value resistors, which minimize desense due to bias noise up conversion.

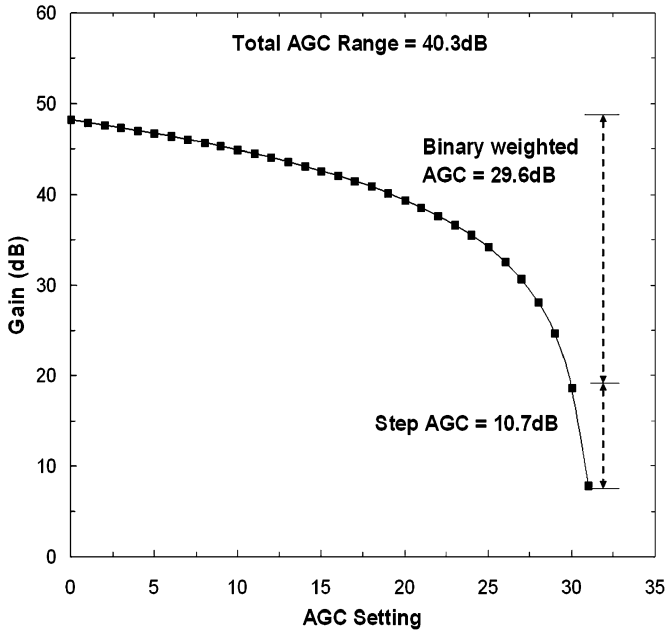

Fig. 10. TCA gain versus AGC settings.

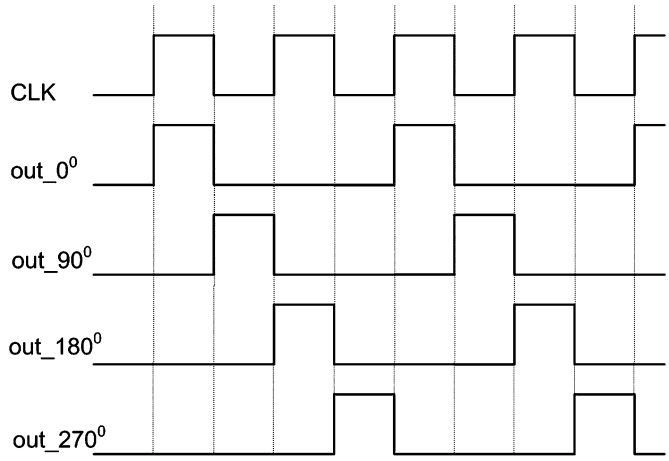

Fig. 11. 25% duty cycle LO waveforms at mixer gates (single-ended).

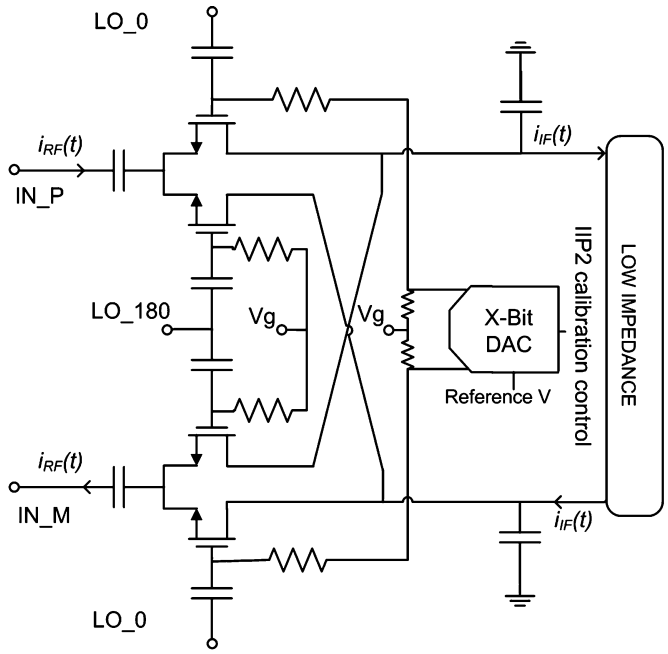

Fig. 12. Simplified schematic of passive mixer circuit for IIP2 calibration (patent pending).

B. Mixer Circuit (Current-Conveyor) for IIP2 Calibration With 25% Duty-Cycle

The RF output current of the TCA, $i_{RF}(t)$ is split into two capacitive coupled current-driven double-balanced passive mixer circuits for IIP2 calibration, supplied by quadrature signals with 25% duty-cycle, as shown in Fig. 7. Since the 0° and 90° pulses do not overlap, as shown in Fig. 11, the full RF current passes through each double-balanced mixer separately as opposed to being split between the I and Q mixers; as in conventional direct conversion receivers with 50% duty-cycle LO signals.

A passive mixer approach was selected because of its potential for low 1/f noise, exceptional large signal handling capability and very low intermodulation distortion. Measured results for single-ended and single-balanced passive FET mixers with LO applied to the gate have been demonstrated which show IIP3 as high of +38 dBm, 1 dB compression point of +9 dBm and 6.2 dB noise figure at X-band frequencies [19]. NMOS devices were chosen over PMOS devices because they achieve the same on-resistance with much lower capacitive load for the quadrature generation block.

A double balanced structure was selected because it cancels out nonlinear dependence of gds on Vds and common-mode DC biasing signals. However, because the DC is averaged out, a new mixer circuit for second-order intercept point calibration was developed, as shown in Fig. 12. Here capacitors are used to separate each of the mixer gates symmetrically and the differential output of an x-bit DAC is used to control the bias of the LO_0 (LO_90) mixer devices. Tuning only two of the gates provides twice the accuracy over tuning all four, and adjustment at the gate of a passive mixer is advantageous since it generates minimal noise and DC offsets. The common-mode of the DAC is used to supply the bias to the LO_180/ (LO_270) mixer devices, which will eliminate any common-mode offset. There is also no temperature delta for the DAC since as R moves, I moves and V stays the same. For an x-bit DAC the offset introduced on the upper mixer device gate is given by V_{m1g} and the offset on the bottom device is given by V_{m2g}

$$V_{m1g} = vg + (2^{x-1} - n) \cdot \left(\frac{Total\_range}{2^x - 1} \right) \tag{28}$$

$$V_{m2g} = vg - (2^{x-1} - n) \cdot \left(\frac{Total\_range}{2^x - 1} \right) \tag{29}$$

where $n = 0, \ldots, 2x - 1$ and $Total\_range$ is the single-ended total range of the DAC. The calibration method will be described further in the calibration section.

This approach has advantages over injection at the passive mixer output [16], which can result in large DC offsets. Large DC offsets can degrade common-mode rejection ratio which can

degrade IIP2 and limit IIP2 calibration range. DC offsets generated from IIP2 calibration can limit ADC headroom or require additional DC offset correction further down the receiver chain. Changes in DC offset with IIP2 calibration are also undesirable since a separate DC offset correction is required after each IIP2 calibration adjustment. This approach also has advantages over techniques based on bipolar/CMOS Gilbert cell mixer topologies [20]–[22] which can potentially have degraded linearity and large signal handling performance versus optimized CMOS topologies based on passive mixers.

Three mixer cores are provided to cover 10 WCDMA bands and 4 EGSM bands. The mixer cores need to be AC coupled through a capacitor due to the fact that the common mode voltage of the DCF is different from the common-mode voltage of the RF transconductor stage. The sizing of the switches and capacitors can be used to affect all of the main receiver performance parameters. The coupling capacitors are roughly scaled with frequency so they present the same impedance for high and low bands. The mixer cores convert the current mode RF signal to baseband I and Q signals. The IF output signals from the three mixer cores are combined at the mixer outputs. A 10 pF capacitor is placed from each IF output to ground to provide a low impedance return path for the RF signal as shown in Fig. 12. The capacitor has been integrated in with the mixer switching devices in the layout in order to filter out the RF as soon as possible after the switching has been performed. The virtual ground property of the DCF provides a low impedance for the IF signal.

The improved receiver gain, linearity and large signal handling performance benefits of using this current driven mixer topology for IIP2 calibration along with 25% duty-cycle with threshold adjustment, can be better understood by examining the operating principle.

1) Operating Principle: Passive Mixer Current Conveyor (25% Duty-Cycle) Gain and NF: In a direct conversion receiver where the current-driven I and Q mixers (operating as current conveyors) are clocked with a 25% duty-cycle LO, all of the current will go to either the I mixer or the Q mixer at one instant in time. This, along with the conversion efficiency of the mixer, results in higher receiver gain relative to a 50% duty-cycle implementation, where the current will be split to both the I and Q mixers.

The mixer conversion loss for different duty-cycle LO waveforms can be derived using the operating principle of a passive FET mixer and Fourier series expansion of the LO waveform. A single passive FET mixer operating as a voltage conveyor (voltage in and voltage out) can be illustrated as an idealized circuit consisting of a switch opening and closing at the LO rate $F(t)$, in series with the RF signal $v_{RF}(t) = \sin w_{RF}t$ when the switch is closed [19]. A value of 1 or 0 can be assigned to $F(t)$ to represent the switching action. The convolution of the input signal with the Fourier series of the LO waveform results in a difference frequency at the mixer output. Similarly, for commutation of an input current using a balanced mixer with a differential LO signal, the output signal at the difference frequency can obtained by convolving the mixer input current with a Fourier series representation of the differential LO waveform. The Fourier series representation for a differential 50% duty-cycle LO waveform with pulse train 1, -1, 1, -1 can be represented as

$$F_{50\%}(t) = \frac{4}{\pi}\left[\cos w_{LO}t - \frac{1}{3}\cos 3w_{LO}t + \frac{1}{5}\cos 5w_{LO}t + \cdots\right]. \quad (30)$$

A differential 25% duty-cycle LO waveform with pulse train 1, 0, -1, 0 can be represented as

$$F_{25\%}(t) = \frac{2\sqrt{2}}{\pi}\left[\cos w_{LO}t + \frac{1}{3}\cos 3w_{LO}t - \frac{1}{5}\cos 5w_{LO}t + \cdots\right]. \quad (31)$$

When either of these LO waveforms is multiplied by $i_{RF}(t) = G_M v_{RF}\sin(w_{RF}t)$, and expanded using trigonometric identities we find the output current $i_{IF}(t)$ at the difference frequency $(f_{RF} - f_{LO})$ for duty-cycle (d) can be shown to be (ignoring the passive voltage gain at the TCA input)

$$i_{IF}(t) = \left(\frac{2}{\pi}\sin \pi d\right)\frac{1}{2d}G_M v_{RF}\sin w_{IF}t. \quad (32)$$

The $1/2d$ term compensates for the increase in current to the mixer as the duty-cycle is changed. Since $v_{IF}(t) = i_{IF}(t)R_F$ and the core receiver conversion gain is equal to v_{IF}/v_{RF}, the difference in gain between a current driven mixer with 25% duty-cycle to that of 50% duty-cycle is

$$\begin{aligned}\Delta G &= 20\log\left(\frac{2\sqrt{2}}{\pi}G_M R_F\right) \\ &\quad - 20\log\left(\frac{2}{\pi}G_M R_F\right) \\ &= 3.0\ \text{dB}. \end{aligned} \quad (33)$$

If positive pulses (from 0 to 1) are used for the LO pulse trains, a 3 dB improvement in gain by using 25% duty-cycle will still be achieved. However the magnitude of the Fourier components with be reduced in half. In this case, the 25% and 50% duty-cycle waveforms will exhibit a DC term (1/2 and 1/4, respectively) and the 25% duty-cycle waveform will contain a second harmonic term $(1/\pi)$. This 3 dB improvement in gain and equal improvement in mixer noise figure, along with the current driven mixer topology with IIP2 calibration, are key components to meet the stringent full duplex noise requirements with only one TCA stage.

Fig. 13 shows simulation results of the core receiver gain and noise figure versus LO duty-cycle. The simulation shows that the core receiver gain is increased by 3 dB and receiver NF is improved by 2.5 dB with approximately 25% duty-cycle LO compared to 50% duty-cycle LO. This figure highlights the importance of the LO pulse rise time which can be compensated for somewhat by threshold adjustment.

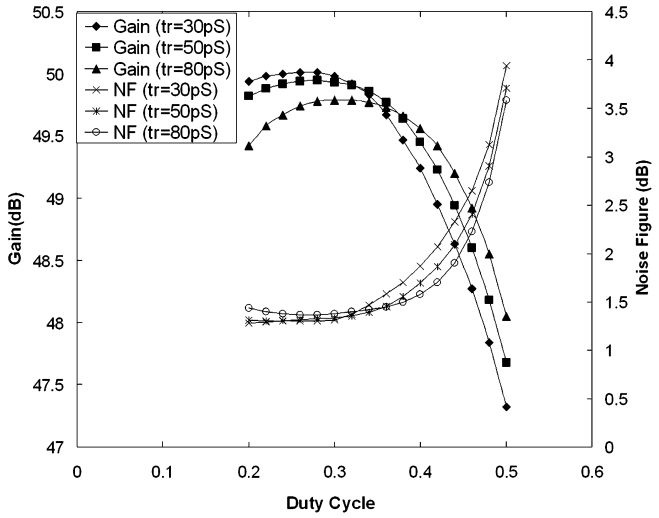

Fig. 13. Simulated core receiver gain and NF versus LO duty-cycle using current driven mixer ($\mathrm{NF} = 1.4$ dB, $G = 50$ dB with 25% duty-cycle, $tr = 30$ pS).

Using 25% duty-cycle with a current driven passive mixer has an additional benefit that it results in an increase in the source and output impedance of the on mixer, which results in less noise amplification at baseband. Because only one of the mixer branches is on at an instant of time, the source impedance of the on mixer becomes equal to the $Zout$ of the LNA, as opposed to a parallel combination with the quadrature mixer Ron and $Zout$. The output impedance of the current driven mixer is ideally very high but is decreased due to the parasitic capacitance $(Cpar)$ at the switching pair input nodes; similar to that of a switched capacitor circuit, where $Rout = (1/2f_{LO} \cdot Cpar)$. This is equivalent to having a resistor at the input of the DCF that can degrade total output noise, similar to a transimpedance amplifier where the output noise of the amplifier is proportional to $(1 + 2\ RF/Rout)$ times the input-referred noise voltage. Thus, by providing higher input impedance to the mixer the output impedance is increased which results in less amplification of opamp noise due to SC sampling and less noise converted to baseband. Also, for current driven topologies, it is optimal to provide high source impedance followed by low input impedance for optimum linearity.

As previously mentioned the principal of operation for a current driven or current commutating passive mixer with duty-cycle reduction, where the current is split between channels, is somewhat different from that of a voltage conveyor approach (voltage in and out) [5], [19]. For the voltage-conveyor approach the mixer load impedance $(Rout)$ is potentially higher than the source impedance (Rin) to boost the voltage signal. The voltage interface can be accomplished by an opamp (with resistive feedback), a differential amplifier, or with a high input impedance post-mixer baseband amplifier structure with one opamp for each differential mixer output port. The latter approach tends to exhibit higher noise because of the contributions of the two amplifiers [23]. The 3 dB benefits in gain can also be achieved in voltage-conveyor topologies with 25% duty-cycle LO. A recent publication using this voltage-conveyor approach with the later output stage topology and conventional passive mixer with four phase clock, for wireless LAN applications (reference published after the development of this IC), achieved a noise figure of 7.5 dB (6.5 dB without balun) [24]. This particular implementation; however, falls short of the 3 dB simplex noise figure target for SAW-less operation. Also, the additional post voltage-mode LNA buffer amplifier used to lower the impedance to the mixer input adds current drain and a high impedance point for LO leakage coupling which can potentially degrade IIP2 [15].

2) Passive Mixer Current-Conveyor (25% Duty-Cycle): Large Signal Handling and Linearity: A significant advantage of using a current driven mixer with 25% duty-cycle is that it is not sensitive to 1/f noise rise and increased intermodulation distortion caused by mixer 0° and 180° LO waveform overlap when a large blocker is present, as in 50% duty-cycle LO implementations. The high equivalent resistance, looking into the current driven mixer output, realized since one of the quadrature mixer paths is off at that instant of time, as well as the virtual ground at the output of the mixer, offer noise and linearity benefits as will be explained further in this section.

Flicker noise is known to be proportional to a devices dc bias channel current. For passive mixers, since a DC bias is not applied, it may seem logical that the flicker noise should be zero. However, it has been shown that with a non-zero time varying drain current, even with zero mean, noise appears around zero frequency and harmonics of the excitation [25]. Also, if a dc offset is present with a large LO excitation and large blocker, it seems possible a small amount of dc current could exist in a passive mixer.

In conventional direct conversion architectures, with 50% quadrature generation, 1/f noise degradation due to 0° and 180° LO crossover has been documented [25]. This can be intuitively understood by looking at ideal and non-ideal LO waveforms. For ideal 50% duty-cycle LO waveforms input to a balanced mixer, the 0° and 180° pulses (binary complements) at the mixer gates are non-overlapping, and the mixer devices are either on or off. However with non-ideal rise and fall times, it is possible that the binary complement LO pulses can cross at a point above that which the gate bias allows the mixer device to turn on. During cross over periods the input and output impedance of both the I and Q mixers decreases, causing the total noise referred to the output of the baseband amplifier to increase. At the same time the partially on mixers cause the signal to short at the differential input to the DCF (virtual ground nodes of the mixer), shown in Fig. 12, which degrades the signal to noise ratio, making 1/f a large contributor to total noise. Reducing the threshold to circumvent the problem can help somewhat until a point when performance drops due to reduced LO turn on swing. Also, when a very large RF blocking signal is present at sensitivity, such as TX leakage in a full duplex system, there is potential for the large signal bias point to shift exacerbating the problem further. The large signal can also potentially increase DC offsets, due to imbalanced parasitic capacitance of non-ideal layouts. It has been demonstrated that increasing AC current through a mixer device channel with a large RF blocker can generate considerably more 1/f noise [25]. This is a significant concern for SAW-less operation and is one reason why simplex noise figure and small signal two-tone IIP2

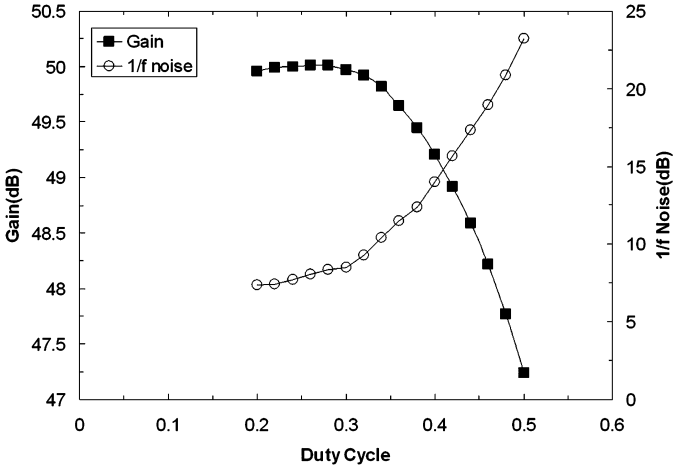

Fig. 14. Simulated gain and spot NF (at 1 kHz) versus LO duty cycle at high power level of −26 dBm. Large signal blocking performance is improved significantly (15 dB) with core topology and 25% duty-cycle.

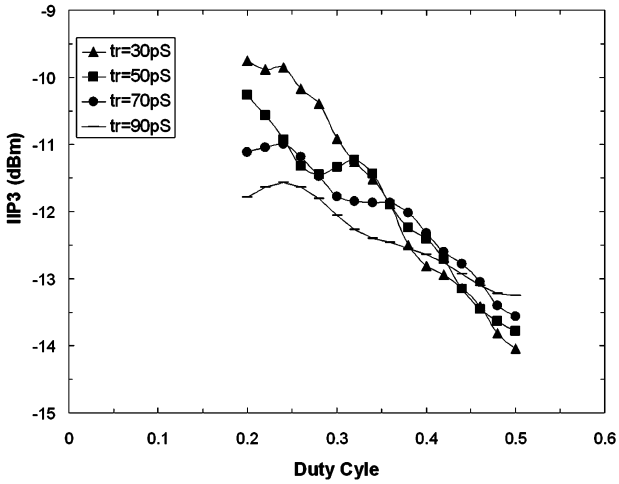

Fig. 15. Simulated IIP3 (10 and 20 MHz) versus LO duty-cycle and LO rise-time (tr = 30, 50, 70 and 90 pS).

measurements are not sufficient to prove W-CDMA SAW-less operation.

With 25% duty-cycle LO, the 0° and 180° pulses and 90° and 270° pulses cannot cross even with non-ideal rise time, since they are not binary complements as shown in Fig. 11, thus avoiding the problems mentioned above. There is also more room for threshold adjustment since the DC average of the LO pulses is lower relative to the max LO signal level making the I and Q mixer performance less sensitive to bias shifts. There is still potential for some crossover of the 90 degree pulses with non-ideal rise time, however since neither the I or Q mixer outputs are shorted the effect is minimal.

Compared to 50% duty-cycle, the DC induced currents are lower since the impedance in the current path is higher, due to the higher effective resistance. The flicker noise voltage, modeled at the input of the mixer device, will have less contribution to overall noise after commutation for a 25% duty-cycle system since the Fourier coefficients have lower relative magnitude and the RF input current signal contribution is relatively larger, resulting in larger signal to noise.

The parallel combination of the output LNA impedance and the off branch impedance is also relatively higher and the parasitic capacitance is lower, which improves noise converted to baseband. The effective resistance looking into the output of this current driven mixer with 25% duty-cycle LO is higher so the flicker noise and opamp noise will be amplified less due to a change in the feedback factor as seen by the input-referred noise voltage of the opamp.

All of these attributes result in improved 1/f performance even with large blocking signals. Fig. 14 shows simulation results of the receiver spot noise figure (at 1 kHz IF) with −26 dBm TX signal present, which is typically dominated by 1/f noise. This plot shows that the spot NF, or 1/f noise, is significantly improved by 15 dB using this core receiver topology with 25% LO duty-cycle compared to 50% LO duty-cycle.

The improvement in third-order and uncalibrated second-order intermodulation distortion, with large modulated TX leakage present, is understood with the same explanation above. Also, the switched parasitic capacitance mixer source which contributes to IIP2 [7], will also be less since one of the quadrature mixer branches is off while the other is on. A 15 dB relative improvement in uncalibrated IIP2 was seen in simulation using this topology with reduced duty-cycle LO. Since mismatches in mixer devices that contribute to IIP2 can be modeled with a DC offset it is logical that compensating offset using this mixer structure for IIP2 calibration with a complex algorithm can maximize IIP2. The linearity of the current driven mixer is also enhanced since there will not be a voltage swing across the switching transistors and across the non-linear parasitic capacitors at the switching pairs input. Providing low impedance at the output of the current driven mixer also eliminates voltage swing at that node which could otherwise cause intermodulation distortion. Fig. 15 shows simulation results of the receiver two-tone (10 and 20 MHz) IIP3 versus LO duty-cycle. The results show that the receiver IIP3 performance is improved significantly with 25% duty-cycle compared to 50% duty-cycle. Noise and linearity are further optimized by adjusting the reference threshold bias at the mixer gates.

C. 25% Duty-Cycle Quadrature Generator With Threshold Adjust

The quadrature generation circuit distributes in-phase and quadrature local oscillator (LO) signals for the receiver. It consists of programmable frequency dividers that generate 25% duty- cycle rail-to-rail LO signals with worst case rise time of 50 pS at 2.17 GHz. In addition it generates a programmable reference voltage level (threshold adjust) to be used by the IIP2 calibration circuit. This allows an optimal bias to be applied to the mixer gate for linearity and noise improvement. The supply of the quadratue generator is provided through a programmable regulator that can be adjusted to relax current drain at reduced TX power levels. A simplified schematic of the quadrature generator, without crossover correction, threshold adjustment and current control is shown in Fig. 16.

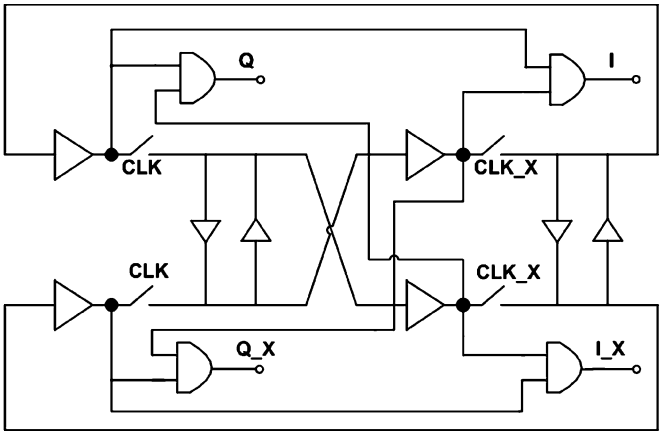

Fig. 16. Simplified quadrature generator schematic—crossover correction, threshold adjust and current control not shown (patent pending).

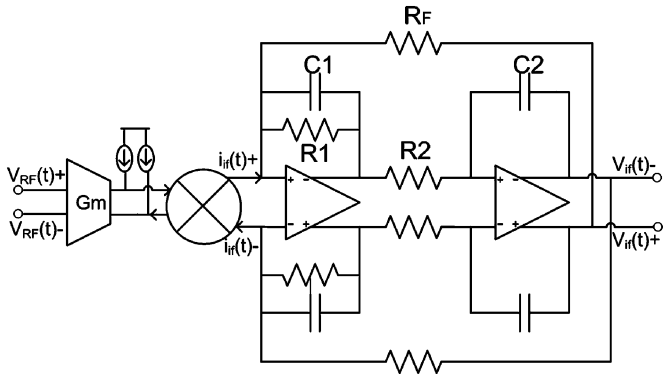

Fig. 17. Simplified schematic of direct coupled current-input filter (DCF) shown after the mixer (patent pending).

D. Direct Coupled Current-Input Complex Filter

The output current of the mixer circuit for IIP2 calibration is input into a current-input direct coupled filter (DCF), with complex poles as is shown in Fig. 17. The bandwidth of the DCF is large enough to maintain low impedance at the differential output (virtual ground nodes) of the mixer across the whole channel band such that the signal current is sent to the feedback resistors. The low impedance for the channel bandwidth is achieved with the feedback structure of the Biquad which creates a virtual ground node at its inputs. In order for the current-input structure to operate with optimum linearity at all frequencies there can be no voltage signal at the virtual ground nodes of the mixer. To provide a low impedance to high frequencies (LO, and LO harmonics generated) shunt capacitors to ground are provided at the mixer output nodes (included within the mixer symbol as in Fig. 12). This allows for the high frequency currents to be filtered out and not be converted to voltages.

If the capacitors were not provided a voltage swing would exist at the input of the DCF due to limited capability of the opamps at high frequencies, which would degrade linearity and degrade LO to IF isolation. The low input impedance to ground at high frequencies and low impedance for channel frequencies at the virtual ground nodes improves linearity and eliminates distortion associated with large signal voltage swings that can occur at a high impedance node. The DCF structure also converts the input current back into a voltage. Approaches that do not use the shunt capacitor are limited by the open loop gain of the transimpedance operational amplifier [26]. The feedback resistor of the DCF (R_F), G_M of the TCA and passive gain at the input of the transconductance amplifier set the conversion gain (CG) of the receiver as follows:

$$CG = \frac{v_{IF}}{v_{RF}} = \frac{2\sqrt{2}}{\pi} G_M R_F Gain_{passive}. \tag{34}$$

The DCF eliminates the need for a transimpedance amplifier (TZA) commonly used with passive mixers [26], which can result in current drain and die area savings. Providing a complex response helps minimize in-band droop and integrated noise across the bandwidth which is important for inter-stage SAW-less operation. Lower filter peaking and better group delay performance can be achieved when compared to topologies with a transimpedance amplifier followed by a biquad. This is due to the fact that the transimpedance amplifier typically has a pole in the modulation bandwidth and the peaking associated with this is compensated in the following baseband filter. The pole in the modulation bandwidth helps linearity but adds noise when integrated over the bandwidth and the peaking can contribute to group delay variation which can affect receiver EVM.

The DCF is similar to a Tow-Thomas biquad [27] topology and is used to realize a pair of complex poles. This topology was chosen for its parasitic insensitive properties and ease of filter corner tuning. The corner of the 3G filter needs to be tuned to a tolerance of $\pm 6\%$ in order to meet 3G RX EVM requirements. This is achieved via factory resistor trimming and digitally assisted calibration of the capacitors. The DCF bandwidth is also selectable between wideband 3G settings and narrowband 2G settings. This is easily done by switching of the capacitors. A significant deviation from the classic Tow-Thomas biquad is the fact that the input resistor is removed. Removing the resistor results in improved noise since this is a large contributor to noise in a classical biquad structure. In this way the DCF provides a virtual ground to the mixer output ports, which results in optimal linearity. Leaving a resistor in series with the input opamp would add noise and allow a potentially large voltage swing, which would exacerbate intermodulation distortion. The DCF also incorporates a linearity-on-demand function in the first integrator of the biquad. The current in the class-A output stage can be adjusted based on blocker conditions to save power.

$$T_{LPF}(s) = \frac{-H\omega_0^2}{s^2 + \left(\frac{\omega_0}{Q}\right)s + \omega_0^2} \tag{35}$$

$$T_{BPF}(s) = \frac{-H\left(\frac{\omega_0}{Q}\right)s}{s^2 + \left(\frac{\omega_0}{Q}\right)s + \omega_0^2} \tag{36}$$

$$H = gm_{TCA} \times R_F \tag{37}$$

$$\omega_0 = \sqrt{\frac{1}{R_2 R_F C_1 C_2}} \tag{38}$$

$$Q = \sqrt{\frac{R_1^2 C_1}{R_2 R_F C_2}}. \tag{39}$$

To minimize receiver gain variation, the DCF shares a constant-g_m bias circuit reference from the TCA. The tradeoff is lower gain variation over process, voltage, and temperature for more variation in DC current.

E. Variable Gain Baseband Amplifier

The main purpose of the baseband amplifier (BBA) is to provide gain and gain control. The gain of the BBA helps reduce impact of ADC noise on the overall noise figure of the receiver. The BBA provides 27 dB of gain control range in 3 dB steps. The BBA also provides an additional pole of filtering and an injection point for the DC offset correction loop. The pole frequency is programmable between 2G and 3G mode.

F. DC Offset and IIP2 Correction System

The DC offset correction system is a critical component for Zero-IF receiver design. There are two DC offset correction systems employed, coarse DC offset correction system and fine DC offset correction system. The coarse DC offset correction system preserves the dynamic range of the analog blocks. The coarse DC offset correction is performed during the receiver warm-up process to remove DC offset of the analog circuits. The offset correction voltage is applied using a 6-bit DAC at the virtual ground of the BBA. The scheme also estimates the correction voltage over the entire gain control range to avoid any transient during baseband gain change. Any residual DC offset after coarse correction is removed in a purely digital fine DC offset correction scheme.

The complex IIP2 of the receiver is one of the most critical specifications to meet for SAW-less operation. To achieve the desired performance over process and temperature, IIP2 calibration is performed during the warm-up process. The IIP2 calibration is done in with automated closed loop routine by injecting calibration signals at the receiver input, setting the DAC offset at the mixer gates, based on an algorithm which is implemented in firmware, detecting the IMD2 components in the baseband and repeating to minimize the second-order distortion component. Calibration tones are generated on chip using the transmit path of the transceiver as shown in Fig. 2. The DAC code is generated in the DSP and fed to the DAC which is embedded in the mixer circuit for IIP2 calibration as shown in Fig. 12. The calibration circuit is capable of achieving a higher complex IIP2 than the minimum required 58 dBm (assuming one data channel), without a correction factor, to guarantee manufacturability. Two-tone IIP2 simulations of the receiver versus correction DAC settings are shown in Fig. 18. The results show that the circuit is capable of achieving a calibrated IIP2 of greater than 100 dBm. Very high IIP2 is shown even at the outer/unoptimized DAC codes. For GSM requirements where the modulated blocker is at 6 MHz from the receive band (AM suppression) the IIP2 requirement is not as stringent and no IIP2 calibration is necessary.

Calibration techniques can be used to improve receiver IP2. However, if the I channel is corrected first followed by the Q channel, the I channel code will no longer be optimal. This is due to the fact that in conventional receivers where I and Q mixers are connected at the RF port, an offset and imbalance introduced on one channel will be up converted and amplify the total offset/imbalance on the other channel [16]. This effect was captured in Fig. 7. DC blocking capacitors do not stop the interaction. To avoid this problem, both mixers are optimized at the same time by using an algorithm to find the optimal DAC code for each mixer which yields the highest composite IIP2. Optimizing the composite value is important since the total IIP2 will be at best 3 dB better than the worst of the two channels.

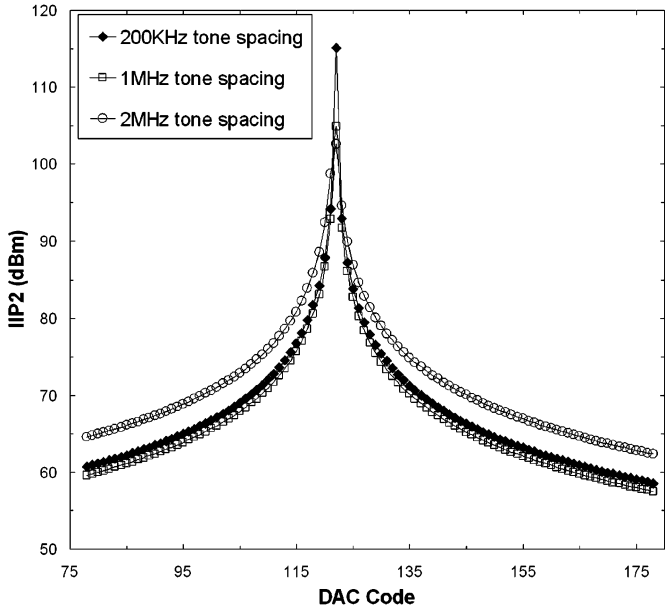

Fig. 18. Simulated IIP2 versus DAC code showing approximately 104 dBm IIP2 using 1 and 2 MHz two-tone spacing at 190 MHz offset.

IV. LAYOUT

A. Floorplan

The chip micrograph is shown in Fig. 19. The receiver lies at the upper end of the die while the transmitter is positioned at the left side, and the digital transceiver, ARM7 and SPI logic is placed in between. The two VCOs are placed at opposite ends of the die to reduce remodulation effects.

B. Isolation

Due to the full duplex nature of WCDMA systems, it is crucial to have a carefully considered die level isolation strategy. There are three main components to the strategy used in our design: distance, substrate isolation structures, and supply partitioning.

First, the distance between the noise generators and susceptible circuits was made as large as possible. This resulted in the transmit outputs, receiver inputs and both VCOs being placed on the periphery of the die, with the corresponding (RX/TX) ports and the RX and TX VCOs being situated at the greatest distance possible. The remaining baseband and support circuitry was then placed in the middle of the die.

In order to prevent degradation in the RX sensitivity, noise in the RX band should not exceed -114 dBm within a 3.84 MHz bandwidth. With 28 dBm power out of the power amplifier and 47 dB TX to RX duplexer isolation (in the RX band) it can be calculated that the on-chip isolation between the RX

TABLE II
MEASURED RECEIVER PERFORMANCE IN 3G MODE (DIGRF OUTPUT)

Parameter	Measured	Specification	Unit
Voltage Gain	61.5	60 +/- 2.5	dB
Noise Figure (Simplex)	2.2	3.0	
Noise Figure (Duplex)	2.39	3.6	dB
NF due to +/- 10 and +/- 20 MHz blockers (IM3 effect)	3.75	7.6	dB
IIP2 due to TX (-190 MHz offset)	> +90 dBm	+58 dBm	dBm
NF due to Adjacent Channel Blocker at +/- 5 MHz	4.7	18.6	dB
NF due to half-duplex IM3	4.1	7.6	dB
NF due to full-duplex IM3	4.2	7.6	dB

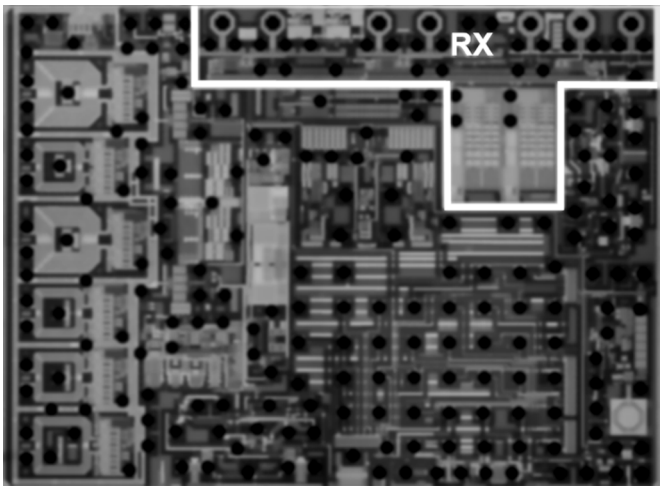

Fig. 19. Die microphotograph of 10-band WCDMA/HSPA, 4-band GSM/EDGE SAW-less radio with DigRF interface.

and TX VCOs must be greater than 95 dB. By using isolated p-wells, p+ guard rings and placing enough distance between the RX and TX VCOs it was possible to achieve such isolation. The floor plan was designed to provide 4 mm between the two VCO coils. At this distance the EM simulation predicts isolation greater than 105 dB.

Second, the transceiver was designed in an all CMOS process that permits the use of isolated p-wells as isolation structures. Circuits that use the isolated p-well have a dedicated metal runner for the n-well bias connection, which connects back to the circuit supply at the die pad. The isolated p-well region back gate bias shares the same ground lines as the circuit. Guard rings (p+) were also placed in the substrate outside the n-well, to help shunt extraneous signals to ground. Dedicated pads were used for the p+ guard rings for a clean ground bias. The analog circuitry was shielded from the digital substrate noise by placing the digital cores inside isolated p-wells.

Finally, the supplies/grounds were partitioned according to either receiver or transmitter sections and then sub-function RF, baseband, frequency generation, and digital. Since unwanted ground loops are notorious for causing signal isolation problems, a conservative approach was taken to create as many supply regions as possible without increasing the die area. In total there were 23 ground/supply pads dedicated to different parts of the receiver. This arrangement was also used to optimize the external supply bypassing for each circuit.

V. MEASURED RECEIVER RESULTS

Measurement results, out of the DigRF interface, referred against several key WCDMA specifications are summarized in Table II. Band I (2110–2170 MHz RX) performance is presented in this Table and chosen for illustrating detailed measured results of WCDMA/HSDPA simplex and duplex noise performance because it has the highest frequency and has the most stringent reference sensitivity requirement. Measured results for duplex and half duplex performance are presented for all bands in this section. Cross-modulation performance is presented for all bands except Band I, where there is no narrowband blocker intermodulation requirement. Key GSM/EDGE measured results are presented for bands II/III.

The zero-IF output spectrum after digitization in the absence of modulated TX leakage is shown in Fig. 20. The desired RF signal was injected at a level of -90 dBm at the IC input. Simplex noise figure, for the full receiver to the DigRF output, was measured to be 2.2 dB. The zero-IF spectrum out of the DigRF measured with a modulated uplink (UL) TX signal of -24.5 dBm at the input of the IC is shown in Fig. 21. The duplex noise figure measured at the DigRF output was 2.39 dB. The simplex and duplex noise figure of the core receiver will be 0.2 dB better than this data since the noise contribution of the DC offset correction, IF amplifier and ADC add 0.2 dB to the total noise figure. As observed from the plots, the total NF degradation attributed to reciprocal mixing and IIP2 is 0.16 dB.

Worst case complex (I and Q) IIP2 performance measured using two CW tones at -190 MHz offset with 1 MHz spacing for Band I after calibration for 13 IC samples taken from two different wafers is shown in Fig. 22 to be > 90 dBm. Since the specification is based on two-tone IIP2, no correction factor was added to this data to approximate modulated IIP2 performance which would be higher by the correction factor achieved. The performance is similar for all bands. A measured 3D-surface plot describing the relation between two-tone complex IIP2 and all possible calibration DAC settings in I and Q paths is shown in Fig. 23. From this plot it can be seen that the uncalibrated IIP2 is also very high. The optimization algorithm steps through a small number of settings for the 8-bit DACs to arrive at the maximum IIP2 condition. As noted in the graph, this is better than +90 dBm. IIP2 improvement after calibration was found to be at least 25 dB. The optimal IIP2 contours are wide and the calibration performance holds up very well over frequency and over temperature.

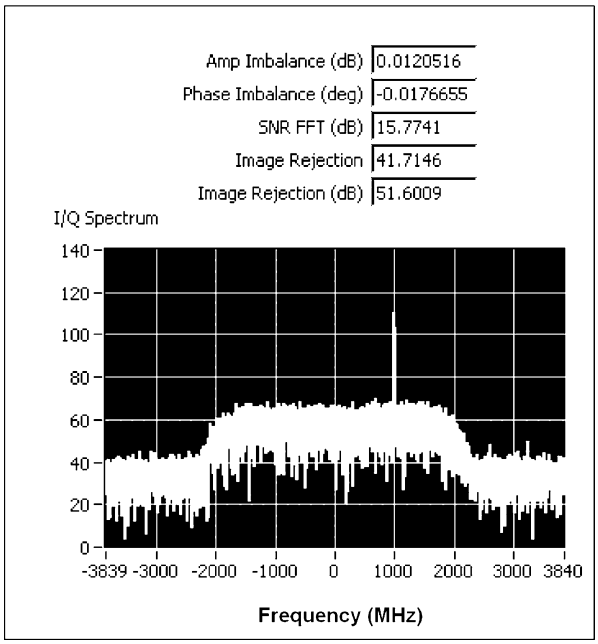

Fig. 20. Measured 3G Band I Simplex NF at DigRF output. Input signal $=$ -90 dBm, input noise $=$ -108 dBm, $\mathrm{SNRin} = 18$ dB, $\mathrm{SNRout} = 15.77$ dB, Simplex NF $=$ 2.2 dB.

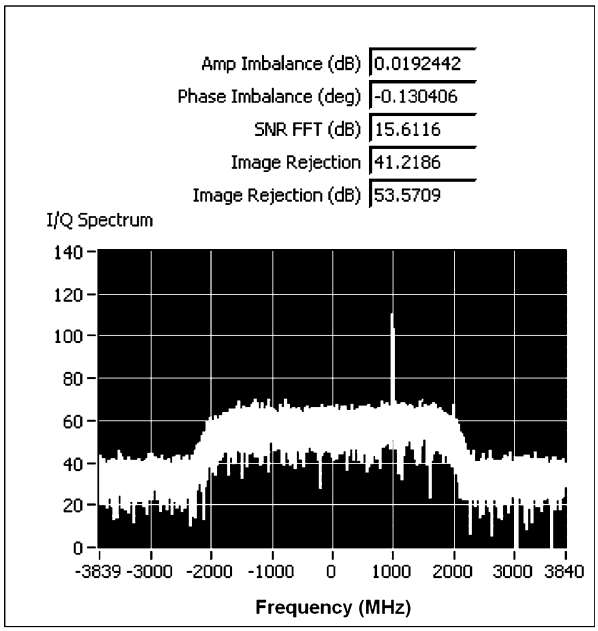

Fig. 21. Measured 3G Band I Duplex NF ($\mathrm{PTX} = -24.5$ dBm) at DigRF output. Input signal $=$ -90 dBm, Input noise $=$ -108 dBm, $\mathrm{SNRin} = 18$ dB, $\mathrm{SNRout} = 15.61$ dB, Duplex NF $=$ 2.39 dB.

Noise performance in the presence of TX with a half-duplex image or full-duplex image blocker present for all the receive bands in WCDMA mode are shown versus specifications in Fig. 24. The transmit signal was injected at 5 dB below maximum power for these tests. It is to be noted that the data presented in Fig. 24 is based on parts measured before IIP2 calibration, thereby reflecting more NF degradation due to TX than during optimal IIP2 operation. Since the duplex spacing varies per band, the full duplex noise figure can be lower than the

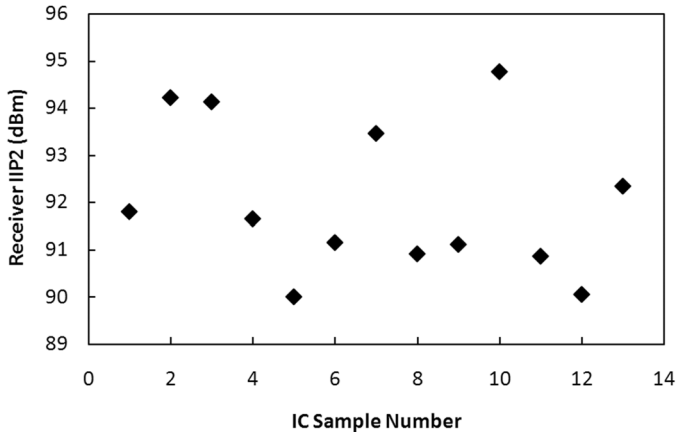

Fig. 22. Measured receiver two-tone complex IIP2 (auto-calibrated) for multiple samples showing IIP2 $>+90$ dBm.

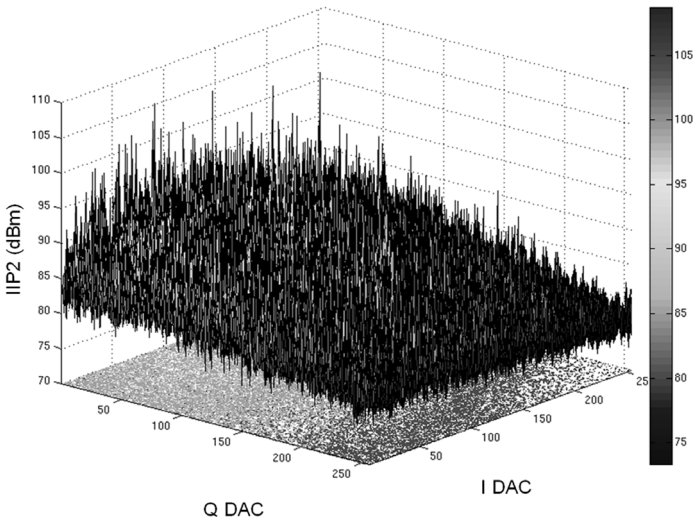

Fig. 23. Measured 3G RX two-tone IIP2 for all possible DAC settings showing >95 dBm complex IIP2 at optimum DAC codes (1 part).

half-duplex noise in some cases. For Band I measured full-duplex and half-duplex image IIP were $+5$ dBm and -1 dBm, respectively across the band.

Transfer of the transmit signal modulation onto a close-in blocker is captured in the cross-modulation noise figure plot in Fig. 25, for all receive bands except Band I which does not have such a test specified.

A summary of GSM/EDGE performance parameters in Band II/III (1805–1880 MHz/ 1930–1990 MHz) is reproduced in Table III. A spectral plot with output SNR at LO frequency of 1930.2 MHz (Band II), is shown at the baseband digital interface in Fig. 26. The desired RF input signal is injected at -100 dBm. A plot showing the DCS/GSM noise performance of the receiver in the presence of the specified CW, EDGE and adjacent channel GMSK blockers is presented in Fig. 27.

All measurements were with performed with parts inserted into a compression mount fixture, which was soldered to an evaluation board (EVB). Further improvements in performance are expected with a part soldered down directly to the EVB.

The total current drawn by the receiver core in UMTS/ WCDMA or PCS/GSM mode is 15.1 mA for high band in

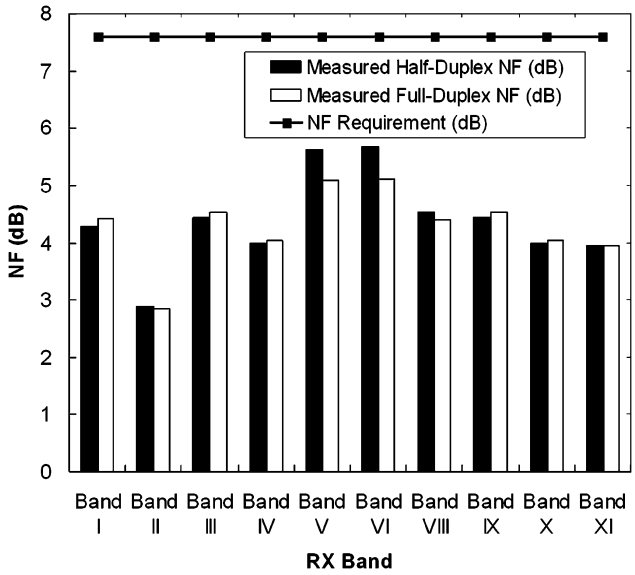

Fig. 24. Measured 3G receiver duplex-image and half-duplex image performance for all bands (IIP2 uncalibrated).

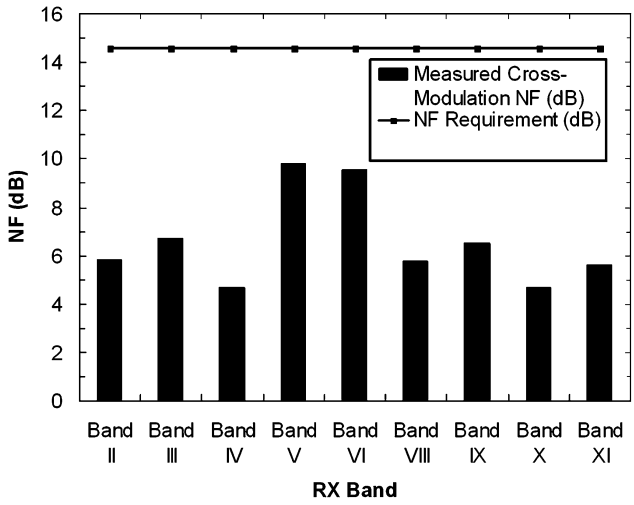

Fig. 25. Measured 3G receiver cross-modulation performance (IIP2 uncalibrated).

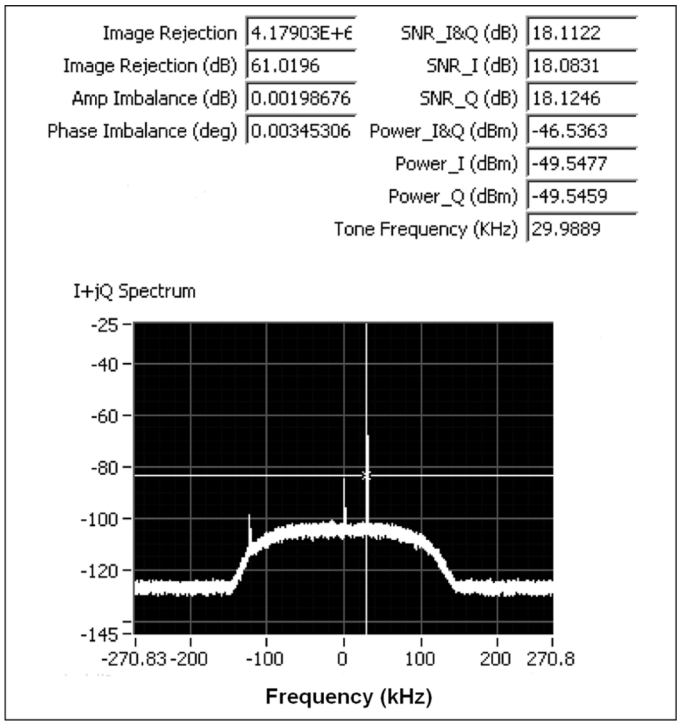

Fig. 26. Measured 2G Band II receiver NF. Input desired signal $= -100$ dBm, Input SNR $= 21.3$ dB, output SNR $= 18.11$ dB, Simplex NF $= 3.19$ dB.

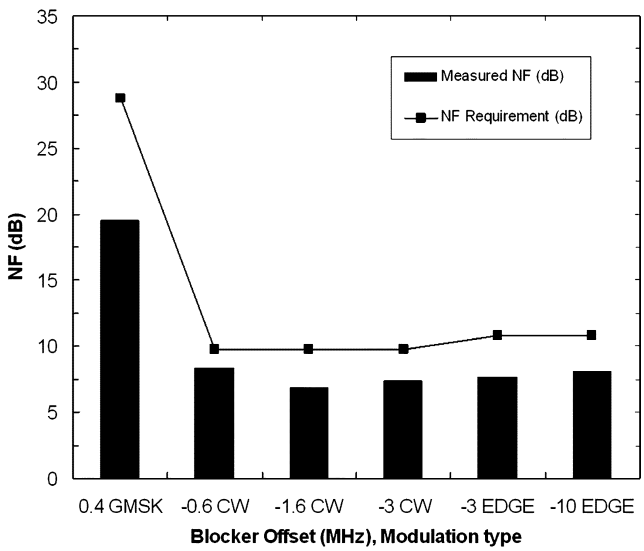

Fig. 27. Receiver 2G/2.5G blocker performance.

the presence of maximum transmitter power as delineated in Table IV. The baseband amplifiers (total I and Q) draw 2.0 mA and the quadrature generator draws 7 mA including LDO current. The current can also be reduced in DRX mode, via SPI control of the receiver blocks. This is possible since the noise due to reciprocal mixing, TX noise in receiver band and IM due to IIP2 are a function of the TX power level.

The WCDMA measured simplex/duplex NF of 2.2/2.4 and minimum complex two-tone IIP2 $(> 90$ dBm$)$ are better than that reported in state-of-the art WCDMA [4]–[6] integrated receivers as shown in Table V. The 22.6 mW power consumption for the core receiver circuits compares favorably to the next lowest power consumption of 75 mW in [5]. Half duplex and full-duplex IIP3 data significantly exceeds the -6 dBm specification and compares favorably to the other references. Even with 60 dB gain this receiver exhibits higher minimum input-referred minimum IIP2 than that of the state-of-the-art mixer in [7] which has $+78$ dBm IIP2 and 16 dB voltage gain.

VI. Conclusion

An inter-stage SAW-less 10-band WCMDA (UMTS)/HSDPA 4-band GSM/EDGE receiver with 3G DigRF has been presented which is part of a single chip SAW-less (RX and TX) reference platform radio IC for smartphones IC. A new core receiver implementation has been shown that has significant advantages in noise, intermodulation distortion and large signal handling capability and is a key enabler for

TABLE III
MEASURED RECEIVER PERFORMANCE IN 2G MODE (DIGRF OUTPUT)

Parameter	Measured	Specification	Unit
Voltage Gain	55	54.5 +/- 3	dB
Noise Figure (PCS)	3.2	4.8	dB
NF due to +/- 0.8 and +/- 1.6 MHz blockers (IM3 effect)	7.2	7.8	dB
Calibrated Image Rejection at -220 kHz offset	> 60	45	dB
NF due to +/- 6 MHz offset GMSK blocker (AM suppression test)	3.8	7.8	dB

TABLE IV
CORE RECEIVER BLOCK CURRENT DRAIN

RX Block	Current Drain	
	High Band	Low Band
TCA	6.6 mA	4.5 mA
Mixer	0 mA	0 mA
Baseband Filters (Total I and Q)	8.5 mA	8.5 mA
Total	15.1 mA	13.0 mA

TABLE V
WCDMA RECEIVER PERFORAMNCE COMPARISION

Design	Simplex NF (dB)	Duplex NF (dB)	TX Power (dBm)	2-Tone IIP2 (dBm) Without Correction Factor	Half Duplex IIP3 (dBm)	Full Duplex IIP3 (dBm)
[4]*	4.9	-	-29	38.8	-7.4	-
[5]	2.9	-	-	49.5	-7	-4
[6]	-	3.1	-25	>65	-	-
This Work **	**2.2**	**2.4**	**-24.5**	**>90**	**-1**	**+5**

* Duplex sensitivity at IC < -109.5dBm. With 2.5dB duplexer loss as described in paper, duplex noise figure = 6.2dB.
** Noise measured out of DigRF interface after ADC and digital transceiver. Complex 2-tone IIP2 is reported.

SAW-less 3G operation. An automatic on chip calibration routine with complex algorithm is used to achieve best-in-class IIP2 performance. Inductive chokes and high Q tuned external components are not used in the TCA load to reduce die size are improve manufacturability, respectively. The full receiver, as measured at the output of the DigRF, achieves 2.2 dB simplex noise figure, 2.39 dB duplex noise figure (at −24.5 dBm TX leakage power), minimum two-tone complex IIP2 of +90 dBm and 60 dB gain. The core receiver consumes only 22.6 mW. The IC has been implemented in a 90 nm CMOS process and uses flip-chip technology.

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Daniel L. Kaczman (M'94) was born in Westfield, MA, in 1962. He received the B.S.E.E. degree from the University of Massachusetts, Amherst, in 1984, and the M.S. degree in electrical engineering from California State University, Northridge, in 1987.

In May 2008, he joined Texas Instruments, Dallas, TX, where he is currently an IC Design Manager and Technical Director working on CMOS SOC wireless products. From 2004 to 2008, he worked at Freescale Semiconductor in Kemper, IL, where he was the 3G Transceiver IC Design Manager and IC Design Lead. Before leaving, he was involved in architecture and was a core team IC Design Lead of a CMOS SAW-less cellular transceiver IC with DigRF interface. He successfully also led the design of two 3G transceiver ICs (MC13821, MC13822), and his department was responsible for the design of three WCDMA/GSM/EDGE transceiver reference platform modules: MMM6017, MMM6007, and MMM7210 used in the i.300–20/21, i.300–30 and MXC300–31 architectures. From 1998 to 2004, he worked for Motorola where he was a Design Manager and led the initial 3G/2G RF reference platform architecture system design. He followed through as Design Lead for Motorola's first tri-band WCDMA direct conversion receiver production IC (MC13778) and has participated in four generations of 3G platform design. In 1994, he helped start up the RF/Mixed Signal IC Design Department for Ericsson in RTP, NC, and was the Technical Manager until 1998. There he successfully managed the design of several cellular ICs including a direct-launch transmitter, multi-band RF receiver and low-IF receiver. Prior to this, he was a Senior RF/Mixed Signal IC Design Engineer at Allied Signal in Maryland, where he was involved in broadband synthesizer and CMOS GPS receiver work. From 1990 to 1994, he was a Senior RF IC Design Engineer at Raytheon in Massachusetts. There he worked on the design of commercial fully integrated single and dual-channel direct broadcast satellite (dBS) receivers, six integrated multi-stage high-efficiency linear power amplifiers, miniature transmit-receive modules, integrated-filter and GPS circuits. From 1984 to 1990, he worked for GM/Hughes Electronics, El Segundo, CA, where he was involved in the design and development of RF/analog and digital integrated circuits, signal conditioning subsystem integration, and flight-hardware module design for the F-15 Fighter diversity phased-array imaging radar.

Manish Shah (M'96) received the B.S. degree in electrical engineering from the University of Illinois at Chicago, Chicago, IL, in 1996, and the M.S. degree in electrical engineering from National Technological University, Fort Collins, CO, in 2003.

He joined Motorola Inc., Libertyville, IL, in 1996, as an RF Design Engineer, where he worked on cellular radios based on AMPS, IS136, and GSM standards. In 2001, he joined the Wireless IC design group, now part of the Cellular Product Group of Freescale Semiconductor, Lake Zurich, IL, where he has been involved in architecture and design of CMOS SAW-less cellular transceivers. Currently, he is a Senior Staff IC Design Engineer working on next-generation transceiver design for 3G chipsets. His research interests include the system architecture and design of high-performance RF, analog and mixed-signal integrated circuits for wireless communication.

Mohammed Alam was born in Rangpur, Bangladesh, in 1973. He received the B.S. degree in electrical engineering from Bangladesh University of Engineering and Technology (BUET), Dhaka, in 1997, and the M.S. degree in electrical engineering from the University of Florida, Gainesville, in 2001.

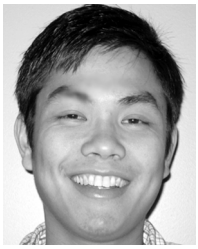
Currently, he is a Senior Design Engineer with Freescale Semiconductor, Lake Zurich, IL. His research interests are in RF, analog and mixed-signal integrated circuits and systems for wireless communications.

Mohammed Rachedine received the Ph.D. degree in electrical engineering from the University of Rhode Island in 1991.

He joined Computer Imaging Reference Systems in Norfolk, VA, as a Development Engineer in the Digital Signal Processing Lab, to which he later became a consultant. In 1991, he also joined the Faculty of Electrical Engineering at Hampton University, Hampton, VA. In 1997, he joined Motorola Personal Communication Sector Research Lab. Currently, he is with Freescale Semiconductor, Wireless and Mobile Systems Group, Lake Zurich, IL. His current interests include RF, analog and mixed-signal integrated circuits and systems for wireless communication.

David L. Cashen (M'96) was born in Hammond, IN, in 1971. He received the B.S. degree in electrical engineering from Purdue University Calumet, Hammond, IN, in 1994, and the M.S. degree in electrical engineering from National Technological University, Fort Collins, CO, in 2002.

In June 2008, he joined SiRF, preceding which he was a Senior Staff Engineer with Freescale Semiconductor's Radio Products Division, Lake Zurich, IL. His research interests include the design of analog and mixed-signal circuits for wireless applications.



Lu M. Han (M'01) was born in Yangon, Myanmar (Burma). He received the B.S. degree in electrical engineering from Iowa State University, Ames, in 2000.

Currently, he is a Senior IC Design Engineer at Freescale Semiconductor's Radio Products Division in Lake Zurich, IL. He is involved in RF and mixed-signal circuit designs for wireless applications.

Anand Raghavan (M'01) was born in Chennai, India, in 1979. He received the B.S. degree in electrical engineering from the Indian Institute of Technology, Chennai, in 2001, and the Ph.D. degree in electrical and computer engineering from the Georgia Institute of Technology, Atlanta, in 2007.

Currently, he is an IC Design Engineer with Freescale Semiconductor's Cellular Products Group in Lake Zurich, IL. His professional interests encompass the design of RF and mixed-signal circuits for wireless applications.