A 1.2-GS/s 8-bit Two-Step SAR ADC in 65-nm CMOS with Passive Residue Transfer

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***Abstract*—A hybrid 2b-1b/cycle, two-step asynchronous SAR ADC exploiting the passive residue transfer technique is reported in this paper. The removal of the residue amplifier results in much savings in the time and power consumed for the residue transfer process. Moreover, the 2b-1b/cycle conversion scheme assisted by the asynchronous time allocation during the bit cycles further enhances the conversion speed. Fabricated in a 65-nm CMOS process, the prototype ADC measured an SNDR of 43.7 dB and an SFDR of 58.1 dB for a near Nyquist input. The total power consumption of the ADC is 5.0 mW and the achieved FoM is 35 fJ/conversion-step, all measured at a sample rate of 1.2 GS/s.**

***Index Terms*—2b-1b/cycle, passive residue transfer, SAR ADC, two-step**

I. Introduction

Communication systems such as ultra-wideband radios, serial link and broadband Ethernet transceivers demand high-speed and medium-resolution analog-to-digital converters (ADCs) with low power consumption. The successive-approximation-register (SAR) conversion architecture is an attractive option for these applications due to its low analog complexity and excellent power efficiency. However, compared to the flash and pipeline architectures, the serial conversion process of the SAR ADC still dramatically limits its conversion speed. In recent years, a few speed-acceleration techniques for non-interleaved, single channel SAR ADC have been reported [1]-[5], which will be briefly reviewed next.

First, resolving multiple bits in each conversion cycle is a popular way of increasing the ADC throughput [1], [2]. Ideally, the speed of a multi-bit SAR ADC could be improved by a factor equal to the number of bits resolved in each cycle. One drawback of this architecture is that its resolution is restricted by the comparator offset—just like the flash ADC, it is necessary to limit the comparator offset to less than half an LSB in each conversion cycle to avoid any gross conversion errors. In addition, a multi-bit SAR ADC also requires two digital-to-analog converters (DACs), a signal DAC (SIG-DAC) and a reference DAC (REF-DAC). The former is employed to perform the sampling and successive approximations of the signal, while the latter is to supply the (multiple) threshold voltages for all the comparators involved during bit cycles. Naturally, this setup invites a mismatch problem between the SIG-DAC and the REF-DAC [2].

Second, the two-step pipeline SAR is another structural extension to the conventional SAR ADC for breaking the speed limit [3], [4]. Its overall quantization is partitioned into two steps and an accurate amplifier is needed to transfer the residue from the first stage to the second. Typically, the conversion throughput and power consumption of the two-step approach are limited in part by the achievable bandwidth and power efficiency of the residue amplifier, respectively.

In this paper, a two-step SAR architecture exploiting the passive residue transfer technique [6] is presented to push the conversion speed. Thanks to the passive residue transfer, the bandwidth-limited amplifier is removed and a faster residue transfer that also consumes less power is obtained. Additionally, an asynchronous 2b-1b/cycle conversion scheme further improves the conversion throughput. A prototype ADC was designed and implemented in a 65-nm CMOS process. At a sample rate of 1.2 GS/s, the ADC measured an SNDR of 43.7 dB and an SFDR of 58.1 dB for a near Nyquist input while consuming a total power of 5.0 mW, culminating in a conversion figure of merit (FoM) of 35 fJ/conversion-step.

II. Two-Step SAR ADC Architecture

A. Passive Residue Transfer

The architecture of the 2b-1b/cycle two-step SAR ADC with passive residue transfer is illustrated in Fig. 1. Normally, there are two approaches to transfer a residue voltage passively. First, the capacitive DAC (CDAC) of the second stage, after being reset, could be utilized to share the residue charge stored on the first-stage CDAC when the first stage completes its conversion cycles. Potential problems associated with this approach are residue signal attenuation and additional clock phases needed for CDAC reset and charge sharing.

The second method, as shown in Fig. 1, is to employ two CDACs in a ping-pong configuration to alternately transfer the residue from the first stage to the second [6]. The operation principle is depicted by the timing diagram shown in Fig. 2. To begin with, both switches S_1 and S_{2a}/S_{2b} turn on and the input signal is sampled by the CDACs of the two stages. Then S_1 turns off and the first stage starts the coarse conversion cycles. In this period, the second stage A/B is idle and its CDAC just appears as a "parasitic capacitor" to

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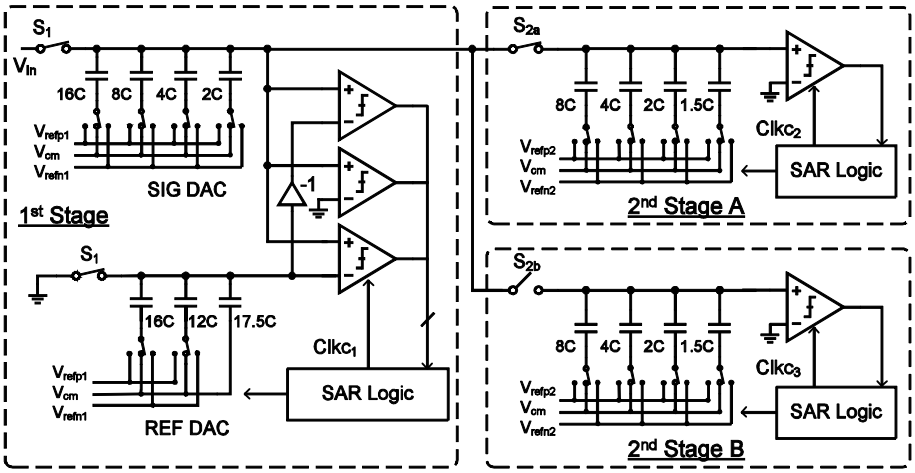


Fig. 1. Architecture of the 2b-1b/cycle two-step SAR ADC with passive residue transfer. Single-ended version is shown for simplicity.

the first-stage. Once the coarse cycles complete, the residue voltage is generated by the first-stage CDAC and the switch S_{2a}/S_{2b} turns off. Finally, the second stage A/B is activated to start the fine conversion cycles. This process is repeated with alternate participation of A and B of the second stage.

For the reason that the CDAC of the second stage participates in the sampling as well as the first-stage cycles, the residue voltage could be transferred immediately when the switch S_{2a}/S_{2b} turns off. Therefore, the second technique doesn't require additional clock phases for residue transfer and reset. Since the residue signal is not attenuated, this technique also provides some SNR benefit. It should be noted that, in this approach, the reference levels of the first stage will be attenuated by the second-stage CDAC during the bit cycles. But for high-speed ADCs, the input signal swing is mainly restricted by the linearity of the S/H instead of the reference swing, so the reference attenuation problem has a minor effect on the overall ADC accuracy.

Because the inter-stage gain of this two-step architecture is ideally unity, the comparator noise of the second stage contributes exactly the same way as in a one-step SAR ADC. Considering that the ping-pong stages work alternately (i.e., one works while the other is mostly idle), the total power of the comparators and the SAR logics are similar to that of the conventional structure without ping pong. Furthermore, as the noise of the three first-stage comparators doesn't contribute to the overall noise budget of the ADC, they are downsized to save power. In summary, even though the ping-pong architecture increases the area overhead of the ADC, this approach does not suffer too much power penalty in comparison to the one-step conventional SAR structure.

Lastly, due to the absence of residue gain, the quantization range of the second stage needs to be scaled down to align with the range of the residue voltage. A large scaling capacitor could be employed in the CDAC of the second stage to downscale the reference voltage [4], which unfortunately enlarges the input capacitive loading dramatically. In this work, a second reference V_{ref2} (equal to $1/16V_{ref1}$) was applied to the second stage, avoiding the large input loading issue.

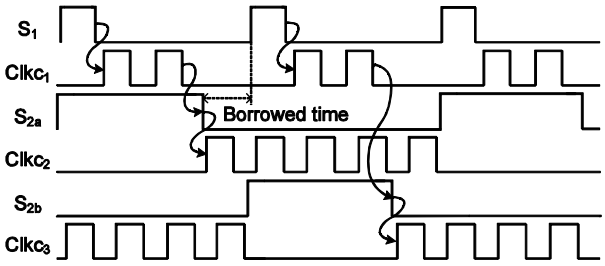


Fig. 2. Timing diagram of the prototype SAR ADC.

B. 2b-1b/cycle Conversion Scheme

From the speed standpoint, making both stages 2b/cycle will probably deliver the highest conversion speed. However, due to the lack of residue amplification, the comparator offsets and the mismatch between the REF-DAC and SIG-DAC in the second stage will make it difficult to achieve the desired resolution. As an alternative, we chose to employ a 1b/cycle second stage in this work, in which the (single) comparator offset does not introduce any DNL errors but merely an input-referred offset. In contrast, as the LSB size of the first stage is much larger (dependent on the partition of the resolution between the first and second stages), the constraints on the comparator offset and DAC mismatch are relaxed, in comparison with those of the second stage in an all 2b/cycle approach.

The resolution partition also affects the overall throughput of the ADC. Considering the 1b overlap between the two stages, there are two options for partitioning: 1) 3×2b for the first stage and 3×1b for the second; 2) 2×2b for the first and 5×1b for the second. While seemingly option 1) is more balanced (i.e., resolving 3 cycles for both stages), the

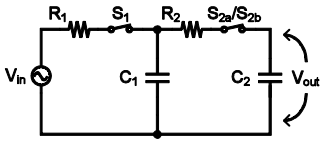


Fig. 3. The equivalent sampling network of the prototype ADC.

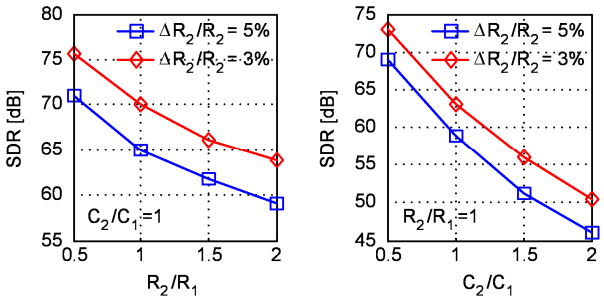


Fig. 4. Simulated signal-to-distortion ratio (SDR) of the sampling network shown in Fig. 3.

more complex 2b/cycle operation consumes more time than the 1b/cycle counterpart, and besides additional time needs to be allocated to the first stage for sampling. Thus, for option 1), the speed bottleneck would be in the first stage. In this work, computer simulation reveals that the maximum throughput for option 1) is limited to 1 GS/s.

The prototype ADC is realized with option 2), in which the second stage is limiting the overall conversion speed. Fortunately, the asynchronous time allocation enables time borrowing and somewhat relieves the timing burden of the second stage. This is depicted in Fig. 2, wherein once the last cycle of the first stage completes, a residue transfer is triggered and the corresponding second stage starts conversion immediately after that. Typically, the two conversion cycles of the first stage finish before the next sampling edge arrives, thus the rest of the time is allocated to the second stage. In other words, the timing budget of the second stage is extended by the asynchronous time allocation. According to the post-layout simulation, the prototype ADC can be clocked maximally at 1.3 GS/s, which is significantly improved relative to the first choice.

III. Prototype Circuit Design

A. CDACs

Since in this work the second-stage CDAC attenuates the reference voltage of the first stage, it is desirable to choose a small value for the second CDAC. On the other hand, to meet the requirement of kT/C noise, the capacitance of the second-stage CDAC cannot be too small [6]. In this design, we chose a 2:1 ratio for the CDAC values between the first and second stages. A scaling capacitor of 17.5C is added to the REF-DAC of the first stage to obtain a nominally identical reference attenuation factor (Fig. 1).

In addition, we also exploited the fact that the CDACs of the two stages are separate to minimize the capacitance

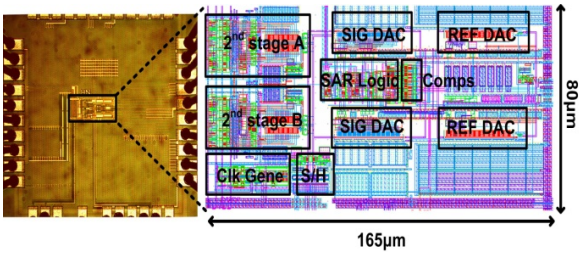


Fig. 5. Die photo.

spread in this work, which is only 8 given an overall 8-b resolution. The unit capacitors in Fig. 1 are realized with fringing metal capacitors of 1 fF. Considering the small total capacitance of 15.5 fF of the second-stage CDAC, it is designed to be a non-binary DAC with the LSB capacitor set to 1.5C to tolerate the comparator kick-back noise.

B. Bandwidth Mismatch of Sampling Network

In the tracking phase, the input signal alternately sees two CDACs of the second stage (i.e., ping pong) through the residue switches S_{2a} and S_{2b}. As a consequence, any mismatch between the two CDACs and/or between S_{2a} and S_{2b} will contribute to the bandwidth mismatch of the sampling network. Fig. 3 shows an equivalent circuit of the sampling network of this ADC, which can be approximated as a first-order system if one time constant is significantly larger than the other [7]. The effective bandwidth is

$$\omega_0 = \frac{1}{R_2 C_2 + R_1 (C_1 + C_2)}. \quad (1)$$

Typically, the mismatch between the MOSFET switches will dominate; hence the induced bandwidth mismatch can be expressed as

$$\frac{\Delta\omega_0}{\omega_0} = \frac{-1}{\frac{R_1}{R_2}(\frac{C_1}{C_2}+1)+1} \cdot \frac{\Delta R_2}{R_2}. \quad (2)$$

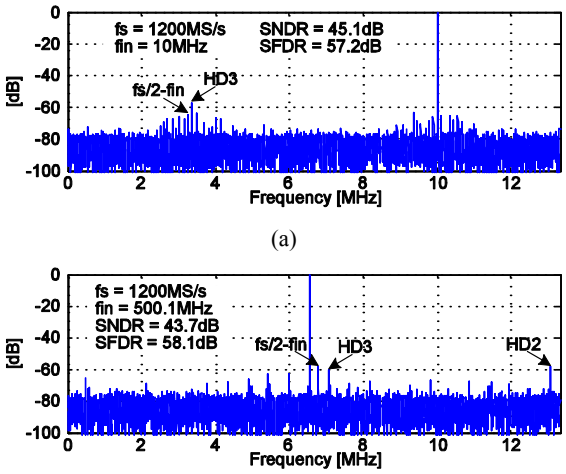
It can be seen clearly that small C_2 and R_2 can alleviate the bandwidth mismatch problem. Circuit simulation results shown in Fig. 4 confirm the above analysis. In this design, C_2 is chosen to be ½C_1 and R_2 is set to be equal to R_1.

C. Comparator

In the prototype ADC, the strong-arm latch is chosen as the comparator with an extra input pair for offset calibration (from off-chip). To reduce the impact of the calibration pair on the speed and noise performance of the comparator, its size is set to ¼ of the main input pair [5]. As the comparator is a critical factor limiting the SAR loop delay, its input common-mode voltage is set to 800 mV to boost the regeneration speed. The input-referred noise of the comparators in the second stage is designed to degrade the overall SNR by no more than 3 dB.

IV. Measurement Results

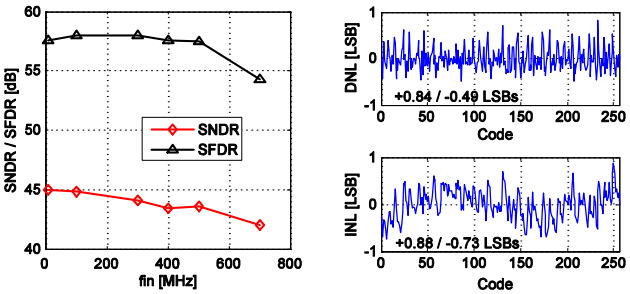
The prototype ADC was fabricated in a 65-nm CMOS process. A die photo is shown in Fig. 5. The ADC occupies



(a)

(b)

Fig. 6. Measured ADC spectra at 1.2 GS/s with (a) a near DC input and (b) a near Nyquist input (both decimated by 45×).



(a) (b)

Fig. 7. Measured (a) SNDR and SFDR at 1.2 GS/s vs. input frequency and (b) DNL and INL profiles.

an active area of 165 µm × 80 µm. In the experiments, with foreground offset calibration for all five comparators shown in Fig. 1, the ADC can be clocked at 1.2 GS/s with a 1.25-V supply while consuming 5.0 mW.

The dynamic performance of the ADC after static radix and ping-pong gain mismatch calibration is shown in Fig. 6; the achieved SNDR is 45.1 dB and the SFDR is 57.2 dB for a 10 MHz input. For a 500.1-MHz input, the measured SNDR is 43.7 dB and the SFDR is 58.1 dB (42.5 dB and 56.8 dB without radix and mismatch calibration, respectively). The spurious tone caused by bandwidth mismatch limits the SFDR to roughly 55 dB near Nyquist, at which the second harmonic also pops up, most likely induced by the phase imbalance between the differential input traces. Fig. 7(a) summarizes the measured dynamic performance.

The measured DNL and INL profiles after calibration are shown in Fig. 7(b). The maximum DNL and INL are +0.84/-0.49 LSBs and +0.88/-0.73 LSBs, respectively. Table I compares this work with some state-of-the-art designs reported recently.

TABLE I PERFORMANCE COMPARISON

Works	JSSC'15 [8]	VLSI'12 [9]	VLSI'12 [10]	JSSC'15 [2]	ISSCC '13 [5]	**This work**	
Architecture	Sub-Ranging	TI-SAR	SAR	SAR	SAR	**SAR**	
CMOS Tech. [nm]	65	65	28	45	32	**65**	
Resolution [bits]	7	8	8	7	8	**8**	
Sample Rate [GS/s]	1.23	1	0.75	1	1.2	**1.2**	
Power [mW]	8.11	4	4.5	7.2	3.1	**5.0**	
Area [mm^2]	0.0875	0.013	0.004	0.016	0.0015	**0.013**	
SNDR [dB]	36.2	42.8	43.2	40.8	39.3	**43.7**	**42.5**†
SFDR [dB]	46.2	58.5	57.5	50.6	50	**58.1**	**56.8**†
FoM [fJ/step]	125	34	41	80	34	**35**	**39**†

† Measured without radix and ping-pong gain mismatch calibration

V. CONCLUSION

In this paper a high-speed, two-step SAR architecture with low power consumption is presented. A passive residue transfer technique is employed to eliminate the time and power consumption associated with residue transfer. A 2b-1b/cycle hybrid conversion scheme utilizing asynchronous time allocation further enhances the conversion speed performance. Fabricated in a 65-nm CMOS process, the prototype ADC achieves an SNDR of 43.7 dB and a FoM of 35 fJ/conversion-step at a sample rate of 1.2 GS/s with a near Nyquist frequency input.

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