Miller Compensation Using Current Buffers in Fully Differential CMOS Two-Stage Operational Amplifiers

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***Abstract*—Several Miller compensation schemes using a current buffer in series with the compensation capacitor to modify the right-half-plane zero in fully differential two-stage CMOS operational amplifiers are analyzed. One scheme uses a current mirror as a current buffer, while the rest use a common-gate transistor as a current buffer. The gain transfer functions are derived for each topology, and approximate transfer-function coefficients are found that allow accurate estimation of the zero(s) and poles.**

***Index Terms*—Compensation, operational amplifiers, poles and zeros.**

I. Introduction

TWO-STAGE operational amplifiers (op-amps) are often used to achieve both high dc gain and large output voltage swing. These op-amps require frequency compensation. When conventional Miller compensation is used in a two-stage op-amp, the compensation capacitor is connected between the input and output of the second gain stage. The compensation capacitor causes the two poles associated with the input and output nodes of the second stage to split apart, giving dominant and nondominant poles that are typically widely spaced. However, the capacitor also provides a feedforward signal path that introduces a right-half-plane (RHP) zero in the op-amp transfer function [1]. This feedforward reverses the polarity of the op-amp gain at a finite frequency by passing the signal directly from the input to the output of the second stage, avoiding the inversion from that stage. This polarity reversal stems from the combination of a -90° phase shift from a left-half-plane (LHP) pole and another -90° phase shift from the RHP zero. The RHP zero is especially important in CMOS technologies that give low device transconductance for a given bias current, causing the magnitudes of the RHP zero and the nondominant pole to be comparable. The RHP zero can be eliminated by adding a resistor [2], [3] or voltage buffer [4] in series with the compensation capacitor, or by adding a transconductance stage to cancel the feedforward signal [5].

Manuscript received April 17, 2003; revised July 12, 2003. This work was supported in part by the University of California under MICRO Grant 01-084 and in part by the National Science Foundation under Grant 9901925.

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Digital Object Identifier 10.1109/TCSI.2003.820254

Alternatively, a current buffer can be connected in series with the compensation capacitor to eliminate the RHP zero or move the zero [6]–[10]. This paper analyzes and compares four current-buffer compensation schemes for fully differential op-amps. Some of these schemes have been analyzed previously for single-ended op-amps. In [7], an ideal current buffer (with zero input impedance and infinite output impedance) was assumed to simplify the analysis. This assumption leads to the conclusion that the zero is eliminated. An analysis using a current buffer with nonzero input impedance shows that the RHP zero is eliminated but a LHP zero exists [8]. The analysis in this paper includes not only nonzero input impedance, but also finite output impedance in the current buffer. A detailed analysis of another configuration was carried out in [9]; however, the transfer function of that single-ended circuit differs from its fully differential counterpart due to the current-mirror load in the input stage of the single-ended op-amp. A current mirror was used as the current buffer in a single-ended folded-cascode op-amp in [10], but the compensation topology used there creates positive feedback when extended to fully differential op-amps. The circuits considered in this paper are balanced and fully differential. Common-mode feedback (CMFB) is ignored for simplicity, but CMFB loading on the differential circuits can be taken into account easily. To simplify the analyzes and the resulting transfer functions, device and parasitic capacitors are lumped into capacitors that connect from each circuit node to ground, as is often done [1], [7], [8], [10]–[12]. In all the circuits, the transistors operate in the saturation region. To simplify the schematics, ideal current sources are shown instead of transistor current sources; however, the effects of finite output impedance in these current sources can be included as presented in the paper.

This paper is divided into four additional parts. Section II analyzes the connection of the compensation capacitors to common-gate stages acting as current buffers. The circuits in this section are known, but the analyses here are new because they consider nonzero input impedance and finite output impedance for the current buffers and because these buffers are applied to fully differential op-amps. Section III presents and analyzes the use of a differential current mirror as a current buffer. Section IV gives the conclusion. The appendices show the analysis details.

II. Common-Gate Stages

This section analyzes the connection of the compensation capacitors to three current buffers that use a common-gate configuration.

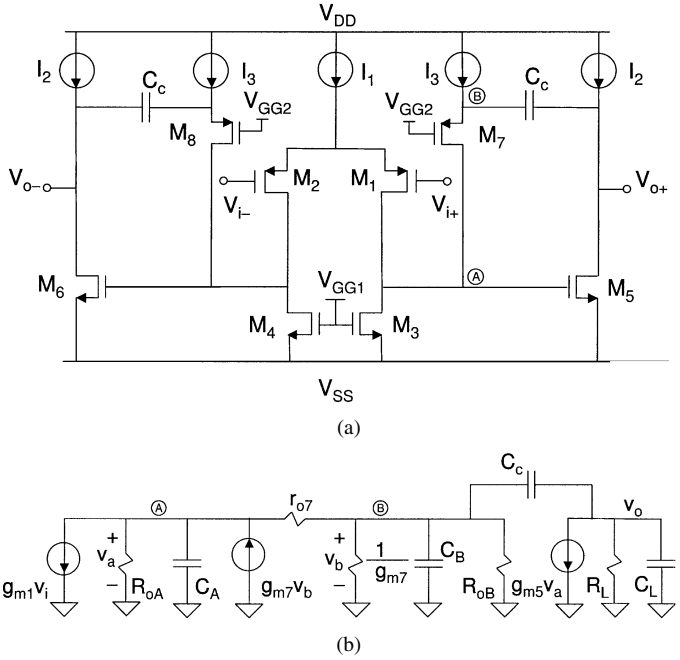


Fig. 1. (a) Two-stage op-amp with each C_c connected to a common-gate transistor. (b) Small-signal DM half circuit. Expressions for R_{oA}, C_A, R_{oB}, C_B, R_L, and C_L in terms of transistor-model parameters are given in the second column of Table I.

A. Separate, Additional Stages

Fig. 1(a) shows a two-stage fully differential op-amp with a pair of common-gate stages to block the feedforward current through the compensation capacitors [7]. Since the circuit is balanced, the characteristics of the entire circuit can be predicted through analysis of one half of the circuit. Consider the right half of the circuit, which contains M_1, M_3, M_5, and M_7. The I_3 current source and transistor M_7 form a common-gate stage. This stage uses components not shared by either the first or second stage in the op-amp. Also, this stage is added to the simplest two-stage op-amp configuration. Therefore, this stage is referred to as a "separate, additional" stage here.

The compensation capacitor is connected from the op-amp output to the source of M_7. Common-gate transistor M_7 allows the capacitor current to flow from the output back toward the input of the second stage but effectively blocks the feedforward current path through the compensation capacitor. If the common-gate stage is modeled as an ideal current-buffer stage with zero input impedance ($g_{m7} \to \infty$), the RHP zero is eliminated and the circuit has two poles and no zero [7]. In the following analysis, the current buffer is not assumed to be ideal.

A differential-mode (DM) half-circuit is shown in Fig. 1(b). Expressions for R_{oA}, C_A, R_{oB}, C_B, R_L and C_L in terms of transistor model parameters are given in the second column of Table I. Here, R_{oA} and C_A model the impedance at node A in Fig. 1(a), and R_{oB} and C_B model the impedance at node B. Elements R_L and C_L model the op-amp output impedance plus the load impedance. Since the ideal current sources in Fig. 1(a) are implemented with transistors in practice, an output resistance and capacitance is associated with each current source. These elements can be incorporated in the elements in the small-signal models, as noted in Table I. An analysis of the circuit in Fig. 1(b) is carried out in Appendix A. From (27), the op-amp gain has one LHP zero [8] approximately given by

$$z \approx -\frac{g_{m7}}{C_B + C_c} \quad . \tag{1}$$

A physical interpretation of this result is that $v_o = 0$ at the zero in (1) because the impedance from the op-amp output to ground through C_c (ignoring r_{o7} and R_{oB}) is zero at $s = z$. That is, $1/sC_c + (1/g_{m7}) || (1/sC_B) = 0$ at $s = z$. A key point here is that the RHP zero is eliminated even with finite g_{m7}.

The op-amp gain also has three poles. From (28), the dominant real pole is the same as with conventional Miller compensation

$$p_1 \approx -\frac{1}{g_{m5} R_L R_{oA} C_c} \quad . \tag{2}$$

Poles p_2 and p_3 can be found exactly from (12) or approximately from (29) if $|p_1| \ll |p_2|, |p_3|$. In general, p_2 and p_3 could be real or complex conjugates, and simple, general expressions for these poles cannot be readily generated.

However, if $g_{m7} \to \infty$, which is the case considered by Ahuja [7], then from Appendix A, $|p_3| \to \infty$. With large g_{m7}, p_2 is approximately given by

$$p_2 \approx -\frac{g_{m5}}{(C_L + C_c)} \frac{C_c}{C_A} \tag{3}$$

[see (30) and the associated condition on g_{m7} in Appendix A]. If $C_c > C_A$, which is typically true, the magnitude of nondominant pole p_2 here is larger than in a conventional Miller compensated op-amp, where $p_2 \approx -g_{m5}/(C_L + C_A)$ [1], [11]. The increase in $|p_2|$ with the current buffer arises because current buffer M_7 eliminates the connection between the input of the second op-amp stage (node A) and the compensation capacitor (and the associated loading). Therefore, to achieve the same unity-gain frequency as with conventional Miller compensation, a smaller C_c and/or a smaller g_{m5} can be used here.

Because M_7 is part of a separate, additional stage, an advantage of this scheme is that it gives flexibility in choosing g_{m7}, which affects the zero and pole p_3, through the choice of I_3 and the W/L of M_7. If desired, g_{m7} can be made large so that the magnitudes of the zero and pole p_3 are well beyond the unity-gain frequency of the op-amp, in which case the op-amp gain can be approximated by a two-pole transfer function. Drawbacks of this approach are that extra devices and dc current are needed to implement the common-gate stages in Fig. 1(a), and mismatch between the I_3 current sources changes the bias currents in the input stage and affects the input-offset voltage of the op-amp. Also, these extra devices increase the equivalent input noise of the op-amp.

B. Embedded in Cascoded First-Stage Loads

A variation of the above scheme is possible when the first-stage loads are cascoded. Fig. 2 shows a schematic of this approach. Common-gate transistors M_7 and M_8 operate as a part of the first-stage loads and are therefore considered to be "embedded" in the first stage. These transistors also act as the current buffers connected to the C_c capacitors. The small-signal DM half-circuit is the same as in Fig. 1(b). Expressions for R_{oA},

TABLE I
APPROXIMATE EXPRESSIONS FOR ELEMENTS SHOWN IN THE DM HALF-CIRCUITS

Element	Fig. 1(a)	Fig. 2	Fig. 3(a)	Fig. 4(a)
R_{oA}	$r_{o1}\|\|r_{o3}$	r_{o1}	r_{o3}	$r_{o1}\|\|r_{o3}\|\|r_{o11}$
C_A	$C_{gs5}+C_{db1}+C_{db3}+C_{db7}$	$C_{gs5}+C_{db1}+C_{db7}$	$C_{gs5}+C_{db3}+C_{db7}$	$C_{gs5}+C_{db1}+C_{db3}+C_{db11}$
R_{oB}	∞ *	r_{o3}	r_{o1}	r_{o9} *
C_B	$C_{gs7}+C_{sb7}$ **	$C_{gs7}+C_{sb7}+C_{db3}$	$C_{gs7}+C_{sb7}+C_{db1}$	$C_{gs9}+C_{gs11}+C_{db9}$ **
R_L ***	r_{o5}	r_{o5}	r_{o5}	r_{o5}
C_L ****	C_{db5}	C_{db5}	C_{db5}	C_{db5}

* In practice, R_{oB} would include the output resistance of the circuit that implements the I_3 current source.

** In practice, C_B would include the drain-to-body capacitance of the output transistor that implements the I_3 current source.

*** In practice, R_L would include the output resistance of the circuit that implements the I_2 current source and any DM resistive loading caused by an external load or a CMFB circuit.

**** In practice, C_L would include the output capacitance of the circuit that implements the I_2 current source and any DM capacitive loading caused by an external load or a CMFB circuit.

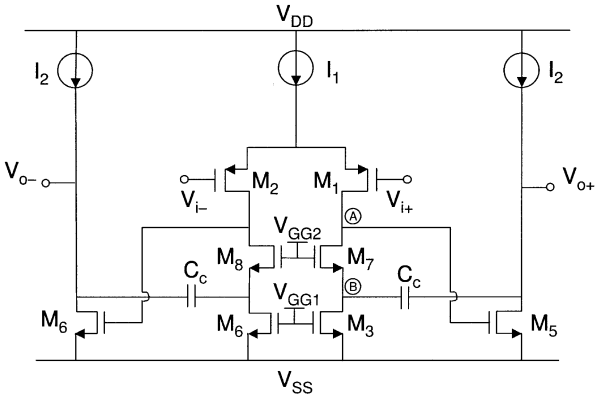
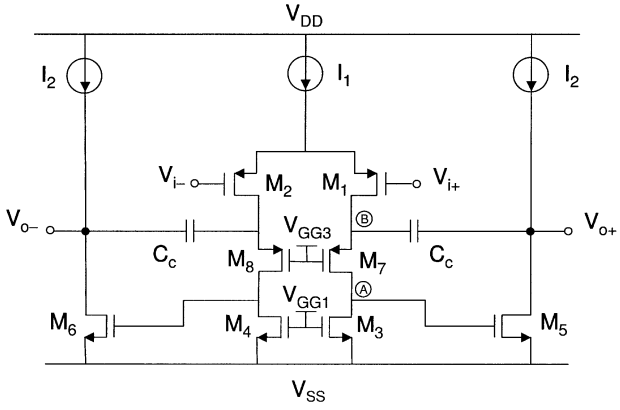
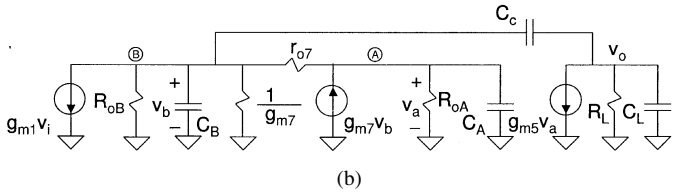


Fig. 2. Two-stage op-amp with each C_c connected to the cascode node in a cascoded active load. The small-signal DM half circuit is the same as in Fig. 1(b). Expressions for $R_{oA}, C_A, R_{oB}, C_B, R_L$ and C_L in terms of transistor model parameters are given in the third column of Table I.



(a)



(b)

Fig. 3. (a) Two-stage op-amp with each C_c connected to the cascode node of a cascoded input transistor. (b) Small-signal DM half circuit. Expressions for $R_{oA}, C_A, R_{oB}, C_B, R_L$ and C_L in terms of transistor model parameters are given in the fourth column of Table I.

R_{oB}, R_L, C_A, C_B, and C_L in terms of transistor model parameters are given in the third column of Table I. Therefore, the op-amp gain has one LHP zero and three poles, as given by the exact or approximate expressions in Appendix A.

Because the common-gate transistors here are embedded in the first-stage loads, the topology in Fig. 2 avoids the extra dc current required to bias the common-gate transistors in Fig. 1(a). However, the choice of g_{m7} is less flexible than in Fig. 1(a) because M_7 is part of the input stage here.

C. Embedded in Cascoded Differential Pairs

When the first stage of the op-amp uses a cascoded differential pair (or a folded-cascode configuration), each compensation capacitor can be connected to the source of a common-gate (cascode) transistor. Fig. 3(a) shows an example of this case [6], [9]. Common-gate transistors M_7 and M_8 form cascodes with the differential pair and are therefore considered to be "embedded." In the previous schemes, the feedforward current path that causes the RHP zero was eliminated by the common-gate transistors. In contrast, the feedforward path is eliminated in Fig. 3(a) only when the common-gate transistors have infinite transconductance ($g_{m7} \rightarrow \infty$). This condition gives zero impedance and zero voltage swing at the sources of the common-gate devices in Fig. 3(a). Under this condition, all the current from the input transistors flows into the sources of the common-gate transistors, eliminating the feedforward current through C_c. In practice, the transconductance g_{m7} is finite, and

some feedforward occurs. However, the impedance and swing at the source of the cascode device are smaller than at its drain. As a result, this connection reduces the feedforward current through C_c when compared to connecting C_c to the gate of M_5.

A small-signal DM half circuit is shown in Fig. 3(b). Expressions for R_{oA}, C_A, R_{oB}, and C_B in terms of transistor model parameters are given in the fourth column of Table I. The analysis of the gain for this circuit in Appendix B gives three poles and two zeros. Dominant pole p_1 is the same as with conventional Miller compensation. The nondominant poles can be found exactly or approximately using the equations in Appendix B. In general, p_2 and p_3 could be real or complex conjugates, and general expressions for these poles cannot be readily generated. Approximations for real p_2 and p_3 that are valid for this circuit when g_{m7} is large are given in Appendix A. (See (30) and (31) and the associated condition on g_{m7}.)

The two zeros are real; one is in the RHP and the other is in the LHP. Exact and approximate expressions for the zeros are given in Appendix B. In all cases, $|\text{zero(RHP)}| < |\text{zero(LHP)}|$. In most cases, the assumptions leading to (56) and (57) are true, and the zeros have magnitudes that are about equal. The reason for the two zeros can be explained intuitively as follows. Two currents that depend on the voltage v_b at node B flow at the op-amp output node in Fig. 3(b). The first current is the feedforward current flowing through the compensation capacitor C_c into the output node, which is

$$i_{fc} = sC_c v_b. \tag{4}$$

The second current is the current i_5 flowing in the g_m controlled source for M_5; $i_5 = g_{m5}v_a$. At high frequencies, $v_a \approx g_{m7}v_b/sC_A$. Therefore

$$i_5 \approx \frac{g_{m5}g_{m7}v_b}{sC_A}. \tag{5}$$

The currents i_{fc} and i_5 depend on v_b. When $i_{fc} - i_5 = 0$, the output voltage v_o is zero, and a zero exists in the op-amp gain. Substituting the last two equations into $i_{fc} - i_5 = 0$ and solving for the zeros gives

$$z_{1,2} \approx \pm\sqrt{\frac{g_{m5}g_{m7}}{C_cC_A}} \tag{6}$$

which agrees with (56) and (57).

With nonzero capacitances, this topology does not eliminate the RHP zero unless $g_{m5} \to \infty$ and/or $g_{m7} \to \infty$. With infinite g_{m5} and finite g_{m7}, nonzero feedforward occurs. However, the gain through the main signal path is infinite at all frequencies and cannot be canceled at any finite frequency by the remaining feedforward. Hence, the RHP zero is eliminated. On the other hand, infinite g_{m7} eliminates the RHP zero by eliminating the feedforward. The key is to observe that nonzero feedforward causes a RHP zero with finite transconductances.

An advantage of the circuit in Fig. 3(a) is that it avoids the extra devices, extra bias current, and mismatch problems in Fig. 1(a). A disadvantage is that it does not eliminate the RHP zero in practice, as described above. However, it introduces a LHP zero, and it increases the RHP zero, when compared to simple Miller compensation (where $z = g_{m5}/C_c$), if $g_{m7}/C_A > g_{m5}/C_c$.

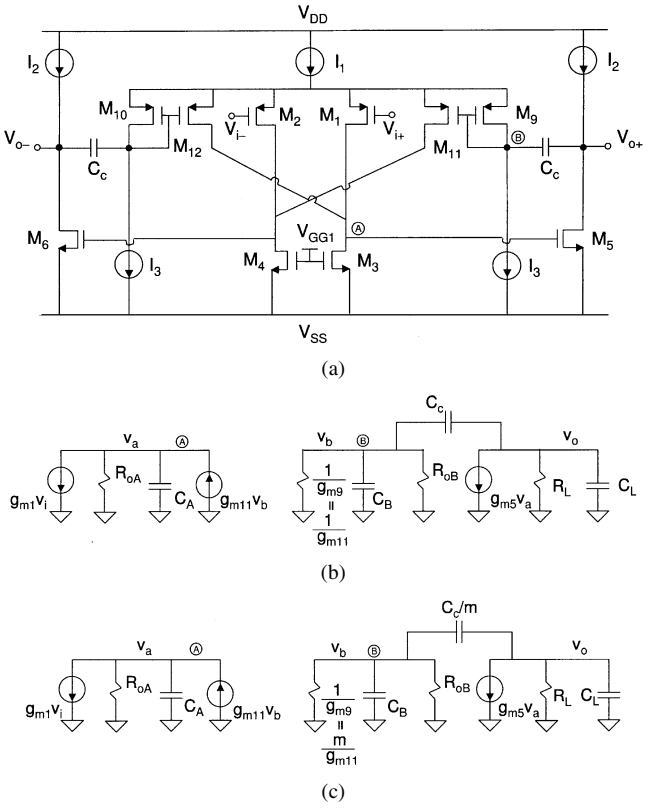


Fig. 4. (a) Two-stage op-amp with each C_c connected to a DM current mirror. (b) Small-signal DM half circuit for (a) when M_9 and M_{11} are matched. (c) Small-signal DM half circuit for (a) when the differential current mirror gain is m [that is, $(W/L)_{11} = m(W/L)_9$] and when the compensation capacitor is scaled by $1/m$. Expressions for $R_{oA}, C_A, R_{oB}, C_B, R_L$ and C_L in terms of transistor model parameters are given in the fifth column of Table I.

III. Current Mirrors

Section II describes the use of common-gate stages as current buffers connected to the compensation capacitors to allow feedback current but to block or reduce the feedforward current. Alternatively, current mirrors can be used to implement the current buffers [10]. Unlike common-gate transistors, however, current mirrors form inverting current buffers, and the extra inversion would introduce positive feedback in a straightforward connection. To overcome this problem, the two current-mirror outputs can be cross coupled in a fully differential op-amp. Fig. 4(a) shows the schematic. The differential current mirror consists of transistors M_9-M_{12}. Since the sources of M_9-M_{12} operate at a small-signal ground for DM signals, M_9, M_{11} and M_{10}, M_{12} act as current mirrors for DM signals. The behavior of these mirrors for common-mode (CM) signals is considered at the end of this section.

Initially, assume M_9-M_{12} are identical. A simplified DM small-signal circuit is shown in Fig. 4(b). The DM small-signal relationship $v_{gs9} = -v_{gs10}$ has been used here, along with $g_{m9} = g_{m10} = g_{m11} = g_{m12}$. If $r_{o7} \to \infty$ in Fig. 1(b) and g_{m7} in Fig. 1(b) is set equal to $g_{m9} = g_{m11}$ in Fig. 4(b), the circuit in Fig. 4(b) is the same as that in Fig. 1(b). Letting $r_{o7} \to \infty$ eliminates the resistance between nodes A and B that models the output resistance of the common-gate transistor M_7 in Fig. 1(a). In Fig. 4(b), the output resistances of the current mirror transistors are included in R_{oA} and R_{oB}. (See Table I.)

Therefore, the results in Appendix A can be applied here if $r_{o7} \to \infty$ and $g_{m7} \to g_{m11}$. Letting $r_{o7} \to \infty$ has no effect on the approximate results in Appendix A. Therefore, the op-amp gain has one LHP zero given approximately by

$$z \approx -\frac{g_{m11}}{C_B + C_c}. \tag{7}$$

As in Fig. 1(a), the LHP zero occurs where the impedance from the op-amp output to ground through C_c is zero.

The op-amp gain has three poles. The poles can be found from the equations in Appendix A, with the substitutions $r_{o7} \to \infty$ and $g_{m7} \to g_{m11}$. Here, the elements in the first column of Table I are associated with the transistor small-signal parameters in the last column of Table I.

If M_9, M_{10}, M_{11}, and M_{12} are identical, this topology is functionally equivalent to Fig. 1. However, the current-mirror topology in Fig. 4 requires more dc bias current than the topology in Fig. 1 because the current mirrors use four branches while the common-gate transistors in Fig. 1 use only two branches. Also, the current-mirror topology has a larger parasitic capacitance C_B than the topology in Fig. 1 because each side of the differential current mirror has two transistors that contribute a gate-source capacitance to C_B while C_B in Fig. 1 is dominated by the gate-source capacitance of only one common-gate transistor. In addition, the output resistance of the M_9, M_{11} current mirror is lower than the output resistance of common-gate M_7 in Fig. 1; therefore, the loading of the first stage by the current buffer is worse here than in Fig. 1. Also, mismatches between the dc drain currents in M_{11} and M_{12} change the bias currents in the input stage and affect the input-offset voltage of the op-amp. For these reasons, the topology in Fig. 1 would be favored over Fig. 4 when M_9-M_{12} are identical.

However, the transistors in each current mirror do not have to be identical. The mirrors provide current gain if $(W/L)_{11} = m(W/L)_9$ and $(W/L)_{12} = m(W/L)_{10}$ with $m > 1$. With a current gain m greater than unity, the DM current fed back to the input of the second gain stage through the current mirror is m times the current flowing through the compensation capacitor. Hence, if the compensation capacitance is decreased by a factor of m, the dominant pole will be unchanged because the current fed back through each compensation capacitor to the input of the second stage, which determines the dominant pole, is unchanged. This scaling provides a degree of design flexibility that does not exist in the other topologies. Being able to reduce C_c is potentially useful when the op-amp is driving a large DM capacitive load, which requires a dominant pole with a very small magnitude for compensation and would require a large compensation capacitor in Figs. 1–3. Here, that compensation capacitor can be decreased by a factor equal to the current mirror gain. Also, if a CMOS process does not have a thin-oxide-capacitor option, the area required for the compensation capacitor might be large even for a moderate-sized compensation capacitor, so the capacitor area (and hence the op-amp area) may be reduced by using Fig. 4(a) with gain in the current mirrors.

Fig. 4(c) shows the DM small-signal model for the circuit in Fig. 4(a) with a current-mirror gain of m and with the compensation capacitor scaled by $1/m$. With a current-mirror gain

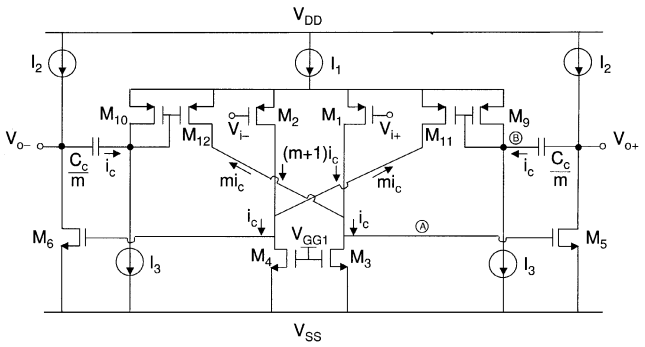


Fig. 5. Circuit in Fig. 4 showing small-signal CM currents, for the general case where the current mirrors have a gain m.

of m, the dc currents and the W/L's of M_9 and M_{11} are ratioed by m, so $g_{m9} = g_{m11}/m$. Equations similar to those in Appendix A could be derived for this circuit when $m \neq 1$. Alternatively, the case $m \neq 1$ can be handled with the existing equations in Appendix A by making one modification. Ignoring the compensation capacitors, the circuits in Fig. 4(b) and (c) are the same except the resistance from node B to ground stemming from diode-connected M_9 changes from $1/g_{m9} = 1/g_{m11}$ in Fig. 4(b) to $1/g_{m9} = m/g_{m11}$ in Fig. 4(c). Note that R_{oB} is in parallel with these resistances. Therefore, the resistance from node B to ground in Fig. 4(b) can be increased from $(1/g_{m11})\|R_{oB}$ to $(m/g_{m11})\|R_{oB}$ by changing R_{oB} to R'_{oB} where

$$R'_{oB} = \frac{1}{\frac{g_{m11}}{m} - g_{m11} + \frac{1}{R_{oB}}}. \tag{8}$$

With this change along with $r_{o7} \to \infty$, $g_{m7} \to g_{m11}$, and $C_c \to C_c/m$, the equations in Appendix A hold for Fig. 4 for any value of m. Approximations for the transfer function coefficients, and equations for the poles and zero based on those coefficients (and other simplifying assumptions) are given in Appendix C.

Finally, the compensation scheme in Fig. 4 is considered for CM signals in the general case where the current mirrors M_9, M_{11} and M_{10}, M_{12} have a gain of m. Fig. 5 shows the key small-signal CM currents; i_c represents the ac CM current flowing through the compensation capacitors. The current mirrors force the CM ac currents flowing into the drains of M_{11} and M_{12} to be mi_c. Because I_1 is constant, the sum of the small-signal currents flowing through M_9 and M_{11}, $(m+1)i_c$, must flow into the source (and out of the drain) of M_1. Similarly, $(m+1)i_c$ flows out of the drain of M_2. Therefore, the net CM feedback current flowing back to node A is equal to the current i_c flowing through the compensation capacitor; it is not affected by the gain m of the current mirror. As a result, the CM current gain of this differential current-mirror topology in Fig. 4 is unity.

In contrast, if conventional current mirrors were used (i.e., if the sources of M_9-M_{12} were connected to V_{DD}), the polarity of the CM current gain would be negative and the magnitude of the gain would be m. Hence, the CM feedback would be positive. The positive polarity of the CM gain through the differential current-mirror connection in Fig. 4 is important because it causes the polarity of the CM feedback to be negative. Since the magnitude of the CM current gain through the differential current mirror is unity, the effective compensation capacitance for

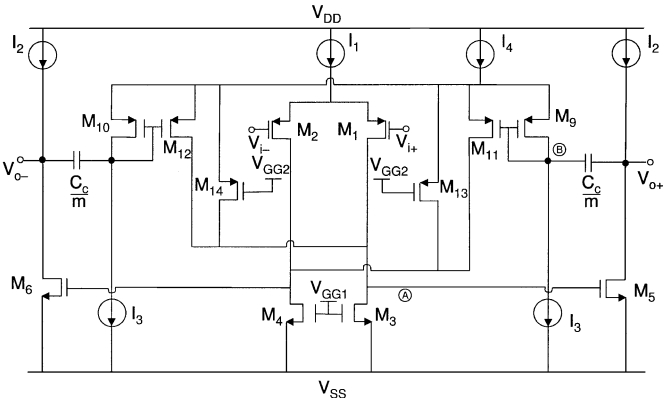


Fig. 6. Two-stage op-amp in Fig. 4, modified to eliminate the connection between the sources of M_1-M_2 and the sources of M_9-M_{12}.

the CM loop is equal to the actual compensation capacitance. Thus, the effective compensation capacitance is smaller for the CM loop than the DM loop when $m > 1$. This situation will be acceptable in cases where the CM loop does not require as large a compensation capacitor as the DM loop. For instance, the DM load capacitance might be greater than the CM load capacitance. Alternatively, the dc gain in the CM loop might be lower than the dc gain in the DM loop, thus the CM loop may not require as large a compensation capacitor as the DM loop.

One drawback of the circuit in Fig. 4 is that the parasitic capacitance at the common-source node of the M_1-M_2 differential pair is increased due to the connections to M_9-M_{12} there. Increasing this parasitic capacitance increases the CM gain at high frequencies. To eliminate the extra capacitance at that node due to M_9-M_{12}, the circuit in Fig. 6 can be used. Here, M_9-M_{12} still form a DM current mirror. M_{13} and M_{14} are common-gate devices that set the dc bias at the sources of M_9-M_{12} and provide a path for the CM currents that flow in M_9-M_{12}. This current is analogous to the CM current that flows in M_1 and M_2 in Fig. 5 [i.e., $(1+m)i_c$]. However, M_{13} and M_{14} carry no DM ac current because the sources of M_9-M_{14} are an ac ground for DM signals.

In some cases, the effective CM compensation capacitance C_c/m in Figs. 5 and 6 may not be large enough to compensate the CM loop. In such cases, the CM compensation could be augmented, perhaps by adding capacitor(s) in the CMFB circuit.

Another option would be to compensate the CM loop independently from the DM loop, which is compensated by the C_c/m capacitors. The effect of these capacitors on the CM gain of the op-amp can be eliminated in at least two ways. First, the following changes can be made to Fig. 6. Transistors M_{13} and M_{14} are each split into two parallel transistors that are ratioed by m [e.g., $M_{13} \rightarrow M_{13A}$ and M_{13B} with $(W/L)_{13A} = m(W/L)_{13B}$]. Then, the drains of M_{13B} and M_{14B} are connected to V_{SS}. Fig. 7(a) shows the modified current mirror. Its response to ac CM input current i_c (the CM current flowing through the compensation capacitors) is labeled. With these changes, the CM ac drain current in M_{13A} (or M_{14A}) is equal in amplitude and opposite in polarity from the CM ac drain current that flows in M_{11} (or M_{12}) because I_4 is constant. As a result, the CM current gain of the modified current mirror is zero, and the C_c/m capacitors do not affect the CM gain of

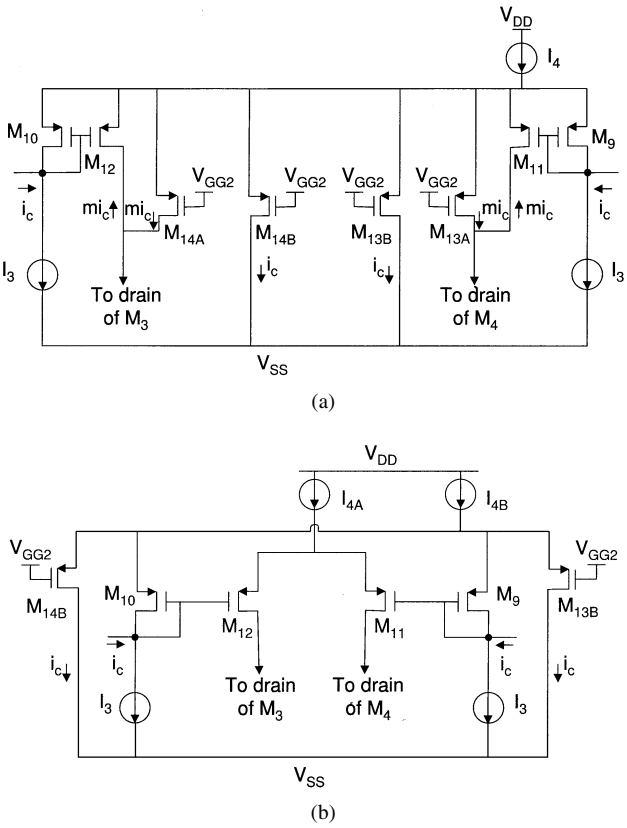


Fig. 7. Differential current mirror in Fig. 6 modified to reduce CM gain: (a) using matching; (b) using degeneration. The responses to ac CM input currents i_c are labeled.

the op-amp. Since CM gain reduction is achieved here through matching, mismatch will increase the magnitude of the CM current gain.

Fig. 7(b) shows a second modification of the current mirror in Fig. 6. This circuit eliminates M_{13A} and M_{14A}. It also separates the sources of M_9 and M_{10} from those of M_{11} and M_{12} and biases each of these source-coupled pairs with its own tail current source. The CM current gain is reduced by degeneration from I_{4A}. In practice, finite output resistance causes nonzero CM current gain. Also, nonzero capacitance at the source of M_{11} and M_{12} causes increasing CM current gain as a function of frequency.

In both of these circuits, CM compensation can be done elsewhere, perhaps by adding capacitor(s) in the CMFB circuit. With the changes to M_{13} and M_{14} as described above, another option is to change the second stage of the op-amp to a differential stage (configure M_5 and M_6 as a differential pair with a tail current source) and use local CMFB around each stage [13], [14]; local CMFB may not require additional capacitance for compensation. Also, it may be possible to use a simple current mirror (with the sources connected to a supply) in series with each compensation capacitor in such an op-amp. The CM feedback current through the current mirrors would not be a limitation here because the magnitude of the CM gain of the second stage would be small, due to the tail current source in the second stage.

Some disadvantages of using the current mirrors are that extra dc current is needed to bias the added transistors; loading of the first stage of the op-amp by the current mirrors reduces the

DM gain, and the CM loop is not affected by the compensation capacitors C_c that compensate the DM loop. Also, these current mirrors increase the equivalent input noise of the op-amp.

IV. Conclusion

Four fully differential op-amp topologies that use a current buffer in series with each compensation capacitor have been considered. Exact and approximate expressions for the op-amp DM gain were given, which can be solved for the poles and zero(s). Also, approximate expressions for the poles and zero(s), which are valid under certain assumptions, were presented. These approximate expressions yield real values for poles p_2 and p_3; however, complex nondominant poles can occur in practice and can be calculated from the quadratic equation in (29), using the approximate or exact transfer function coefficients presented in this paper.

The exact and approximate expressions for the transfer function coefficients presented in each appendix were verified for a number of different sets of component values. For each case, the transfer function coefficients were calculated using the formulas in the appendices, the poles and zero(s) were found by factoring the numerator and denominator of the transfer function, and those results were compared to the poles and zero(s) from a HSPICE [15] pole–zero analysis of the same small-signal circuit.

The gain expressions for the topologies in Sections II-A, II-B and III have a LHP zero but do not have a RHP zero. The RHP zero was eliminated because added circuitry blocks feedforward through the compensation capacitor, but the added circuitry in series with the compensation capacitor introduces a LHP zero. The topology in Section II-C gives a LHP and RHP zero. The RHP zero was not eliminated here because a feedforward path through the compensation capacitor remains in this case. However, the RHP zero is different (typically larger) than the value of the RHP zero with conventional Miller compensation.

All the topologies presented could be used in low-supply-voltage applications, since the current buffer stages do not require bias voltages that exceed the supply and they do not limit the output voltage swing. However, Figs. 1(a) and 4(a) have fewer transistors stacked between the supplies than do Figs. 2 and 3, so the former circuits may be more attractive in very low-voltage applications. On the other hand, Figs. 1(a) and 4(a) require extra bias current that is not required in Figs. 2 and 3. When comparing Figs. 2 and 3, the former has two potential advantages. First, the RHP zero has been eliminated in Fig. 2 but not in Fig. 3. Second, large g_{m7} is desirable in both circuits, and realizing a large transconductance will be easier with the NMOS cascode device in Fig. 2 than the PMOS cascode transistor in Fig. 3.

The topology in Fig. 4(a) offers one unique degree of design flexibility, since its current buffers are current mirrors that can have a current gain greater than unity. Increasing the gain in the current mirror allows the compensation capacitor to be decreased by the factor that the gain was increased without changing the dominant pole of the DM gain; such scaling can potentially save silicon area. However, this scheme has some significant disadvantages: extra dc current is needed to bias the added transistors; loading of the first stage of the op-amp by the current mirrors reduces the DM gain, and the compensation capacitors C_c that compensate the DM loops do not affect the CM loops in the same way as the DM loops. Also, these current mirrors increase the equivalent input noise of the op-amp. These disadvantages may limit the use of current mirrors to special applications.

The common-gate and current-mirror stages in Figs. 1(a) and 4(a) require extra bias current. If these stages are not used, this current could instead be used in other stages to change op-amp parameters such as the dc gain and/or pole and zero locations.

Appendix A

The transfer function of the small-signal circuit in Fig. 1(b) is analyzed here. With appropriate substitutions, the results of this analysis can be applied to the circuits in Figs. 1(a), 2, and 4(a). Applying Kirchhoff's Current Law at the two internal nodes and at the output node gives three equations

$$sC_Lv_o+\frac{v_o}{R_L}+g_{m5}v_a=sC_c(v_b-v_o) \tag{9}$$

$$sC_Bv_b+\frac{v_b}{R_{oB}}+g_{m7}v_b+\frac{(v_b-v_a)}{r_{o7}}=sC_c(v_o-v_b) \tag{10}$$

$$g_{m1}v_i+\frac{v_a}{R_{oA}}+sC_Av_a+\frac{(v_a-v_b)}{r_{o7}}=g_{m7}v_b. \tag{11}$$

These equations can be manipulated into the desired op-amp gain v_o/v_i. The gain transfer function is

$$\frac{v_o}{v_i}(s)=G\frac{n_0+n_1s}{a_0+a_1s+a_2s^2+a_3s^3} \tag{12}$$

where the exact expressions for the coefficients are

$$a_0=1+\frac{1}{g_{m7}R_{oB}}+\frac{R_{oA}}{g_{m7}r_{o7}R_{oB}}+\frac{1}{g_{m7}r_{o7}} \tag{13}$$

$$\begin{aligned}a_1=&g_{m5}R_{oA}R_LC_c\left(1+\frac{1}{g_{m7}r_{o7}}\right)\\&+C_AR_{oA}\left(1+\frac{1}{g_{m7}r_{o7}}+\frac{1}{g_{m7}R_{oB}}\right)\\&+\frac{C_B+C_c}{g_{m7}}\left(1+\frac{R_{oA}}{r_{o7}}\right)+R_L(C_L+C_c)\\&\cdot\left(1+\frac{1}{g_{m7}r_{o7}}+\frac{1}{g_{m7}R_{oB}}+\frac{R_{oA}}{g_{m7}R_{oB}r_{o7}}\right)\end{aligned} \tag{14}$$

$$\begin{aligned}a_2=&\frac{C_A(C_B+C_c)R_{oA}}{g_{m7}}\\&+\frac{(C_BC_L+C_BC_c+C_LC_c)R_L}{g_{m7}}\left(1+\frac{R_{oA}}{r_{o7}}\right)\\&+(C_L+C_c)C_AR_{oA}R_L\left(1+\frac{1}{g_{m7}r_{o7}}+\frac{1}{g_{m7}R_{oB}}\right)\end{aligned} \tag{15}$$

$$a_3=\frac{(C_LC_BC_A+C_cC_BC_A+C_LC_cC_A)R_{oA}R_L}{g_{m7}} \tag{16}$$

$$G=g_{m1}g_{m5}R_{oA}R_L \tag{17}$$

$$n_0=1+\frac{1}{g_{m7}r_{o7}}+\frac{1}{g_{m7}R_{oB}} \tag{18}$$

$$n_1=\frac{C_B+C_c}{g_{m7}}-\frac{C_c}{g_{m5}g_{m7}r_{o7}}. \tag{19}$$

Assuming that g_{m5}, $g_{m7}\gg 1/R_{oA}, 1/R_{oB}, 1/R_L, 1/r_{o7}$; $C_c, C_L \gg C_A, C_B$; $g_{m7}r_{o7}\gg R_{oA}/R_{oB}$; and $g_{m5}R_{oA}\gg$

C_L/C_c, an approximate, simplified set of coefficients for the transfer function in (12) is

$$a_0' = 1 \tag{20}$$
$$a_1' = g_{m5}R_{oA}R_LC_c \tag{21}$$
$$a_2' = \frac{R_L(C_BC_L + C_BC_c + C_LC_c)}{g_{m7}}\left(1 + \frac{R_{oA}}{r_{o7}}\right) + R_{oA}R_L(C_L + C_c)C_A \tag{22}$$
$$a_3' = \frac{R_{oA}R_L(C_LC_BC_A + C_cC_BC_A + C_LC_cC_A)}{g_{m7}} \tag{23}$$
$$G' = g_{m1}g_{m5}R_{oA}R_L \tag{24}$$
$$n_0' = 1 \tag{25}$$
$$n_1' = \frac{C_B + C_c}{g_{m7}}. \tag{26}$$

Using the approximate expressions n_0' and n_1' for the numerator coefficients, the zero is given by

$$z \approx -\frac{n_0'}{n_1'} = -\frac{g_{m7}}{C_B + C_c}. \tag{27}$$

The dominant real pole is given by (assuming $|p_1| \ll |p_2|, |p_3|$)

$$p_1 \approx -\frac{a_0'}{a_1'} = -\frac{1}{g_{m5}R_LR_{oA}C_c}. \tag{28}$$

Assuming a dominant pole and considering $|s| \gg |p_1|$, a_0 in (12) is negligible and the dominator in (12) becomes approximately $a_1s + a_2s^2 + a_3s^3 \approx a_1's + a_2's^2 + a_3's^3$. Therefore, approximate values of the poles p_2 and p_3 are the roots of

$$a_1' + a_2's + a_3's^2 = 0. \tag{29}$$

These poles can be real or complex, depending upon the element values. Poles p_2 and p_3 will be real and widely spaced if $(a_2')^2 \gg 4a_3'a_1'$ [1]. One way this condition can be satisfied is with large g_{m7} [i.e., $g_{m7} \gg 4g_{m5}C_c[(C_L||C_c) + C_B]/(C_L + C_c)C_A$], where $x||y = xy/(x + y)$. Also, if $g_{m7} \gg (1/R_{oA} + 1/r_{o7})(C_B + C_L||C_c)/C_A$, $a_2' \to R_{oA}R_L(C_L + C_c)C_A$. Under these assumptions, the widely spaced nondominant poles are given by

$$p_2 \approx -\frac{a_1'}{a_2'} = -\frac{g_{m5}}{(C_L + C_c)}\frac{C_c}{C_A} \tag{30}$$
$$p_3 \approx -\frac{a_2'}{a_3'} = -\frac{g_{m7}}{(C_L||C_c) + C_B}. \tag{31}$$

As $g_{m7} \to \infty$, $|p_3| \to \infty$.

If the approximations above for z, p_2, and p_3 are valid, $|z| < |p_3|$ since $C_L||C_c < C_c$, and the pole–zero diagram will be as shown in Fig. 8. As a result, the phase shift of the op-amp gain will never reach $-180°$. Therefore, the op-amp will be stable in a feedback circuit if no additional poles or zeros are introduced by the feedback circuit.

APPENDIX B

The transfer function of the small-signal circuit in Fig. 3(b) is analyzed here. Applying Kirchhoff's Current Law at the two internal nodes and at the output node gives three equations

$$\frac{v_o}{Z_L} + g_{m5}v_a = sC_c(v_b - v_o) \tag{32}$$

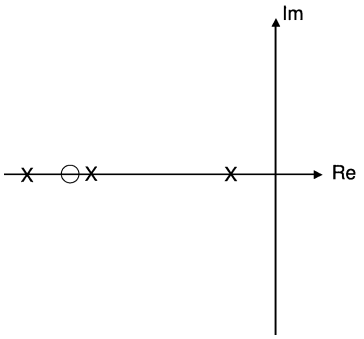


Fig. 8. Pole–zero diagram based on the approximate expressions for the poles and zero in Appendix A.

$$g_{m7}v_b = \frac{v_a}{Z_A} - \frac{(v_b - v_a)}{r_{o7}} \tag{33}$$
$$-g_{m1}v_i = \frac{v_b}{Z_B} + sC_c(v_b - v_o) + \frac{(v_b - v_a)}{r_{o7}} + g_{m7}v_b \tag{34}$$

where

$$Z_A = \frac{R_{oA}}{(1 + sR_{oA}C_A)} \tag{35}$$
$$Z_B = \frac{R_{oB}}{(1 + sR_{oB}C_B)} \tag{36}$$
$$Z_L = \frac{R_L}{(1 + sR_LC_L)}. \tag{37}$$

These equations can be used to find the transfer function

$$\frac{v_o}{v_i}(s) = G\frac{n_0 + n_1s + n_2s^2}{a_0 + a_1s + a_2s^2 + a_3s^3} \tag{38}$$
$$a_0 = 1 + \frac{R_{oA}}{g_{m7}R_{oB}r_{o7}} + \frac{1}{g_{m7}R_{oB}} + \frac{1}{g_{m7}r_{o7}} \tag{39}$$
$$a_1 = \tau_A\left(1 + \frac{1}{g_{m7}R_{oB}} + \frac{1}{g_{m7}r_{o7}}\right) + \frac{\tau_B}{g_{m7}R_{oB}}\left(1 + \frac{R_{oA}}{r_{o7}}\right) + \tau_L\left(1 + \frac{1}{g_{m7}R_{oB}} + \frac{1}{g_{m7}r_{o7}} + \frac{R_{oA}}{g_{m7}R_{oB}r_{o7}}\right) + R_LC_c\left(1 + \frac{1}{g_{m7}R_{oB}} + \frac{1}{g_{m7}r_{o7}} + \frac{R_{oA}}{g_{m7}R_{oB}r_{o7}}\right) + g_{m5}R_LR_{oA}C_c \cdot \left(1 + \frac{1}{g_{m7}r_{o7}} + \frac{1}{g_{m5}g_{m7}R_LR_{oA}} + \frac{1}{g_{m5}g_{m7}r_{o7}R_L}\right) \tag{40}$$
$$a_2 = \tau_B\tau_L\left(\frac{R_{oA}}{g_{m7}R_{oB}r_{o7}} + \frac{1}{g_{m7}R_{oB}}\right) + \tau_BR_LC_c\left(\frac{R_{oA}}{g_{m7}R_{oB}r_{o7}} + \frac{1}{g_{m7}R_{oB}}\right) + \tau_A\tau_L\left(1 + \frac{1}{g_{m7}R_{oB}} + \frac{1}{g_{m7}r_{o7}}\right) + \tau_AR_LC_c\left(1 + \frac{1}{g_{m7}R_{oB}} + \frac{1}{g_{m7}r_{o7}} + \frac{1}{g_{m7}R_L}\right) + \tau_LR_{oA}C_c\left(\frac{1}{g_{m7}r_{o7}} + \frac{1}{g_{m7}R_{oA}}\right) + \tau_B\tau_A\left(\frac{1}{g_{m7}R_{oB}}\right) \tag{41}$$

$$a_3 = \frac{\tau_A(C_B\tau_L + C_B R_L C_c + \tau_L C_c)}{g_{m7}} \tag{42}$$

$$G = g_{m1}g_{m5}R_{oA}R_L \tag{43}$$

$$n_0 = 1 + \frac{1}{g_{m7}r_{o7}} \tag{44}$$

$$n_1 = -\frac{(R_{oA} + r_{o7})C_c}{g_{m5}R_{oA}g_{m7}r_{o7}} \tag{45}$$

$$n_2 = -\frac{C_A C_c}{g_{m5}g_{m7}} \tag{46}$$

where

$$\tau_A = R_{oA}C_A \tag{47}$$

$$\tau_B = R_{oB}C_B \tag{48}$$

$$\tau_L = R_L C_L. \tag{49}$$

Assuming that g_{m5}, $g_{m7} \gg 1/R_{oA}, 1/R_{oB}, 1/r_{o7}, 1/R_L$; $C_c, C_L > C_A$; $C_c, C_L \gg C_B$; $g_{m7}r_{o7} \gg R_{oA}/R_{oB}$; and $g_{m5}R_{oA} \gg C_L/C_c$, the approximate denominator coefficients are given by the expressions for a_0'-a_3' in Appendix A, and the other transfer-function coefficients are approximately given by

$$G' = g_{m1}g_{m5}R_{oA}R_L \tag{50}$$

$$n_0' = 1 \tag{51}$$

$$n_1' = -\frac{(R_{oA} + r_{o7})C_c}{g_{m5}R_{oA}g_{m7}r_{o7}} \tag{52}$$

$$n_2' = -\frac{C_A C_c}{g_{m5}g_{m7}}. \tag{53}$$

Using the numerator coefficients n_0', n_1' and n_2', the zeros are

$$\text{zero(LHP)} = -\frac{1}{2(R_{oA}\|r_{o7})C_A} - \sqrt{\frac{1}{4(R_{oA}\|r_{o7})^2C_A^2} + \frac{g_{m7}g_{m5}}{C_A C_c}} \tag{54}$$

$$\text{zero(RHP)} = -\frac{1}{2(R_{oA}\|r_{o7})C_A} + \sqrt{\frac{1}{4(R_{oA}\|r_{o7})^2C_A^2} + \frac{g_{m7}g_{m5}}{C_A C_c}}. \tag{55}$$

The zeros are real, with $|\text{zero(LHP)}| > |\text{zero(RHP)}|$. If $g_{m7}g_{m5}/C_A C_c \gg 1/4(R_{oA}\|r_{o7})^2C_A^2$, the expressions for the zeros simplify to

$$\text{zero(LHP)} \approx -\sqrt{\frac{g_{m7}g_{m5}}{C_A C_c}} \tag{56}$$

$$\text{zero(RHP)} \approx +\sqrt{\frac{g_{m7}g_{m5}}{C_A C_c}}. \tag{57}$$

Since the approximate expressions for the denominator coefficients in Appendix A apply here, the approximate expressions for the dominant real pole and for the other poles also apply here. If p_2 and p_3 are not real, the magnitudes of these complex poles can be approximated from (29) as

$$|p_2| = |p_3| \approx \sqrt{\frac{a_1'}{a_3'}} \approx \sqrt{\frac{g_{m7}g_{m5}}{C_A C_L}} \tag{58}$$

where the second approximation is valid if $C_L, C_c \gg C_A, C_B$. If $C_c \approx C_L$, the magnitude of these poles is about equal to the magnitude of the LHP zero in (56). Since complex p_2 and p_3 will typically be positioned close to the real axis to avoid high-frequency peaking in the op-amp gain [9], the complex poles and LHP zero will be clustered as shown in Fig. 9. If the effect of this cluster can be approximately modeled by one pole, then from a macroscopic viewpoint, the op-amp gain will resemble a transfer function with two LHP poles and one RHP zero.

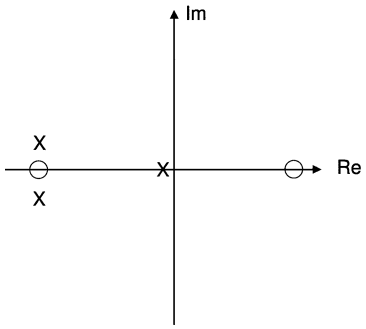


Fig. 9. Pole–zero diagram based on the approximate expressions for the zeros and dominant pole in Appendix B, when the nondominant poles are complex and near the LHP zero.

APPENDIX C

The small-signal circuit in Fig. 4(c) models Fig. 4(a) with a current-mirror gain of $m > 1$ (i.e, $g_{m11} = mg_{m9}$) and with the compensation capacitor scaled by $1/m$. The transfer function of this circuit is given by (12) and the coefficients in Appendix A, with those coefficients modified by the variable changes in Section III. When $r_{o7} \to \infty$, many terms in a_0-a_2 are eliminated. Assuming that g_{m5}, $g_{m11}/m \gg 1/R_{oA}, 1/R_{oB}, 1/R_L$; $C_c/m, C_L > C_A$; $C_c/m, C_L \gg C_B$; $g_{m7}r_{o7} \gg R_{oA}/R_{oB}$; and $g_{m5}R_{oA} \gg C_L/C_c$, simple, approximate expressions for the coefficients in the transfer function are (after multiplying the numerator and denominator coefficients by m)

$$a_0' = 1 \tag{59}$$

$$a_1' = g_{m5}R_{oA}R_L C_c \tag{60}$$

$$a_2' = R_{oA}R_L\left(C_L + \frac{C_c}{m}\right)C_A + \frac{R_L C_L C_c}{g_{m11}} \tag{61}$$

$$a_3' = \frac{(mC_L C_B C_A + C_c C_B C_A + C_L C_c C_A)\,R_{oA}R_L}{g_{m11}} \tag{62}$$

$$G' = g_{m1}g_{m5}R_{oA}R_L \tag{63}$$

$$n_0' = 1 \tag{64}$$

$$n_1' = \frac{(mC_B + C_c)}{g_{m11}}. \tag{65}$$

Using the approximate expressions n_0' and n_1' for the numerator coefficients, the zero is given by

$$z \approx -\frac{n_0'}{n_1'} = -\frac{g_{m11}}{(mC_B + C_c)}. \tag{66}$$

The dominant real pole is given by (assuming $|p_1| \ll |p_2|, |p_3|$)

$$p_1 \approx -\frac{a_0'}{a_1'} = -\frac{1}{g_{m5}R_L R_{oA}C_c}. \tag{67}$$

Assuming a dominant pole and considering $|s| \gg |p_1|$, approximate values of the poles p_2 and p_3 are the roots of (29). Poles p_2 and p_3 will be real and widely spaced if $(a_2')^2 \gg 4a_3'a_1'$. One way this condition can be satisfied is by making g_{m11} sufficiently large [i.e., $g_{m11} \gg 4mg_{m5}C_c[(C_L||(C_c/m))+C_B]/[(C_L+(C_c/m))C_A]$ and $g_{m11} \gg m[C_L||(C_c/m)]/(R_{oA}C_A)$]. Under these assumptions, the widely spaced nondominant poles are given by

$$p_2 \approx -\frac{a_1'}{a_2'} = -\frac{g_{m5}}{\left(C_L + \frac{C_c}{m}\right)}\frac{C_c}{C_A} \tag{68}$$

$$p_3 \approx -\frac{a_2'}{a_3'} = -\frac{g_{m11}}{\left[\left(C_L||\frac{C_c}{m}\right) + C_B\right]m} \tag{69}$$

where $x||y = xy/(x+y)$. As $g_{m11} \to \infty$, $|p_3| \to \infty$. However, making g_{m11} large enough to satisfy both inequalities above may be difficult in practice; therefore, p_2 and p_3 may be real and closely spaced or complex conjugate in many cases.

While the dominant pole is approximately independent of m, the other poles and zero are affected by m.

ACKNOWLEDGMENT

The authors are grateful to J. Simonson for running some circuit simulations and to the reviewers for their helpful suggestions.

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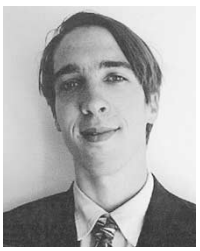

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