Global Standards for the Microelectronics Industry

LPDDR5 overview and operation

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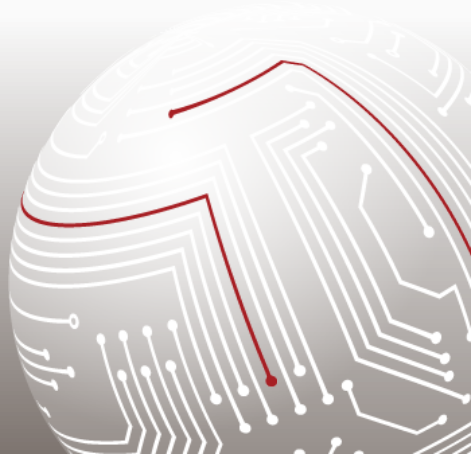

LPDDR5 Workshop

Agenda

- Architecture Outline
- LPDDR4 vs. LPDDR5 Comparison
- Bank Operations
- Pin Configuration
- Refresh Operation
- Latency variations
- Dynamic Voltage Frequency Scaling : DVFS
- Byte mode MR control
- Decision Feedback Equalization : DFE

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Architecture Outline

- Simplify Die Architecture
  - Only Single Channel configuration
    - No dual channel definition
- Rotated ball out concept for dual / quad channel PKG
- X16 and X8 are defined as native configuration
- Addressing are defined from 2Gb/die to 32Gb/die
- Lower power consumption
  - Lower VDD2 and VDDQ supply than LPDDR4
  - Dynamic Supply Voltage Control

Architecture

- Support various requirements
  - Flexible Architecture
    - Programable Bank organization
    - Byte mode and x16 mode
  - High reliability function
- High data rate friendly clocking system
  - Dual Clock for CA bus and DQ bus
- Low Power features
  - Reduce data transfer
  - Clocking power optimize

Architecture

- Flexible training schemes
  - QD training : FIFO, pre-programed
  - CA training : Consolidated CBT
  - Foreground / background ZQ calibration
- Support equivalent formfactor as LPDDR4
  - POP
  - MCP
  - FBGA

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LPDDR4 vs. LPDDR5 Comparison

Item	LPDDR4X	LPDDR5	Comments
Supply			
VDD1	1.8V	1.8V	
VDD2	1.1V		
VDD2H		1.05V	
VDD2L		0.9V (1.05V)	Can support mono VDD2(1.05V)
VDDQ	0.6V	0.5V term / 0.3V un-term	DVFSQ support

LPDDR4 vs. LPDDR5 Comparison

Item	LPDDR4X	LPDDR5	Comments
Architecture			
Channel configuration	2ch / 1ch	1ch	
Bank organization	8Banks	4Bank Group 4Banks / 8Banks /16Banks	MR selectable
Page Size	2Kbyte (x16) 1Kbyte (x8)	BG: 2Kbyte (x16), 1Kbyte (x8) 8Bank: 4Kbyte (x16), 2Kbyte (x8)	
Maximum Data rate	4266Mbps	6400Mbps	
DQs per Ch	x16 / x8	x16 / x8	
Burst length	16 / 32	16, 32 interleave and 32 seamless	8Banks and 16Banks support 32 seamless

LPDDR4 vs. LPDDR5 Comparison

Item	LPDDR4X	LPDDR5	Comments
Clocking			
Clock input	CK	CK / WCK	separate clock for CA and DQ
Synchronization	N/A	WCK2CK sync is required	
Frequency	CK up to 2.1GHz	CK up to 800MHz WCK up to 3.2GHz	
Clock termination	VSS ODT	VSS ODT	
WCK CK ratio	N/A	4:1 and 2:1 supported	2:1 can support up to 3.2Gbps
Duty Cycle Adjustment	N/A	programmable DCA	MR control
Duty Cycle Monitor	N/A	Read/Write one monitor	

LPDDR4 vs. LPDDR5 Comparison

Item	LPDDR4X	LPDDR5	Comments
CA Bus			
Pin count	6pins CA[5:0]	7pins CA[6:0]	Removing CKE
CA rate	SDR	DDR	Same Max CA bandwidth
Data bus			
Link protection	N/A	Optional : Link ECC	Optional : SECDED is supported
Read strobe	DQS	RDQS	single ended (_t or _c) supported
Write strobe	DQS	WCK	single ended (_t or _c) supported
pins per byte	11 pins 8DQ+1DMI+2DQS	13 pins 8DQ+1DMI+2RDQS+2WCK	

LPDDR4 vs. LPDDR5 Comparison

Item	LPDDR4X	LPDDR5	Comments
Interface			
DQ / CA scheme	LVSTL 0.6	LVSTL 0.5/0.3	DVFSQ, 0.3V for un-terminated
Mask shape	Rectangular	Hexagonal	
ZQ Calibration	Command	Back ground and command	ZQ connected to VDDQ
Reset VIH	VDD2	0.8*VDD2H	
CS input level	LVSTL 0.6	Sync mode fixed Vref, Smaller swing CMOS	Sync mode VrefCS=VDD2H/3
DFE	N/A	1 TAP DFE	

LPDDR4 vs. LPDDR5 Comparison

Item	LPDDR4X	LPDDR5	Comments
Low Power			
Clock power reduction	Single ended CK and DQS	Single Ended CK and WCK	Single ended support with _t or _c selectable
Dynamic Voltage Frequency Scaling	N/A	Core and DQ scaling	
Data copy	N/A	Vertical copy	
Write X	N/A	supported	
PASR	Bank and Segment Mask	Segment Mask	
PAAR	N/A	Segment Mask	Auto Refresh Segment Mask

LPDDR4 vs. LPDDR5 Comparison

Item	LPDDR4X	LPDDR5	Comments
Training			
Command Bus Training	x16 and x8 different	Unified training scheme, Rise and Fall CK edge separated	Two options w/ and w/o Vref training
Read DQ training	supported	supported	
FiFO Read/Write	supported	supported	8 depth
RDQS Training	DQS training mode	Enhanced RDQS training / RDQS toggle mode	

LPDDR4 vs. LPDDR5 Comparison

Item	LPDDR4X	LPDDR5	Comments
Other functions			
Frequency Set Point	2sets	3sets	
BL command select	BL16 and BL32 by CA op	BL16 and BL32 by different command	can support in BG mode and 16bank
Timing monitor	tDQS2DQ OSC	tWCK2DQI OSC and tWCK2DQO OSC	Cannot support simultaneous count
Temp Offset	supported	supported	
Vref program	CA and DQ	CA, per Byte DQ	Single ended CK/WCK Vref = VDDQ/2 fixed

LPDDR4 vs. LPDDR5 Comparison

Item	LPDDR4X	LPDDR5	Comments
Other functions			
MRW byte selectable	N/A	Supported	MR control Byte selectable MRW for Byte mode
VRCG	supported	supported	
Non Target ODT	deleted	Supported	No command bus snoop
Post PKG Repair	supported	supported	Guard Key protection
Serial ID MR	N/A	8MRs for serial ID	

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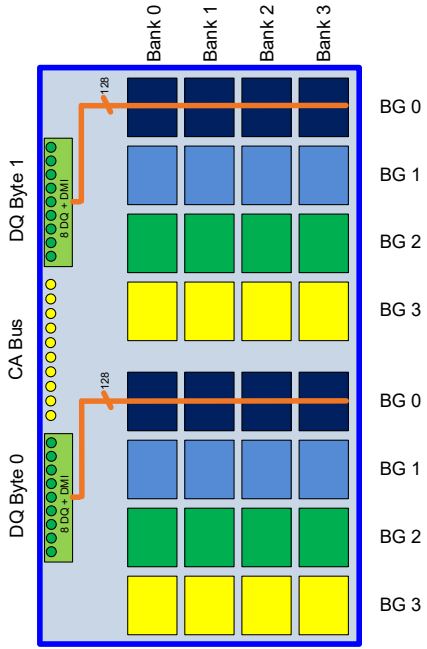
Bank Operations

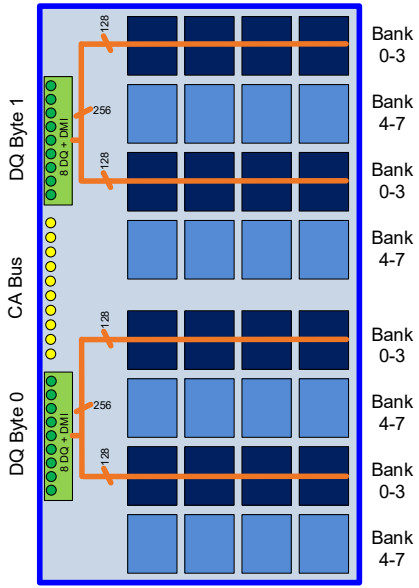
- LPDDR5 support three Bank organization.
  - There are different burst mode for each bank organization.
  - Selected by mode register write
  - Please refer to read/write operation.
- 8B mode
  - Full Frequency range
- BG mode
  - 4Bank group with 4Banks per Bank group.
  - High data rate support (more than 1.6GHz WCK)
- 16B mode
  - Low data rate support (equal and less than 1.6Ghz WCK)

Bank Operations

4Banks / 4Bank Groups Configuration

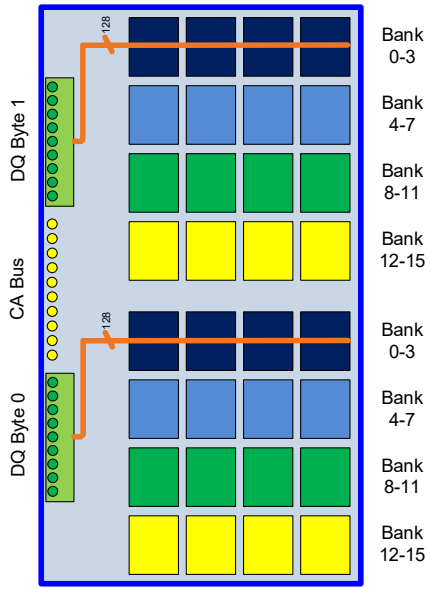


8Banks Mode Configuration



Bank Operations

16Banks Mode Configuration



Bank Architecture	BG	BA0	BA1	BG0	BG1
	8B	BA0	BA1	BA2	B4
	16B	BA0	BA1	BA2	BA3

NOTE 1 BA0-3: Bank Address, BG0-1: Bank Group address, B4: Burst Starting Address.

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Pin Configuration

- Minimizing pin count increase
- CA Bus
  - 7 CA input, increase 1pin from LPDDR4
  - Removing CKE, decrease 1pin from LPDDR4
- DQ Bus
  - 2 differential WCK, increase 1pin from LPDDR4
  - Combined differential RDQS/DMI/Parity

Pin Configuration

Pins Per-Byte Signal List/Description for Link Protection disabled

Pin Name	DBI Enable	SE RDQS		SE RDQS		Diff RDQS	
		Link Protection disabled					
		(MR20 OP[1:0]=01		(MR20 OP[1:0]=11		(MR20 OP[1:0]=10	
		Write	Read	Write	Read	Write	Read
#11 DMI	No	DM	N/A	DM	N/A	DM	N/A
	Yes	DMI	DBI	DMI	DBI	DMI	DBI
#12 RDQS_t	No	N/A	RDQS_t	N/A	N/A	N/A	RDQS_t
	Yes	N/A	RDQS_t	N/A	N/A	N/A	RDQS_t
#13 RDQS_c	No	N/A	N/A	N/A	RDQS_c	N/A	RDQS_c
	Yes	N/A	N/A	N/A	RDQS_c	N/A	RDQS_c

Pins Per-Byte Signal List/Description for Link Protection enabled

Pin Name	DBI Enable	SE RDQS		SE RDQS		Diff RDQS	
		Link Protection enabled					
		(MR20 OP[1:0]=01		(MR20 OP[1:0]=11		(MR20 OP[1:0]=10	
		Write	Read	Write	Read	Write	Read
#11 DMI	No	DM	parity	DM	parity	DM	parity
	Yes	DMI	parity	DMI	parity	DMI	parity
#12 RDQS_t	No	parity	RDQS_t	parity	N/A	parity	RDQS_t
	Yes	parity	RDQS_t	parity	N/A	parity	RDQS_t
#13 RDQS_c	No	N/A	N/A	N/A	RDQS_c	N/A	RDQS_c
	Yes	N/A	N/A	N/A	RDQS_c	N/A	RDQS_c

Pin Configuration

Symbol	Type
CK_t, CK_c	Input
CS	Input
CA[6:0]	Input
DQ[15:0]	I/O
WCK[1:0]_t, WCK[1:0]_c	Input
RDQS [1:0]_t , RDQS[1:0]_c	RDQS_t :I/O, RDQS_c :Output
DMI[1:0]	I/O
ZQ	Reference
VDDQ, VDD1, VDD2H, VDD2L	Supply
VSS	GND
RESET_n	Input

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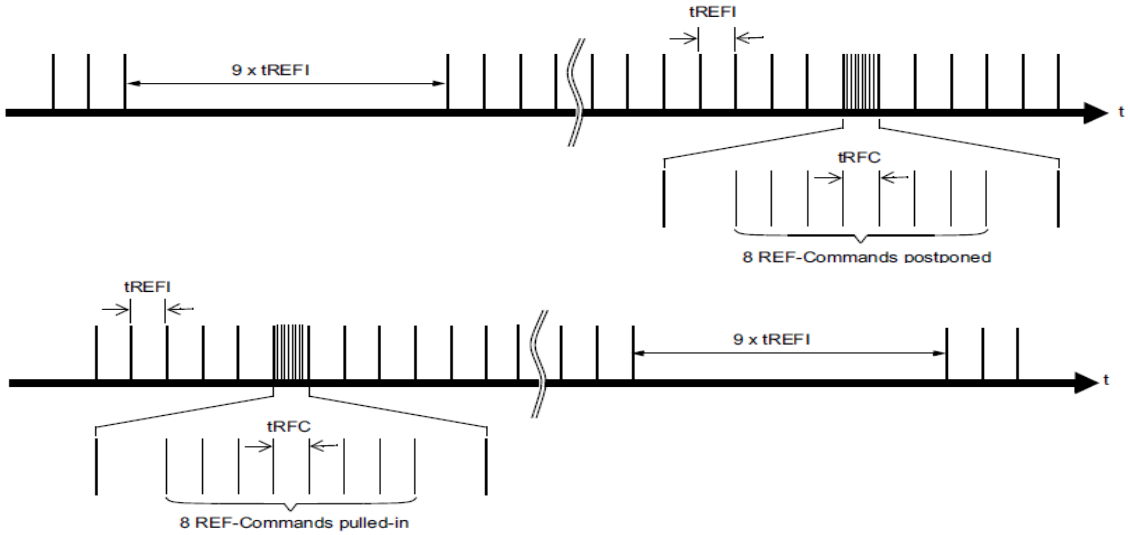
Refresh Operation

- LPDDR5 refresh operation is any time 8B mode base regardless bank architecture.
  - LPDDR5 support all bank refresh and per bank refresh
    - 8B / 16B mode : per bank refresh use BA[2:0] as bank address
    - BG mode : per bank refresh use BG0, BA[1:0] as bank address
  - 8times of per bank refresh are treated as one all bank refresh
    - All 8B must be refreshed within 8times of per bank refresh operations.
- Refresh interval definition
  - Actual Refresh interval : tREFIe at given condition is defined with tREFI and refresh multiplier (MR4 OP[4:0])
    - tREFIe = tREFI * refresh multiplier

Refresh Operation

- Refresh can be pull-in or postponed. # of pull-n and postpone defied with RM.

Example



Refresh Operation

MR4 OP[4:0]	Refresh rate	Max. No. of pulled-in or postponed REFab	Max. Interval between two REFab	Max. No. of REFab within max(2xtREFI x refresh rate multiplier,16xtRFC)	Per-bank Refresh
00000_B	Low temp. Limit	N/A	N/A	N/A	N/A
00001_B	8 x tREFI	1	2 x 8 x tREFI	2	1/8 of REFab
00010_B	6 x tREFI	1	2 x 6 x tREFI	2	1/8 of REFab
00011_B	4 x tREFI	2	3 x 4 x tREFI	4	1/8 of REFab
00100_B	3.3 x tREFI	2	3 x 3.3 x tREFI	4	1/8 of REFab
00101_B	2.5 x tREFI	3	4 x 2.5 x tREFI	6	1/8 of REFab
00110_B	2.0 x tREFI	4	5 x 2.0 x tREFI	8	1/8 of REFab
00111_B	1.7 x tREFI	5	6 x 1.7 x tREFI	10	1/8 of REFab
01000_B	1.3 x tREFI	6	7 x 1.3 x tREFI	12	1/8 of REFab
01001_B	1 x tREFI	8	9 x 1 x tREFI	16	1/8 of REFab
01010_B	0.7 x tREFI	8	9 x 0.7 x tREFi	16	1/8 of REFab
01011_B	0.5 x tREFI	8	9 x 0.5 x tREFI	16	1/8 of REFab
01100_B	0.25 x tREFi, no de-rating	8	9 x 0.25 x tREFI	16	1/8 of REFab
01101_B	0.25 x tREFi, with de-rating	8	9 x 0.25 x tREFI	16	1/8 of REFab
01110_B	0.125 x tREFi, no de-rating	8	9 x 0.125 x tREFI	16	1/8 of REFab
01111_B	0.125 x tREFi, with de-rating	8	9 x 0.125 x tREFI	16	1/8 of REFab
11111_B	SDRAM High temperature operating limit exceeded	N/A	N/A	N/A	N/A

Refresh Operation

- LPDDR5 support Partial Array Refresh Control (PARC) to reduce IDD5 power.
  - When MR25 OP[6] : PARC is set to 1B, LPDDR5 skip refresh operation based on Segment Mask: MR23 OP[7:0] information.

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Latency variations

- Read Latency
  - Read latency has dependency with following functions.
    - Byte mode
    - Read DBI or Read Data Copy (one of each)
    - Read Link ECC
    - DVFSC
  - Read latency has defined with three tables
    - Link ECC off / DVFSC disabled
    - Link ECC off / DVFSC enabled
    - Link ECC on / DVFSC enabled

Latency variations

- Read latency set definition
  - Read latency defined with set 0, set 1 and set 2
  - RL Set 0 applies when no features are enabled.
  - RL Set 1 applies when one feature is enabled (1 or 2).
  - RL Set 2 applies when two features are enabled.

Feature	Description
1	Byte Mode
2	Read DBI and/or Read Data Copy

Latency variations

Read Latencies for Link ECC off case (DVFSC disabled)

Data Rate Lower Limit (Mbps)	Data Rate Upper Limit (Mbps)	WCK: CK Ratio	Lower Clock Frequency Limit (>) (MHz)	Upper Clock Frequency Limit (<=) (MHz)	Read Latency			nRBTP [nCK]
					Set 0	Set 1	Set 2	
40	533	2:1	10	133	6	6	6	0
533	1067		133	267	8	8	8	0
1067	1600		267	400	10	10	12	0
1600	2133		400	533	12	14	14	0
2133	2750		533	688	16	16	18	2
2750	3200		688	800	18	20	20	2
40	533	4:1	5	67	3	3	3	0
533	1067		67	133	4	4	4	0
1067	1600		133	200	5	5	6	0
1600	2133		200	267	6	7	7	0
2133	2750		267	344	8	8	9	1
2750	3200		344	400	9	10	10	1
3200	3733		400	467	10	11	12	2
3733	4267		467	533	12	13	14	2
4267	4800		533	600	13	14	15	3
4800	5500		600	688	15	16	17	4
5500	6000		688	750	16	17	19	4
6000	6400		750	800	17	18	20	4

Latency variations

Read Latencies for Link ECC off case (DVFSC enabled)

Data Rate Lower Limit (Mbps)	Data Rate Upper Limit (Mbps)	WCK: CK Ratio	Lower Clock Frequency Limit (>) (MHz)	Upper Clock Frequency Limit (<=) (MHz)	Read Latency			nRBTP [nCK]
					Set 0	Set 1	Set 2	
40	533	2:1	10	133	6	6	6	0
533	1067		133	267	8	10	10	0
1067	1600		267	400	12	12	14	0
40	533	4:1	5	67	3	3	3	0
533	1067		67	133	4	5	5	0
1067	1600		133	200	6	6	7	0

Read Latencies for Link ECC on case (DVFSC disabled)

Data Rate Lower Limit (Mbps)	Data Rate Upper Limit (Mbps)	WCK: CK Ratio	Lower Clock Frequency Limit (>) (MHz)	Upper Clock Frequency Limit (<=) (MHz)	Read Latency		nRBTP [nCK]
					Set 0	Set 1 (Byte Mode)	
3200	3733	4:1	400	467	12	13	2
3733	4267		467	533	13	14	2
4267	4800		533	600	15	16	3
4800	5500		600	688	17	18	4
5500	6000		688	750	18	20	4
6000	6400		750	800	19	21	4

Latency variation

- Write Latency has impact by DVFSC
- Users can select set A or set B via MR3 OP[5] same as LPDDR4.

Write Latency: DVFSC Enabled

MR1 OP[7:4]	WCK: CK Ratio	Data Rate Range [Mbps]		CK Frequency Range [MHz]		WL		Unit
		Lower Limit (>)	Upper Limit (≤)	Lower Limit (>)	Upper Limit (≤)	Set A	Set B	
0000	2:1	40	533	10	133	4	4	nCK
0001	2:1	533	1067	133	267	4	6	nCK
0010	2:1	1067	1600	267	400	6	8	nCK
0000	4:1	40	533	5	67	2	2	nCK
0001	4:1	533	1067	67	133	2	3	nCK
0010	4:1	1067	1600	133	200	3	4	nCK

Latency variation

Write Latency: DVFSC Disabled

MR1 OP[7:4]	WCK: CK Ratio	Data Rate Range [Mbps]		CK Frequency Range [MHz]		WL		Unit
		Lower Limit (>)	Upper Limit (≤)	Lower Limit (>)	Upper Limit (≤)	Set A	Set B	
0000	2:1	40	533	10	133	4	4	nCK
0001	2:1	533	1067	133	267	4	6	nCK
0010	2:1	1067	1600	267	400	6	8	nCK
0011	2:1	1600	2133	400	533	8	10	nCK
0100	2:1	2133	2750	533	688	8	14	nCK
0101	2:1	2750	3200	688	800	10	16	nCK
0000	4:1	40	533	5	67	2	2	nCK
0001	4:1	533	1067	67	133	2	3	nCK
0010	4:1	1067	1600	133	200	3	4	nCK
0011	4:1	1600	2133	200	267	4	5	nCK
0100	4:1	2133	2750	267	344	4	7	nCK
0101	4:1	2750	3200	344	400	5	8	nCK
0110	4:1	3200	3733	400	467	6	9	nCK
0111	4:1	3733	4267	467	533	6	11	nCK
1000	4:1	4267	4800	533	600	7	12	nCK
1001	4:1	4800	5500	600	688	8	14	nCK
1010	4:1	5500	6000	688	750	9	15	nCK
1011	4:1	6000	6400	750	800	9	16	nCK

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Dynamic Voltage Frequency Scaling : DVFS

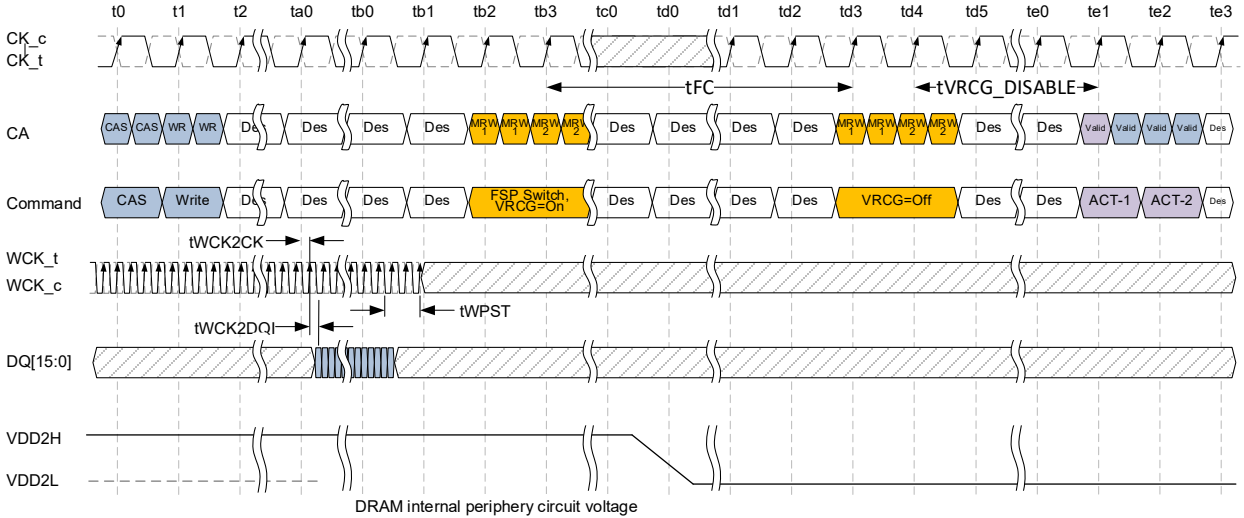
- LPDDR5 support two kind of DVFS scheme to reduce power. To enable DVFS function, there are frequency upper limits.
  - DRAM internal power reduction : DVFSC
  - Interface power reduction : DVFSQ

Dynamic Voltage Frequency Scaling : DVFS

- DVFSC stands for DVFS core
- Concept
  - Power supply : two different stable power supplies are required.
    - VDD2H : 1.05V nominal
    - VDD2L : 0.9V nominal
    - LPDDR5 internally change supply source based on MR OP condition
  - MR19 OP[1:0] controls DVFSC enable / disable.
  - DVFSC can support up to WCK = 800MHz

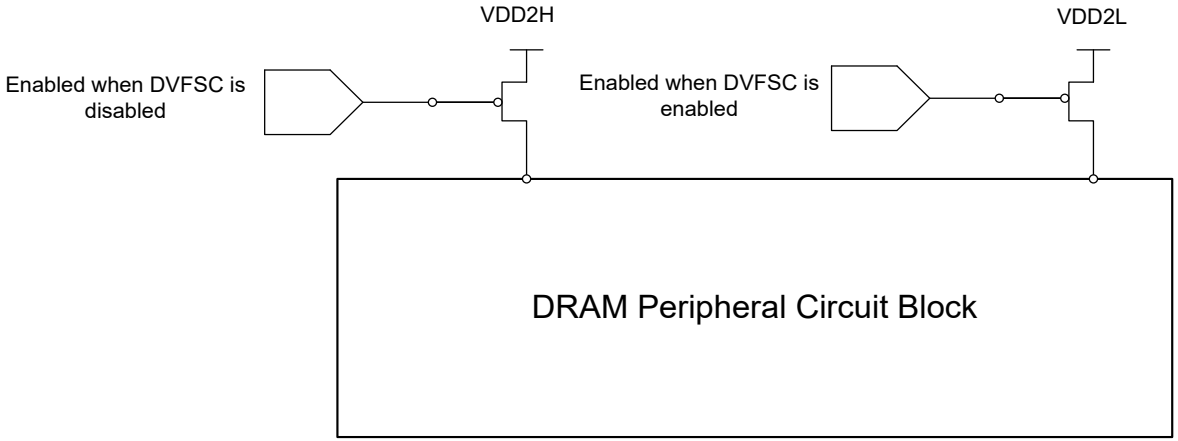
Dynamic Voltage Frequency Scaling : DVFS

- DVFSC timing (example)



Dynamic Voltage Frequency Scaling : DVFS

- DVFSC conceptual block diagram

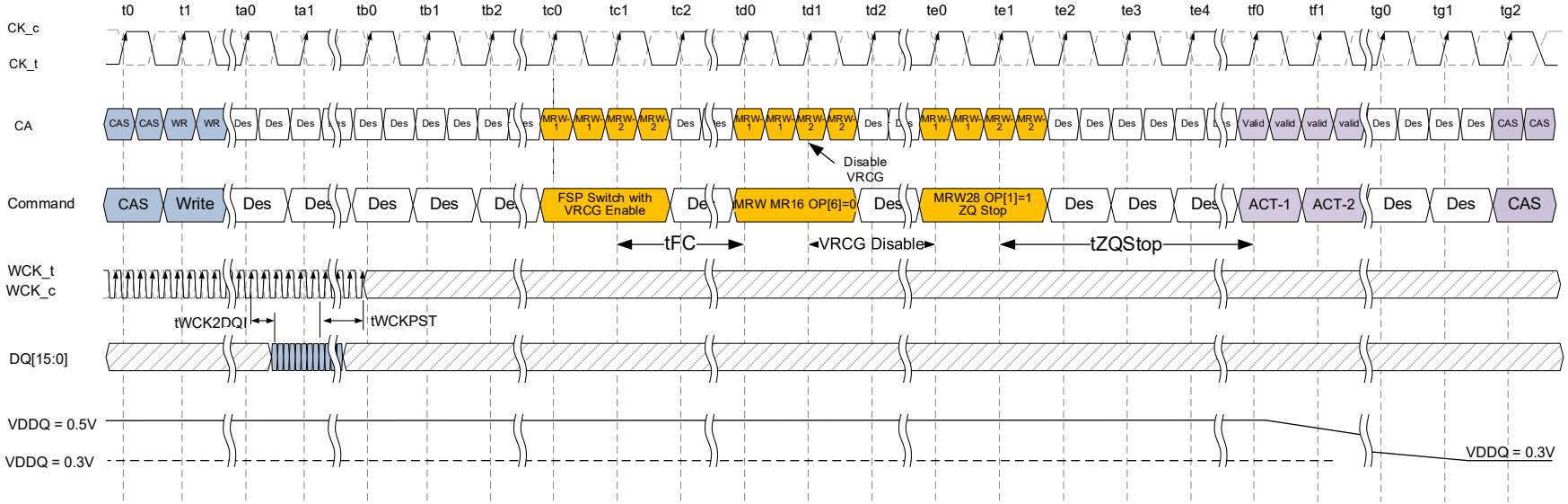


Dynamic Voltage Frequency Scaling : DVFS

- DVFSQ stands for DVFS VDDQ
- Concept
  - Power supply : two different power supply level is supported.
    - DVFSQ disabled : VDDQ=0.5V nominal, Can support terminated and un-terminated I/F
    - DVFQS enabled : VDDQ=0.3V nominal, Only support un-terminated I/F
    - During VDQQ ramp up and down, LPDDR5 can operate with DVFSQ enabled condition.
  - MR19 OP[3:2] controls DVFSQ enable / disable.

Dynamic Voltage Frequency Scaling : DVFS

- DVFSQ timing example



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Byte mode MR control

- Byte mode devices share CS and CA.
- Some Mode Registers are need to be programed differently for upper byte and lower byte device
- MR20 OP[5:4] controls MR write for upper byte and lower byte device
  - MR13 OP[1:0] Thermal Offset
  - MR25 OP[5:4] CA BUS TERM, CK BUS TERM
  - MR41 OP[4] PPRE
  - MR41 OP[7:5] NT DO ODT

Byte mode MR control

- Vref code has different control scheme to selectable Vref set for upper byte device and lower byte device
  - Vref CA : MR12 OP[7] VBS (VREF(CA) Byte Select)
  - Vref DQ : upper byte and lower byte use separate MR14 and MR15
- Duty Cycle Adjustment has separate OP for upper and lower byte.

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Decision Feedback Equalization : DFE

- LPDDR5 provide Decision Feedback Equalization (DFE) capability as optional feature.
  - Byte controllable function
    - MR24 OP[2:0] lower byte, MR24 OP[6:4] upper byte
  - DFE support higher than 800MHz WCK.

End of Presentation