28nm Timing Signoff Guidelines

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Objective:

The objective of this document is to setup a guideline for STA (Static Timing Analysis) signoff. Timing signoff of 28nm design has become very complex. TSMC recommends timing signoff on multiple corners for library and parasitic extraction. This is required mainly to model the delay variation caused by process variations in device, the metal thickness, dielectric thickness, etc as well as variations in temperature & voltage. The goal of this document is to define minimum set of corners required to perform STA without compromising the quality of silicon performance and facilitate Marvell's ability for fast turn around on project design schedules. This document has been reviewed and approved by the company CTO.

Information in this document is based on the study of two 28nm designs with HPM library with different library and RC corners for setup and hold cases. This document will be updated with additional data as it becomes available. Each design group should conduct its own study and, if it is necessary, adjust the signoff guideline.

Setup Analysis:

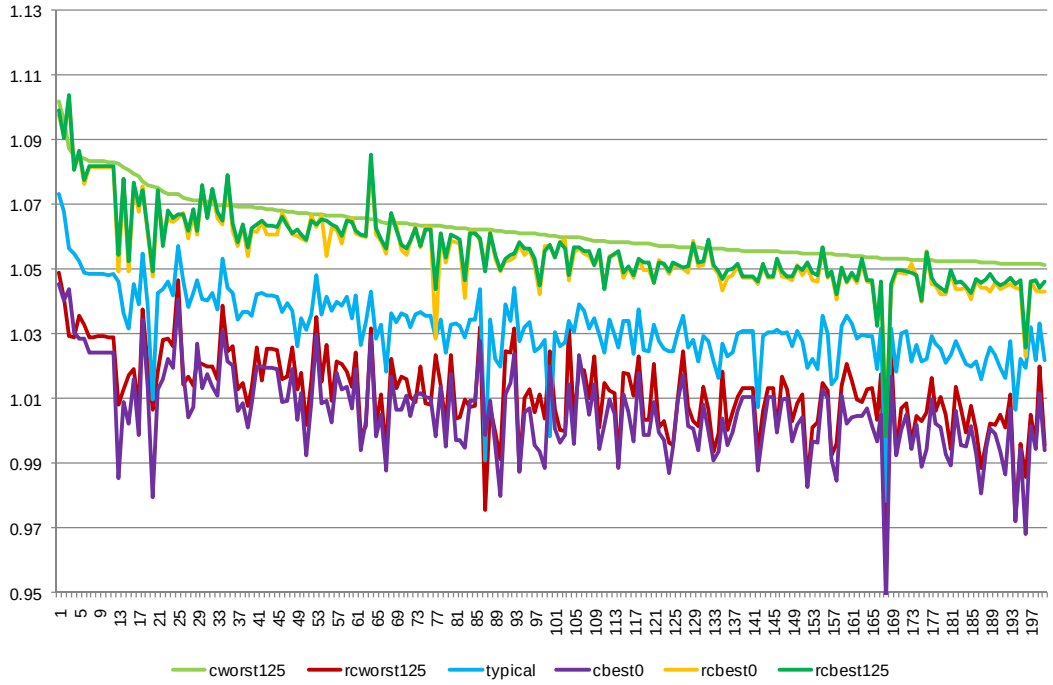
Signoff guidelines:

a. The setup analysis should be performed on slow library corner characterized at $V_{norminal}$-10% and 125C with worst process. The parasitic RC extraction should be performed at Cworst corner at 125C. . The setup analysis should also be performed on slow library corner characterized at $V_{norminal}$-10% and -40C or 0C based on design's operating temperature.
b. $V_{norminal}$ is defined as: 0.85v for HP and 0.9v for HPM
c. OCV based analysis with timing derates is not required for setup signoff in slow corner.
d. Clock uncertainty to model design specification like clock jitter should be added to the signoff requirement for each design in addition to the guideline described in this document. Recommended clock jitter is 30ps.
e. SI analysis for crosstalk induced delay and noise is required for setup signoff. SI related setup violations should be fixed.

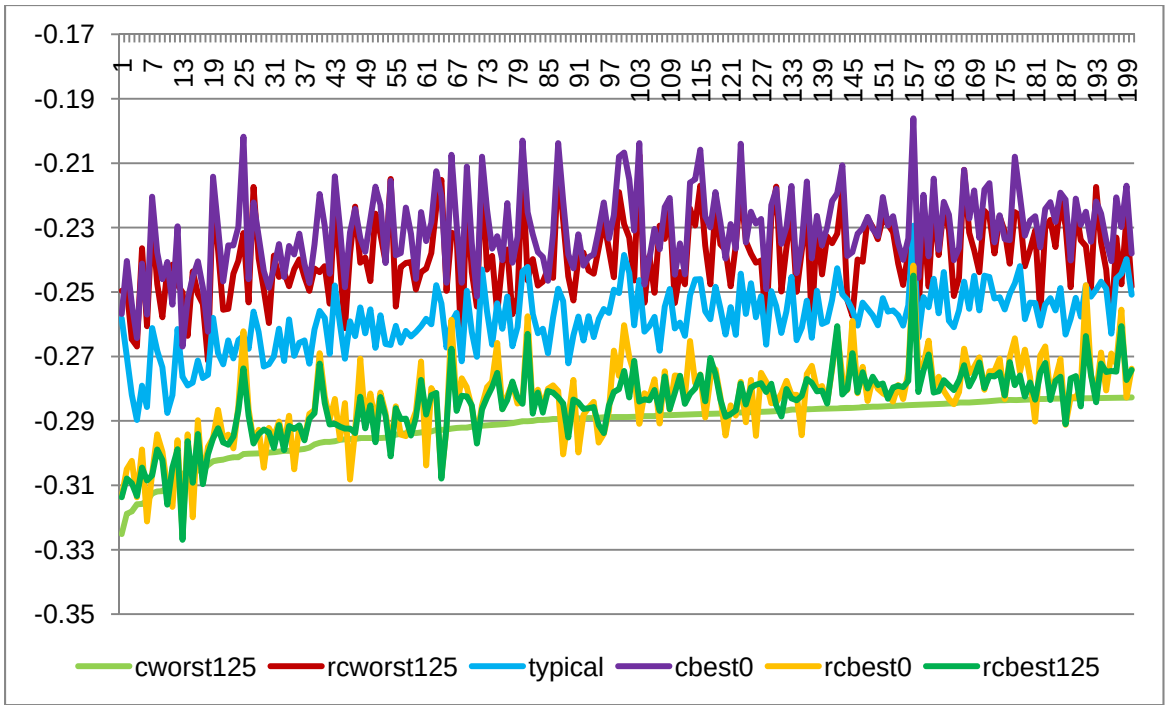
RC corners:

Following chart shows the effect of RC variation in a 28nm design on setup timing based on the study of one particular design. Similar results confirm this finding in another design as well.

Five corners are used for RC extraction, Cworst, Cbest, Ctypical, RCworst and RCbest. The following graph shows that Cworst parasitic corner give the longest path delay compared to other parasitic corner. Since setup analysis is dominated by path delay, using Cworst will almost cover all the other RC corners.



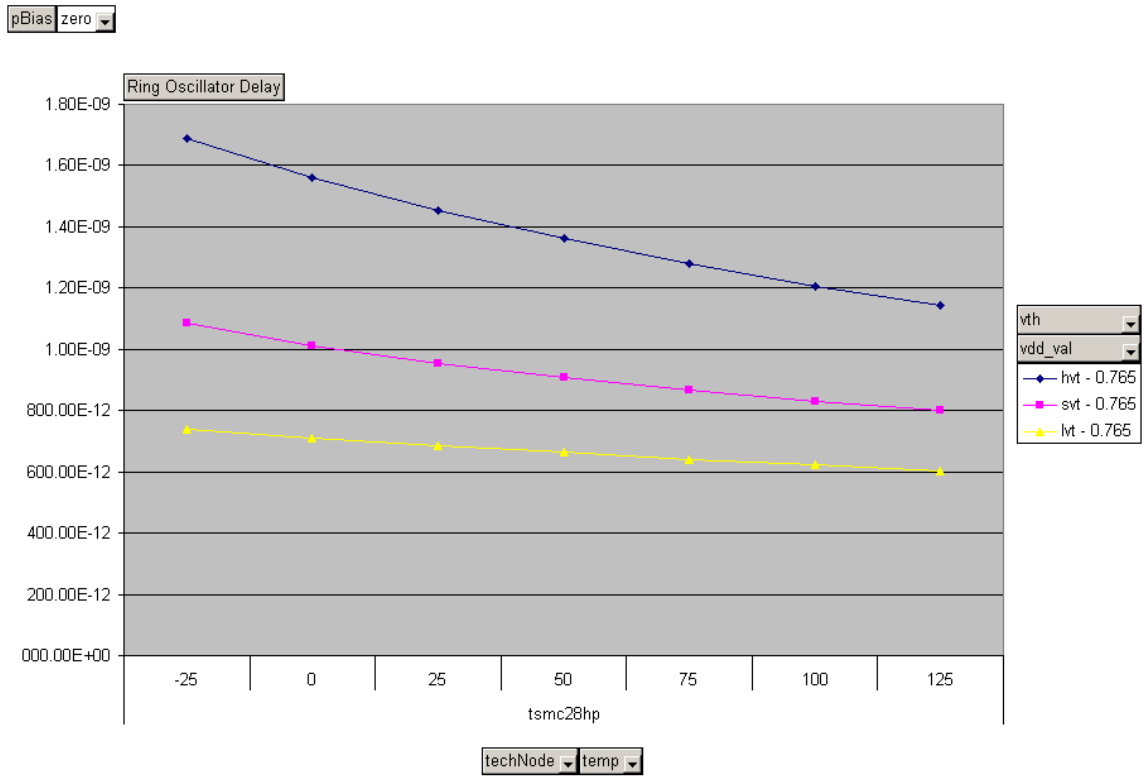
The following graph shows that Cworst is the worst corner for setup analysis in terms of WNS. Therefore using Cworst will almost cover all the other RC corners. Additional margin of 30ps on Cworst corner is added as there are some outliers with bigger violations in RCbest corner.


-0.17
-0.19
-0.21
-0.23
-0.25
-0.27
-0.29
-0.31
-0.33
-0.35
1
7
13
19
25
31
37
43
49
55
61
67
73
79
85
91
97
103
109
115
121
127
133
139
145
151
157
163
169
175
181
187
193
199
cworst125
rcworst125
typical
cbest0
rcbest0
rcbest125

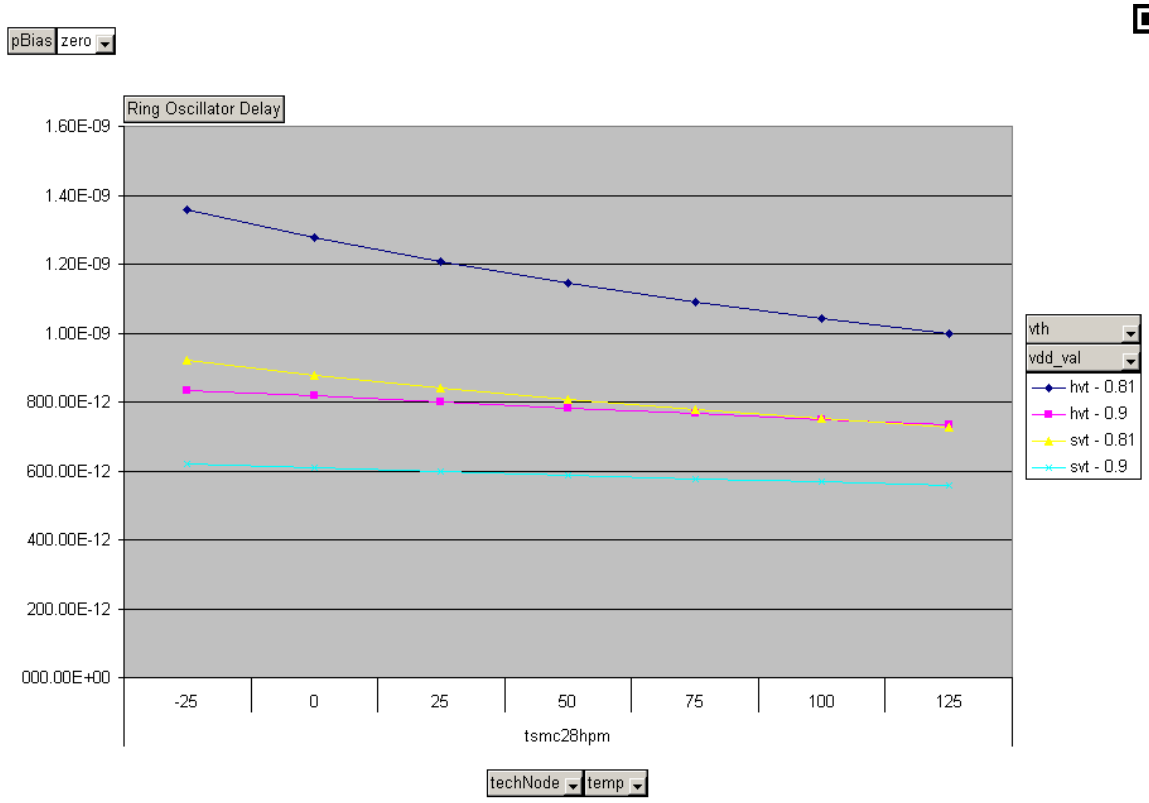
Temperature inversion:

a. In general, under similar process and voltage condition, cells are faster at lower temperature, but it has been found that some of the cells are slower when at lower temperature. This abnormal behavior is observed in technologies below 90nm and is referred to as temperature inversion effect. The temperature inversion effect is inversely proportional to voltage. When the voltage increases temperature inversion decreases and eventually goes away and we get the typical delay curve as a function on temperature.

b. Library team has provided following graph highlighting the effect of temperature inversion on the path delay of a ring oscillator circuit which includes buffers, inverters and complex combinational cells. The X axis shows the temperature and Y axis shows the delay of the ring oscillator circuit at a specific temperatureIf the operating temperature for the chip is below -10C, then both the regular STA run as described earlier and an additional STA run with slow library characterized at -10% and -40C should be performed for signoff.



28HP



28HPM

c. For the process with temperature inversion effect, the timing signoff for setup and hold should include slow library characterized at -10% voltage and 125C as well as slow library characterized at -10% voltage and -40C
d. If the chip is not planned to operate at temperature below 0C, then we do not need to signoff setup at -40C. In such case, the timing signoff for setup and hold should include slow library characterized at -10% voltage and 125C as well as slow library characterized at -10% voltage and 0C.

This is summarized as below:

Setup signoff corner table for operating temperature between -40C and 125C

Library			RC Extraction	OCV Derate		Margin	Clock	Xtalk
Process	**Voltage**	**Temp.**	**Process**	**Launch**	**Capture**	**Uncertainty**	**Jitter**	**SI/Noise**
Slow	$V_{norminal}$-10%	125C	Cworst@125C	0%	0%	30ps	30ps	Yes
Slow	$V_{norminal}$-10%	-40C	Cworst@-40C	0%	0%	30ps	30ps	Yes

Setup signoff corner table for operating temperature between 0C and 125C

Library			RC Extraction	OCV Derate		Margin	Clock	Xtalk
Process	**Voltage**	**Temp.**	**Process**	**Launch**	**Capture**	**Uncertainty**	**Jitter**	**SI/Noise**
Slow	$V_{norminal}$-10%	125C	Cworst@125C	0%	0%	30ps	30ps	Yes
Slow	$V_{norminal}$-10%	0C	Cworst@0C	0%	0%	30ps	30ps	Yes

Hold Analysis:

Hold analysis checks for the race condition on the clock paths. Even a small delay variation on clock network on short path could cause hold violations. Caution should be exercised to avoid excessive margin and derating factor, as such can lead to unnecessary buffer being added, resulting in routing congestion. This is especially serious at 28nm, since cell delays are shorter; therefore more delay cells are needed to fix the hold violation.

Signoff guidelines:

a. The final hold timing signoff for tape out should be performed with timing analysis with the combination of the three corners at Fast, Typical and Slow timing libraries with the RC parasitic extracted at the corresponding conditions.
b. OCV derating of +/-7% should be used for final signoff.
c. SI analysis for crosstalk induced delay and noise should be performed for hold analysis.
d. A margin should be used to guardband against the RC corner variation at the other two corners. This is explanation in the following “RC corners” section.
e. The delay through the *dly* cells has a bigger variation compared to the regular buffers and inverters. So it is recommended to use 20% derating on the delay cells.

This is summarized as below:

Hold signoff corner table for operating temperature between -40C and 125C

Library			RC Extraction	OCV Derate (Both Cells & Net)			
Process	**Voltage**	**Temp.**	**Process**	**Launch**	**Capture**	**Margin**	**SI/Noise**
Fast	$V_{norminal}$+10%	0C	Cbest@0C	-7%	+7%	15ps	Yes
Typical	$V_{norminal}$	50C	Ctyp@50C	-7%	+7%	30ps	Yes
Slow	$V_{norminal}$-10%	125C	Cworst@125C	-7%	+7%	45ps	Yes
Slow	$V_{norminal}$-10%	-40C	Cworst@-40C	-7%	+7%	45ps	Yes

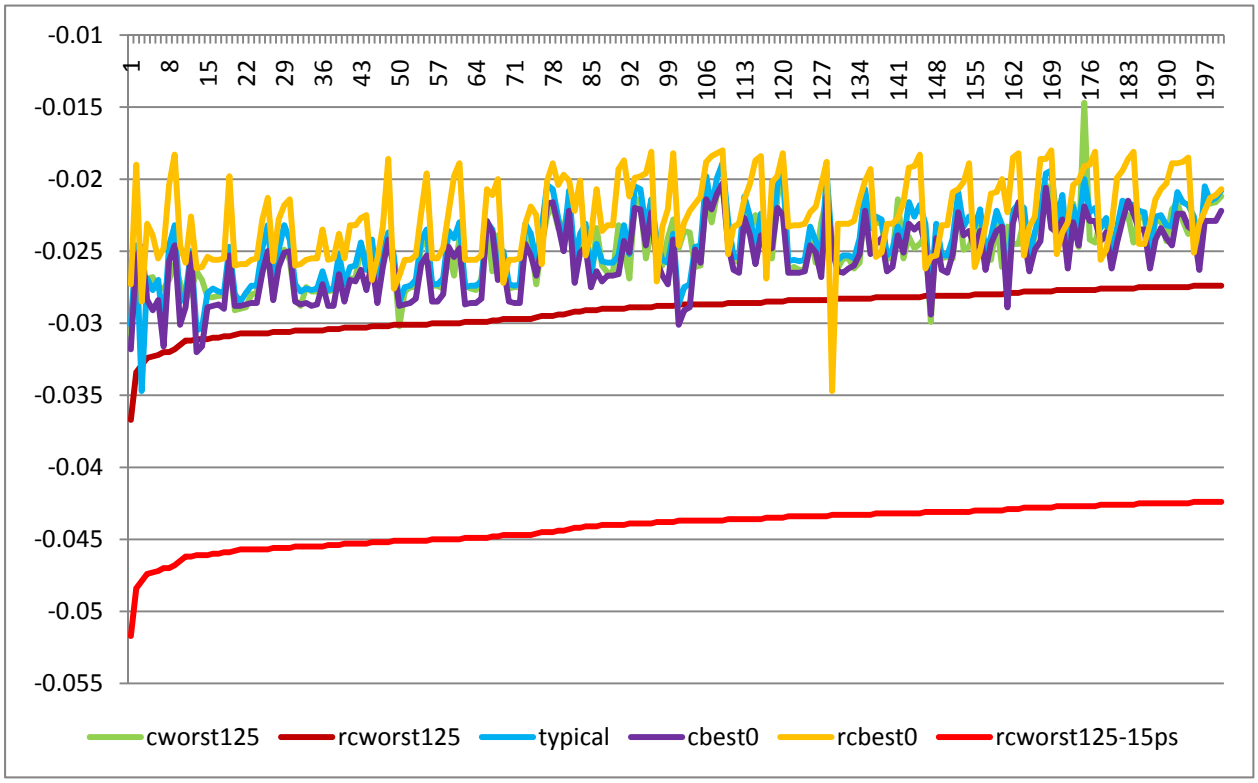
Hold signoff corner table for operating temperature between 0C and 125C

Library			RC Extraction	OCV Derate (Both Cells & Net)			
Process	**Voltage**	**Temp.**	**Process**	**Launch**	**Capture**	**Margin**	**SI/Noise**
Fast	$V_{norminal}$+10%	0C	Cbest@0C	-7%	+7%	15ps	Yes
Typical	$V_{norminal}$	50C	Ctyp@50C	-7%	+7%	30ps	Yes
Slow	$V_{norminal}$-10%	125C	Cworst@125C	-7%	+7%	45ps	Yes
Slow	$V_{norminal}$-10%	0C	Cworst@0C	-7%	+7%	45ps	Yes

RC corners:
Following chart shows the effect of RC variation in a 28nm design on hold timing based on the study of couple of designs. More study is planned on other designs to validate these results.

The following graph is plotted for min violation slack. An additional curve is plotted to represent -15ps guardbanding around RCWorst RC extraction. Using this margin to guardband STA runs, variations on RC corners can be contained.

The margin to guardband the RC corner variation could vary. It is design and technology dependent. The designers need to validate the margin to ensure all corners are covered, if necessary.



Well Proximity Effect:

Library characterization of standard cells is based on the condition that the cells are placed in the middle of the die and are surrounded by nWell on all four sides. The timing of a cell placed on the boundary of a block can degrade up to 2-3% compared to the same cell in the middle of the block. This is called Well Proximity Effect (WPE). WPE should be taken into account during STA signoff in all corners and modes. Library group requires STA signoff to include 0-3% of instance-specfic OCV derating on these cells.
There is no easy way in place and route implementation to completely avoid WPE without impacting the die size. So WPE should be addressed as a post processing step in the physical design flow after cell placement and timing optimization. The place and route engineer will deliver the list of cell instances that are potentially impacted by WPE along with netlist and SPEF, so the designers can derate the delay of these cells appropriately for timing signoff.
In most cases the timing impact of WPE in the design may not be significant. Typical path delay, in a design with clock frequency of 500Mhz, will be over 2ns in the slow corner. The typical buffer delay in such path will be less than 100ps. If such buffer is placed on the boundary of a block, WPE can degrade the timing of this buffer by less than 3ps. The probability of having multiple cells in a critical path on the boundary of a block is very slim. Nevertheless, designers should derate the delay on WPE impacted cells in PrimeTime-SI for signoff check using the following guidelines.

Hold Analysis

```
set_operating_condition –analysis_type on_chip_variation
set_timing_derate –early 0.93                                          …Note1
set_timing_derate –late  1.07                                          …Note1
set_timing_derate -late  1.095 [get_cells $wpeCellList \
                                    -filter "ref_name!~ *${libDelayCell}*"] …Note2
set_timing_derate -late  1.230 [get_cells $wpeCellList \
                                    -filter "ref_name=~**${libDelayCell}*"] …Note2
```

Setup Analysis

```
set_operating_condition –analysis_type on_chip_variation
set_timing_derate –late  1.030 [get_cells $wpeCellList \
                                     -filter "ref_name!~*${libDelayCell}*"] …Note3
set_timing_derate -late  1.230 [get_cells $wpeCellList \
                                     -filter "ref_name=~*${libDelayCell}*"] …Note3
```

`$wpeCellList` is WPE impacted cell instances listed by Place and Route engineer.
`$libDelayCell` is the pattern in library delay reference cell name. Eg.

```
For s90 library use:  set libDelayCell dly
For TSMC library use: set libDelayCell DEL
```

Note1: Assuming +/- 7% OCV derating is used in this case for hold analysis.
This command will apply +/-7% derating to all the cells in the design
Note2: Addition 3% OCV derating applied to WPE impacted instances.
The derating on non delay cells in the WPE instance list +9.6%.
The derating on delay cells in the WPE instance list is +23%
Note3: Assumes 0% OCV derating for setup analysis. If the design group requires *X* % OCV derating, then the derating on the WPE impacted cell instances should be adjusted to (*X* + 3)%.
The derating on the delay cells in WPE instance list is +23%

Delay Cell Usage

OCV derating for delay cells is bigger than regular buffers and inverters. The delay cell uses long channel length which increases the timing variation for these cells. User can use two types of delay cells for hold fixing. User should set +/-20% OCV derating in their STA signoff for szd_sdly* cells. The STA signoff OCV derating for szd_sdlylocv* cells should be set to +/-13%. The *locvx* cells uses regular poly length sized devices to help their timing track better with the normal standard cells. But because these cells use small width devices their timing variation is higher than the regular standard cells.

The following PT-SI commands should be used as global setting. WPE specific timing derate commands should be added in PrimeTime run as discussed in the previous page.

```
set si_enable_analysis true
set_operating_condition –analysis_type on_chip_variation
si_filter_per_aggr_noise_peak_ratio 0.01
set si_xtalk_delay_analysis_mode  all_paths
set_timing_derate -early 0.93
set_timing_derate -late  1.07
set_timing_derate -early 0.800 [get_lib_cells s88_syn/*dly*]
set_timing_derate -late  1.200 [get_lib_cells s88_syn/*dly*]
set_timing_derate -early 0.870 [get_lib_cells s88_syn/*locvx*]
set_timing_derate -late  1.130 [get_lib_cells s88_syn/*locvx*]
```