9.4 A 20dBm 2.4GHz Digital Outphasing Transmitter for WLAN Application in 32nm CMOS

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Integration of radios in SoCs along with digital baseband and application processors is desirable for cost and form-factor reasons. Digital processors are typically implemented in the latest CMOS process to take advantage of the increased density and performance afforded by CMOS scaling. Integration of traditional RF circuits, however, requires accurate RF and passive models that typically lag behind digital transistor models by several quarters. This makes RF integration the limiting factor for time-to-market for the whole SoC, or results in sub-optimal multiple-chip solutions. Furthermore, traditional RF circuits do not benefit from scaling as digital circuits do, e.g. due to extensive use of inductors, the ever-lowering supply voltage, etc. This work presents a digital WiFi transmitter (TX) implemented in a 32nm digital CMOS process to address these issues. An outphasing architecture allows implementation of both amplitude and phase modulation using scaling-friendly, delay-based, switching *phase* modulators. The integrated PA was already shown to be possible to design with no RF models [1]; known issues of outphasing PA design (e.g. output impedance modulation, linearity, efficiency) are also addressed in [1]. The phase modulator uses an open-loop architecture to accommodate OFDM bandwidths up to 40MHz. The TX achieves state-of-the-art performance already in 32nm and is moreover expected to: (1) improve with scaling and (2) port easily over successive process nodes.

Outphasing signals can be generated with DACs and IQ upconversion [2], an analog-intensive approach. Digital switching phase modulators have also been proposed based on both PLL and phase interpolation. Two-point modulation has been applied to extend digital PLL bandwidth to cover 5MHz WCDMA signals [3], but might be limited for wider bandwidth due to excessive VCO tuning range and linearity requirements. Phase interpolators are promising for wideband operation due to their open-loop nature, e.g. [4] achieves 5MHz channel bandwidth. A 20MHz OFDM-compliant phase modulator was presented in [5]. The current work uses a simplified, open-loop version of [5] allowing for lower power and wider-bandwidth operation up to 40MHz.

The TX architecture is shown in Fig. 9.4.1. The two phase modulators dynamically delay *each* LO edge to produce the two constant-amplitude, phase-modulated signals s_1 and s_2. The digital data driving the modulators is derived from the IQ inputs with upsampling, CORDIC decomposition, etc. [3], which has been implemented in a fixed-point software and loaded through an SRAM. The s_1 and s_2 signals are combined using transformers in the PA. The PA uses inverter-based Class-D stages for optimum linearity and power efficiency [1]. Contrary to prior art [4,5] that used separate modulators for OFDM phase (φ) and amplitude [θ=acos(A)], this work introduces both ($\varphi\pm\theta$) in a single modulator, thus leading to lower power consumption and noise.

System-level simulations have shown that each LO edge needs to be delayed with 8b resolution over 1 LO period (T_{LO}) to meet WiFi 2.4GHz specifications. Each phase modulator (Fig. 9.4.2) uses a segmented coarse-fine open-loop architecture. A tapped-delay-line (TDL) provides coarse 3b quantization by selecting one of the eight 45°-spaced phases using a phase-MUX and is designed to prevent glitches [5], which could degrade output spectrum. The present TDL design can implement phase jumps up to $\pm T_{LO}/4$ in one LO period, adequate for WiFi signals. The digital DLL used in the TDL is discussed in [6].

The remaining 5 bits of phase resolution are provided by the digitally controlled delay line (DCDL) which has a target resolution of 1.6ps. The DCDL turns on-off small varactors to introduce small required *incremental* delays (Fig. 9.4.3). The varactors have been distributed into 3 identical stages, each with 4 binary-weighted switched MOS capacitors. 48 delay steps (rather than 2^5=32) are used in the DCDL to allow for the correction of TDL tap mismatches. Additional tri-state inverters are used to coarsely adjust the DCDL cell driving strength to achieve the target resolution over process corners. Wave-pipelining (self-retiming) is used along the DCDL to ensure that the same modulation word is applied on the same LO edge as it propagates through the DCDL stages.

An on-chip start-up calibration routine is used to measure TDL tap mismatches and the DCDL total delay (Fig. 9.4.4); an LUT to dynamically pre-distort the phase modulation data is populated using these values [5]. The TDL and DCDL are closed into a ring-oscillator (~1ns period) whose periods are counted over a fixed time window (2µs needed to achieve 0.5ps resolution). The measurement is performed for each TDL tap and for minimum and maximum DCDL delay. From these one can calculate the TDL tap and DCDL delays for the LUT.

The TDL and DCDL outputs have a duty cycle of $3/8T_{LO}$ (set for optimum phase MUX timing margin). A pulse-width-modulation (PWM) stage restores 50% duty cycle on s_1 s_2 signals while preserving the phase modulation. The PWM delays every rising edge by $T_{LO}/2$ to produce a falling edge. The PWM also corrects for any amplitude and delay mismatch between the two outphasing paths.

All delay cells and control circuits use CMOS gates for low power, while registers use dynamic flip-flops. The delay of CMOS stages is sensitive to supply and ground noise, e.g. due to possible PA coupling. To preserve modulation fidelity, an LDO is used to supply the sensitive, edge-processing parts of the phase modulator (TDL, DCDL, PWM). Also, power supply and ground of the PA and the phase modulator have been isolated on-chip and domain-crossing circuits have been deployed at the interfaces.

The chip has been implemented in digital SoC 32nm CMOS with a flip-chip BGA package. The TX has been tested with 802.11g 20MHz 64-QAM signals. Figure 9.4.5 shows the measured spectrum at average power of +20dBm (signal clipped at 5.9dB above average) with total PAE of 22%; the power level is set by EVM target of -25dB. No PA pre-distortion is required, given good AM-AM and AM-PM linearity. Far-out spectral emissions are set by 8b phase quantization and they are consistent with system-level simulations. EVM can be improved by increasing backoff at power and efficiency expense, similar to linear TX (e.g. measured EVM is -31.5dB at +18.4dBm with 18.2% total PAE). The PA uses two supplies of 2.05V and 1V. The core modulator dissipates 38mA from 1.05V supply during OFDM modulation (23mA blocks under regulated supply, 15mA digital blocks); an additional 14mA is used for LDO bias (supplied at 1.8V). The total modulator power consumption is 82mW including all LDO overhead, leading to 18.6% total TX OFDM efficiency. Figure 9.4.5 also compares this TX performance with other published 802.11g TX with integrated PA: this TX achieves the best efficiency at -25dB EVM without PA predistortion and has low TX-chain (i.e. phase modulator) power consumption.

The TX has also been tested with 802.11n 40MHz MCS7 signals: the TX delivers +12.1dBm (only half PA active) at -28dB EVM without PA predistortion (Fig. 9.4.6); the phase modulator power consumption is still 82mW.

The total TX area is 2.6mm^2 (Fig. 9.4.7): phase modulators, LDOs, and PA active areas are respectively 0.1, 0.4 and 0.8mm^2. The all-digital phase modulator design is compatible with and benefits from further CMOS scaling.

Acknowledgments:
The authors would like to thank H. Alavi, B. Carlton, A. Jimenez, Q. Wang, P. Karidi, P. Mendoza, C. Nieva, S. Suzuki, and R. Bishop.

References:
[1] H. Xu et al. "A Flip-Chip-Packaged 25.3dBm Class-D Outphasing Power Amplifier in 32nm CMOS for WLAN Application", *IEEE J. Solid-State Circuits*, vol. 46, no. 7, pp. 1596-1605, July 2011.
[2] I. Hakala et al. "A 2.14-GHz Chireix outphasing transmitter", *IEEE Trans. Microwave Theory and Techniques*, vol. 53, no. 6, pp. 2129-2138, June 2005.
[3] Z. Boos et al., "A Fully Digital Multimode Polar Transmitter Employing 17b RF DAC in 3G Mode", *ISSCC Dig. Tech. Papers*, pp. 376-377, Feb. 2011.
[4] M. E. Heidari et al, "All-Digital Outphasing Modulator for a Software-Defined Transmitter", *IEEE J. Solid-State Circuits*, vol. 44, no. 4, pp. 1260-1271, Apr. 2009.
[5] A. Ravi et al., "A 2.5GHz delay-based wideband OFDM outphasing modulator in 45nm-LP CMOS", *IEEE Symposium on VLSI Circuits*, pp. 26-27, June 2011.
[6] K. Chandrashekar et. al., "A 32nm CMOS All-Digital Reconfigurable Fractional Frequency Divider for LO Generation in Multistandard SoC Radios With On-the-Fly Interference Management", *ISSCC Dig. Tech. Papers*, pp. 352-353, Feb. 2012.

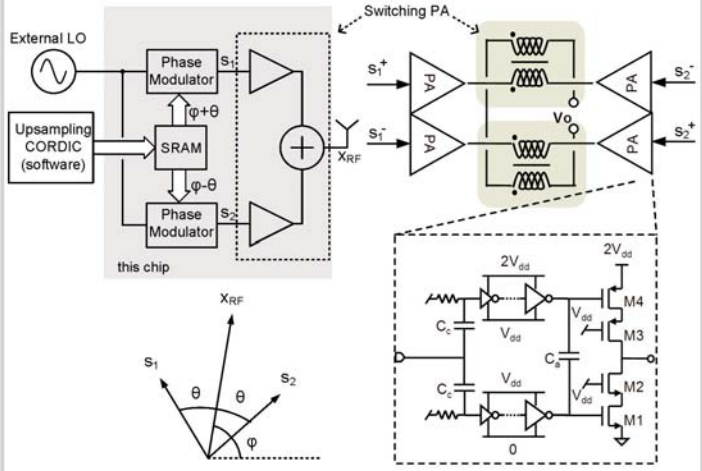


Figure 9.4.1: Diagram of the implemented outphasing digital transmitter; on the right PA architecture and circuit details of PA unit cell.

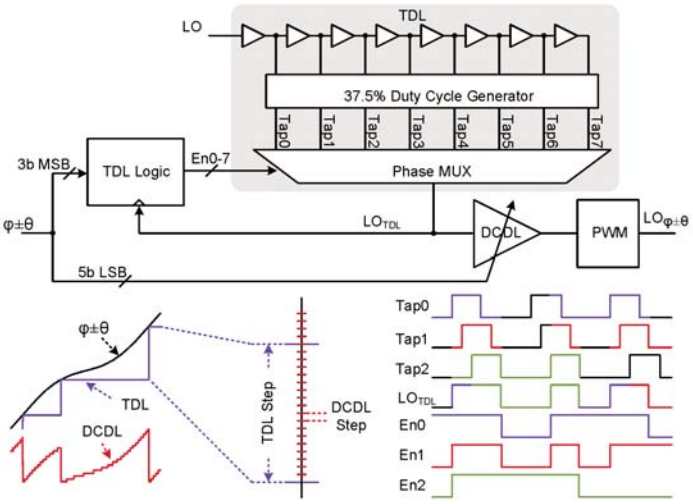


Figure 9.4.2: Open-loop phase modulator diagram and timing diagram showing glitch-free TDL operation.

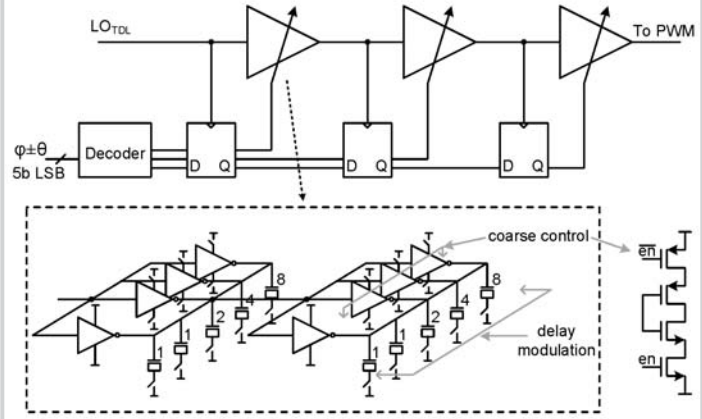


Figure 9.4.3: Diagram of the DCDL (including self-retiming) and circuit implementation of each delay stage.

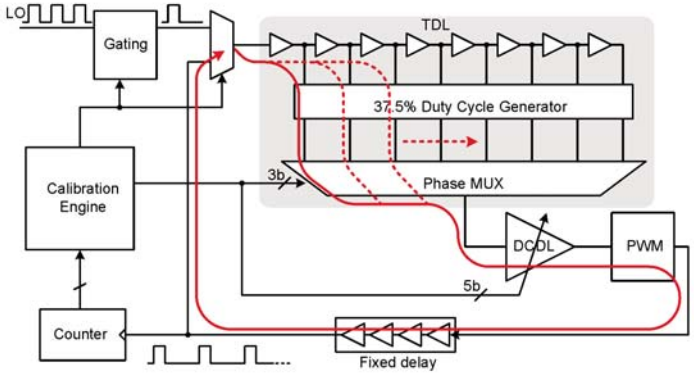
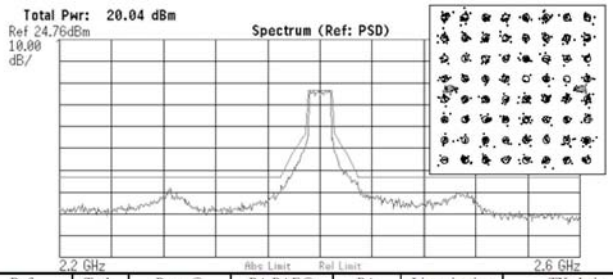


Figure 9.4.4: Calibration of phase-modulator mismatch: the modulator is configured as a ring oscillator, whose period is measured with a counter.



Ref	Tech.	P_{AVG} @ -25dB EVM	PA PAE@ -25dB EVM	PA Supply	Linearization	TX chain Power
C.P. Lee ISSCC '10	65nm	21dBm	N/A	3.3V	Yes	97mW
O. Degani ISSCC '08	90nm	18dBm	29%	3.3V	Yes	154mW (Tx eff on conf slide)
M. Terrovitis ESSCIRC '09	130nm	20dBm	13.4%	3.3V	Yes	N/A
H. Lakdawala ISSCC '12	32nm	20.3dBm	14% (total TX eff.)	1.8V	No	N/A
This work	**32nm**	**20dBm**	**22%**	**2.05V**	**No**	**82mW**

Figure 9.4.5: Measured spectrum and constellation (EVM = -25dB) at maximum power with 802.11g signal and comparison table.

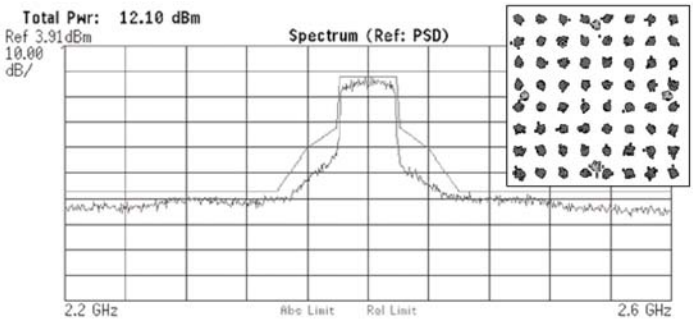


Figure 9.4.6: Measured spectrum and constellation (EVM = -28dB) with 802.11n 40MHz MCS7 signal.

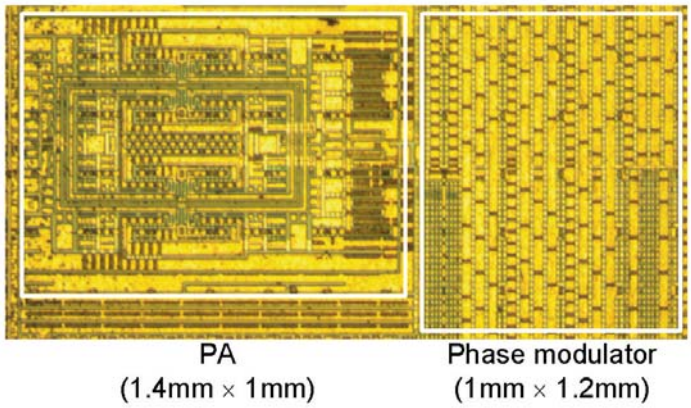


Figure 9.4.7: Die micrograph of the digital outphasing transmitter.

978-1-4673-0377-4/12/$31.00