Behavioral Modeling for Operational Amplifier in Sigma-Delta Modulators with Verilog-A

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***Abstract*—This paper presents the behavioral models for Operational amplifier (Opamp) by using analog hardware description language, Verilog-A. The Opamp's behavioral model is built with limited unit-gain bandwidth, slew-rate and nonlinear gain. A hyperbolic tangent model has been used to describe the nonlinearity of the Opamp's gain, which provides the error less than 0.26% against the transistor-level implementation. During the simulation of Sigma-Delta Modulator, the Switch-capacitor circuits and comparator are implemented in transistor level, simulations are performed at the transistor and behavioral mixed level, thus the error caused by time sequence has been introduced into the simulation results. The comparative results show that the Verilog-A model for Opamp incurs an error of no more than 0.3 dB in the magnitude of harmonics while providing a 15x advantage in the simulation speed with respect to transistor-level implementations.**

Key words: Verilog-A, Opamp, tanh, SDM.

I. INTRODUCTION

Sigma-Delta Modulator (SDM) is widely used in the applications requiring high A/D conversion with narrow bandwidth. And it can provide extremely high resolution ADC without relatively high performance of the analog circuit and high accuracy device matching. The recent research shows that SDM has the potential to fulfill the requirement of high speed, high-resolution and low-power mixed-signal interface.

Simulation is fundamental step in the design cycle. Especially to the SDM design, simulation is irreplaceable to examine the stability of the system, and to obtain accurate results. As the complexity of the SDM increased, the transistor-level simulation becomes prohibitive due to the unacceptable long running time. For this reason, it is usually left only to the final verification of the design. This situation has led circuit designers to consider alternate modeling techniques.

The most commonly used simulation approaches are based on finite-difference equations. They provide for easy code writing and fast simulation speeds [1]. However these methods do not consider several nonidealities of interest. Look-up table methodologies have also been proposed [2]. Their main disadvantage is the need to generate new tables when parameter values are changed. Hyperbolic tangent model is a good approximation to the actual Opamp's input-output characteristics, but the limited DC gain, UGB and SR have not been modeled to K. Abdelfattah and B. Razavi's research [3].Other simulation techniques based on behavioral models of sub-circuits have also been reported [4] From these methods, the simulation of using behavioral models has become the focus of attention for a large portion of the design community. Behavioral models offer the designer a set of reusable building blocks that represent components and nonidealities. Moreover, this approach brings the simulation of mixed-signal circuits closer to logic simulation, which is a more time-efficient and practical solution.

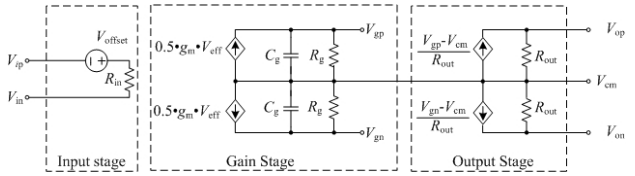

Figure 1. The small signal model of Opamp

This paper presents a Verilog-A model for Opamp where proper representations of nonideality are considered. Since the simulations are performed on transistor and behavioral mixed-level, special attention has been given to the operational amplifier because that its nonideality largely affect the performance of SDM.

II. OPERATIONAL AMPLIFIER MODEL

Incomplete charge transfer constitutes one of the main error sources in SC circuits. Particularly for SDM, this non-ideal effect is dominated by three characteristic s of the operational amplifiers [5]:

1. Finite unit-gain-bandwidth (UGB).
2. Finite Slew-Rate (SR) or limitation of the output voltage charge rate.
3. Finite and nonlinear DC open loop gain.

The proposed Verilog-A model for Opamp is built based on the small signal model of the differential amplifier as

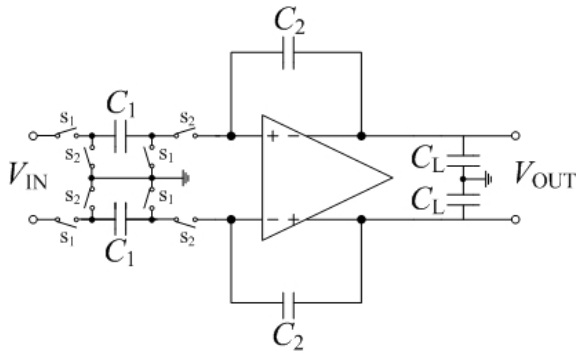

Figure 2. Switch-capacitor integrator with an Opamp

shown in Fig.1, the pins of the Verilog-A model are given in Table. I. Table. II shows the parameter of the Opamp's behavioral model which include UGB, SR and DC gain. Table. III shows the internal variable which are used in Fig. 1.

TABLE I. PIN OF THE VERILOG-A OPAMP MODEL

Pin	Description
Vip	Differential positive input voltage
Vin	Differential negative input voltage
Vop	Differential positive output voltage
Von	Differential negative output voltage
Vcm	Common mode output voltage
Vsp	Positive supply voltage
Vsn	Negative supply voltage

TABLE II. PARAMETERS OF THE VERILOG-A OPAMP MODEL

Parameters	Description
Gain	DC open loop gain of the Opamp
UBW	Unit gain bandwidth of the Opamp
R_{in}	Input resistance of the Opamp
I_{max}	Maximum tail current
SR	Slew rate of the Opamp
R_{out}	Output resistance of the Opamp
V_{offset}	Offset voltage of the Opamp

TABLE III. INTERNAL VARIABLES OF THE VERILOG-A OPAMP MODEL

Internal Variables	Description
C_g	Output capacitance of the gain stage
g_m	Circuit's transconductance
R_g	Output resistance of the gain stage
V_{max_IN}	Maximum input voltage
V_{eff}	Effective differential input voltage
V_{gp}	Positive output voltage of the gain stage
V_{gn}	Negative output voltage of the gain stage

The relation ship between the parameters and internal variables are shown below.

$$C_g = I_{max} / SR \,. \tag{1}$$

$$g_m = 2 \times \pi \times UGB \times C_g \,. \tag{2}$$

$$R_g = Gain / g_m \,. \tag{3}$$

$$V_{max\_in} = I_{max} / g_m \,. \tag{4}$$

$$V_{eff} = V_{ip} - V_{in} + V_{offset} \,. \tag{5}$$

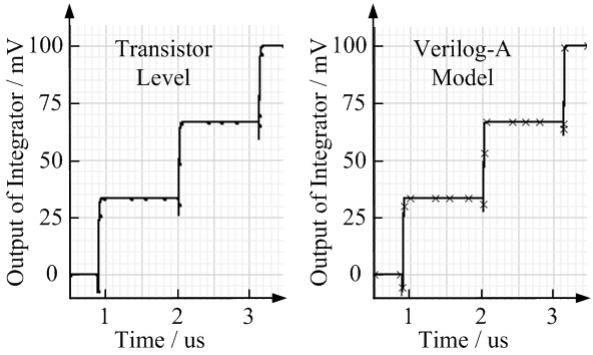

Figure 3. Simulation results of Switch-capacitor integrator

Fig.2 shows the topology of a switch-capacitor (SC) integrator, where C_1 is the sampling capacitor, C_2 is the integration capacitor, C_L is the load capacitor, C_P is the parasitic capacitor of the input transistors of the Opamp, V_a is the differential voltage on the input of the Opamp. According to the analysis on [5], The value of $V_a(t)$ immediately after the commutation of the switches is obtained by applying the principle of charge conservation slightly before and after the commutation, resulting in:

$$V_{ai} = -\frac{C_1}{C_{eq}}\left(1 + \frac{C_L}{C_2}\right) V_{IN} \,. \tag{6}$$

Where

$$C_{eq} = C_1 + C_P + C_L\left(1 + \frac{C_1 + C_P}{C_2}\right). \tag{7}$$

If $|V_{ai}| > V_{max\_IN}$, the slewing time t_0 can be defined as:

$$t_0 = -\frac{C_{eq}}{g_m} + \frac{C_1}{I_{max}}\left|V_{IN}\right|\left(1 + \frac{C_L}{C_2}\right). \tag{8}$$

Thus, based on the value of V_{ai}, V_{max_IN} and t_0, the transient response of SC-integrator can be distinguished into three cases:

1. $|V_{ai}| < V_{max\_IN}$: in this case, the operation of the circuit shown in Fig.2 is linear, that is the amplifier is not saturated in current. The transient response is described by Eq. (9) shown in the bottom of this page.
2. $|V_{ai}| > V_{max\_IN}$ and $t < t_0$: in this case, the amplifier provides constant output current of value I_{max} to charge C_2 and C_L. Thus the transient response is described as Eq. (10) shown in the bottom of this page.
3. $|V_{ai}| > V_{max\_IN}$ and $t > t_0$: in this case, the amplifier returns to its linear region again. The transient response is described as Eq. (11) shown in the bottom of this page.

In the SDM applications, case 2 and 3 are happened at the most of time. Fig.3 shows the simulation results of SC-integrator with transistor level and Veirlog-A model Opamp respectively. In such simulations, switches implemented with

NMOS and PMOS transistors, and the Opamp is implemented

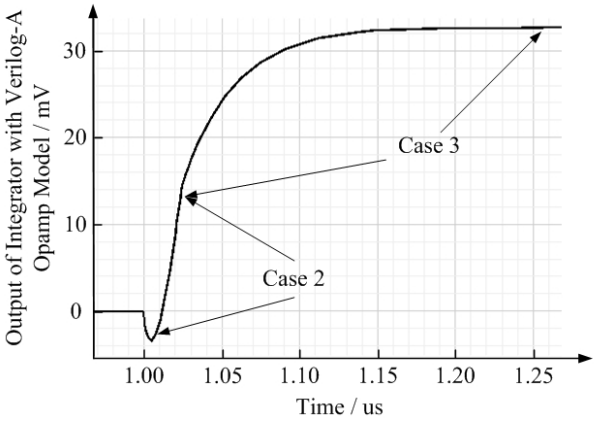

Figure 4. Details of Simulation results of Switch-capacitor integrator with Verilog-A Opamp model.

with TSMC 0.35um technology with cascode structure.

Fig.4 shows the detail of the Verilog-A model's simulation result. It can be seen that the output voltage first jumps in the opposite direction to that of final increase due to the charge conservation[5], then follows the transient response function described in case 2 and 3.

III. NONLINEARITY MODEL OF OPERATIONAL AMPLIFIER

In the section II, an Opamp with constant gain has been modeled. In order to model the harmonic distortion of the Opamp, the nonlinearity of Opamp's gain should be realized. According to K. Abdelfattah and B. Razavi's research, a simple hyperbolic tangent provides an analytical approximation of the input-output characteristic of the Opamp in transistor level.

The input-output characteristics are described as [3]:

$$V_{\mathrm{OUT}} = a \times \tanh\left(b \times V_{\mathrm{IN}}\right) = g\left(V_{\mathrm{IN}}\right). \tag{12}$$

Where $f(V_{\mathrm{IN}})$ is the input-output characteristics of the Opamp in transistor level.

According to K. Abdelfattah and B. Razavi's research, in order to minimize the error between $g(V_{\mathrm{IN}})$ and the actual characteristics $f(V_{\mathrm{IN}})$, the parameter a and b need to fulfill such restrictions [3]:

$$\left.\frac{d}{dV_{\mathrm{IN}}} g\left(V_{\mathrm{IN}}\right)\right|_{V_{\mathrm{IN}}=0} = a \times b = \left.\frac{d}{dV_{\mathrm{IN}}} f\left(V_{\mathrm{IN}}\right)\right|_{V_{\mathrm{IN}}=0}. \tag{13}$$

$$a \times \tanh\left(b \times \pm V_{\mathrm{IN.max}}\right) = f\left(\pm V_{\mathrm{IN.max}}\right). \tag{14}$$

According to Eq.(13), the gain of the hyperbolic tangent model is $a \times b$, since the parameter "*Gain*" has already in the Verilog-A model, only parameter "*b*" is added.

According to the input-output characteristic of the Verilog-A model is

$$V_{\mathrm{OUT}} = Gain \times V_{\mathrm{IN}}. \tag{15}$$

The parameter *Gain* is modified with hyperbolic tangent model with new parameter *b*.

$$Gain\_fix = \frac{Gain \times \tanh\left(b \times V_{\mathrm{IN}}\right)}{b \times V_{\mathrm{IN}}}. \tag{16}$$

Fig.5 shows the input-output characteristics of transistor level circuit and Verilog-A model. Fig. 6 shows the error voltage between two output voltages. It can be seen that the maximum error voltage is 16mV, only 0.26% to the 6V differential output voltages.

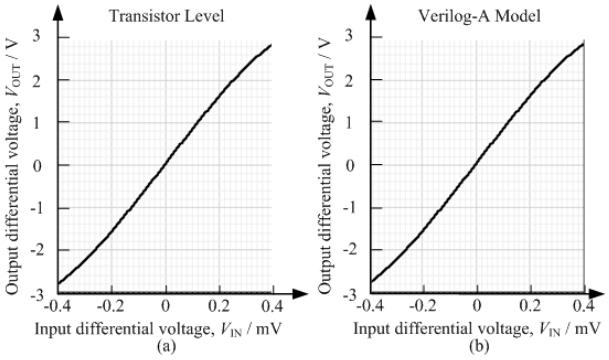

Figure 5. The input-output characteristics of Verilog-A model and transistor level circuit

As expected, such a small error leads to accurate prediction of harmonic components in closed-loop circuits.

$$V_{\mathrm{OUT}}(t) = \frac{V_{\mathrm{OUT,n-1}} + (C_1/C_2)V_{\mathrm{IN}}}{1 + (1/g_m R_{\mathrm{OUT}})\left[1 + (C_1 + C_{\mathrm{P}})/C_2\right]} + \left[-\frac{V_{\mathrm{OUT,n-1}} + (C_1/C_2)V_{\mathrm{IN}}}{1 + (1/g_m R_{\mathrm{OUT}})\left[1 + (C_1 + C_{\mathrm{P}})/C_2\right]} + V_{\mathrm{OUT,n-1}} - (C_1/C_{eq})V_{\mathrm{IN}}\right] \exp\left(-\frac{g_{\mathrm{m}}C_2 + (1/R_{\mathrm{OUT}})(C_1 + C_2 + C_{\mathrm{P}})}{C_2 C_{\mathrm{eq}}} t\right). \tag{9}$$

$$V_{\mathrm{OUT}}(t) = V_{\mathrm{OUT,n-1}} + \frac{C_1}{C_2}V_{\mathrm{IN}} + \left(1 + \frac{C_1 + C_{\mathrm{P}}}{C_2}\right)\left\{-\frac{C_1(C_2 + C_{\mathrm{L}})}{C_{\mathrm{eq}}C_2}V_{\mathrm{IN}} + \frac{I_{\max}\,\mathrm{sgn}(V_{\mathrm{IN}})}{C_{\mathrm{eq}}}t\right\}. \tag{10}$$

$$V_{\mathrm{OUT}}(t) = V_{\mathrm{OUT,n-1}} + \frac{C_1}{C_2}V_{\mathrm{IN}} + \left(1 + \frac{C_1 + C_P}{C_2}\right)\left\{-\frac{V_{\mathrm{OUT,n-1}} + (C_1/C_2)V_{\mathrm{IN}}}{1 + g_m R_{\mathrm{OUT}} + (C_1 + C_{\mathrm{P}})/C_2} + \left[\frac{V_{\mathrm{OUT,n-1}} + (C_1/C_2)V_{\mathrm{IN}}}{1 + g_m R_{\mathrm{OUT}} + (C_1 + C_P)/C_2} - \frac{I_{\max}\,\mathrm{sgn}(V_{\mathrm{IN}})}{g_{\mathrm{m}}}\right]\right\} \times \exp\left(-\frac{g_{\mathrm{m}}C_2 + (1/R_{\mathrm{OUT}})(C_1 + C_2 + C_{\mathrm{P}})}{C_2 C_{\mathrm{eq}}}(t - t_0)\right). \tag{11}$$

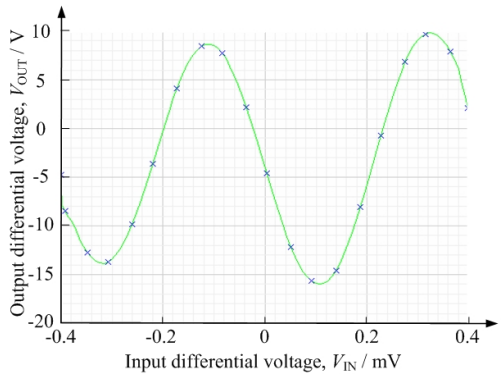

Figure 6. The error between transistor level and Verilog-A model

For example, the simple continuous-time amplifier depicted in Fig. 7(a) exhibits the output spectra shown in Figs. 7(b) with transistor level and Verilog-A model Opamp, respectively. The error in the harmonic magnitudes is less than 0.01 dB.

IV. SDM Simulation with Verilog-A Opamp Model

The proposed methodology serves as a powerful tool for analyzing SDM, allowing the inclusion of various architectural concepts as well as circuit nonidealities in platforms such as Spectre. Furthermore, Verilog-A behavioral model can be simulated with transistor level blocks in many simulators such as Spectre, thus it provides many choices between efficiency (behavioral model only) and accuracy (transistor level only), which can not be done with Matlab.

The Verilog-A Opamp model has been used in a second order SDM design with 1-bit quantizer as shown in Fig.8. Except the Opamp, the other parts of the circuits are implemented with transistors and capacitors. Fig. 9(a) shows the output spectrum obtained from Cadence for a modulator with transistor-level implementation for all circuits, and Fig. 9(b) plots the simulation result with Verilog-A Opamp model. The behavioral simulation incurs an error of 0.3 dB in the magnitude of the harmonics while providing a 15x advantage in simulation speed (62 minutes versus 15.7 hours).

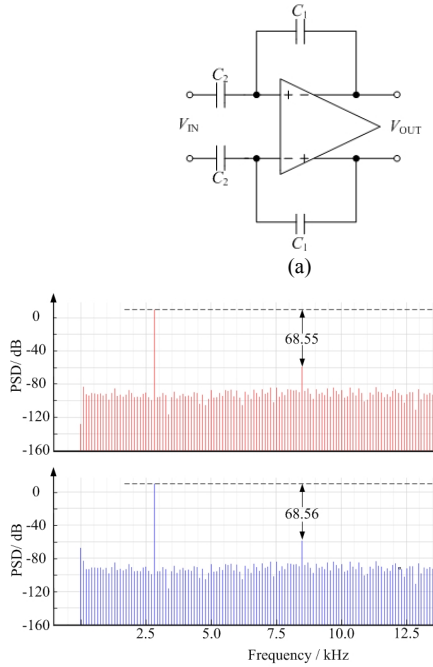

Figure 7. (a) Continuous-time amplifier, (b) output spectrum with transistor level and Verilog-A model Opamp

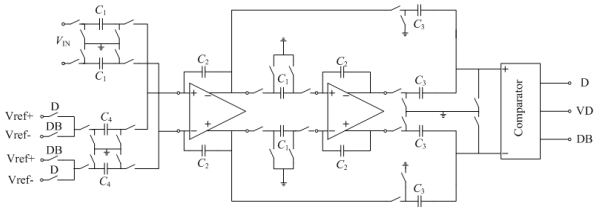

Figure 8. The second order SDM

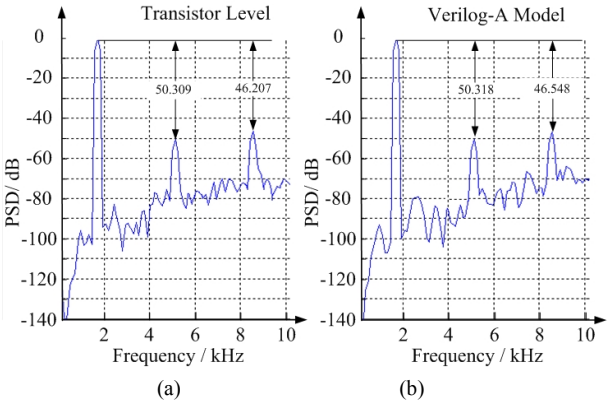

Figure9. PSD of SDM with (a) transistor level and (b) Veirlig-A model Opamp

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