A DCVSL Delay Cell for Fast Low Power Frequency Synthesis Applications

Didem Z. Turker, *Student Member, IEEE*, Sunil P. Khatri, *Member, IEEE*, and Edgar Sánchez-Sinencio, *Life Fellow, IEEE*

***Abstract*—In this paper, a low-cost, power efficient and fast Differential Cascode Voltage-Switch-Logic (DCVSL) based delay cell (named DCVSL-R) is proposed. We use the DCVSL-R cell to implement high frequency and power-critical delay cells and flip-flops of ring oscillators and frequency dividers. When compared to TSPC, DCVSL circuits offer small input and clock capacitance and a symmetric differential loading for previous RF stages. When compared to CML, they offer low transistor count, no headroom limitation, rail-to-rail swing and no static current consumption. However, DCVSL circuits suffer from a large low-to-high propagation delay, which limits their speed and results in asymmetrical output waveforms. The proposed DCVSL-R circuit embodies the benefits of DCVSL while reducing the total propagation delay, achieving faster operation. DCVSL-R also generates symmetrical output waveforms which are critical for differential circuits. Another contribution of this work is a closed-form delay model that predicts the speed of DCVSL circuits with 8% worst case accuracy. We implement two ring-oscillator-based VCOs in 0.13 μm technology with DCVSL and DCVSL-R delay cells. Measurements show that the proposed DCVSL-R based VCO consumes 30% less power than the DCVSL VCO for the same oscillation frequency (2.4 GHz) and same phase noise (-113 dBc/Hz at 10 MHz). DCVSL-R circuits are also used to implement the high frequency dual modulus prescaler (DMP) of a 2.4 GHz frequency synthesizer in 0.18 μm technology. The DMP consumes only 0.8 mW at 2.48 GHz, a 40% reduction in power when compared to other reported DMPs with similar division ratios and operating frequencies. The RF buffer that drives the DMP consumes only 0.27 mW, demonstrating the lowest combined DMP and buffer power consumption among similar synthesizers in literature.**

***Index Terms*—Alpha-power model, current mode logic (CML), differential cascode voltage switch logic (DCVSL), DCVSL-R, frequency divider, frequency synthesizers, oscillator, prescaler, propagation delay, phase locked loops, TSPC, ZigBee.**

I. Introduction

As handheld and wireless devices become a central part of everyday life, low-power circuit techniques are becoming increasingly important for enhanced battery life. The frequency synthesizer is one of the key building blocks of any wireless transceiver system. Since it is active during both transmit and receive modes, the frequency synthesizer consumes a significant fraction of the overall power.

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The authors are with the Department of Electrical and Computer Engineering, Texas A&M University, College Station, TX 77843-3128 USA (e-mail: didem@tamu.edu).

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The key power-hungry circuits in a frequency synthesizer are the voltage-controlled oscillator (VCO) and the frequency dividers [1], especially the programmable dividers that operate at the RF frequency. Another power hungry block is the RF buffers between the VCO and the frequency dividers. Along with frequency of operation and technology speed, the circuit design technique of the frequency dividers is key in determining their and their driving buffer's power consumption. Until recently, Current Mode Logic (CML) circuits [2], [3] were widely employed in the frequency dividers of synthesizers [4], [5] because they could operate at high frequencies. With the migration towards sub-micron technologies, digital dynamic-circuit techniques such as True-Single-Phase Clocking (TSPC) are becoming popular [6]–[8] to optimize the power consumption of high-speed frequency dividers.

In this paper, we explore the Differential Cascode Voltage-Switch Logic (DCVSL) circuit design methodology, and propose an improvement to DCVSL for use in the RF dividers of a frequency synthesizer. The key benefits of DCVSL are its low input capacitance, differential nature (providing symmetrical loading for the VCO and RF buffers), and low power consumption. However, DCVSL delay cells have a delay asymmetry; their low-to-high-transition propagation delay ($\tau_{\rm PLH}$) is inherently larger than their high-to-low-transition propagation delay ($\tau_{\rm PHL}$). The large $\tau_{\rm PLH}$ presents a speed bottleneck for the DCVSL cells and results in asymmetric differential output waveforms where the rising output lags the falling output. While the discrepancy between the two differential outputs is addressed in a few earlier works [9], [10], a detailed analysis of the inherent delay problem is not presented, and the resulting solutions are not suitable for high frequency applications.

The outline of this paper is as follows. Section II discusses various circuit topologies and offers DCVSL circuits as a candidate to implement the RF frequency dividers of frequency synthesizers. Section III analyzes the delay behavior of DCVSL inverters and proposes a closed-form model to describe the inherent delay asymmetry of the DCVSL circuits. Then, in Section IV we propose a circuit solution, which we term Differential Cascode Voltage Switch Logic with Resistive-enhancement (DCVSL-R), to overcome this delay asymmetry and reduce $\tau_{\rm PLH}$ and hence reduce the total propagation delay $\tau_{\rm PLH}+\tau_{\rm PLH}$. Since DCVSL-R resolves the asymmetric output problem of DCVSL circuits, it can better implement the differential clock signals for the following stages of dividers and ring oscillators. It also features smaller parasitic capacitances in it's input and output nodes, when compared to it's counterparts

such as CML and TSPC. Therefore, DCVSL-R achieves faster operation while maintaining rail-to-rail swing and low power operation.

We explore the use of the proposed circuit in high-frequency programmable dividers of low-power synthesizers, and in the delay cells of ring oscillators. Section V discusses the implementation of two ring-oscillator-based VCOs in 0.13 μm CMOS technology, that utilize DCVSL and DCVSL-R delay cells and demonstrates the performance improvement of the latter through measurements. Then, in Section VI we implement a frequency synthesizer in 0.18 μm CMOS technology that uses the proposed DCVSL-R technique in it's RF dual modulus prescaler (DMP). The frequency synthesizer generates 2.4 GHz quadrature outputs and it's measured performance is suitable for low power transceiver applications such as IEEE 802.15.4/ZigBee. We demonstrate that, the DCVSL-R based DMP achieves 40% lower power when compared to other similar reported DMPs that employ other circuit techniques, and decreases the power consumption of the high-frequency buffer that drives it. Section VII concludes this paper.

The key contributions of this paper are summarized below.

- An improved circuit (DCVSL-R) with advantages of symmetric τ_{PLH} and τ_{PHL}, lower total delay, small clock capacitance.
- Replacement of DCVSL delay cells in ring oscillators with DCVSL-R cells to achieve power reduction for a desired oscillation frequency, or speed improvement for a desired power budget, without sacrificing phase noise.
- The first use of a DCVSL style design for high frequency dividers of a synthesizer in literature, to reduce the power consumption of the dividers and their driving buffers, and to provide symmetrical loading to VCO.
- A closed-form model to estimate the value of propagation delay in DCVSL circuits.
- Validation of the above points via measurements of a 0.18 μm synthesizer and 0.13 μm ring oscillators.

II. Circuit Techniques for Frequency Dividers

A commonly used circuit technique in the high frequency dividers of wireless radio synthesizers is CML [4], [5]. A CML latch is shown in Fig. 1. CML circuits enable high-speed operation with small signal swing. Their constant DC bias current minimizes switching noise, and their differential nature makes them immune to common-mode noise. However, CML, though high speed, consumes considerable power due to it's DC bias current and has limited headroom due to stacked transistors. Load resistance and bias current values determine the output swing and DC common mode level, putting a lower limit on the bias current value. Moreover, a CML D-flip-flop requires two CML latches of Fig. 1, using fourteen transistors and four resistors for a single flip-flop, resulting in much more area than traditional flops.

As an alternative to CML, TSPC circuits implement the frequency dividers of wireless-radio frequency synthesizers [6]–[8]. Fig. 2 shows a rising-edge triggered TSPC D-flip-flop. They consume no static power and use fewer transistors. However, they have stacked transistors that present large bias-dependent capacitive loading. Due to these large internal

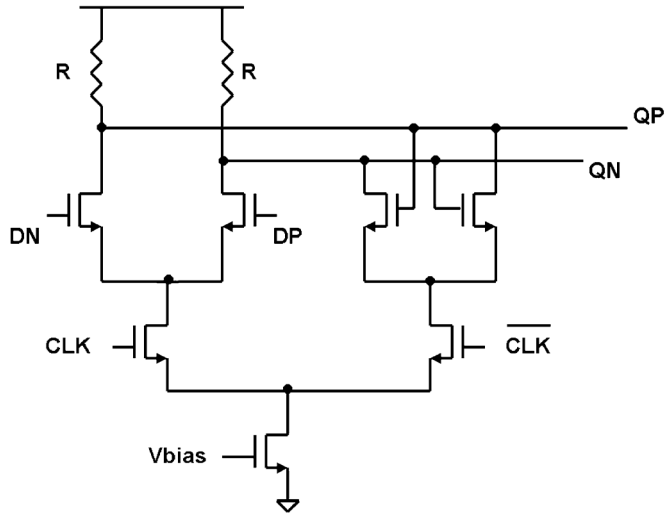


Fig. 1. Schematic of a CML latch.

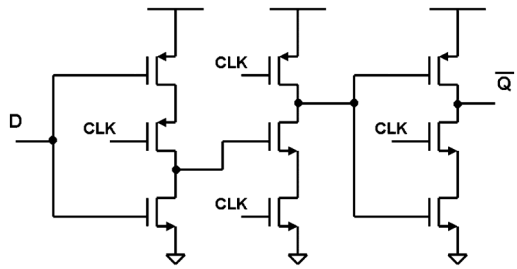


Fig. 2. Schematic of a TSPC D-flip-flop.

parasitics and the hard-switching nature of the transistors, they have high switching current peaks, leading to noise.

In a PLL, frequency dividers are driven either by a buffer or directly by the VCO, and VCO architectures are often differential. Single-ended frequency dividers such as TSPC, result in an asymmetrical loading at the VCO output, which leads to mismatch at the LO signals of a transceiver. To minimize the mismatch, dummy circuits can be used to provide symmetric loading for the VCO [7]. Such dummy circuits will not only generate additional parasitics at the RF nodes but also if left disconnected from VDD to save power, they will not completely remove mismatch. Differential-to-single-ended conversion buffers may also be employed; however, at high frequency these buffers consume large power. [6] uses such a buffer followed by an inverter chain and while the TSPC significantly reduces the dual-modulus-prescaler (DMP) power, the buffers consume as much power as the DMP. [7] uses a modified version called E-TSPC to avoid stacked transistors. This reduces buffer power but E-TSPC has charge sharing issues and static power dissipation.

The differential cascode voltage-switch-logic (DCVSL) family, first introduced in 1984, has small input gate capacitance (compared to full CMOS logic styles) and can implement complex logic functions with low transistor count [11]. A simple DCVSL inverter is shown in Fig. 3. One drawback of this circuit technique occurs while the pMOS load transistors are in latching mode. For a brief period, both pMOS and nMOS transistors in at least one of the differential branches are on

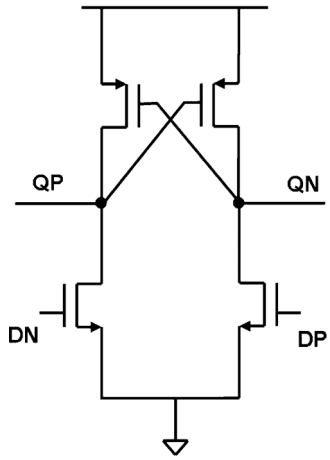


Fig. 3. Schematic of a DCVSL inverter.

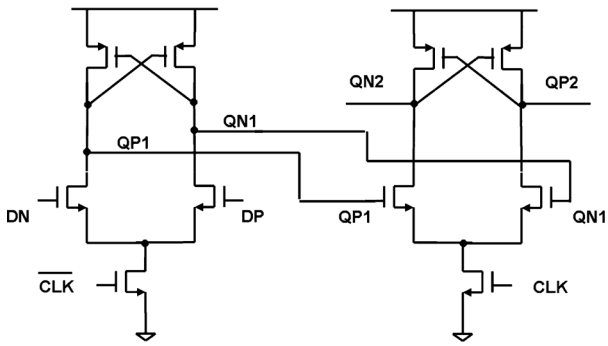


Fig. 4. Two-clock-phase DCVSL flip-flop.

at the same time, leading to crowbar current for a short time. However, this transition period also smoothens the instantaneous current switching of these logic gates and generates less switching supply noise compared to hard-switching, static, full-CMOS logic. Several DCVSL based flip-flops are discussed and compared in [12]. The D-flip-flop (DFF) of Fig. 4 shows the best candidate for high speed applications due to its simplicity and low transistor count. By avoiding precharge schemes, additional pMOS clock transistors are eliminated.

Among the various circuit families discussed in this section, we found that the non-precharge, two-phase-clocked DCVSL D-flip-flop of Fig. 4 is best suited for the frequency dividers of a synthesizer. Due to its small number of transistors, this flip-flop is fast. The whole flip-flop has only two clock transistors and no stacking, resulting in a very small clock input capacitance. Such small capacitance is crucial to minimize the clock driver buffers' power consumption. The flop has a crowbar current drawn during input transitions, yet the average power consumption is still much less than that of CML circuits. DCVSL circuits have lower power-supply glitches, as their switching capacitance is lower than that of TSPC. The pseudo-differential clocking of the DCVSL flip-flop in Fig. 4 offers symmetric loading for the VCO, preventing mismatch problems at PLL outputs. However, the DCVSL structure has an inherent delay bottleneck that limits its operation speed and results in asymmetrical outputs, as will be discussed in the next section.

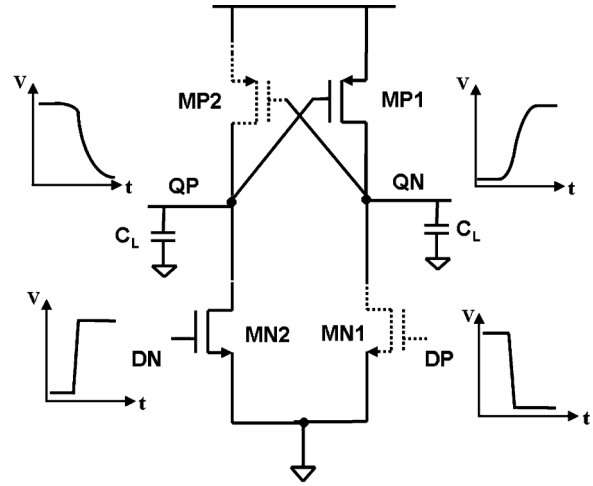


Fig. 5. DCVSL inverter setup for transient delay analysis.

III. Delay Analysis for DCVSL Circuits

Digital circuits' speed is characterized by their propagation delays, i.e., the low-to-high switching propagation delay τ_{PLH} (the delay from the input falling from logic high to low to the output rising from logic low to high) and the high-to-low switching propagation delay τ_{PHL} [13]. To understand the transient behavior of DCVSL circuits, we analyze the propagation delay of a simple DCVSL inverter. Fig. 5 shows the DCVSL inverter with a load capacitance C_L and with switching complementary inputs. Delay behavior of standard CMOS inverters were analyzed in [14]–[16]. To develop a delay model for the DCVSL inverter, we revisit the simple yet intuitive Sakurai-Newton delay model of [14] that was developed for a conventional static CMOS inverter. The transistor current-voltage equations of the alpha-power model of [14] are shown in (1), where α is a unitless technology-dependent parameter for a given transistor length and is derived from simulations as described in [14]. V_{DSO} and I_{DO} are the drain saturation voltage and drain current, respectively, of the transistor when $V_{\mathrm{GS}} = V_{\mathrm{DS}} = \mathrm{VDD}$; and V_{TH} is the threshold voltage

$$
\begin{aligned}
I_D &= I_{\mathrm{DO}} \left(\frac{V_{\mathrm{GS}} - V_{\mathrm{TH}}}{\mathrm{VDD} - V_{\mathrm{TH}}} \right)^{\alpha}, (V_{\mathrm{DS}} \geq V'_{\mathrm{DS0}}) \\
I_D &= V_{\mathrm{DS}} \frac{I_{\mathrm{DO}}}{V_{\mathrm{DSO}}} \left(\frac{V_{\mathrm{GS}} - V_{\mathrm{TH}}}{\mathrm{VDD} - V_{\mathrm{TH}}} \right)^{\frac{\alpha}{2}}, (V_{\mathrm{DS}} < V'_{\mathrm{DS0}}) \\
V'_{\mathrm{DSO}} &= V_{\mathrm{DSO}} \left(\frac{V_{\mathrm{GS}} - V_{\mathrm{TH}}}{\mathrm{VDD} - V_{\mathrm{TH}}} \right)^{\frac{\alpha}{2}}. \qquad (1)
\end{aligned}
$$

The motivation behind this analysis is to derive a closed-form model to understand the behavior of DCVSL circuits. Therefore, in our delay model derivation, we follow similar assumptions as [14] to simplify the delay equations. One such assumption is that the inverter input- and output-waveform slewrates are similar. For the target applications of the DCVSL cells in this work (delay cells of ring oscillators and frequency dividers) we can safely assume that the DCVSL cells are driven by other DCVSL cells with similar delays. Fig. 6(a) shows the inverter

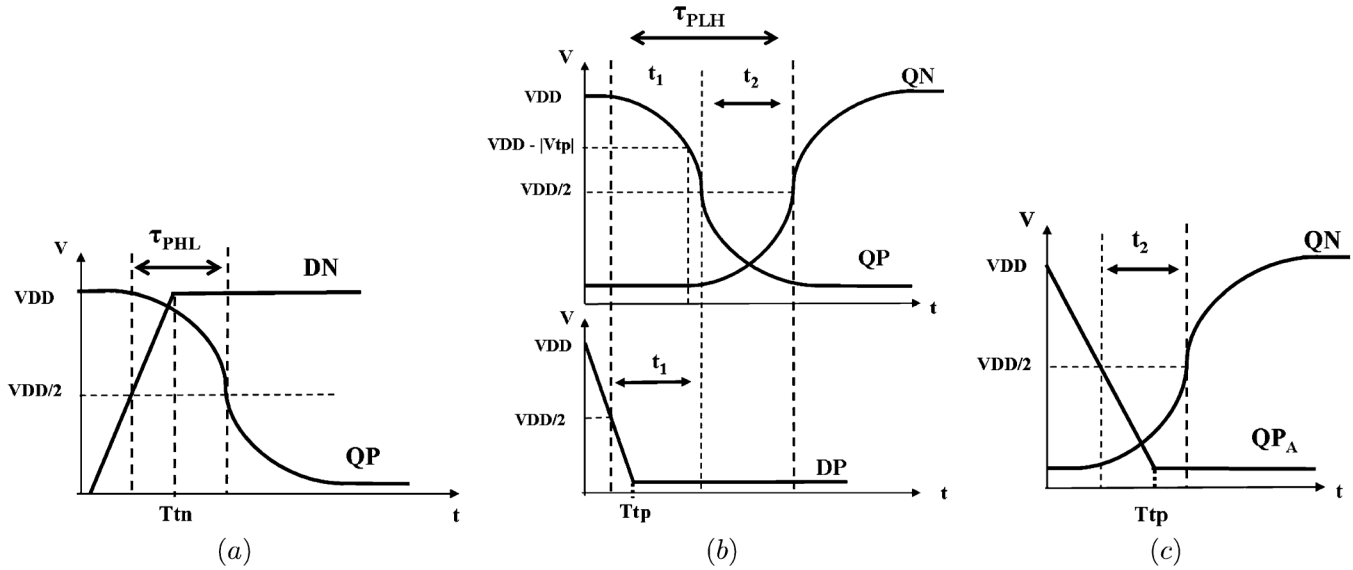


Fig. 6. Propagation delay derivations (a) $\tau_{\rm PHL}$ (b) $\tau_{\rm PLH} = t_1 + t_2$ (c) Approximation of t_2.

input and output waveforms and the propagation delay, for the case of $\tau_{\rm PHL}$. The input waveform is approximated with a linear ramp where Ttn is the rising-input-waveform transition time (likewise, falling-input transition time will be referred to as Ttp for the case of $\tau_{\rm PLH}$). For the inverter under analysis, the nMOS driver transistor generates the rising input signal, and the pMOS load generates the falling input. Then, Ttn and Ttp can be approximated as [14]

$$T_{\rm tn} = C_L \frac{\rm VDD}{I_{\rm DOP}} \left(\frac{0.9}{0.8} + \frac{V_{\rm DSOP}}{0.8 \times \rm VDD} \ln \left(\frac{10 \times \rm VDD}{e \times \rm VDD} \right) \right)$$
$$T_{\rm tp} = C_L \frac{\rm VDD}{I_{\rm DON}} \left(\frac{0.9}{0.8} + \frac{V_{\rm DSON}}{0.8 \times \rm VDD} \ln \left(\frac{10 \times \rm VDD}{e \times \rm VDD} \right) \right). \quad (2)$$

where C_L is the load capacitance; $I_{\rm DOP}, V_{\rm DSOP}$ and $I_{\rm DON}, V_{\rm DSON}$ are the drain currents; and saturation voltages of the pMOS and nMOS transistors of the driving stage, respectively.

We also assume that the input waveform reaches its final value before the output reaches VDD/2, i.e., the point where propagation delay is measured. Moreover, to derive $\tau_{\rm PHL}$, (when DN is the rising input and QP is the falling output as shown in Fig. 6(a)), we ignore the current conducted by MP2 before this transistor turns off completely. Therefore, we assume that QP is pulled down solely by MN2 (later, we will add a correction factor to the delay expression to compensate for this assumption). Then, the derivation of $\tau_{\rm PHL}$ of a DCVSL inverter is similar to that of a standard CMOS inverter, and we can use the the expression derived in [14]

$$\tau_{\rm PHL} = \tau_{05\_\rm HL} - \frac{T_{\rm tn}}{2} \quad (3)$$

where

$$\tau_{05\_\rm HL} = T_{\rm tn} \left(\frac{v_{\rm TN} + \alpha_N}{1 + \alpha_N} + C_L \frac{\rm VDD}{2 I_{\rm DON}} \right) \quad (4)$$

and

$$v_{\rm TN} = \frac{V_{THN}}{\rm VDD}, v_{\rm TP} = \frac{V_{\rm THP}}{\rm VDD} \quad (5)$$

are the ratios of the threshold voltages of nMOS and pMOS transistors to the supply voltage.

To derive $\tau_{\rm PLH}$ of a DCVSL inverter, Fig. 6(b) shows the case where the QN output is rising. Note that MP1, the transistor that pulls QN up, is triggered by QP, not DP. In other words, the input signal for the rising output QN, is QP. However, propagation delay $\tau_{\rm PLH}$ is defined as the delay between the time when the rising output (in this case QN) and the falling input (DP) of the inverter reaches VDD/2. Then, as shown in Fig. 6(b), we can represent $\tau_{\rm PLH}$ as the summation of two delay components, t_1 and t_2.

$$\tau_{\rm PLH} = t_1 + t_2 \quad (6)$$

where t_1 is determined by the speed of the nMOS pull-down transistor MN2 and is given by (7)

$$t_1 = \tau_{05\_\rm LH} - \frac{T_{\rm tp}}{2}. \quad (7)$$

To find t_2, we approximate QP as a linear ramp, just as we do with the input signals DN and DP when deriving (2), since we assumed that the input and output signals have similar slew-rates. Then, we obtain t_2 just like we found $\tau_{\rm PHL}$, as shown in Fig. 6(c) where $\rm QP_A$ is the linearly approximated QP

$$t_2 = T_{\rm tp} \left(\frac{v_{\rm TP} + \alpha_P}{1 + \alpha_P} + C_L \frac{\rm VDD}{2 I_{\rm DOP}} \right) - \frac{T_{\rm tp}}{2}. \quad (8)$$

As mentioned earlier, the expressions for $\tau_{\rm PHL}$ and $\tau_{\rm PLH}$ (given in (3) to (8)), are derived ignoring the brief current conduction of nMOS transistor (MN1) for $\tau_{\rm PLH}$ and that of pMOS loads (MP2) for $\tau_{\rm PHL}$. This assumption results in optimistic delay expressions. In reality, for $\tau_{\rm PHL}$, the pMOS load transistor conducts crowbar current during the output transition, reducing the output-node discharge current to be less than $I_{\rm DN}$. This reduction creates an error factor in the delay model, that is related

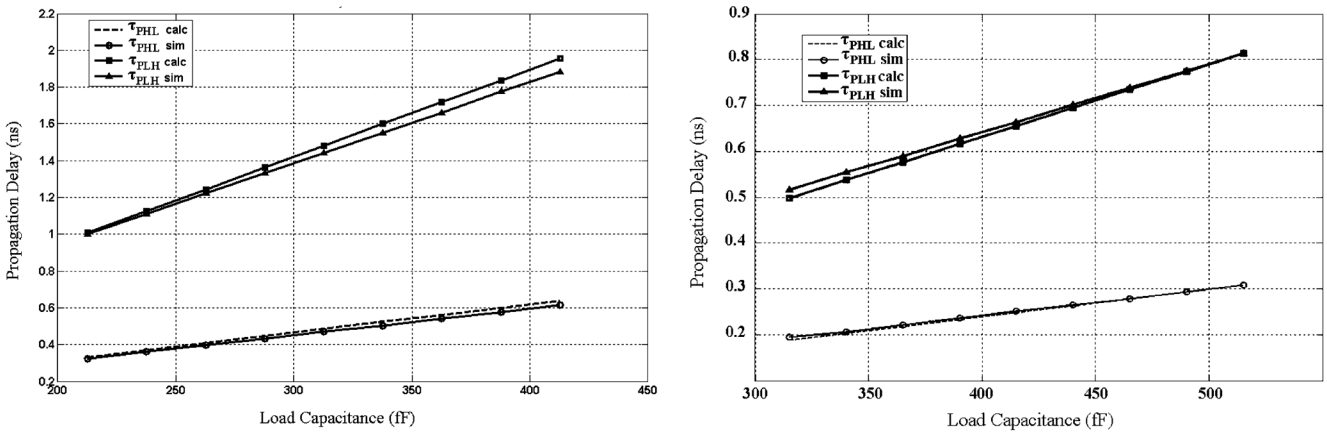


Fig. 7. Comparison of calculated versus simulated values of $\tau_{\rm PLH}$ and $\tau_{\rm PHL}$ (a) for $({\rm WP}/{\rm WN}) = 1.33$ in 0.18 μm technology (b) for $({\rm WP}/{\rm WN}) = 1.57$ in 0.13 μm technology.

to the "internal configuration ratio" (WP/WN assuming same length). The internal configuration ratio of an inverter affects the delay, particularly given deep-sub-micron-technology field effects such as velocity saturation [17]. Therefore, we propose the following DCVSL equations:

$$\tau_{\rm PHL} = K_{\rm HL} \times \left[T_{\rm tn} \left(\frac{v_{\rm TN} + \alpha_N}{1 + \alpha_N} + C_L \frac{\rm VDD}{2 I_{\rm DON}} \right) - \frac{T_{\rm tn}}{2} \right]$$

$$\tau_{\rm PLH} = K_{\rm LH} \times \left[T_{\rm tn} \left(\frac{v_{\rm TN} + \alpha_N}{1 + \alpha_N} + C_L \frac{\rm VDD}{2 I_{\rm DON}} \right) - \frac{T_{\rm tp}}{2} + T_{\rm tp} \left(\frac{v_{\rm TP} + \alpha_P}{1 + \alpha_P} + C_L \frac{\rm VDD}{2 I_{\rm DOP}} \right) - \frac{T_{\rm tp}}{2} \right] \quad (9)$$

where

$$K_{\rm HL} = \left(\gamma_N + \frac{\zeta_N}{({\rm WP}/{\rm WN})} \right)^{-1}$$

$$K_{\rm LH} = \left(\gamma_P + \frac{\zeta_P}{({\rm WP}/{\rm WN})} \right)^{-1}. \quad (10)$$

Note that γ_P, ζ_P, and γ_N, ζ_N are empirical correction factors obtainable from simulations, and should be constant across transistor sizes and loading conditions for a given technology. Note the $\tau_{\rm PLH}$ correction factor, $K_{\rm LH}$, is proportional to (WP/WN), because $\tau_{\rm PLH}$ strongly depends on the nMOS transistor, for the pMOS pull-up transistor is controlled by the falling output, as explained earlier.

The voltage dependence of the load capacitance should be considered when calculating C_L. For a DCVSL inverter under test (IUT), such as the one shown in Fig. 5, load capacitance includes the input capacitance of the following fan-out stages, interconnect capacitance of the routing and capacitance due to the pMOS load transistor of the IUT itself. Note that the transition of interest is from VDD to VDD/2 and from 0 to VDD/2 for falling and rising outputs, respectively. We demonstrated that $\tau_{\rm PLH}$ is inherently larger than $\tau_{\rm PHL}$ (the rising output waits for the falling output to begin it's transition). For the falling output QP, since QN will wait for QP, MP1 will be in saturation while QP falls to VDD/2. For the rising output QN, we can assume that QP will fall enough for MP2 to have $V_{\rm DSOP}$ before QN begins rising, due to the inherent delay asymmetry of DCVSL. Then, MP2 will be in saturation during the transition of QN from 0 to VDD/2. Therefore, we safely assume that the pMOS transistors of the IUT (MP2 for QN and MP1 for QP) contribute saturation gate capacitance to the output. Similar analysis can be performed to the gate capacitance of the following fan-out stages to determine their operating region and capacitance.

To test the accuracy of the proposed delay models of (9), we compare the calculated delay values to the results of schematic simulations, for 0.18 μm and 0.13 μm CMOS technologies. To simulate realistic input and output waveforms for the target applications, we place DCVSL inverters in a three-stage ring oscillator setting with capacitive loading at each stage and vary the load capacitors as well as transistor sizes. Fig. 7(a) and (b) compare the calculated values of $\tau_{\rm PLH}$ and $\tau_{\rm PHL}$ from (9) to their circuit-level simulated values for 0.18 μm and 0.13 μm technologies, respectively. Table I lists the simulated and calculated values of the propagation delays for various transistor ratios as well as the values of γ_N, γ_P and ζ_N, ζ_P that we use for each technology. Note that the model error—defined as the ratio of the difference between the calculated and simulated delays over the simulated delay—is within $\pm 4\%$ for $\tau_{\rm PHL}$ and within $\pm 8\%$ for $\tau_{\rm PLH}$, quite good for a closed-form model that avoids complex expressions and provides insight to the designer.

The proposed model is also tested over the process corners provided in the technology model. The empirical correction factor values given in Table I are used over process corners. It is observed that all of the errors reported in Table I are still within the reported 8% worst case accuracy. Therefore, the sensitivity of the proposed model and empirical factors to process variations is minimal.

The delay analysis shows that the rising output of a DCVSL cell is inherently lagging the falling output since the pMOS that pulls the rising output up, has to wait for the falling output. The delay expressions of (9) show that $\tau_{\rm PLH}$ has an extra delay component when compared to $\tau_{\rm PHL}$ and therefore is larger. Note that increasing the size of pMOS loads to decrease t_2 of $\tau_{\rm PLH}$, increases the load capacitance and the overall delay of the inverter. Also, increasing the size of pMOS loads to have similar

TABLE I
A LIST OF CALCULATED AND SIMULATED VALUES OF $\tau_{\rm PLH}$ AND $\tau_{\rm PHL}$ FOR VARIOUS TRANSISTOR CONFIGURATIONS

Technology	$\frac{WP}{WN}$	τ_{PLH} (ps) calculated	τ_{PLH} (ps) simulated	τ_{PLH} error	τ_{PHL} (ps) calculated	τ_{PHL} (ps) simulated	τ_{PHL} error
TSMC 0.18μm γ_N=0.26 γ_P=0.36 ζ_N=0.403 ζ_P=0.245 α_N=1.1 α_P=1.4	1	1528	1420	7.6 %	410.6	398.7	2.9 %
	1.33	1719	1660	3.5 %	562.5	543	3.6 %
	1.66	1499	1586	-5.4 %	578.4	584.2	-1 %
	0.8	1381	1291	7 %	322.2	381.1	1.3 %
	0.66	1263	1208	4.5 %	264.8	267.7	-1.1 %
	0.5	1439	1454	-1 %	258.2	261.1	-1.1 %
	1.19	1495	1417	5.5 %	451.1	436.6	3.3 %
UMC 0.13μm γ_N=0.3 γ_P=0.39 ζ_N=0.44 ζ_P=0.28 α_N=1.3 α_P=1.5	1.57	576.7	589.7	-2.2 %	218.1	220.7	1.1 %
	1.37	550.7	545.1	1 %	192.2	192.1	0.1 %
	1.12	622.5	591.9	5.1 %	192	187.4	2.4 %
	1	534.1	509.2	4.9 %	154.9	153.4	1 %
	0.8	797	742	7.3 %	204.3	198.5	2.9 %
	0.61	745	726	2.6 %	169.6	170.7	0.6 %
	0.5	816	829	-1.5 %	170.5	172.8	-1.3 %

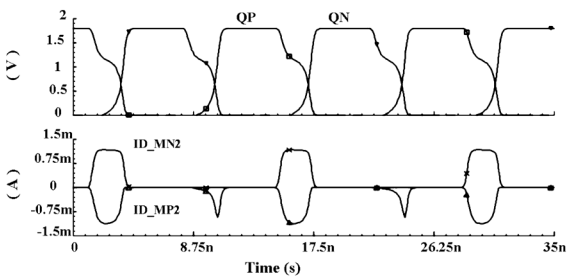


Fig. 8. Simulated voltage and current waveforms of DCVSL inverter in 0.18 μm for $\rm WP/WN = 3$.

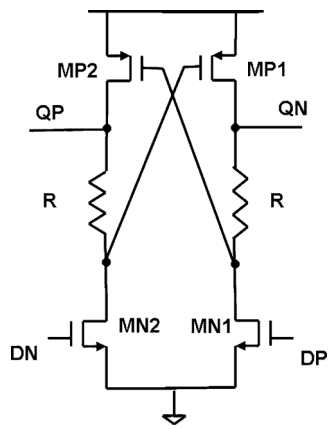


Fig. 9. Proposed DCVSL-R circuit.

current driving capability as nMOS transistors, results in a midtransition slow-down in the falling output.

To demonstrate this midtransition slow-down, we set $\rm WP/WN = 3$ in 0.18 μm technology and simulate DCVSL inverters in a ring oscillator configuration and obtain the voltage and current waveforms of Fig. 8. For the QP waveform, the slow-down occurs when MP2 and MN2 are ON simultaneously and when they have similar drain currents that compete against each other. Note that the inherent lead/lag asymmetrical shape of DCVSL output waveforms QP and QN extends the duration when pMOS and nMOS are both ON, causing this slow-down to effect $\tau_{\rm PHL}$ considerably. To avoid this slow-down, ensure that the pMOS device is sized such that its current drive is less than that of the nMOS transistor. This shows that the delay bottleneck of DCVSL circuits that stem from a large $\tau_{\rm PLH}$ can not be corrected by increasing the size of pMOS transistors and another solution is needed to improve the total propagation delay.

IV. PROPOSED SPEED-ENHANCED CIRCUIT: DCVSL-R

DCVSL circuits have a larger $\tau_{\rm PLH}$ than $\tau_{\rm PHL}$ and based on the discussion from Section III, we conclude that increasing the pMOS transistor sizing does not necessarily help this problem. The inherent delay problem of DCVSL structures is addressed in [9], [10] without going into a detailed analysis. The authors of [9] propose two types of enhanced precharge DCVSL (ED-CVSL) structures that operate at 100 MHz. The first structure prevents the crowbar current flow that was mentioned earlier. The second structure is proposed as a solution to prevent the asymmetry between the falling and rising outputs of the circuit. To solve the delay asymmetry problem, the authors of [10] add a pMOS pull-up network to the DCVSL scheme. However, all of the proposed circuits require several additional transistors, eliminating the benefit of low transistor count of DCVSL circuits and increasing internal parasitics, which are a primary concern in RF applications.

Fig. 9 shows our proposed solution, DCVSL with resistive enhancement (which we call DCVSL-R), to solve the inherent extra delay component of $\tau_{\rm PLH}$ in DCVSL circuits. The resistors increase the gate overdrive of the pMOS load transistors. If we consider the switching conditions of Fig. 5, when MN2 turns on and starts conducting current, the gate voltage of MP1 is

$$V_{G\_\rm MP1}(t) = V_{\rm QP}(t) - I_{D\_\rm MN2}(t) \times R. \tag{11}$$

Note that in the delay derivations for DCVSL circuits, we assumed that the transistors operate in saturation region until the output reaches VDD/2. However, in the DCVSL-R circuit, the drain node of the nMOS transistors (also the gate of the pMOS transistors) drop quickly as shown in (11), and push the transistors into linear region. Therefore, the delay analysis of DCVSL-R involves more complex expressions than the closed-form ones derived for DCVSL.

However, based on Section III, an intuitive analysis can explain how the DCVSL-R circuit improves the propagation delay

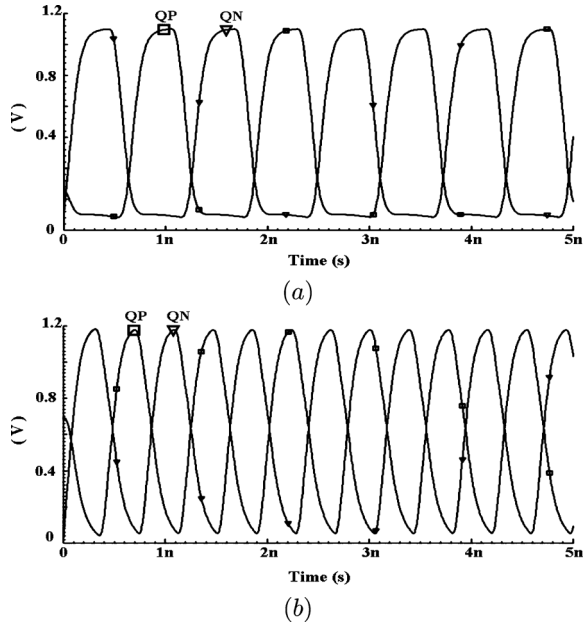


Fig. 10. Inverter output waveforms in a ring oscillator setting (a) for conventional DCVSL (b) for proposed DCVSL-R.

of DCVSL circuits. The extra delay element t_1 of (6) in $\tau_{\rm PLH}$ is due to MP1 waiting for QP to drop. By adding the resistors, we put an additional load to the drain of the nMOS transistors and increase the voltage drop at the gates of pMOS to turn on the pMOS transistors faster and minimize this waiting time. Therefore, based on the value of the resistor, we can achieve $\tau_{\rm PLH} = \tau_{\rm PHL}$ which results in symmetrical output waveforms. More importantly, due to the reduced $\tau_{\rm PLH}$, the total delay of the DCVSL inverter will be reduced.

To demonstrate, we simulate DCVSL and DCVSL-R cells in a ring oscillator setting and plot the outputs for both, in Fig. 10. For ease of comparison, transistor sizes of both cells are the same and only resistors are added to the DCVSL-R cell. The waveforms of Fig. 10 show how rising output lags falling output in DCVSL case and that this problem is eliminated in the DCVSL-R case.

Note that by adding additional resistance to the drain of nMOS transistors, $\tau_{\rm PHL}$ is degraded due to a larger time constant. [14] provides an analysis on the effects of drain resistance in the delay degradation. However, as long as we satisfy

$$R_{MN} > R \tag{12}$$

where R_{MN} is the resistance of the nMOS transistor in linear region and R is the added extra resistor, the degradation of $\tau_{\rm PHL}$ due to R will be insignificant when compared to the improvement we obtain in $\tau_{\rm PLH}$.

Fig. 11(a) shows circuit-level simulation results of the values of $\tau_{\rm PLH}, \tau_{\rm PHL}$ and $\tau_{\rm TOTAL}$ with respect to the value of R, for DCVSL-R inverters where

$$\tau_{\rm TOTAL} = \tau_{\rm PLH} + \tau_{\rm PHL}. \tag{13}$$

The values of these delays when $R = 0$ represent the delay performance of DCVSL inverter. Note that in Fig. 11(a), as R increases (and is kept at a reasonable value based on (12), the improvement in $\tau_{\rm PLH}$ is much more significant than the degradation of $\tau_{\rm PHL}$, and the total effective propagation delay improves considerably. The key observation is that the total propagation delay of the DCVSL-R circuit, (which determines frequency of operation when used in an oscillator) is significantly reduced (46% reduction for $R = 800$ ohms that achieves symmetric $\tau_{\rm PLH}$ and $\tau_{\rm PHL}$), compared to the DCVSL circuit. Note that if R is increased further, the degradation in $\tau_{\rm PHL}$ will start becoming more visible and the improvement in $\tau_{\rm TOTAL}$ will slow down. The delay asymmetry will occur again, resulting in $\tau_{\rm PHL}$ to be larger than $\tau_{\rm PLH}$. Fig. 11(b) demonstrates this delay behavior when R is increased further than the recommended range and point of symmetry.

Similar to CML circuits, speed performance of the DCVSL-R circuit might be affected by resistor value variations. While in ring oscillator based VCOs, frequency tuning controls can take care of such variations, in frequency dividers enough margin should be kept in the maximum operating frequency, based on process variation expectations of the design technology. Relative mismatch between the resistors in the differential branches of the circuit can however, be effectively minimized by symmetric layout techniques and the use of dummy resistors. Note that the DCVSL-R circuit does not speed up by limiting the output signal swing. Rather, the speedup is achieved by eliminating an inherent additional delay of DCVSL circuits. Therefore, it maintains the rail-to-rail switching, making it very suitable for low voltage applications.

V. RF Voltage Controlled Oscillators Based on DCVSL and DCVSL-R Cells

A. Implementation

DCVSL inverter based delay cells, also called Lee-Kim delay cells [18] are often employed in ring oscillators. These cells provide a simple solution with easy frequency tuning, but are susceptible to supply variation as opposed to the more complex Maneatis delay cells [19] that offer better power supply rejection. However, the ring oscillator supply-noise-based PLL jitter can be minimized through supply noise cancellation schemes as in [20] and by employing on-chip voltage regulators. Other important performance metrics of ring oscillators include phase noise, power consumption and frequency of operation.

Frequency of operation is determined by the total delay of the unit cells of the oscillator and is closely related to power consumption. To optimize this speed and power trade off, we propose the DCVSL-R circuits to replace the conventional DCVSL delay cells of ring oscillators. As discussed in Section IV, DCVSL-R circuits provide less delay by improving the inherently slow $\tau_{\rm PLH}$ of their DCVSL counterpart.

To compare the two techniques, we implemented two ring-oscillator-based VCOs in 0.13 μm CMOS process. Both are three-stage ring oscillators, as shown in Fig. 12. While OSC1 uses the standard DCVSL inverter based delay cell of Fig. 13(a), OSC1-R uses the proposed DCVSL-R based delay cell shown in Fig. 13(b). To see the direct effect of the resistors in the speed, power and noise performance of the ring oscillators, we kept the transistor sizing of both oscillators the same and only added resistors to OSC1-R. We used high-resistivity poly re-

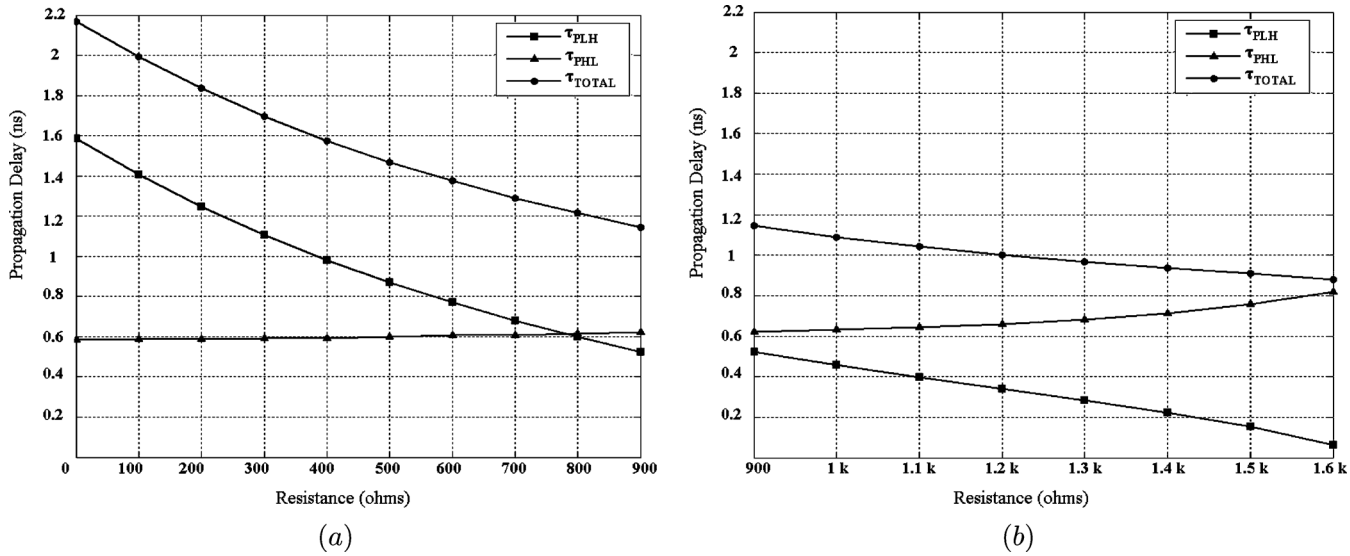


Fig. 11. Circuit-level simulation results for $\tau_{\rm PLH}$, $\tau_{\rm PHL}$ and $\tau_{\rm TOTAL}$ values versus the resistance R for a DCVSL-R inverter with $({\rm WP}/{\rm WN}) = 1.66$ in 0.18 μm technology (a) for recommended range of R where improvement in $\tau_{\rm TOTAL}$ is significant and symmetry is achieved (b) for values of R where asymmetry occurs and improvement in $\tau_{\rm TOTAL}$ slows down.

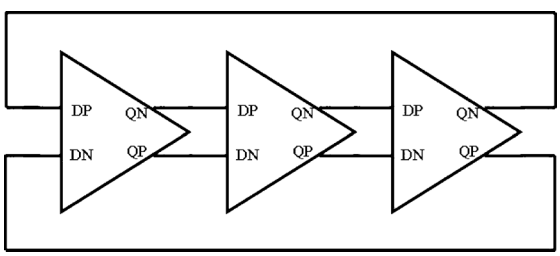


Fig. 12. Block diagram of three stage ring oscillators.

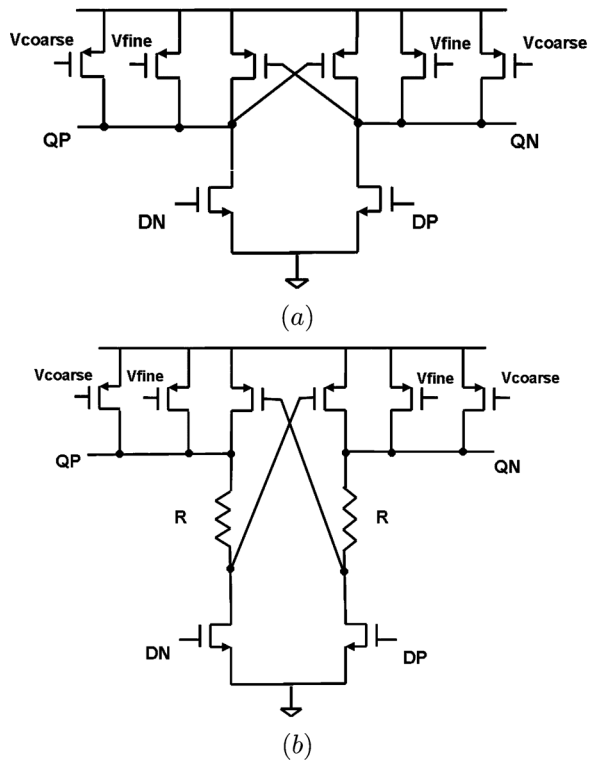


Fig. 13. VCO delay cells (a) conventional DCVSL for OSC1 (b) proposed DCVSL-R for OSC1-R.

sistors that implement 420 ohms with 1.5 μm $\times$ 5.9 μm area in layout. OSC1 is designed to target 2.4 GHz operation, with coarse (VCOARSE) and fine tuning (VFINE) controls. Since the transistor sizes are the same, when operated at the same supply voltage, OSC1-R should give a higher operating frequency due to improved delay performance. In terms of phase noise, since R is a cascode element on top of the input transistors, we expect the noise contribution of R to the phase noise to be negligible.

B. Measurement Results

The two oscillators are fabricated in UMC 0.13 μm CMOS technology. The dies are packaged in a surface mount QFN type package and mounted on an FR-4 printed-circuit-board (PCB) for measurements. Oscillator outputs are connected to on-chip open drain buffers to drive an on-board RF balun that converts the differential outputs to a single node and drives the 50 ohms impedance of the spectrum analyzer.

Table II lists the measured performance of both oscillators. Power consumption and areas are listed for core oscillators only, since open drain buffers are added for testing purposes. Note that the difference in the areas of the two oscillators show the area added by the resistors (including dummy resistors for matching). The frequency range is the tuning range of the oscillators, obtained through coarse and fine tuning controls. When a supply voltage of 1.2 V is applied to both oscillators, OSC1-R oscillates at a 40% higher frequency range than OSC1. For a fair comparison of speed with power consumption and phase noise in mind, we set the power consumption of both oscillators to 2.8 mW and observe that OSC1 oscillates at 2.4 GHz with -113 dBc/Hz phase noise at 10 MHz offset while OSC1-R oscillates at 3.12 GHz, delivering -112.8 dBc/Hz phase noise at 10 MHz offset. Therefore, for the same power and noise performance, the DCVSL-R based oscillator is 30% faster than the DCVSL based one.

TABLE II
MEASURED PERFORMANCE SUMMARY OF OSC1 (BASED ON FIG. 13(A)) AND OSC1-R (BASED ON FIG. 13(B))

Oscillator Topology	Frequency Range	Power Consumption (2.4GHz operation)	Phase Noise (2.4GHz operation)	Area (mm^2)
OSC1	2.16GHz - 2.77GHz (VDD = 1.2V)	2.8 mW	-113dBc/Hz at 10MHz offset	54.2μm x 21μm
OSC1-R	3.14GHz - 3.89GHz (VDD = 1.2V) 2.34GHz - 3.11GHz (VDD = 1.05V)	2 mW	-113dBc/Hz at 10MHz offset	70.4μm x 21.3μm

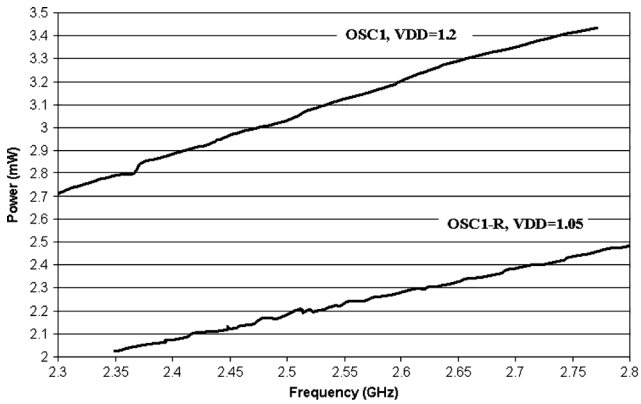


Fig. 14. Ring VCO measured Power versus Frequency curves for OSC1 and OSC1-R.

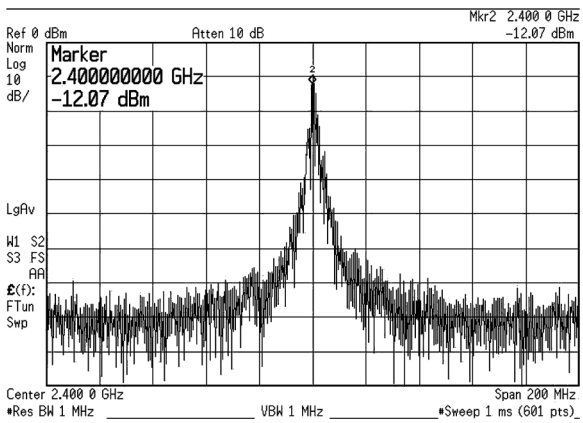


Fig. 15. Measured output frequency spectrum of OSC1-R at 2.4 GHz operation.

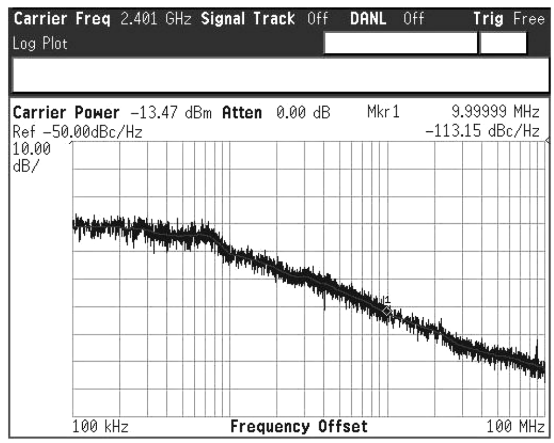


Fig. 16. Measured phase noise spectrum of OSC1-R at 2.4 GHz operation.

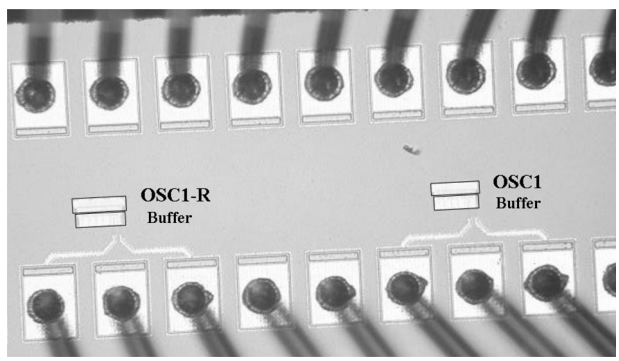


Fig. 17. Die micrograph of OSC1 and OSC1-R.

Table II shows that OSC1-R oscillates at a higher frequency range than OSC1 when same supply voltage is applied. Then, to compare both oscillators at the same target frequency, we reduce the supply voltage of OSC1-R to 1.05 V to pull it to a lower frequency range. Fig. 14 shows the power consumption versus frequency of operation curves for both oscillators with this new power supply setting. For the same power consumption, OSC1-R operates considerably faster than OSC1. At an operation frequency of 2.4 GHz (where OSC1-R has 1.05 V and OSC1 has 1.2 V supply), both oscillators demonstrate -113 dBc/Hz phase noise at 10 MHz offset with OSC1 consuming 2.8 mW and OSC1-R consuming 2 mW of power. The power consumption of OSC1-R is 30% less for the same phase noise and frequency of operation. Fig. 15 shows the output spectrum of OSC1-R at 2.4 GHz while Fig. 16 shows the phase noise spectrum of OSC1-R at the same frequency. Fig. 17 shows the die micrograph for both oscillators. A Figure Of Merit (FOM) for oscillators [21] is shown in (14) where f_0 is the oscillation frequency and PN is the phase noise in dBc/Hz at an offset frequency of Δf. FOM is a useful performance metric that takes the power, speed and noise performances of the oscillator into account. It is demonstrated in [22] that for ring oscillators, the theoretical minimum achievable FOM is -165.2 dBc/Hz ($7.33\times$ kT, where k is Boltzmann constant and T is temperature).

$$\text{FOM (dBc/Hz)} = PN + 10\log\left(P(\text{mW}) \times \frac{\Delta f^2}{f_0^2}\right) \quad (14)$$

Table III provides a comparison of the proposed OSC1-R with state of the art ring-oscillator-based VCOs operating at similar frequencies. It is seen that this work demonstrates a competitive FOM of -157.6 dBc/Hz when compared to the state of

TABLE III
PERFORMANCE COMPARISON OF OSC1-R WITH PREVIOUSLY REPORTED SOLUTIONS

	[24]	[25]	[23]	[26]	[27]	**This Work (OSC1-R)**
Architecture	2 stage ring	3 stage ring	RC - BPF	2 stage ring	2 stage ring	3 stage ring
Technology	0.35μm	0.35μm	0.13μm	0.18μm	0.28μm	0.13μm
Frequency	2.5 GHz	2.4 GHz	2.5 GHz	2 GHz	2.45 GHz	2.4 GHz
Power	10 mW	15 mW	2.86 mW	0.7 mW	19.2 mW	2 mW
Phase Noise (dBc/Hz)	-80 at 5MHz	-97 at 1MHz	-95.4 at 1MHz	-90 at 1MHz	-96 at 1MHz	-93 at 1MHz
FOM (dBc/Hz)	-124	-153	-159	-157	-151	-157.6

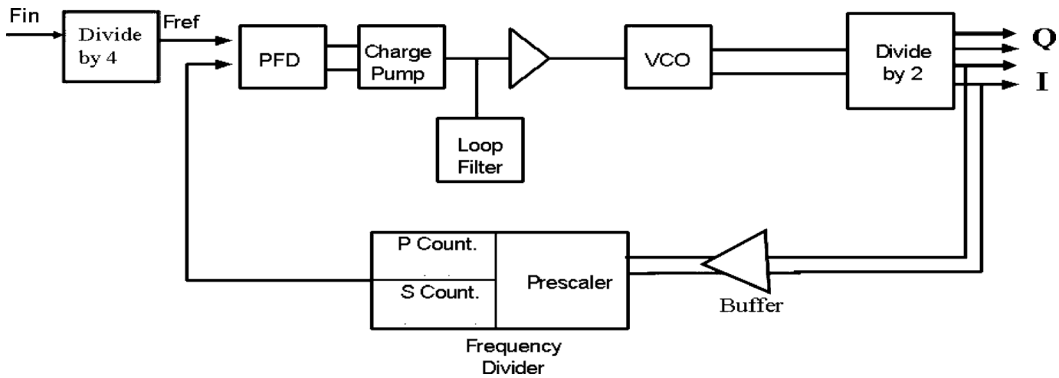


Fig. 18. PLL building block diagram.

the art oscillators. Note that FOM does not take area into consideration. While [23] reports an FOM of -159 dBc/Hz, the oscillator area is 0.006 mm^2, four times that of the proposed OSC1-R oscillator. Therefore, this work demonstrates a good FOM and a low cost solution that consumes only 0.0015 mm^2 of area.

VI. A LOW POWER FREQUENCY SYNTHESIZER WITH DCVSL-R FREQUENCY DIVIDERS

IEEE 802.15.4/ZigBee [28] is a wireless personal area network (WPAN) standard that targets remote control and sensor applications. ZigBee defines a flexible networking system to accommodate up to tens of thousands of nodes in a single network. Such large number of sensors is feasible only through a very low cost wireless solution for each node, and requires long battery lives measured in years. ZigBee has low data rate (up to 250 kbps depending on the frequency band) and short range specifications (1–100 m) that enable the extreme low cost and long battery life. With this motivation, the design of a ZigBee transceiver, both at system and individual block level, must minimize power consumption.

We implemented an integer-N phase-locked loop (PLL) based frequency synthesizer for ZigBee wireless transceiver applications at the 2.4 GHz operating-frequency band. In this section, we focus on the proposed speed-enhanced DCVSL-R circuits in the high-frequency programmable divider of the PLL, optimizing the power consumption. We show that the DCVSL-R based dual-modulus prescaler (DMP) and the buffer that drives it, have the lowest combined power consumption among the reported similar divider implementations at the same operating frequency. To the authors' knowledge, this work is the first to demonstrate DCVSL circuits in gigahertz range frequency dividers.

A. Synthesizer Implementation

The frequency synthesizer is implemented in TSMC 0.18 μm CMOS technology and is based on a previously reported ZigBee synthesizer [6] that employs an *LC* tank VCO and a TSPC prescaler in its programmable dividers. In [6], the TSPC dual-modulus prescaler consumes 2.6 mW in 0.18 μm technology. However, the large capacitance of conventional TSPC circuits' input-clock path results in an additional 2.6 mW of buffer power. To solve this problem and improve the total power consumption, the proposed PLL employs a DCVSL-R based dual-modulus prescaler.

Fig. 18 shows the PLL block diagram. The center frequencies of 16 ZigBee channels in the targeted band are in the range from 2.405 GHz to 2.48 GHz and are spaced by 5 MHz, which is the reference frequency of this PLL. The divide-by-4 circuit before the PFD is employed to minimize the effect of coupling from external reference signal to the sensitive nodes of the PLL and to reduce resulting spurs. The strong external reference signal is at 20 MHz, and the desired reference frequency is generated by the internal divide-by-4 circuit. Therefore, any coupling from the strong input clock to the PLL control node will be pushed to appear at 20 MHz offset, where spur suppression will be better than it would be at 5 MHz offset.

The PFD and charge pump (CP) both use thick-oxide transistors and have a 3 V supply instead of the nominal 1.8 V to allow for cascode transistors in the charge pump and to improve matching. This configuration also increases the dynamic range of the control voltage and allows for a low VCO gain to achieve the desired frequency range. The loop filter (LF) is a fully integrated solution that features an active capacitance multiplier [6]. The LC-tank VCO operates at twice the channel frequency range (4.81 GHz–4.96 GHz). A divide-by-2 circuit generates

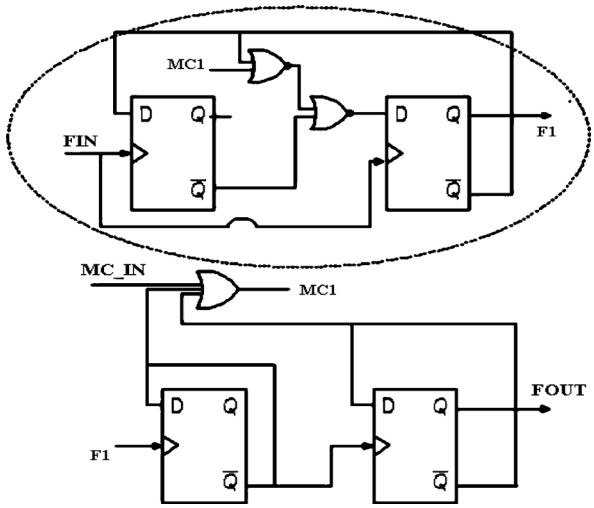


Fig. 19. Dual modulus (15/16) prescaler block diagram.

quadrature LO signals to be used by up/down conversion mixers of a transceiver. This divide by 2 circuit is implemented with CML for quadrature signal generation with very small IQ mismatch and with smaller controlled swing at the LO to improve mixer linearity.

The pulse-swallow divider consists of a 5-bit programmable (P) counter, 4-bit channel selections (S counter), and a 15/16 dual-modulus prescaler. The overall programmable division ratio of the pulse-swallow divider is given by N

$$N = 481, 482, \ldots, 495, 496. \tag{15}$$

Fig. 19 displays the block diagram of the 15/16 prescaler where FIN is the input clock signal to be divided in frequency, $FOUT$ is the output clock signal and MC_IN is the input modulus control that is generated by the P and S counters. The prescaler divides FIN by 15 when MC_IN is low and by 16 otherwise. The prescaler consists of a divide-by$-3/4$ core marked with a circle in the figure, as well as asynchronous divide-by-2 stages. Note that the physical connections between the divide-by-3/4 stage and the following /2 stages in the prescaler are not drawn for simplicity but are marked with signal names such that the output of 3/4 stage, $F1$, is the clock input of the third flip-flop stage and the output of the OR stage, $MC1$, acts as the modulus control of the 3/4 stage.

The prescaler speed limitation arises during /15 operation, which employs the divide-by-3 mode of the /3 or /4 circuit. The critical delay path in the /3 circuit and the timing condition that the circuit should satisfy is given by:

$$\mathrm{TD}_{\mathrm{DFF2\_Slave}} + 2 \times \mathrm{TD}_{\mathrm{NOR2}} \leq \frac{T_{\mathrm{CLK}}}{2} \tag{16}$$

where $\mathrm{TD}_{\mathrm{DFF2\_Slave}}$ is the delay of the slave latch of the second flip-flop, $\mathrm{TD}_{\mathrm{NOR2}}$ is the delay of the two input NOR gate and $\mathrm{TD}_{\mathrm{CLK}}$ is the input clock period. The delay values TD include not only the propagation delay of those circuits but also the corresponding setup and hold times. Note that FIN is the highest frequency in the divider and therefore half of it's period sets a very strict time limitation on the divide-by-3 circuit. The flip-flops and gates shown in Fig. 19 are implemented with

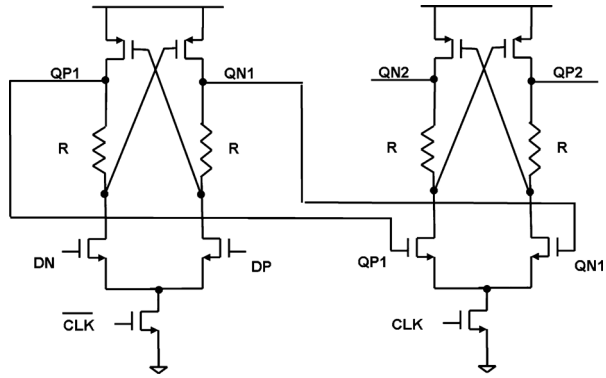


Fig. 20. Circuit level diagram of D flip-flops used in the DCVSL-R based prescaler.

TABLE IV
MEASURED PERFORMANCE SUMMARY OF THE FREQUENCY SYNTHESIZER

Frequency Synthesis	2.405GHz - 2.48GHz
VCO Frequency	4.4GHz - 5.22GHz
Technology	0.18μm CMOS
Spur Suppression	-48 dBc at 5MHz offset -55 dBc at 10MHz offset
Phase Noise	-135 dBc/Hz at 10MHz offset -127 dBc/Hz at 3.5MHz offset
Settling Time	58μs
Power Consumption	8.3mW
Area	0.56 mm^2

DCVSL-R structure. Fig. 20 shows the D flip-flop implementation based on DCVSL-R and use high-resistivity poly resistors. The whole 15/16 prescaler takes 71 μm $\times$ 24 μm area. Since the operating frequency falls down to a few hundred MHz frequency range at the output of the prescaler, the P and S counters are implemented with standard complementary CMOS logic.

B. Synthesizer Measurement Results

The frequency synthesizer is fabricated in TSMC 0.18 μm CMOS, mounted on an FR-4 PCB, and measured. An on-chip open-drain buffer measures the PLL output. Table IV summarizes the PLL measurement results. The PLL output frequency spectrum is shown for the first channel, 2.405 GHz operation, in Fig. 21(a). Spur suppression at 10 MHz offset frequency is -55 dBc/Hz, to meet the alternate channel rejection specification of ZigBee [6]. Fig. 21(b) illustrates the phase noise performance of the closed loop PLL for the same channel. Phase noise is -135 dBc/Hz at 10 MHz offset frequency at 2.405 GHz operation, and settling time is 58 μs. The synthesizer consumes 8.3 mW total power. Note that operating the VCO at double the channel frequency increases the power consumption of the PLL. This is due to the generation of quadrature LO signals for ZigBee which employs OQPSK modulation. Fig. 22 displays the die micrograph, where the PLL occupies an area of 0.8 mm by 0.7 mm.

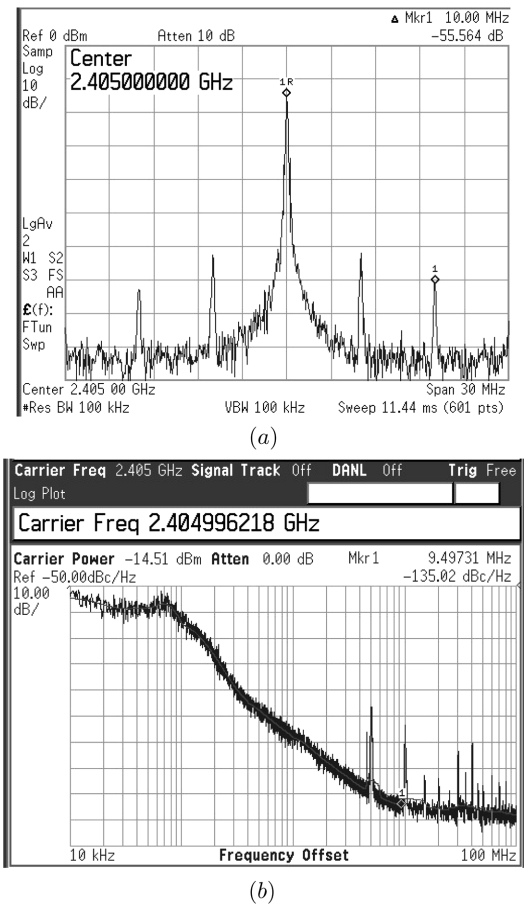
C. Discussion on Divider Performance

Power consumption of frequency dividers are determined by their division ratio, input frequency and the technology they are implemented in. While there are figures of merit [29], [30] that are proposed in literature that relate these parameters to have a

TABLE V
PERFORMANCE COMPARISON OF THE DCVSL-R PRESCALER WITH PREVIOUSLY REPORTED SOLUTIONS

	[5]	[6]	[7]	[8]	**This Work**
Input Frequency	2.5 GHz	2.48GHz	2.5GHz	2.45GHz	2.48 GHz
Division Ratio	22 / 23	15 / 16	8 / 9	16 / 17	15 / 16
Circuit Implementation	SCL	TSPC	E-TSPC	TSPC with powerdown	DCVSL-R
Technology	0.24μm	0.18 μm	0.25 μm	0.18 μm	0.18 μm
Input Buffer Power	No buffers	2.6mW	1.1mW	Not specified	0.27mW
Prescaler Power	19mW	2.6mW	3.025mW	1.33mW	**0.8mW**
Buffer+Prescaler Total Power	19mW	5.2mW	4.125mW	Not Specified *	**1.07mW**

* The divider power is specified as 1.33mW but it is not specified if this includes the power consumption of the inverter chain buffer.



(a)

(b)

Fig. 21. Frequency synthesizer measurements at first channel 2.405 GHz (a) output frequency spectrum (b) phase noise spectrum.

common base of comparison, it is not trivial to do a fair comparison of various divider techniques when all of these parameters are different. This is because the effect of each parameter in the overall performance is not always linear as often predicted by figures of merit.

For instance, for an m stage divider, the power consumption will be dominated by the first x stages, the value of x depends on the input frequency and technology node. Then, after the first x stages, additional division stages will not increase the overall power consumption significantly. Therefore, an assumption of linear relation between the power consumption and the division ratio will not always give an accurate understanding on the performance of the divider. Another issue to consider is if the

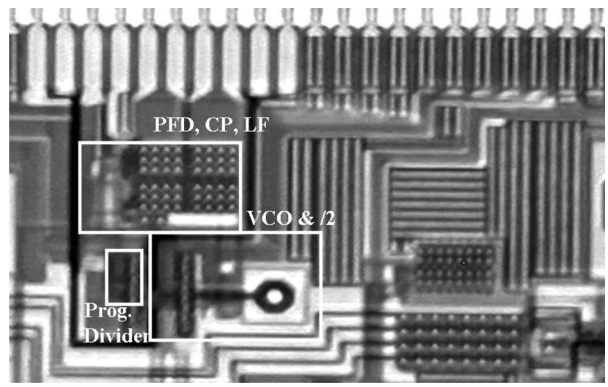


Fig. 22. Die micrograph of the PLL.

divider is a fixed ratio or a multi-modulus divider. Frequency dividers whose divide ratio is a power of 2 could employ n cascaded /2 stages to divide by 2^n. In such a case, the timing constraint on the divider would come from each /2 stage that should operate fast enough at a negative feedback condition, at it's input clock speed. However, in a dual modulus prescaler, the division also involves a feedback that contains the modulus signal and logic gates that enforces certain output states to be skipped. This results in critical timing paths as the one shown in (16). Therefore, for a fair performance comparison, dual modulus prescaler circuits should be compared to other dual modulus prescalers rather than fixed division ratio circuits.

Based on the above discussion, when comparing the performance of various dividers a safe approach is to compare them at similar operating conditions. Table V shows a comparison of prescalers from literature that are used in frequency synthesizers and employ various circuit techniques. Since the power consumption is directly related to the operating frequency, all of these works feature a pulse-swallow divider with a prescaler input frequency of 2.5 GHz, a popular operating frequency for wireless transceiver frequency synthesizers. They are also implemented in similar technology nodes and are using similar division ratios.

The proposed DCVSL-R based dual-modulus prescaler of the PLL consumes 0.8 mW, while the buffer that drives it only consumes 0.27 mW. The power consumption of the prescaler alone is not a sufficient metric, its driving-buffer power should also be taken into account as an indicator of the clock input capacitance of the prescaler and the prescaler's overall impact on the synthesizer power consumption. Note that this work has

the lowest power consumption, 0.8 mW, in its dual-modulus prescaler which demonstrates a 40% reduction from the other works in literature. It also demonstrates the lowest total power consumption for the prescaler and it's driving input buffer. Since DCVSL-R circuits provide a symmetrical differential non-stacked clock input loading to it's driving RF stage, no dummy dividers or differential to single ended converters are employed and the quality of the differential quadrature LO signals are maintained.

VII. Conclusion

DCVSL based delay cells have been analyzed for RF frequency-divider and ring oscillator applications. We have presented a closed-form delay model for DCVSL inverters that demonstrates 8% worst case accuracy for various transistor sizing ratios and for two different technologies (0.13 μm and 0.18 μm CMOS). The inherent speed bottleneck of DCVSL structures that cause $\tau_{\mathrm{PLH}} > \tau_{\mathrm{PHL}}$ have been addressed and a solution (DCVSL-R) that reduces τ_{PLH} and the total propagation delay of the circuit, offered.

Two ring-oscillator-based VCOs employing DCVSL based cells and proposed DCVSL-R cells have been implemented, and measured results have been compared. At the same operating frequency of 2.4 GHz for the same phase noise, the proposed DCVSL-R based oscillator consumes 30% less power than its standard counterpart. When compared to other state-of-the-art ring oscillators, the proposed oscillator performs with a good figure of merit, and small area.

The proposed speed-enhanced DCVSL-R circuits have implemented the RF dual-modulus prescaler of a low-power frequency synthesizer that satisfies ZigBee specifications, in 0.18 μm technology. The proposed dual-modulus prescaler of this synthesizer consumes the lowest power (0.8 mW), 40% less, among similar dividers that employ different circuit techniques such as CML and TSPC in literature. The RF buffer that drives the DMP consumes only 0.27 mW due to the low clock input capacitance of the DCVSL-R circuit. In short, the proposed circuit proves to be a good candidate to replace existing RF frequency-divider circuits. The proposed cell reduces the power consumption of the infamously power-hungry frequency dividers of frequency synthesizers while providing a low-cost, differential, low-input-capacitance and high-speed solution. To the authors' knowledge, this work is the first to demonstrate the use of DCVSL logic style in RF frequency dividers of frequency synthesizers.

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Didem Z. Turker was born in Antalya, Turkey. She received the B.S. degree in microelectronics engineering from Sabanci University, Istanbul, Turkey in 2003. Since August 2003, she has been working towards her Ph.D. at the Analog and Mixed Signal Design Center at the Department of Electrical and Computer Engineering, Texas A&M University, College Station, TX.

In summers of 2005 and 2006, she worked as a co-op Researcher in the Analog and Mixed Signal Communications IC Design group of IBM T.J. Watson Research Center in York Town Heights, NY, where she worked on equalization in high speed serial links and all digital PLLs for clocking applications. During her doctoral program she has worked on RFID systems, frequency synthesizers, high speed digital circuit techniques, frequency dividers, ring oscillators and all digital PLLs. Her research interests are analog and mixed signal circuit design and RF and high speed communication circuits.

Sunil P. Khatri received the B.Tech. degree in electrical engineering from the Indian Institute of Technology Kanpur, Kanpur, India, the M.S. degree in electrical and computer engineering from the University of Texas, Austin, and the Ph.D. degree in electrical engineering and computer science from the University of California, Berkeley.

He was with Motorola, Inc., for four years, where he was a member of the design teams of the MC88110 and PowerPC 603 RISC microprocessors. He is currently an Associate Professor with the Department of Electrical Computer Engineering, Texas A&M University, College Station. His research interests include logic synthesis, novel VLSI design approaches to address issues such as power, cross-talk, hardware acceleration of CAD algorithms, and cross-disciplinary applications of these topics. He has coauthored about 160 technical publications, 6 U.S. Patents, 5 research monographs, and 3 book chapters.

Dr. Khatri was a recipient of four Best Paper Awards and three separate Best Paper Nominations. He serves as an Associate Editor for the IEEE TRANSACTIONS ON COMPUTERS, and also has served or serves on the Program Committees of several conferences.

Edgar Sánchez-Sinencio (F'92–LF'09) was born in Mexico City, Mexico. He received the degree in communications and electronic engineering (Professional degree) from the National Polytechnic Institute of Mexico, Mexico City, the M.S.E.E. degree from Stanford University, Stanford, CA, and the Ph.D. degree from the University of Illinois at Champaign-Urbana, in 1966, 1970, and 1973, respectively.

His research work has more than 2725 citations according to the Thomson Reuters Scientific Citation Index. He has graduated 44 M.Sc. and 35 Ph.D. students. He is a coauthor of six books on different topics, such as RF circuits, low-voltage low-power analog circuits, and neural networks. He is currently the TI J. Kilby Chair Professor and Director of the Analog and Mixed-Signal Center at Texas A&M University. His current interests are in the area of power management, analog and medical electronics circuit design.

Dr. Sánchez-Sinencio is a former Editor-in-Chief of IEEE TRANSACTIONS ON CIRCUITS AND SYSTEM II: EXPRESS BRIEFS. In November 1995 he was awarded a Honoris Causa Doctorate by the National Institute for Astrophysics, Optics and Electronics, Mexico. This degree was the first honorary degree awarded for microelectronic circuit-design contributions. He is a co-recipient of the 1995 Guillemin–Cauer Award for his work on cellular networks. He was also the co-recipient of the 1997 Darlington Award for his work on high-frequency filters. He received the IEEE Circuits and Systems Society Golden Jubilee Medal in 1999. He also received the prestigious IEEE Circuits and Systems Society 2008 Technical Achievement Award. He was the IEEE Circuits and Systems Society's Representative to the IEEE Solid-State Circuits Society during 2000–2002. He was a member of the IEEE Solid-State Circuits Society Fellow Award Committee from 2002 to 2004. He has been Associate Editor of the *IEEE Circuits and System Magazine*, IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS, and the IEEE TRANSACTIONS ON NEURAL NETWORKS. He is a former IEEE CAS Vice President-Publications.