An 82–107.6-GHz Integer-N ADPLL Employing a DCO With Split Transformer and Dual-Path Switched-Capacitor Ladder and a Clock-Skew-Sampling Delta–Sigma TDC

Zhiqiang Huang and Howard C. Luong, *Fellow, IEEE*

***Abstract*— A W-band integer-N all-digital phase-locked loop (ADPLL) aiming for wide frequency tuning range (TR) and low phase noise is proposed. The W-band ADPLL employs a digitally controlled oscillator (DCO) with split transformer and dual-path exponentially scaled switched-capacitor ladder and a clock-skew-sampling delta–sigma time-to-digital converter (TDC). The 65-nm CMOS W-band ADPLL measures a frequency TR of 27% from 82 to 107.6 GHz and phase noise from −106 to −110 dBc/Hz at 10-MHz offset and −84 to −87 dBc/Hz at 100-kHz offset while consuming 35.5 mW and occupying a 0.36 mm^2 core area, corresponding to a figure of merit (FOM) of −171 ∼ −173 dB and FOM$_T$ of −178 ∼ −181 dB.**

***Index Terms*— All-digital phase-locked loop (ADPLL), digitally controlled oscillator (DCO), magnetic tuning, millimeter wave (mmW), switched-capacitor (SC) ladder, time-to-digital converter (TDC), W-band.**

I. Introduction

DUE to low atmospheric attenuation (<1 dB/km), which enables longer transmission distance [1], the W-band frequency spectrum from 75 to 110 GHz has attracted extensive research attention and applications [2]–[7]. With its short wavelength (∼3 mm) and compact antenna size, a W-band imaging radar can yield high image resolution [2]–[5] and offer a fully integrated solution [2], [3]. Finally, thanks to the ultra-wide frequency spectrum available, it can also support high-data-rate wireless communication up to 56 Gb/s [6], [7].

On the other hand, as a critical sub-system in imaging and wireless communication systems, frequency synthesizers have critical effects on the overall system performance, such as chip area, signal-to-noise ratio, and frequency operation range [2], [7]. Currently, the millimeter-wave (mmW) frequency synthesizers are still dominated by charge-pump-based analog phase-locked loops (PLLs) using external bulky and costly analog loop filters [8]–[12], which are not easily scaled with more advanced technology nodes. An all-digital PLL (ADPLL), in contrast, can fully integrate a digital loop filter (DLF) on-chip and offers extensive programmability and re-congfigurability. However, as of now, only a few proposed ADPLLs can operate at the mmW frequency range, with the maximum operation frequency being limited to 66 GHz [13], [14], and the W-band ADPLL working over 100 GHz has not yet been reported. The main bottleneck of such high-frequency ADPLLs is the limited frequency resolution of digitally controlled oscillators (DCOs) and the high frequency-division ratio, which magnifies the time-to-digital converter (TDC)'s quantization noise contribution to the ADPLL's output phase noise. Moreover, because of much smaller tank capacitor at higher operation frequencies, the DCO frequency becomes more sensitive to capacitor variation, which makes it difficult to achieve sub-100-kHz resolution at the W-band frequencies.

Apart from the quantization noise issue affecting ADPLLs' phase noise performance, wide frequency tuning range (TR) is also needed for multi-band high-data-rate wireless communication [7]. The frequency coarse-tuning realized by varactors or switched-capacitor arrays (SCAs) with extremely low quality factor Q (∼3 at 100 GHz) introduces a stringent tradeoff between the frequency TR and phase noise. This is the main reason why the existing W-band PLLs can only achieve frequency TR limited to ∼12 GHz at 100 GHz (∼11.4%) [12], which cannot fully utilize the frequency resources from 75 to 110 GHz.

In order to overcome these limitations, this paper proposes a W-band ADPLL with several techniques, including using a split transformer as a variable inductor to increase the TR without severely degrading the tank Q, a dual-path exponentially scaling SC ladder to enhance the frequency resolution with small bandwidth (BW) variation, and a clock-skew-sampling-based delta–sigma TDC to reduce the close-in phase noise. The first-ever reported ADPLL operating over 100 GHz achieves an in-band phase noise of −87 dBc/Hz and

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The authors are with the Department of Electronic and Computer Engineering, The Hong Kong University of Science and Technology, Hong Kong (e-mail: zhuangah@connect.ust.hk; eeluong@ust.hk).

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out-band phase noise of −110 dBc/Hz at 10-MHz offset, with a wide TR from 82 to 107.6 GHz. Significantly expanded from our conference paper [15], this paper presents more in-depth analysis, more detailed circuit implementation, and more measurement results.

Section II reviews the existing frequency tuning methods at high frequencies. Section III describes the proposed W-band ADPLL architecture. Section IV presents the design of the wide-TR high-resolution and low-phase-noise W-band ADPLL, including DCO and TDC as its key building blocks. The experimental results are discussed in Section V, followed by the conclusion in Section VI.

II. Frequency Tuning Methods

The existing frequency tuning techniques can be classified as capacitance tuning [12], [16]–[20] or magnetic tuning [21]–[23].

A. Capacitance Tuning

Capacitance tuning using varactors or SCAs, which is popular at gigahertz frequencies, is not suitable for the W-band frequencies because their quality factor Q becomes extremely low (∼3 at 100 GHz). As a result, the tradeoff between the start-up condition, phase noise, and the TR becomes more stringent, limiting the available TR. The harmonic extraction with a lower oscillation frequency for higher tank Q [12], [17]–[20], [32], [33] can alleviate the problem to reduce the phase noise, but it suffers from weak amplitude and requires power-hungry wideband amplifiers or wide-locking-range injection-locked oscillators at 100 GHz as buffers. Although the harmonic can be boosted with a high-order tank, the low harmonic-current generation efficiency still limits the output amplitude [33]. Besides, the harmonic extraction requires extra filtering to reject spurs at the fundamental frequency [33].

B. Magnetic Tuning

Unlike the capacitance tuning method, magnetic tuning has a better quality factor (∼10) for the same TR when oscillating over 100 GHz. However, coarse magnetic tuning using a switched transformer with multiple secondary coils [14], [21] may create a large frequency tuning step, which still requires a large capacitor with low Q to cover the tuning step.

The variable inductor using a transformer with a continuously tuned variable resistor [22], [23] can provide continuous frequency tuning to avoid a frequency tuning gap, as shown in Fig. 1(a), from which the input impedance of the primary coil is given by

$$Z_{\text{in}} = \frac{j\omega M[j\omega(L_2-M)+R]}{j\omega M+[j\omega(L_2-M)+R]} + j\omega(L_1-M) = j\omega L_1 - \frac{(\omega M)^2}{(\omega L_2)^2+R^2} j\omega L_2 + \frac{(\omega M)^2 R}{(\omega L_2)^2+R^2}. \quad (1)$$

It follows that the tank inductance L_{eq} and the corresponding tank quality factor Q can be derived as

$$L_{\text{eq}} = L_1 - \frac{(\omega M)^2}{(\omega L_2)^2+R^2} L_2 \quad (2)$$

$$Q = \frac{\omega L_{\text{eq}}}{(L_1-L_{\text{eq}})\frac{R}{L_2}} \quad (3)$$

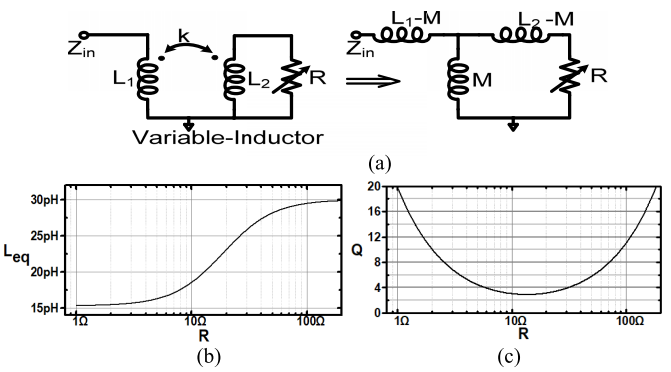


Fig. 1. (a) Magnetic tuning using a transformer and variable resistor and its equivalent circuit. (b) Simulated tank inductance L_{eq}. (c) Simulated tank Q at 100 GHz versus the tuning variable resistor R ($L_1 = L_2 = 30$ pH and $k = 0.7$).

as plotted in Fig. 1(b) and (c), respectively. When the variable resistor R is turned off, $L_{\text{eq}} = L_1$. When it is turned on, $L_{\text{eq}} = L_1-(M^2/L_2)$. As a result, the corresponding TR of inductance becomes

$$\text{TR} = \frac{\Delta L_{\text{eq}}}{L_1} = \frac{L_1-\left(L_1-\frac{M^2}{L_2}\right)}{L_1} = \frac{M^2}{L_1L_2} = k^2 \quad (4)$$

where k is the transformer coupling coefficient.

When the variable resistance R is tuned to match the output impedance of the secondary coil

$$R = \omega(L_2-M) + \frac{\omega M \times \omega(L_1-M)}{\omega L_1} \approx \omega L_2 \quad (5)$$

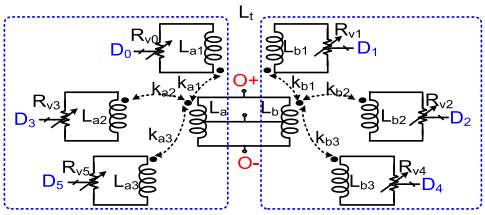
the variable inductor delivers the maximum output power to the variable resistor, resulting in a minimum quality factor Q_{min}, as shown in Fig. 1(b). From (1) and (5), the minimum quality factor Q_{min} can be obtained as

$$Q_{\text{min}} = \frac{\left[\omega L_1 - \frac{(\omega M)^2\omega L_2}{(\omega L_2)^2+R^2}\right]}{\frac{(\omega M)^2 R}{(\omega L_2)^2+R^2}} \approx \frac{\omega L_1 - \frac{(\omega M)^2}{2\omega L_2}}{\frac{(\omega M)^2}{2\omega L_2}} = \frac{2}{k^2} - 1 = \frac{2}{\text{TR}} - 1. \quad (6)$$

In other words, the low-Q region's minimum quality factor highly depends on the coupling k and the TR of the variable inductor. When its coupling factor k is increased to achieve a wider TR, more loss is introduced from the variable resistor to the primary coils and further degrades the tank Q. When the variable resistor is 0 or ∞, the variable inductor is operated in a high-Q region with high quality factor.

C. Proposed Magnetic Tuning With Split Transformer

In order to minimize the Q degradation, a split transformer with multiple secondary coils is proposed as the variable inductor, as shown in Fig. 2. The proposed split transformer consists of two parallel transformers L_{a} and L_{b}, each of which is designed to have three parallel secondary coils with small coupling factor k_{i} to maximize $Q_{\text{min,i}}$. 7–8-bit binary-weighted transistors (R_{v0}–R_{v5}) with each being 60 nm length and less than 3-Ω ON-resistance are added in parallel with each secondary coil as variable resistors for frequency tuning. Theoretically, the minimum quality factor



	Width [um]	Res. [Ω]	Bit
R_{v0}	31	2.9	7
R_{v1}	42.5	2.23	7
R_{v2}	43.5	2.18	7
R_{v3}	49.5	1.92	7
R_{v4}	43.75	2.17	8
R_{v5}	54.75	1.75	8

Fig. 2. Schematic of the proposed split transformer as variable inductor.

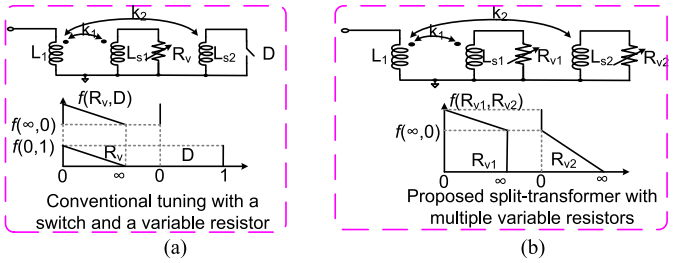


Fig. 3. Comparison of the frequency tuning for (a) conventional tuning with a switch and a variable resistor [23] and (b) proposed split transformer with multiple variable resistors.

contributed by each variable resistor is $Q_{\min} \approx (2N/\mathrm{TR}) - 1$, where N is the total number of secondary coils and each coil is sized uniformly with a TR of (TR/N). Because $\mathrm{TR_i}$ of each secondary coil is k_i^2, the split transformer can achieve an effective overall coupling factor $k_{eq} = (\sum k_i^2)^{1/2}$. In comparison, for the same 50% inductance TR and 30% frequency TR at 100 GHz, the conventional variable inductor [22] requires k of 0.71 with limited $Q_{\min}$ of only 3, while the proposed split transformer only needs k_i of 0.41 with $Q_{\min}$ of 11 for $N = 3$ and k_i of 0.29 with $Q_{\min}$ of 23 for $N = 6$.

As an illustration, Fig. 3 shows the comparison of the frequency tuning between the conventional switched-transformer-based tuning scheme employing a switch D and a variable resistor R_V [23] and the proposed tuning scheme employing two variable resistors R_{V1} and R_{V2} for the split transformer. (For clarity, only the tuning with two secondary coils is illustrated, but the proposed scheme is actually extended to all six secondary coils in this paper.) For the conventional tuning in Fig. 3(a), the control signals (R_V, D) need to be switched from ($R_V = \infty$ and $D = 0$) to ($R_V = 0$ and $D = 1$) for further tuning in another band after the frequency is continuously tuned down from $f(R_V = 0$ and $D = 0)$ to $f(R_V = \infty$ and $D = 0)$. Due to the mismatch, $f(R_V = \infty$ and $D = 0)$ can be higher than $f(R_V = 0$ and $D = 1)$, resulting in a frequency gap. However, the proposed tuning scheme in Fig. 3(b) can use R_{V2} for further tuning in another band without switching the control signals after the frequency is continuously tuned down from $f(R_{V1} = 0$ and $R_{V2} = 0)$ to $f(R_{V1} = \infty$ and $R_{V2} = 0)$, which guarantees no frequency gap between the adjacent tuning bands.

For the proposed split transformer, the secondary coils can be simply designed to be uniform. However, at higher frequencies, more variable resistors need to be turned on for smaller inductance, and the overall Q would inevitably be degraded.

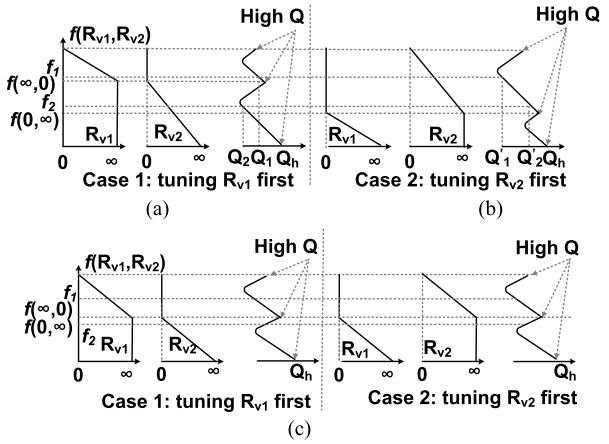


Fig. 4. Proposed split transformer using swapping scheme with (a) non-uniform TR with R_{V1} tuned first, (b) non-uniform TR with R_{V2} tuned first, and (c) uniform TR.

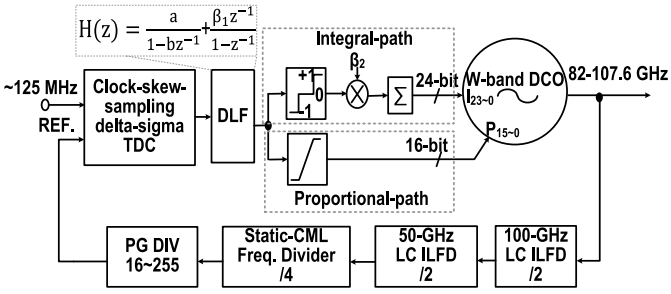


Fig. 5. Block diagram of the proposed W-band integer-N ADPLL.

To tackle the problem, the secondary coils are designed to be non-uniform with progressively scaled k_i and $\mathrm{TR_i}$. As such, the secondary coil with a smaller TR is selected for tuning at a higher frequency, which enables the split transformer to operate in the region with a higher Q. Besides, the non-uniform secondary coils can create more high-Q regions to reduce the quality factor degradation. Assuming that the two secondary coils are designed so that $\mathrm{TR_1} < \mathrm{TR_2}$, there are two possible cases to achieve a target frequency by tuning R_{V1} before R_{V2} or tuning R_{V2} before R_{V1}. As illustrated in Fig. 4(a) and (b), for f_1, tuning R_{V2} first (Case 2) would result in a low-Q region whereas tuning R_{V1} first (Case 1) would operate the tank in a high-Q region. Similarly, for another target frequency f_2, the tank can be operated in a high-Q region by swapping the tuning order from Case 1 to Case 2 with R_{V2} being tuned first. As a comparison, if the split transformer were designed uniformly, there would be no difference in swapping the tuning order, and the split transformer would be operated in a low-Q region for the two frequencies f_1 and f_2 in both the cases, as shown in Fig. 4(c).

III. Block Diagram of Proposed W-Band ADPLL

Fig. 5 shows the block diagram of the proposed W-band integer-N ADPLL with a DCO oscillating directly at W-band frequencies. The W-band DCO consists of a six-port split

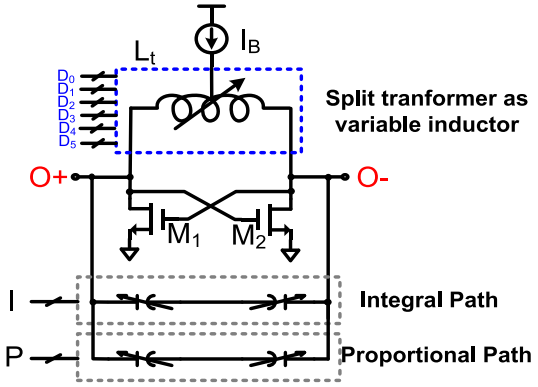


Fig. 6. Schematic of the implemented W-band DCO.

transformer as a variable inductor controlled by digital signals D_0–D_5 to coarsely tune the output frequency from 82 to 107.6 GHz and a dual-path exponentially scaling SC ladder to finely tune the frequency for phase locking and frequency calibration under process, voltage and temperature (PVT) variations. A three-stage frequency pre-scaler, consisting of 100- and 50-GHz LC-based injection-locked divide-by-2 frequency dividers (LC-ILFDs) and a static current-mode logic (CML) divide-by-4 frequency divider, is used to divide down the DCO output frequency to ~6 GHz.

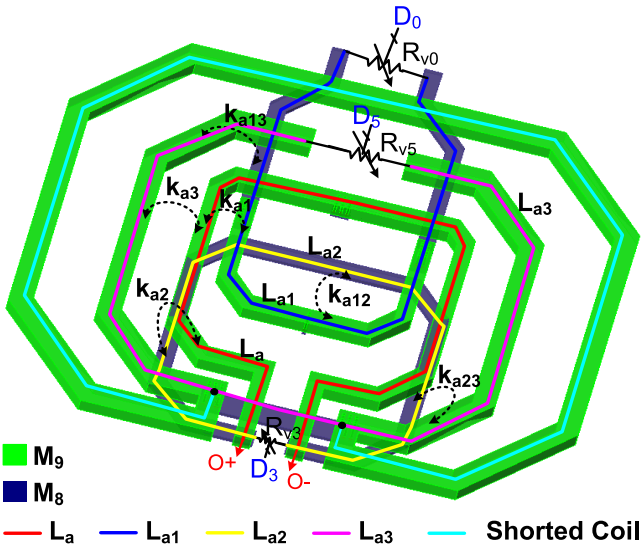
A programmable frequency divider with division ratio from 16 to 255 is employed to further divide down the DCO output to the reference frequency of ~125 MHz. The time difference between the reference input and frequency divider output is digitized by a proposed clock-skew-sampling delta–sigma TDC and then fed to a 2nd-order DLF. The DLF output is split into two paths to control the dual-path exponentially scaling SC ladder to tune the oscillation frequency, resulting in a type-III operation. In the integral path, the DLF output is quantized by a three-level quantizer and then integrated to control a 24-bit integral-path SC ladder. Meanwhile, in the proportional path, the DLF output directly controls a 16-bit proportional-path exponentially scaled SC ladder with a limiter constraining the output range, whose boundary sets the threshold of the three-level quantizer.

IV. Circuit Implementation of Key Building Blocks

A. Implemented W-Band DCO

Fig. 6 shows the schematic of the implemented W-band DCO, which consists of an NMOS cross-coupled pair ($M_{1,2}$) to sustain the oscillation, the proposed split transformer L_t with six port controls, D_0–D_5, for coarse frequency tuning as described above, and a dual-path exponentially scaled SCAs with a proportional path P and an integral path I for fine frequency tuning.

As the variable resistor degrades the quality factor when the transistor is fully turned on, a large transistor size is required to minimize the loss. However, the increase of its parasitic capacitance would lower the self-resonant frequency and boost the amplitude at the secondary coil due to series LC peaking, introducing higher loss. As a result, the variable



L_a, L_b	27.6 pH	Q_a, Q_b	15.1	k_{a12}	0.0625
L_{a1}, L_{b1}	29.7 pH	Q_{a1}, Q_{b1}	14.3	k_{a13}	0.142
L_{a2}, L_{b2}	29.4 pH	Q_{a2}, Q_{b2}	13.2	k_{a23}	0.261
L_{a3}, L_{b3}	31.4 pH	Q_{a3}, Q_{b3}	16.4	k_{b12}	0.0995
k_{a1}	0.208	k_{b1}	0.248	k_{b13}	0.164
k_{a2}	0.377	k_{b2}	0.377	k_{b23}	0.261
k_{a3}	0.308	k_{b3}	0.322		

Fig. 7. Layout of the proposed split transformer L_a and its parameters.

resistors R_{v0}–R_{v5} should be sized optimally to make the self-resonant frequencies higher than the oscillation frequency without introducing too much loss.

Because the mutual coupling between the secondary coils effectively provides a shielding effect and reduces the coupling factor to the primary coil when the secondary coils are turned on [21], the coupling factor between the secondary coils and primary coil should be increased accordingly to keep the same TR. At the same time, to minimize the mutual coupling between secondary coils, the transformer is further split into two parallel transformers L_a and L_b with similar structures. Three or more transformers in parallel would reduce the tank impedance and increase the power consumption. The layout of the transformer L_a together with its design parameters is shown in Fig. 7. As shown in Figs. 2 and 7, the transformer L_a has a primary coil L_a and three secondary coils L_{a1}, L_{a2}, and L_{a3} with variable resistors R_{v0}, R_{v3}, and R_{v5} controlled by D_0, D_3, andD_5, respectively. Each coil is implemented by top metals M_9 and M_8 with only one turn. The inner coils L_{a1} and L_{a2} are, respectively, coupled to the upper and lower parts of the primary coil L_a to minimize the overlap between L_{a1} and L_{a2} and to reduce the mutual coupling factor k_{a12} between L_{a1} and L_{a2} to 0.0625. To avoid a shorted circuit with the other coils, L_{a1} is implemented with M_9 and then M_8 while L_{a2} is placed underneath L_a using only M_8. The outer coil L_{a3} is placed away from L_{a1} and L_{a2}, with mutual coupling factors k_{a13} between L_{a1} and L_{a3} of 0.142 and k_{a23} between L_{a2} and L_{a3} of 0.261. Finally, a shorted coil surrounding L_{a3} is added to reduce the inductance of L_{a3} to 31.4 pH not to degrade the self-resonant frequency.

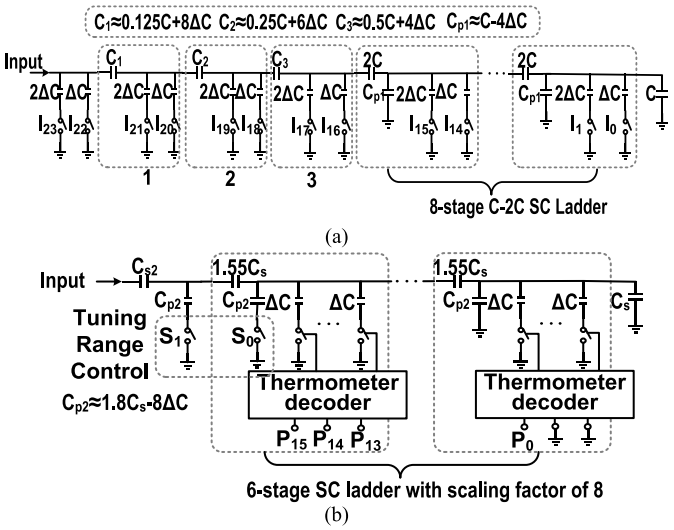


Fig. 8. (a) Half circuit of the integral-path SC ladder. (b) Half circuit of the proportional-path SC ladder.

B. Dual-Path Switched-Capacitor Ladder

As the tuning slope of the variable resistors can decrease to around 0, meaning it has larger gain variation than capacitance tuning, as shown in Fig. 1(b), the split transformer tuning is not suitable for phase locking. Although the capacitance tuning has low Q, it is still can be used for fine tuning without severe Q degradation. To maintain a stable gain for phase locking and to achieve a fine frequency resolution to minimize the quantization noise, the W-band DCO employs an exponentially scaling SC ladder with a multi-stage capacitor ladder to scale down the tuning step of multi-bit SC units in each stage [24], as shown in Fig. 8. However, the scaling factor can vary, especially for a large number of bits, and cause variations in both DCO control gain and loop BW [24]. In order to reduce the BW variation using a smaller number of bits, a dual-path architecture with integral-path and proportional-path controls in the loop filter [25], [26] is adopted. As shown in Fig. 5, the W-band ADPLL behaves as a type-III PLL before being locked, and the integral-path SC ladder is controlled by the three-level quantizer and the integrator to track the frequency error. After locking, the output of the three-level quantizer is 0, and the integrator's output becomes constant, and thus has no effect on the ADPLL loop BW. Because the ADPLL is not used for signal modulation, the nonlinearity of SC ladder is not important.

As shown in Fig. 8(a), the 24-bit integral-path SC ladder with ∼1-GHz TR has 11 stages, each of which provides a scaling factor of ∼4 with quality factor dominated by ladder capacitor C [24]. The first three stages use small series capacitors C_{1-3} to reduce the input capacitance, whereas the other eight stages are implemented using C–$2C$ SC ladder. As shown in Fig. 8(b), the proportional-path SC ladder, with a TR of ∼4 MHz and a simulated frequency resolution of 1.5 kHz, utilizes a six-stage 16-bit SC ladder and is controlled by the DLF output for phase locking. Before locking, the proportional-path control signal is pulled to saturation by the DLF. After locking, the DCO output frequency approaches the correct value and it is not saturated anymore. Then, only the 16-bit proportional path is used for phase locking to reduce gain and BW variation. In order to have better monotonicity, a higher scaling factor of ∼8 and 3-bit thermometer-coded SC units in each stage is used. To avoid time skews among different digital bits, the retimed D flip-flops can be added at the digital outputs.

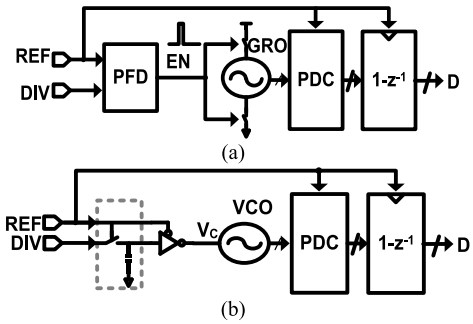


Fig. 9. Block diagrams of (a) conventional delta–sigma TDC [28] and (b) proposed clock-skew-sampling delta–sigma TDC.

C. Proposed Clock-Skew-Sampling Delta–Sigma TDC

Normally, the ADPLL's in-band phase noise is limited by the TDC's noise [27], including quantization noise and active noise. The simplest way to implement a TDC is to use a delay line to compare and quantize the input time difference [27]. However, its time resolution is limited by the inverter delay and constrained by the process technology. To reduce the quantization noise, several techniques, including using a delta–sigma TDC [28], [29], as shown in Fig. 9(a), have been proposed. The conventional delta–sigma TDC [28] consists of a phase–frequency detector (PFD) to generate the input time difference, a gate ring oscillator (GRO) to integrate the time difference into the phase domain, a phase-to-digital converter (PDC) to quantize the output phase, and finally a differentiator $(1 - z^{-1})$ to recover the input time difference in the digital domain. With a noise-shaping effect introduced by the differentiator to suppress the close-in quantization noise, the TDC's time resolution can be greatly improved. However, the active noise of the GRO cannot be suppressed, even with a higher order delta–sigma TDC [29], which dominates the close-in phase noise of the ADPLL.

To suppress the input close-in quantization noise, a clock-skew-sampling delta–sigma TDC is proposed, as shown in Fig. 9(b). By using a clock-skew-sampling phase detector [30] instead of a PFD to provide high-gain phase detection, the input-referred noise of the ring oscillator and PDC can be greatly reduced. The detected phase error is, then, integrated into the phase domain with a ring oscillator and differentiated by the digital circuit to achieve delta–sigma operation. With the reduction of both active and quantization noises, the power consumption of the ring oscillator can also be reduced without using a high-power multi-path GRO [28]. Since the detection gain of clock-skew sampler depends on the slope of DIV and affects the ADPLL's loop BW, an *RC* filter, which has less PVT variation than inverter, can be used at DIV output to reduce the gain variation.

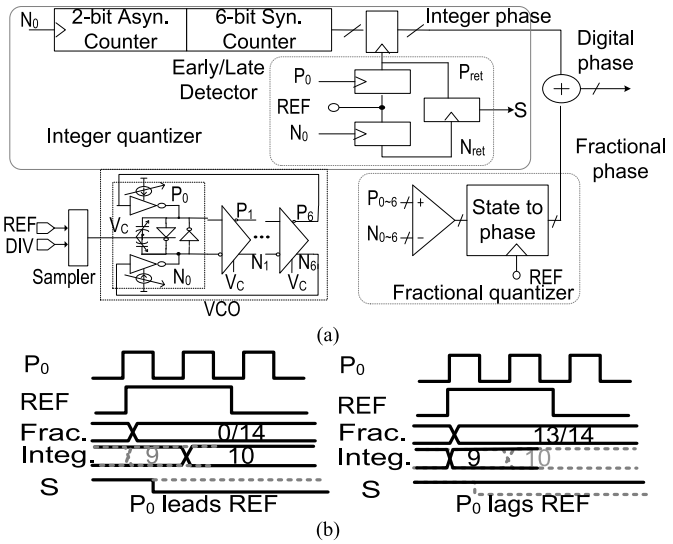


Fig. 10. (a) Block diagram of the proposed PDC and (b) time diagram of proposed TDC with (dashed) and without (solid) time difference mismatch.

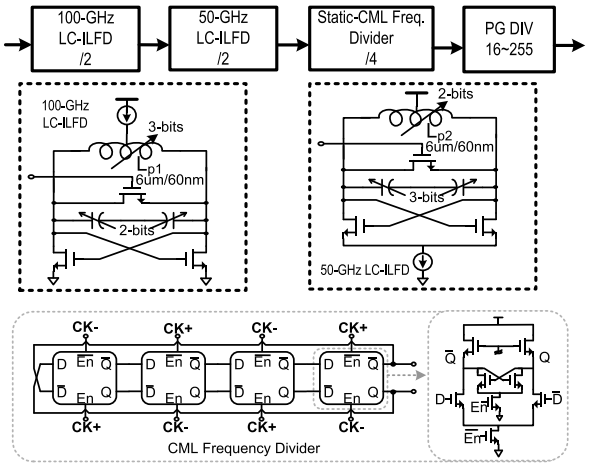


Fig. 11. Block diagram and schematics of the frequency divider chain.

Fig. 10(a) shows the block diagram of the proposed PDC. The output of the voltage-controlled oscillator (VCO), counted by an 8-bit counter, is used to quantize the integer phase. Since an 8-bit synchronous or asynchronous counter is difficult to operate at gigahertz range, a 2-bit asynchronous counter is followed by a 6-bit synchronous counter to lower the synchronous counter's operation frequency and to reduce the delay of the asynchronous counter. The VCO is a seven-stage differential ring oscillator oscillating from 0.83 to 1.4 GHz with 500-MHz/V frequency sensitivity. The seven differential outputs P_{0-6} and N_{0-6} of the VCO are quantized into fractional phases with a resolution of 1/14 using comparators and a state-to-phase decoder. The simulated quantization noise contribution is below -100 dBc/Hz at 100-kHz offset, and TDC's in-band noise is not dominated by quantization noise. Ideally, as shown in Fig. 10(b), the timing difference between the ring-oscillator output P_0 and reference input REF is the same in both the integer and fractional quantizers. However, due to time mismatch, when P_0 leads REF in the fractional quantizer with an output of 0, P_0 may lag REF in the integer quantizer and incorrectly reduce the output by 1. Similarly, when P_0 lags REF in the fractional quantizer but leads REF in the integer quantizer, the output is incorrectly increased by 1.

To compensate for the errors, an early/late detector with output S is proposed to detect the time difference between P_0 and REF in the integer quantizer. The signal S indicates whether P_0 leads or lags REF. When P_0 leads REF in the fractional phase quantizer, the fractional output becomes 0. If there is no time mismatch, S becomes 0. If P_0 lags REF in the integer phase quantizer, S becomes 1, and the counter misses one period. As a consequence, the digitized output can be compensated according to S and the quantized fractional phase. If P_0 leads REF in the integer quantizer with output S of 0 and the fractional output is 13/14, the digitized output has to be reduced by 1. If P_0 lags REF in the integer quantizer with output S of 1 and the fractional output is 0, the digitized output has to be increased by 1.

D. Frequency Divider Chain

The block diagram of the frequency divider chain, which consists of a three-stage frequency pre-scaler and a programmable frequency divider with a division ratio from 16 to 255, is shown in Fig. 11. The frequency pre-scaler uses a 100-GHz *LC*-ILFD followed by a 50-GHz ILFD and a 25-GHz static CML frequency divider. To cover the output frequency of the DCO, the 100-GHz *LC*-ILFD should provide a locking range larger than 26 GHz with sufficient margin. Due to the narrow locking range of the *LC*-ILFD, the 100-/50-GHz ILFDs use a switched transformer and an SCA to tune the output frequency.

Because an SCA increases the tank capacitance and tank current, which requires larger injection current, the enhancement of the locking range becomes limited. As a result, the 100-GHz *LC*-LFD uses a 3-bit switched transformer for coarse tuning of the self-oscillation frequency and a 2-bit SCA for fine tuning to provide locking range overlap for the adjacent coarse tuning band. With the 3-bit switched transformer to provide eight-band operation and to reduce the locking range requirement in each band, the size of the injection transistor is designed to be 6 μm/60 nm to reduce the loading of the DCO. The primary coil of the switched transformer L_{p1} is 80 pH, and the simulated locking range of the 100-GHz *LC*-ILFD is 44 GHz from 75 to 119 GHz with 5–6-GHz locking range for each band.

The second stage of the 50-GHz *LC*-ILFD also uses a switched transformer for coarse tuning and an SCA for fine tuning. Because its locking range requirement is smaller than that of the 100-GHz *LC*-ILFD, only a 2-bit switched transformer with a 265-pH primary coil is needed. The simulated locking range of the 50-GHz *LC*-ILFD is 26 GHz from 34 to 60 GHz, which can cover the output frequency of the first stage.

After the 100-GHz DCO is divided down to 25 GHz, a frequency divider with a four-stage static-CML latch [13], [31] is used to divide down the frequency by four times. The simulated locking range can reach from 14 to 33 GHz, with a 10% margin for an output frequency of the 50-GHz *LC*-ILFD.

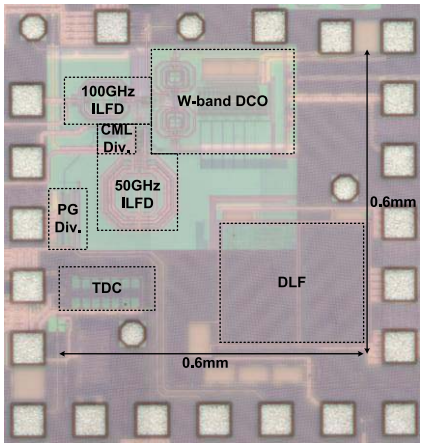


Fig. 12. Chip photograph of the proposed *W*-band ADPLL.

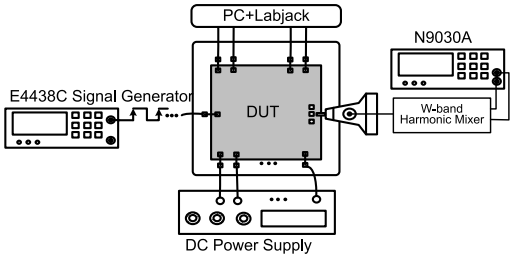


Fig. 13. Measurement setup for the proposed *W*-band ADPLL.

V. Experimental Results

The proposed *W*-band ADPLL is fabricated in a 65-nm CMOS process and occupies a core chip area of 0.36 mm^2, with the fully integrated loop filter occupying only 0.084 mm^2, as shown in Fig. 12. The *W*-band ADPLL consumes 35.5 mW with 0.8- and 1.2-V supply. The DCO and *LC*-ILFDs consume 12 and 10.7 mW, respectively, at a 0.8-V supply for low power consumption while the rest of the loop consumes 12.8 mW (4.8 mW for CML and programmable divider, 4.9 mW for DLF, and 3.1 mW for TDC) at a 1.2-V supply.

As shown in Fig. 13, the output phase noise and frequency spectrum of the *W*-band ADPLL are measured using a waveguide probe with a *W*-band harmonic mixer to down-convert it to lower frequency, and by an Agilent N9030A spectrum analyzer. The reference input is generated by an Agilent E4438C signal generator.

The split transformer can be reconfigured into $N = 1$ with the same control signal for D_{0-5}, as shown in Fig. 14(a), and $N = 3$ with $D_0 = D_1$, $D_2 = D_3$, and $D_4 = D_5$, as shown in Fig. 14(b). To verify the effectiveness of the split transformer, the measurement of the DCO's start-up current is carried out with different configurations of the split transformer. As shown in Fig. 15(a), with $N = 1$, because of severe quality factor degradation, the DCO fails to oscillate at most of the frequencies. As N is increased, the overall tank Q is improved, and the start-up current becomes smaller. Specifically, for $N = 6$, as compared to $N = 3$, not only does the DCO oscillate over a much wider TR (from 21.5% to 27%) but it also has a better start-up current (7 mA instead

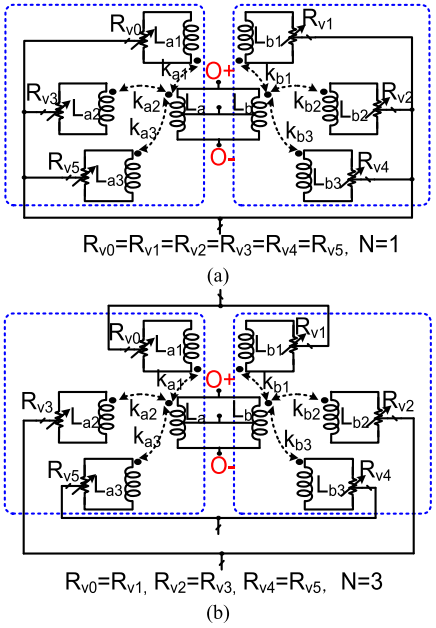


Fig. 14. Reconfiguration of the split transformer for (a) $N = 1$ and (b) $N = 3$.

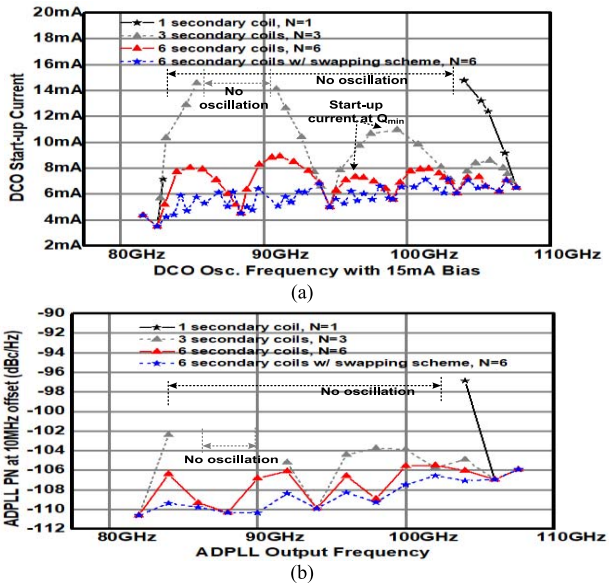


Fig. 15. Measurements of the proposed DCO. (a) Measured start-up current versus the DCO frequency. (b) Measured 10-MHz phase noise for different configurations of the split transformer versus the ADPLL output frequency with BW <0.2 MHz.

of 11 mA) and thus better Q and phase noise (-106 dBc/Hz instead of -102 dBc/Hz at 84 GHz). With the swapping scheme, the 10-MHz phase noise is further improved from -106 to -109 dBc/Hz at 84 GHz. The TRs of D_0–D_5 are 1.2, 2.95, 4.45, 4.4, 6.2, and 5.8 GHz, respectively, which enables similarly high Q over the entire frequency range.

The free-running DCO measures a frequency TR from 82- to 107.6-GHz and 10-MHz offset phase noise from -106 to -110 dBc/Hz, as shown in Fig. 15(b). It draws 15 mA from a 0.8-V supply, which corresponds to a figure of merit (FOM) from -175.8 to -177.5 dB and an FOM$_T$ from -184.4 to -186.1 dB. Table I summarizes the

TABLE I

PERFORMANCE SUMMARY AND COMPARISON OF THE *W*-BAND DCO WITH STATE-OF-THE-ART ~100-GHz OSCILLATORS

	Adnan, RFIC'13 [16]	Adnan, ISSCC'14 [17]	H. Koo, TCASI'15 [20]	Chiang, ISSCC'14 [18]	Kananizadeh ISSCC'16 [19]	Liu, A-SSCC'16 [23]	This Work
Freq. (GHz)	99~110	123.5~131.75	112~127	93.3~101.1	85.4~105	95.7~110.5	82~107.6
TR (%)	9.5	4.3	12.5	8	20.5	14.3	27
Phase Noise (dBc/Hz)	-92.8 @1 MHz	-91~-100 @1 MHz	-104.4~-116.9 @10 MHz	-86.3 @1 MHz	-101 ~ -108.6 @10 MHz	-100.6 ~ -106.9 @10 MHz	-106~-110 @10 MHz
Power (mW)	54	227	18.5	105.6	294/183	6.2	12
FOM * (dB)	-175.5	-169.5~-178.4	-185.2~-173.8	-165.7	-166.4~-154.9	-172.3~ -178.6	-175.8~-177.5
FOMT ** (dB)	-175	-162.2~-171.1	-187.1~-175.7	-163.7	-172.6~-161.1	-175.4~-181.7	-184.4~ -186.1
Process	CMOS 65-nm	CMOS 65-nm	CMOS 65-nm	BiCMOS 90-nm	BiCMOS 130-nm	CMOS 65-nm	CMOS 65-nm

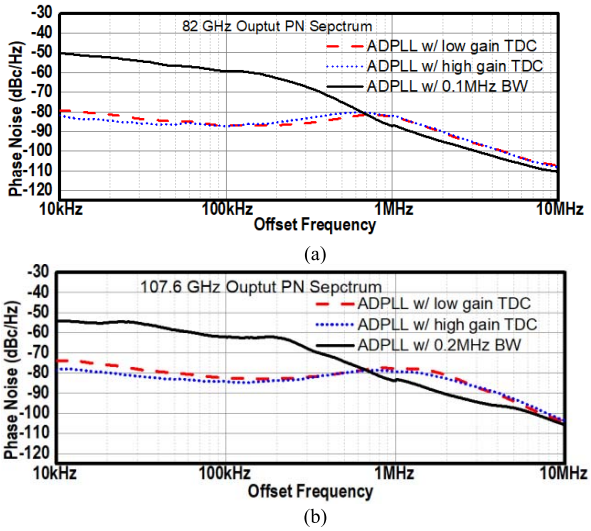


Fig. 16. Measured phase noise spectrum of the *W*-band ADPLL at (a) 82 and (b) 107.6 GHz.

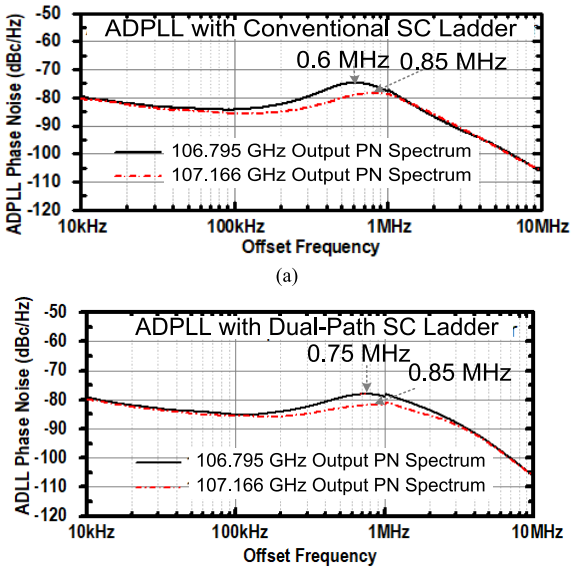


Fig. 17. Measured phase noise spectra of the proposed ADPLL (a) with conventional SC ladder and (b) with dual-path SC ladder.

performance of the proposed *W*-band DCO and compares it with the existing oscillators whose fundamental frequencies are around 100 GHz. Thanks to the proposed split transformer, the *W*-band DCO achieves the widest tuning, of up to 27%, and the best worst-case FOM_T, as well as a comparable FOM among the existing 100-GHz oscillators.

Fig. 16 shows the measured phase noise spectra of the *W*-band ADPLL at 82- and 107.6-GHz output frequency with different gains of the TDC and BW. The high-gain TDC uses a 1-V/80-ps clock-skew sampler while the low-gain TDC uses a 1-V/160-ps clock-skew sampler. With the high-gain TDC, the gain of the DLF is reduced by half to maintain a ~1-MHz BW, and the close-in phase noise at 10-kHz offset is improved from −79.2 to −81.7 dBc/Hz at 82 GHz and from −74.1 to −78.6 dBc/Hz at 107.6 GHz. The phase noise at 100-kHz offset is better than −84.2 dBc/Hz and almost not affected by a larger phase-detection gain, which means TDC has minor noise contribution. The measured 10-MHz phase noise is also included for a 0.2-MHz BW to illustrate the DCO's phase noise. The integrated jitter from 10 to 100 kHz is 49–50 fs, showing the close-in contribution of the TDC and of the reference/frequency divider while the integrated jitter from 10 kHz to 10 MHz is 0.278–0.328 ps.

Fig. 17 shows the measured phase noise spectra of the ADPLL with a conventional SC ladder and of the ADPLL with the dual-path SC ladder. The conventional SC ladder is configured by bypassing the integrator in the integral path, as shown in Fig. 5, and adjusting the DLF gain for a 0.85-MHz BW at 107.166 GHz. The SC ladders are tuned to change the output frequency from 107.166 to 106.795 GHz, which introduces the scaling factor and BW variation. By directly using the conventional SC ladder, the BW varies from 0.85 to 0.6 MHz [Fig. 17(a)] while the BW varies from 0.85 to 0.75 MHz with the dual-path tuning scheme [Fig. 17(b)], showing BW variation reduction using the dual-path SC ladder. Fig. 18(a) and (b) shows the measured downconverted output spectra at 82 and 107.6 GHz with reference spur of −53 and −34 dBc, respectively. Because of wide TR and high control gain, the DCO becomes more sensitive to coupling

TABLE II

PERFORMANCE SUMMARY AND COMPARISON OF STATE-OF-THE-ART mmW PLLs

	Szortyka, JSSC'15 [9]	Wu, JSSC'14 [13]	Hussein, ISSCC'17 [14]	Kang, TMTT'14 [11]	Chao, RFIC'14 [12]	This Work	
	60-GHz PLLs			100-GHz PLLs			
PLL Architecture	Integer-N	Fractional-N	Fractional-N	Integer-N	Integer-N	Integer-N	
	Sub-sampling PLL	ADPLL	ADPLL	CP-PLL	CP-PLL + 2nd harmonic	ADPLL	
Freq. (GHz)	53.8-63.3 (16.2%)	56.4-63.4 (11.7%)	50.2-66.5 (27.9%)	92.7-100.2 (7.8%)	96.8-108.5 (11.4%)	82.0~107.6 (27%)	
f_{REF} (MHz)	40	100	100	1500	200	125	
Close-in PN (dBc/Hz)	-80 @10 kHz -89 ~ -92 @0.2-MHz	-75 @10 kHz -72 @0.1 MHz	-79~-83 @10-kHz	-92.5 @0.1 MHz	-77 @10 kHz -84 @0.1 MHz	-78.6~-81.7@10 kHz -84.2~-87.1 @0.1 MHz (BW≈1 MHz)	
PN (dBc/Hz) Δf=10 MHz	-108	-110	-116~-126	-105.5	-104	-106~-110 (BW<0.2 MHz)	-104~-108 (BW≈1 MHz)
Power(mW)	42	48	46	469.3	14	35.5	
Ref. Spur (dBc)	-40	-74	-59.1~-68	-60	-35	-34~-52 (BW≈1 MHz)	
VDD (V)	1	1.2	1	3.3,2.5,1.2	1.2/0.6	1.2/0.8	
On-Chip Loop Filter	N/A	Yes	Yes	Yes	No	Yes	
Jitter(ps)	0.2~0.35 (10 K~100 M)	0.59 (10 K~10 M)	0.22~0.26 (Unknown)	0.0785 (10 K~100 M)	N/A	0.276~0.328 (10 K~10 M, BW≈1 MHz)	
FOM_J*(dB)	-237.7~-232.9	-227.8	-236.5~-235	-235.4	N/A	-235.7~-234.2	
FOM ** (dB) Δf=10-MHz	-167.3	-168.8	-175.7~ -183.5	-158.3	-172.5	-171~-173 (BW<0.2 MHz)	-169~-171 (BW≈1 MHz)
FOM_T ** (dB) Δf=10-MHz	-171.4	-170.1	-184.6~ -192.4	-156.2	-173.6	-178~-181 (BW<0.2 MHz)	-176~-179 (BW≈1 MHz)
Area [mm2]	0.16	0.48	0.45	0.93	0.39	0.36	
Process	CMOS 40-nm	CMOS 65-nm	CMOS 65-nm	SiGe 130-nm	CMOS 65-nm	CMOS 65-nm	

*FOM_J = 20log(Jitter/1 s) + 10log(Power/1 mW) **FOM = PN - 20log(f_o/Δf) + 10log(Power/1 mW) ***FOM_T = PN - 20log(f_o /Δf *FTR/10%) + 10log(Power/1-mW)

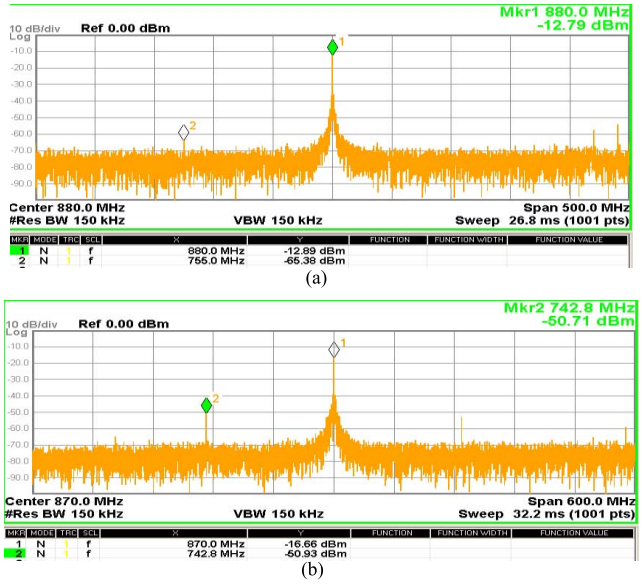


Fig. 18. Measured downconverted spectra at (a) 82- and (b) 107.6-GHz output.

from reference spur. When the variable resistors are turned on for the highest frequency, the spur can modulate the ON-resistance and then modulate the DCO frequency.

Table II summarizes the performance of the proposed *W*-band ADPLL, which is the very first ADPLL operating over 100 GHz, and compares with the existing mmW PLLs. With 125-MHz reference and divided-by-16 frequency pre-scaler, the ADPLL achieves a 2-GHz frequency tuning step. Thanks to the exponentially scaling SC ladder with dual-path architecture, the proposed ADPLL achieves the highest operation frequency among mmW ADPLLs. With the proposed split transformer technique, the proposed ADPLL achieves a 25.6-GHz TR, which is the widest among existing *W*-band PLLs [11], [12], and with the proposed clock-skew-sampling delta–sigma TDC, it achieves low in-band phase noise down to around −87 dBc/Hz and 0.278-ps integrated jitter, which is comparable to even the existing 60-GHz ADPLLs [13], [14] and analog PLLs [9]. Compared with [12], our worst-case reference spur is still comparable even with a larger division ratio and lower reference frequency.

VI. CONCLUSION

A split transformer as a variable inductor was proposed to relax the tradeoff between phase noise and TR and achieve a frequency TR from 82 to 107.6 GHz. Moreover, by utilizing a dual-path architecture, the scaling factor variation of high-resolution exponentially scaling SC ladder is suppressed to reduce BW variation of the proposed *W*-band ADPLL. Finally, a clock-skew sampling delta–sigma TDC was proposed to achieve in-band phase noise of −87 dBc/Hz at 100 GHz, which is still comparable with the existing analog PLLs and ADPLLs operating at 60 GHz. To the best of our knowledge, this is the very first CMOS *W*-band ADPLL operating over 100 GHz with the widest TR while consuming only 35.5 mW.

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Zhiqiang Huang was born in Zhangzhou, Fujian, China, in 1990. He received the B.E. degree in integrated circuit design and integrated systems from the University of Electronic Science and Technology of China, Chengdu, China, in 2012, and the Ph.D. degree from The Hong Kong University of Science and Technology, Hong Kong, in 2017.

In 2018, he joined Samsung Semiconductor Inc., San Jose, CA, USA. His research interests include frequency synthesis from RF to millimeter wave in CMOS.

Howard C. Luong (F'14) received the B.S., M.S., and Ph.D. degrees in electrical engineering and computer sciences from the University of California at Berkeley, Berkeley, CA, USA, in 1988, 1990, and 1994, respectively.

Since 1994, he has been the Electrical and Electronic Engineering Faculty with The Hong Kong University of Science and Technology, Hong Kong, where he is currently a Professor. He has co-authored three technical books entitled the *Design Techniques for Transformer-Based VCOs and Frequency Dividers*, *Low-Voltage RF CMOS Frequency Synthesizers*, and *Design of Low-Voltage CMOS Switched-Opamp Switched-Capacitor Systems*. His research interests include RF and analog integrated circuits and systems for wireless and portable applications.

Dr. Luong is currently serving as a Technical Program Committee Member for the IEEE International Solid-State Circuits Conference (ISSCC) and an Associate Editor for the IEEE SOLID-STATE CIRCUITS LETTERS and the IEEE VIRTUAL JOURNAL ON RFIC. He was also a Distinguished Lecturer of the IEEE Solid-State Circuits Society from 2012 to 2014.