A Bandgap Reference Circuit Design for Power-on Reset Related Circuits

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***Abstract*— There are many portable devices applications implemented in System On a Chip (SOC) technology, which need to have a safety operation in extreme conditions for voltage power supplies. Due to that, a good voltage level power supply evaluation is required. This paper proposes a possible design for bandgap reference (BGR) used to generate multiple reference voltage levels for a Power-On Reset (POR) circuit. In this way, a reduced sensitivity to temperature and various process variations is achieved for the POR voltage threshold levels. The BGR circuit has been designed, simulated, and implemented. The results show that the reference voltage V_{REF} has only a 5% variation under the temperature range from -55.DEG.C. to 125.DEG.C. The power consumption is 40uW considering a 3.3 V power supply.**

I. INTRODUCTION

Complex circuits that contain various voltage levels need a certain sequence of voltages for startup. These sequences are determined by the power supply voltage levels, and can be in the range of 1V, 1.2V, 1.5V, 1.8V, 2,5V and 3.3V. In critical applications, the correct operation of each block is guaranteed only if the power supply level of that specific block does not fall below a certain critical level, which can be 30-50% of the nominal voltage supply. In a standard CMOS technology with voltage references based on the physical parameters of the devices (such as the threshold voltage of transistors, inverters or direct-biased p-n junctions) is difficult to obtain a temperature or process invariant reference voltage. In this case it is recommended to use a BGR circuit to generate the required reference voltage levels for the POR circuit [1].

A BGR designed for a POR circuit has to fulfill several conditions such as:

(1) Low current consumption.

(2) Correct functionality starting from a voltage almost equal to its output reference voltage.

(3) Startup time close to zero

(4) Ability to generate an enable signal, which flags the presence of the required reference voltage level at the output of the BGR circuit.

(5) Ability to provide the necessary power supply references needed by the blocks that make up the POR circuit (it is recommended for the BGR circuit to generate several voltage reference levels such as 0.4V, 0.5V, 0.6V, 0.8V, 1.0V, 1.2V which can be compared either to the supply voltages or to a ratio of the supply voltages).

The core voltage supply (1V) is too close to the diode forward voltage (0.6-0.8V) and due to that, the core voltage supply, VDD, is not properly monitored provided the BGR circuit would be implemented in this voltage supply domain. The best solution is to implement BGR circuit in the highest possible I/O voltage supply domain, VCC. In this case, the BGR circuit will work properly for a voltage supply greater than 1.25V and that would represent less than 40-50% of the I/O nominal voltage supply value (VCC can be 3.3V or 2.5V).

II. THEORETICAL CONCEPTS

Figure 1 depicts the schematic of the proposed BGR circuit. The most robust manner for BGR circuit design is to ensure the necessary current ratio I_{E1}/I_{E2} through the resistors ratio R_2/R_1, where ($R_2 = R_{21}+R_{22}$).

$$I_{E1}R_1 = I_{E2}R_2 \tag{1}$$

The proposed structure of the BGR (Fig. 1) allows the 'OUT_12' output to be directly connected to a resistive divisor (R_{DV1}–R_{DV6}), without a supplemental signal conditioning circuit. In the following theoretical evaluation, V_{REF} is similar to the output voltage V(OUT_12). The algorithm is inspired from [2] and [3]. The reference voltage can be expressed as:

$$V_{REF} = V_{BE1} + \frac{R_2}{R_3}\Delta V_{BE} \tag{2}$$

where $\Delta V_{BE} = V_{BE1} - V_{BE2}$

The values of the emitter and saturation currents (I_E) and (I_S) of the transistors are given by:

$$I_E \approx I_S \exp\left(\frac{q}{kT}V_{BE}\right) \tag{3}$$

$$I_S \approx A_E \eta T^{\gamma} \exp\left(-\frac{qE_0}{kT}\right) \tag{4}$$

where A_E is the emitter-base area of the bipolar transistor, η is a temperature independent constant, γ is a temperature coefficient, typically γ=3.2 and 'E_0' is the silicon band-gap voltage, a temperature independent constant (E_0 =1.205V).

From equations (1)-(4) it can be concluded that:

$$\Delta V_{BE} = \frac{kT}{q}\ln\left(\frac{I_{E1}}{I_{E2}}\cdot\frac{I_{S2}}{I_{S1}}\right) = \frac{kT}{q}\ln\left(\frac{R_2}{R_1}\cdot\frac{A_{E2}}{A_{E1}}\right) \tag{5}$$

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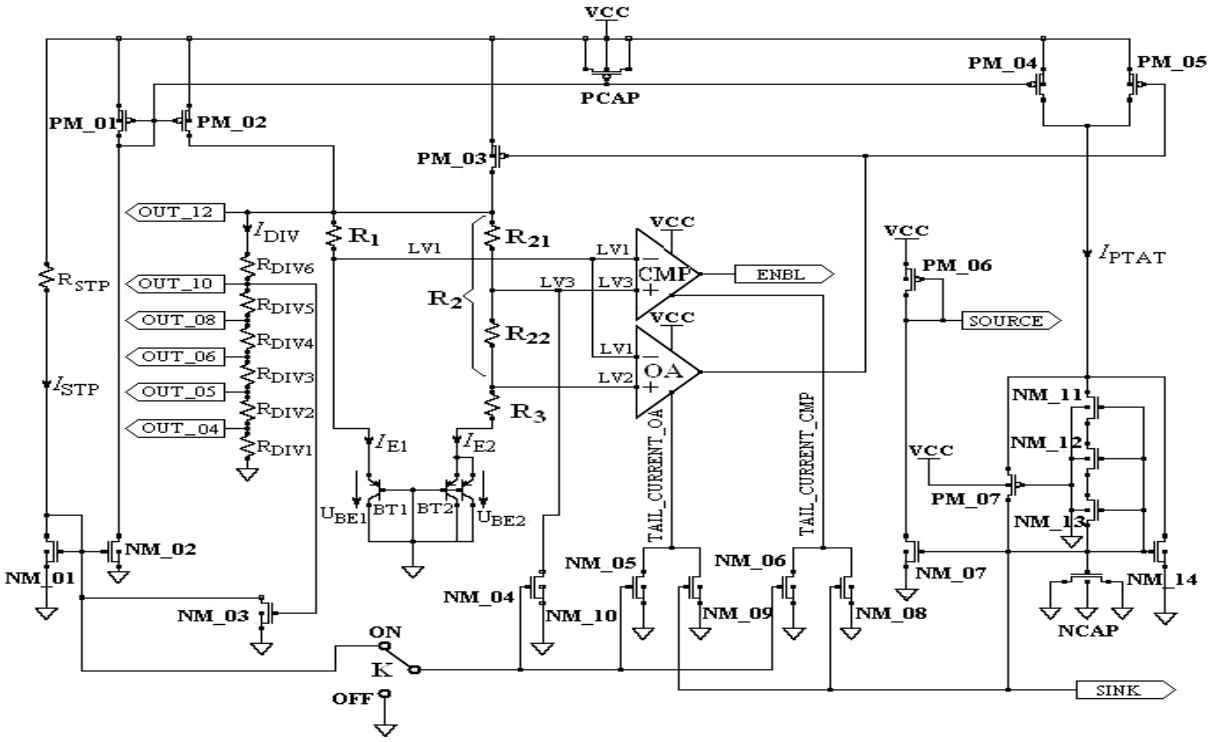

Figure 1. Proposed bandgap reference circuit

where A_{E1} and A_{E2} are the total emitter-base areas of the equivalent bipolar transistors BT1 and BT2, respectively. The voltage V_{BE1} in (2) can be considered the unknown element and may be determined from the chart that depicts its variation with temperature. Supposing that T_0 is the reference temperature, the next step is to determine the voltage $V_{BE1}(T)$ as referred to the known voltage value $V_{BE1}(T_0)$ and the ratio T/T_0, where T is the circuit operating temperature.

From Fig. 1, I_{E2} current can be expressed as:

$$I_{E2}(T) = \frac{\Delta V_{BE}(T)}{R_3} \tag{6}$$

Combining (2), (3), (4), (5) and (6) results:

$$\frac{I_{E1}(T)}{I_{E1}(T_0)} = \frac{T}{T_0} \cdot \frac{R_{3T0}}{R_{3T}} \approx \left(\frac{T}{T_0}\right)^{\alpha} \tag{7}$$

and, then, the reference voltage value, $V_{REF}(T)$ is given by:

$$V_{REF}(T) = E_0 + \left\{ \frac{T}{T_0}\left[V_{BE1}(T_0) - E_0\right] + (\alpha - \gamma)\frac{kT}{q}\ln\left(\frac{T}{T_0}\right) + \frac{kT}{q}\cdot\frac{R_2}{R_3}\ln\left(\frac{R_2}{R_1}\cdot\frac{A_{E2}}{A_{E1}}\right)\right\} \tag{8}$$

In (7) R_{3T} and R_{3T0} represent the values of the resistor R_3 at temperatures T and T_0, respectively. If R_3 is temperature insensitive, then coefficient α is 1.

Starting from this point, the design procedure diverges from the standard BGR circuit procedure. The goal is not to obtain a very performance reference voltage, but rather to ensure that the required voltage levels do not overlap, due to temperature or process variation. Taking into consideration both the requested voltage reference levels (0.4V, 0.5V, 0.6V, 0.8V, 1.0V and 1.2V), and the layout design demands for a matching resistive divisor layout, the best solution would be to design the BGR circuit for a 1.2V reference output voltage:

$$V_{REF}(T_0) = V_{OUT\_120}(T_0) = E_0 \approx 1.2V \tag{9}$$

Therefore, no derivation for (8) will be performed and the reference voltage variation will be theoretically estimated in (12) and compared afterward to the simulation results.

III. BGR CIRCUIT DESIGN

To design the BGR circuit, the following rates and resistor value are imposed at first:

$$\frac{A_{E2}}{A_{E1}} = 2; \qquad \frac{I_{E1}}{I_{E2}} = 3 \quad and \quad R_1 = 100k\Omega \tag{10}$$

Combining (1) and (10) and then (8) and (9), yields

$$R_2 = \frac{I_{E1}}{I_{E2}}R_1 = 300k\Omega \quad and \quad R_3 = 30k\Omega \tag{11}$$

If the reference temperature is considered to be 300°K, the value for voltage $V_{BE1}(T_0)$ and the equivalent current $I_{E1}(T_0)$ may be obtained with a test circuit. Considering a temperature variation between T_1=220°K and T_2=400°K, the reference voltage $\Delta V_{REF}(T)$ is evaluated with (8):

$$\begin{aligned} \Delta V_{REF}(T_1) &= V_{REF}(220) - V_{REF}(300) = +0.007V \\ \Delta V_{REF}(T_2) &= V_{REF}(400) - V_{REF}(300) = -0.028V \end{aligned} \tag{12}$$

Assuming a reference temperature of T_0=300°K and the BGR voltage imposed by (9), the reference voltage variations (12) point to a theoretical relative value lower than 2.5%. This accuracy is satisfactory for the voltage reference used in the POR related circuits.

IV. THE REFERENCE VOLTAGE VALIDATION CIRCUIT

The BGR generates a set of fractional reference voltages, which are used for evaluating the values of the supply voltages. The result of this comparison is subsequently translated into a set of validation signals which enable or disable some blocks of the chip. Therefore, it is essential to verify that the values given by the BGR at outputs OUT_04, OUT_06, OUT_08, OUT_10 and OUT_12 (Fig. 1) are correct.

On the other hand, the diode branches of a BGR circuit can be used as a level detector if the output of the operational amplifier is disconnected from the diodes branches and used as a comparator. At the same time the diode branches have to be connected to the voltage source, whose voltage level has to be detected. If the desired voltage level., V_{LEVEL} , is chosen to be less that V_{REF} , both functions (reference voltage and voltage detector) can be performed using the same diodes' branches. Thus, the output of OA amplifier (Fig. 1) generates the reference voltage V_{REF} and the voltage level detection is performed by CMP comparator and the divisor R_{21} –R_{22} .

The amplifier OA assures the same voltage for the LV1 and LV2 nodes. Substituting (1) and (5) in (2) another expression for V_{REF} can be obtained:

$$V_{REF} = V_{BE1} + \frac{R_{21}+R_{22}}{R_3}\cdot\frac{kT}{q}\ln\left(\frac{R_{21}+R_{22}}{R_1}\cdot\frac{A_{E2}}{A_{E1}}\right) \qquad (13)$$

where $R_{21}+R_{22}=R_2$.

When V(OUT_12)=V_{REF}, the potential of node LV3 is greater than that of node LV2 (Fig. 1). The value of the output voltage V(OUT_12) for which nodes LV2 and LV3 have the same potential is given by (16) and represent the toggle point for the comparator CPM:

$$V_{LEVEL} = V_{BE1} + \frac{R_{21}}{R_3+R_{22}}\cdot\frac{kT}{q}\ln\left(\frac{R_{21}}{R_1}\cdot\frac{A_{E2}}{A_{E1}}\right) < V_{REF} \qquad (14)$$

For resistor R_{22} the recommended value is the smallest value compatible to the layout of resistors R_1, R_{21}, R_{22} and R_3, which have to be properly matched.

$$R_{21} = 290k\Omega \qquad R_{22} = 10k\Omega \qquad (15)$$

In Fig. 2, the toggle point of the circuit from Fig. 1 when K is in OFF position, is point B, and has a voltage value of 1.1V. It is important to notice that when ENBL signal toggles, the voltage V(OUT_120) and the supply voltage VCC are equal.
The signal ENBL toggles to '1' when the BGR circuit is able to generate a reference voltage level with a relative error less than 8%. Also, as long as V(OUT_12) is less than the reference voltage value, V_{REF}, given in (9), and ENBL signal is '1', the voltage V(OUT_12) is almost equal to the voltage supply VCC. As soon as the supply voltage VCC is greater than the reference voltage the BGR circuit will generate the desired voltage value.

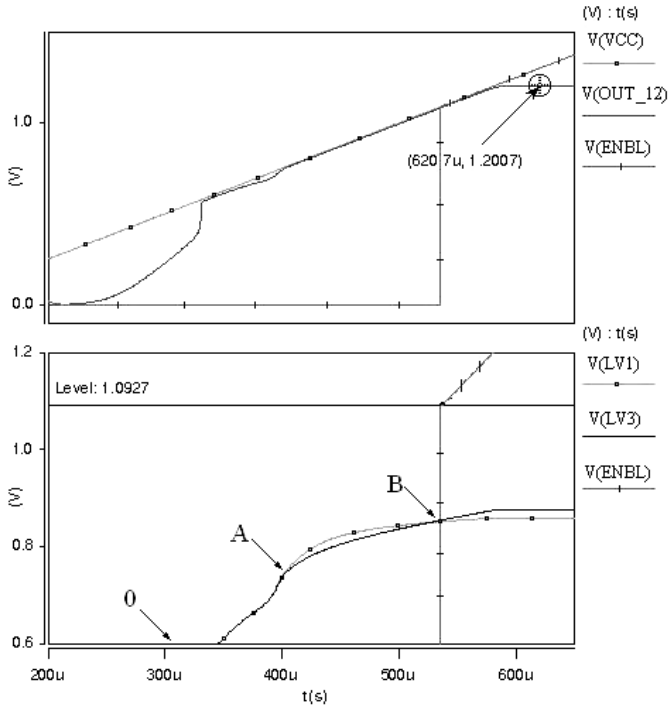

Figure 2. Toggle point for ENBL signal

V. START-UP CIRCUIT

In Fig. 1, when the K switch is in OFF position, a standard start-up circuit is enabled (transistors NM_01, NM_02, NM_03, PM_01, PM_02 and resistor R_{STP}) [5].

Due to the special purpose of the BGR circuit presented in Fig. 1, two main circuit demands have to be accomplished:

- Low power consumption during steady-state operation.
- Fast and safe start-up for any temperature and process variations.

Due to the first demand, a small tail current for amplifier (OA) and comparator (CMP) is required. On the other hand, analyzing Fig. 2, during the VCC supply rise up, there is a voltage interval for which the voltage levels V(LV1) and V(LV2) are almost equal (R_{21} is 290K and R_{22} is 10K so V(LV3) is a little greater than V(LV2), but practically they are equal: V(LV3) ≈V(LV2). For clarity, in Fig. 2 and Fig. 3 only V(LV3) is plotted). In Fig. 3 this interval is between points 0 and A. In case NM_03 turns on, while the voltages V(LV1) and V(LV2) are still below point A, the differential input voltage of OA (Fig. 1), is too small to force the amplifier output to transfer the current from transistor PM_02 to transistor PM_03. This situation appears in the Monte-Carlo simulations. A very good solution for this issue is presented in Fig. 1, considering the switch K in ON position.

During the start-up interval (as long as NM_03 is OFF and VCC supply is rising), the OA tail current is improved by transistors MN_05 and PM_04. On the other hand MN_04 will push down the voltage potential of nodes LV3 and LV2. This will assure a significant improvement of the OA input differential voltage (Fig. 3). In the same time, the transistor

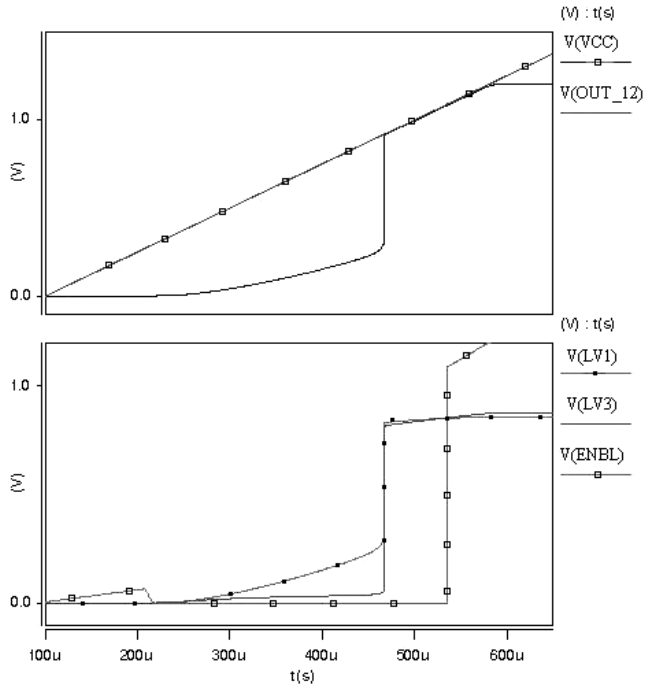

Figure 3. Voltage waveforms for improved start-up operation

PM_02 is a weak transistor and due to this fact, almost all current is assured by the amplifier output through PM_03.

VI. SIMULATION RESULTS

Based on the procedure presented in this paper, a BGR circuit was designed and implemented in 45nm CMOS technology. That means that for 3.3V I/O voltage domain, the minimum transistors' length is 0.36um. The transistors BT1 and BT2, are factory pre-defined vertical PNP transistors and their dimensions are 3.2x3.2μm^2. The circuit was implemented in silicon, but for testing only POR's top signals were available. The simulations were performed in HSPICE. Significant post layout simulations results are presented in Fig. 3 to Fig. 5. In Fig. 4 are depicted the I/O voltage supply current (I(VCC)) and the reference voltage (V_{REF}=V(OUT_12)) variations under power supply rise and the temperature range variation from the values of –55.DEG.C. to 125.DEG.C. During start up, the circuit absorbs a consistent increased amount of current, which forces

the BGR circuit to achieve the nominal steady state operation as soon as the supply voltage VCC exceeds the reference voltage level V_{REF} (9). For the steady state operation, the power supply current I(VCC) is less than 10uA, for all the power supply voltage levels greater than 1.3V. The maximum power consumption is less than 40uW (when VCC is 3.3V). Fig. 4 also points out that the output reference voltage variation (V(OUT_12=V_{REF}) is between 1.1903V and 1.2025V which represents a relative range between –0.8% and +0.2% from the reference nominal value (9). These values are better than the theoretical ones (12).

The Monte Carlo simulations point out an absolute reference voltage variation under both temperature and power supply voltage between -0.0617V (-5.1%) and +0.0548V (4.5%). Fig. 5

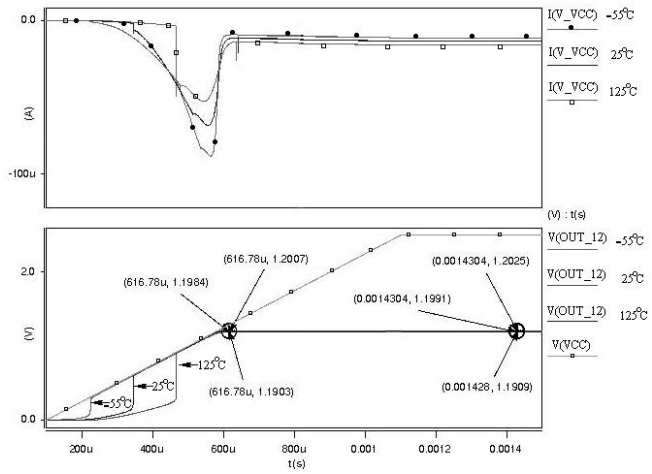

Figure 4. Supply current and reference voltage variation under different temperature conditions

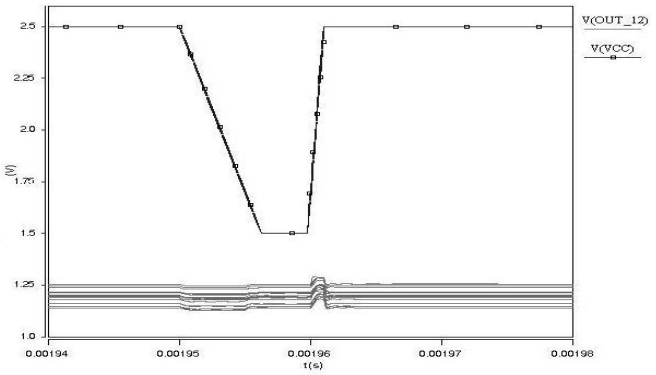

Figure 5. Monte Carlo results for reference voltage during power supply glitch

shows the reference voltage variation (V(OUT_12)) in case when a voltage glitch (rate 1V/us) appears on the power supply.

VII. CONCLUSIONS

The experimental results reflect a good dinamic behavior of the BGR circuit presented in this paper, and also a low power consumption. The circuit can be succesfully used in POR related circuits for a correct evaluation of all supplies voltage levels. The circuit assures also a good imunity to voltage glitches that can apear on the power supply.

VIII. REFERENCES

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