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A 352nW, 30 ppm/°C all MOS nano ampere current reference circuit☆

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ABSTRACT

In this work, an ultra low power all-MOSFET based current reference circuit, developed in 0.18 μm CMOS technology, is presented. The proposed circuit is based on the classical resistor-less beta multiplier circuit with an additional temperature compensation feature. The circuit is capable of providing the reference current in a nanoampere range for the supply voltage ranging from 1 V to 2 V in the industrial temperature range of −40 °C to 85 °C. The measurements were performed on 10 prototypes. The measured mean value of the reference current is 58.7 nA with a mean temperature coefficient value of 30 ppm/°C. In addition, the measured mean line regulation is 3.4%/V in the given supply voltage range. The total current consumption of the circuit is 352 nA and the chip area is 0.036 mm^2.

1. Introduction

Internet of Things (IoT) has become a global phenomenon due to the ongoing developments in smart portable devices with capability to connect to the internet [1]. These are mainly battery-operated, hence, nano-power integrated circuits that can extend the battery life have been in highly appreciated. The typical building blocks of these portable devices are the sensor interface circuit, analog to digital converters (ADC), storage memories, the micro-controller and the transceiver system [2,3]. The successful operation of these components strongly depends on a special class of circuits that is commonly known as a reference circuit. They are a part of the biasing network and are responsible for providing a proper quiescent point to the core circuits, irrespective of the supply voltage, temperature and process variations. Three types of reference circuits are mainly used in the designing which are the voltage reference circuit, the current reference circuit and the frequency reference circuit [4].

The focus of this work is on the development of a circuit for nanoampere reference current generation [5]. In the literature, the implementation strategies for the reference current circuit can be divided into three parts: The first is the conversion of a reference voltage into a reference current [6]. Generally, the bandgap reference generation techniques are used to obtain the reference voltage, which is the temperature compensated base-emitter (V_{be}) voltage of Bipolar Junction Transistor (BJT) [7,8].

In the second method, the reference current is obtained by combining the Proportional To Absolute Temperature (PTAT) and the Complementary To Absolute Temperature (CTAT) currents [9,10].

The third strategy is a direct method where the current reference circuit implementations are based on the classical beta-multiplier circuit [11]. However, the presence of a resistor (See Fig. 1a) in the circuit makes it unsuitable for nano-ampere current generation, since for obtaining these current values, a gigaohms or higher value of resistor would be required. To make the beta-multiplier circuit suitable for nano-ampere current values, the passive resistor was replaced by the Metal Oxide Semiconductor Field Effect Transistor (MOSFET) operating in the triode region (See Fig. 1b). The bias voltage required for nMOSFET(n-type MOSFET) resistor M_{n3} is obtained from the diode-connected transistor M_{n4}. This implementation is also known as Resistor-less Beta Multiplier (RBM) circuit [12]. Various current reference circuits based on the RBM circuit are reported in the literature with nano-watt power consumption [13–16]. The proposed current reference circuit is also based on the RBM topology where, the aim is to obtain a reference current value lower than 60 nA with a moderate temperature coefficient (<100 ppm/°C) in a supply voltage range of 1–2 V.

The following sections provide the details of the proposed current reference circuit. Section 2 describes the implementation principle of the proposed circuit. Measurement results are shown in Section 3. Finally, the conclusions are presented in Section 4.

2. Design implementation

The resistor-less beta multiplier based current reference circuit used in this implementation is shown Fig. 2 where, M_{p1} to M_{p6} are pMOSFETs (p-type MOSFET), M_{na}, M_{nb}, M_{ny} and M_{n1} are nMOSFETs and I_{ref} is the reference current flowing through the branches of the circuit. In the

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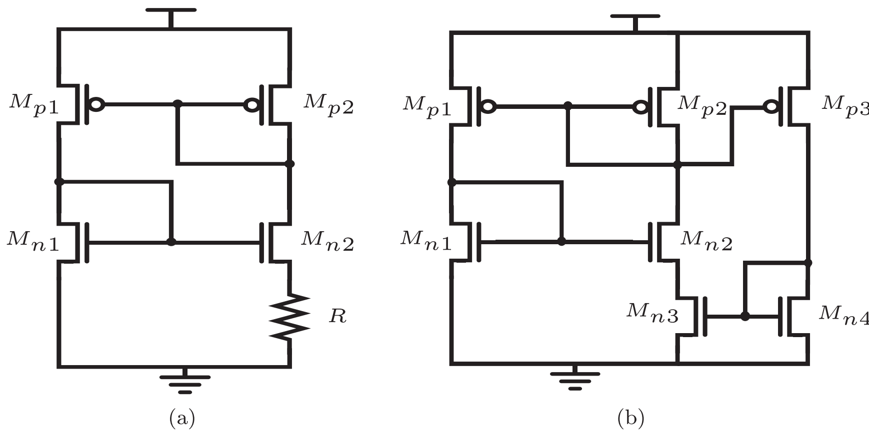

Fig. 1. (a) Conventional Beta Multiplier [11] (b) Resistor-less Beta multiplier circuit [12].

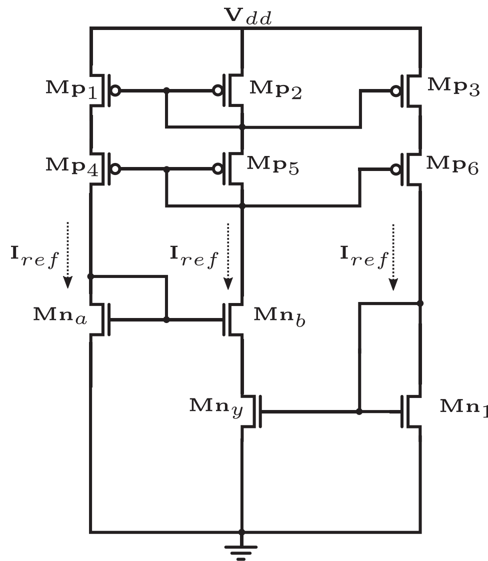

Fig. 2. Resistor-less beta multiplier circuit used in the proposed implementation.

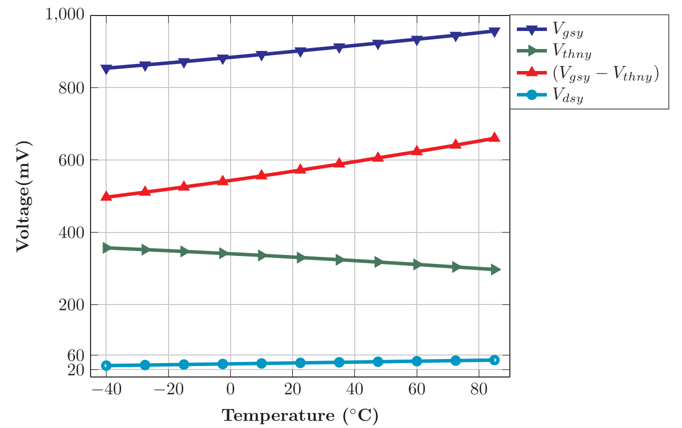

Fig. 3. Simulation results showing variation of voltages of M_{ny} with temperature in redesigned schematic of RBM.

circuit, M_{ny} is operating in a linear region and I_{ref} is flowing through it. Thus,

$$I_{ref} = \mu_n C_{ox} S_y \cdot (V_{gsy} - V_{thn}) \cdot V_{dsy} \tag{1}$$

where μ_n is the mobility parameter, C_{ox} is the gate-oxide capacitance, V_{thn} is the threshold voltage, S is the aspect ratio, V_{gs} is the gate-source voltage and V_{ds} is the drain-source voltage.

To determine the thermal behavior of I_{ref}, differentiate (1) with respect to temperature T:

$$\frac{dI_{ref}}{dT} = C_{ox} S_3 \left[\mu_n V_{dsy} \cdot \underbrace{\frac{d}{dT}(V_{gsy} - V_{thn})}_{a} + \mu_n (V_{gsy} - V_{thn}) \cdot \underbrace{\frac{dV_{dsy}}{dT}}_{b} + \underbrace{(V_{gsy} - V_{thn}) V_{dsy}}_{c} \cdot \frac{d\mu_n}{dT} \right] \tag{2}$$

It can be observed from (2) that the thermal slope of I_{ref} is a function of parameters that are marked using (a), (b) and (c). To understand the impact of the terms, simulations were performed using the Spectre simulator in the Cadence environment. The simulations were done at the supply voltage V_{dd} = 1.25 V for the targeted reference current of 45 nA@22.5 °C over the industrial temperature range of −40 °C to +85 °C in steps of 12.5 °C.

The simulation results of the voltages of the redesigned RBM (See Fig. 2) are shown in Fig. 3.

The first order thermal slope of the voltages V_{gsy}, V_{thn}, (V_{gsy}-V_{thn}) and V_{dsy} obtained from the simulations, are 0.83 mV/°C, −0.48 mV/°C, 1.3 mV/°C and 0.123 mV/°C respectively. By substituting the data obtained from the simulations into (2), it is possible to comment that the reference current I_{ref} will show Proportional To Absolute Temperature (PTAT) behavior which has already been reported in the literature [12,15,17].

Thus, based on the simulation results, to obtain temperature independence in I_{ref}, three conditions should be satisfied. First, the thermal slope of the gate-source (V_{gsy}) and the threshold (V_{thn}) voltages of M_{ny} should be equal *i.e.*, term(a)⇒ 0. Second, the variation of drain-source voltage V_{dsy} with temperature should be minimum thus, term (b)⇒ 0. Finally, if V_{gsy} follows V_{thn} with same magnitude and/or the magnitude of V_{dsy} is small enough then it can be considered that the term(c)⇒ 0. This lowering of the voltage values will also reduce the magnitude of the influence of the mobility parameter over the reference current with the change in temperature.

To achieve the first design goal *i.e* minimizing term (a), an extension to the redesigned RBM, as highlighted in Fig. 4 (Subcircuit A) has been developed. Here, a composite cascode arrangement is formed using nMOSFETs M_{n2} and M_{n3} where, M_{n2} is operating in saturation region and M_{n3} is working in the linear region. The drain terminal of M_{n1} has been tied to the drain terminal of M_{n3} so that the drain-source voltage of M_{n3} also contributes in obtaining the gate-source voltage for M_{ny}.

Applying KVL in the loop formed by Mn_y, Mn_1 and Mn_3 and differentiating w.r.t T will result in,

$$\frac{dV_{gsy}}{dT} = \frac{dV_{gs1}}{dT} + \frac{dV_{ds3}}{dT} = \frac{dV_{thn1}}{dT} + \frac{d}{dT}\sqrt{\frac{I_{ref}}{\mu_n C_{ox} S_1}} + \frac{dV_{ds3}}{dT} \tag{3}$$

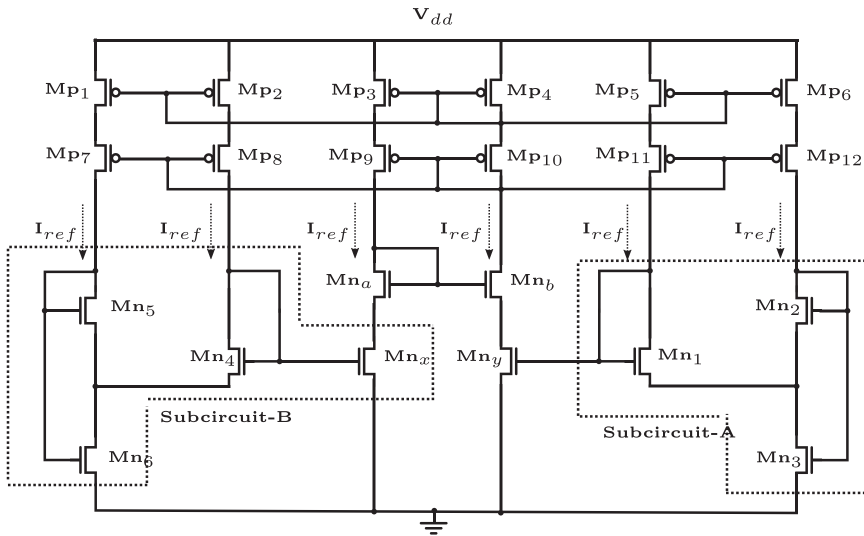

Fig. 4. Proposed reference current generator circuit.

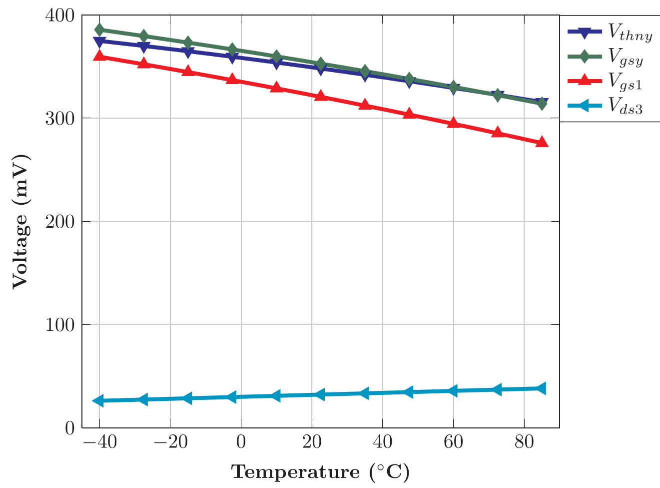

Fig. 5. Simulation results showing variation of voltages of M_{ny} with temperature after including Subcircuit-A.

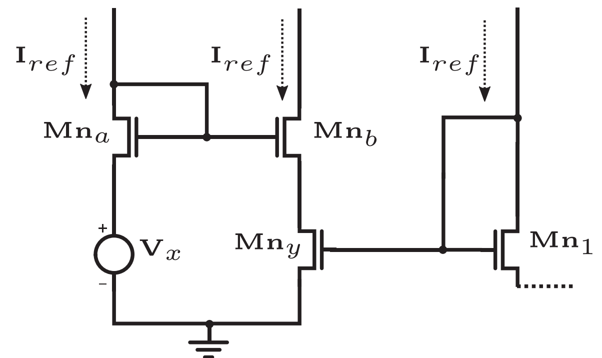

Fig. 6. Conceptual circuit diagram.

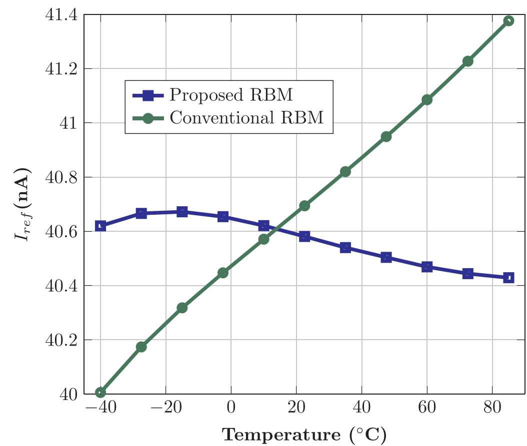

Fig. 7. Simulated reference currents from conventional and proposed RBM circuits.

Table 1
Device sizing used in the implementations.

Device	Conventional	Proposed	Size(W/L)	Remark
pMOSFET	M_{p1} to M_{p6}	M_{p1} to M_{p12}	30 μm/ 5 μm	–
nMOSFET	M_{na}, M_{nb}	M_{na}, M_{nb}	10 μm/5 μm, 40 μm/5 μm	–
nMOSFET	M_{ny}, M_{n1}	–	2 μm/261 μm, 1 μm/736 μm	–
nMOSFET	–	M_{ny}, M_{n1}	2.5 μm/ 20 μm,10 μm/ 42 μm	94%↓, 99.5%↓
nMOSFET	–	M_{nx}, M_{n4}	10 μm/ 5 μm,10 μm/42 μm	
nMOSFET	–	$M_{n2}(M_{n5})$, $M_{n3}(M_{n6})$	10 μm/20 μm	–

To obtain a temperature independent I_{ref} *i.e.* $\frac{dI_{ref}}{dT} = 0$, the following condition is required:

$$\frac{dV_{gsy}}{dT} = \frac{dV_{thn1}}{dT} + \frac{dV_{ds3}}{dT} \tag{4}$$

It is well known that the threshold voltage decreases with increasing temperature and it is technology node dependent quantity [18]. This makes the thermal slope of V_{ds3} as the only circuit-level parameter that can be used to change the thermal slope of V_{gsy}. Ideally, the constraint here is to match the thermal behavior of V_{gsy} with V_{thn} therefore to achieve this condition the thermal slope of V_{ds3} should be positive. Hence, a composite cascode arrangement has been formed by using Mn_2 and Mn_3 This arrangement is commonly known as the PTAT (Proportional To Absolute Temperature) voltage generator in the literature [19]. According to that the thermal slope of PTAT voltage is a function of the magnitude of current flowing,and the device dimension of transistors Mn_3 and Mn_2. The simulation results of the redesigned RBM with the proposed Subcircuit-A are shown in Fig. 5. The results show that the gate-source voltage V_{gsy} is following the threshold voltage V_{thn}

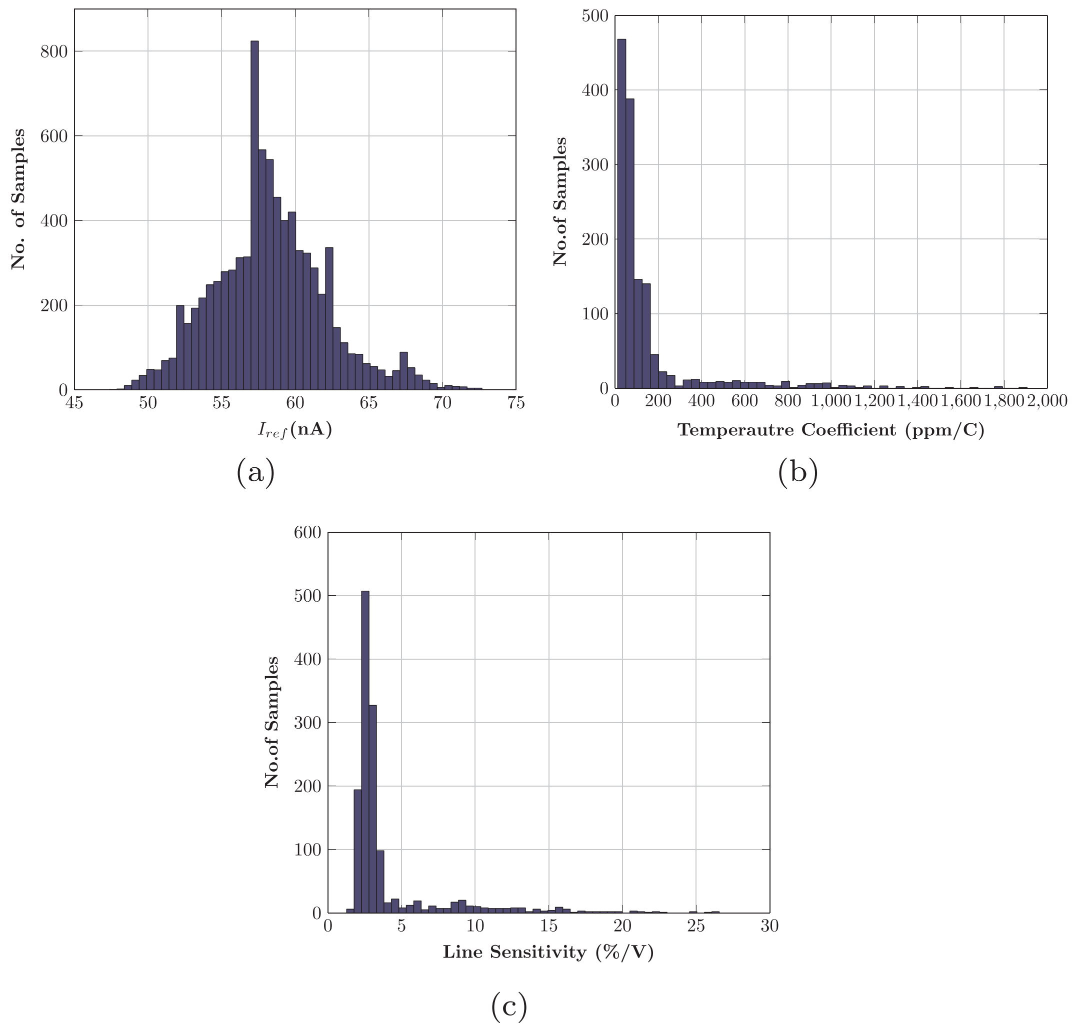

Fig. 8. Distribution plots of the Monte Carlo simulations of the proposed current reference circuit.

Table 2
Summary of statistical analysis obtained after the Mote Carlo simulations.

Parameter	Avg (μ)	Std. Dev. (σ)	Spread(%) (σ/μ)
I_{ref}	45.644 nA	2.9 nA	6.3
TC	236.33 ppm/° C	148 ppm/° C	62.64
LS	4.1%/V	3.7%/V	90.25

and their first order thermal slopes are −0.57 mV/°C and −0.47 mV/°C respectively. Hence, the condition to achieve a thermal independent reference current depicted in the term(a), is fully satisfied. Additionally, this is also contributing in the reduction of magnitudes of terms (b) and (c). To achieve the next design goals (terms(b,c)), revisit the circuit shown in Fig. 2 where, the transistors M_{ny} and M_{n1} are operating in linear and saturation region respectively. Since the same reference current I_{ref} is flowing through them therefore:

$$\mu_n C_{ox} S_y \cdot (V_{gsy} - V_{thn}) \cdot V_{dsy} = \frac{\mu_n C_{ox} S_{n1}}{2} \cdot (V_{gs1} - V_{thn})^2 \tag{5}$$

In the implementation (See Fig. 2), transistor M_{ny} is a MOSFET-based resistor and the gate-voltage that is required to keep it in the deep linear region is provided by the diode-connected transistor M_{n1}. Therefore in (5), V_{gsy} is equal to V_{gs1} and thus V_{dsy} can be given as follow:

$$(V_{gs1} - V_{thn}) = \frac{2S_y}{S_{n1}} \cdot V_{dsy} \tag{6}$$

Substituting (6) in (1) will result in:

$$I_{ref} = \mu_n C_{ox} \cdot \frac{2S_y^2}{S_{n1}} \cdot V_{dsy}^2 \tag{7}$$

Next, by applying KVL in the loop formed by the transistors M_{na}, M_{nb} and M_{ny}.

$$V_{gsa} = V_{gsb} + V_{dsy} \tag{8}$$

Here the transistors M_{na} and M_{nb} are operating in sub-threshold saturation region and M_{ny} is working in the linear region. Hence, re-writing (8) by using [20] as follows:

$$V_{thn} + \eta V_T ln\left(\frac{I_{ref}}{S_a I_o}\right) = V_{thn} + \eta V_T ln\left(\frac{I_{ref}}{S_a I_o}\right) + V_{dsy} \tag{9}$$

where η is the sub-threshold slope, V_T is the thermal voltage, I_o is the saturation current, S_a and S_b are the aspect ratio (W/L) of transistors M_{na} and M_{nb} respectively. Solving (9) for V_{dsy} will result in

$$V_{dsy} = \eta V_T^2 ln\left(\frac{S_a}{S_b}\right) \tag{10}$$

The Eq. (10) shows that V_{dsy} is a function of the thermal voltage V_T. Hence, V_{dsy} increases with increasing temperature (T) as shown in Fig. 3. It can be observed from (10) and (7) that to obtain the value of I_{ref} in the nanoampere range, either decrease the value of S_y or decrease the value of V_{dsy}. The use of minimum device dimensions is one of constraints hence, in these implementations, the cascode arrangement

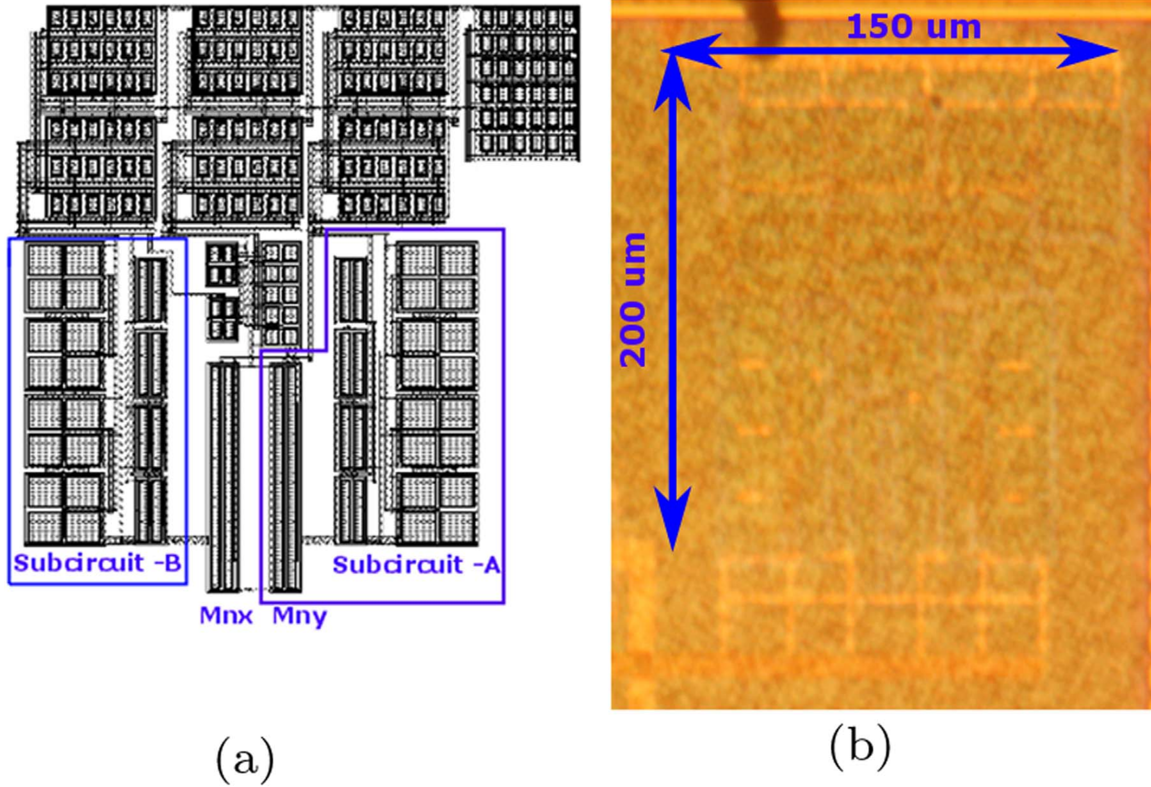

Fig. 9. (a) Layout and (b) Micrograph of the proposed current reference circuit.

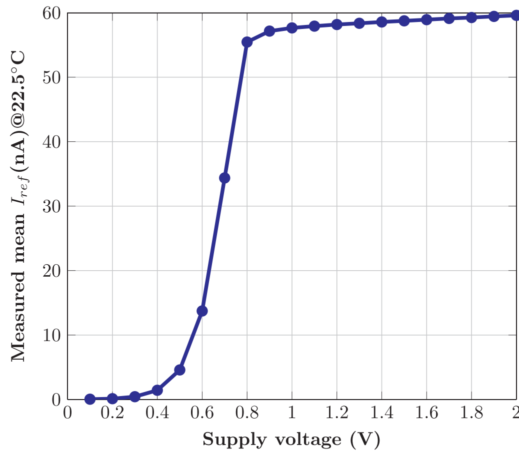

Fig. 10. Measured mean reference current I_{ref} at 22.5 °C across different supply voltages.

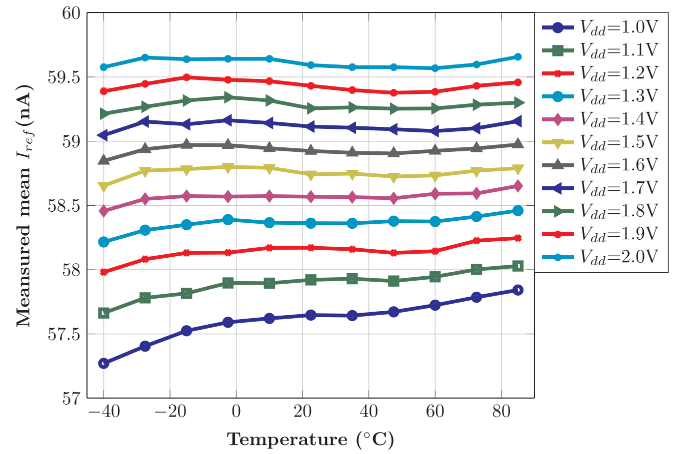

Fig. 11. Measured thermal performance of the mean reference current I_{ref} for different supply voltages.

has been used (See Figs. 2 and 4) to avoid any change in a standard ratio of M_{nb} and M_{na} aspect ratio. Thus, the solution for obtaining a nanoampere current value in the existing circuit (Fig. 2) is to decrease the value of S_y *i.e.*, increase the channel length of nMOSFET M_{ny}.

The device dimensions that have been used to achieve the targeted current of value 45 nA@22.5° in the redesigned RBM circuit (See Fig. 2) are listed in Table 1. It can be observed that transistors with exceptionally long channel lengths are required to achieve the current value in nanoampere region. This design constraint has also been reported in [12].

As a solution to this design issue, consider the conceptual circuit diagram shown in Fig. 6. In the circuit, a provision for the use of an additional voltage source V_x in the loop formed by M_{na}, M_{nb} and M_{ny} has been proposed. Here, the transistors M_{na} and M_{nb} are set to operate in the saturation region which is in-contrast to the conventional implementation. To understand the constraint, consider that M_{na} and M_{nb} are working in a sub-threshold region *i.e.* the conventional approach. Applying KVL in the loop formed by M_{na}, M_{nb}, M_{ny} and V_x:

$$V_{gsa} + V_x = V_{gsb} + V_{dsy} \tag{11}$$

Rewriting (11) by using [20] will result in:

$$V_x - V_{dsy} = \eta V_T ln\left(\frac{S_a}{S_b}\right) \tag{12}$$

Some of the following conclusions can be obtained from (12):

1. The difference of the voltages V_x and V_{dsy} has became the function of device dimension of the transistors M_{na} and M_{nb}. This prevents the symmetrical implementation *i.e.* selection of same device dimensions in the circuit and therefore the PVT sensitivity will increase [21].

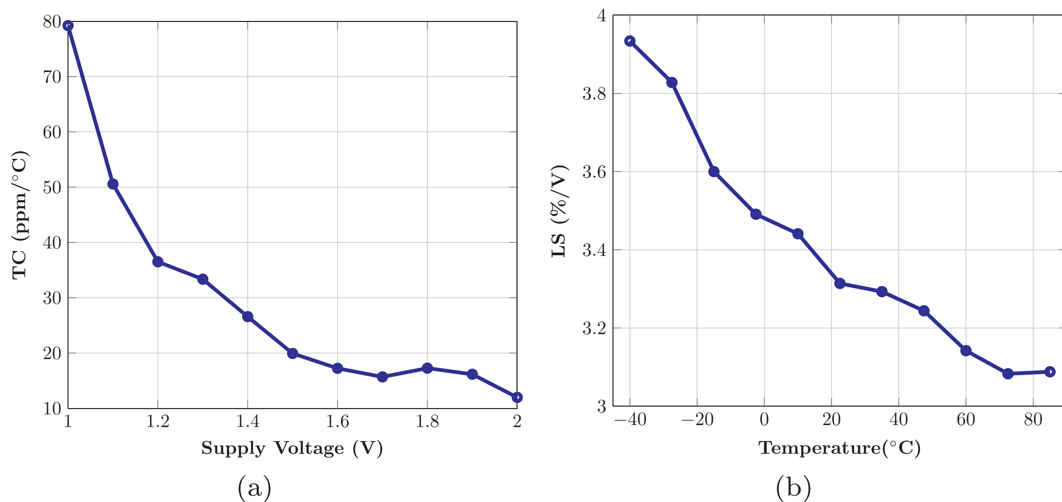

Fig. 12. (a) Measured mean TC at different supply voltages and (b) Measured mean LS at different temperatures.

Fig. 13. Measured D2D statistical distributions of proposed current reference circuit.

Table 3
Summary of statistical distribution obtained from ten prototypes.

Parameter	Avg(μ)	Std. Dev.(σ)	Spread(%) (σ/μ)
I_{ref}	58.69	0.632	1.07
TC	29.375	19.66	67%
LS	3.4	0.276	8.12%

2. It is evident from the equation that thermal slope of V_x and V_{dsy} is different. Hence, to obtain the temperature independence additional thermal compensation method would be required like diode referenced self biasing [20,22].
3. Finally, a direct dependency of the reference current I_{ref} over V_x and V_{dsy} is absent therefore the use of these parameters to control the current value further up to a nano-ampere range is limited.

Thus based on the above observations the transistors M_{na} and M_{nb} have been set to operate in the saturation region. This implementation practice is widely in use and reported in literature [23]. Thus rewriting (11) for the saturation region and solving for I_{ref} will be resulted into:

Applying KVL in the loop and solving for I_{ref} will result in:

$$I_{ref} = \frac{\mu_n C_{ox}}{2}\left(\frac{\sqrt{S_a S_b}}{\sqrt{S_b} - \sqrt{S_a}}\right)^2 (V_{dsy} - V_x)^2 \tag{13}$$

It can be observed from (13) that due to the presence of V_x, the influence of V_{dsy} over the value of I_{ref} reduces. Hence, it becomes possible to achieve a nano-ampere current with a moderate device sizing, when compared with the conventional RBM circuit.

Differentiating (13) with respect to temperature T results in:

$$\frac{dI_{ref}}{dT} = \frac{C_{ox}}{2}\left(\frac{\sqrt{S_a S_b}}{\sqrt{S_b} - \sqrt{S_a}}\right)^2 \left[\underbrace{(V_{dsy}(T) - V_x(T))^2}_{d} \cdot \frac{d\mu_n}{dT} - 2(V_{dsy}(T) - V_x(T))\left(\underbrace{\frac{dV_{dsy}}{dT} - \frac{dV_x}{dT}}_{f}\right)\cdot \mu_n\right] \tag{14}$$

The conditions to obtain a temperature independent current are marked in (14). According to that, if the magnitude and thermal slope of V_{dsy} and V_x are equal (terms(d,f)) then the thermal effects over the current I_{ref} will become minimum.

In order to obtain the equal magnitude V_{dsy} and V_x (term (d)) and hence, to obtain similar thermal slope (term(f)), a simple strategy of replicating the subcircuit-A as shown in Fig. 4 has been proposed. The arrangement is marked as Subcircuit-B in the figure and V_x has been realized using nMOSFET M_{nx} operating in the linear region.

The simulation results of the reference current obtained from the redesigned RBM (Fig. 2) and the proposed circuit (Fig. 4) at supply voltage of 1.25 V are shown in Fig. 7. In the results, the current obtained from the conventional circuit exhibits PTAT behavior with Temperature Coefficient (TC) of value 270 ppm/ °C [12]. On the other hand in the proposed circuit, the targeted reference current with the TC of value 48 ppm/°C has been obtained. The low value of TC shows that the proposed circuit techniques to obtain the thermal compensation in the current are working as predicted using the first order mathematical expressions. The device sizing used in these implementations are listed in Table 1 where, it can be seen in the remark column that the sizing of the transistors which are critical for obtaining the current in nanoampere range have been reduced by more than 90% when compared with the redesigned RBM and the conventional RBM circuits. However, the power dissipation has been doubled due to the inclusion of additional three branches in the circuit with same current values.

It should be noted that it is possible to reduce the power dissipation by selecting the current values lesser than I_{ref} in the sub circuits A, B. However, this strategy was not opted in the present implementation to maintain the symmetry with the conventional RBM circuit.

To confirm the working of the proposed arrangement, a total 1400 post layout Monte Carlo simulations were performed using the Spectre simulator in the Cadence environment. These simulations include variations in the supply voltage values in the range of 1–2 V for the temperature values in the range of −40 °C to 85 °C across various process corners. The distribution plots obtained are shown in Fig. 8 in terms of the reference current, temperature coefficient and line sensitivity. A brief summary of the results is also listed in Table 2.

3. Measurement results

The proposed current reference is implemented in a standard 180 nm CMOS process. The transistors used in the implementation are selected from the standard library and the body terminals of pMOSFET and nMOSFET are connected to the supply and ground terminals respectively. The layout and micrograph of the proposed circuit are shown in Fig. 9 where the core area is 200 µm × 150 µm.

The temperature characterizations of the prototypes were done in the temperature chamber VTM 7004 for the temperature range of −40 °C to +85 °C in the steps of 12.5 °C. A calibrated precision Pt-100 thermometer (± 0.015 °C) was placed close to the prototype to obtain the true ambient temperature.

The measurements were performed on ten prototypes. The measured mean value of the reference current at room temperature (22.5 °C) for the supply voltage ranging from 0.1 to 2 V is given in Fig. 10. It can be observed from the results that the proposed circuit has started working from 0.8 V. However, to be used as a reference current generator with a TC value less than 100 ppm/°C, the working supply voltage should be selected from 1 V to 2 V. The deviation in the mean reference current value over this supply voltage range is 4.22 nA which, corresponds to the measured mean line sensitivity of 3.3%/V at 22.5 °C. A poor line sensitivity is a result of deviation in the voltage value of V_{gsa} with change in V_{gsb} and V_{dsy} (See equation (??). This phenomenon of a high line sensitivity in the architectures based on resistor-less RBM circuit has been also reported in [12,24,14]. One of the solutions to improve the performance against supply voltage variations is to use a voltage regulation circuit based implementation, as mentioned in [6].

The thermal performance of the mean reference current in the

Table 4
Performance comparison with the-state-of-the-art current reference circuits.

Parameter	This work	[12]	[13]	[25]	[26]	[27]
Process (nm)	180	2000	350	350	350	180
Supply voltage (V)	1 to 2	>2	1.8 to 3	>1.3	5	–
Temperature°C	−40 to 85	−60 to 80	0 to 80	−20 to 80	0 to 80	0 to 110
I_{ref} (nA)	58.7	1–100	96	9.95	50	6.64
TC(ppm/(°C)	30	–	520	1190	128	283
LS(%/V)	3.4	10	0.2	0.46	150	1.16
Power Dissipation (nW)	352 @ 1 V	–	1000@1.8	88.53@1.3	5700@5	9.3
Area (mm^2)	0.036	0.006	0.015	0.12	0.005824	0.055

temperature range of − 40° C to + 85 °C for various supply voltages, are shown in Fig. 11. It can be seen that the measured thermal performance matches with the simulation result shown in Fig. 7. However, the measured current is approximately 30% higher than the selected target specification of the reference current(45 nA@22.5 ˚C). The performance characterizations of reference current have been done in terms of the Temperature Coefficient (TC) and Line Sensitivity (LS) which are shown in Fig. 12.

Ten samples of the proposed current reference circuit were measured. The Device to Device (D2D) variations in terms of the reference current (I_{ref}), temperature coefficient(TC) and line sensitivity (LS) are shown in Fig. 13 and the summary is listed in Table 3. The performance comparison of the proposed current reference circuit with the state-of-the-art current reference circuits available in the literature is presented in Table 4.

4. Conclusion

In this work, a low power, all-MOSFET based nano ampere current reference circuit designed and fabricated in a standard 180 nm CMOS technology has been presented. The proposed circuit is based on the conventional resistor-less beta multiplier circuit. The device generates a supply and temperature compensated output current of value 59 nA in the operating supply voltage range of 1–2 V. The operation of the circuit has been demonstrated by using measurements. The measured result show that the circuit consumes power in nanowatt range, which, enables the use of the proposed architecture in LSI devices used for IoT application.

Acknowledgment

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