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# 3

# Bipolar Technology




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## 3.1 Introduction

The development of a bipolar technology for integrated circuits goes hand in hand with the steady improvement in semiconductor materials and discrete components during the 1950s and 1960s. Consequently, silicon bipolar technology formed the basis for the IC market during the 1970s. As circuit dimensions shrink, the MOSFET (or MOS) has gradually taken over as the major technological platform for silicon integrated circuits. The main reasons are the ease of miniaturization and high yield for MOS compared to bipolar technology. However, during the same period of MOS growth, much progress was simultaneously achieved in bipolar technology.[1,2] This is illustrated in Fig. 3.1 where the reported gate delay time for emitter-coupled logic (ECL) is plotted versus year. [2,3] In 1984, the 100 ps/gate limit was broken and, since then, the speed performance has been improved by a factor of ten. The high speed and large versatility of the silicon bipolar transistor still make it an attractive choice for a variety of digital and analog applications.[4]

Apart from high-speed performance, the bipolar transistor is recognized by its excellent analog properties. It features high linearity, superior low- and high-frequency noise behavior, and a very large transconductance.[5] Such properties are highly desirable for many RF applications, both for narrow-band as well as broad-band circuits.[6] The high current drive capability per unit silicon area makes the bipolar transistor suitable for input/output stages in many IC designs (e.g., in fast SRAMs). The disadvantage of bipolar technology is the low transistor density, combined with a large power dissipation. High-performance bipolar circuits are therefore normally fabricated at a modest integration level (MSI/LSI). By using BiCMOS design, the benefits of both MOS and bipolar technology are utilized.[7] One example is mixed analog/digital systems where a high-performance bipolar process is integrated with high-density CMOS. This technology forms a vital part in several system-on-a-chip designs (e.g., for telecommunication circuits).

In this chapter, a brief overview of bipolar technology is given with an emphasis on the integrated silicon bipolar transistor. The information presented here is based on the assumption that the reader is

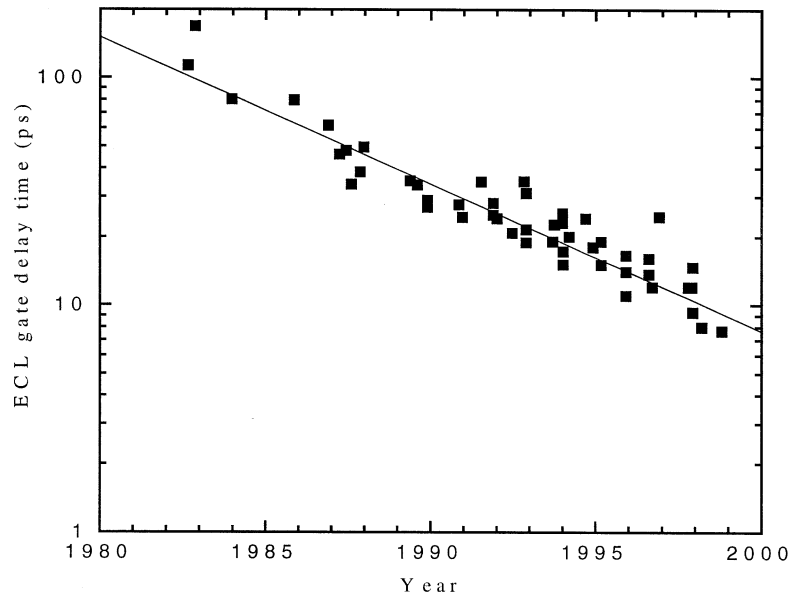


**FIGURE 3.1** Reported gate delay time for bipolar ECL circuits vs. year.

familiar with bipolar device fundamentals and basic VLSI process technology. Bipolar transistors are treated in detail in the well-known textbooks by Ashburn[8] and Roulston.[9] The first part of this chapter will outline the general concepts in bipolar process design and optimization (Section 3.2). The second part will present the three generations of integrated devices representing state-of-the-art bipolar technologies for the 1970s, 1980s, and 1990s (Sections 3.3, 3.4, and 3.5, respectively). Finally, some future trends in bipolar technology are outlined.

## 3.2 Bipolar Process Design

The design of a bipolar process starts with the specification of the application target and its circuit technology (digital or analog). This leads to a number of requirements formulated in device parameters and associated figures-of-merit. These are mutually dependent and must therefore be traded off against each other, making the final bipolar process design a compromise between various conflicting device requirements.

### Figures-of-Merit

In the digital bipolar process, the cutoff frequency ($f_T$) is a well-known figure-of-merit for speed. The $f_T$ is defined for a common-emitter configuration with its output short-circuit when extrapolating the small signal current gain to unity. From a circuit perspective, a more adequate figure-of-merit is the gate delay time ($\tau_d$) measured for a ring-oscillator circuit containing an odd number of inverters.[10] The $\tau_d$ can be expressed as a linear combination of the incoming time constants weighted by a factor determined by the circuit topology (e.g., ECL)[10,11] Alternative expressions for $\tau_d$ calculations have been proposed.[12] Besides speed, power dissipation can also be a critical issue in densely packed bipolar digital circuits, resulting in the power-delay product as a figure-of-merit.[4]

In the analog bipolar process, the dc properties of the transistor are of utmost importance. This involves minimum values on common-emitter current gain ($\beta$), Gummel plot linearity ($\beta_{max}/\beta$) breakdown voltage ($BV_{CEO}$), and Early voltage ($V_A$). The product $\beta \times V_A$ is often introduced as a figure-of-merit for the device

dc characteristics.[13] Rather than $f_T$, the maximum oscillation frequency, $f_{max} = \sqrt{f_T/(8\pi R_B C_{BC})}$ is preferred as a figure-of-merit in high-speed analog design, where $R_B$ and $C_{BC}$ denote the total base resistance and the base-collector capacitance, respectively.[14] Alternative figures-of-merit for speed have been proposed in the literature.[15,16] Analog bipolar circuits are often crucially dependent on a certain noise immunity, leading to the introduction of the corner frequency and noise figure as figures-of-merit for low-frequency and high-frequency noise properties, respectively.[17]

## Process Optimization

The optimization of the bipolar process is divided between the intrinsic and extrinsic device design. This corresponds to the vertical impurity profile and the horizontal layout of the transistor, respectively.[10] See example in Fig. 3.2, where the device cross-section is also included. It is clear that the vertical profile and horizontal layout are primarily dictated by the given process and lithography constraints, respectively.

Figure 3.3 shows a simple flowchart of the bipolar design procedure. Starting from the specified dc parameters at a given operation point, the doping profiles can be derived. The horizontal layout must be adjusted for minimization of the parasitics. A (speed) figure-of-merit can then be calculated. An implicit relation is thus obtained between the figure-of-merit and the processing parameters.[11,18] In practice, several iterations must be performed in the optimization loop in order to find an acceptable compromise between the device parameters. This procedure is substantially alleviated by two-dimensional process simulations of the device fabrication[19] as well as device simulations of the bipolar transistor.[20,21] For optimization of a large number of device parameters, the strategy is based on screening out the unimportant factors, combined with a statistical approach (e.g., response surface methodology.)[22]

## Vertical Structure

The engineering of the vertical structure involves the design of the collector, base, and emitter impurity profiles. In this respect, $f_T$ is an adequate parameter to optimize. For a modern bipolar transistor with suppressed parasitics, the maximum $f_T$ is usually determined by the forward transit time of minority carriers through the intrinsic component. The most important $f_T$ tradeoff is against $BV_{CEO}$, as stated by the Johnson limit for silicon transistors:[23] the product $f_T \times BV_{CEO}$ cannot exceed 200 GHz-V (recently updated to 500 GHz-V).[24]

### Collector Region

The vertical n-type collector of the bipolar device in Fig. 3.2 consists of two regions below the p-type base diffusion: a lowly or moderately doped n-type epitaxial (epi) layer, followed by a highly doped $n^+$-subcollector. The thickness and doping level of the subcollector are non-critical parameters; a high arsenic or antimony doping density between $10^{19}$ and $10^{20}$ $cm^{-3}$ is representative, resulting in a sheet resistance of 20 to 40 Ω/sq. In contrast, the design of the epi-layer constitutes a fundamental topic in bipolar process optimization.

To first order, the collector doping in the epi-layer is determined by the operation point (more specifically, the collector current density) of the component (see Fig. 3.3). A normal condition is to have the operation point corresponding to maximum $f_T$, which typically means a collector current density on the order of $2–4 \times 10^4$ $A/cm^2$. As will be recognized later, bipolar scaling results in increased collector current densities. Above a certain current, there will be a rapid roll-off in current gain as well as cutoff frequency. This is due to high-current effects, primarily the base push-out or Kirk effect, leading to a steep increase in the forward transit time.[25] Since the critical current value is proportional to the collector doping,[26] a minimum impurity concentration for the epi-layer is required, thus avoiding $f_T$ degradation (typically around $10^{17}$ $cm^{-3}$ for a high-speed device). Usually, the epi-layer is doped only in the intrinsic structure by a selectively implanted collector (SIC) procedure.[27] An example of such a doping profile is seen in Fig. 3.4. Such a collector design permits an improved control over the base-collector junction; that is, shorter base width as well as suppressed Kirk effect. The high collector doping concentration,

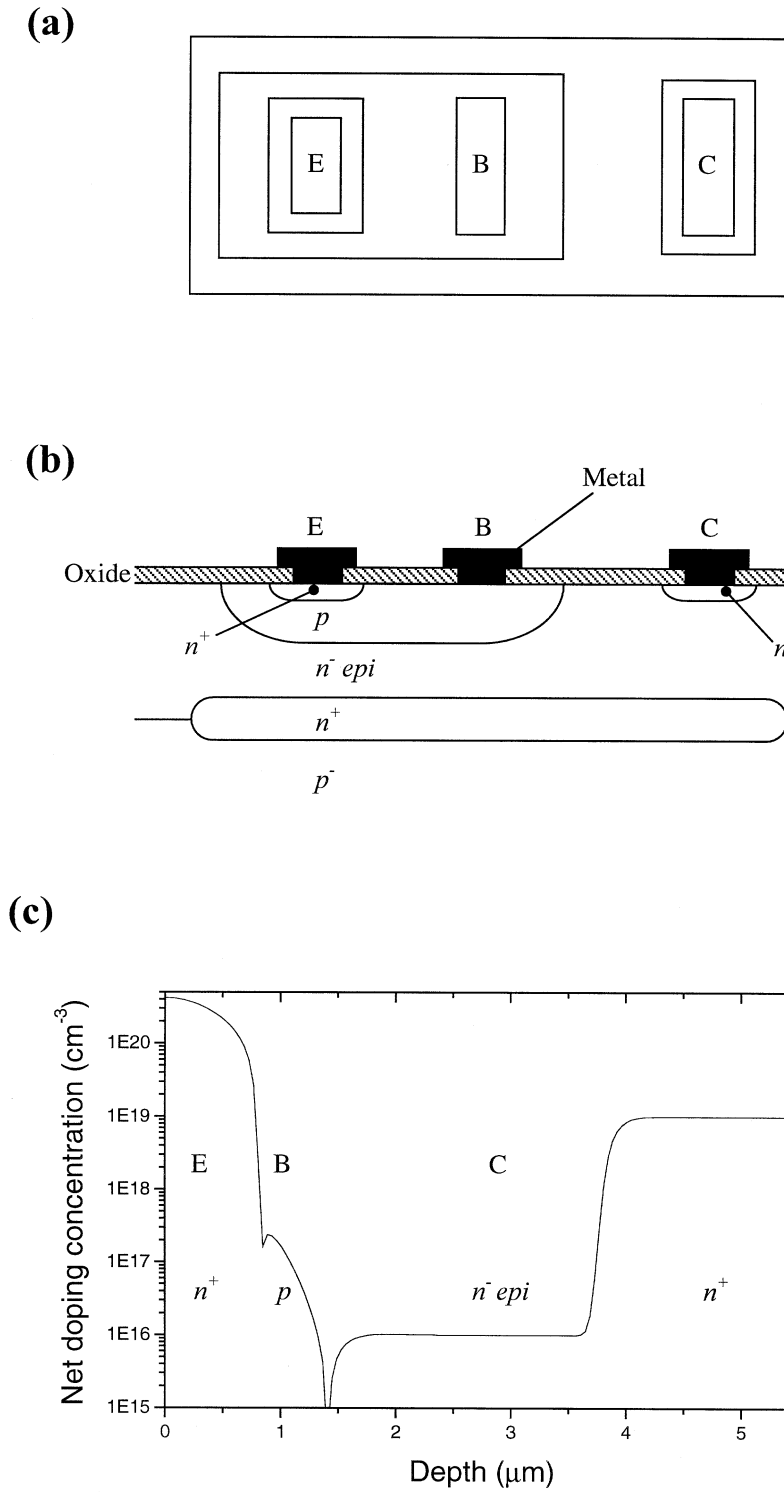


**FIGURE 3.2** (a) Layout, (b) cross-section, and (c) simulated impurity profile through emitter window for an integrated bipolar transistor (E = emitter, B = base, C = collector).

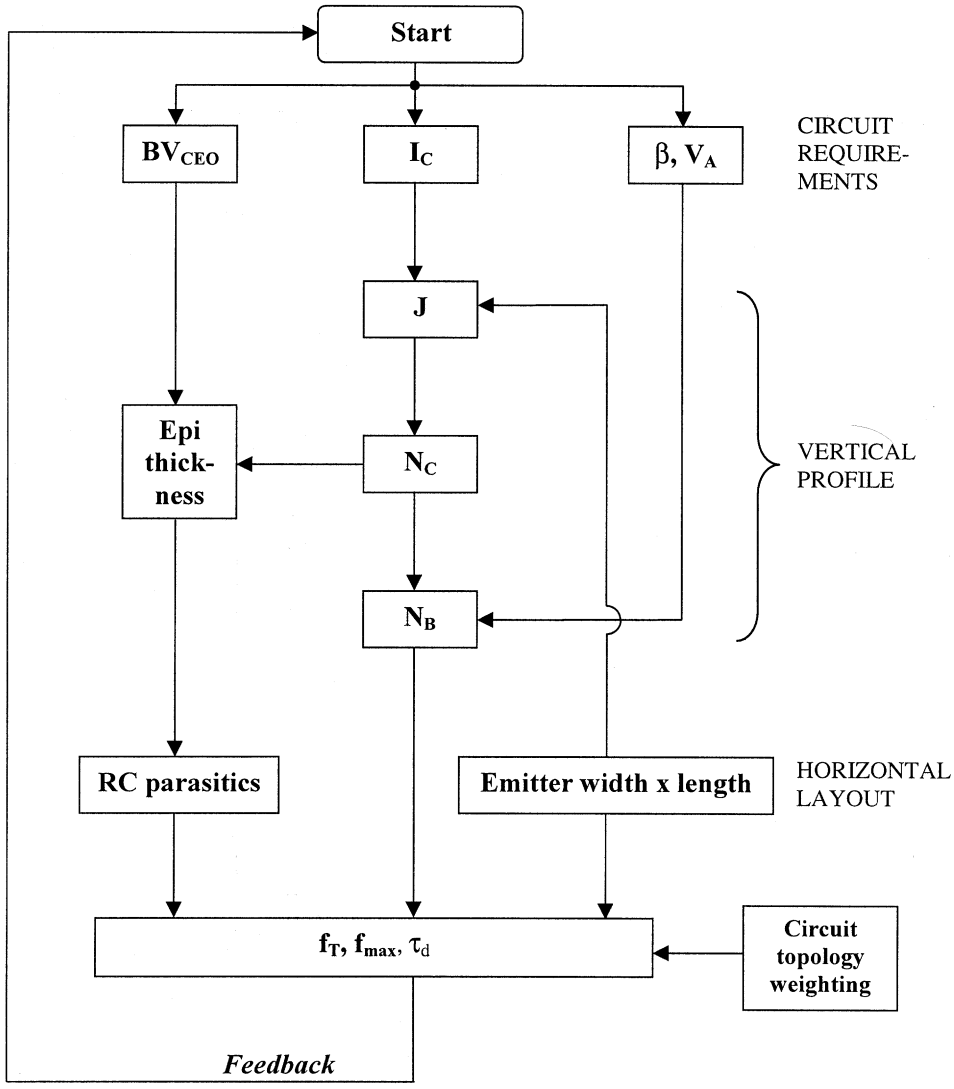


**FIGURE 3.3** Generic bipolar device optimization flowchart.

however, may be a concern for both $C_{BC}$ and $BV_{CEO}$. The latter value will therefore often set a higher limit on the collector doping value. One way to reduce the electrical field in the junction is to implement a lightly doped collector spacer layer between the heavily doped base and collector regions.[28,29] A retrograde collector profile with a low impurity concentration near the base-collector junction and then increasing toward the subcollector has also been reported to enhance $f_T$.[30,31]

The thickness of the epi-layer exhibits large variations between different device designs, extending several micrometers in depth for analog bipolar components, whereas a high-speed digital design typically has an epi-layer thickness around 1 μm or below, thus reducing total collector resistance. As a result, the transistor breakdown voltage is sometimes determined by reach-through breakdown (i.e., full depletion penetration of the epi-collector). The thickness of the collector layer can therefore be used as a parameter in determining $BV_{CEO}$, which in turn is traded off vs. $f_T$.[32]

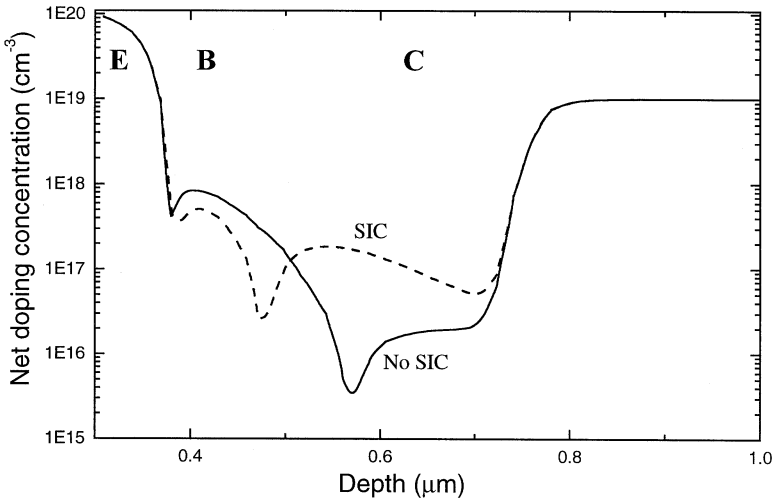


**FIGURE 3.4** Simulated vertical impurity profile with and without SIC.

In cases where $f_{max}$ is of interest, the collector design must be carefully taken into account. Compared to $f_T$, the optimum $f_{max}$ is found for thicker and lower doped collector epi-layers.[33,34] The vertical collector design will therefore, to a large extent, determine the tradeoff between $f_T$ and $f_{max}$.

## Base Region

The width and peak concentration of the base profile are two of the most fundamental parameters in vertical profile design. The base width $W_B$ is normally in the range 0.1 to 1 μm, whereas a typical base peak concentration lies between $10^{17}$ and $10^{18}$ cm$^{-3}$. The current gain of the transistor is determined by the ratio of the Gummel number in the emitter and base. Usually, a current gain of at least 100 is required for analog bipolar transistors, whereas in digital applications, $\beta$ around 20 is often acceptable. A normal base sheet resistance (or pinch resistance) for conventional bipolar processes is of the order of 100 Ω/sq., whereas the number for high-speed devices typically is in the interval 1 to 10 kΩ/sq. This is due to the small $W_B < 0.1$ μm necessary for a short base transit time ( $\propto W_B^2$ ). On the other hand, a too narrow base will have a negative impact on $f_{max}$ because of its $R_B$ dependence. As a result, $f_{max}$ exhibits a maximum when plotted against $W_B$.[35]

The base impurity concentration must be kept high enough to avoid punch-through at low collector voltages; that is, the base-collector depletion layer penetrates across the neutral base. In other words, the base doping level is also dictated by the collector impurity concentration. Punch-through is the ultimate consequence of base width modulation or the Early effect manifested by a finite output resistance in the $I_C$-$V_{CE}$ transistor characteristic.[36] The associated $V_A$ or the product $\beta \times V_A$ serves as an indicator of the linear properties for the bipolar transistor. The $V_A$ is typically at a relatively high level (>30 V) for analog applications, whereas digital designs often accept relatively low $V_A < 15$ V.

Figure 3.5 demonstrates simulations of current gain versus the base doping for various $W_B$.[37] It is clearly seen that the base doping interval permitting a high current gain while avoiding punch-through will be pushed to high impurity concentrations for narrow base widths. In addition, Fig. 3.5 points to another limiting factor for high base doping numbers above $5 \times 10^{18}$ cm$^{-3}$, namely, the onset of forward-biased tunneling currents in the emitter-base junction[38] leading to non-ideal base current characteristics.[39] It is concluded that the allowable base doping interval will be very narrow for $W_B < 0.1$ μm.

The shape of the base profile has some influence over the device performance. The final base profile is the result of an implantation and diffusion process and, normally, only the peak base concentration is given along with the base width. Nonetheless, there will be an impurity grading along the base profile (see Figs. 3.2 and 3.4), creating a built-in electrical field and thereby adding a drift component for the

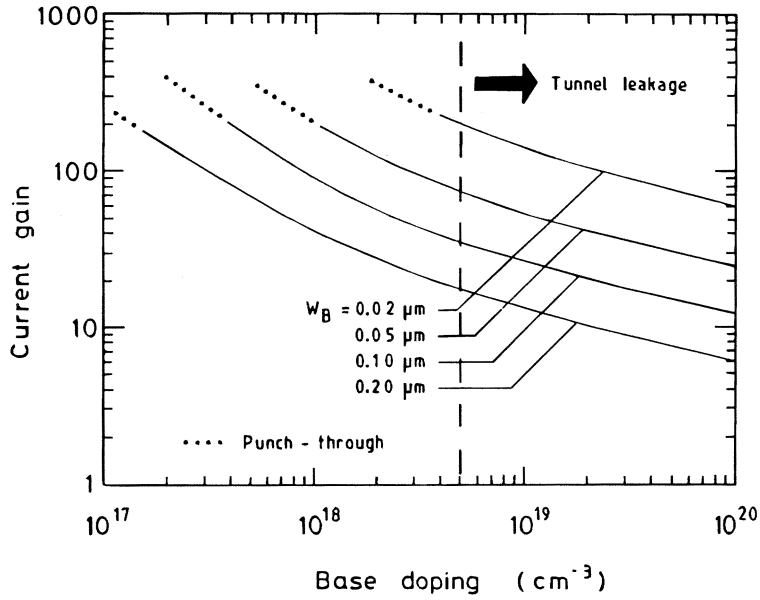


**FIGURE 3.5** Simulated current gain vs. base doping density for different base widths ($N_C = 6 \times 10^{16}$ cm$^{-3}$, $N_E = 10^{20}$ cm$^{-3}$, and emitter depth 0.20 μm) (after Ref. 37, copyright© 1990, IEEE).

minority carrier transport.[40] Recent research has shown that for very narrow base transistors, the uniform doping profile is preferable when maximizing $f_T$.[41,42] This is also valid under high injection conditions in the base.[43] Uniformly doped base profiles are common in advanced bipolar processes using epitaxial techniques for growing the intrinsic base.

During recent years, base profile design has largely been devoted to implementation of narrow bandgap SiGe in the base. The resulting emitter-base heterojunction allows a considerable enhancement in current gain, which can be traded off against increased base doping, thus substantially alleviating the problem with elevated base sheet resistances typical of high-speed devices.[44] Excellent dc as well as high-frequency properties can be achieved. The position of the Ge profile with respect to the boron profile has been discussed extensively in the literature.[45–47] More details about SiGe heterojunction engineering are found in Chapter 5 by Cressler.

### Emitter Region

The conventional metal-contacted emitter is characterized by an abrupt arsenic or phosphorus profile fabricated by direct diffusion or implantation into the base area (see Fig. 3.2).[48] In keeping emitter efficiency close to unity (and thus high current gain), the emitter junction cannot be made too shallow (~1 μm). The emitter doping level lies typically between $10^{20}$ and $10^{21}$ cm$^{-3}$ close to the solid solubility limit at the silicon surface, hence providing a low emitter resistance as well as a large emitter Gummel number required for keeping current gain high. Bandgap narrowing, however, will be present in the emitter, causing a reduction in the efficient emitter doping.[49]

When scaling bipolar devices, the emitter junction must be made more shallow to ensure a low emitter-base capacitance. When the emitter depth becomes less than the minority carrier recombination length, the current gain will inevitably degrade. This precludes the use of conventional emitters in a high-performance bipolar technology. Instead, polycrystalline (poly) silicon emitter technology is utilized. By diffusing impurity species from the polysilicon contact into the monocrystalline (mono) silicon, a very shallow junction (< 0.2 μm) is formed; yet gain can be kept at a high level and even traded off against a higher base doping.[50] A gain enhancement factor between 3 and 30 for the polysilicon compared to the monosilicon emitter has been reported (see also Section 3.4).[51,52]

## Scaling Rules

The principles for vertical design can be summarized in the bipolar scaling rules formulated by Solomon and Tang; [53,54] see Table 3.1. Since the bipolar transistor is scaled under constant voltage, the current density increases with reduced device dimensions. At medium or high current densities, the vertical structure determines the speed. At low current densities, performance is normally limited by device parasitics. Eventually, tunnel currents or contact resistances constitute a final limit to further speed improvement based on the scaling rules. A solution is to use SiGe bandgap engineering to further enhance device performance without scaling.

**TABLE 3.1** Bipolar Scaling Rules (Scaling factor $\lambda < 1$)

| Parameter | Scaling Factor |
|---|---|
| Voltage | 1 |
| Base width $W_B$ | $\lambda^{0.8}$ |
| Base doping $N_B$ | $W_B^{-2}$ |
| Current density J | $\lambda^{-2}$ |
| Collecting doping | J |
| Depletion capacitances | $\lambda$ |
| Delay | $\lambda$ |
| Power | 1 |
| Power-delay product | $\lambda$ |

## Horizontal Layout

The horizontal layout is carried out in order to minimize the device parasitics. Figure 3.6 shows the essential parasitic resistances and capacitances for a schematic bipolar structure containing two base contacts. The various RC constants in Fig. 3.6 introduce time delays. For conventional bipolar transistors, such parasitics often limit device speed. In contrast, the self-alignment technology applied in advanced bipolar transistor fabrication allows for efficient suppression of the parasitics.

In horizontal layout, $f_{max}$ serves as a first-order indicator in the extrinsic optimization procedure because of its dependence on $C_{BC}$ and (total) $R_B$. These two parasitics are strongly connected to the geometrical layout of the device. The more advanced $\tau_d$ calculation takes all major parasitics into account under given load conditions, thus providing good insight into the various time delay contributions of a bipolar logic gate.[55]

From Fig. 3.6, it is seen that the collector resistance is divided into three parts. Apart from the epi-layer and buried layer previously discussed, the collector contact also adds a series resistance. Provided the epi-layer is not too thick, the transistor is equipped with a deep phosphorus plug from the collector contact down to the buried layer, thus reducing the total $R_C$.

As illustrated in Fig. 3.6, the base resistance is divided into intrinsic ($R_{Bi}$) and extrinsic ($R_{Bx}$) components. The former is the pinched base resistance situated directly under the emitter diffusion, whereas the latter constitutes the base regions contacting the intrinsic base. The intrinsic part decreases with the current due to the lateral voltage drop in the base region.[56] At high current densities, this causes current crowding effects at the emitter diffusion edges. This results in a reduced onset for high-current effects in the transistor. The extrinsic base resistance is bias independent and must be kept as small as possible (e.g., by utilizing self-alignment architectures). By designing a device layout with two or more base contacts surrounding the emitter, the final $R_B$ is further reduced at the expense of chip area. Apart from enhancing $f_{max}$, the $R_B$ reduction is also beneficial for device noise performance.

The layout of the emitter is crucial since the effective emitter area defines the intrinsic device cross-section.[57] The minimum emitter area, within the lithography constraints, is determined by the operational collector current and the critical current density where high-current effects start to occur.[58] Eventually, a tradeoff must be made between the base resistance and device capacitances as a function of emitter geometry; this choice is largely dictated by the device application. Long, narrow emitter stripes, meaning

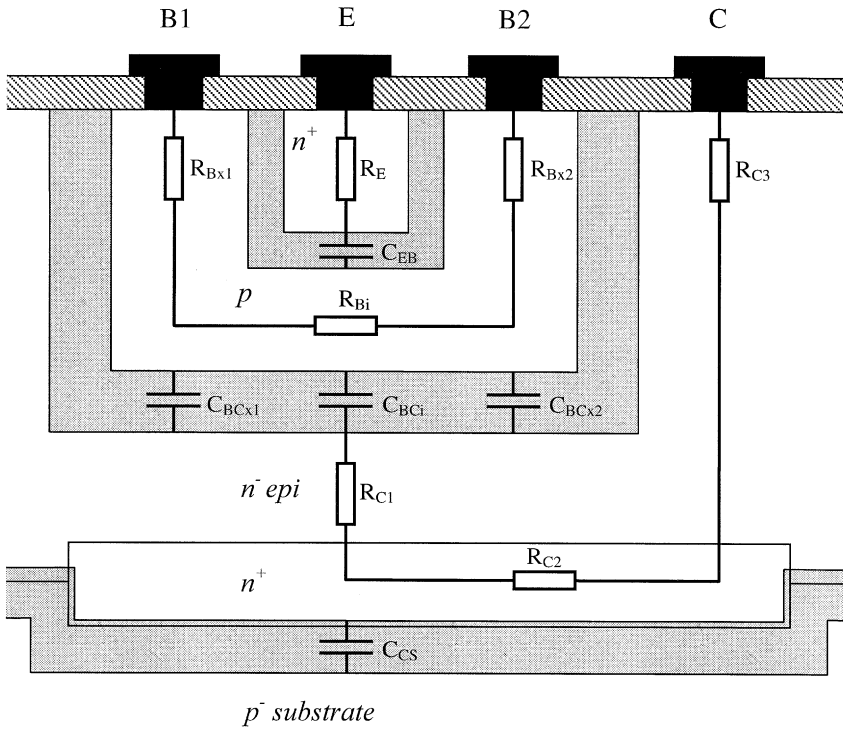


**FIGURE 3.6** Schematic view of the parasitic elements in a bipolar transistor equipped with two base contacts. $R_E$ = emitter resistance, $R_{Bi}$ = intrinsic base resistance, $R_{Bx}$ = extrinsic base resistance, $R_C$ = collector resistance, $C_{EB}$ = emitter-base capacitance, $C_{BCi}$ = intrinsic base-collector capacitance, $C_{BCx}$ = extrinisic base-collector capacitance, and $C_{CS}$ = collector-substrate capacitance. Gray areas denote depletion regions. Contact resistances are not shown.

a reduction in the base resistance, are frequently used. The emitter resistance is usually non-critical for conventional devices; however, for polysilicon emitters, the emitter resistance may become a concern in very small-geometry layouts.[3]

Of the various junction capacitances in Fig. 3.6, the collector-base capacitance is the most significant. This parasitic is also divided into intrinsic ($C_{BCi}$) and extrinsic ($C_{BCx}$) contributions. Similar to $R_{Bx}$, the $C_{BCx}$ is kept low by using self-aligned schemes. For example, the fabrication of a SIC causes an increase only in $C_{BCi}$, whereas $C_{BCx}$ stays virtually unaffected. The collector-substrate capacitance $C_{CS}$ is one of the minor contributors to $f_T$; the $C_{CS}$ originates from the depletion regions created in the epi-layer and under the buried layer. $C_{CS}$ will become significant at very high frequencies due to substrate coupling effects.[59]

## 3.3 Conventional Bipolar Technology

Conventional bipolar technology is based on the device designs developed during the 1960s and 1970s. Despite its age, the basic concept still constitutes a workhorse in many commercial analog processes where ultimate speed and high packing density are not of primary importance. In addition, a conventional bipolar component is often implemented in low-cost BiCMOS processes.

### Junction-Isolated Transistors

The early planar transistor technology took advantage of a reverse-biased pn junction in providing the necessary isolation between components. One of the earliest junction-isolated transistors, the so-called triple-diffused process, is simply based on three ion implantations and subsequent diffusion.[60] This device

has been integrated into a standard CMOS process using one extra masking step.[61] The triple-diffused bipolar process, however, suffers from a large collector resistance due to the absence of a subcollector, and the npn performance will be low.

By far, the most common junction-isolated transistor is represented by the device cross-section of Fig. 3.7, the so-called buried-collector process.[60] This device is based on the concept previously shown in Fig. 3.2 but with the addition of an $n^+$-collector plug and isolation. This is provided by the diffused $p^+$-regions surrounding the transistor. The diffusion of the base and emitter impurities into the epi-layer allows relatively good control of the base width (more details of the fabrication is given in the next section on oxide-isolated transistors).

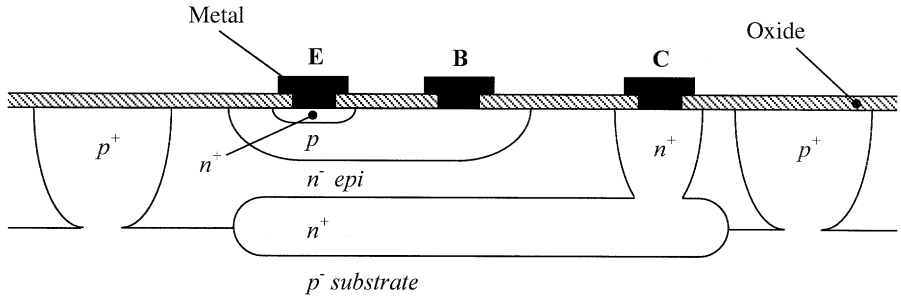


**FIGURE 3.7** Cross-section of the buried-collector transistor with junction isolation and collector plug.

A somewhat different approach of the buried-collector process is the so-called collector-isolation diffusion.[62] This process requires a p-type epi-layer after formation of the subcollector. An $n^+$-diffusion serves both as isolation and the collector plug to the buried layer. After an emitter diffusion, the p-type epi-layer will constitute the base of the final device. Compared to the buried-layer collector process, the collector-isolated device concept does not result in very accurate control over the final base width.

The main disadvantage of the junction-isolated transistor is the relatively large chip area occupied by the isolation region, thus precluding the use of such a device in any VLSI application. Furthermore, high-speed operation is ruled out because of the large parasitic capacitances associated with the junction isolation and the relatively deep diffusions involved. Indeed, many of the conventional junction-isolated processes were designed for doping from the gas phase at high temperatures.

## Oxide-Isolated Transistors

Oxide isolation permits a considerable reduction in the lateral and vertical dimensions of the buried-layer collector process. The reason is that the base and collector contacts can be extended to the edge of the isolation region. More chip area can be saved by having the emitter walled against the oxide edge. The principal difference between scaling of junction-and oxide-isolated transistors is visualized in Fig. 3.8.[63] The device layouts are Schottky clamped; that is, the base contact extends over the collector region. This hinders the transistor to enter saturation mode under device operation. In Fig. 3.8(b), the effective surface area of the emitter contact has been reduced by a so-called washed emitter approach: since the oxide formed on the emitter window during emitter diffusion has a much higher doping concentration than its surroundings, this particular oxide can be removed by a mask-less wet etching. Hence, the emitter contact becomes self-aligned to the emitter diffusion area.

The process flow including mask layouts for an oxide-isolated bipolar transistor of the buried-layer collector type is shown in Fig. 3.9.[64] After formation of the subcollector by arsenic implantation through an oxide mask in the $p^-$-substrate, the upper collector layer is grown epitaxially on top (Fig. 3.9(a)). The device isolation is fabricated by local oxidation of silicon (LOCOS) or recessed oxide (ROX) process

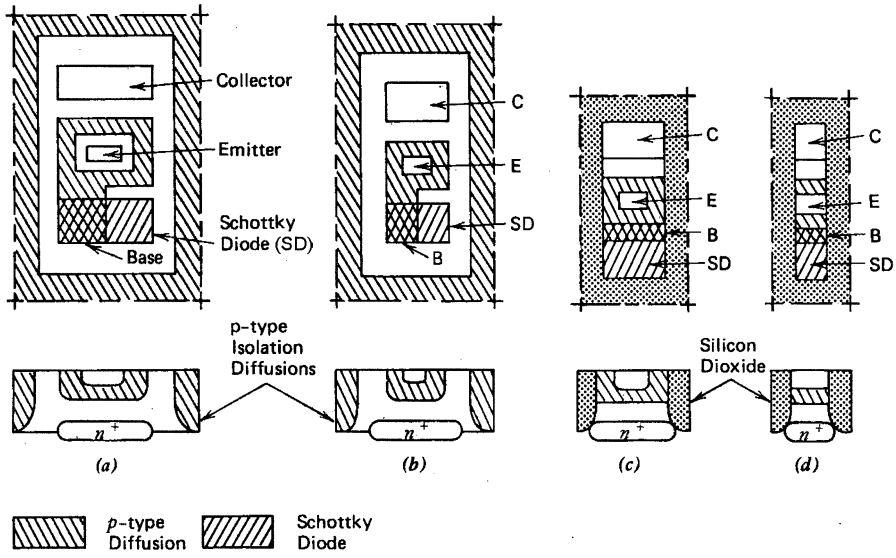


**FIGURE 3.8** Device layout and cross-section demonstrating scaling of (a)-(b) junction-isolated and (c)-(d) oxide-isolated bipolar transistors (after Ref. 63, copyright© 1986, Wiley).

(Figs. 3.9(b) to (d)). The isolation mask in Fig. 3.9(b) is aligned to the buried layer using the step in the silicon (Fig. 3.9(a)) originating from the enhanced oxidation rate for highly doped $n^+$-silicon compared to the $p^-$-substrate during activation of the buried layer. The ROX is thermally grown (Fig. 3.9(d)) after the boron field implantation (or chan-stop) (Fig. 3.9(c)). This $p^+$-implant is necessary for suppressing a conducting channel otherwise present under the ROX. The base is then formed by ion implantation of boron or $BF_2$ through a screen oxide (Fig. 3.9(d)); in the simple device of Fig. 3.9, a single base implantation is used; in a more advanced bipolar process, the fabrication of the intrinsic and extrinsic base must be divided into one low dose and one high dose implantation, respectively, adding one more mask to the total flow. After base formation, an emitter/base contact mask is patterned in a thermally grown oxide (Fig. 3.9(e)). The emitter is then implanted using a heavy dose arsenic implant (Fig. 3.9(f)). An $n^+$ contact is simultaneously formed in the collector window. After annealing, the device is ready for metallization and passivation.

Apart from the strong reduction in isolation capacitances, the replacement of a junction-isolated process with an oxide-isolated process also adds other high-speed features such as thinner epitaxial layer and shallower emitter/base diffusions. A typical base width is a few 1000 Å and the resulting $f_T$ typically lies in the range of 1 to 10 GHz. The doping of the epitaxial layer is determined by the required breakdown voltage. Further speed enhancement of the oxide-isolated transistor is difficult due to the parasitic capacitances and resistances originating from contact areas and design-rule tolerances related to alignment accuracy.

## Lateral pnp Transistors

The conventional npn flow permits the bipolar designer to simultaneously create a lateral pnp transistor. This is made by placing two base diffusions in close proximity to each other in the epi-layer, one of them (pnp-collector) surrounding the other (pnp-emitter) (see Fig. 3.10). In general, the lateral pnp device exhibits poor performance since the base width is determined by lithography constraints rather than vertical base control as in the npn device. In addition, there will be electron injection from the subcollector into the p-type emitter, thus reducing emitter efficiency.

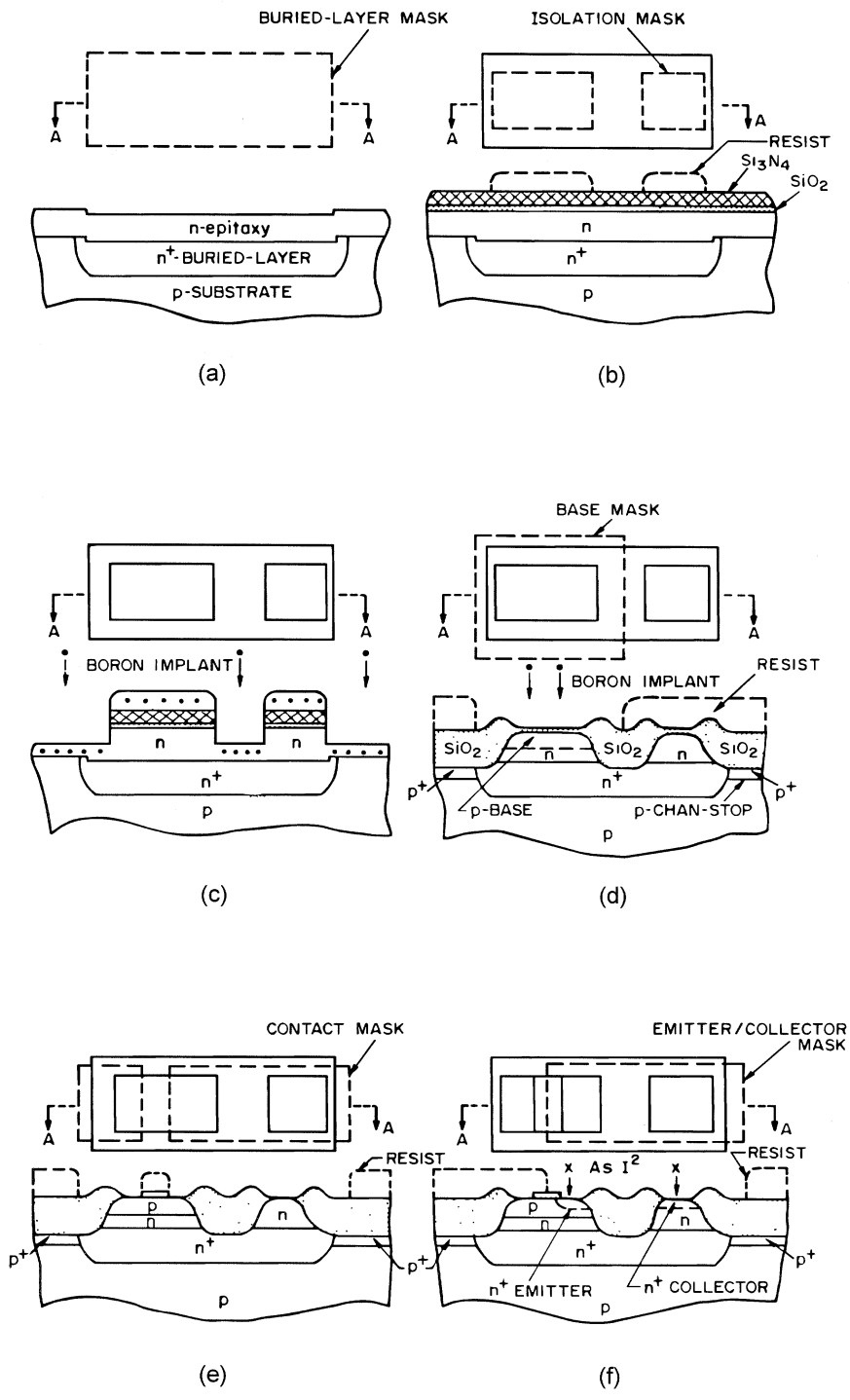


**FIGURE 3.9** Layout and cross-section of the fabrication sequence for an oxide-isolated buried-collector transistor (after Ref. 64, copyright© 1983, McGraw-Hill).

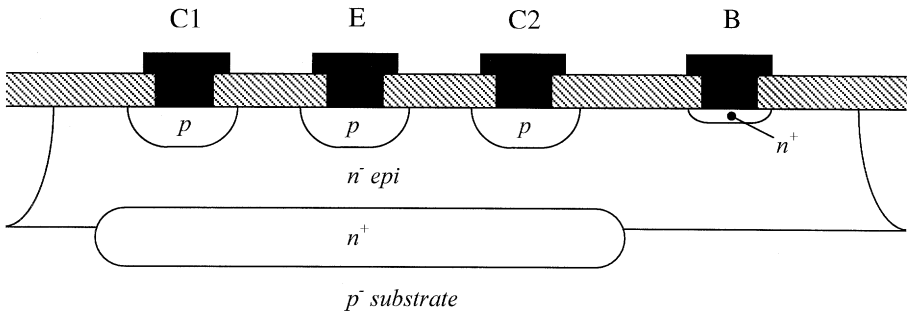


**FIGURE 3.10** Schematic cross-section of the lateral pnp transistor.

## 3.4 High-Performance Bipolar Technology

The development of a high-performance bipolar technology for integrated circuits signified a large step forward, both with respect to speed and packing density of bipolar transistors. A representative device cross-section of a so-called double-poly transistor is depicted in Fig. 3.11. The important characteristics for this bipolar technology are the polysilicon emitter contact, the advanced device isolation, and the self-aligned structure. These three features are discussed here with an emphasis on self-alignment where the two basic process flows are outlined — the single-poly and double-poly transistor.

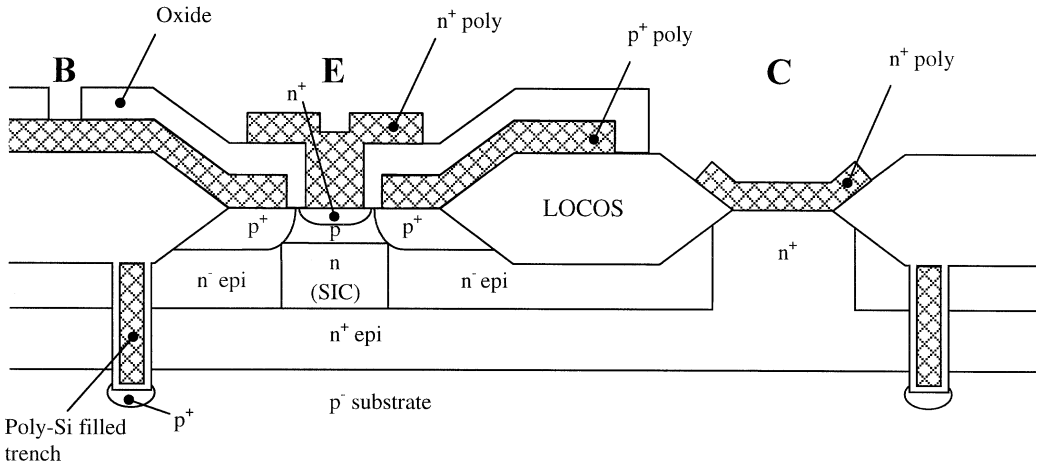


**FIGURE 3.11** A double-poly self-aligned bipolar transistor with deep-trench isolation, polysilicon emitter and SIC. Metallization is not shown.

### Polysilicon Emitter Contact

The polysilicon emitter contact is fabricated by a shallow diffusion of n-type species (usually arsenic) from an implanted $n^+$- polysilicon layer into the silicon substrate[65] (see emitter region in Fig. 3.11). The thin oxide sandwiched between the poly- and monosilicon is partially or fully broken up during contact formation. The mechanism behind the improved current gain is strongly related to the details of the interface between the polysilicon layer and the monosilicon substrate.[52] Hence, the cleaning procedure of the emitter window surface before polysilicon deposition must be carefully engineered for process robustness. Otherwise, the average current gain from wafer-to-wafer will exhibit unacceptable variations.

The emitter window preparation and subsequent drive-in anneal conditions can also be used in tailoring the process with respect to gain and emitter resistance.

From a fabrication point of view, there are further advantages when introducing polysilicon emitter technology. By implanting into the polysilicon rather than into single-crystalline material, the total defect generation as well as related anomalous diffusion effects are strongly suppressed in the internal transistor after the drive-in anneal. Moreover, the risk for spiking of aluminum during the metallization process, causing short-circuiting of the pn junction, is strongly reduced compared to the conventional contact formation. As a result, some of the yield problems associated with monosilicon emitter fabrication are, to a large extent, avoided when utilizing polysilicon emitter technology.

## Advanced Device Isolation

With advanced device isolation, one usually refers to the deep trenches combined with LOCOS or ROX as seen in Fig. 3.11.[66] The starting material before etching is then a double-epitaxial layer ($n^+$-n) grown on a lowly doped $p^-$-substrate. The deep trench must reach all the way through the double epi-layer, meaning a high-aspect ratio reactive-ion etch. Hence, the trenches will define the extension of the buried layer collector for the transistor.

The main reason for introducing advanced isolation in bipolar technology is the need for a compact chip layout.[67] Quite naturally, the bipolar isolation technology has benefited from the trench capacitor development in the MOS memory area. The deep trench isolation allows bipolar transistors to be designed at the packing density of VLSI.

The fabrication of a deep-trench isolation includes deep-silicon etching, chan-stop $p^+$-implantation, an oxide/nitride stack serving as isolation, intrinsic polysilicon fill-up, planarization, and cap oxidation.[66] The deep-trench isolation is combined with an ordinary LOCOS or ROX isolation, which is added before or after trench formation. The most advanced isolation schemes take advantage of shallow-trench isolation rather than ordinary LOCOS after the deep-trench process; in this way, a very planar surface with no oxide lateral encroachment ("birds beak") is achieved after the planarization step. The concern regarding stress-induced crystal defects originating from trench etching requires careful attention so as not to seriously affect yield.

## Self-Aligned Structures

Advanced bipolar transistors are based on self-aligned structures made possible by polysilicon emitter technology. As a result, the emitter-base alignment is not dependent on the overlay accuracy of the lithography tool. The device contacts can be separated without affecting the active device area. It is also possible to create structures where the base is self-aligned both to the collector and emitter, the so-called sidewall-based contact structure (SICOS).[68] This process, however, has not been able to compete successfully with the self-aligned schemes discussed below.

The self-aligned structures are divided into single-polysilicon (single-poly) and double-polysilicon (double-poly) architectures, as visualized in Fig. 3.12.[69] The double-poly structure refers to the emitter polysilicon and base polysilicon electrode, whereas the single-poly only refers to the emitter polysilicon. From Fig. 3.12, it is seen that the double-poly approach benefits from a smaller active area than the single-poly, manifested in a reduced base-collector capacitance. Moreover, the double-poly transistor in general exhibits a lower base resistance. The double-poly transistor, however, is more complex to fabricate than the single-poly device. On the other hand, by applying inside spacer technology for the double-poly emitter structure, the lithography requirements are not as strict as in the single-poly case where more conventional MOS design rules are used for definition of the emitter electrode.

### Single-Poly Structure

The fabrication of a single-poly transistor has been presented in several versions, more or less similar to the traditional MOS flow. An example of a standard single-poly process is shown in Fig. 3.13.[70] After

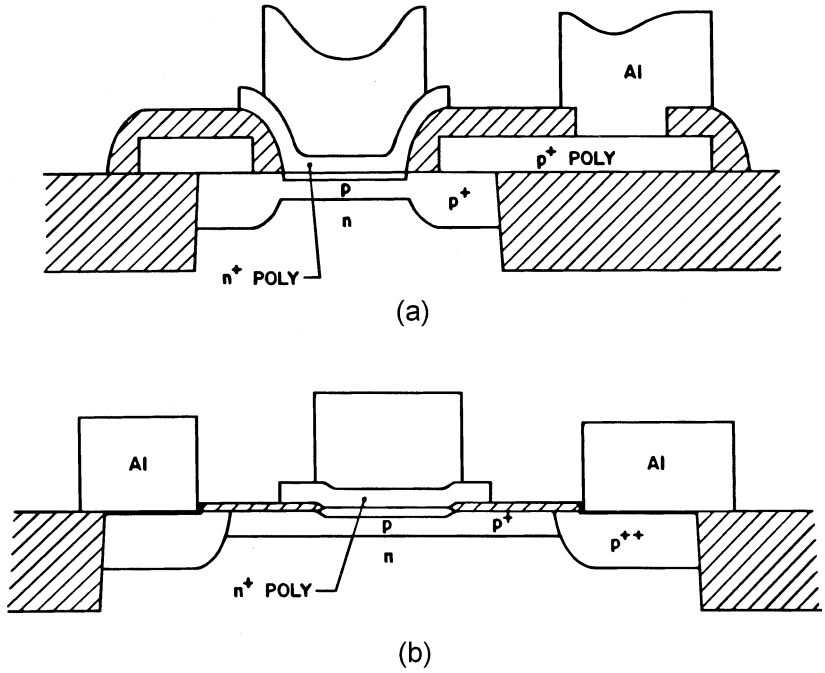


**FIGURE 3.12** (a) Double-poly structure and (b) single-poly structure. Buried layer and collector contact are not shown (after Ref. 69, copyright© 1989, IEEE).

arsenic emitter implantation (Fig. 3.13(a)) and polysilicon patterning, a so-called base-link is implanted using boron ions (Fig. 3.13(b)). Oxide is then deposited and anisotropically etched to form outside spacers, followed by the heavy extrinsic base implantation (Fig. 3.13(c)). Shallow junctions (including emitter diffusion) are formed by rapid thermal annealing (RTA). A salicide or polycide metallization completes the structure (Fig. 3.13(d)).

The intrinsic base does not necessarily need to be formed prior to the extrinsic part. Li et al.[71] have presented a reverse extrinsic-intrinsic base scheme based on a disposable emitter pedestal with spacers. This leads to improved control over the intrinsic base width and a lower surface topography compared to the process represented in Fig. 3.13.

Another variation of the single-poly architecture is the so-called quasi-self-aligned process (see Fig. 3.14).[72] A base oxide is formed by thermal oxidation in the active area and an emitter window is opened (Fig. 13.14(a)). Following intrinsic base implantation, the emitter polysilicon is deposited, implanted, and annealed. The polysilicon emitter pedestal is then etched out (Fig. 3.14(b)). The extrinsic base process, junction formation, and metallization are essentially the same as in the single-poly process shown in Fig. 3.13. Note that in Fig. 13.4, the emitter-base formation is self-aligned to the emitter window in the oxide, not to the emitter itself, hence explaining the term quasi-self-aligned. As a result, a higher total base resistance is obtained compared to the standard single-poly process.

The boron implantation illustrated in Fig. 3.13(b) is an example of so-called base-link engineering aimed at securing the electrical contact between the heavily doped $p^+$-extrinsic base and the much lower doped intrinsic base. Too weak a base link will result in high total base resistance, whereas too strong a base link may create a lateral emitter-base tunnel junction leading to non-ideal base current characteristics.[73] Furthermore, a poorly designed base link jeopardizes matching between individual transistors since the final current gain may vary substantially with the emitter width.

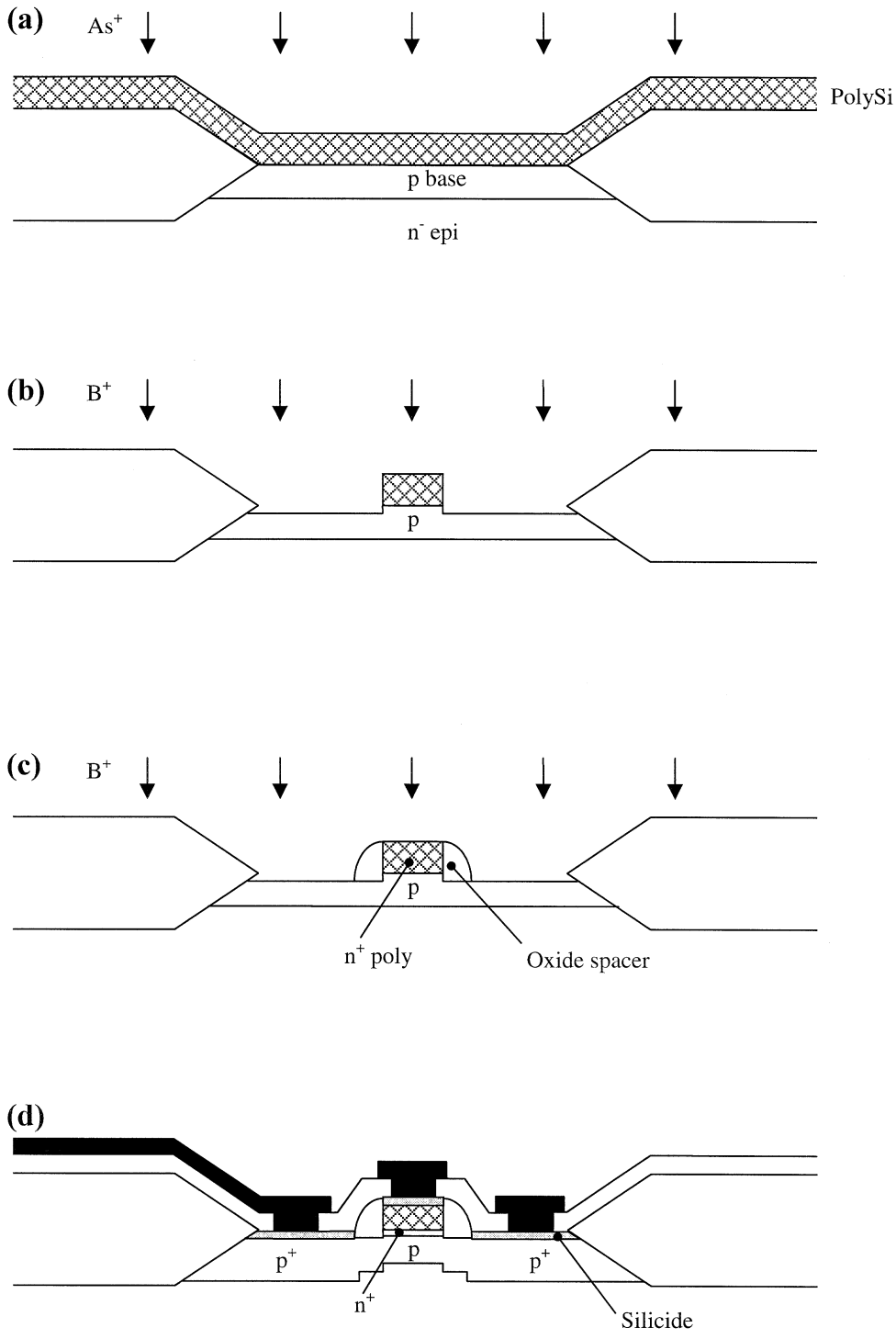


**FIGURE 3.13** The single-poly, self-aligned process: (a) polyemitter implantation, (b) emitter etch and base link implantation, (c) oxide spacer formation and extrinsic base implantation, and (d) final device after junction formation and metallization.

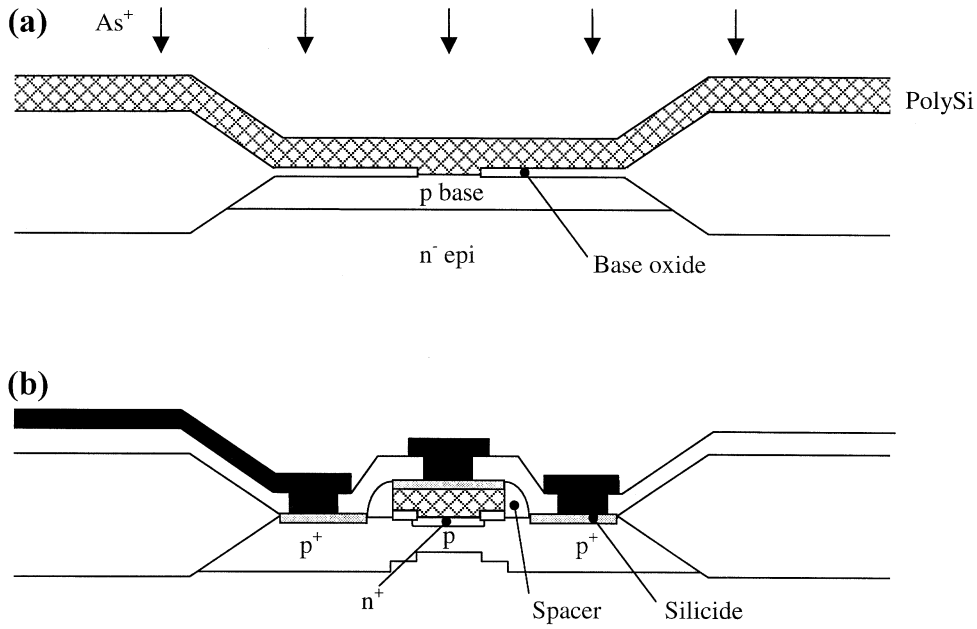


**FIGURE 3.14** The single-poly, quasi-self-aligned process: (a) polyemitter implantation, (b) final device.

### Double-Poly Structure

The double-poly structure originates from the classical IBM structure presented in 1981.[74] Most high-performance commercial processes today are based on double-poly technology. The number of variations are less than for the single-poly, mainly with different aspects on base-link engineering, spacer technology, and SIC formation. One example of a double-poly fabrication is presented in Fig. 3.15. After deposition of the base polysilicon and oxide stack, the emitter window is opened (Fig. 3.15(a)) and thermally oxidized. During this step, $p^+$-impurities from the base polysilicon diffuse into the monosilicon, thus forming the extrinsic base. In addition, the oxidation repairs the crystal damage caused by the dry etch when opening the emitter window. A thin silicon nitride layer is then deposited, the intrinsic base is implanted using boron, followed by the fabrication of amorphous silicon spacers inside the emitter window (Fig. 3.15(b)). The nitride is exposed to a short dry etch, the spacers are removed, and the thin oxide is opened up by an HF dip. Deposition and implantation of the polysilicon emitter film is carried out (Fig. 3.15(c)). The structure is patterned and completed by RTA emitter drive-in and metallization (Fig. 3.15(d)). The emitter will thus be fully self-aligned with respect to the base. Note that the inside spacer technology implies that the actual emitter width will be significantly less than the drawn emitter width.

The definition of the polyemitter in the single- and double-poly process inevitably leads to some overetching into the epi-layer, see Figs. 3.13(b) and 3.15(a), respectively. The final recessed region will make control over base-link formation more awkward.[75,76] In fact, the base link will depend both on the degree of overetch as well as the implantation parameters.[77] This situation is of no concern for the quasi-self-aligned process where the etch of the polysilicon emitter stops on the base oxide.

In a modification of the double-poly process, a more advanced base-link technology is proposed.[78] After extrinsic base drive-in and emitter window opening, $BF_2$-implanted poly-spacers are formed inside the emitter window. The boron is out-diffused through the emitter oxide, thus forming the base link. The intrinsic base is subsequently formed by conventional implantation through the emitter window. New dielectric inside spacers are formed prior to polysilicon emitter deposition, followed by arsenic implantation and emitter drive-in.

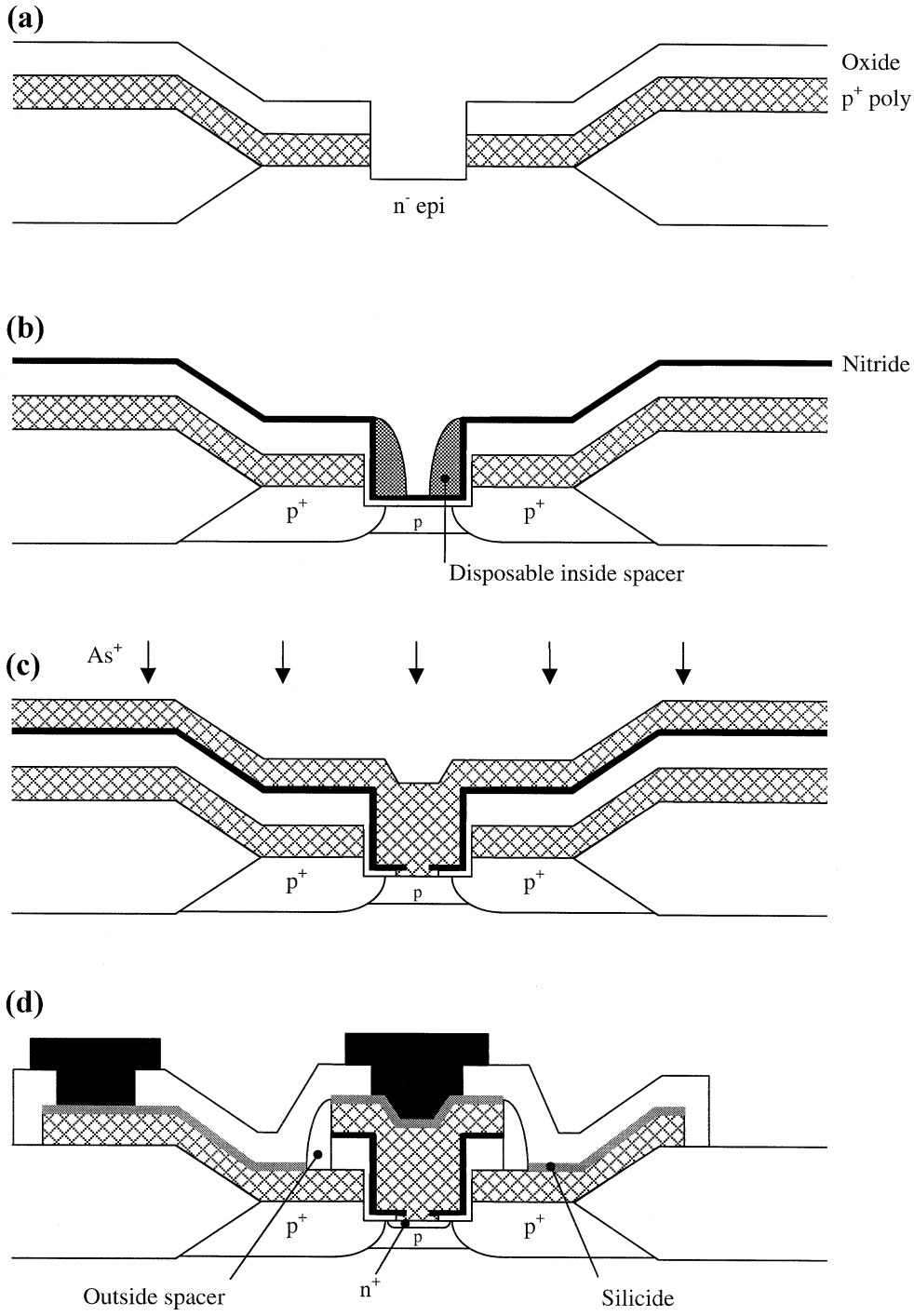


**FIGURE 3.15** The double-poly, self-aligned process: (a) emitter window etch, (b) intrinsic base implantation through thin oxide/nitride stack followed by inside spacer formation, (c) polyemitter implantation, (d) final device after emitter drive-in and metallization.

Also, vertical pnp bipolar transistors based on the double-poly concept have been demonstrated.[79] Either boron or $BF_2$ is used for the polyemitter implantation. A pnp device with $f_T$ of 35 GHz has been presented in a classical double-poly structure.[80]

## 3.5 Advanced Bipolar Technology

This chapter section treats state-of-the-art bipolar technologies reported during the 1990s (but not necessarily put into production). Alongside the traditional down-scaling in design rules, efforts have focused on new innovations in emitter and base electrode fabrication. A key issue has been the integration of epitaxial Si or SiGe intrinsic base into the standard npn process flow. This section concludes with an outlook on the future trends in bipolar technology after the year 2000.

### Implanted Base

Today's most advanced commercial processes are specified with an $f_T$ around 30 GHz. The major developments are being carried out using double-poly technology, although new improvements have also been reported for single-poly architectures.[72,81] For double-poly transistors, it was demonstrated relatively early that by optimizing a very low intrinsic base implant energy below 10 keV, devices with an $f_T$ around 50 GHz are possible to fabricate.[82] The emitter out-diffusion is performed by a combined furnace anneal and RTA. In this way, the intrinsic base width is controlled below 1000 Å, whereas the emitter depth is only around 250 Å.

Since ion implantation is associated with a number of drawbacks such as channeling, shadowing effects, and crystal defects, it may be difficult to reach an $f_T$ above 50 to 60 GHz based on such a technology. The intrinsic base implantation has been replaced by rapid vapor deposition using $B_2H_6$ gas around 900°C.[83] The in-diffused boron profile will form a thin and low-resistive base. Also, the emitter implantation can be removed by utilizing *in situ* doped emitter technology (e.g., $AsH_3$ gas during polysilicon deposition).[84] Two detrimental effects are then avoided; namely, emitter perimeter depletion and the emitter plug effect.[85] The former effect causes a reduced doping concentration close to the emitter perimeter, whereas the latter implies the plugging of doping atoms in narrow emitter windows causing shallower junctions compared to larger openings on the same chip.

Arsenic came to replace phosphorus as the emitter impurity during the 1970s, mainly because of the emitter push-effect plaguing phosphorus monosilicon emitters. The phosphorus emitter has, however, experienced a renaissance in advanced bipolar transistors by introducing the so-called *in situ* phosphorus doped polysilicon (IDP) emitter.[86] One motivation for using IDP technology is the reduction in final emitter resistance compared to the traditional As polyemitter, in particular for aggressively down-scaled devices with very narrow emitter windows. In addition, the emitter drive-in for an IDP emitter is carried out at a lower thermal budget than the corresponding arsenic emitter due to the difference in diffusivity between the impurity atoms. Using IDP and RVD, very high $f_T$ values (above 60 GHz) have been realized.[83] It has been suggested that the residual stress of the IDP emitter and the interfacial oxide between the poly- and the monosilicon creates a heteroemitter action for the device, thus explaining the high current gains of IDP bipolar transistors.[87]

Base electrode engineering in advanced devices has become an important field in reducing the total base resistance, thus improving $f_{max}$ of the transistor. One straightforward method in lowering the base sheet resistance is by shunting the base polysilicon with an extended silicide across the total base electrode. This has recently been demonstrated in an $f_{max} = 60$ GHz double-poly process.[88] A still more effective concept is to integrate metal base electrodes.[89] This approach is combined with *in situ* doped boron polysilicon base electrodes as well as an IDP emitter in a double-poly process (see Fig. 3.16). The tungsten electrodes are fully self-aligned using $WF_6$-selective deposition. The technology, denoted SMI (self-aligned metal IDP), has been applied together with RVD base formation. The bipolar process was shown to produce $f_T$ and $f_{max}$ figures of 100 GHz at a breakdown voltage of 2.5 V.[90]

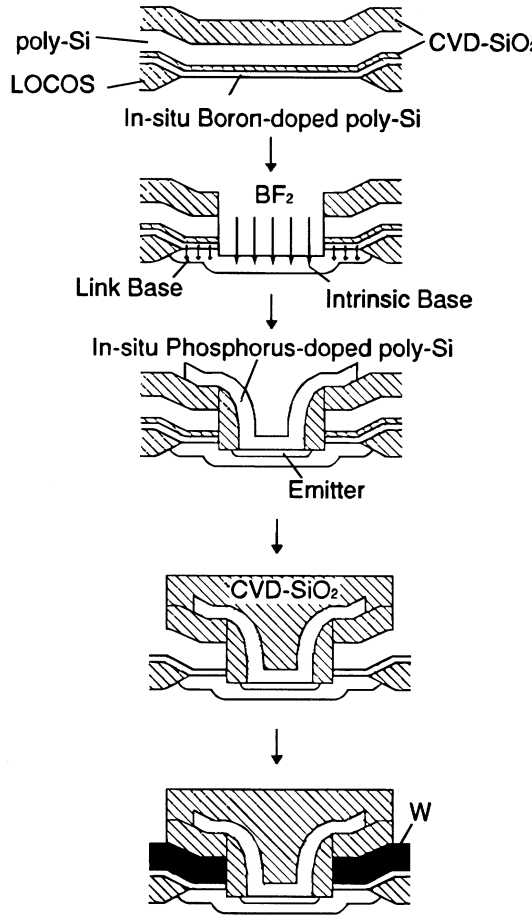


**FIGURE 3.16** The self-aligned metal IDP process using selective deposition of tungsten base electrodes (after Ref. 89, copyright© 1997, IEEE).

## Epitaxial Base

By introducing epitaxial film growth techniques for intrinsic base formation, the base width is readily controlled on the order of some hundred angstroms. Both selective and non-selective epitaxial growth (SEG and NSEG, respectively) have been reported. One example of a SEG transistor flow is illustrated in Fig. 3.17.[91] Not only the epitaxial base, but also the $n^-$-collector is grown using SEG. The $p^+$-poly overhangs warrant a strong base link between the SEG intrinsic base and the base electrode. This $f_T = 44$ GHz process was capable of delivering divider circuits working at 25 GHz.

A natural extension of the Si epitaxy is to apply the previously mentioned SiGe epitaxy, thus creating a heterojunction bipolar transistor (HBT). For example, the transistor process in Fig. 3.17 was later extended to a SiGe process with $f_T = 61$ GHz and $f_{max} = 74$ GHz.[92] Apart from high speed, low base resistance is a trademark for many SiGe bipolar processes. For details of the SiGe HBT, the reader is referred to Chapter 5. Here, only some process integration points of view are given of this very important technology for advanced silicon-based bipolar devices during the 1990s.

While the first world records in terms of $f_T$ and $f_{max}$ were broken for non-self-aligned structures or mesa HBTs, planar self-aligned process schemes taking advantage of the benefits using SiGe have

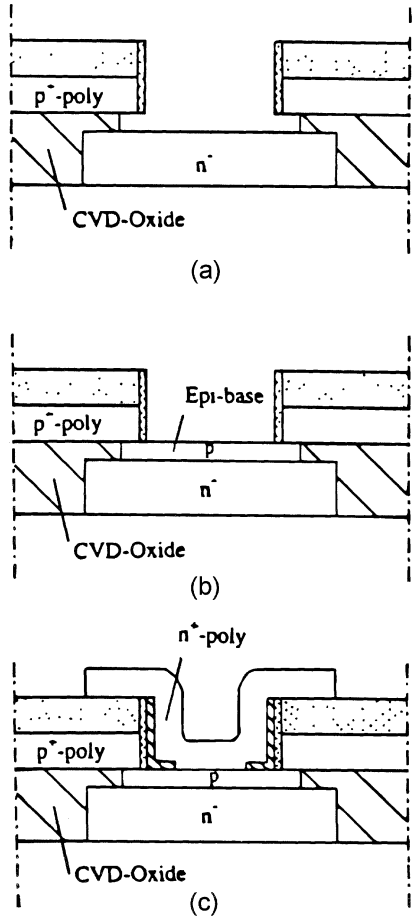


**FIGURE 3.17** Process demonstrating selective epitaxial growth: (a) self-aligned formation of $p^+$-poly overhangs, (b) selective epitaxial growth of the intrinsic base, (c) emitter fabrication (after Ref. 91, copyright© 1992, IEEE).

subsequently been demonstrated. In recent years, both single-poly and double-poly SiGe transistors exhibiting excellent dc and ac properties have been presented. This also includes the quasi-self-aligned approach where a fully CMOS compatible process featuring an $f_{max}$ of 71 GHz has been shown.[93] A similar concept featuring NSEG, so-called differential epitaxy, has been applied in the design of an HBT with a single-crystalline emitter rather than a polysilicon emitter.[94] This process, however, requires a very low thermal budget because of the high boron and germanium content in the intrinsic base of the transistor. Excellent properties for RF applications are made possible by this approach, such as high $f_T$ and $f_{max}$ around 50 GHz, combined with good dc properties and low noise figures.[95]

In double-poly structures, the extrinsic base is usually deposited prior to SiGe base epitaxy, which is then carried out by SEG (as shown in Fig. 3.17). Several groups report $\tau_d$ below 20 ps using this approach. One example of the most advanced bipolar technologies is the SiGe double-poly structure shown in Fig. 3.18.[96] This technology features the SMI base electrode technology, together with SEG of SiGe. The device is isolated by oxide-filled trenches. The reported $\tau_d$ was 7.7 ps and the $f_{max}$ was 108 GHz, thus approaching the SiGe HBT mesa record of 160 GHz.[97] A device similar to the one in Fig. 3.18 was also reported to yield an $f_T$ of 130 GHz.[98]

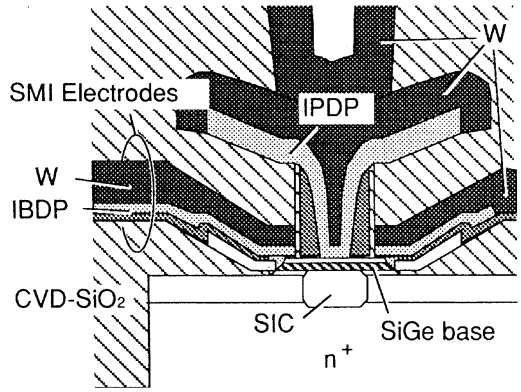


**FIGURE 3.18** A state-of-the-art bipolar device featuring SMI electrodes, selectively grown epitaxial SiGe base, *in situ* doped polysilicon emitter/base and oxide-filled trenches (after Ref. 96, copyright© 1998, IEEE).

## Future Trends

The shrinking of dimensions in bipolar devices, in particular for digital applications, will proceed one or two generations behind the MOS frontier, leading to a further reduction in $\tau_d$. Several of the concepts reviewed above for advanced bipolar components are expected to be introduced in the next commercial high-performance processes; for example, *in situ* doped emitter and low-resistivity base electrodes. Similar to CMOS, the overall temperature budget must be reduced in processing. Evidently, bipolar technology in the future also continues to benefit from the progress made in CMOS technology; for example, in isolation and back-end processing. CMOS compatibility will be a general requirement for the majority of bipolar process development because of the strong interest in mixed-signal BiCMOS processes.

Advanced isolation technology combining deep and shallow trenches, perhaps on silicon-on-insulator (SOI) or high-resistivity substrates, marks one key trend in future bipolar transistors. Bipolar technology based on SOI substrates may well be accelerated by the current introduction of SOI into CMOS production. However, thermal effects for high current drive bipolar devices must be solved when using SOI. An interesting low-cost alternative insulating substrate for RF-bipolar technology is the silicon-on-anything concept recently presented.[99] In addition, copper metallization will be introduced for advanced bipolars provided that intermetal dielectrics as well as passive components are developed to meet this additional advantage.[100]

The epitaxial base constitutes another important trend where both Si and SiGe are expected to enhance performance in the high-frequency domain, although the introduction may be delayed due to progress in ion-implanted technology. In this respect, SEG technology has yet to prove its manufacturability.

Future Si-based bipolar technology with $f_T$ and $f_{max}$ greater than 100 GHz will continue to play an important role in small-density, high-performance designs. The most important applications are found in communication systems in the range 1 to 10 GHz (wireless telephony and local area networks) and 10 to 70 GHz (microwave and optical-fiber communication systems) where Si and/or SiGe bipolar technologies are expected to seriously challenge existing III-V technologies.[101]

## Acknowledgments

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