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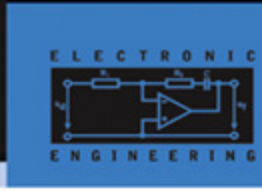

Phase-Locked Loop Synthesizer Simulation

- ✔ Open loop, closed loop, and phase error response calculations
- ✔ Noise definition and analysis
- ✔ Direct Digital Synthesizer
- ✔ CD containing all Mathcad and SIMetrix files to perform analyses described in book

Giovanni Bianchi

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Preface

Many good books are available on phase-locked loop (PLL) theory. It is not my intention to compete with them in this field. This book primarily describes how to calculate PLL performances by using standard mathematical or circuit analysis programs. Theoretical descriptions are limited to the minimum needed to explain how to perform calculations. Although presented methods of analysis can be implemented with many commercial programs, their description always refers to MATHCAD for mathematical programs and to SIMETRIX for circuit analysis programs.

MATHCAD[†] is an integrated environment for performing and communicating math-related work. It is calculation software that allows you to enter mathematics as you would write them on a piece of paper, and it will automatically update all calculations, graphs, and results when you change values or equations. Further, MATHCAD includes hundreds of built-in mathematical functions and operations; operates on scalars, vectors, and matrices; and automatically tracks and converts units. It can also generate updatable symbolic solutions.

The SIMETRIX simulator core comprises a direct matrix analog simulator closely coupled with an event-driven digital simulator. This combination is often described as "mixed-mode" and has the ability to efficiently simulate both analog and digital circuits together. The analog simulator is a derivation of SPICE 3 developed by the CAD/IC group at the University of California at Berkeley, while the event-driven digital simulator is based on XSPICE from the Georgia Technical Research Institute. However, only about 50 percent of the SIMETRIX simulator code can be directly traced to these programs. CATENA Software Ltd. has rewritten some parts and has added its own original code to others. The additions and changes were made to improve speed, add new functionality, and improve convergence.

[†]Mathcad is a registered trademark of Mathsoft Engineering and Education, Inc., *www.mathsoft.com*.

This book includes a CD-ROM[†] with

- An academic evaluation version of MATHCAD 11b: a fully functional version of MATHCAD that will operate for 120 days from installation.
- A demo version of SIMETRIX[‡]. Virtually all features are enabled, but a circuit size limit applies which allows the demo program to run all included circuit files.
- All MATHCAD and SIMETRIX files to perform the analyses described in the book. The reader can play with them and modify values and/or configurations in order to adapt to different PLLs.

Most of the calculations are possible with both methods, although one or the other may be easier in a particular case.

Chapter 1 describes basic PLL theory and explains some important concepts like loop stability, PLL classification, and transfer functions. Chapter 2 describes the operation of loop components: the phase detector, loop filter, VCO and crystal oscillator, and frequency divider. Descriptions are not given with the purpose to explain the design of these components (with the only exception of the loop filter) but just to show problems related with their use in PLLs. Chapter 3 is dedicated to the fractional frequency divider with analog and digital compensation. Chapter 4 is the core chapter of this book and describes in detail how to calculate and optimize PLL performance: mainly stability, phase noise, and settling time. Chapter 5 is a miscellaneous chapter covering PLL testing and debugging, sampled PLLs, multiloop synthesizers, and DDSs.

Half of the time spent writing this book was dedicated to finding and eliminating mistakes; nevertheless I am sure I was not 100 percent successful. Readers can contact the author by e-mail[§] with comments, suggestions, and detected errors.

Special thanks to Mrs. Stefania Stramaglia and Dr. Elisa Tordella for their assistance in checking the accuracy of the wording of this book and to Lucy Mullins for the final copyediting.

Giovanni Bianchi

[†]All programs are supplied as they are. No responsibility is taken for wrong results, bugs or problems to computer where they are installed.

[‡]An updated version can be downloaded at *www.catena.uk.com*.

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Chapter

1

Phase-Locked Loop Basics

1.1 Introduction

The *phase-locked loop* (PLL) is the most important technique for generation of radio frequency and microwave signals. It allows the generation of variable output frequency with the same stability of a crystal oscillator by means of feedback. This chapter describes the basic concepts that will be developed in subsequent chapters.

Linear block diagrams and their analysis will be examined, and fundamental equations will be derived. A PLL is a feedback system, so stability analysis is quite important: fundamental concepts of stability analysis will be introduced. In addition, the classification of PLL by order and type will be given. The description of simple second-order PLLs will also be used to define some fundamental parameters like unit bandwidth and peak response. Second-order PLL analysis will also provide the opportunity to show some introductory simple simulations.

All concepts will be explained with a minimum of mathematics. The number and complexity of equations used to develop simulation techniques in subsequent chapters will be the minimum required. For the same reason, some assertions will not be rigorous from the mathematical point of view. Again all mathematical descriptions are necessary for the implementation of calculations in computer programs. Any mathematical inexactness that could be present will not affect the precision of calculated results.

1.2 PLL Working Principles

The schematic block diagram of a PLL is shown in Fig. 1.1. It contains four basic blocks:

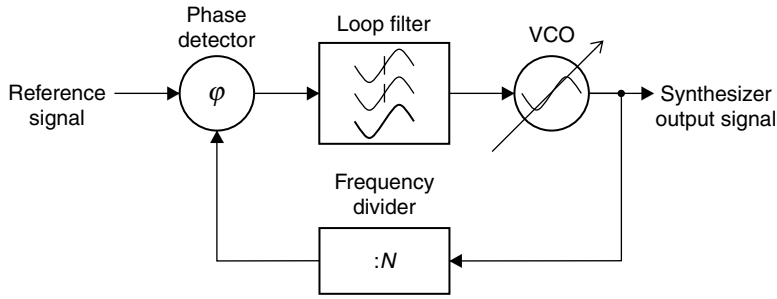


Figure 1.1 PLL block diagram.

1. Phase detector (PD). The PD compares a periodic input signal (reference signal, normally a sine or square wave) with the frequency divider output signal. The PD output voltage is proportional to the phase difference between the two signals.
2. Loop filter. This is a lowpass filter that smoothes the PD output signal and applies it to the VCO input.
3. Voltage-controlled oscillator (VCO). The output frequency of this device is a monotonic increasing function of input voltage. As a first approximation we will assume that the output frequency is directly proportional to the tuning voltage.
4. Frequency divider. The output of the frequency divider is a signal with a frequency equal to the VCO output frequency divided by N.

The PLL is a servo-controlled system. If its loop gain is high enough and the loop is stable, the system will reach a stable condition where two PD inputs have the same phase and thus the same frequency (the angular frequency is the derivative of the phase with respect to the time). In this condition, the output frequency equals the input frequency multiplied by N.

$$\text{ReferenceSignal}(t) = V_r \cos(\omega_r t)$$

$$\text{SynthesizerOutputSignal}(t) = V_o \cos(N\omega_r t)$$

When the frequency division factor N is modified, the output frequency will be modified accordingly. If the reference signal is a very stable one, the output frequency will become very stable as well. This is the PLL frequency synthesizer principle of working.

The PD, VCO, and frequency divider have instantaneous input-output relations. The loop filter input-output relation is difficult to write in terms of an instantaneous relation. We will therefore use the Laplace transform to represent PLL signals.

1.3 Laplace and Fourier Transforms

1.3.1 Definitions

$$G(s) = \mathscr{L}[g(t)] = \int_0^\infty g(t)\exp(-st)\,dt$$

$$G(f) = \mathscr{F}[g(t)] = \int_{-\infty}^\infty g(t)\exp(-j2\pi t)\,dt$$

where $G(s)$ is the Laplace transform of $g(t)$ and $G(f)$ is the Fourier transform of $g(t)$. The Laplace variable is complex: $s = \sigma + j\omega$. For functions equal to zero for $t < 0$, the Laplace transform calculated on the imaginary axis $s = j\omega = j2\pi f$ coincides with the Fourier transform.

1.3.2 Basic properties

Linearity:

$$\mathscr{L}[af(t) + bg(t)] = a\mathscr{L}[f(t)] + b\mathscr{L}[g(t)]$$
$$\mathscr{F}[af(t) + bg(t)] = a\mathscr{F}[f(t)] + b\mathscr{F}[g(t)]$$

Transform of derivative:

$$\mathscr{L}\left\{\frac{d[g(t)]}{dt}\right\} = sG(s)$$
$$\mathscr{F}\left\{\frac{d[g(t)]}{dt}\right\} = j2\pi f\,G(f)$$

Transform of integral:

$$\mathscr{L}\left[\int_0^t g(\tau)\,d\tau\right] = \frac{1}{s}G(s)$$
$$\mathscr{F}\left[\int_{-\infty}^t g(\tau)\,d\tau\right] = \frac{1}{j2\pi f}G(f)$$

Transform of time translated function:

$$\mathscr{L}[g(t-\tau)] = G(s)\,\exp(-s\tau)$$
$$\mathscr{F}[g(t-\tau)] = G(f)\,\exp(-j2\pi f\,\tau)$$

Translation over frequency I:

$$\mathscr{L}[g(t)\ \exp(at)] = G(s-a)$$
$$\mathscr{F}[g(t)\exp(j2\pi\nu t)] = G(f\ -\nu)$$

Translation over frequency II:

$$\mathscr{L}[G(t)\ \cos(at)] = \frac{G(s-ja)+G(s+ja)}{2}$$
$$\mathscr{F}[g(t)\ \cos(2\pi\nu t)] = \frac{G(f\ -\nu)+F(f\ +\nu)}{2}$$

Translation over frequency III:

$$\mathscr{L}[g(t)\sin(at)] = \frac{G(s-ja)-G(s+ja)}{2j}$$
$$\mathscr{F}[g(t)\sin(2\pi\nu t)] = \frac{G(f\ -\nu)-G(f\ +\nu)}{2j}$$

Initial value theorem:

$$f\,(t=0) = \lim_{s\to\infty}[sF(s)]$$

Final value theorem:

$$\lim_{t\to\infty} f\,(t) = \lim_{s\to 0}[sF(s)]$$

1.3.3 Transforms of some important functions

Unit step:

$$\eta(t) = \begin{cases} 0 & (t<0) \\ 1 & (t>0) \end{cases}$$

Rectangular pulse:

$$\mathrm{rect}_{\Delta T}\,(t) = \begin{cases} \frac{1}{\Delta T} & (0<t<\Delta T) \\ 0 & \text{elsewhere} \end{cases}$$

Dirac distribution:

$$\delta(t) = \lim_{\Delta T\to 0}\mathrm{rect}_{\Delta T}\,(t) = \frac{d\,[\eta(t)]}{dt}$$

Laplace and Fourier transform of Dirac distribution:

$$\mathscr{L}[\delta(t)] = \mathscr{F}[\delta(t)] = 1$$

Laplace and Fourier transform of unit step:

$$\mathscr{L}[\eta(t)] = \mathscr{F}[\eta(t)] = \frac{1}{s}$$

Laplace transform of exponential function:

$$\mathscr{L}[\exp(\alpha t)] = \frac{1}{s-\alpha}$$

Fourier transform of a constant:

$$\mathscr{F}[1] = \delta(f)$$

1.4 PLL Transfer Functions

In our representation, only the phase (or angular frequency) of signals is considered. We will concentrate on the phase (or angular frequency) of the signals. *Phase* is the integral of angular frequency.

$$\text{ReferenceSignal}(t) = V_r \cos\left[\int_{-\infty}^{t} \omega_r(\tau)\, d\tau\right] = V_r \cos[\theta_r(t)]$$

$$\text{SynthesizerOutputSignal}(t) = V_o \cos\left[\int_{-\infty}^{t} \omega_o(\tau)\, d\tau\right] = V_r \cos[\theta_o(t)]$$

For subsequent considerations lowercase letters will denote time-domain expressions, and corresponding Laplace transforms will be denoted by capital letters; e.g., $F(s) = \mathscr{L}[f(t)]$. We will also suppose that all conditions for the existence of the Laplace transform will be satisfied. One of the main advantages of Laplace transforms is that integrals (derivatives) of time domain functions correspond to their Laplace transforms multiplied by $1/s(s)$. Using the Laplace transform properties, it is possible to find some simple representations of the PLL blocks. In detail, the frequency divider output frequency equals the input frequency divided by N; the same holds true for the angular frequency and phase. The frequency divider can be represented as one multiplier by the constant $1/N$. The loop filter is characterized by its transfer function which is the rational function of the variable s; its representation is a multiplier by the transfer function. The VCO output angular frequency is proportional to the control voltage, so it can be represented as a multiplier by constant K_v; if we are interested in the VCO's output phase rather than its output angular frequency, the K_v gain block has to be followed by one integrator which is a multiplier by $1/s$ in the Laplace domain. The phase detector output is the phase difference

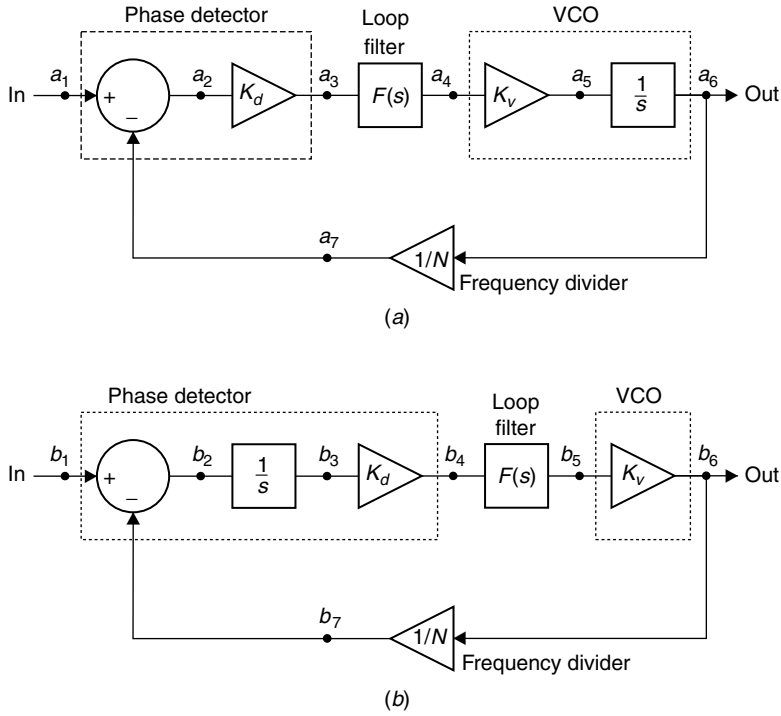


Figure 1.2 PLL transfer function. (a) From input to output phase. a_1—reference signal phase $\Theta_r(s)$; a_2—phase error $\Theta_e(s) = \Theta_r(s) - \Theta_v(s)$; a_3—PD output $V_{\text{det}}(s) = K_d\,\Theta_e(s)$; a_4—VCO tuning voltage $V_t(s) = V_{\text{det}}(s)F(s)$; a_5—VCO output angular frequency $\Omega_o(s) = K_v V_t(s)$; a_6—VCO (and PLL) output phase $\Theta_o(s) = \Omega_o(s)/s$; a_7—frequency divider output phase $\Theta_v(s) = \Theta_o(s)/N$. ($b$) From input to output in angular frequency. b_1—reference signal angular frequency $\Omega(s)$; b_2—angular frequency error $\Omega_e(s) = \Omega_r(s) - \Omega_v(s)$; b_3—phase error $\Theta_e(s) = \Omega_e(s)/s$; b_4—phase detector output $V_{\text{det}}(s) = K_d\,\Theta_e(s)$; b_5—VCO tuning voltage $V_t(s) = V_{\text{det}}(s)F(s)$; b_6—VCO (and PLL) output angular frequency $\Omega_o(s) = K_v V_t(s)$; b_7—frequency dvider output angular frequency $\Omega_v(s) = \Omega_o(s)/N$.

between inputs multiplied by the phase detector gain K_d; if we choose to represent angular frequency, we multiply the angular frequency difference by $1/s$ to obtain the phase difference.

Two PLL block diagrams are possible. In the first (see Fig. 1.2a), the input is the reference signal phase and the output is the output signal phase. In the second (see Fig. 1.2b), the input and the output are the reference signal and output signal angular frequency, respectively.

Consider the block diagram of Fig. 1.2a. Regrouping relations for quantities a_1 through a_7 it is possible to write

$$\Theta_o(s) = K_d K_v F(s)\left[\Theta_r(s) - \frac{\Theta_o(s)}{N}\right]\frac{1}{s}$$

Consequently the transfer function from the reference signal to the synthesizer output signal phase is given by

$$\frac{\Theta_o(s)}{\Theta_r(s)} = N \frac{\frac{K_d K_v}{N} \frac{F(s)}{s}}{1 + \frac{K_d K_v}{N} \frac{F(s)}{s}} \tag{1.1}$$

The same transfer function can be found for the angular frequency by analyzing the block diagram of Fig. 1.2*b*.

$$\frac{\Omega_o(s)}{\Omega_r(s)} = N \frac{\frac{K_d K_v}{N} \frac{F(s)}{s}}{1 + \frac{K_d K_v}{N} \frac{F(s)}{s}} \tag{1.2}$$

The transfer function from the reference signal phase (angular frequency) to the output signal phase (angular frequency) is given by the frequency division factor N multiplied by the PLL closed-loop transfer function:

$$H_L(s) = \frac{\frac{K_d K_v}{N} \frac{F(s)}{s}}{1 + \frac{K_d K_v}{N} \frac{F(s)}{s}} \tag{1.2'}$$

The Laplace variable is in general complex: $s = \sigma + j\omega$. Replacing it with the imaginary only variable $s = j\omega = j2\pi f$ corresponds to using the Fourier transform. The PLL closed-loop transfer function becomes the PLL frequency response:

$$H(f) = \frac{\frac{K_d K_v}{N} \frac{F(j2\pi f)}{j2\pi f}}{1 + \frac{K_d K_v}{N} \frac{F(j2\pi f)}{j2\pi f}} \tag{1.3}$$

and the transfer functions (1.1) and (1.2) become the PLL closed-loop gain:

$$\text{ClosedLoopGain}(f) = N \frac{\frac{K_d K_v}{N} \frac{F(j2\pi f)}{j2\pi f}}{1 + \frac{K_d K_v}{N} \frac{F(j2\pi f)}{j2\pi f}} = NF(f) \tag{1.3'}$$

The PLL frequency response $H(f)$ can also be seen as the gain from the reference input to the frequency divider output.

We supposed that the loop filter is lowpass. In terms of its frequency response this means that

$$\lim_{f \to 0} |F(j2\pi f)| > 0 \qquad \text{and} \qquad \lim_{f \to \infty} |F(j2\pi f)| \le |F(j2\pi f)|_{f=0} < \infty \tag{1.4}$$

These assumptions imply that

$$\lim_{f\to\infty} H(f) = \lim_{f\to\infty} \frac{\frac{K_d K_v}{N} F(j2\pi f)}{j2\pi f + \frac{K_d K_v}{N} F(j2\pi f)} = 0$$

and

$$H(f=0) = \left.\frac{\frac{K_d K_v}{N} F(j2\pi f)}{j2\pi f + \frac{K_d K_v}{N} F(j2\pi f)}\right|_{f=0} = \frac{\frac{K_d K_v}{N} F(0)}{\frac{K_d K_v}{N} F(0)} = 1$$

In other words, the closed-loop PLL frequency response is lowpass with the unit gain in direct current. The combination of Eq. (1.3) with Eqs. (1.1) and (1.2) has a very interesting physical interpretation. It tells us that any phase (frequency) modulation on the reference signal modulates the phase (frequency) output signal multiplied by N and lowpass filtered. Thus, slow varying modulation affects the output signal; fast varying modulation doesn't.

1.4.1 PLL stability analysis

The stability of the loop is one important concept that needs to be discussed. The starting point is the open-loop frequency response. Open-loop gain can be calculated from Fig. 1.2*a* (or Fig. 1.2*b*); it is the gain from node a_1 to node a_7 (or from b_1 to b_7):

$$H_{\text{OpenLoop}}(f) = \frac{K_d K_v}{N} \frac{F(j2\pi f)}{j2\pi f} \tag{1.5}$$

Closed-loop stability analysis can be made by analyzing the open-loop frequency response. For this purpose the open-loop gain amplitude and phase calculation are needed. Control system theory states that a system is stable if the poles of its transfer function[†] have a negative real part. We will assume that the loop filter is stable by itself. From feedback control system theory we know that a system is unstable if the phase shift ϕ_o at the frequency where the open-loop gain has unitary amplitude, f_o, equals $\pi(180^\circ)$.[‡]

Open-loop gain is the product of three factors:

1. Constant factor $K_d K_v/N$
2. Lowpass function $F(j2\pi f)$ having the properties of Eq. (1.4)
3. Integrator transfer function $1/(j2\pi f)$

[†]In the Laplace domain, the complex variable $s = \sigma + j\omega$.

[‡]Remember that $+\pi$ and $-\pi$ are the same phase shift.

Comparing the open-loop and closed-loop transfer functions [Eqs. (1.3) and (1.5)]; it can be seen that at high frequencies the denominator of Eq. (1.3) can be approximated by 1 because $\lim_{f\to\infty} F(j2\pi f)$ has a finite value and $\lim_{f\to\infty} j2\pi f = \infty$. Thus

$$\lim_{f\to\infty} \frac{F(j2\pi f)}{j2\pi f} = 0$$

So at high frequencies the open- and closed-loop gains are the same.

The open-loop gain amplitude is the product of the amplitudes of three factors. At zero frequency open-loop gain is infinite because the loop filter frequency response amplitude is greater than 0 and the integrator frequency response becomes infinite. At infinite frequency the open-loop gain is zero because the loop filter term is finite and the integrator term is zero. So the open-loop gain amplitude ranges from infinity (at zero frequency) to zero (at very high frequencies). Thus there is at least one frequency value that makes the open-loop gain have unitary amplitude. The phase of the open-loop gain is the sum of the phases of the previous listed three terms. The constant factor's phase is zero, the loop filter phase is a delay variable with frequency, and the integrator phase is $-\pi/2$ and is constant over frequency. In the next sections we will see that a zero-order loop filter has less than a $-\pi/2$ phase shift, so the total open-loop phase shift is less than π and the loop is always stable. Higher-order filters are not unconditionally stable. One parameter that is often used to evaluate loop stability is the *phase margin*. It is, by definition, the phase shift amount that has to be added to open-loop gain to make it become unstable. In other words the phase margin is the distance of the open-loop phase shift, calculated at unity gain frequency, from $+\pi$ or $-\pi$, whichever is closest. Of course, the higher the phase margin, the stronger the stability. Bode and Nyquist diagrams are normally used to check the phase margin. Their use will be explained in Sec. 1.7.

PLL *phase error response* is also of interest. Looking at Fig. 1.2*a*, the input is the reference signal phase $\Theta_r(s)$ (node a_1); the output is the phase error $\Theta_e(s) = \Theta_r(s) - \Theta_v(s)$ (node a_2). The transfer function is called the *error response* and can be computed with the same procedure used for closed-loop transfer function derivation. This gives

$$\begin{aligned}
\frac{\Theta_e(s)}{\Theta_r(s)} &= \frac{\Theta_r(s) - \Theta_v(s)}{\Theta_r(s)} = \frac{1}{1 + \frac{K_d K_v}{N}\frac{F(s)}{s}} = 1 - H(s) \\
\frac{\Theta_e(f)}{\Theta_r(f)} &= \frac{1}{1 + \frac{K_d K_v}{N}\frac{F(j2\pi f)}{j2\pi f}} = \frac{j2\pi f}{j2\pi f + \frac{K_d K_v}{N}F(j2\pi f)}
\end{aligned} \tag{1.6}$$

Regarding the loop filter frequency response we already assumed lowpass conditions (1.4), so

$$\lim_{f\to 0}\frac{\Theta_e(f)}{\Theta_r(f)}=0 \qquad \text{and} \qquad \lim_{f\to\infty}\frac{\Theta_e(f)}{\Theta_r(f)}=1$$

Thus, the error response is highpass.

1.5 PLL Order and PLL Type

We previously stated that the loop filter is a lowpass filter whose transfer function is a rational function with real coefficients of the variable s (or $j2\pi f$). The loop filter frequency response can be written as

$$F(f)=\frac{\sum_{k=0}^{N_A}A_k(j2\pi f)^k}{\sum_{k=0}^{N_B}B_k(j2\pi f)^k} \tag{1.7}$$

It has to satisfy conditions (1.4), implying that

$$\lim_{f\to 0}|F(f)|=\left|\frac{A_0}{B_0}\right|>0\Rightarrow A_0\neq 0$$

and

$$\begin{aligned}\lim_{f\to\infty}|F(f)| &= \lim_{f\to\infty}\left|\frac{A_{N,A}(j2\pi f)^{N_A}}{B_{N,B}(j2\pi f)^{N_B}}\right| \\ &= \left|\frac{A_{N,A}}{B_{N,B}}\right|\lim_{f\to\infty}\left|(j2\pi f)^{N_A-N_B}\right|\le\left|\frac{A_0}{B_0}\right|<\infty\Rightarrow N_B\ge N_A\end{aligned}$$

In other words the numerator of the frequency response has a constant term different from zero, and the denominator order is greater than or equal to the numerator order. Define the order of the loop filter as the order of its frequency response denominator. Let's write the PLL frequency response using an explicit expression of the loop filter frequency response.

$$H(f)=\frac{\frac{K_dK_v}{N}\frac{\sum_{k=0}^{N_A}A_k(j2\pi f)^k}{\sum_{k=0}^{N_B}B_k(j2\pi f)^k}}{j2\pi f+\frac{K_dK_v}{N}\frac{\sum_{k=0}^{N_A}A_k(j2\pi f)^k}{\sum_{k=0}^{N_B}B_k(j2\pi f)^k}}$$

$$H(f)=\frac{\frac{K_dK_v}{N}\sum_{k=0}^{N_A}A_k(j2\pi f)^k}{j2\pi f\sum_{k=0}^{N_B}B_k(j2\pi f)^k+\frac{K_dK_v}{N}\sum_{k=0}^{N_A}A_k(j2\pi f)^k}$$

$$H(f)=\frac{\frac{K_dK_v}{N}\sum_{k=0}^{N_A}A_k(j2\pi f)^k}{\sum_{k=0}^{N_B}B_k(j2\pi f)^{k+1}+\frac{K_dK_v}{N}\sum_{k=0}^{N_A}A_k(j2\pi f)^k} \tag{1.8}$$

$H(f)$ is a rational function of variable $j2\pi f$; the numerator is an N_A-order polynomial, and the denominator is an (N_B+1)-order polynomial. Both polynomials have real coefficients. From conditions (1.4), we have that the numerator has a nonzero constant term and that the denominator order is strictly greater than the numerator order. The PLL order is the same as the closed-loop frequency response denominator order which is N_B+1. The PLL order equals the loop filter order plus one.

Another PLL classification can be made by the number of poles of open-loop gain at zero frequency. Remembering open-loop gain expression (1.5) and lowpass conditions (1.4), we can find that the open-loop gain has at least one pole located at zero frequency given by the integrator factor $1/(j2\pi f)$. The loop filter can have at most one additional pole at zero frequency; it can't have more because circuit theory tells us that one network with two coincident poles on the imaginary axis of variable s (including zero) is unstable. Summarizing, open-loop gain can have one or two poles at zero frequency depending on whether the loop filter DC gain is finite or infinite. The number of poles at zero frequency of the open-loop frequency response is the type of the PLL (1 or 2).

1.6 First-Order PLL

The simplest loop filter frequency response satisfying conditions (1.4) is a constant one: $V_{\text{out}} = AV_{\text{in}}$. If the $A < 1$ loop filter is a resistive voltage divider, the loop filter order is zero. In the simplest case, $A = 1$ and the loop filter simply consists of a piece of wire. The zero-order loop filter gives the first-order PLL whose frequency response is given by

$$H(f) = \frac{\frac{K_d K_v}{N} A}{j2\pi f + \frac{K_d K_v}{N} A} = \frac{1}{j\frac{f}{K_d K_v A/(2\pi N)} + 1} = \frac{1}{1 + j\frac{f}{f_n}} \tag{1.9}$$

The first-order PLL frequency response is a first-order lowpass response; its cutoff frequency is called the "natural frequency of PLL" and is given by

$$f_n = \frac{K_d K_v A}{2\pi N}$$

Normally, K_v, K_d, and N are determined, so the only flexibility in the PLL design is with the loop filter parameters. The zero-order loop filter has only one parameter: its gain A. Natural frequency is the only parameter of a first-order PLL closed-loop response; it can be changed by changing the loop filter gain. A first-order PLL is impossible to realize, one reason being that any practical VCO has a limited modulation bandwidth, and thus the VCO transfer function isn't a simple constant K_v.

1.7 Second-Order PLL

First-order loop filters, which correspond to second-order PLLs, are widely used. Figure 1.3*a* and *b* shows passive and active first-order loop filters. The first-order filter is more realistic than the zero-order one because it can be designed with a bandwidth narrower than the VCO modulation bandwidth and thus the effect of the latter can be neglected. For this reason the second-order loop will be used to investigate some PLL functions like the closed-loop response and the error response and to introduce some concepts needed for stability analysis.

The passive filter frequency response is given by

$$F_{1,\,\text{passive}}(f) = \frac{j2\pi\tau_2 f + 1}{j2\pi(\tau_1 + \tau_2)f + 1} \qquad \text{with} \qquad \tau_1 = R_1 C \qquad \tau_2 = R_2 C \tag{1.10}$$

The active filter frequency response is given by

$$F_{1,\,\text{active}}(f) = \frac{j2\pi\tau_2 f + 1}{j2\pi\tau_1 f} \qquad \text{with} \qquad \tau_1 = R_1 C \qquad \tau_2 = R_2 C \tag{1.11}$$

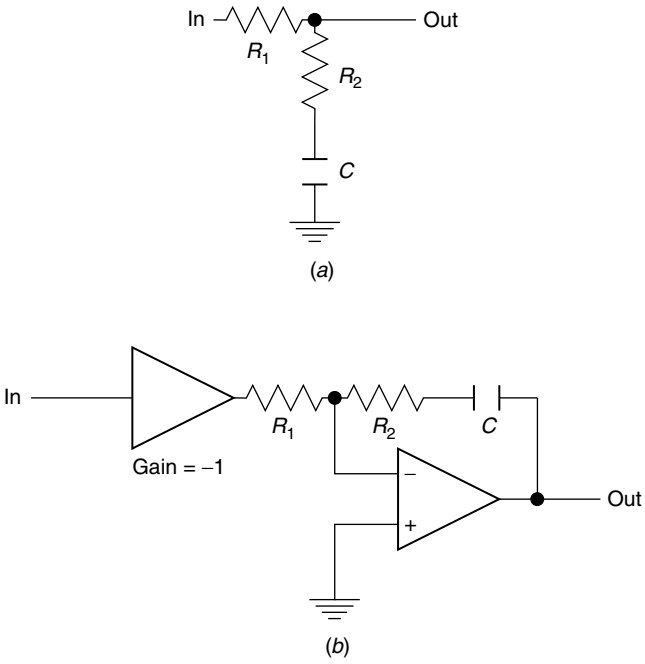


Figure 1.3 First-order loop filters. (*a*) Passive, and (*b*) active.

Note that both passive and active first-order filters have three components, but their frequency responses have only two parameters: τ_1 and τ_2. This is because the frequency response depends on the ratio between two impedances: the first given by R_2 in series with C, the second by R_1. The passive (active) filter second-order PLL frequency response can be calculated substituting Eq. (1.10) [Eq. (1.11)] in Eq. (1.3) and rearranging the expressions. The passive first-order loop has a finite DC gain; an active one has an infinite DC gain (in practical cases, finite but very high). So the second-order PLL with a passive filter is type I and with an active filter is type II.

$$H_{\text{Passive}}^{\text{2ndOrder}}(f) = \frac{j2\pi f\left(\frac{1}{Q}\frac{1}{2\pi f_n} - \frac{N}{K_d K_v}\right) + 1}{\left(j\frac{f}{f_n}\right)^2 + j\frac{1}{Q}\frac{f}{f_n} + 1} \tag{1.12}$$

with

$$f_n = \frac{1}{2\pi}\sqrt{\frac{K_d K_v}{N}\frac{1}{\tau_1+\tau_2}} \quad \text{and} \quad Q = \left[\left(\frac{N}{K_d K_v} + \tau_2\right)\sqrt{\frac{K_d K_v}{N}\frac{1}{\tau_1+\tau_2}}\right]^{-1}$$

$$H_{\text{Active}}^{\text{2ndOrder}}(f) = \frac{j\frac{1}{Q}\frac{f}{f_n} + 1}{\left(j\frac{f}{f_n}\right)^2 + j\frac{1}{Q}\frac{f}{f_n} + 1} \tag{1.13}$$

with

$$f_n = \frac{1}{2\pi}\sqrt{\frac{K_d K_v}{N}\frac{1}{\tau_1}} \qquad \text{and} \qquad Q = \left[\tau_2\sqrt{\frac{K_d K_v}{N}\frac{1}{\tau_1}}\right]^{-1}$$

As found on the first-order PLL, f_n is the natural frequency while Q is the damping factor of the loop. In most textbooks the damping factor is indicated with variable ζ instead of Q and $2\zeta = 1/Q$. As stated in Sec. 1.3, the PLL closed-loop denominator order is higher by one than that of the loop filter. The highest power of f in the frequency response is in its denominator and equals two[†]: that's why the PLL is known as the *second-order PLL*. Function (1.12) coincides with (1.13) if

$$\frac{1}{Q}\frac{1}{2\pi f_n} \gg \frac{N}{K_d K_v} \Rightarrow \tau_2 \gg \frac{N}{K_d K_v}$$

[†]According to the general rule found in Sec. 1.5, the PLL order equals the loop filter order plus one.

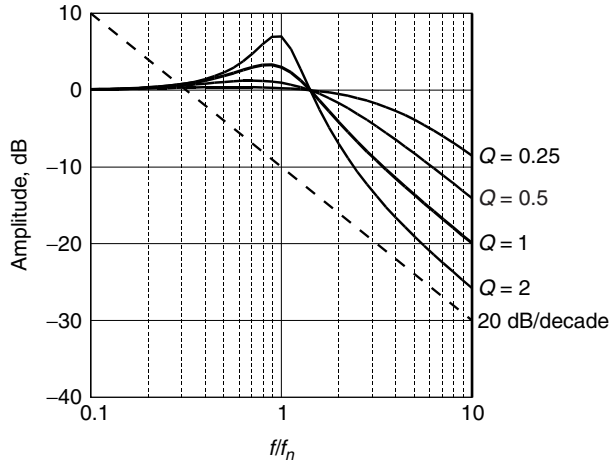


Figure 1.4 Active second-order PLL frequency response.

During subsequent considerations only active second-order PLLs will be considered. The amplitude of the frequency response (dB) is given by

$$\mathrm{dB}\left[H_{\text{Active}}^{\text{2ndOrder}}(f)\right] = 10\log_{10}\left\{\frac{\left(\frac{1}{Q}\frac{f}{f_n}\right)^2 + 1}{\left[1-\left(\frac{f}{f_n}\right)^2\right]^2 + \left(\frac{1}{Q}\frac{f}{f_n}\right)^2}\right\} \tag{1.14}$$

For $f < f_n$, the denominator of Eq. (1.14) is less than the numerator for any value of Q. This implies that for $f < f_n$, the frequency response magnitude is greater than 0 dB. The frequency response magnitude for several Q factors is plotted in Fig. 1.4. This graph shows that the loop operates like a lowpass filter on input signal (reference) phase modulations. Filter asymptotic slope is 20 dB/decade for any Q value; the peak on frequency response is increasing with Q. All curves have one common point ($f/f_n = \sqrt{2}$; 0). Frequency response (1.14) has a well-defined −3-dB frequency and response peak. The 3-dB frequency can be calculated from Eq. (1.13) and is

$$\left(\frac{f}{f_n}\right)^2_{-3\mathrm{dB}} = \frac{1+2Q^2+\sqrt{(1+2Q^2)^2+4Q^4}}{2Q^2}$$

The response peak occurs at the value where the derivative of Eq. (1.14) equals zero, which is

$$\left(\frac{f}{f_n}\right)^2 = Q\left(\sqrt{Q^2+2}-Q\right)$$

TABLE 1.1 Second-Order PLL 3-dB Frequency, Peak Response, and Peak Frequency for Some Values of the Damping Factor

Q	−3-dB f/f_n	Peak, dB	Peak f/f_n
0.10	10.100	0.076	0.132
0.25	4.249	0.400	0.297
0.50	2.482	1.249	0.500
0.71	2.054	2.102	0.619
1.00	1.817	3.334	0.732
2.00	1.622	7.171	0.899

The corresponding frequency response in dB is

$$\text{ClosedLoopPeak}(Q) = -10\log_{10}\left[1 - Q^2\left(Q - \sqrt{Q^2+2}\right)^2\right]$$

Table 1.1 lists the −3-dB normalized frequency, peak amplitude, and frequency for some Q values.

The active filter second-order PLL error response is

$$\text{dB}\left[1 - H_{\text{Active}}^{\text{2ndOrder}}(f)\right] = 10\log_{10}\left\{\frac{\left(\frac{f}{f_n}\right)^4}{\left[1-\left(\frac{f}{f_n}\right)^2\right]^2 + \left(\frac{1}{Q}\frac{f}{f_n}\right)^2}\right\} \quad (1.15)$$

Equation (1.15) is plotted in Fig. 1.5 for Q values of 0.25, 0.5, 1, 2. It can be seen that it is a highpass frequency response with a slope of

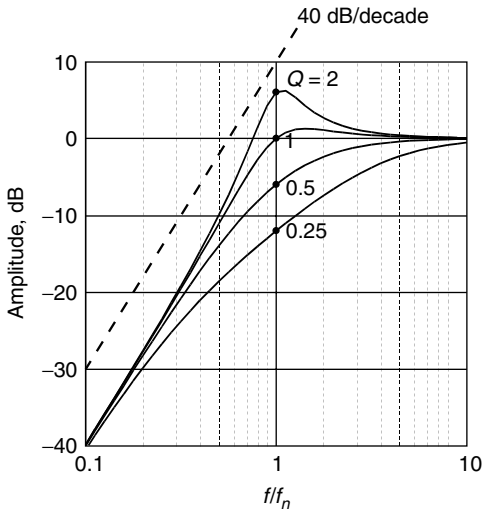


Figure 1.5 Active second-order PLL error response.

TABLE 1.2 Error Response Peak

Q	Peak, dB	Peak f/f_n
0.75	0.054	3.000
1.00	1.249	1.414
2.00	6.301	1.069
5.00	14.023	1.010

40 dB/decade. The error response presents a peak if $Q^2 > 0.5$. The peak amplitude increases with Q and is given by

$$\text{ErrorResponsePeak}(Q) = 10\log_{10}\left(\frac{4Q^4}{4Q^4 - 1}\right)$$

Table 1.2 lists error response peaks and their normalized frequency for different Q values.

Consider now the *stability analysis* of a type II, second-order loop. In order to calculate open-loop gain, we substitute active first-order loop gain [Eq. (1.10)] into PLL open-loop gain [Eq. (1.5)], and we obtian

$$H_{\text{OpenLoop}}(f) = \frac{K_d K_v}{N}\frac{1}{j2\pi f}\frac{j2\pi f\,\tau_2 + 1}{j2\pi f\,\tau_1}$$

Applying the definitions of f_n and Q from Eq. (1.11) we can write

$$H_{\text{OpenLoop}}(f) = \frac{j\frac{1}{Q}\frac{f}{f_n} + 1}{\left(j\frac{f}{f_n}\right)^2}$$

For stability analysis purposes, we need to calculate the amplitude and phase of open-loop gain. The amplitude (dB) and phase (rad) are respectively given by

$$\text{dB}\left[H_{\text{OpenLoop}}(f)\right] = 10\ \log_{10}\left[\left(\frac{1}{Q}\frac{f}{f_n}\right)^2 + 1\right] - 20\ \log_{10}\left(\frac{f}{f_n}\right)$$

$$\arg\left[H_{\text{OpenLoop}}(f)\right] = \arctan\left(\frac{1}{Q}\frac{f}{f_n}\right) - \pi$$

To check stability conditions, we will first find the unit gain frequency and then calculate the phase shift at that frequency. Let's call f_z the

frequency at which the open-loop gain amplitude is 1[†]:

$$\frac{\left(\frac{1}{Q}\frac{f_z}{f_n}\right)^2+1}{\left(\frac{f_z}{f_n}\right)^4}=1\Rightarrow\left(\frac{f_z}{f_n}\right)^4-\frac{1}{Q^2}\left(\frac{f_z}{f_n}\right)^2-1$$

$$=0\Rightarrow\underline{\underline{\left(\frac{f_z}{f_n}\right)^2=\frac{\frac{1}{Q^2}+\sqrt{\frac{1}{Q^4}+4}}{2}}}$$

The phase shift at the unit gain frequency is

$$\arctan\left(\frac{1}{Q}\frac{f_z}{f_n}\right)-\pi=\arctan\left(\frac{1}{Q}\sqrt{\frac{1}{2Q^2}+\sqrt{\frac{1}{4Q^4}+1}}\right)-\pi$$

The phase margin is

$$\text{PhaseMargin}^{\text{Active}}_{\text{SecondOrder}}(Q)=\arctan\left(\frac{1}{Q}\sqrt{\frac{1}{2Q^2}+\sqrt{\frac{1}{4Q^4}+1}}\right)$$

The phase margin is always positive for any value of Q; it tends to zero when Q tends to infinity and tends to $\pi/2$ (90°) when Q tends to zero.

From another point of view, we also know that a system is stable if all poles f_p of its closed-loop transfer function lie in the left half of the s plane; i.e., Re $(j2\pi f_p)<0$. Now poles of second-order closed-loop transfer function are the zeros of the denominator[‡] of in Eq. (1.12) or (1.13) which is:

$$\left(j\frac{f}{f_n}\right)^2+j\frac{1}{Q}\frac{f}{f_n}+1$$

Poles are given by

$$j\frac{f_p}{f_n}=j\frac{2\pi f_p}{2\pi f_n}=-\frac{1}{2}\frac{1}{Q}\pm\sqrt{\frac{Q^2}{4}-1}$$

If $Q<\frac{1}{2}$, we have two real negative distinct poles; if $Q=\frac{1}{2}$, we have two real coincident poles $jf_p/f_n=0.5/Q$; if $Q>\frac{1}{2}$, we have two complex conjugate poles having real part $0.5/Q$. In any case, since f_n and Q are positive quantities by definition, the two poles have a real part less

[†]The double underscore in the equation indicates the final result.

[‡]The denominator is a Hurwitz polynomial of the variable s (or $j2\pi f$).

than 0; thus the second-order loop is always stable. Looking at the open-loop response, we arrive at the same conclusion because $\arctan(\frac{1}{Q}\frac{f}{f_n})$ is always greater than 0 for any finite value of the frequency, and the open-loop phase shift is always less than π. Nevertheless the second-order loop can be used to demonstrate the use of two important tools for stability analysis. The first is the *Bode diagram*, on the same rectangular graph, magnitude (dB) and phase (degrees) of open-loop gain versus frequency are plotted. Normally frequency has a logarithmic scale. The phase margin can easily be found with the following procedure:

- Find the unit gain frequency; which is the frequency where the open-loop gain amplitude equals 1 (or 0 dB).
- Read the open-loop gain phase at that frequency; this is the phase shift at unit gain.
- Determine the phase margin by taking the difference between the unit gain phase shift and 180° (or −180°).

Figure 1.6*a* shows the Bode diagram of a type II (active-loop filter), second-order PLL having $Q = 1$; the frequency axis is normalized to natural frequency. The phase margin is also drawn and is about 51.8°.

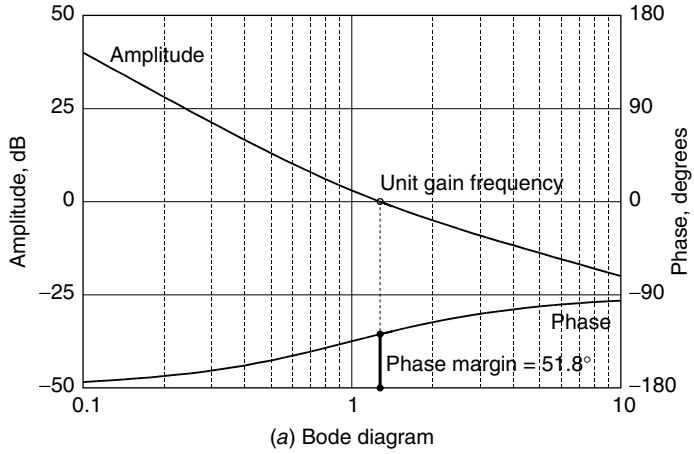
Another useful graph for stability analysis is the *Nyquist diagram*. On that diagram the imaginary part of the open-loop gain is plotted versus its real part. This is done for both positive and negative frequencies; $f \in [-\infty; +\infty]$. The PLL open-loop gain is the product of three factors: a constant function, a loop filter function, and an integrator transfer function (as mentioned in Sec. 1.3); all these factors are real positive functions of variable s. If $F_{rp}(s)$ is a real positive function of complex variable $s = \sigma + j\omega$ it implies that

$$F_{rp}(j\omega) = conjugate[F_{rp}(-j\omega)]$$

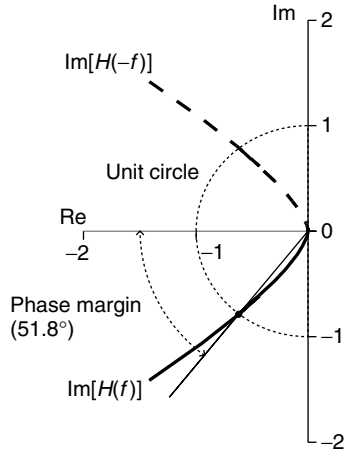
or that

$$Im[F_{rp}(j\omega)] = -Im[F_{rp}(-j\omega)]$$

Consequently the imaginary part of the open-loop gain for negative frequencies has the same plot as for the positive part but mirrored on the x axis. The Nyquist stability criterion applied to our case tells us that the PLL is stable if the curve doesn't encircle point $(-1; j0)$. Again, the phase margin is the phase shift amount that has to be added to the open-loop gain to make it encircle the point $(-1; j0)$. It is easier to read the phase margin from the Nyquist diagram than from the Bode diagram. To do so:



(*a*) Bode diagram



(*b*) Nyquist diagram

Figure 1.6 Active second-order PLL with $Q = 1$. (*a*) Bode diagram. (*b*) Nyquist diagram.

- Locate the point where the curve crosses the unit circle.
- The phase margin is the arc from this point to the x axis.

Figure 1.6*b* shows the Nyquist diagram of type II (active-loop filter), second-order PLL† having $Q = 1$; the curve for negative frequency is dashed. The phase margin is also drawn and is about 51.8°.

†Same PLL as in Fig. 1.6*a*.

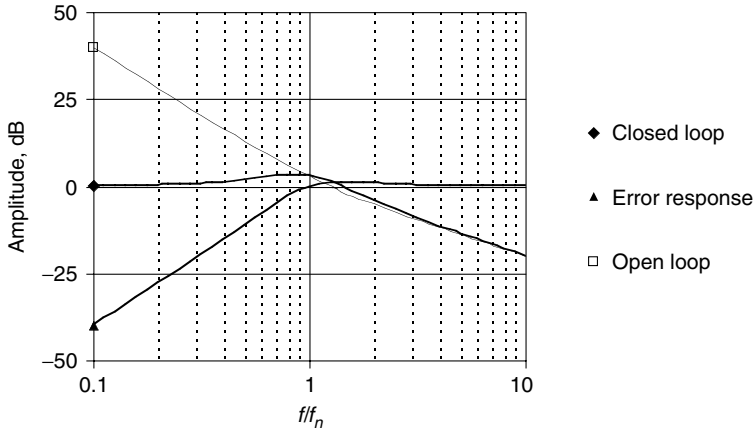


Figure 1.7 Active second-order PLL frequency responses ($Q = 1$).

Figure 1.7 shows type II second-order PLL, $Q = 1$, frequency responses: open-loop response, closed-loop response (almost coincident for $f/f_n > 3$ as anticipated in Sec. 1.5), and error response.

The closed loop[†] and error response[‡] amplitude peaks together with the phase margin versus Q are Plotted in Fig. 1.8.

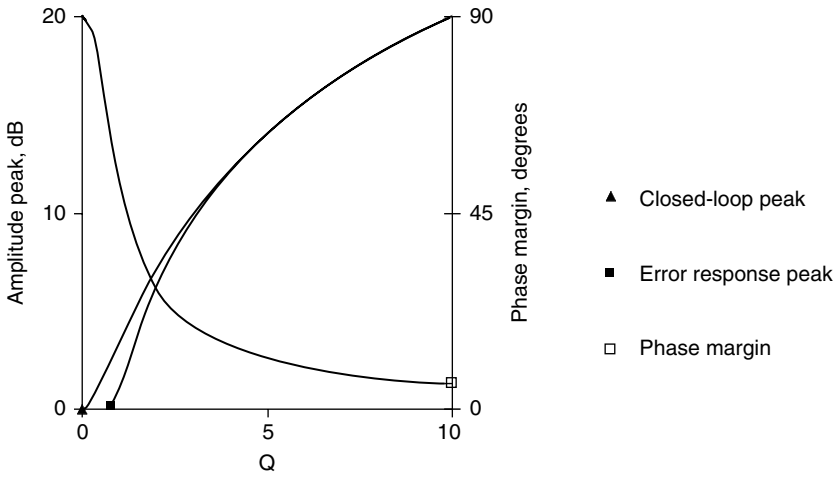


Figure 1.8 Active second-order PLL frequency response parameters.

[†]See also Table 2.1.

[‡]See also Table 2.2.

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Chapter

2

Loop Components

2.1 Introduction

This chapter is dedicated to the description of PLL elements. Detailed explanations on the design of loop components is beyond the scope of this chapter. However, descriptions of the circuits include all details needed to understand the operation of real loop components and to show the problems involved with their use. The internal operation of loop components will be examined in order to show the origin of their nonideality. Nevertheless some ideas on how to simulate circuit performance will be given. Those simulations contain all the ingredients for more complex and accurate predictions on the performances of the circuits.

The section on phase detectors describes the most used circuits: multipliers and phase frequency detectors. They are also the oldest and the newest types, respectively. Many other circuits can be used, and their descriptions can be found in the references. The circuits presented here allow us to describe the main problems coming from real phase detectors, including the sampling operation of PLLs.

A detailed description of active- and passive-loop filters is given in Sec. 2.3. The loop filter is the key element of a PLL design. It is an analog circuit; thus it is easy to analyze with a circuit simulator, but difficult to analyze with a mathematical program. For this reason closed-form equations for the response of the filters are derived. Scaling rules for loop filters are explained at the end of Sec. 2.3. Here we explain how to modify the filter in order to maintain PLL performance while changing remaining loop components or to shift the frequency response.

The description of oscillators and VCOs in Secs. 2.4 and 2.5 includes basic linear and nonlinear design techniques. The causes and quantification of phase noise, and VCO nonlinear tuning characteristics are shown.

Section 2.6 deals with variable frequency dividers. Frequency limitations and configurations with fixed and/or variable prescalers are explained. Only integer dividers are discussed; fractional dividers are described in Chap. 3.

2.2 Phase Detector

In Sec. 1.4 we described the phase detector as a block whose output is proportional to the phase difference between its two inputs. Practical phase detectors realize this function with some approximations.

2.2.1 Multiplier as phase detector

The simpler phase detector consists of an ideal multiplier; a double balanced mixer is a good approximation of it at RF and microwave frequencies. Let's consider the arrangement of Fig. 2.1*a*. The two multiplier inputs are the reference and frequency divider output signals; the output is the product of these:

$$\text{ReferenceSignal}(t) = V_r \cos\left[\theta_r(t)\right]$$

$$\text{DividerOutputSignal}(t) = V_d \cos\left[\frac{\theta_o(t)}{N}\right]$$

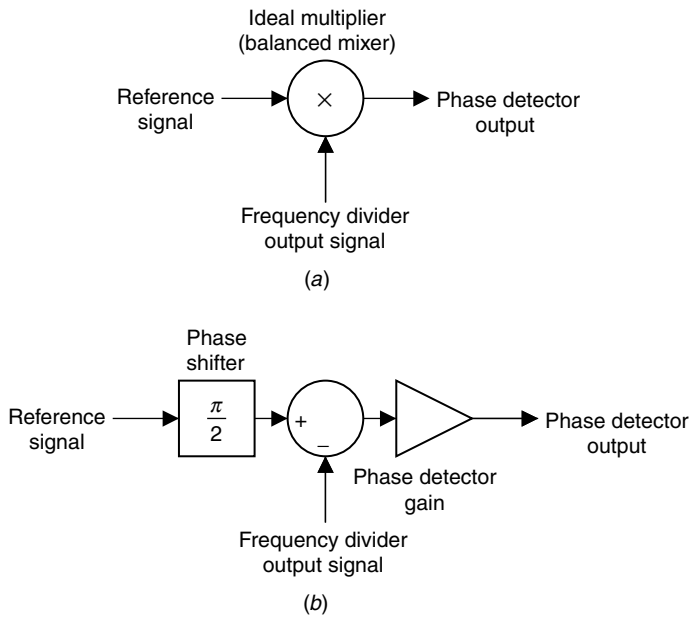


Figure 2.1 Multiplier as phase detector. (*a*) Schematic. (*b*) Linear approximation for small phase error.

where $\theta_o(t)$ is the VCO output phase and N is the frequency division factor.

$$\begin{aligned}\text{MultiplierOutput}(t) = A_m \cdot \text{ReferenceSignal}(t) \\ \times \text{DividerOutputSignal}(t)\end{aligned}$$

where A_m is the multiplier constant expressed in V^{-1}. Thus,

$$\text{MultiplierOutput}(t) = A_m V_r V_d \cos\left[\theta_r(t)\right] \cos\left[\frac{\theta_o(t)}{N}\right]$$

$$\begin{aligned}\text{MultiplierOutput}(t) = A_m \frac{V_r V_d}{2} \cos\left[\theta_r(t) - \frac{\theta_o(t)}{N}\right] \\ + A_m \frac{V_r V_d}{2} \cos\left[\theta_r(t) + \frac{\theta_o(t)}{N}\right]\end{aligned}$$

The preceding formula contains two terms, the second one being a sinusoidal function with a frequency about twice that of the reference signal; it will be filtered out by the PLL.[†] Consequently we will neglect that term and write:

$$\begin{aligned}\text{MultiplierOutput}(t) &= A_m \frac{V_r V_d}{2} \cos\left[\theta_r(t) - \frac{\theta_o(t)}{N}\right] \\ &= \underline{\underline{A_m \frac{V_r V_d}{2} \sin\left[\theta_r(t) - \frac{\theta_o(t)}{N} - \frac{\pi}{2}\right]}} \qquad (2.1)\end{aligned}$$

The multiplier output signal is proportional to the sine of the phase difference between its inputs and decreased by $\pi/2$. If

$$\left|\theta_r(t) - \frac{\theta_o(t)}{N} - \frac{\pi}{2}\right| \ll \frac{\pi}{2}$$

Eq. (2.1) can be approximated as

$$\text{MultiplierOutput}(t) \cong A_m \frac{V_r V_d}{2} \left[\theta_r(t) - \frac{\pi}{2} - \frac{\theta_o(t)}{N}\right] \qquad (2.1')$$

Within this approximation the multiplier output signal is proportional to the difference between the phase of the reference signal (delayed

[†]Remembering that the closed-loop response is lowpass, this suggests that the $H(f)$ unit gain bandwidth has to be $\ll$ than the reference frequency. Consider also that leakage signals of the reference frequency and its harmonics are present and their amplitude is difficult to predict.

by $\pi/2$) and the frequency divider output signal. Note that the phase detector gain is given by $A_m V_r V_d/2$. This means that the phase detector output depends on the signals' amplitudes too; for proper PLL operation constant amplitude has to be ensured for the reference and frequency divider output signals.

The output characteristic of the phase detector realized with the multiplier is shown in Fig. 2.2*a*. The phase detector gain $A_m V_r V_d/2$ is

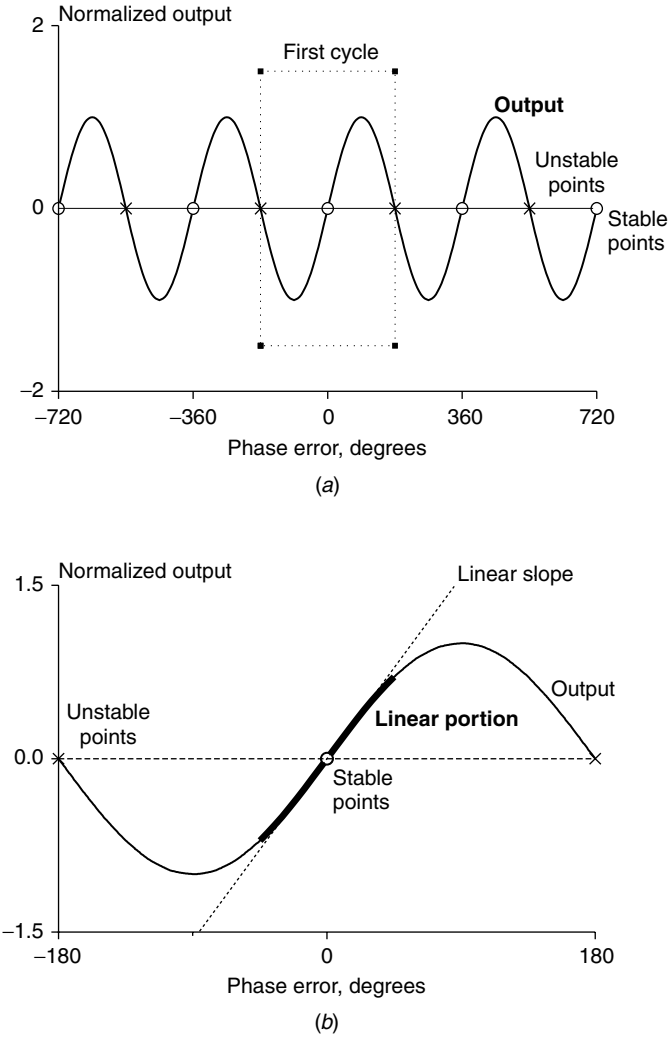


Figure 2.2 Multiplier phase detector output characteristic. (*a*) Expanded plot with many cycles of phase error. (*b*) Detail of (*a*) of first cycle region in part (*a*).

supposed to be unitary; the phase error on the abscissa is the quantity $\theta_e = \theta_r - \pi/2 - \theta_o/N$ expressed in degrees. Two series of zero-output points are shown: the first is marked with O and the phase error equals the integer multiple of 2π (360°); the other is marked with X and the phase error equals the odd integer multiple of π(180°). Points marked with O are stable points because the output slope is positive† around those points; likewise points marked with X are unstable points. Another important drawback of this phase detector realization is that its output signal can reasonably be considered proportional to the phase error only under the hypothesis of $\left|\theta_r(t) - \theta_o(t)/N - \pi/2\right| \ll \pi/2$. Figure 2.2*b* shows a close-up view of the multiplier phase detector output together with the linear output characteristic. The phase error range is $[-\pi; \pi]$, it can be seen that the multiplier output is a good approximation of the ideal one only if |Phase Error| $< \pi/4$.

The second drawback of the multiplier is its limited lock range.‡ As found, the multiplier output is the sum of two signals: One is filtered out from the PLL; the other is given by Eq. (2.1). Expressing the reference and divided VCO signals in terms of their frequencies, Eq. (2.1) can be written as

$$\text{ReferenceSignal}(t) = V_r \cos\left[2\pi \int_{-\infty}^{t} f_{\text{ref}}(\tau)\, d\tau\right]$$

$$\text{DividerOutputSignal}(t) = V_d \cos\left[2\pi \int_{-\infty}^{t} \frac{f_{\text{VCO}}(\tau)}{N}\, d\tau\right]$$

$$\text{MultiplierOutput}(t) = A_m \frac{V_r V_d}{2} \times \sin\left\{2\pi \int_{-\infty}^{t} \left[f_{\text{ref}}(\tau) - \frac{f_{\text{VCO}}(\tau)}{N}\right] d\tau - \frac{\pi}{2}\right\}$$

The multiplier output frequency is the difference between the reference frequency and the divided VCO frequency. If the VCO initial frequency is very far from the locking value (the reference frequency multiplied by N), the multiplier output is filtered out by the loop filter and has no effect on the VCO. The PLL locks only if the initial VCO frequency is within a given distance from the lock value. This topic will be discussed

†Points with positive slope are stable because if θ_e is increasing this means that θ_o is increasing, and thus the correction signal has to become negative.

‡See Sec. 4.5 for more details.

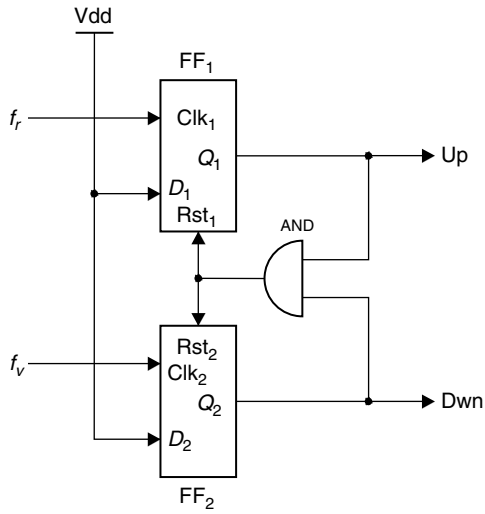


Figure 2.3 Phase frequency detector schematic.

in detail later; for now it has to be known that the PLL employing the multiplier as a phase detector has a limited lock range, so it has to be ensured someway that the initial VCO frequency is within that limit.

2.2.2 Phase frequency detector

A more advanced phase detector circuit is the *phase frequency detector* (PFD). Its schematic is shown in Fig. 2.3. It contains two "D" type flip-flops (FF_1 and FF_2) and one AND port. FF_1 and FF_2 respond to the rising edges of the input clock signals: reference applied to port f_r, and divided VCO applied to port f_v. Input signals are square waves with a low value lower than the maximum logic "0," and a high value higher than the minimum logic "1." The duty cycle is not important because FF_1 and FF_2 respond only to rising edges. Once these conditions are satisfied, the PFD output is independent from the input amplitude unlike the multiplier phase detector. Let's suppose that at the beginning FF_1 and FF_2 are in the reset state ($Q_1 = Q_2 =$ "0"). The first rising edge, from f_r (or f_v), causes FF_1 (or FF_2) to set. The next rising edge from f_v (or f_r) causes FF_2 (or FF_1) to set, but this condition of $Q_1 = Q_2 =$ "1" is momentary because it makes the AND port output become "1", resetting both FF_1 and FF_2 back to their initial conditions. Up (or Dwn)† is a very short pulse whose width equals the propagation time of the AND port plus the reset time of the flip-flop.

†Items outside of parentheses refer to f_r leading f_v or a positive phase error; items within parentheses refer to the opposite condition.

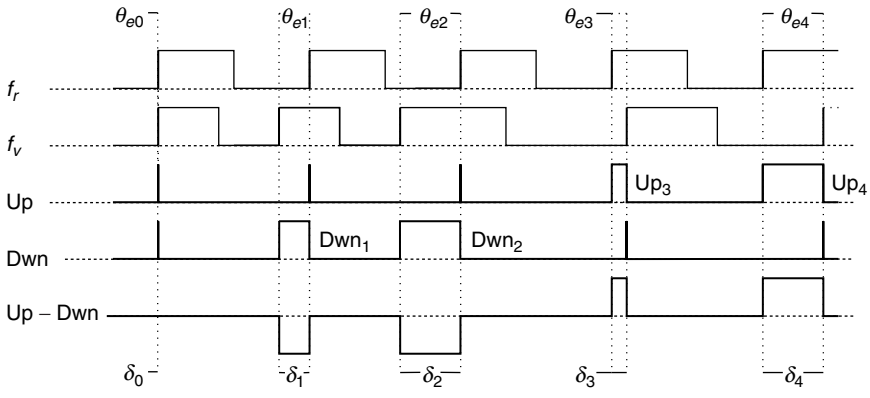


Figure 2.4 Phase frequency detector waveforms.

PFD waveforms are shown in Fig. 2.4. Three conditions are possible for phase error:

1. Positive. f_r leads f_v; see the f_r and f_v rising edges marked with θe_3 and θe_4. Up is a rectangular waveform whose width equals the time distance between the f_r and f_v rising edges; see the pulses marked with Up_3 and Up_4. Dwn is a very short pulse.
2. Negative. f_v leads f_r; see the rising edges marked with θe_1 and θe_2. Up is a very short pulse; Dwn is a rectangular waveform whose width equals the time distance between the f_v and f_r rising edges; see pulses marked with Dwn_1 and Dwn_2.
3. Zero. f_r is synchronous with f_v; see the edges marked with θe_0. Both Up and Dwn are very short pulses.

In any case the Up and Dwn low level is logic "0" voltage V_{low}, while the high logic level "1" is V_{high}. The final result is that the Up – Dwn signal is a rectangular pulse with amplitude $V_{\text{high}} - V_{\text{low}}$, which is positive (or negative) if the phase error is positive (or negative) and where the duty cycle is equal to the time distance between f_r and f_v divided by the reference period; in other words the duty cycle equals the phase error magnitude divided by 2π. Averaging that voltage, like a PLL normally does,[†] we have

$$\overline{\text{Up} - \text{Dwn}} = (V_{\text{high}} - V_{\text{low}})\frac{\theta_e}{2\pi} \tag{2.2}$$

[†]The PLL closed-loop response unit gain bandwidth has to be $\ll$ than the reference frequency as also found for the case of the multiplier phase detector.

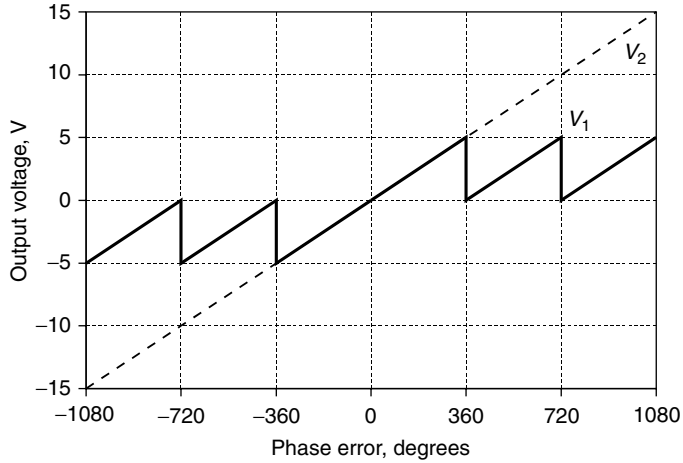


Figure 2.5 Averaged PFD (V_1) and ideal phase detector (V_2) output voltage versus phase error.

so the PFD gain is

$$K_{d,\,\mathrm{PFD}} = \frac{V_{\mathrm{high}} - V_{\mathrm{low}}}{2\pi} \tag{2.3}$$

The PFD waveforms can be calculated for any phase error using a graphic method like the one in Fig. 2.4 or by running the PFD schematic on a mixed mode circuit simulator.† The averaged output voltage Up − Dwn is shown in Fig. 2.5 where it is supposed that $V_{\mathrm{high}} = 5$ V and $V_{\mathrm{low}} = 0$ V. The closed-form analytic expression for the averaged output voltage as a function of the phase error is given by

$$\overline{\mathrm{Up} - \mathrm{Dwn}}\,(\theta_e) = \left\{ 2 \arctan\left[\tan\left(\frac{\theta_e}{2} - \frac{\pi}{2} \right) \right] + \frac{|\theta_e|}{\theta_e}\pi \right\} \frac{V_{\mathrm{high}} - V_{\mathrm{low}}}{2\pi} \tag{2.4}$$

The PFD output is linear until the phase error is within the limit $\pm 2\pi$; the multiplier phase detector linearity range is a lot narrower. Figure 2.6 compares three phase detectors with the same gain: the multiplier, PFD, and ideal one which is linear for any phase error.

The PFD has one important advantage over the multiplier. The PFD averaged output is monotonically increasing with the frequency difference between f_r and f_v if they are different. This is exactly the condition when the PLL is not locked. Then if the PLL is not locked, whatever the VCO initial frequency is, the PFD will push the output

†See the SIMETRIX file PhaseFrequencyDetector_Phase.sxsch.

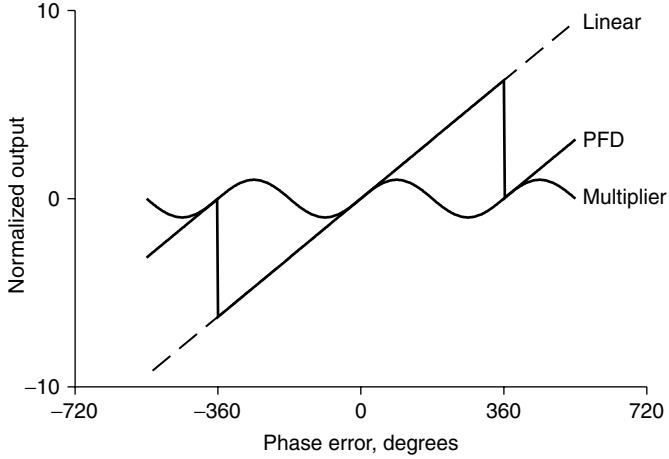


Figure 2.6 Multiplier, PFD, and linear PD output voltage versus phase error.

frequency toward the lock value. To recognize this very important property let's suppose first that the reference frequency is higher than the VCO divided one; this means that f_r has more rising edges per unit time than fv. FF_1 will be set more frequently than FF_2, while FF_1 and FF_2 are reset always simultaneously. The Up average value is higher than that of Dwn. The final result is that the higher the frequency difference between f_r and f_v, the higher the PFD average output, and vice versa. Two extreme cases are when the divided VCO frequency or reference signal is zero. In the first case FF_1 is set by the first f_v rising edge and never reset, while f_v is reset forever: Up – Dwn is a DC voltage with amplitude $V_{\text{high}} - V_{\text{low}}$. The second case can be reduced to the first by swapping f_v, FF_1, Up with f_r, FF_2, Dwn: Up – Dwn is a DC voltage with amplitude $-(V_{\text{high}} - V_{\text{low}})$. The exact computation of the PFD averaged output versus the frequency error can be done by simulating the circuit on a mixed mode simulator.† The result is shown in Fig. 2.7 where ideal complementary metal oxide semiconductor (CMOS) components have been used for simulation having $V_{\text{high}} = 5$ V and $V_{\text{low}} = 0$. The reference to divided VCO frequency ratio is plotted on a logarithmic scale; the curve is antisymmetric on that scale. Note that the PFD average output becomes $\pm(V_{\text{high}} - V_{\text{low}})/2$ for any reference to divided VCO frequency ratio a little bit greater or lower than 1 and tends to $\pm V_{\text{high}} - V_{\text{low}}$ for a frequency ratio tending to infinity or zero.

†See the SIMETRIX file PhaseFrequencyDetector_Frequency.sxsch.

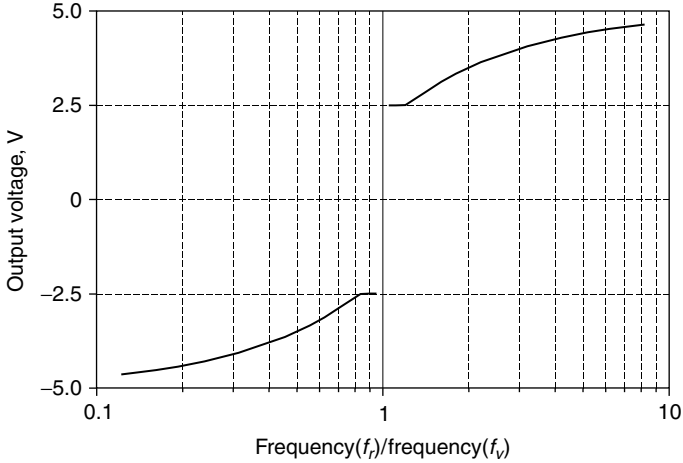


Figure 2.7 PFD averaged output voltage versus reference to divided VCO frequency ratio.

2.2.2.1 Dead zone. For very small phase errors, PFD output voltage is no longer proportional to the phase error because the PFD internal components' delay dominates the phase delay between inputs. Around zero phase error the PFD transfer characteristic is quite different from the straight line shown by Fig. 2.5 assuming more or less the aspect shown in Fig. 2.8*a*. The phase detector incremental gain is the derivative of the output voltage with respect to the phase error; it is shown in Fig. 2.8*b* together with the one of an ideal phase detector. Note that practical PFD gain for small phase error can be quite different from its nominal value: orders of magnitude higher or lower than nominal, zero, or even negative. Consequently a PLL transfer function can be quite different from the calculated one and the PLL can become unstable. This problem is known as the *dead zone* or *crossover distortion*. Unfortunately the dead zone affects the most important part of the PFD characteristic because the PLL in the lock state has zero phase error by definition. A PLL with PFD affected by crossover distortion may appear to work normally, but it is possible to momentarily see its spectrum looking like free-running VCO because the PLL is operating in open-loop mode due to the zero PFD gain. Momentary instability due to the loop gain increasing can be observed as well. The exact lock state phase error value is affected by internal PLL offsets (normally very small), so any change in their values can cause the operating point to move into points where the gain disappears or becomes very high or even negative. Some solutions have been proposed (most of the cases have been patented) to eliminate dead zone effects. One solution is to force the PLL to lock with

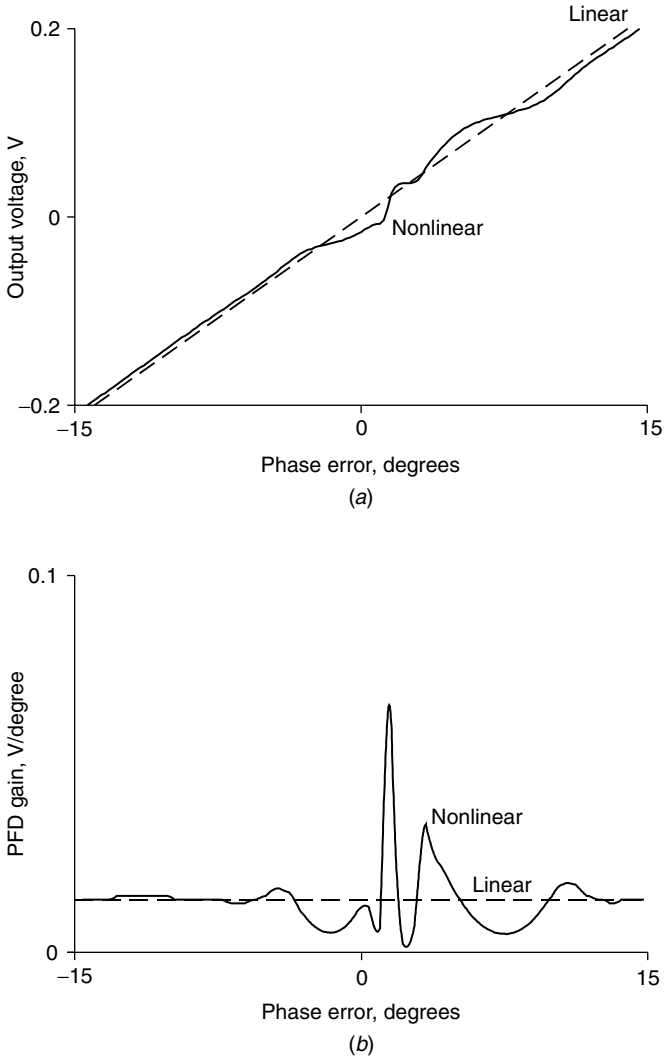


Figure 2.8 PFD with and without dead zone. (*a*) Output characteristic. (*b*) Gain.

nonzero phase error. This can be done by summing a fixed (positive or negative) offset voltage V_{FIX} to the PFD output as shown in Fig. 2.9. Referring to that schematic it can be seen that V_{det} equals zero in the lock state because the PLL has DC infinite gain. It follows that the PFD output Up − Dwn $= -V_{\mathrm{FIX}}$ and that the phase error is given by $\theta_e = \theta_r - \theta_v = V_{\mathrm{FIX}}/K_d$. This way the lock state phase error is moved out of zero and the dead zone is not used. The offset voltage has to be

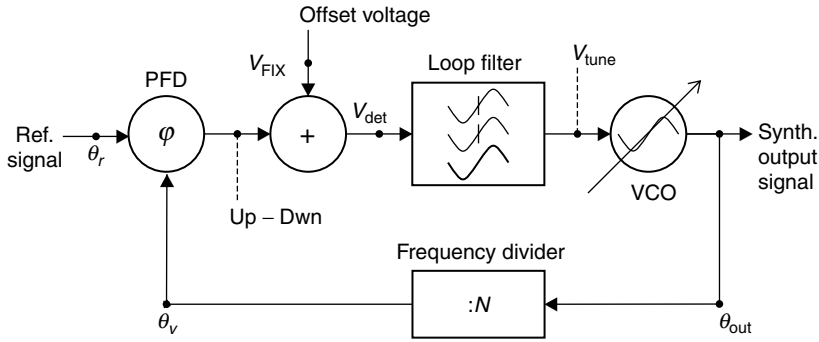


Figure 2.9 PLL with PFD and dead zone elimination circuity.

dimensioned in order to pull the operating point out of the dead zone.

$$\theta_{e,\,\mathrm{LOCKED}} = V_{\mathrm{FIX}}\frac{1}{K_d} = V_{\mathrm{FIX}}\frac{2\pi}{V_{\mathrm{high}} - V_{\mathrm{low}}} \Rightarrow V_{\mathrm{FIX}}$$

$$= \frac{\theta_{e,\,\mathrm{LOCKED}}}{2\pi}(V_{\mathrm{high}} - V_{\mathrm{low}})$$

The phase error in the lock state must be high enough to make the PLL work outside of the dead zone; e.g., the phase error amplitude has to equal the dead zone amplitude plus some margin.

$$V_{\mathrm{FIX}} = \frac{\theta_{e,\,\mathrm{LOCKED}}}{2\pi}(V_{\mathrm{high}} - V_{\mathrm{low}}) = \frac{\theta_{\mathrm{DeadZone}} + \theta_{\mathrm{Margin}}}{2\pi}(V_{\mathrm{high}} - V_{\mathrm{low}})$$

$$= \frac{\theta_{\mathrm{safety}}}{2\pi}(V_{\mathrm{high}} - V_{\mathrm{low}})$$

Expressing the phase in degrees, we obtain

$$V_{\mathrm{FIX}} = \frac{\Theta_{\mathrm{safety,\,degrees}}}{360}(V_{\mathrm{high}} - V_{\mathrm{low}}) \tag{2.5}$$

2.2.2.2 PFD spurs. As discussed, the PFD output is the difference between two rectangular waves: Up and Dwn. Ideally, in the lock state, Up and Dwn are two identical periodic rectangular waveforms having a fundamental frequency equal to reference one (f_{ref}), an amplitude equal to the difference between the "1" and "0" state flip-flop voltage ($V_{\mathrm{high}} - V_{\mathrm{low}}$), and a very short pulse width. Thus the ideal PFD output voltage is a perfect zero in the lock state. The practical case is different because the Up and Dwn pulses are not perfectly simultaneous; they have different amplitudes and pulse widths. The resulting waveform still has a zero average value but with a superimposed pseudo-rectangular waveform whose fundamental period equals the reference

signal period. The PLL output spectrum is modulated by the reference signal residual which can only be filtered by the loop filter. Some nonidealities on the PFD signals Up and Dwn can be present. Three nonideal cases together with perfectly balanced PFD are shown in Fig. 2.10; real cases are combinations of them.

- Figure 2.10*a* shows the ideal case. Up and Dwn are two identical rectangular waves with periods equal to the reference signal. The PFD out voltage is perfectly zero.
- Figure 2.10*b* shows the first kind of degradation of perfectly balanced PFD. Up and Dwn are like case (*a*) but there is a nonzero delay between them. The PFD out voltage still has a zero average value but with positive and negative rectangular pulses superimposed.
- Figure 2.10*c* shows the case of Up and Dwn with different amplitudes. The PFD average output has to be zero in the lock state; it follows that Up and Dwn will have different pulse widths to maintain a zero average output.
- Figure 2.10*d* shows the important case of offset applied to PFD output. This situation is very often present in PLLs and is intentionally caused when dead zone elimination offset is applied. If the arrangement in Fig. 2.9 is used, the PFD average value is no longer zero. It follows that the Dwn (or Up) signal presents wider pulses if $V_{\mathrm{FIX}} > 0$ (or $V_{\mathrm{FIX}} < 0$), while the Up (or Dwn) signal has very short pulses (ideally of zero width).

In any case the PFD output is periodic with period $1/f_{\mathrm{ref}}$, and its spectrum can be calculated by using Fourier series expansion. The most interesting case is that of the dead zone. The PFD harmonic amplitude can be calculated as follows.

Let's assume $V_{\mathrm{FIX}} < 0$. Then the PFD output voltage in one period is given by

$$\mathrm{PFD}_{\mathrm{out}}(t)_{t\in[0;T_{\mathrm{ref}}]} = \mathrm{if}\,(t < \delta_T, V_{\mathrm{high}} - V_{\mathrm{low}}, 0)$$

To find δT we set the PFD average value equal to V_{FIX}:

$$\begin{aligned}\frac{1}{T_{\mathrm{ref}}}\int_0^{T_{\mathrm{ref}}} \mathrm{PFD}_{\mathrm{out}}(t)\,dt &= \frac{1}{T_{\mathrm{ref}}}\int_0^{\delta T}(V_{\mathrm{high}} - V_{\mathrm{low}})\,dt \\ &= \frac{\delta T}{T_{\mathrm{ref}}}(V_{\mathrm{high}} - V_{\mathrm{low}}) = V_{\mathrm{FIX}} \\ \delta T &= \frac{V_{\mathrm{FIX}}}{V_{\mathrm{high}} - V_{\mathrm{low}}}T_{\mathrm{ref}} = \frac{\Theta_{\mathrm{DegreesSafety}}}{360}T_{\mathrm{ref}}\end{aligned}$$

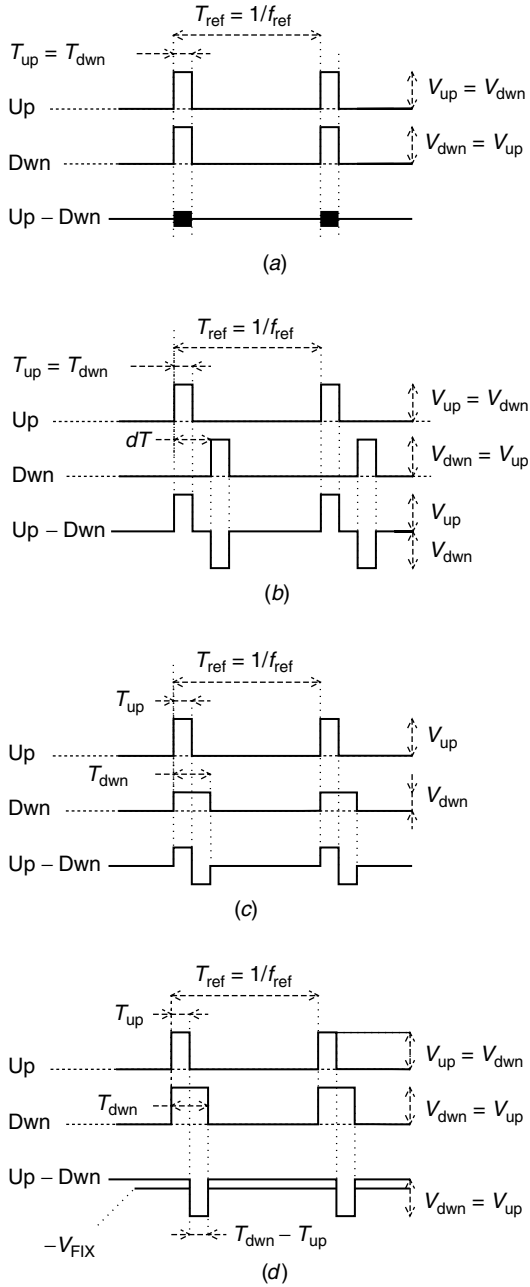


Figure 2.10 PFD output in lock state nonidealities. (*a*) Ideal case, (*b*) Up – Dwn delay, (*c*) unequal amplitude/width, (*d*) offset applied.

The PFD output voltage expansion in Fourier series is given by

$$\mathrm{PFD}_{\mathrm{out}}(t) = \sum_{k=0}^{\infty} a_k \sin(k2\pi f_{\mathrm{ref}} t) + b_k \cos(k2\pi f_{\mathrm{ref}} t)$$

where the Fourier coefficients are given by

$$\begin{aligned} b_0 &= \frac{1}{T_{\mathrm{ref}}} \int_0^{T_{\mathrm{ref}}} \mathrm{PFD}_{\mathrm{out}}(t)\, dt = V_{\mathrm{FIX}} \\ b_{k>0} &= \frac{1}{T_{\mathrm{ref}}} \int_0^{T_{\mathrm{ref}}} \mathrm{PFD}_{\mathrm{out}}(t) \cos(k2\pi f_{\mathrm{ref}} t)\, dt \\ &= \frac{V_{\mathrm{high}} - V_{\mathrm{low}}}{T_{\mathrm{ref}}} \int_0^{\delta T} \cos(k2\pi f_{\mathrm{ref}} t)\, dt \\ a_k &= \frac{1}{T_{\mathrm{ref}}} \int_0^{T_{\mathrm{ref}}} \mathrm{PFD}_{\mathrm{out}}(t) \sin(k2\pi f_{\mathrm{ref}} t)\, dt \\ &= \frac{V_{\mathrm{high}} - V_{\mathrm{low}}}{T_{\mathrm{ref}}} \int_0^{\delta T} \sin(k2\pi f_{\mathrm{ref}} t)\, dt \end{aligned}$$

The nth($n > 0$) harmonic amplitude is given by

$$c_n = \sqrt{a_n^2 + b_n^2} = \frac{2}{\pi} \frac{\sin\left(n \frac{\Theta_{\mathrm{DegreesSafety}}}{360} \pi\right)}{n} (V_{\mathrm{high}} - V_{\mathrm{low}}) \tag{2.6}$$

The low-order harmonic approximate amplitude expression is

$$c_n \cong \frac{\Theta_{\mathrm{DegreesSafety}}}{180} (V_{\mathrm{high}} - V_{\mathrm{low}}) = 2V_{\mathrm{FIX}} \tag{2.6'}$$

Reference harmonic spurs modulate the VCO causing the PLL spectrum to be affected by side tones that are spaced out by the reference frequency around the carrier. Figure 2.11 shows the output spectrum of a PLL having an output frequency of 200 MHz and a reference frequency of 10 MHz. The amplitude of the reference spurs is about 60 dB below the carrier.

2.2.2.3 Charge pump. The PFD needs the circuit of Fig. 2.3 plus an additional circuit for generating the voltage difference Up − Dwn. Many modern PLLs use another approach; they generate a current rather than a voltage proportional to the phase error. A PFD with current output is also known as a *charge pump* (CP). The basic schematic is shown in Fig. 2.12*a*. TR_1 and TR_2 are complementary P and N channel transistors; they are used as the on/off modulated current source and sink, respectively. More in detail, when Up (which is the same signal as Q_1)

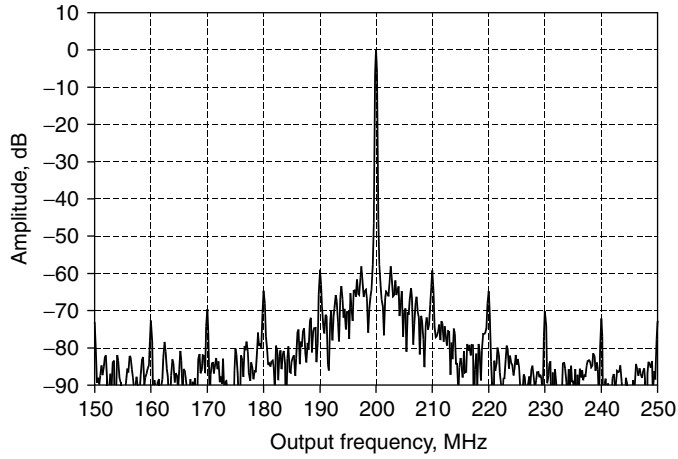


Figure 2.11 PLL output spectrum with reference spurs.

is high, the TR_1 gate-source voltage is −Vdd; thus TR_1 is conducting, and a positive current flows from output to GND; when Up (and thus Q_2) is high, the TR_2 gate-source voltage becomes Vdd making the TR_2 remove current from the output. Four combinations are possible:

1. Both TR_1 and TR_2 are on. The output current is close to (but not equal to) zero because the currents generated from TR_1 and TR_2 are very close (but not identical, which is the ideal case). Looking at the waveforms illustrated in Fig. 2.4, it is possible to observe that Up

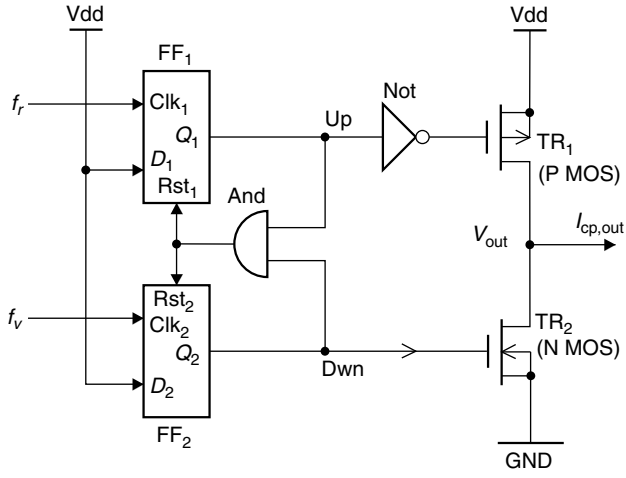


Figure 2.12 Charge pump phase detector.

and Dwn are simultaneously high only for a very short time, so this condition is not frequent.

2. Both TR_1 and TR_2 are off. The output current is zero. This is the most frequently used condition, particularly when the PLL is locked.
3. TR_1 is on and TR_2 is off. This happens when the phase error is positive: A positive current rectangular pulse flows through the output; its width equals the phase delay between inputs, and its amplitude equals the saturated drain current of TR_1, $Idss_1$.
4. TR_1 is off and TR_2 is on. This happens when the phase error is negative. A negative current rectangular pulse flows through the output (or there is a current sink from the output), its width equals the magnitude of the phase delay between inputs, and its amplitude (<0) equals the saturated drain current of TR_2, $Idss_2$.

If the PLL is locked, condition 2 occurs for most of the time and condition 1 for the rest of the time. If PLL is not locked, combinations of conditions 2 and 3 or 2 and 4 occur depending on the phase error between the CP inputs. Providing that TR_1 and TR_2 are as complementary as possible, i.e., $Idss_1 = Idss_2 = Idss$, we will have zero output current when the PLL is locked. In that condition, the CP will generate short rectangular current pulses having a width equal to the phase delay between the CP inputs (the time delay between the f_r and f_v rising edges), an amplitude equal to Idss, and the same sign as that of the phase error. In other words we can write the CP average output current expression as

$$\overline{I_{\text{cp,Out}}} = \text{Idss}\frac{\theta_e}{2\pi} \tag{2.7}$$

It is possible to define a phase detector current gain as

$$K_{di} = \frac{\text{Idss}}{2\pi} \tag{2.8}$$

The output current versus phase error and frequency error are the same functions found for the voltage output PFD [see Eq. (2.4) and Figs. 2.6 and 2.7]. The only change that has to be made is replacing the voltage amplitude factor $V_{\text{high}} - V_{\text{low}}$ with the current amplitude factor Idss. The timing diagrams of Figs. 2.4 and 2.10 are still valid if we replace Up – Dwn with I_{out}, V_{up} with $Idss_1$, and V_{dwn} with $Idss_2$ on the bottom waveform. Same considerations can be applied also for the dead zone and reference spurs. The dead zone can be pulled out by adding an offset current (instead of a voltage offset); this can be easily done by adding a fixed shunt current generator between the output and GND or V_{dd}.

We must consider one last thing regarding the charge pump: TR_1 and TR_2 operation reasonably approximates current generators until

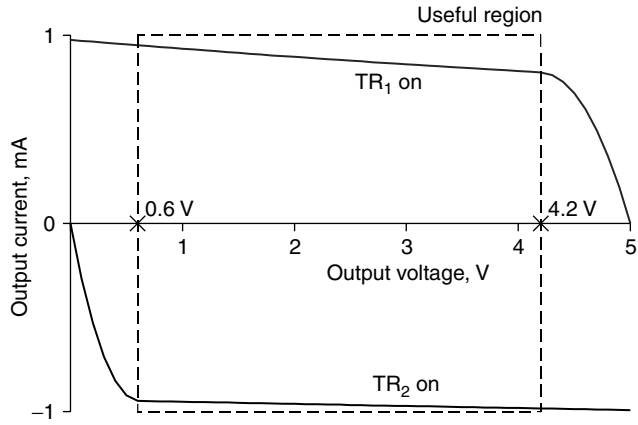


Figure 2.13 Charge pump output current.

the drain-source voltage magnitude is higher than a given minimum value. Output current versus output voltage is shown in Fig. 2.13 where a charge pump current Idss a little bit less than 1 mA is assumed. Conditions 3 and 4 are represented. Note that both transistors' output characteristics approximate the current generators (horizontal lines) only if the output voltage is within the current saturation region of both TR_1 and TR_2 (between about 0.6 and 4.2 V in the plotted example). The PLL will work as expected only if the CP output voltage is within its valid range.

2.2.2.4 Sampled PLL. One of the most important peculiarities of the PFD is that unlike that of the multiplier, its output changes only in correspondence with rising edges of input signals. The output voltage or current can be considered proportional to a "sampled" phase error signal. Mathematical implications of this kind of situation will be discussed in the following. The PFD output is a rectangular pulse with constant amplitude and a width equal to the phase delay between inputs. Continuous-time approximation (the one used most) consists of replacing output waveforms with their average value or DC component. That approximation can be applied because of averaging due to the loop filter whose bandwidth is much lower than that of the reference frequency. A more accurate approximation can be obtained by replacing PFD rectangular pulses with Dirac pulses having the same area. In other words, rectangular pulses with constant amplitude and variable width are replaced by ideal pulses with constant (zero) width and variable amplitude; the average output is the same because of the Dirac pulse definition. In the lock state, the PFD output pulse width becomes

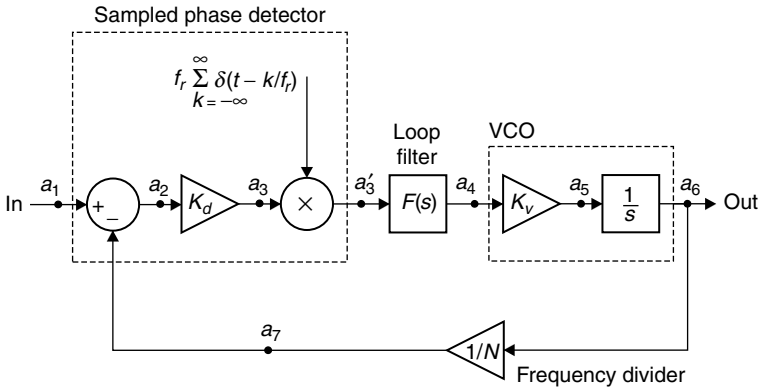


Figure 2.14 PLL with sampling schematization of PFD.

very short. The proposed approximation becomes more accurate as the PLL approaches the lock state (which is the most important state). A PLL with the new schematization of PFD is shown by Fig. 2.14. The PFD is schematized with an ideal phase detector whose output is a direct current proportional to the phase error followed by a multiplier by a periodic sequence of Dirac pulses. The sampling sequence frequency equals the reference frequency. The area of each individual pulse is equal to the reference frequency so that the input and output of the sampler have the same DC component. The PLL closed-loop frequency response taking into account sampling effects can be determined by using the following block diagram equations.
Sampled phase detector output (node a_3'):

$$\mathrm{PFD}^*_{\mathrm{out}}(f) = K_d \left[\Theta_r(f) - \Theta_o(f)\frac{1}{N}\right]^*$$

PLL output (node a_6):

$$\Theta_o(f) = \mathrm{PFD}^*_{\mathrm{out}}(f)\frac{F(j2\pi f)}{j2\pi f}K_v$$

Substituting the PLL output expression into the sampled PFD one and applying the following properties of sampled functions:

$$[\mathrm{Constant}G(f)]^* = \mathrm{Constant}[G(f)]^*$$
$$[G_1(f)G_2(f)]^* = [G_1(f)]^*\,[G_2(f)]^*$$
$$[G(f)]^* = \left\{[G(f)]^*\right\}^*$$

we obtain

$$\mathrm{PFD}^*_{\mathrm{out}}(f) = \frac{K_d}{1 + \frac{K_d K_v}{N}\left[\frac{F(j2\pi f)}{j2\pi f}\right]^*}[\Theta_r(f)]^*$$

Finally substituting the PFD output into the PLL output, we obtain

$$\Theta_o(f) = N\frac{\frac{K_d K_v}{N}\frac{F(j2\pi f)}{j2\pi f}}{1 + \frac{K_d K_v}{N}\left[\frac{F(j2\pi f)}{j2\pi f}\right]^*}[\Theta_r(f)]^* \tag{2.9}$$

Let's write explicit expressions of time sampled functions. The Fourier transform of time sampled functions is given by

$$[G(f)]^* = \mathscr{F}\left[g(t) f_r \sum_{k=-\infty}^{+\infty} \delta\left(t - \frac{k}{f_r}\right)\right] = \sum_{k=-\infty}^{+\infty} G(f - k\, f_r)$$

where $\delta(t)$ is the unitary area Dirac pulse at $t = 0$, and f_r is the reference frequency. The ideal sampling in the time domain causes the corresponding Fourier transform to be composed of an infinite number of aliases, each centered on an integer multiple of the sampling frequency. The Fourier transform of a time sampled signal is periodic over the frequency with the period given by the sampling frequency. For this reason, sampled Fourier transforms have to be evaluated over a frequency range from zero to the sampling frequency rather than from $-\infty$ to $+\infty$. For practical purposes the infinite terms of the sampled Fourier transforms can be replaced with a truncated sum:

$$\begin{aligned}[G(f)]^* &= \mathscr{F}\left[g(t) f_r \sum_{k=-\infty}^{+\infty} \delta\left(t - \frac{k}{f_r}\right)\right] \\ &= \sum_{k=-\infty}^{+\infty} G(f - k f_r) \cong \sum_{k=-N_{\mathrm{alias}}}^{+N_{\mathrm{alias}}} G(f - k f_r)\end{aligned}$$

The preceding equation shows that the Fourier transform of a time sampled function includes an infinite number of terms (see third expression). We replace the infinite sum with an approximated expression containing a finite number of terms, $\mathrm{N_{alias}}$, which is found by imposing the condition that the difference

$$\left| \sum_{k=-(N_{\mathrm{alias}}+1)}^{N_{\mathrm{alias}}+1} G(f - k f_r) - \sum_{k=-N_{\mathrm{alias}}}^{+N_{\mathrm{alias}}} G(f - k f_r) \right|$$

has to be lower than a specified value within the range from zero to the sampling frequency. Equation (2.9) can also be written as

$$\Theta_o(f) = N \frac{\frac{K_d K_v}{N} \frac{F(j2\pi f)}{j2\pi f}}{1 + \frac{K_d K_v}{N} \sum_{k=-\infty}^{+\infty} \frac{F[j2\pi(f - kf_r)]}{j2\pi(f - kf_r)}} \sum_{k=-\infty}^{+\infty} \Theta_r[j2\pi(f - kf_r)] \tag{2.9'}$$

The closed-loop frequency response, taking into account sampling effects, is

$$H_{\text{sampled}}(f) = \frac{\frac{K_d K_v}{N} \frac{F(j2\pi f)}{j2\pi f}}{1 + \frac{K_d K_v}{N} \sum_{k=-\infty}^{+\infty} \frac{F[j2\pi(f - kf_r)]}{j2\pi(f - kf_r)}} \tag{2.10}$$

The numerators of the sampled and continuous-time PLL closed-loop gains coincide [compare Eq. (2.10) to Eq. (1.3)]. The continuous-time PLL gain denominator is one plus the numerator, while the sampled time denominator is one plus the sampled numerator. Regarding stability analysis, in general the phase margin predicted taking into account sampling effects is smaller than the phase margin calculated using continuous-time approximation. PLL stability can be checked by calculating the poles of the closed-loop frequency response. Generalizing what we found in Sec. 1.6, it is possible to say that the denominator of Eq. (2.10) (the sampled approximation):

$$1 + \frac{K_d K_v}{N} \sum_{k=-\infty}^{+\infty} \frac{F[j2\pi(f - kf_r)]}{j2\pi(f - kf_r)}$$

plays the same role as the denominator of Eq. (1.3) (continuous time approximation):

$$1 + \frac{K_d K_v}{N} \frac{F(j2\pi f)}{j2\pi f}$$

Then the phase margin for the sampled PLL can be calculated from the Bode or Nyquist diagram of the factor

$$\frac{K_d K_v}{N} \sum_{k=-\infty}^{+\infty} \frac{F[j2\pi(f - kf_r)]}{j2\pi(f - kf_r)}$$

instead of the factor

$$\frac{K_d K_v}{N} \frac{F(j2\pi f)}{j2\pi f}$$

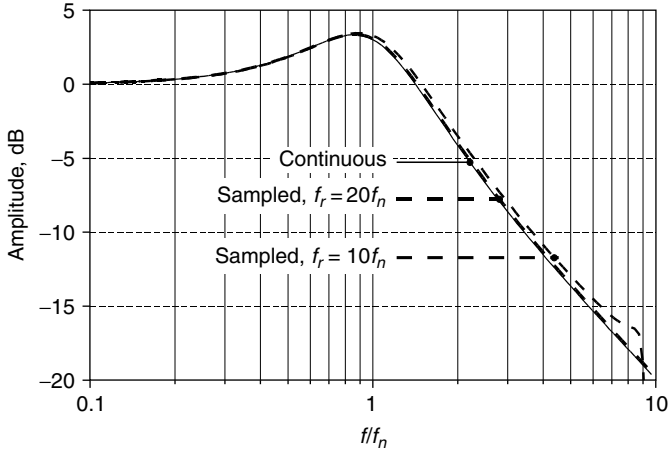


Figure 2.15 Continuous-time and sampled PLL closed-loop frequency responses (second-order, type II, $Q = 1$).

which is used for continuous-time approximation. One example[†] was considered of type II second-order PLL with $Q = 1$, $f_n = f_r/10$, and $f_n = f_r/20$. Closed-loop frequency responses calculated with Eq. (1.3) and Eq. (2.10) truncated to Nalias = 11 are plotted in Fig. 2.15. The curve for $f_n = f_r/20$ is hardly distinguished by the curve for the continuous-time approximation (the difference is less than 0.2 dB up to $f/f_n = 10$). The phase margin has been calculated with some different number of alias terms. The result is shown in Table 2.1. In the worst case of $f_n = f_r/10$ there is a phase margin degradation of about 3°; it is less than 1° when $f_n = f_r/20$. The general concept coming out of this consideration is that continuous-time calculation is a good approximation for the PLL closed-loop frequency response providing that the closed-loop unit gain bandwidth is $\ll$ than the sampling frequency. With this assumption, Eq. (2.9′) can be written as

$$\Theta_o(f) \cong NH(f) \sum_{k=-\infty}^{+\infty} \Theta_r[j2\pi(f - kf_r)] \tag{2.11}$$

Equation (2.11) states that the PLL output spectrum is not only given by the reference spectrum close to the reference frequency (about plus or minus the PLL closed-loop bandwidth around the reference frequency) but also by the reference spectrum around the integer multiple of the carrier frequency, because of folding back into the reference frequency due to sampling effects.

[†]See the MATHCAD file SecondOrderSampledPLL.MCD.

TABLE 2.1 Type II, Second-Order PLL ($Q = 1$) Phase Margin Calculations

		Sampled	
N_{alias}	Continuous time	$f_n = 20 f_r$	$f_n = 10 f_r$
3		51.160	49.140
5		51.111	48.944
7	51.827	51.087	48.852
9		51.074	48.799
15		51.054	48.721

2.3 Loop Filter

The basic properties of the loop filter have already been defined in Sec. 1.4 by Eq. (1.4); the loop order and type classification in finite or infinite DC gain (types I and II) were defined in Sec. 1.5. Some simple loop filter types were discussed in Secs. 1.6 and 1.7.

2.3.1 Reference spur filtering

From the discussion about phase detectors in Sec. 2.2, we know that practical phase detectors present at their output not only a signal proportional to the phase error but also residuals of the reference signal and its harmonics. One of the requirements for the loop filter is that it has to filter out reference spurs in order to prevent frequency modulation of the VCO.

In order to calculate the effect of phase detector spurs on the PLL output spectrum, we can modify the block diagram of Fig. 1.2*a* by the addition of a signal to the phase detector output. This is done in Fig. 2.16. Referring to that schematic, the PLL output phase is given by a sum of two terms, one due to the reference signal, the other to the reference

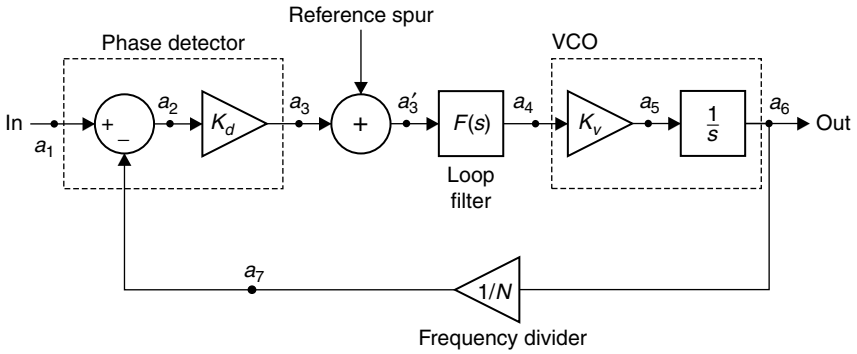


Figure 2.16 PLL block diagram including phase detector spurs.

spur. Both terms are weighted by their own transfer function. Those weighting functions can be calculated by applying Mason's rule, which states that on a feedback system the contribution of an input to the output is filtered by the gain from that input to output divided by one plus the total loop gain. The PLL output phase is then

$$\Theta_o(s) = N\frac{\frac{K_d K_v}{N}\frac{F(s)}{s}}{1+\frac{K_d K_v}{N}\frac{F(s)}{s}}\Theta_r(s) + \frac{N}{K_d}\frac{\frac{K_d K_v}{N}\frac{F(s)}{s}}{1+\frac{K_d K_v}{N}\frac{F(s)}{s}}\,\text{ReferenceSpur}(s) \tag{2.12}$$

It is clearly possible to recognize that reference spurs and reference phase contributions to the output spectrum are filtered by functions depending on frequency in the same way, just with a different multiplying constant. Both functions are proportional to the PLL closed-loop transfer function. Passing from the Laplace variable to the frequency, we can say that reference spurs are filtered by the PLL closed-loop frequency response given by Eq. (1.3) multiplied by the frequency division factor and divided by the phase detector gain, as given in the following formula:

$$\text{ReferenceSpurFiltering}(f) = \frac{N}{K_d}H(f) = \frac{N}{K_d}\frac{\frac{K_d K_v}{N}\frac{F(j2\pi f)}{j2\pi f}}{1+\frac{K_d K_v}{N}\frac{F(j2\pi f)}{j2\pi f}} \tag{2.13}$$

Considering the direct path from the reference spur to the output, the reference spur weighting function is

$$K_v\frac{F(j2\pi f)}{j2\pi f}$$

This latter determination is a good approximation of the exact formula (2.13) when the loop gain magnitude is $\ll 1$ as it normally is at frequencies higher than the reference frequency.

$$\left.\frac{N}{K_d}H(f)\right| \cong \frac{N}{K_d}\frac{K_d K_v}{N}\frac{F(j2\pi f)}{j2\pi f} = K_v\frac{F(j2\pi f)}{j2\pi f}$$
$$\text{if} \quad \left|\frac{K_d K_v}{N}\frac{F(j2\pi f)}{j2\pi f}\right| \ll 1$$

The multiplying factor N/K_d is independent from the loop filter, so closed-loop responses with different loop filters have to be compared in order to evaluate the loop filter effectiveness in cutting out reference spurs. When we described loop filters in Chap. 1, we saw that the zero-order PLL transfer function is completely characterized by

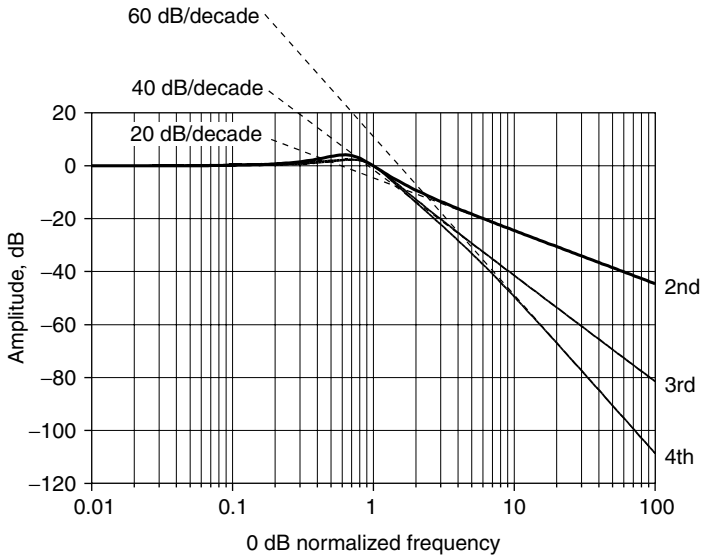


Figure 2.17 Second-, third-, and fourth-order PLL closed-loop gains.

its only parameter, which is natural frequency, and that second-order PLL is characterized by the natural frequency and the damping factor. As the PLL order increases, the number of free parameters will increase accordingly, but it is difficult to find a physical interpretation for their meaning. The concepts of closed-loop unit gain bandwidth and phase margin were introduced in Sec. 1.7. Those concepts can be usefull when comparing the filtering action of PLLs with different orders. Figure 2.17 shows the magnitudes of closed-loop frequency responses of three PLLs (second, third, and fourth order) having the same unit gain frequency and phase margin (45°). Note that the unit gain frequency and the phase margin completely identify the second-order PLL transfer function, while higher-order PLLs have a higher number of free parameters, so they have many frequency responses with the same closed-loop bandwidth and the same phase margin. Figure 2.17 shows one among the infinite possible frequency responses. Three functions are plotted versus frequency normalized to the unit gain frequency, so their amplitudes are unitary at a normalized frequency of 1. Figure 2.17 clearly shows that the higher the PLL order, the higher the spur reference attenuation. The asymptotic attenuation is given by

$$\text{Slope} = 20\ (\text{PLL}_{\text{order}} - 1)\ \text{dB/decade}$$

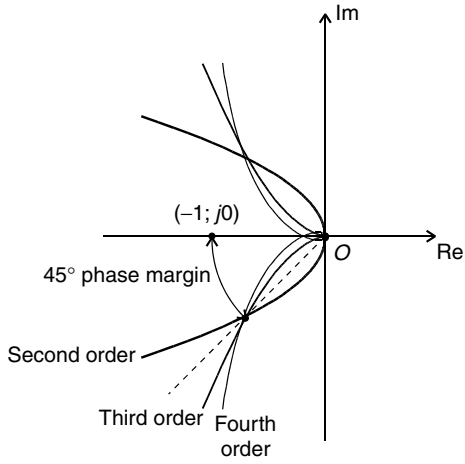


Figure 2.18 Second-, third-, and fourth-order PLL Nyquist diagram.

Consequently, the higher the PLL order, the higher the reference spur attenuation. Figure 2.18 shows the Nyquist diagram of the PLL of Fig. 2.17. The phase margin for all PLLs is 45°.

2.3.2 Loop filters for voltage output phase detectors

First-order loop filters were presented in Sec. 1.7. Going back to the active first-order loop filter of Fig. 1.3*b*, we can now see that the unit gain inverting amplifier can be omitted when a multiplier phase detector is used, because the inverting loop filter transfer function sign there is just a swap between stable and unstable zero outputs (see Fig. 2.2*a*). A schematic of the basic loop filter for the voltage output PFD is shown in Fig. 2.19. When the PFD is used, the loop filter input signal has to be the voltage difference, Up − Dwn, so the circuit of Fig. 2.3 is not complete; a difference amplifier has to be inserted between the PFD outputs and the loop filter input (the loop filter can be one of those in Fig. 1.3). Figure 2.19*a* shows a more clever solution; one single operational amplifier (opamp) and some passive components perform difference and filtering functions. The filter output is given by

$$V_{\text{out}} = \left(1 + \frac{Z_2}{R_1}\right) \frac{Z_2'}{R_1' + Z_2'} \text{Up} - \frac{Z_2}{R_1} \text{Dwn}$$

$$= \frac{R_1 + Z_2}{R_1} \frac{Z_2'}{R_1' + Z_2'} \text{Up} - \frac{Z_2}{R_1} \text{Dwn}$$

if

$$\frac{R_1 + Z_2}{R_1} \frac{Z_2'}{R_1' + Z_2'} = \frac{Z_2}{R_1} \Rightarrow \frac{R_1'}{Z_2'} = \frac{R_1}{Z_2}$$

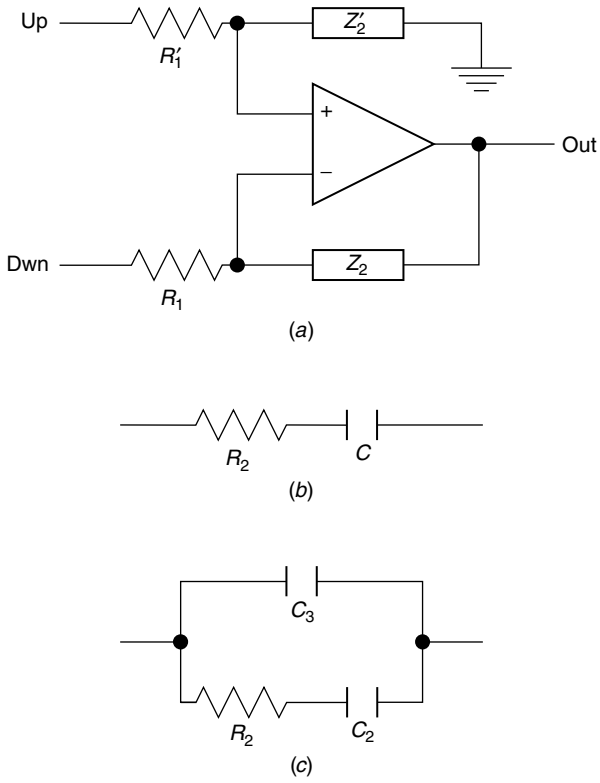


Figure 2.19 Loop filters for a PFD. (*a*) Filter schematic, (*b*) Z_2 and Z_2' for a second-order PLL, (*c*) Z_2 and Z_2' for a third-order PLL.

(This balancing condition is in particular satisfied if $R_1 = R_1'$ and $Z_2 = Z_2'$). Then the output becomes

$$V_{\text{out}} = \left(1 + \frac{Z_2}{R_1}\right)\left(1 + \frac{R_1'}{Z_2'}\right)^{-1} \text{Up} - \frac{Z_2}{R_1}\text{Dwn}$$

$$= \frac{1 + \frac{Z_2}{R_1}}{1 + \frac{Z_2'}{R_1'}} \frac{Z_2'}{R_1'} \text{Up} - \frac{Z_2}{R_1}\text{Dwn} = \underline{\underline{\frac{Z_2}{R_1}(\text{Up} - \text{Dwn})}} \qquad (2.14)$$

Equation (2.14) states that the output voltage equals the difference between inputs filtered by the factor Z_2/R_1.

Filters configured as in Fig. 2.19 are particularly suited for a PFD because they perform difference and filtering actions simultaneously. Anyway they can still be used with a multiplier phase detector after removing R_1' and Z_2' and connecting the opamp noninverting input to

ground: The same transfer function with the opposite sign will be obtained. Three particular cases will be considered.

1. Z_2 is a simple resistor, the transfer function is a constant, and we have a first-order PLL.
2. See Fig. 2.19*b*. Z_2 is a series RC (like in Fig. 1.3). The frequency response has the same expression as Eq. (1.11). The PLL is thus second-order.

$$V_{\text{out}} = \frac{j2\pi f\, CR_2 + 1}{j2\pi f\, CR_1}(\text{Up} - \text{Dwn}) = \frac{j2\pi f\, \tau_2 + 1}{j2\pi f\, \tau_1}(\text{Up} - \text{Dwn}) \tag{2.15′}$$

3. See Fig. 2.16*c*. Z_2 is a series RC with one capacitor in parallel. The frequency response is

$$V_{\text{out}} = \frac{j2\pi f\, C_2R_2 + 1}{(j2\pi f\,)^2 C_2C_3R_1R_2 + j2\pi f\,(C_2 + C_3)R_1}(\text{Up} - \text{Dwn}) \tag{2.15″}$$

The loop filter is second-order; the PLL is consequently third-order. Equation (2.15″) can also be rewritten as

$$\left.\frac{V_{\text{out}}}{\text{Up} - \text{Dwn}}\right|_{\text{3rdOrder}} = \frac{j2\pi f\, C_2R_2 + 1}{j2\pi C_2\left(\frac{C_2+C_3}{C_2}R_1\right)} \frac{1}{j2\pi f\, \frac{C_2C_3}{C_2+C_3}R_2 + 1} \tag{2.15‴}$$

Equation (2.15‴) clearly shows that the second-order loop filter is the cascade of a first-order filter with an RC lowpass filter. The second-order transfer function can also be realized with the schematic of Fig. 2.20 (where components' values are indicated with lowercase letters).

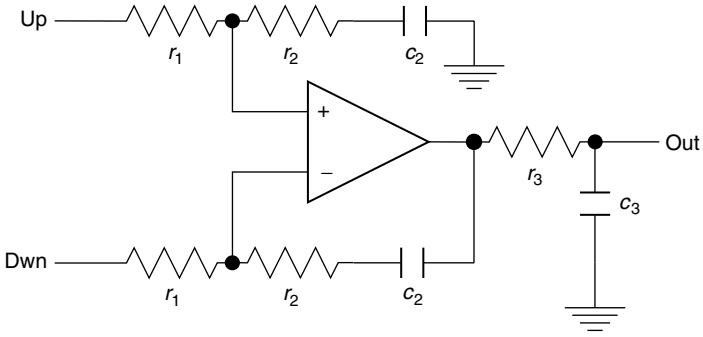


Figure 2.20 Alternative second-order loop filter for a PFD.

Transfer functions of networks in Fig. 2.19*a* (with Z and Z' given by Fig. 2.19*c*) and Fig. 2.20 coincide if

$$c_2 = C_2 \qquad c_3 = \frac{C_2 C_3}{C_2 + C_3} = C_2 // C_3 \qquad r_1 = \frac{C_2 + C_3}{C_2} R_1 \qquad r_2 = r_3 = R_2$$

If spur attenuation has to be increased, the loop filter order can be increased in many ways.

1. Complicating Z_2 by adding other series RC elements in parallel. But this will not change the asymptotic filter slope because the RC series element always adds a pole-zero couple on impedance. The impedance, and gain slope as well, is always 20 dB/decade at most.
2. Modifying the filter of Fig. 2.19*a* by splitting input resistors R_1 and R_1' into two half-value resistors and connecting one capacitor C_{in} from the splitting node to ground. That configuration is shown by Fig. 2.21; the filter order is increased by one. The main advantage of this configuration is the limited slew rate of signals at the opamp inputs. Up and Dwn outputs are short rectangular pulses with a very fast slope (in the order of 100 V/μs). There is the possibility to dynamically saturate the opamp if its slew rate is not sufficiently high (opamp slew rates are usually about 10 V/μs, 10 times slower). Input RC prefiltering made by $R_1/2$ and C_{in} quite reduces the speed of signals as seen by opamp inputs preventing dynamic saturation. The frequency response of the loop filter in Fig 2.21 is

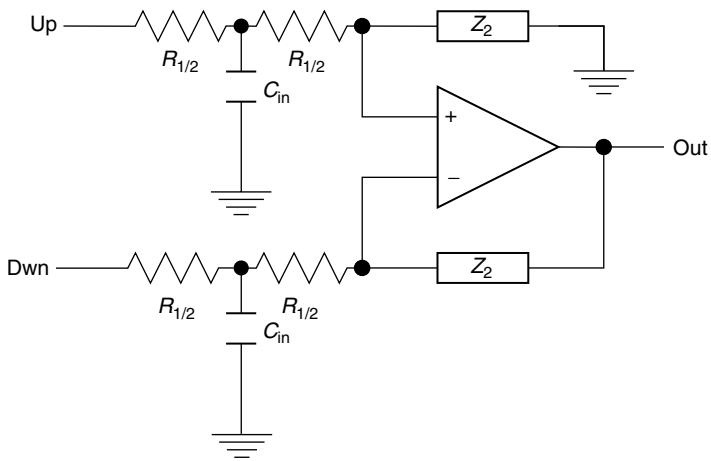


Figure 2.21 Loop filter with input prefiltering network.

given by

$$\frac{V_{\text{out}}}{\text{Up} - \text{Dwn}} = \frac{Z_2}{R_1} \frac{1}{j2\pi f \frac{R_2}{4} C_{\text{in}} + 1} \tag{2.16}$$

where Z_2 can be the impedance used for the zero-, first-, and second-order loop filters discussed before and whose responses are given by general expression (2.14). Comparing expressions (2.15) with (2.16), it can be seen that the filter of Fig. 2.21 has two filtering terms, the first is identical to Eq. (2.15); the second is a first-order lowpass filter with a time constant of $R_1 C_{\text{in}}/4$. The order of the filter in Fig. 2.21 is higher by one than the corresponding filter of Fig. 2.19 (the two filters coincide if C_{in} is removed).

3. Modifying the loop filter in Fig. 2.20 by replacing the output RC lowpass filter with second-order RC, LC, or active lowpass filters. Some possible solutions are shown in Fig. 2.22. All these filters have a second-order lowpass frequency response given by

$$\frac{V_{\text{out}}}{V_{\text{in}}} = F_{\text{aux}}(f) = \left[1 + \frac{1}{Q_t}\left(j\frac{f}{f_t}\right) + \left(j\frac{f}{f_t}\right)^2\right]^{-1}$$

The cutoff frequency and damping factor are given by

a. Passive RC

$$f_t = \frac{1}{2\pi\sqrt{R_1 R_3 C_2 C_4}}$$

$$Q_t = \sqrt{\frac{R_1}{R_3}\frac{C_2}{C_4}}\left[1 + \frac{R_1}{R_3}\left(1 + \frac{C_2}{C_4}\right)\right]^{-1} < 0.5$$

b. Passive RLC

$$f_t = \frac{1}{2\pi\sqrt{LC}} \qquad Q_t = \frac{1}{R}\sqrt{\frac{L}{C}}$$

c. Active RC (Sallen & Key)

$$f_t = \frac{1}{2\pi\sqrt{R_1 R_3 C_2 C_4}} \qquad Q_t = \sqrt{\frac{R_1}{R_3}\frac{C_2}{C_4}}\left(1 + \frac{R_1}{R_3}\right)^{-1}$$

Solutions 1, 2, and 3 can be combined to increase the loop filter order.

2.3.3 Loop filters for charge pump

When the charge pump phase detector is used, the loop filter has to transform the output current (proportional to the phase error) generated from the CP to a voltage for VCO tuning. The loop filter transfer

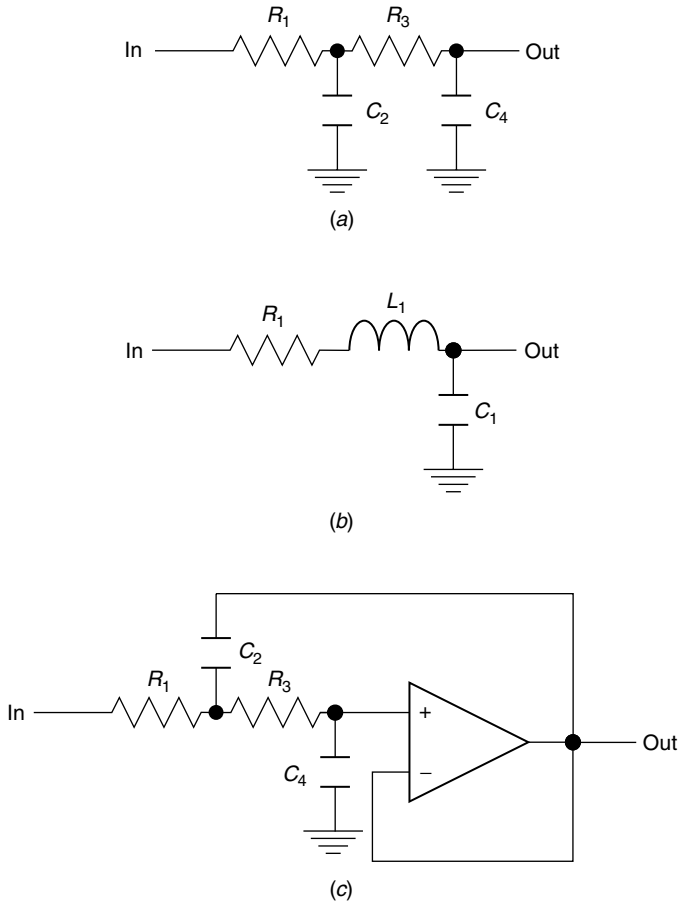


Figure 2.22 Some possible auxiliary loop filters. (*a*) Passive RC, (*b*) passive RLC, (*c*) active RC (Sallen & Key).

function is then a transimpedance. In Sec. 2.2.2.3 it was shown that the CP output voltage has to be kept within a limited range (with both CP transistors operating in their current saturation range) in order to guarantee proper operation of the CP. For this reason both passive and active realizations of CP loop filters are frequency-depending lowpass transimpedance with low-input impedance on transients. This way the CP output voltage is almost constant even when one of the two output transistors is switched on.

2.3.3.1 Passive loop filters for charge pump. Pure passive CP loop filters are shown in Fig. 2.23. A low input impedance on transients is ensured by input shunt capacitor C_1; for this reason the minimum practical

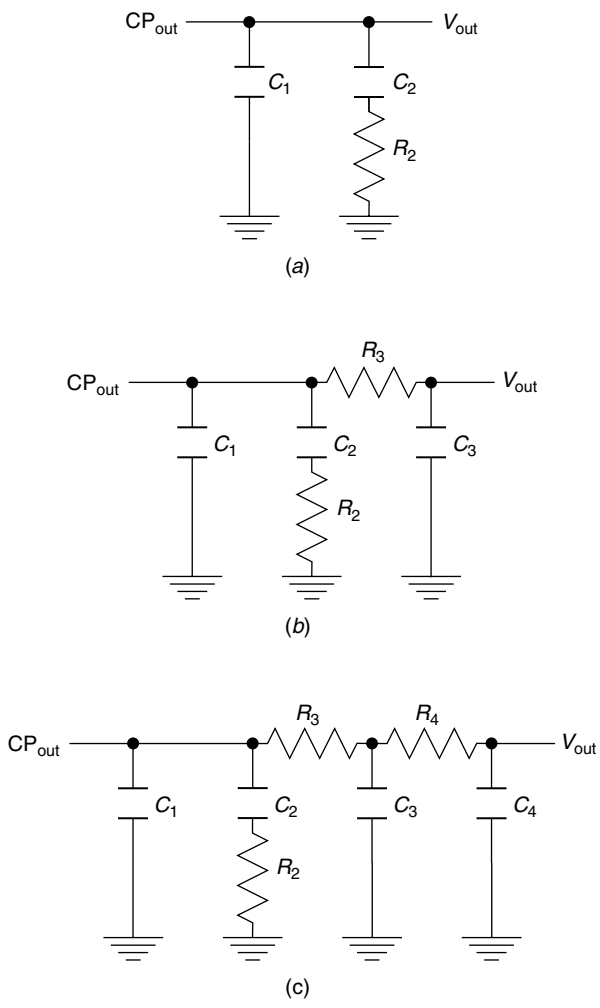


Figure 2.23 (a) Second-, (b) third-, and (c) fourth-order passive loop filters for charge pump.

loop filter order is 2 and only a type II PLL is possible. Figures 2.23a to c show second-, third-, and fourth-order loop filters, respectively. It is assumed that the VCO tuning port has infinite DC input resistance with, eventually, one shunt capacitor. The effect of the VCO tuning port input capacitance is to increase the value of C_1, C_3, and C_4 for the second-, third-, and fourth-order filters, respectively. With these assumptions the fourth-order filter is simplified into third-order if C_4 is removed (or if $C_4 = 0$) and into second-order if C_3 is removed too

(or $C_3 = C_4 = 0$). The general expression for the fourth-order passive transimpedance is

$$F(f) = Z(f) = \frac{\sum_{k=0}^{1} N_k (j2\pi f)^k}{\sum_{k=1}^{4} D_k (j2\pi f)^k} \tag{2.17}$$

where the coefficients of the numerator and denominator are given by

$$\begin{aligned}
N_0 &= 1 \\
N_1 &= C_2R_2 \\
D_1 &= C_1 + C_2 + C_3 + C_4 \\
D_2 &= C_3C_4R_4 + C_1[C_2R_2 + C_3R_3 + C_4(R_3 + R_4)] \\
&\quad + C_2[C_3(R_2 + R_3) + C_4(R_2 + R_3 + R_4)] \\
D_3 &= C_2C_3C_4(R_2 + R_3)R_4 + C_1\{C_3C_4R_3R_4 + C_2R_2[C_3R_3 \\
&\quad + C_4(R_3 + R_4)]\} \\
D_4 &= C_1C_2C_3C_4R_2R_3R_4
\end{aligned} \tag{2.18}$$

The third-order coefficients can be obtained by putting $C_4 = 0$ in Eq. (2.18), and the second-order coefficient can be obtained by letting $C_3 = C_4 = 0$. Note that these simplifications don't affect the numerator coefficients.

The main advantage of the passive CP loop filter is that no active component is required which normally adds noise to the tuning voltage. The main drawback is that the CP output voltage range is limited (usually less than 5 V), and thus so is the tuning voltage. When a wider tuning voltage range is required, active components have to be used. The simplest solution is to insert a voltage amplifier between the passive loop filter output and the VCO tuning port. The voltage amplifier has to respect the same conditions on its input impedance assumed for the VCO tuning port, and its output impedance has to be as low as possible in order to minimize interactions with the tuning port input impedance. Both of these two conditions can be reasonably satisfied by using one operational amplifier as shown in Fig. 2.24. Letting K (for the circuit of Fig. 2.14, $K = 1 + r_4/r_5$) be the voltage gain of the amplifier, the loop filter frequency response becomes the same as that of Eq. (2.17) [its coefficients are still given by Eq. (2.18)]

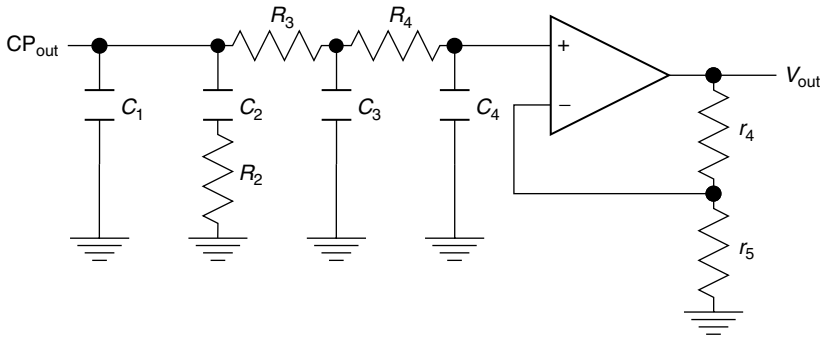


Figure 2.24 Passive transimpedance loop filter with gain.

multiplied by K:

$$F(f) = Z(f) = K \frac{\sum_{k=0}^{1} N_k (j2\pi f)^k}{\sum_{k=1}^{4} D_k (j2\pi f)^k} \tag{2.19}$$

Additional filters of Fig. 2.22 can also be inserted between the loop filter output and the VCO tuning port in Fig. 2.24 in order to further increase the PLL order. Equation (2.19) is multiplied by the second-order lowpass function of Fig. 2.22*a*.

2.3.3.2 Active loop filters for charge pump. One possible realization of transimpedance using an operational amplifier is shown in Fig. 2.25. Its transfer function from the charge pump current to the tuning voltage is given by

$$V_{\text{out}} = -Z_2 I_{\text{CP}} \tag{2.20}$$

Comparing Eq. (2.20) with Eq. (2.14), it can be seen that these two expressions have the same dependence on frequency due to impedance Z_2. The two expressions differ for a constant positive multiplying factor R_1, and Eq. (2.19) has the opposite sign with respect to Eq. (2.14). This sign inversion can easily be removed by adding a further inversion (e.g., inserting one inverting amplifier between the filter output and VCO tuning port) or by inverting the CP output characteristic by swapping the reference and divided VCO signals at the PFD inputs. The main advantage of the circuit in Fig. 2.25 is that the input impedance from the inverting to noninverting input is always very close to zero. By choosing the noninverting input voltage bias V_{ref}, a value right in the middle of the CP dynamic range, proper operation of the charge pump is automatically ensured. At the beginning of Sec. 2.3.3.1 it was

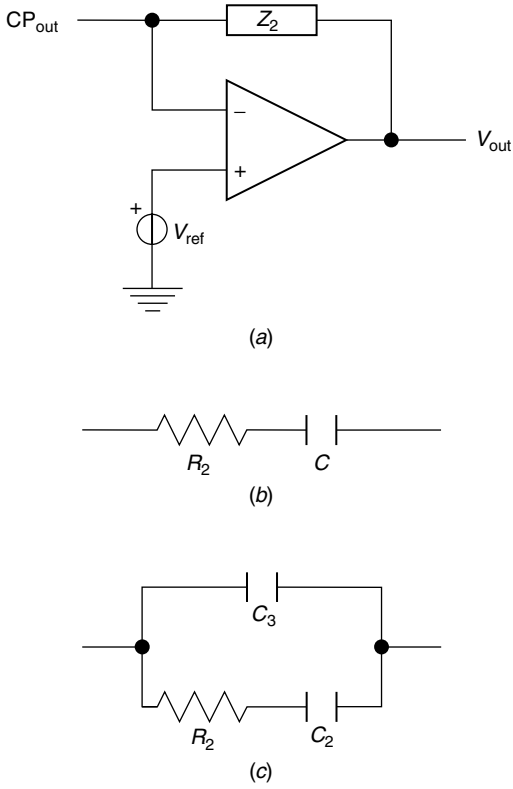


Figure 2.25 Active loop filters for a CP. (a) Filter schematic, (b) Z_2 for a first-order loop filter, (c) Z_2 for a second-order loop filter.

shown that the minimum order for PLL with CP and a passive filter is three and only type II PLLs are possible. If the passive loop filter is replaced with that of Fig. 2.25, these restrictions are removed. Then any PLL order and type are possible. Similarly to the filter of Fig. 2.19, the first- and second-order loop filter frequency responses of Fig. 2.25 are given by

$$V_{\text{out}} = -\frac{j2\pi f CR_2 + 1}{j2\pi f C} I_{\text{CP}} \tag{2.20'}$$

$$V_{\text{out}} = -\frac{j2\pi f C_2 R_2 + 1}{(j2\pi f)^2 C_2 C_3 R_2 + j2\pi f (C_2 + C_3)} I_{\text{CP}} \tag{2.20''}$$

Similarly to the filters of Figs. 2.19, 2.21, and 2.24, additional filters of Fig. 2.22 can be cascaded to the filter output of Fig. 2.25, increasing the PLL order and multiplying the transfer functions of Eqs. (2.19), (2.19′), and (2.19″) by the second-order lowpass function of Fig. 2.22.

2.3.4 Loop filter scaling

The scope of this section is to show loop filter alterations needed to achieve some variations on loop performance or to take into account variations on loop components. The first kind of loop filter scaling is needed when one loop filter, designed to operate with a given PLL, has to be modified in order to operate with a different PLL having different component values. In other words let's consider a given PLL with known values of the phase detector gain K_d, VCO tuning sensitivity K_v, and frequency division factor N. Also suppose we have a loop filter such that the closed-loop PLL frequency response is satisfactory for a given specification. The problem to be solved is how to modify the loop filter components so that the filter can be used on a different PLL having one or more different parameters, say K'_d, K'_v, N' but keeping the same closed-loop frequency response.[†] The original PLL closed-loop frequency response is given by Eq. (1.3):

$$H(f) = \frac{\frac{K_d K_v}{N} \frac{F(j2\pi f)}{j2\pi f}}{1 + \frac{K_d K_v}{N} \frac{F(j2\pi f)}{j2\pi f}}$$

where $F(j2\pi f)$ is the original loop filter transfer function. The new PLL closed-loop frequency response is

$$H'(f) = \frac{\frac{K'_d K'_v}{N'} \frac{F'(j2\pi f)}{j2\pi f}}{1 + \frac{K'_d K'_v}{N'} \frac{F'(j2\pi f)}{j2\pi f}}$$

where $F'(j2\pi f)$ is the new loop filter transfer function. We want the original and new PLLs to have the same frequency response, $H(f) = H'(f)$. It means that

$$H(f) = H'(f) \Rightarrow \frac{\frac{K_d K_v}{N} \frac{F(j2\pi f)}{j2\pi f}}{1 + \frac{K_d K_v}{N} \frac{F(j2\pi f)}{j2\pi f}} = \frac{\frac{K'_d K'_v}{N'} \frac{F'(j2\pi f)}{j2\pi f}}{1 + \frac{K'_d K'_v}{N'} \frac{F'(j2\pi f)}{j2\pi f}}$$

$$H(f) = H'(f) \Rightarrow \underline{\underline{F'(j2\pi f) = \frac{K_d}{K'_d} \frac{K_v}{K'_v} \frac{N'}{N} F(j2\pi f)}}$$

Define the scale factor as a constant over frequency:

$$\alpha = \frac{K_d}{K'_d} \frac{K_v}{K'_v} \frac{N'}{N}$$

[†]This condition may happen if a different VCO and/or phase detector needs to be used; modifications of the frequency division factor occur when a different reference and/or output frequency needs to be used.

The new loop filter transfer function is the old one multiplied by the scale factor:

$$F'(j2\pi f) = \alpha F(j2\pi f) \tag{2.21}$$

Condition (2.21) can be satisfied in different ways depending on the loop filter configuration:

1. If the loop filter configuration is one of those of Figs. 1.3*b*, 2.19, or 2.20, it can be done by either dividing input resistor R_1 (or r_1) or multiplying feedback impedance Z_2 by α (i.e., multiply all its resistance and dividing all its capacitance by α).
2. If the loop filter configuration is the one of Fig. 2.21, it can be done either by dividing the input resistors $R_{1/2}$ and simultaneously multiplying input capacitors C_{in} by α or multiplying feedback impedance Z_2 by α.
3. If the loop filter configuration is one of Figs. 2.23, 2.24, or 2.25, it can be done by multiplying all its resistors and dividing all its capacitors by α.
4. For the loop filter of Fig. 2.24, there is the additional option to multiply the amplifier gain by α, but this has to be considered very carefully because decreasing the amplifier gain reduces the tuning voltage range, and increasing the gain increases noise in the tuning voltage.
5. In any case no modifications have to be made on auxiliary output filters (if present).

Another kind of loop filter scaling is used when a different closed-loop frequency response with a different cutoff frequency but with the same shape over the frequency is needed.† Let's call $H''(f)$ a new closed-loop frequency response. We want the following:

$$H''(f) = H(\beta f) \Rightarrow \frac{\frac{K_d K_v}{N}\frac{F''(j2\pi f)}{j2\pi f}}{1+\frac{K_d K_v}{N}\frac{F''(j2\pi f)}{j2\pi f}} = \frac{\frac{K_d K_v}{N}\frac{F(j2\pi\beta f)}{j2\pi\beta f}}{1+\frac{K_d K_v}{N}\frac{F(j2\pi\beta f)}{j2\pi\beta f}}$$

$$H''(f) = H(\beta f) \Rightarrow \underline{\underline{F''(j2\pi f) = \frac{1}{\beta}F(j2\pi\beta f)}} \tag{2.22}$$

The new loop filter frequency response has to be scaled over the frequency and by the magnitude by the same factor. Amplitude scaling is the same operation previously discussed. It can be done following

†This implies that the new PLL has the same Nyquist diagram, the same phase margin, the same peak response, etc.

instructions 1 to 4 (depending on the loop filter used) where scaling factor α has to be replaced with $1/\beta$. The loop filter translation can be performed as follows:

6. If the loop filter configuration is one of those in Figs. 1.3*b*, 2.19, or 2.20, it can be done by dividing all capacitors by β^2 and multiplying all resistors of feedback impedance Z_2 by β.
7. If the loop filter configuration is that of Fig. 2.21, the modifications in instruction 6 have to be done together by dividing the capacitance of the input capacitors C_{in} by β.
8. If the loop filter configuration is one of those in Figs. 2.23, 2.24, or 2.25, it can be done by multiplying all capacitors by β^2 and dividing all resistors excluding amplifier feedback resistors by β.
9. In any case the auxiliary output filter (if present) has to be modified by dividing the cutoff frequency f_t by β without changing Q_t. This corresponds to
   a. Multipling all resistors and all capacitors of passive RC or Sallen & Key filters by β.
   b. Multipling the inductor and capacitor on the RLC filter by β.

For the particular case of the charge pump with a pure passive loop, instruction 8 has to be applied as in the following example[†] where a loop filter as in Fig. 2.23*c* is used. The PLL components' values are as follows:

- Phase detector (CP) gain

$$K_d = (1 \times 10^{-3})/2\pi$$

- VCO modulation sensitivity

$$K_v = 2\pi(50 \times 10^6)$$

- Frequency division factor

$$N = 40$$

- Frequency scaling factor

$$\beta = 2$$

The loop filter components (scaled filter with lowercase letters) are

- $C_1 = 1$ nF $\qquad c_1 = 4$ nF
- $C_2 = 22$ nF $\qquad c_2 = 88$ nF

[†]See the file LoopFilterScaling.MCD.

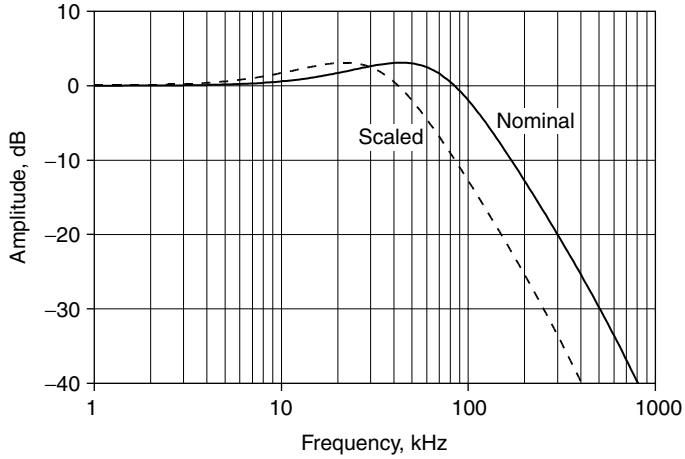


Figure 2.26 Closed-loop frequency response for nominal and scaled loop filters.

- $R_2 = 330\ \Omega$ $r_2 = 165\ \Omega$
- $R_3 = R_4 = 470\ \Omega$ $r_3 = r_4 = 235\ \Omega$
- $C_3 = C_4 = 470$ pF $c_3 = c_4 = 1.88$ nF

The PLL parameters (scaled filter within parentheses) are

- Closed-loop unit gain bandwidth 84.39 kHz (42.195 kHz)
- Closed-loop gain peak 3.092 dB (3.092 dB)
- Closed-loop peak frequency 43.738 kHz (21.869 kHz)
- Phase margin 44.185° (44.185°)

The closed-loop frequency response for both nominal and scaled loop filters are plotted in Fig. 2.26.

2.4 VCO

2.4.1 Principle of working

The VCO acts as a quasi-sinusoidal† generator whose output frequency is a defined function of the tuning voltage. Usually, radio frequency (RF) and microwave oscillators employ a combination of selective positive feedback with a gain element. A general block diagram of such an

†The output signal is a distorted sinusoid, containing some harmonics.

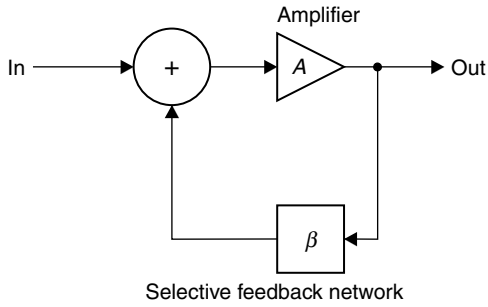


Figure 2.27 General block diagram of RF oscillator.

oscillator is shown in Fig. 2.27. The gain from the input to the output can easily be found by applying Mason's rule:

$$\frac{\text{Out}}{\text{In}} = \text{Gain}(f) = \frac{A(f)}{1 - A(f)\beta(f)} \tag{2.23}$$

where $A(f)$ and $\beta(f)$ are the frequency-dependent gain of the amplifier and the feedback element. If at some frequency, the loop gain $A(f)\beta(f)$ becomes unitary, the closed-loop gain of Eq. (2.23) becomes infinite. This means that there is a finite output signal with a zero input signal. This implies oscillations by definition.

So at unit loop gain the frequency loop oscillates at that frequency. The onset of oscillations can be explained by linear considerations although the amplitude of oscillations is determined by compression of the active device. Oscillations build up from noise or some switch on transient. At startup the amplitude is very small and the loop gain is higher than 1. As oscillations build up to the active element compression level, the gain is reduced according to the amplifier compression curve. Steady-state amplitude is reached when the loop gain is compressed down to 1. Such nonlinear limitation of the output level also generates harmonics that have to be filtered out.

Selective networks consist of some reactive elements with at least one capacitor and one inductor. Sometimes one or more elements of a feedback network are given by parasitic elements of an active device. An oscillator's output frequency can be changed by modifying the value of one or more elements of the feedback network. An oscillator becomes voltage controlled if one of more elements of a frequency selective feedback network changes its value according to a control voltage. The most widely used device is called a *varactor*, which is a reverse-biased junction diode whose capacitance monotonically decreases with reverse bias. Varactors are usually realized using silicon for frequencies up to a few gigahertz or gallium arsenide for frequencies up to 40 GHz or more. Whatever material they are made of, varactors can

be classified into two different classes according to the doping profile of their junction: abrupt and hyperabrupt. Without going deeply into semiconductor physics, abrupt varactors have a lower parasitic series resistance (higher merit factor) and a lower capacitance variation over the bias voltage comparing to hyperabrupt varactors. The junction capacitance C_j versus the reverse-bias voltage V_j can be expressed as

$$C_j(V_j) = \frac{C_0}{\left(1 - V_j/V_\varphi\right)^\gamma} + C_{\min} \tag{2.24}$$

where C_o = zero-bias junction capacitance
V_φ = junction potential
γ = grading coefficient
$C_{\min}$ = parasitic (or residual) shunt capacitance or junction capacitance for very high reverse bias

Although Eq. (2.24) can be derived from semiconductor physics, from a VCO design point of view, Eq. (2.24) is just a compact representation of voltage-depending capacitance. Its parameters are calculated by curve fitting with a measured $C - V$ curve. Figure 2.28 shows capacitance versus voltage of one abrupt gallium arsenide varactor. The dashed line is measured, and the continuous line comes from Eq. (2.24) with the following parameters:

$$C_o = 3.50 \text{ pF} \qquad C_{\min} = 0.15 \text{ pF} \qquad V_\varphi = 9.91 \text{ V} \qquad \gamma = 4.06$$

Agreement between the two curves is excellent.

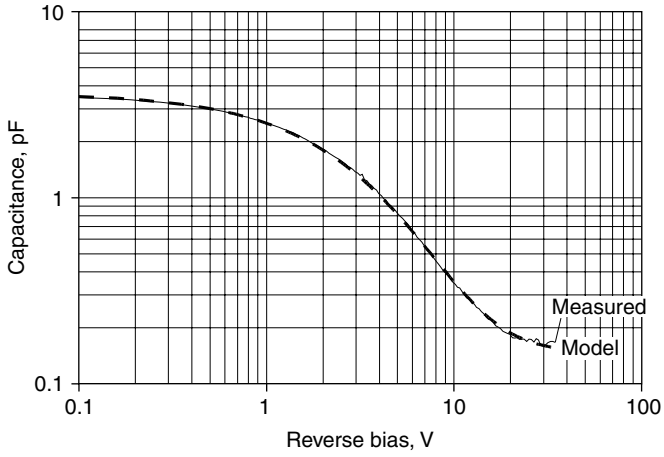


Figure 2.28 Measured and modeled capacitance versus voltage of abrupt GaAs varactor.

A varactor is not a pure capacitor. It can be better modeled as a series RC network† due to its parasitic resistance. The varactor merit factor at a given frequency is defined as the ratio between its capacitive reactance at that frequency divided by the parasitic series resistance. The varactor merit factor ranges from 10 to 100 at microwave frequencies.

Some microwave VCOs employ a yttrium-iron-garnet (YIG) resonator instead of a varactor. A YIG resonator is a parallel LC circuit, not just a capacitor. It is tuned by a magnetic field at a very linear rate. A magnetic field is generated by electromagnets, so the YIG resonant frequency and the oscillator output frequency are controlled by current flowing through the electromagnet. A YIG tuned oscillator (YTO) is current controlled rather than voltage controlled. In addition, big solenoids of an electromagnet don't allow for fast variation on output frequency. YTOs for PLL applications have two tuning coils: a *main coil* for coarse tuning (high current, very limited bandwidth), and the so-called *FM coil* (relatively wide bandwidth and low current) for PLL correction of output frequency to its exact value. The main advantage of a YIG resonator over a varactor is the Q factor which is 10 to 100 times higher.

2.4.2 VCO analysis

A detailed and in-depth description of VCO configurations is beyond the scope of this book. Here some examples will be presented just to show some design techniques and problems involved with VCO applications on a PLL. Figure 2.29 shows the schematic of a VCO which is widely used for output frequency up to 2 GHz. It is known as "Clapp" oscillator. The frequency selective positive feedback network consists of components C_{be}, C_{bo}, and the elements of the thank circuit. *Thank circuit* is a series LC resonator where the capacitance is voltage-dependent. It includes C_{tuning}, L_{tuning}, the varactor DV_1, and the varactor bias resistor RT_1. C_{tuning}, which acts like a DC-block between the base and varactor voltage, can be used to modify the output frequency versus the tuning voltage characteristic since it is in series with the varactor capacitance. The value of R_{bias} is in kilo-ohms. It allows the tuning voltage to reverse bias the varactor without loading it at radio frequencies; it can be replaced or combined with an inductor. The active element is a bipolar transistor (usually silicon) BJT_1 with its bias network made by resistors R_{bc}, R_{bo}, and R_{bias}. The L_{bias} inductor is sometimes used to prevent R_{bias} from loading too much from the feedback network. The output is

†Normally a series inductance also has to be considered, whose value mainly depends on the used package chip, beam lead, a surface-mount device (SMD), or axial package. Series inductance is very low for beam lead devices, about 1 nH for an SMD package, and even higher for axial in-hole packages.

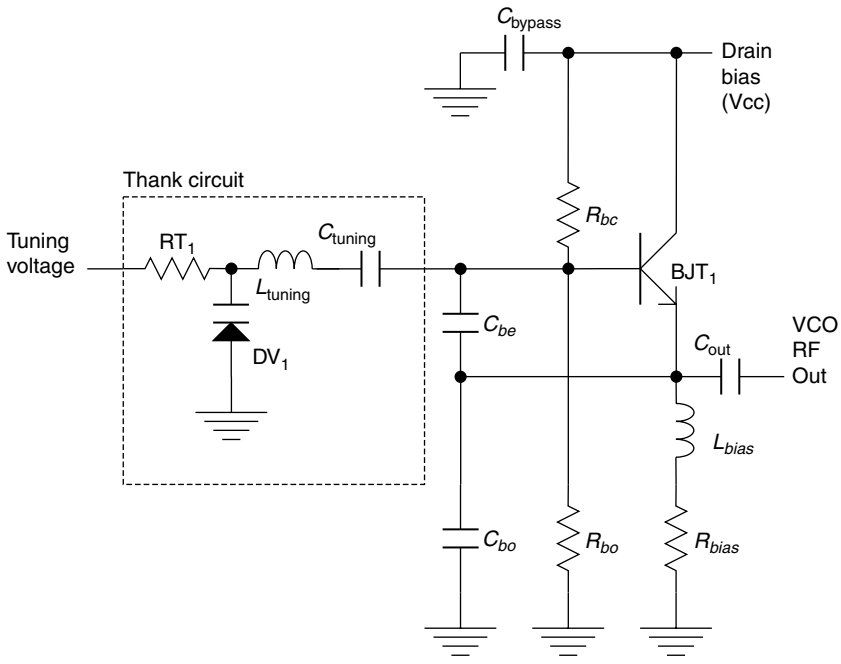


Figure 2.29 Schematic of an oscillator suitable for RF frequencies.

connected to the emitter with a DC decoupling capacitor C_{out}, and the collector is connected to ground at radio frequencies by capacitor C_{bypass} which is placed very close to the transistor.

Another very popular schematic for frequencies from 3 to 20 GHz is shown in Fig. 2.30. The active device MESFET_1 is a GaAs metal epitaxial semiconductor field effect transistor (MESFET). The thank circuit is a parallel LC, the varactor anode is DC connected to ground via L_d, the cathode is connected to the tuning voltage via RT_1. At radio frequencies the cathode is grounded. Resistor RT_1 is less critical than the one of Fig. 2.29 because CT_1 has a very low impedance to ground, so the minimum decoupling is needed to the tuning port. The feedback network consists of the previously described thank circuit, gate inductor L_g, and the parasitic gate-source capacitance of the active device MESFET_1. The drain bias network consists of R_{bias}, L_{bias} (high impedance at RF, low DC impedance), C_{bypass} (low RF impedance to decouple Vcc pin), and DC block C_{out}. An approximate calculation of the oscillation frequency of the circuit of Fig. 2.30 can be done by using a simplified linear model for the active element, which is a voltage-controlled current source (VCCS) with a parasitic input capacitance C_{gs} having series resistor R_i.

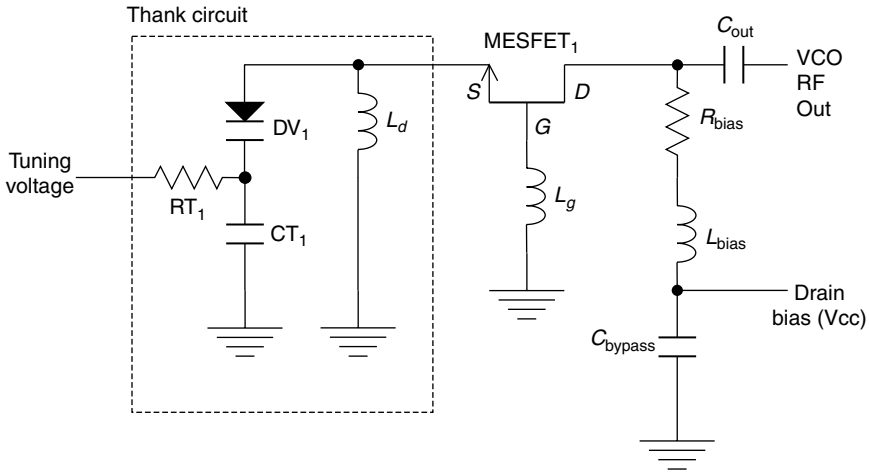


Figure 2.30 Schematic of an oscillator suitable for microwave frequency.

A linearized circuit is shown in Fig. 2.31*a* where the bias network is omitted and the thank circuit is replaced by a parallel RLC resonating circuit. The oscillation frequency is calculated from the open-loop gain expression. The loop can be opened by breaking connections between the gate and control pin of the VCCS on the field effect transistor (FET) linear model, as shown in Fig. 2.31*b*.

The circuit is analyzed by using the FET source as a reference node for all voltages instead of ground. This technique is known as virtual ground and simplifies the analysis. The open-loop gain is given by

$$G_{\text{ol}}(f) = -\frac{g_m L_d (j2\pi f)}{\sum_{k=0}^{4} a_k (j2\pi f)^k} \tag{2.25}$$

with

$$a_0 = 1$$

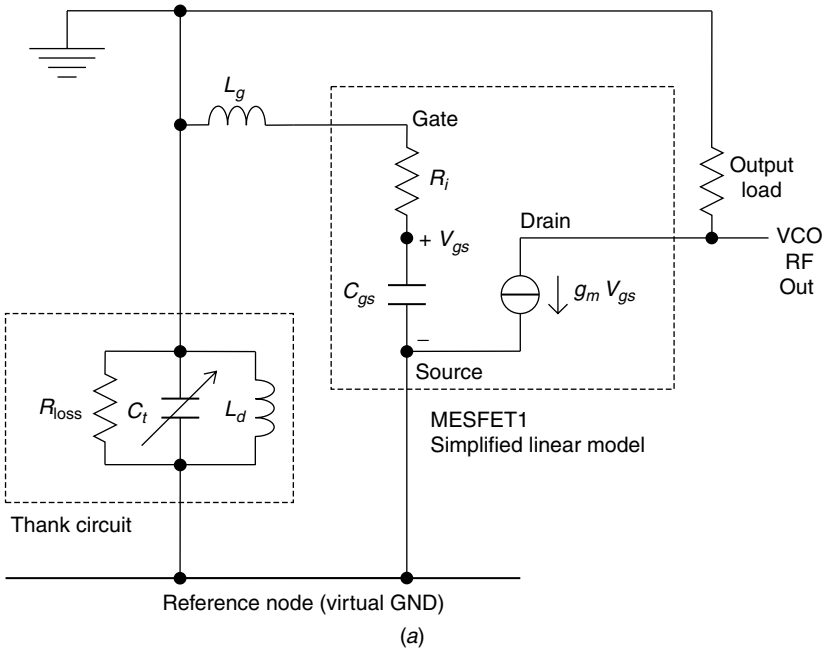
$$a_1 = \frac{L_d}{R_{\text{loss}}} + C_{gs} R_i$$

$$a_2 = L_d \left[C_t + C_{gs} \left(1 + \frac{R_i}{R_{\text{loss}}} \right) \right] + L_g C_{gs}$$

$$a_3 = L_d C_{gs} \left(C_t R_i + \frac{L_g}{R_{\text{loss}}} \right)$$

$$a_4 = C_{gs} C_t L_g L_d$$

The oscillation condition is the unitary loop gain. The loop gain is a complex number, so the oscillation condition is equivalent to two



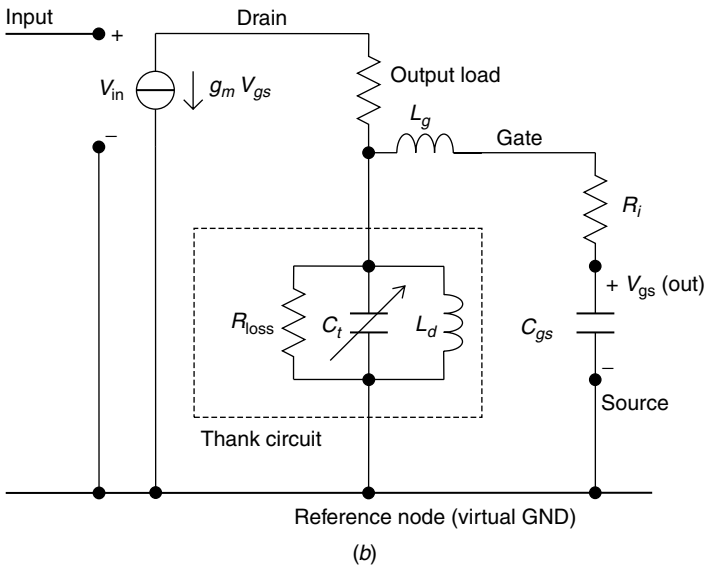


Figure 2.31 Simplified linear schematic of the oscillator of Fig. 2.29. (*a*) Closed loop, and (*b*) open loop.

conditions:

$$|G_{\text{ol}}(f)| = 1 \qquad \arg[G_{\text{ol}}(f)] = 0$$

The numerator of $G_{\text{ol}}(f)$ is purely imaginary. The argument is zero if the real part of the denominator is zero and the imaginary coefficient has the opposite sign† of that of the numerator:

$$a_0(j2\pi f)^0 + a_2(j2\pi f)^2 + a_4(j2\pi f)^4 = 0$$
$$a_1(j2\pi f)^1 + a_3(j2\pi f)^3 = -g_m L_d(j2\pi f)$$

or

$$a_0 - a_2(2\pi f)^2 + a_4(2\pi f)^4 = 0$$
$$a_1 - a_3(2\pi f)^2 = -g_m L_d$$

Let's momentarily suppose that the condition on the real part of the denominator is satisfied. The loop gain amplitude is ≥ 1 if

$$a_1 - a_3(2\pi f)^2 \leq -g_m L_d \Rightarrow g_m \geq \frac{a_3(2\pi f)^2 - a_1}{L_d}$$

$$g_m \geq \frac{\left[L_d C_{gs}\left(C_t R_i + \frac{L_g}{R_{\text{loss}}}\right)\right](2\pi f)^2 - C_{gs}R_i + \frac{L_d}{R_{\text{loss}}}}{L_d} \tag{2.26}$$

where g_m and L_d are both positive quantities. Equation (2.26) contains positive quantities only. This implies that the numerator of the second member of Eq. (2.26) has to be nonnegative‡:

$$f \geq \frac{1}{2\pi}\sqrt{\frac{C_{gs}R_i + \frac{L_d}{R_{\text{loss}}}}{L_d C_{gs}\left(C_t R_i + \frac{L_g}{R_{\text{loss}}}\right)}} \tag{2.27}$$

In the special case of $R_i = 0$, Eq. (2.27) simplifies to

$$f \geq \frac{1}{2\pi\sqrt{C_{gs}L_g}} \tag{2.27'}$$

The minimum potential oscillation frequency is given by the resonance of the gate inductor with the gate-source capacitance and is

†Equation (2.25) has a minus sign.

‡Equation (2.26) has to be satisfied with an equals sign when g_m indicates FET transconductance at power compression, e.g., steady-state oscillations with a stabilized amplitude.

independent from the thank circuit in the simplified case of $R_i = 0$ (in the more general case of $R_i > 0$, it is slightly affected by the thank circuit values). In practice the circuit can oscillate in a frequency range: the lower limit is given by Eq. (2.27) [or the simplified Eq. (2.27′)], and the upper limit is due to the FET gain decreasing at high frequencies. There is a frequency value that makes the FET gain go low enough to where it does not satisfy the condition (2.26). The calculation of this upper limit of oscillation frequency is difficult and thus a more complex FET model is needed. If condition (2.26) is satisfied, the oscillation frequency is given by the zeros in the real part of the loop gain denominator:

$$a_0 - a_2(2\pi f)^2 + a_4(2\pi f)^4 = 0 \Rightarrow (2\pi f)^2 = \frac{a_2}{2a_4} \pm \sqrt{\left(\frac{a_2}{2a_4}\right)^2 - \frac{a_0}{a_4}}$$

Substituting the values of the coefficients of the loop gain denominator $(a_0, a_1, \ldots, a_4)$ into this expression, we obtain two values for oscillation frequency, but only one value is the good one since only one will satisfy condition (2.26). If there is only one oscillating frequency, the oscillator is well designed. If there are many oscillating frequencies, the oscillator is not well designed and doesn't work properly. Such a poorly designed oscillator is affected by the output frequency jumping from one value to the other; this phenomenon is sometimes called *mode jumping* where typically the output frequency changes when the supply voltage is switched off and on.

$$f = \frac{1}{2\pi}\sqrt{\frac{a_2}{2a_4} \pm \sqrt{\left(\frac{a_2}{2a_4}\right)^2 - \frac{a_0}{a_4}}} \tag{2.28}$$

The oscillation frequency given by Eq. (2.28) depends on the tuning capacitance C_t and thus on the tuning voltage according to Eq. (2.24). Determination of the output frequency using Eq. (2.28) is very qualitative due to the very simplified models used for the thank circuit, active elements, and output load (bias network omitted). Nevertheless it can be used as a good starting point. More accurate calculations can be made by using nonlinear circuit simulators like SPICE. A more detailed description of a VCO having a configuration as in Fig. 2.30 is given by the following SPICE netlist† including nonlinear models for the varactor [based on Eq. (2.24)] and for the MESFET (based on the Statz model). Gate and source inductors are modeled with series RL networks; one resistor is added in series with the varactor to model varactor parasitic resistance, and all capacitors are modeled with ideal elements. That SPICE circuit file can be used to see the oscillation buildup from the

†See the SIMETRIX file MicrowaveVCO.sxsch.

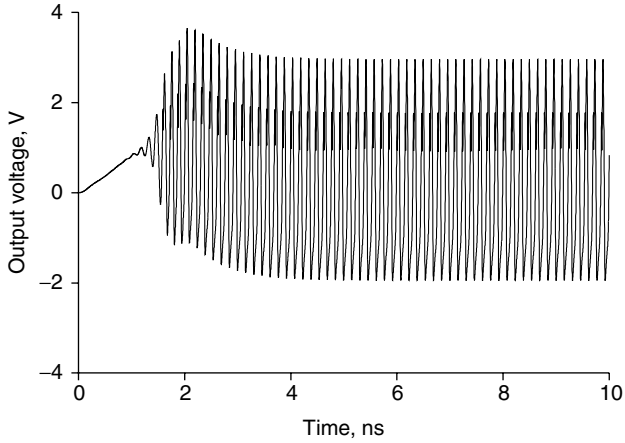


Figure 2.32 SPICE simulation of VCO transient output voltage.

switch on transient as shown in Fig. 2.32 and to calculate the steady-state oscillation frequency versus the tuning voltage. Although circuit description is not very accurate (real active and passive components should have more complicated models), it still gives relativly good predictions about output frequency and power.

```
V3      Vtuning       0             3 *Tuning Voltage
R3      1             Vtuning       220
C4      1             0             10p
R1      1             2             1
D1      Source        2             Varactor
C7      Source        2             150f
Ld      Source        3             3n
R2      0             3             1
Z$Q1    Drain         Gate Source   MESFET1
Lg      4             Gate          1.5n
R12     4             0             3
R4      Drain         5             22
L2      6             5             6n
V1      6             0             5 Pulse(0 5 0 2n 2n) *Vcc
Cout    Drain         Out           10p
R5      OUT           0             50 *Load Resistor
.TRAN 0 10n 0 1p
.model MESFET1 NMF
+ (VTO = -0.655 ALPHA = 2.9 LAMBDA = 0.062 BETA = 0.057
Cgd = 0.1pF + Cgs = 0.3pF Cds = 0.1pF M = 2.84 VBI = 1.54)
.model VARACTOR D (CJO = 3.5pF m = 4.06 VJ = 9.91)
```

A physical VCO construction is shown in Fig. 2.33. The gate and drain inductors are realized with a high-impedance microstrip transmission

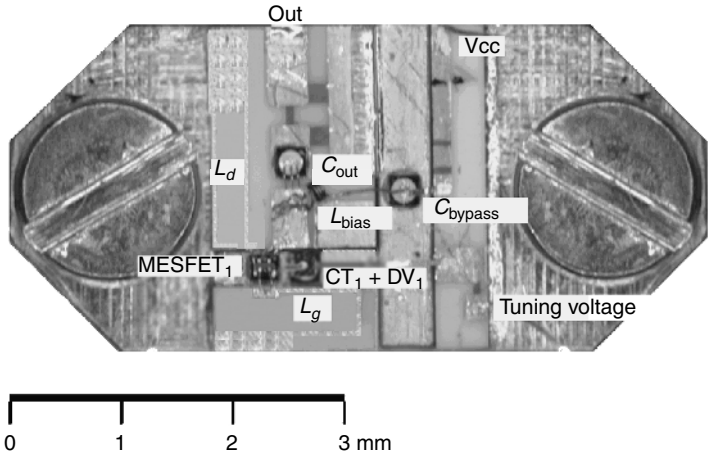


Figure 2.33 Physical VCO realization.

line; the FET, varactor, and capacitors are in chip form; and the connections are made by bonding wires. The circuit is built with alumina substrate ($h = 0.635$ mm, $\varepsilon_r = 9.9$) on a 5 mm $\times$ 8 mm carrier. Three output frequency curves are plotted on Fig. 2.34: The first is given by Eq. (2.24) ($g_m = 10$ mS, $C_{gs} = 0.5$ pF, $R_i = 6$, $L_g = 1.5$ nH, $L_d = 3$ nH, resonator unloaded $Q = 30$),† the second is the SPICE simulation result, and the third is the measured one.

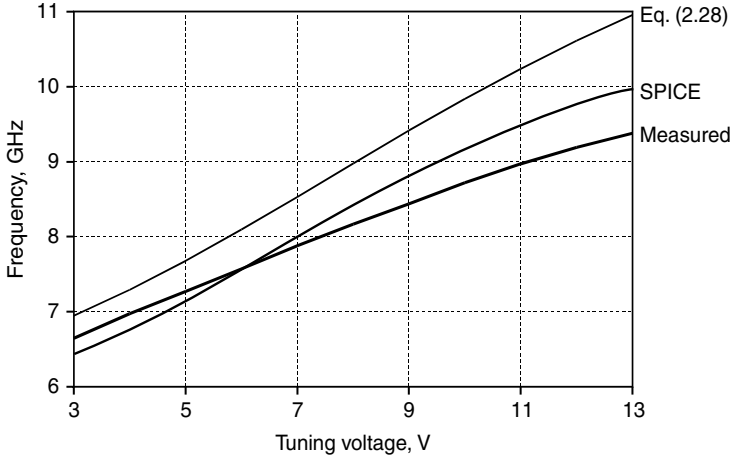


Figure 2.34 VCO output frequency versus tuning voltage.

†See the MATHCAD file VCO.mcd.

In Sec. 1.4 we gave a first definition of the VCO in-out relation; more precisely it was assumed that the output angular frequency is proportional to the tuning voltage through a proportionality constant named VCO_{gain} (K_v). The VCO tuning characteristic is not linear. In the general case the output angular frequency isn't a linear function of the tuning voltage: The VCO gain has to be defined as the derivative of the output angular frequency with respect to the tuning voltage:

$$K_v = \frac{d\left[\omega_{\text{out}}\left(V_{\text{tuning}}\right)\right]}{d\left(V_{\text{tuning}}\right)} = 2\pi \frac{d\left[f_{\text{out}}\left(V_{\text{tuning}}\right)\right]}{d\left(V_{\text{tuning}}\right)} = 2\pi K_v' \tag{2.29}$$

The VCO gain K_v has a unit of rad s^{-1} V^{-1}. Very often K_v' is used which has the unit Hz/V. It is the derivative of the frequency with respect to the tunning voltage rather than of the angular frequency. K_v' is usually called the *modulation sensitivity* and is often expressed in MHz/V. The modulation sensitivity of the VCO in Fig. 2.33 together with its tuning curve is plotted in Fig. 2.35. Note that the modulation sensitivity ranges from 328 (at minimum output frequency) to 188 MHz/V (at maximum frequency).

In order to evaluate the effect of K_v variation, we will employ the VCO of Fig. 2.35 over its output frequency range (6.7 to 9.3 GHz) in one type II second-order PLL. If f_r is the reference frequency expressed in MHz,

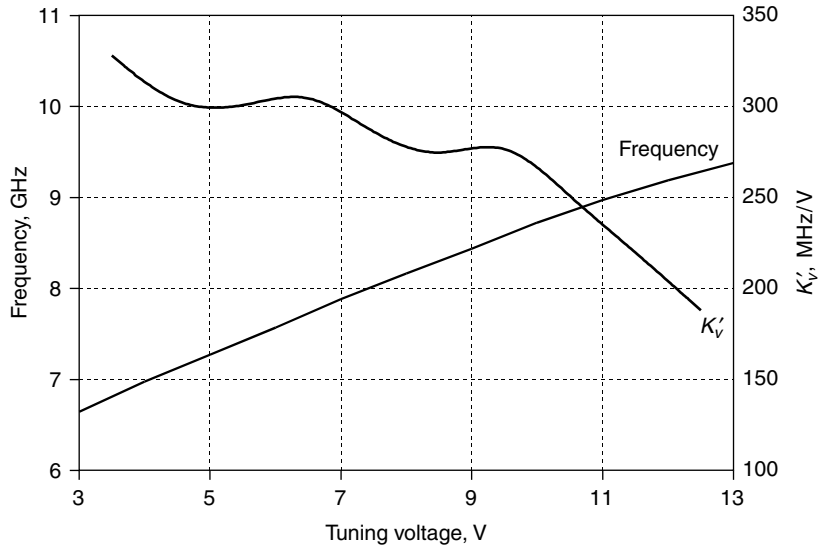


Figure 2.35 VCO output frequency versus tuning voltage and modulation sensitivity.

the frequency division factors at the minimum and maximum output frequencies are respectively given by

$$N_a = \frac{6700}{f_r} \qquad N_b = \frac{9300}{f_r}$$

Corresponding VCO gains are

$$K_{va} = 2\pi(328 \times 10^6) \qquad K_{vb} = 2\pi(188 \times 10^6)$$

The PLL natural frequencies are

$$f_{na} = \frac{1}{2\pi}\sqrt{\frac{K_d K_{va}}{N_a}\frac{1}{\tau_1}} = \sqrt{\frac{K_d(328 \times 10^6) f_r}{2\pi 6700}\frac{1}{\tau_1}}$$

$$f_{nb} = \sqrt{\frac{K_d(188 \times 10^6) f_r}{2\pi 9300}\frac{1}{\tau_1}}$$

$$Q_a = \frac{\tau_2}{\sqrt{\frac{K_d K_{va}}{N_a}\frac{1}{\tau_1}}} = \frac{\tau_2}{\sqrt{\frac{K_d 2\pi(328\times 10^6) f_r}{6700}\frac{1}{\tau_1}}}$$

$$Q_b = \frac{\tau_2}{\sqrt{\frac{K_d 2\pi(188\times 10^6) f_r}{9300}\frac{1}{\tau_1}}}$$

so

$$\frac{f_{na}}{f_{nb}} = \sqrt{\frac{K_{va}}{K_{vb}}\frac{N_b}{N_a}} = \sqrt{\frac{328}{188}\frac{9300}{6700}} \cong 1.56 \qquad \text{and} \qquad \frac{Q_a}{Q_b} = \frac{f_{nb}}{f_{na}} \cong 0.64$$

At the minimum output frequency, the PLL natural frequency is at a maximum and the damping factor is at a minimum, and vice versa. Keeping in mind that the higher the Q the lower the phase margin, choose τ_1 and τ_2 to have a maximum damping factor $Q_b = 1.197$ (45° phase margin). We will have $Q_a = Q_b(0.64) \cong 0.769$ (about 62° phase margin). Likewise if τ_2 gives the minimum natural frequency $f_{nb} = 1$ kHz, it will also be $f_{na} = 1.56$ kHz. Summarizing, at the highest output frequencies, the loop gain is decreased by two factors: VCO modulation sensitivity decreases and frequency division factor increases. The closed-loop gain, together with the error response of that PLL at the minimum and maximum output frequencies, is plotted in Fig. 2.36. The offset frequency is normalized to f_{nb}, being $f_{nb} = 1$ kHz. The abscissa can also be read as the offset frequency expressed in kilohertz.

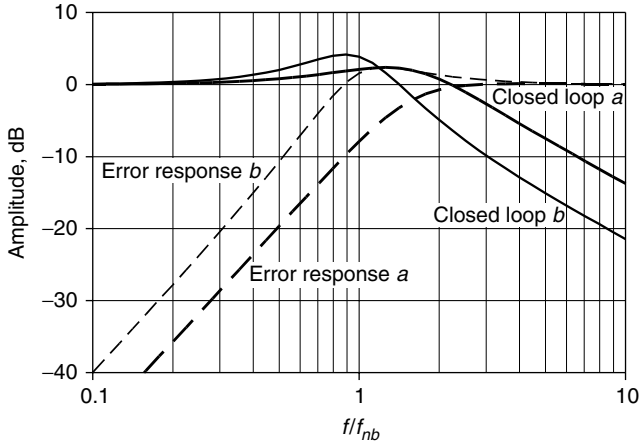


Figure 2.36 Closed-loop gain and phase error response at the minimum and maximum output frequency.

Some VCO designs try to compensate for the two factors discussed by increasing K_v to a high tuning voltage (thus at the highest output frequency). This result is very difficult to achieve because at a high tuning voltage, the varactor capacitance tends to saturate (see Fig. 2.28). In addition the higher the output frequency, the more it is affected by parasitic elements of both the active and passive components of the VCO and the less it depends on varactor capacitance. Sometimes one variable gain amplifier is inserted between the loop filter output and VCO tuning port. The gain of that amplifier is programmed together with the frequency divider such that the loop gain is almost constant over the output frequency in order to minimize variations on the PLL closed-loop transfer function.

2.4.3 Phase Noise

Noise sources within active and passive devices in the oscillator will modulate the output spectrum: noise sidebands are produced around the fundamental frequency. Active device noise usually dominates over noise due to passive components. Transistor noise has two components:

1. Low-frequency noise. Its power density is proportional to $1/f$. It is also known as *flicker noise*.
2. Thermal noise. Its power density is constant over the frequency. It is also known as *white noise*.

Output signal modulations due to noise sources can be classified into three classes: AM, FM, and PM.[†] FM and PM produce the same effect on the output spectrum; AM is typically orders of magnitude lower than the previous two. The oscillator output signal can be written as

$$V_{\text{out,VCO}}(t) = [V_o + n_{\text{AM}}(t)]\ \sin[2\pi f_{\text{VCO}} t + \theta_n(t)] \tag{2.30}$$

where V_o = output signal amplitude
$n_{\text{AM}}(t)$ = AM noise
f_{VCO} = VCO output frequency or carrier frequency
$\theta_n(t)$ = PM noise

Phase modulation due to noise produces two symmetrical sidebands around the carrier frequency. They can be characterized by the ratio of noise power in a 1-Hz bandwidth at a given frequency f_m offset from the carrier to the signal or carrier power. This ratio is very often expressed in dBc/Hz. Leeson found a closed-form expression for single sideband (SSB) phase noise[‡]:

$$\mathscr{L}(f_m) = 10\ \log_{10}\left\{\frac{1}{2}\left[1 + \left(\frac{f_{\text{out}}}{2Q_L f_m^2}\right)^2\right]\left(1 + \frac{f_c}{f_m}\right)\frac{NFKT}{P_s}\right\} \tag{2.31}$$

where f_{out} = VCO output frequency
f_m = offset frequency
NF = active device noise figure
K = Boltzmann's constant = 1.38×10^{-23} J/K
T = room temperature = 298 K
f_c = flicker noise corner of active device[§]
P_s = average power at input of active device
Q_L = resonator's loaded Q

Equation (2.31) can be expanded into a polynomial of variable $1/f_m$:

$$\mathscr{L}(f_m) = 10\ \log_{10}\left(A_0 + \frac{A_1}{f_m} + \frac{A_2}{f_m^2} + \frac{A_3}{f_m^3}\right) = 10\ \log_{10}\left(\sum_{K=0}^{3}\frac{A_K}{f_m^K}\right) \tag{2.32}$$

[†]Amplitude modulation, frequency modulation, and phase modulation, respectively.

[‡]A more precise definition of phase noise will be given in Sec. 4.3.1.

[§]Below f_c, the noise density of the active device increases with a slope of $1/f$ (10 dB/decade).

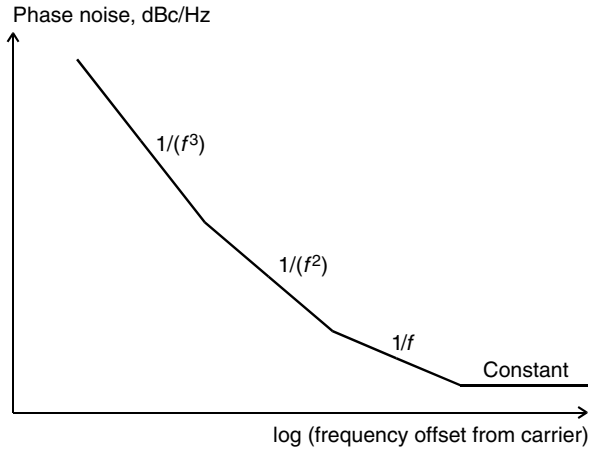


Figure 2.37 Tangential approximation of VCO phase noise shape.

with

$$A_0 = \frac{NFKT}{2P_s}$$

$$A_1 = f_c \frac{NFKT}{2P_s}$$

$$A_2 = \left(\frac{f_{\text{out}}}{2Q_L}\right)^2 \frac{NFKT}{2P_s}$$

$$A_3 = \left(\frac{f_{\text{out}}}{2Q_L}\right)^2 f_c \frac{NFKT}{2P_s}$$

A typical phase noise shape is shown in Fig. 2.37 where Eq. (2.32) is tangentially approximated by four segments with constant slope.

Equation (2.31) gives some suggestions about how to minimize oscillator phase noise. The active device has to be chosen with the minimum possible noise figure even if the noise figure mentioned in Eq. (2.31) is relative to the transistor operating in the compression region: it can be quite different from the small signal noise figure usually declared by transistor manufacturers. The active device has to be chosen with the flicker noise corner as low as possible as well. The oscillator has to be designed in order to maximize power at the input of the active device. The highest possible Q resonator has to be used. Loaded Q is always lower than unloaded (or the intrinsic resonator's Q): Resonator loading due to the active device together with the feedback network has to be minimized. Given that YIG Q is 10 to 100 times higher than varactor

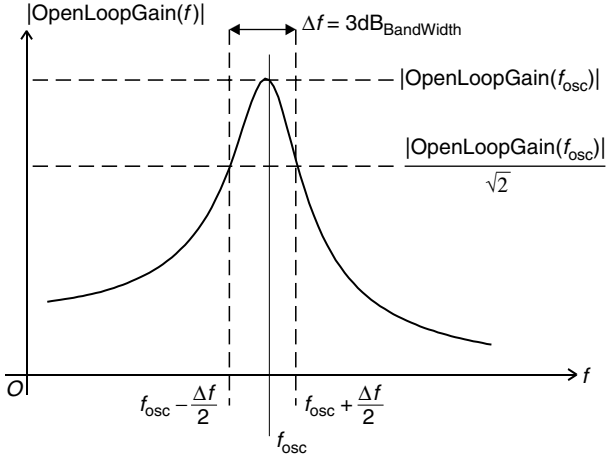


Figure 2.38 Open loop gain for the oscillator of Fig. 2.31.

Q, a YIG VCO has a 20- to 40-dB better phase noise compared with a varactor VCO. Anyway Eq. (2.31) has two terms that don't contain Q_L and have constant and $1/f_m$ dependence over the offset frequency. Improvements on Q_L don't improve the constant and $1/f_m$ sloped part of the phase noise spectrum. Q_L can be approximately calculated from the open-loop gain as drawn in Fig. 2.38, which shows the open-loop gain of the oscillator of Fig. 2.31[†] with same components' values used for the calculation of K_v. It can be seen that the maximum loop gain frequency slightly differs from the oscillation frequency (where the loop gain phase is zero). This is due to the phase shift introduced by the feedback network and parasitic elements of the active device. Loaded Q is defined as the ratio of oscillation frequency to open-loop gain 3-dB bandwidth: $Q_L = f_{\text{osc}}/\Delta f$. The main approximation of this approach consists in considering that transconductance g_m is the only circuit parameter changing from the onset to stabilized amplitude oscillations. It is assumed that g_m reduction due to transistor compression stabilizes the amplitude of the oscillation by making open-loop gain equal to 1 at the oscillation frequency. In practice many other elements change due to nonlinear effects: inside the active device and sometimes even inside the resonator (typically the varactor).

The phase noise of the VCO in Fig. 2.33 was measured at an output frequency of 8 GHz. The result is shown in Fig. 2.39. The measured

[†]See the MATHCAD file Vco.mcd.

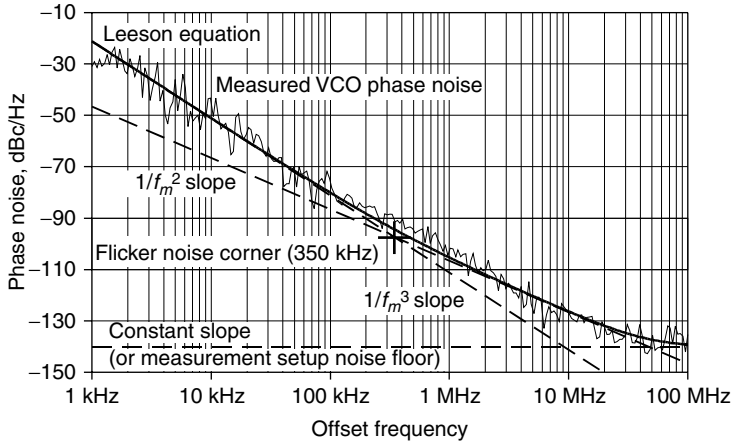


Figure 2.39 Phase noise of the VCO of Fig. 2.33.

phase noise spectrum is well approximated by

$$\mathscr{L}(f_m) = 10 \log_{10}\left(A_0 + \frac{A_2}{f_m^2} + \frac{A_3}{f_m^3}\right) \tag{2.33}$$

with

$$A_3 = 7.6 \times 10^6, \qquad A_2 = 21.7, \qquad A_0 = 9.8 \times 10^{-15}$$

Comparing Eq. (2.33) with (2.32), it can be seen that the $1/f_m$ slope term is missing. This is due to the phase noise meters noise floor of -140 dBc/Hz masking both $1/f_m$ and the constant terms of Eq. (2.32). Figure 2.39 shows the modeled phase noise [Eq. (2.33)] and its three terms together with the measured phase noise. Note that Eq. (2.32) states that the $1/f_m^2$ and $1/f_m^3$ sloped noise terms cross at $f_m = f_c$ (flicker noise corner). In the case of Fig. 2.39 the flicker noise corner is about 350 kHz.

2.4.4 Pulling and pushing

Oscillator *pulling* is defined as variation of the output frequency caused by a given variation of the output load. It is normally defined as the output frequency variation for a load with 2:1 standing wave radio (SWR) and any phase from 0 to 360°. High pulling values can be dangerous for PLL performance because mismatched loads make the frequency versus tuning voltage curve to be rippled. K_v is consequently affected by big variations in the tuning voltage, which cause the PLL to respond by presenting a large variation in its output frequency, even bigger than those shown in Fig. 2.36. Attenuators, high-isolation amplifiers,

isolators, and a combination of these have to be inserted between the VCO output and the load in order to minimize that risk.

Oscillators are also affected by output frequency variations caused by variations in the supply voltage. This characteristic is called *pushing*; it can increase VCO (and PLL) phase noise and/or generate spurs if noise and/or periodic disturbs are superimposed on the VCO bias supply voltage.

2.5 Reference Sources

A reference source oscillator is one of the key component of a PLL synthesizer. It provides the stability of the PLL output signal, and its phase noise strongly determines the output signal phase noise within the PLL bandwidth. The most common type of reference sources are crystal oscillators, although more stable components are available such as cesium or rubidium frequency standards but at a very high cost, size, and current consumption.

Crystal† oscillators are basically oscillators that employ a piezoelectric resonator, usually cut from quartz, as a resonating circuit. The main advantage of such a component is that its Q factor can be as high as 10^6 or more. A typical crystal oscillator scheme is like the oscillator of Fig. 2.29 where the thank circuit (components RT_1, DV_1, L_{tuning}, and C_{tuning} is replaced by a crystal resonator whose equivalent circuit is shown in Fig. 2.40. That circuit has a low-impedance series resonance frequency:

$$f_s = \frac{1}{2\pi\sqrt{L_s C_s}}$$

and one parallel resonant frequency given by

$$f_p = \frac{1}{2\pi\sqrt{L_s \frac{C_s C_p}{C_p + C_s}}}$$

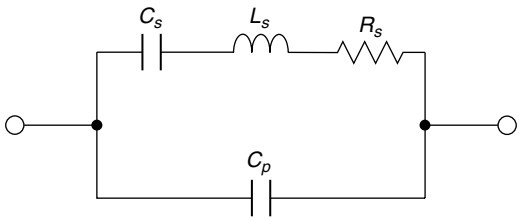


Figure 2.40 Equivalent circuit of a crystal resonator.

†Sometimes the word *crystal* is shortened to *Xtal*.

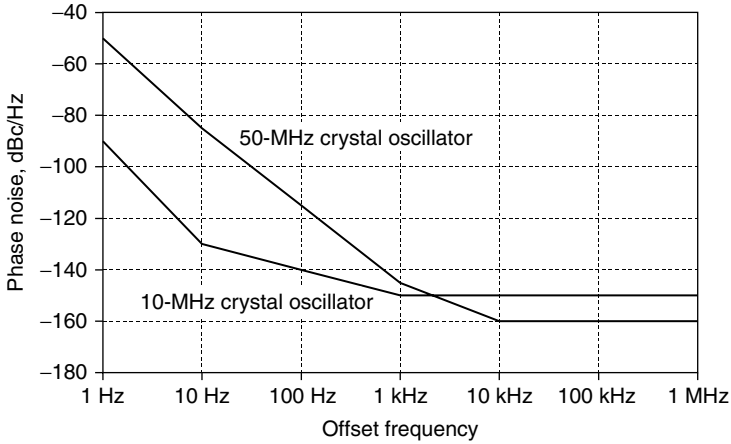


Figure 2.41 Phase noise of two crystal oscillators.

The parallel capacitance is usually some thousand times higher than the series capacitance, so series and parallel frequency resonant frequencies are very close to each other. Oscillators can use either parallel or series resonance.

Crystal resonators can have Q factors higher than one million as anticipated. If properly used, they can give very low phase noise oscillators as the Leeson equation predicts. The phase noise of two different crystal oscillators is plotted in Fig. 2.41.

A crystal oscillators output frequency ranges from a few tens of kilohertz to some hundreds of megahertz. For higher output frequencies, surface acoustic wave (SAW) resonators are used up to about 2 GHz, but SAW devices have lower Q factors compared with those of crystal resonators.

Several techniques are used to minimize frequency variations over the temperature changes in crystal oscillators. Three solutions are available with different costs and performances.

1. The variation in frequency due to the temperature characteristics of a crystal resonator is a function of the cut angle. The cut angle can be chosen in order to minimize frequency variations within a given temperature range. Variations of ± 5 parts per million (ppm) over a temperature range of 100°C can be achieved. Typical output frequency variation versus temperature curves are shown in Fig. 2.42 for different values of the cut angle.
2. Temperature compensated crystal oscillators (TCXO). In these circuits one varactor is added in series or in parallel with the crystal resonator. A temperature-dependent voltage is applied to that

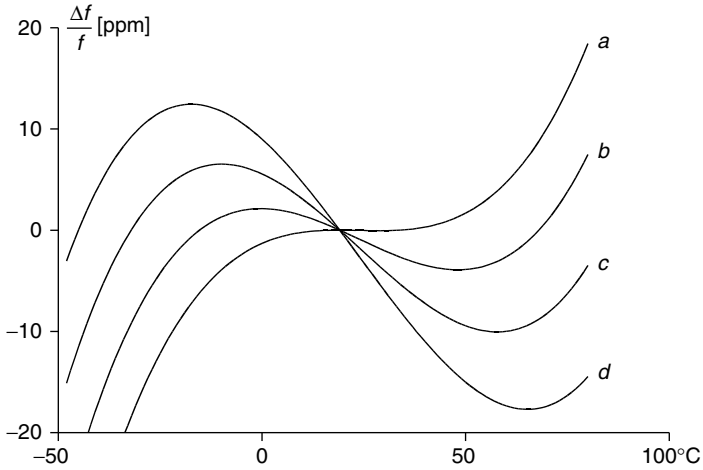


Figure 2.42 Crystal oscillator frequency versus temperature for different cut angles.

varactor to compensate for the temperature variation of the resonator. Variations of ±2 ppm over a temperature range of 100°C can be achieved. The major drawback of this technique is Q reduction due to the varactor loading the resonator resulting in phase noise degradation.

3. Oven controlled crystal oscillators (OCXO). The complete oscillator (including crystal resonator) temperature is stabilized at a value higher than the maximum working temperature by using electrical heaters. The output frequency becomes virtually constant over temperature. The current consumption is higher than for circuits 1 and 2 due to heater power dissipation.

Similarly to all other oscillators, crystal oscillators are affected by pulling and pushing; thus noise in the supply will increase the phase noise.

2.6 Frequency Dividers

In PLL frequency synthesizers, the VCO normally operates at a frequency higher than the reference frequency. The phase detector input signal comes from the VCO output via a frequency divider which divides the output frequency up to the reference frequency. The simplest frequency divider is the so-called T (toggle) flip-flop. It simply consists of one J-K flip-flop whose J and K inputs are connected to the "1" logic value. Its schematic and the input and output waveforms are shown in

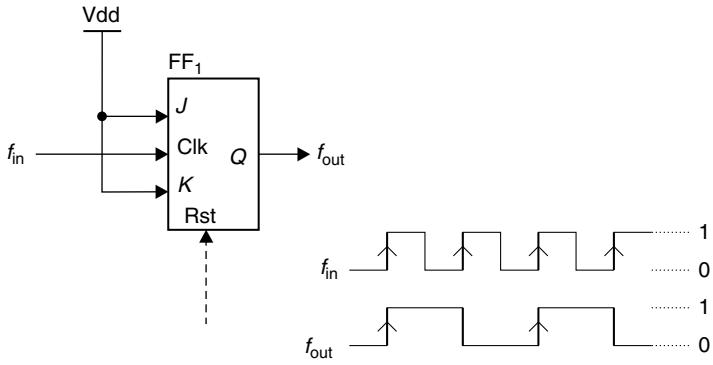


Figure 2.43 Toggle (T) flip-flop.

Fig. 2.43. The input signal is connected to the clock. The output toggles its state at each rising edge of the input signal; this way the output frequency is half of the input one.

Higher-frequency division factors can be obtained by cascading n toggle flip-flops. That circuit is known as a ripple counter. Figure 2.44

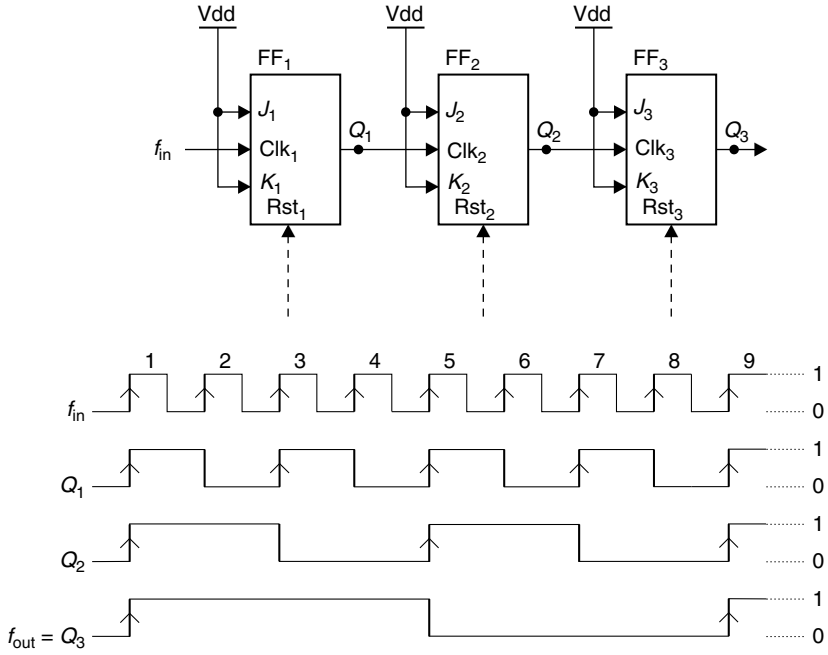


Figure 2.44 Ripple counter.

shows a schematic of a three-stage ($n = 3$) ripple counter and its waveforms. The output frequency equals the input frequency divided by 2^n; thus this configuration only allows division factors of 1, 2, 4, 8, etc. The circuit of Fig. 2.44 can of course be used to divide by 8, 4, 2, and 1 connecting the output to Q_3, Q_2, Q_1, and the input, respectively. A PLL synthesizer employing a ripple counter as a frequency divider can only generate output frequency values that are a reference frequency multiplied by an integer power of 2. A more flexible design would have a frequency divider that works for all integer values. This can be done by adding one combinatory network to the circuit of Fig. 2.44 as shown in Fig. 2.45. We can understand how this circuit works by observing the timing diagram of Fig. 2.44. It shows that voltages of a ripple counter (considered as a whole) are periodic with a period of 2^n multiplied by the period of the input signal. Output signal Q_3 can divide the input frequency for any integer in the range 1 to 2^n if counting is stopped before it is completed.

Depending on the required frequency division of 1, 2, 3, . . . , 7, counting has to be stopped before the second, third, fourth, . . . , eighth input rising edge, respectively. This can be done by resetting all the flip-flops

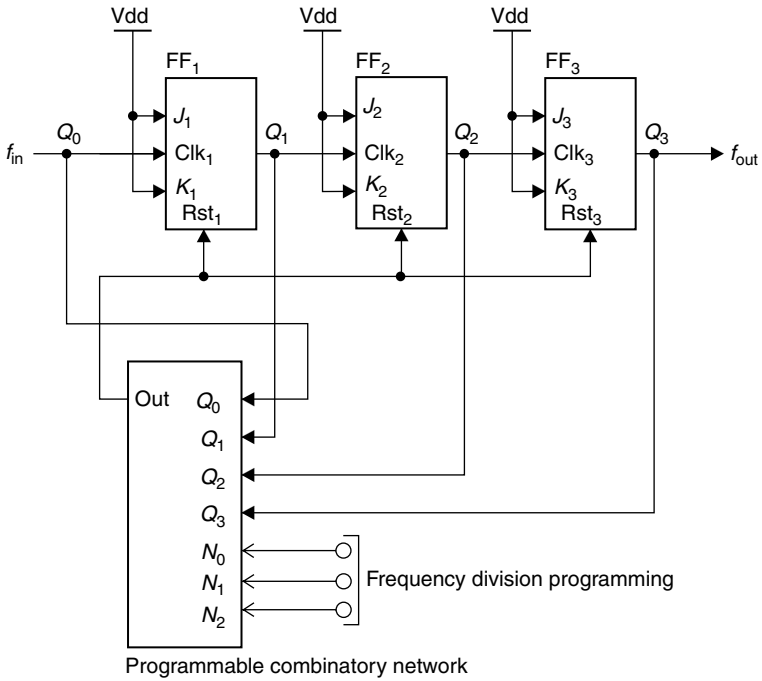


Figure 2.45 Three-bit programmable divider, $N = 1 \div 8$.

TABLE 2.2 Combinatory Logic for Different Division Factors

Rising edge no.	Q_1	Q_2	Q_3	Frequency division	Reset signal
1	1	1	1	1	$Q_1Q_2Q_3\overline{\text{Input}}$
2	0	1	1	2	$\overline{Q_1}Q_2Q_3$
3	1	0	1	3	$Q_1\overline{Q_2}Q_3$
4	0	0	1	4	$\overline{Q_1}Q_2Q_3$
5	1	1	0	5	$Q_1Q_2\overline{Q_3}$
6	0	1	0	6	$\overline{Q_1}Q_2\overline{Q_3}$
7	1	0	0	7	$Q_1\overline{Q_2}\,\overline{Q_3}$
8	0	0	0	8	Always 0

from their asynchronous reset input.† This way, counting is restarting after the first, second, third, . . . , seventh input rising edge. Thus the output waveform period equals the input period multiplied by 1, 2, 3, . . . , 7 (or 8 if an asynchronous reset signal is not used). If a division factor of $M < 2^n$ has to be obtained, a combinatory network has to recognize the ripple counter state after M input pulses and generate one reset signal before the $M + 1$ input rising edge arrival. Logic functions for reset signal generation in case of $n = 3$ are listed in Table 2.2 for any frequency division factor from 1 to 8. A programmable frequency divider is obtained if fixed combinatory logic is replaced by a programmable one in the circuit of Fig. 2.45. Since an n-stages ripple counter can divide up to 2^n, n bits are needed to program the frequency division factor. Programmable logic will have one output bit (reset signal), n input bits for programming (N_0, N_1, N_2 in Fig. 2.45), n input bits for connections to n flip-flop outputs (Q_1, Q_2, Q_3 in Fig. 2.45), and one input bit to be connected to the divider input (Q_0 in Fig. 2.45). The total number of bits is then $2n + 1$. The combinatory network has to realize different logic functions depending on the programming inputs. It can be implemented with a read-only memory (ROM); its contents are listed in Table 2.3.

The circuit of Fig. 2.45 has a maximum input frequency of working due to internal propagation delay. More precisely, a flip-flop has a propagation delay from the input rising edge to the output signal toggle $T_{\text{flip-flop}}$, a reset delay from the input to output T_{reset}, and a combinatory logic input-output propagation delay $T_{\text{combinatory}}$.

1. The counter needs time to complete its state (e.g., to propagate the rising edge from the input to the output of the last flip-flop) given by $nT_{\text{flip-flop}}$.

†See the following SIMETRIX files: FrequencyDivider_By1.sxsch, FrequencyDivider_By2.sxsch, FrequencyDivider_By3.sxsch, FrequencyDivider_By4.sxsch, and FrequencyDivider_By6.sxsch for simulation.

TABLE 2.3 Reset Signal Generation ROM

Frequency division factor	ROM inputs (address)							ROM output
	Input and flip-flop output				Division programming inputs			
	Q_0	Q_1	Q_2	Q_3	N_0	N_1	N_2	
1	0	1	1	1	0	0	0	1
2	—	0	1	1	1	0	0	1
3	—	1	0	1	0	1	0	1
4	—	0	0	1	1	1	0	1
5	—	1	1	0	0	0	1	1
6	—	0	1	0	1	0	1	1
7	—	1	0	0	0	1	1	1
8	—	—	—	—	1	1	1	0
All remaining combinations								0

2. The reset combinatory logic needs $T_{\text{combinatory}}$ time to generate a reset signal after the counter completes the proper configuration.
3. All flip-flops need T_{reset} time to reset their outputs after the reset signal arrives.
4. The total cycle time is the sum of times 1, 2, and 3: $T_{\text{cycle}} = nT_{\text{flip-flop}} + T_{\text{combinatory}} + T_{\text{reset}}$.

The reset process will begin after the Mth input rising edge and has to be completed after the $M+1$ input rising edge. The reset process has to be quicker than the input period, so

$$\frac{\text{Input frequency} < 1}{nT_{\text{flip-flop}} + T_{\text{combinatory}} + T_{\text{reset}}}$$

The maximum input frequency is decreasing as the divider number of stages is increasing (or the maximum division factor is increasing). The counter speed can be increased if a synchronous counter is used. The ripple counter shown in Fig. 2.44 is an asynchronous counter because all flip-flops use a different clock signal. The fastest possible counter configuration is the parallel carry synchronous counter[†] shown in Fig. 2.46. Since each flip-flop is using the same clock (input frequency), the counter propagation time is no longer the value 1 but is reduced to $T_{\text{flip-flop}} + T_{\text{AND}}$ where T_{AND} is the input-output propagation delay of AND gates (usually a lot shorter than $T_{\text{flip-flop}}$). A programmable divider based on a synchronous counter has the same schematic of

[†]See the SIMETRIX file SynchronousCounter_ParallelCarry.sxsch for simulation.

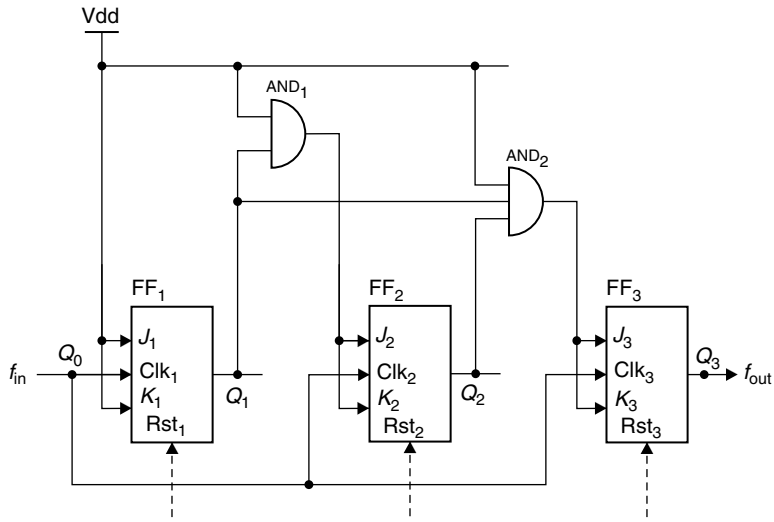


Figure 2.46 Parallel carry three-stage synchronous counter.

Fig. 2.45 but with the ripple counter (FF_1, FF_2, and FF_3) replaced by the synchronous counter of Fig. 2.46. Its maximum input frequency is then

$$\text{Input frequency} < \frac{1}{(T_{\text{flip-flop}} + T_{\text{AND}} + T_{\text{combinatory}} + T_{\text{reset}}}$$

and is no longer depending on the number of stages.

Even when it has synchronous counters, a programmable frequency divider has a maximum input frequency on the order of some tens of megahertz when CMOS or transistor-transistor logic (TTL) technology is used. Faster emitter coupled logic (ECL) logic can be used, but its high current consumption and low integration capability is a problem in most applications. For higher-frequency synthesizers, the arrangement shown in Fig. 2.47 can be used. A fast logic frequency divider is inserted between the VCO output and the programmable divider input. This device is commonly called a prescaler, and it supplies a frequency division factor P (usually 32, 64, 128, and higher powers of 2). This way the programmable divider input frequency is kept below its operating limits even if the VCO frequency reaches gigahertz values. The global frequency division factor is MP where M is programmable and can assume any integer value from 1 to 2^n, while P is a fixed value. The division step is thus P, and the output frequency step will be Mf_{ref}. If a smaller step is required, a lower reference frequency has to be used with consequent limitations on the PLL bandwidth as explained in Sec. 3.1.

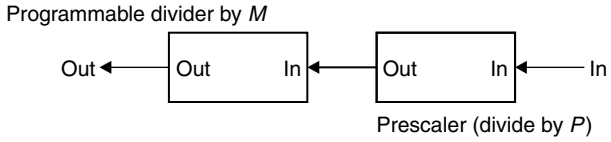


Figure 2.47 Programmable frequency divider with high-frequency prescaler.

To extend the frequency range beyond programmable divider limits without increasing the frequency step, a dual modulus prescaler has to be used. Such a configuration is shown in Fig. 2.48. The circuit consists of four blocks:

- Two programmable frequency dividers A and M like those in Fig. 2.45 (thus operating up to 10–50 MHz).
- One high-frequency dual modulus prescaler which divides by P or $P + 1$ depending on whether the modulus control (MC) level is high or low. Dual modulus prescalers are also referred to as pulse swallow counters.
- One set-reset flip-flop.

The MC level will be low at the beginning of a count cycle and will remain low until the :A counter has counted down from its programmed value. At this time, the MC goes high and remains high until the :M counter has counted the rest of the way down from its programmed value. The MC is then set back to low, the counters preset to their

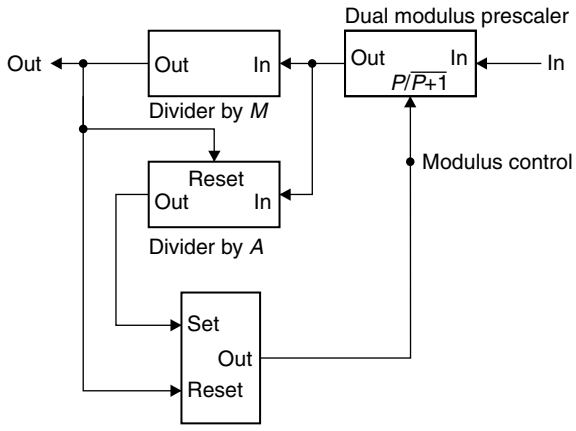


Figure 2.48 Frequency divider with dual modulus prescaler.

respective programmed values, and the sequence is repeated. The cycle can be divided into two portions:

- The first portion is from the beginning to the end of :A counting down. During this time the MC signal is low and the dual modulus prescaler is dividing by $P + 1$. This takes A rising edges from the prescaler output and thus $(P + 1)A$ from the prescaler input.
- The second is from the end of :A counting down to the end of :M counting down. During this time the MC signal is high and the dual modulus prescaler is dividing by P. This takes $M - A$ rising edges from the prescaler output and thus $P(M-A)$ from the prescaler input.

The total cycle takes $N = (P + 1)A + P(M - A)$ periods of the input signal to generate one pulse at the output of the :M divider. The frequency division factor is thus

$$N = A + MP \tag{2.34}$$

Since both A and M are programmable, N is programmable as well, and it is incremented by 1 or P (P is usually an integer power of 2, $P = 16$, 32, 64, or 128) if A or M are incremented by 1, so A and M represent fine and coarse frequency division steps, respectively. A has to be programmable from zero to $P - 1$ in order to make N assume all integer values. From the previous description of the counting cycle it follows that :A counting has to end before the :M one. This implies $M > A$. If all integer frequency division factors have to be covered, the above inequality has to be verified for any A. This means that $M > P - 1$ and consequently that the minimum achievable frequency division factor is given by Eq. (2.34) when both A and M assume their minimum value (0 and P, respectively) $N_{\min} = P^2$. So the higher is P, the lower the frequency is at the programmable divider inputs, but the higher the minimum division factor as well, and vice versa.

Insertion of a microwave prescaler (usually fixed) will further extend the operation frequency of pulse swallow dividers up to microwave frequencies even if at the expense of a reduction in the frequency resolution.

2.6.1 Frequency divider phase noise

It can be demonstrated that the phase noise level at the input of an ideal frequency divider (multiplier) is reduced (increased) by N at the divider (multiplier) output where N is the division (multiplication) factor. Referring to the dB expression, a term $20\log_{10}(N)$ has to be subtracted from the divider output signal or added to the multiplier output signal. It follows that the signal output of a cascaded ideal frequency

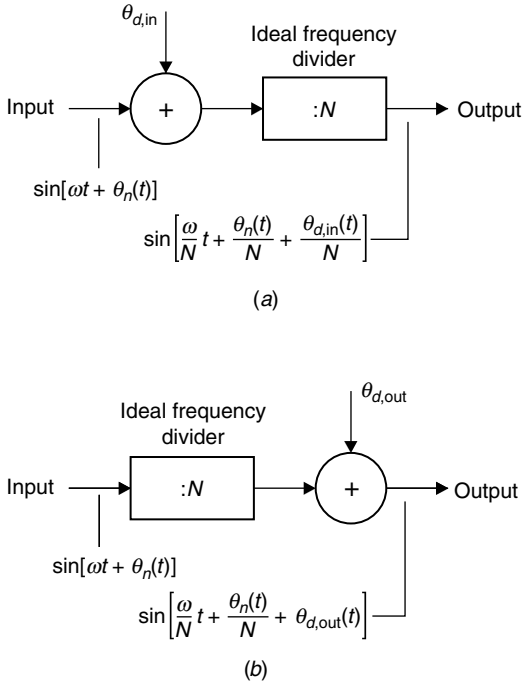


Figure 2.49 Frequency divider phase noise representations. (*a*) Phase noise referred to output. (*b*) Phase noise referred to input.

multiplier and divider with the same factor is identical to that at the input, including phase noise, and this consequence is quite reasonable. A real frequency divider exhibits an internal phase noise contribution which adds to the output signals. Frequency divider phase noise can be represented by a phase noise source added to the input or output as shown in Fig. 2.49*a* and *b*, respectively.

The output phase noise of the circuit in Fig. 2.49*a* is

$$\theta_{\text{out},A} = \frac{\theta_n}{N} + \frac{\theta_{d,\text{in}}}{N}$$

while that of the circuit in Fig. 2.49*b* is

$$\theta_{\text{out},B} = \frac{\theta_n}{N} + \theta_{d,\text{out}}$$

where θ_n is the phase noise of the input signal and $\theta_{d,\text{in}}$ and $\theta_{d,\text{out}}$ are the input and output equivalent phase noises of the frequency divider.

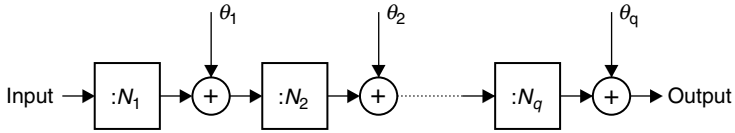


Figure 2.50 Model for phase noise performance calculation of q cascaded dividers.

Two expressions and consequently two circuits A and B coincide if

$$\theta_{d,\,\text{out}} = \frac{\theta_{d,\,\text{in}}}{N}$$

The phase noise of several cascaded frequency dividers can be calculated by analyzing the diagram of Fig. 2.50 where the output noise source representation was chosen.

The output phase noise is given by

$$\theta_{\text{out},B} = \frac{\theta_1}{N_2N_3N_4\cdots N_q} + \frac{\theta_2}{N_3N_4\cdots N_q} + \theta_q = \sum_{k=1}^{q}\theta_k \prod_{j=k+1}^{q}\frac{1}{N_q} \tag{2.35}$$

Note that the contribution to the global noise source of q cascaded frequency dividers is due to a given divider increasing as the divider gets close to the output: This is exactly the opposite of what happens with the noise figure of cascaded amplifiers.

From these considerations it follows that to compare performances of different frequency dividers, it is important to characterize devices with the same input frequency and division factors. Figure 2.51 shows typical

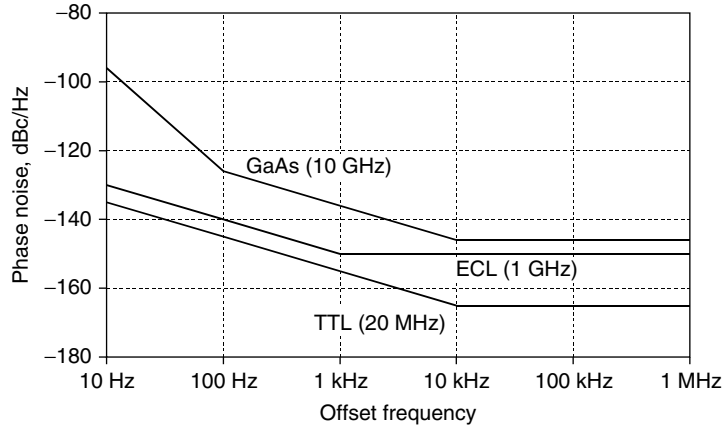


Figure 2.51 Typical output phase noise of a :8 frequency divider.

output noise of three frequency dividers dividing by 8 and with input frequencies from 10 MHz to 10 GHz. Note that the higher the input frequency, the higher the noise. The good news comes from Eq. (2.35); i.e., a higher noise divider (one with higher input frequency) has a less important contribution to global noise.

Most general frequency divider chains for a microwave synthesizer include one GaAs divider that divides the input frequency from about 10 GHz down to about 1 or 2 GHz, one ECL (or equivalent technology) dual modulus prescaler with output frequency around 10 MHz, and two TTL or CMOS programmable frequency dividers operating together with the dual modulus prescaler. All of the mentioned dividers can have different voltages for the logic high and low levels. Level translators have to be inserted if needed. Modern technology offers integrated circuits which include all components needed for the schematic of Fig. 2.48. Together with a phase frequency detector, the integrated PLL input dynamic range is typically in the order of 0 to 25 dBm, and GaAs output levels are generally compatible with that range.

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Chapter

3

Fractional-*N* Frequency Divider

3.1 Introduction

The principal limit of the standard PLL is that the output frequency can assume only integer multiples of the reference frequency. Thus the resolution frequency equals the reference frequency. If fine resolution is needed, a low reference frequency has to be chosen, which means there will be a narrow PLL closed-loop bandwidth which leads to a slow output frequency settling and a small VCO phase noise reduction.[†] The fractional-N technique has been developed to circumvent this obstacle.

Single- and multiple-accumulator fractional dividers are examined in this chapter. The origin of fractional spurs is explained, and analog and digital compensation techniques are also discussed. So far full digital multi-accumulator fractional divider architecture appears to be the best-performing one. Special consideration is given to the multi-accumulator configuration; it is analyzed by applying equations originally derived for sigma–delta modulators and using an analogy between the two systems. The implication of fractional dividers on PLL design is also discussed.

3.2 Single-Accumulator Fractional Divider

A fractional-N synthesizer is essentially a synthesizer where the frequency divider divides by an integer plus a fraction—not just an integer. Since the frequency divider can only divide by integer factors, the

[†]See Chap. 4.

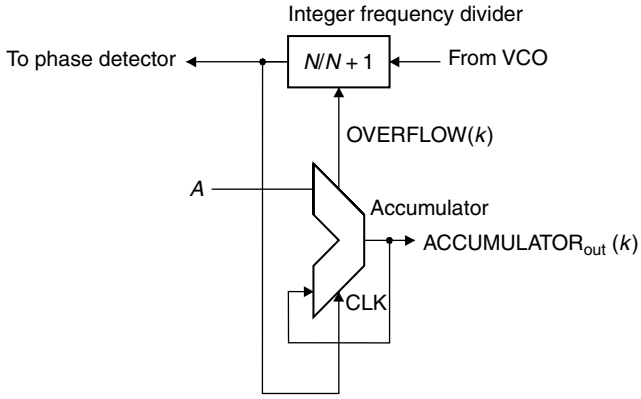

Figure 3.1 Fractional-N frequency divider.

required fractional division is obtained by averaging a time-varying division factor over a time interval. The basic idea is to cyclically switch between N and $N+1$. The frequency divider divides by $N+1$ every A reference periods and by N the rest of the $Q-A$ reference periods. The average division factor over Q reference signal periods is the effective division ratio given by

$$N^* = N + \frac{A}{Q} \tag{3.1}$$

This means that the synthesizer output frequency can be a fractional multiple of the reference frequency. N is the integer part of the division factor. A/Q is a rational number that can assume values between 0 and 1; it is the fractional part of the division factor. Figure 3.1 shows one possible realization of the fractional-N frequency divider. The accumulator is clocked by the divided VCO frequency. At each reference clock period, the accumulator sums modulo Q the binary number A to its output value. If the accumulator overflows, the frequency division is increased by 1 passing from N to $N+1$.

Operation of the accumulator fractional divider can be explained with the following two examples.

Example 3.1 The $A=3$, $Q=8$ accumulator output sequence is

```
Reference cycle = 1 2 3 4 5 6 7 8 9 ...
ACCUMULATOR =     0 3 6 1 4 7 2 5 0 ...
OVERFLOW =        1 0 0 1 0 0 1 0 1 ...
```

Repetitive sequence of 8 cycles, 3 overflows each 8 cycles.

Example 3.2 $A = 2$, $Q = 8$ accumulator output sequence is

```
Reference cycle = 1 2 3 4 5 6 7 8 9 ...
ACCUMULATOR =     0 2 4 6 0 2 4 6 0 ...
OVERFLOW =        1 0 0 0 1 0 0 0 1 ...
```

Repetitive sequence of 4 cycles, 2 overflows each 8 cycles.

The results of Examples 3.1 and 3.2 can be generalized as follows: If A is the addendum and Q is the modulo of the accumulator, the waveforms are periodic with period Q and with A overflows per period. If Q is an integer multiple of A, the period becomes Q/A. The frequency division factor averaged on Q reference periods is consequently given from Eq. (3.1) with the above described meaning of Q and A. One of the main consequences is that the fractional-N frequency resolution is given by the reference frequency divided by the accumulator size rather than by the reference frequency alone. Providing that the accumulator size Q is large enough, the PLL resolution can be arbitrarily reduced keeping the reference signal frequency as high as needed. The major drawback of this technique is that the frequency at the output of the frequency divider is modulated by the OVERFLOW signal. This makes the phase detector output generate a beat note that frequency modulates the VCO. Given a reference frequency f_r and the frequency of the signal at the output of frequency divider f_v, if the PLL is a locked VCO, we have

$$f_v = \begin{cases} f_r \left(N + \frac{A}{Q}\right) \frac{1}{N} > f_r & \text{if OVERFLOW} = 0 \\ f_r \left(N + \frac{A}{Q}\right) \frac{1}{N+1} < f_r & \text{if OVERFLOW} = 1 \end{cases}$$

The VCO divided frequency is always higher or lower than the reference one. The PLL phase error increases by the frequency difference multiplied by the reference period and by 2π at each reference period:

$$\Delta\varphi = 2\pi(f_r - f_v)\frac{1}{f_v} = 2\pi\left(\frac{f_r}{f_v} - 1\right)$$

or

$$\Delta\varphi = \frac{1}{N + A/Q}\frac{2\pi}{Q}\begin{cases} -A & \text{(if OVERFLOW = 0)} \\ Q - A & \text{(if OVERFLOW = 1)} \end{cases} \tag{3.2}$$

The error signal is a staircase waveform. Each step is negative or positive depending on whether OVERFLOW = 0 or 1. Phase error steps

generate corresponding steps on the phase detector output signal. Their amplitude is given by the phase error multiplied by the phase detector gain:

$$\Delta n_{\text{DET}}^{\text{FRAC-N}} = \Delta\varphi\, K_d = \frac{1}{N + A/Q}\frac{2\pi}{Q}K_d \begin{Bmatrix} -A & \text{if OVERFLOW} = 0 \\ Q - A & \text{if OVERFLOW} = 1 \end{Bmatrix}$$

The explicit waveform expression can be calculated from incremental values considering that the accumulator incremental output values are the exact opposite of the factor between the braces:

$$n_{\text{DET}}^{\text{FRAC-N}}(t) = -\frac{1}{N + A/Q}\frac{2\pi}{Q}K_d \cdot \text{ACCUMULATOR}_{\text{out}}(t) \tag{3.3}$$

The effect of this waveform is to push the VCO frequency down and up around its average value, i.e., to frequency modulate it. Frequency modulation affects the synthesized spectrum exactly like a noise added to the phase detector output. The frequency response from this source to the output spectrum is given by[†]

$$\frac{\varphi_{\text{OUT}}}{n_{\text{DET}}} = \frac{N^*}{K_d}H(f)$$

The synthesizer output phase error spectrum is

$$\varphi_{\text{OUT}}^{\text{FRAC-N}}(f) = n_{\text{DET}}^{\text{FRAC-N}}(f)\frac{N + A/Q}{K_d}H(f) \tag{3.4}$$

or

$$\varphi_{\text{OUT}}^{\text{FRAC-N}}(f) = \frac{2\pi}{Q}\,\text{ACCUMULATOR}_{\text{out}}(f)H(f) \tag{3.4′}$$

Spectral components of Eq. (3.4) can be calculated with the following considerations. It was previously found that accumulator outputs are discrete-time periodic sequences with period Q/f_r in the most general case. The discrete fourier transform (DFT) of those sequences can be calculated over one period. Points of the sequence are spaced over time by $1/f_r$. The sampling frequency is then f_r; and hence the maximum frequency of DFT is $f_r/2$. Time sequences have Q samples within

[†]See Eq. (4.6).

$$\Theta_o = NH(f)\Theta_r + \frac{N}{K_d}H(f)n_{\text{DET}} + \frac{N}{K_d}\frac{H(f)}{F(f)}n_{\text{FILT}} + [1 - H(f)]n_{\text{VCO}} - NH(f)n_{\text{DIV}}$$

where the integer division factor N has to be replaced by Eq. (3.1).

one period, so the corresponding DFTs have $Q/2$ terms. The conclusion is that the accumulator waveform spectra have $Q/2$ spectral components from 0 to $f_r/2$ spaced by fundamental frequency f_r/Q. The fractional-N phase error spectrum contains the same discrete lines filtered by the PLL closed-loop response. In order to filter out all error signal spectral components, the PLL closed-loop bandwidth needs to be narrower than f_r/Q. This condition is the same as that coming from one integer-N PLL having a reference frequency f_r/Q which has the same frequency resolution. So far it seems that nothing was gained from fractional-N. To keep the potential advantage of the fractional-N synthesizer, techniques are needed for phase error compensation.

The first of those consists of injecting the opposite signal of Eq. (3.3) into the phase detector output. It will cancel fractional-N associated frequency modulation. The correction signal can be taken from the accumulator output whose waveform has the same phase error shape, but with one different multiplying constant. The circuitry basically consists of one digital-to-analog converter (DAC) followed by one gain-controlled amplifier whose output (voltage or current depending on the phase detector output type) is summed to the phase detector. The DAC and amplifier have to multiply the accumulator by the factor Knf calculated from Eq. (3.3):

$$\begin{aligned} \text{Knf} \times \text{ACCUMULATOR}_{\text{out}}(t) = -n_{\text{DET}}^{\text{FRAC-N}}(t) \Rightarrow \text{Knf} \\ = \frac{1}{N + A/Q} \frac{2\pi}{Q} K_d \end{aligned} \tag{3.5}$$

The basic block diagram is shown by Fig. 3.2.

The analog compensation circuitry has to apply one correction factor which depends on the frequency division factor. The error canceling performance will be affected by the temperature, aging, and the components' tolerance. One other disadvantage of this kind of compensation technique is the difficulty of getting the correct timing of compensating waveforms. Some calculation on accumulator waveforms, compensation waveforms, and tolerance on compensating circuitry can be made with MATHCAD.†

An 8-bit accumulator ($Q = 256$) was considered; it was also supposed that $A = 11$. Figure 3.3 shows the accumulator output and overflow waveforms. Note that there are 11 overflows each 256 time steps.

Figure 3.4 shows the fractional-N phase error and accumulator output multiplied by factor $(2\pi/Q)/(N + A/Q)$. The first curve lays below the x axis, the second above. Note that the two curves are opposite each

†See the file AccumulatorNfractional.MCD.

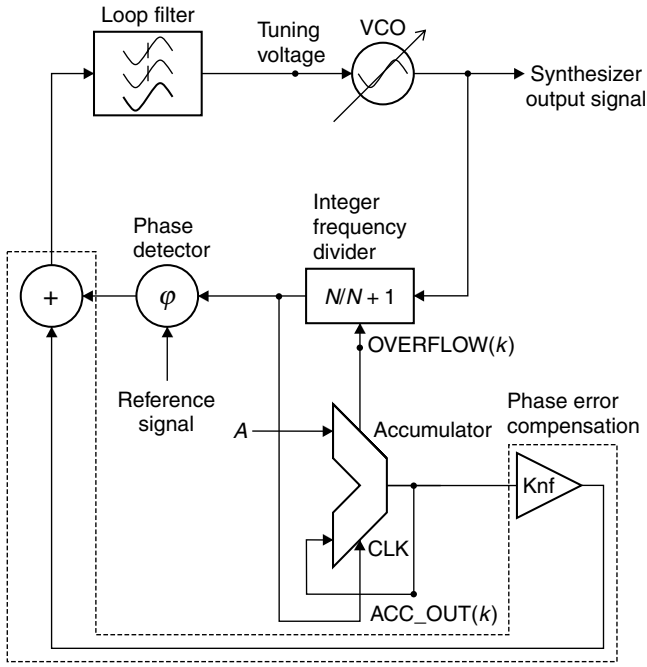

Figure 3.2 Fractional-N PLL with analog phase error compensation.

other. Figure 3.5 shows the magnitude of the phase error spectrum. The abscissa is the offset frequency normalized to the reference frequency.

Regarding the effect of the nonexact amplitude and the time compensation waveform, we found that multiplying the accumulator output by

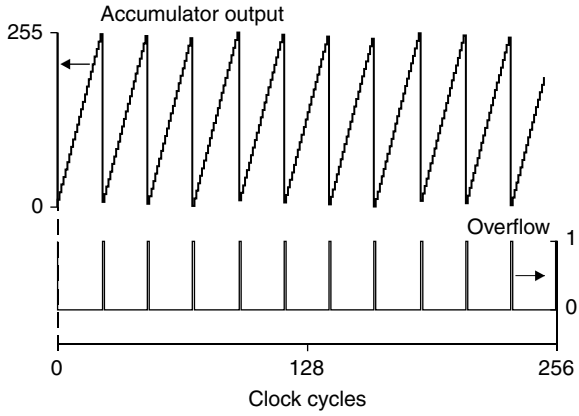

Figure 3.3 Accumulator output and overflow ($A = 11$, $Q = 256$).

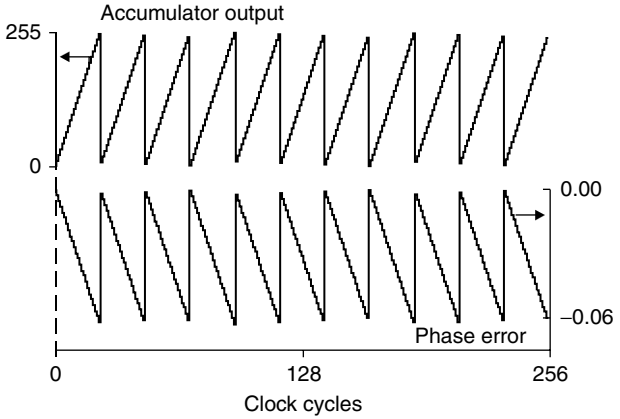

Figure 3.4 The upper trace is the accumulator output, and the lower trace is the phase error.

factor Knf given by Eq. (3.5) and adding this signal to the phase detector output will result in a complete cancellation of the fractional-N phase error. In practice neither the amplitude or the timing of the correction signal will be exact. So the phase error after correction will be

$$n_{\mathrm{DET}}^{\mathrm{RESIDUAL}}(t, K, T_d) = \frac{1}{N + A/Q}\frac{2\pi}{Q}K_d ACCUMULATOR_{\mathrm{out}}(t) - ACCUMULATOR_{\mathrm{out}}(t - T_d)(1 - K)$$

K is a factor that takes into account the nonexact amplitude of the error correction signal: $K = 0$ means no correction; $K = 1$ means exact

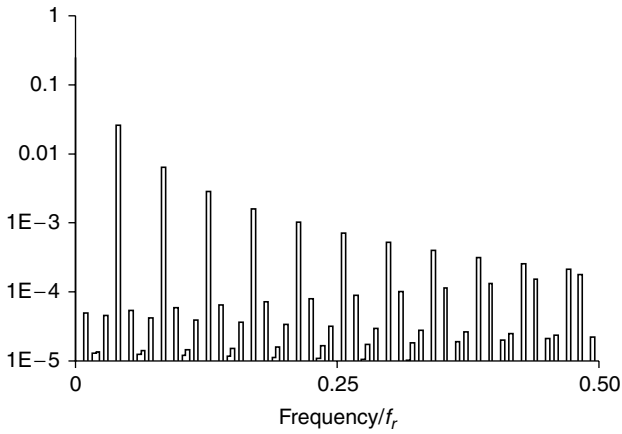

Figure 3.5 Fractional-N phase error spectrum.

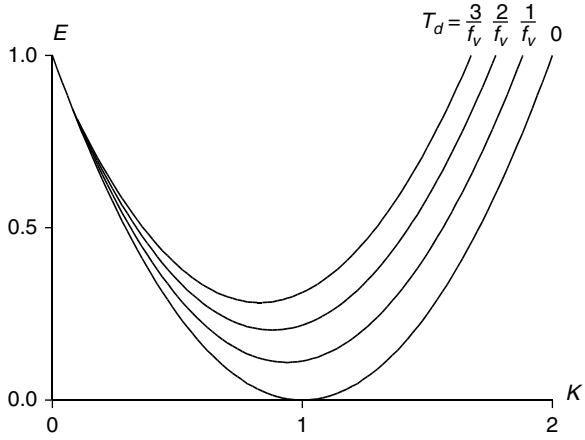

Figure 3.6 Fractional-N phase error relative power for non-perfect compensation.

amplitude. T_d represents the time shift between the error and error correction signals.

The phase error total power is given by

$$\varepsilon(K, T_d) = \frac{1}{Q} \sum_{k=0}^{Q-1} \left[n_{\text{DET}}^{\text{RESIDUAL}} \left(k \frac{1}{f_r}, K, T_d \right) \right]^2 \tag{3.6}$$

If $K = 0$, Eq. (3.6) gives the error power without correction, so the correction's effectiveness can be measured with the following ratio:

$$E = \frac{\varepsilon(K, T_d)}{\varepsilon(0, T_d)}$$

The ratio is plotted in Fig. 3.6.

Another possible technique for fractional-N phase error compensation is to add a time-variable phase delay stage between the frequency divider output and the phase detector input; it compensates for the accumulated integer and reduces spurious levels. This technique is still affected by the amplitude and phase error and tends to increase phase noise.

3.3 Multiple-Accumulator Fractional Dividers

More recently, new totally digital techniques have been developed, which are not sensitive to aging and tolerance. The basic idea is the one used by the sigma-delta ($\Sigma - \Delta$) analog-to-digital converter (ADC).

That technique will be discussed showing the perfect analogy of 1-bit $\Sigma - \Delta$ ADC and the accumulator-based frequency division modulator of Fig. 3.2.

3.3.1 *Z* transform

The Z transform is a widely used method for analysis of time-invariant discrete-time systems. Let $f(t)$ be a function defined for discrete values of the variable $t = kT_s$ with k assuming all negative and positive integer values and where T_s is the sampling interval. The Z transform of $f(t)$ is defined as

$$F(z) = Z[f(t)] = \sum_{k=-\infty}^{+\infty} f(kT_s)z^{-k} \qquad \text{Definition of } Z \text{ transform}$$

From the definition we get the following:

$$Z[f(t - T_s)] = \frac{1}{z}Z[f(t)] \qquad Z \text{ transform of delayed sequence}$$

z is a complex variable and can be written in cartesian form, $z = x + jy$, or polar form, $z = \rho \exp(j\phi)$. The Z transform is a series that converges if $\rho < \rho_{\max}$ (circle of convergence). If the circle of convergence includes the unit circle ($\rho_{\max} > 1$), a special case of the unit magnitude z variable can be considered, $z = \exp(j2\pi T_s)$. The Z transform expression becomes

$$F[z = \exp(j2\pi f\, T_s)] = \sum_{k=-\infty}^{+\infty} f(kT_s)\exp(jk2\pi f\, T_s)$$

which is the DFT of $f(t)$. The delayed sequence transform becomes

$$Z[f(t - T_s)] = Z[f(t)]\exp(-j2\pi f\, T_s)$$

The preceding relation coincides with the Fourier transform of the function translated by one sampling time T_s. In the following calculations of this chapter it will always be assumed that the convergence of the Z transform is within the unit circle, and the Z transform will be considered as a compact way to write the DFT.

3.3.2 First-order Σ-Δ modulator

Figure 3.7 shows a block diagram of a first-order Σ-Δ modulator. It contains one difference operator, one unit delay element, one discrete integrator, and one 1-bit quantizer whose output is the sum of the input and quantization noise Eq 1.

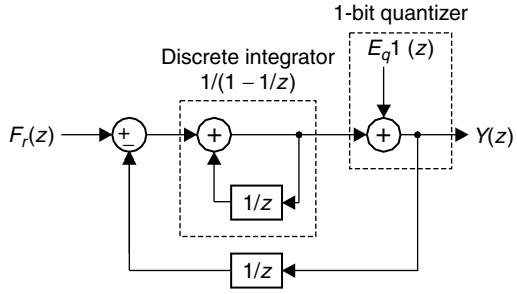

Figure 3.7 First-order Σ-Δ modulator.

Let us calculate the discrete-time integrator transfer function in the Z domain. Assuming that $g(t)$ is the discrete-time integration of $f(t)$, it is possible to find a recursive relation between the integrand and integral:

$$g(nT_s) = \sum_{k=-\infty}^{n} f(kT_s) = f(nT_s) + \sum_{k=-\infty}^{n-1} f(kT_s) = f(nT_s) + g[(n-1)T_s]$$

Discrete-time signals and systems can easily be represented with the Z transform. Using capital letters to denote the Z-transformed function, e.g., $F(z) = Z[f(t)]$ and $G(z) = Z[g(t)]$, and using the time-delay property of the Z transform, $Z[g(t-T)] = \frac{1}{z}Z[g(t)]$, we can write

$$G(z) = F(z) + \frac{1}{z}G(z) \Rightarrow \left(1 - \frac{1}{z}\right) G(z) = F(z)$$

Thus

$$G(z) = \left(1 - \frac{1}{z}\right)^{-1} F(z) \tag{3.7}$$

Let us calculate the relation between the input and output of a first-order Σ-Δ modulator. It is given by Eq. (3.8).

$$\begin{aligned} Y(z) &= \frac{\left(1 - \frac{1}{z}\right)^{-1}}{1 + \frac{1}{z}\left(1 - \frac{1}{z}\right)^{-1}} F_r(z) + \frac{1}{1 + \frac{1}{z}\left(1 - \frac{1}{z}\right)^{-1}} E_q 1(z) \\ &= \frac{F_r(z)}{1 - \frac{1}{z} + \frac{1}{z}} + \frac{E_q 1(z)}{1 - \frac{1}{z} + \frac{1}{z}} \\ Y(z) &= F(z) + \left(1 - \frac{1}{z}\right) E_q 1(z) \end{aligned} \tag{3.8}$$

The output signal is the sum of two terms: The first is the input; the second is the 1-bit ADC quantization noise which is frequency shaped by the factor $(1 - 1/z)$. That factor is the Z-domain transfer function of the discrete-time differentiator and is the reciprocal of the discrete-time integrator given by Eq. (3.7).

The quantization noise power density can be computed by passing from the Z transform to the DFT:

$$1 - \frac{1}{z} \rightarrow 1 - \exp(-j\omega T_s) = \exp\left(-j\frac{\omega T_s}{2}\right) 2j \sin\left(\frac{\omega T_s}{2}\right)$$

Let $E_1(f)$ and $E_{1,\Sigma\Delta}(f)$ be the quantization noise power density of a 1-bit quantizer and a first order Σ-Δ modulator, respectively. The relation between the two functions is given by

$$E_{1,\Sigma\Delta}(f) = 4\sin^2\left(\pi\frac{f}{f_s}\right) E_1(f) \tag{3.9}$$

The 1-bit quantizer output equals q (or 0) if input $> q/2$ (or $< q/2$). If the input amplitude probability is uniformly distributed in the range $[0; q]$, the quantization noise will be uniformly distributed between $-q/2$ and $+q/2$.

Let $p(e_q)$ be the density of the probability of quantization error e_q. Then the quantization noise power is given by the quantization noise variance:

$$P_1 = \int_{-0.5q}^{0.5q} eq1^2 p(eq) d(eq1) = \frac{1}{q}\int_{-0.5q}^{0.5q} eq1^2\, d(eq1)$$

$$= \frac{1}{q}\left[\frac{eq1^3}{3}\right]_{-0.5q}^{0.5q} = \frac{1}{q}\frac{1}{3}\left(\frac{q^3}{8} + \frac{q^3}{8}\right) = \frac{q^2}{12}$$

$$P_1 = \sigma_{\text{eq1}}^2 = \frac{q^2}{12} \tag{3.10}$$

Assuming that the 1-bit quantization noise density is constant over frequenies from $-f_s/2$ to $f_s/2$ (where f_s is the sampling frequency), $E_1(f)$ is given by

$$E_1(f) = \frac{q^2}{12}\frac{1}{f_s} \tag{3.11}$$

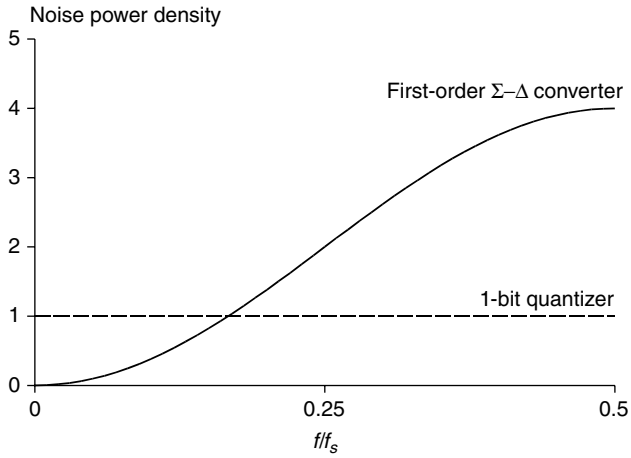

Figure 3.8 Quantization noise. (*a*) 1-bit quantizer, and (*b*) first-order Σ-Δ converter.

Consequently $E_{1,\Sigma\Delta}(f)$ is given by

$$E_{1,\Sigma\Delta}(f) = 4\sin^2\left(\pi\frac{f}{f_s}\right)\frac{q^2}{12}\frac{1}{f_s} \tag{3.12}$$

The first-order Σ-Δ converter total quantization noise can be calculated by integrating Eq. (3.12) over the frequency:

$$P_{1,\Sigma\Delta} = \int_{-f_s/2}^{f_s/2} E_{1,\Sigma\Delta}(f)\,df = \frac{q^2}{6}\frac{1}{f_s}\int_{-f_s/2}^{f_s/2} 2\,\sin^2\left(\pi\frac{f}{f_s}\right)df = \frac{q^2}{6}$$

$$P_{1,\Sigma\Delta} = \frac{q^2}{6} = 2P_1 \tag{3.13}$$

Compared with the 1-bit quantizer, the first-order Σ-Δ converter has double the total noise, but its density is pushed toward high frequencies. Figure 3.8 shows the quantization noise power density versus frequency for (*a*) a 1-bit quantizer and (*b*) a first-order Σ-Δ converter.

3.3.3 Higher-order Σ-Δ converters

The noise shaping property expressed by Eq. (3.8) suggests a way to combine more Σ-Δ converters in order to further reduce the low-frequency quantization noise power density. Figure 3.9 shows the block diagram of a third-order Σ-Δ converter. Consider its outputs $Y_1(z)$,

$Y_2(z), Y_3(z)$:

$$Y_1(z) = F_r(z) + \left(1 - \frac{1}{z}\right) Eq1(z)$$

$$Y_2(z) = -Eq1(z) + \left(1 - \frac{1}{z}\right) Eq2(z)$$

$$Y_3(z) = -Eq2(z) + \left(1 - \frac{1}{z}\right) Eq3(z)$$

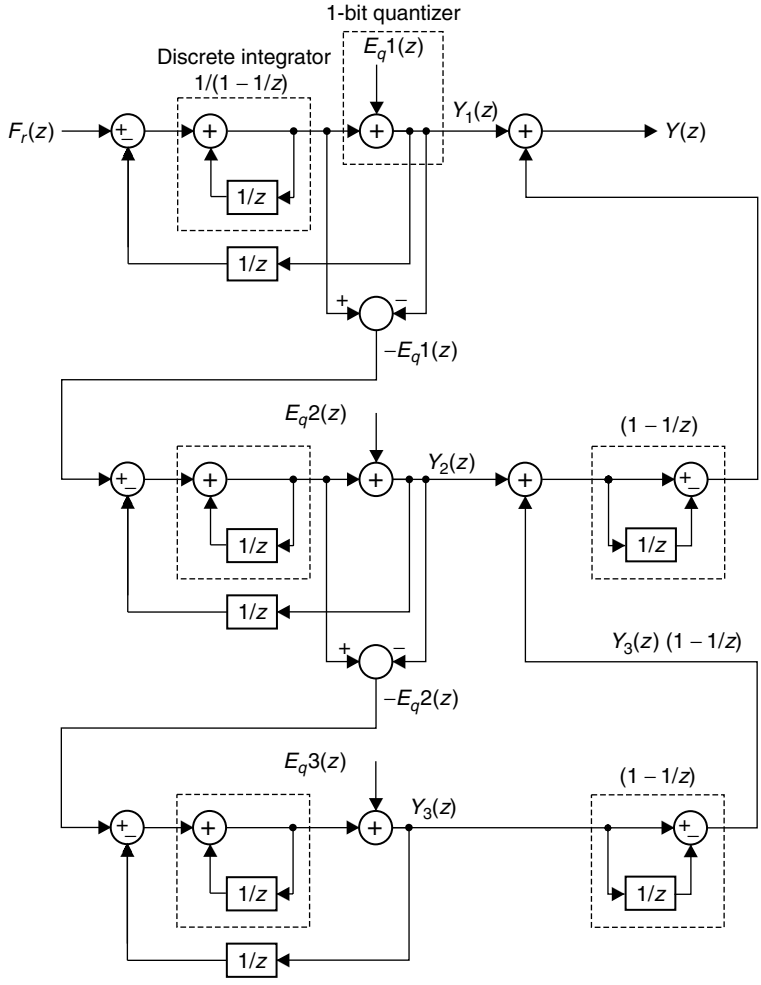

Figure 3.9 Third-order Σ-Δ converter.

Now, multiply $Y_1(z)$ by $1 = (1 - 1/z)^0$, $Y_2(z)$ by $(1 - 1/z)^1$, $Y_3(z)$ by $(1 - 1/z)^2$. Summing the resulting terms, we have

$$Y_1(z)\left(1-\frac{1}{z}\right)^0 = F(z) + \left(1-\frac{1}{z}\right)Eq1(z)$$

$$Y_2(z)\left(1-\frac{1}{z}\right)^1 = -\left(1-\frac{1}{z}\right)Eq1(z) + \left(1-\frac{1}{z}\right)^2 Eq2(z)$$

$$Y_3(z)\left(1-\frac{1}{z}\right)^2 = -\left(1-\frac{1}{z}\right)^2 Eq2(z) + \left(1-\frac{1}{z}\right)^3 Eq3(z)$$

and

$$Y(z) = Y_1(z)\left(1-\frac{1}{z}\right)^0 + Y_2(z)\left(1-\frac{1}{z}\right)^1 + Y_3(z)\left(1-\frac{1}{z}\right)^2$$

Thus,

$$Y(z) = F(z) + \left(1-\frac{1}{z}\right)^3 Eq3(z)$$

Generalizing the procedure applied for third-order Σ-Δ, we have that the M-order Σ-Δ modulator quantization noise power density and the total quantization noise power are given by Eqs. (3.14) and (3.15), respectively.

$$E_{M,\Sigma\Delta}(f) = \left[2\sin\left(\pi\frac{f}{f_s}\right)\right]^{2M}\frac{q^2}{12}\frac{1}{f_s} \tag{3.14}$$

$$P_{M,\Sigma\Delta}(f) = \frac{q^2}{12}\frac{2}{f_s}\int_{-f_s/2}^{f_s/2}\left[2\sin\left(\pi\frac{f}{f_s}\right)\right]^{2M} df$$

$$= P_1\frac{1}{\pi}\int_{f=-f_s/2}^{f_s/2}\left[2\sin\left(\pi\frac{f}{f_s}\right)\right]^{2M} d\left(\pi\frac{f}{f_s}\right)$$

$$= P_1\frac{1}{\pi}\int_{-\pi}^{\pi}\left[2\sin(x)\right]^{2M} dx$$

$$= P_1\frac{2}{\pi}\int_{0}^{\pi}\left[2\sin(x)\right]^{2M} dx \tag{3.15}$$

An M-order Σ-Δ modulator quantization noise power density normalized to a 1-bit quantizer is plotted on Fig. 3.10 (log scale on x and y). Note that all curves have one common point $[{}^1/_3(f/f_s); 1]$. The quantization

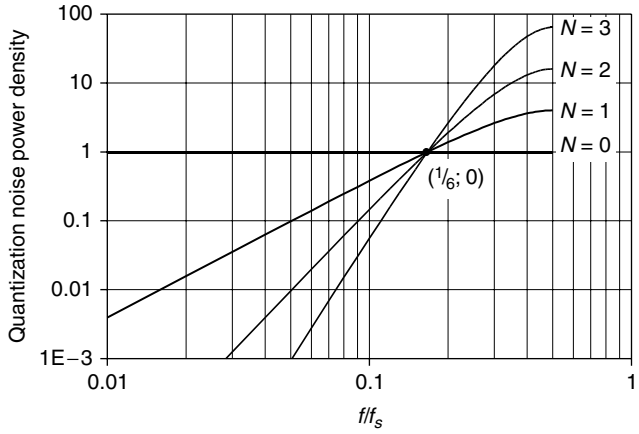

Figure 3.10 N order Σ-Δ modulator quantization noise power density.

noise power relative to the 1-bit quantizer is reported by Table 3.1 for $M = 1, 2, \ldots, 7$.

The Σ-Δ converter quantization noise power density given by Eq. (3.14) can be approximated for the low-frequency range. Since if $x \ll 1 \sin(x) \cong x$,

$$E_{M,\Sigma\Delta}(f) \cong 2^{2N} \frac{q^2}{12} \frac{1}{f_s} \left(\pi \frac{f}{f_s}\right)^{2M}$$

A three-stage Σ-Δ converter having the block diagram of Fig. 3.9 is also known as a multistage noise shaper or MASH. Summarizing, given one quantizer and one sampling frequency, an M-order Σ-Δ converter has a quantization noise power density proportional to the frequency raised to $2M$ and a total quantization noise power that increases with M.

TABLE 3.1 Total Quantization Noise Power for the *M* = order Σ-Δ Modulator

Σ-Δ modulator order M	Total quantization relative noise power†
0‡	1 (0 dB)
1	2 (3.01 dB)
2	6 (7.78 dB)
3	20 (13.01 dB)
4	70 (18.45 dB)
5	252 (24.01 dB)
6	924 (29.66 dB)
7	3432 (35.36 dB)

†Number in parentheses = $10 \log_{10}$ (number not in parentheses).
‡1-bit quantizer only.

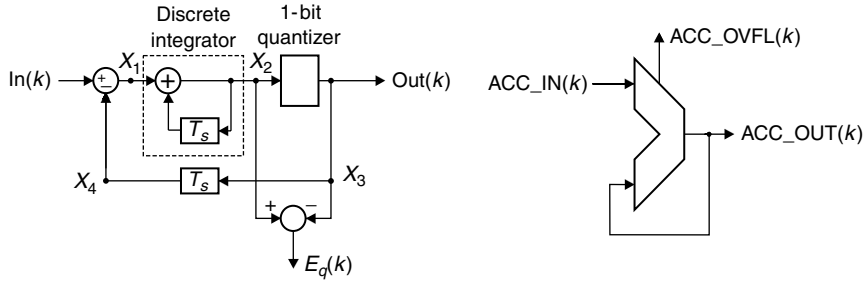

Figure 3.11 Time-domain first-order Σ-Δ modulator and accumulator block diagrams.

Comparing first-order Σ-Δ modulator and accumulator waveforms, we can note that $E_q(k)$ is the same as the accumulator output ACC_OUT(k), and Out(k) has the same shape as the accumulator's overflow ACC_OVFL(k) multiplied by Q. Two circuits are shown in Fig. 3.11.

The calculation of first-order Σ-Δ modulator output waveforms can be done by implementing the following routine:

```
`All to zero at the beginning of the process
B(0) = C(0) = D(0) = 0
For k = 1 to Kmax
    X1(k) = A(k) - X3(k-1)    `Integrator input
    X2(k) = X1(k) + X2(k-1)   `Integrator output
    If X2(k)> Q Then           `Output
                X3(k) = Q
                Else
                X3(k) = 0
                End If
Next k
```

One possible implementation is the following Mathcad program[†]:

```
X := | X0,0 ← 0
     | X1,0 ← 0
     | X2,0 ← 0
     | X3,0 ← 0
     | for k ∈ 1 .. Kmax − 1
     |     | X0,k ← k
     |     | X1,k ← A - X3,k-1
     |     | X2,k ← X1,k+ X2,k-1
     |     | X3,k ← q if X2,k≥q
     |     | X3,k ← 0 ifX2,k< q
     | X
```

[†]See the file SigmaDelta1.MCD.

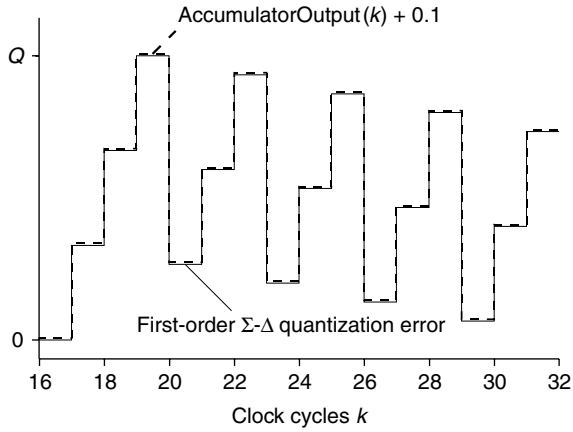

Figure 3.12 First-order Σ-Δ quantization error and accumulator output.

The accumulator output can be calculated with the following formulas:

$$ACC\_OUT_0 := 0$$

$$k := 1 .. K_{max} - 1$$

$$ACC\_OUT_k := \text{if } [ACC\_OUT_{k-1} + A < Q,\ ACC\_OUT_{k-1} + A,\ (ACC\_OUT_{k-1} + A) - Q]$$

$$ACC\_OVFL_0 := 0$$

$$ACC\_OVFL_k := \text{if } (ACC\_OUT_k > ACC\_OUT_{k-1},\ 0,\ 1)$$

One particular case is considered: $Q = 16$ and $A = 5$. This case is simple enough to calculate by hand and compare.

Figure 3.12 shows the Σ-Δ quantization error $E_{q,k}$ and the accumulator output. The two curves are identical. Figure 3.13 shows the accumulator output versus the time index k and the same curve translated by Q samples. The two curves are identical. The waveform is periodic over time with period Q as expected. Figure 3.14 shows Σ-Δ output X_3 and the accumulator overflow. In all plots the second curve is y shifted by 0.1 in order to help it to be distinguished from the first one. Variable k represents the discrete-time index. Different calculations can be done with different accumulator sizes Q and different input values. In any case output waveforms are periodic by Q time samples:

- $E_{q,k}$ = ACC_OUT$_k$
- $X_{3k}Q$ = ACC_OVFL$_k$
- X_3, ACC_OVFL have a duty cycle = A/Q

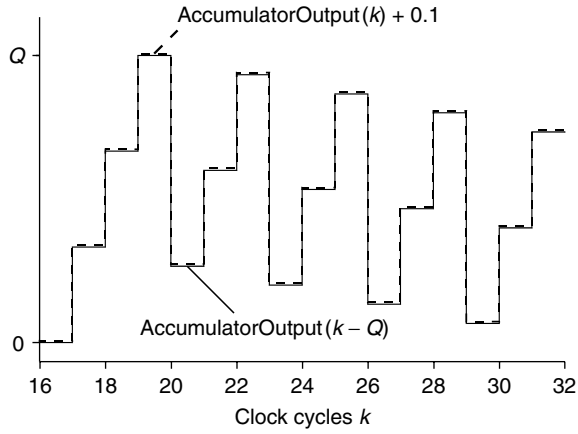

Figure 3.13 Normal and translated accumulator output.

3.3.4 Multiple-accumulator fractional-*N* phase noise

Given the correspondence between the first-order Σ-Δ converter and the accumulator circuit, the fractional-N circuit equivalent of the third-order Σ-Δ converter of Fig. 3.9 is shown by Fig. 3.15. It is a three-accumulator frequency divider circuit. In the single accumulator fractional-N divider, the frequency divider factor is increased by 1 each time the accumulator overflow occurs; in this case the control signal can be only 1 or 0. In a multi-accumulator fractional-N divider, the control signal OUT(k) may assume many different values. The instantaneous frequency division factor consequently assumes more values. OUT(k)

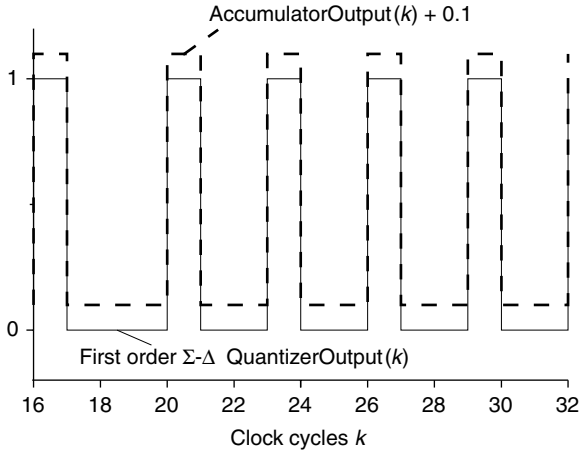

Figure 3.14 Accumulator overflow and Σ-Δ output.

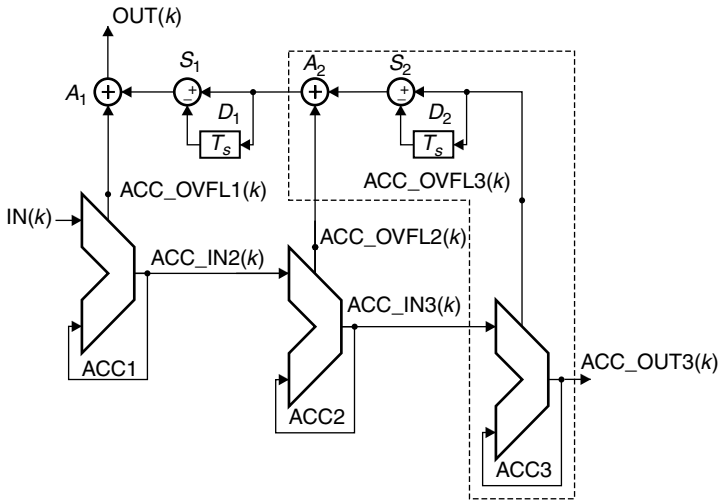

Figure 3.15 Three-accumulator fractional-N divider modulator. (All three accumulator clocks are coming out from the frequency divider.)

is affected by the first accumulator overflow at the kth time sample, by the second one at the kth and $(k-1)$th time samples, and by third one at the kth, $(k-1)$th, and $(k-2)$th time samples. Examining the diagram of Fig. 3.15 we found that the transfer function from the first, second, and third accumulator overflows to output in the Z domain are given respectively by $1 = (1-1/z)^0$, $(1-1/z)^1$, $(1-1/z)^2$, so we can write

$$\begin{aligned}
\mathrm{OUT}(z) &= \sum_{j=1}^{3} \mathrm{ACC_OVFL}_j \left(1-\frac{1}{z}\right)^j \\
&= \mathrm{ACC_OVFL}_1(z) \\
&\quad + \mathrm{ACC_OVFL}_2(z) - \frac{1}{z}\,\mathrm{ACC_OVFL}_2(z) \\
&\quad + \mathrm{ACC_OVFL}_3(z) - 2\frac{1}{z}\,\mathrm{ACC_OVFL}_3(z) \\
&\quad + \frac{1}{z}\frac{1}{z}\,\mathrm{ACC_OVFL}_3(z)
\end{aligned}$$

which corresponds in the time domain to Eq. (3.16).

$$\begin{aligned}
\mathrm{OUT}(k) &= \mathrm{ACC_OVFL}_1(k) \\
&\quad + \mathrm{ACC_OVFL}_2(k) - \mathrm{ACC_OVFL}_2(k-1) \\
&\quad + \mathrm{ACC_OVFL}_3(k) - 2\,\mathrm{ACC_OVFL}_3(k-1) \\
&\quad + \mathrm{ACC_OVFL}_3(k-2)
\end{aligned} \tag{3.16}$$

OUT(k) is the sum of 4 positive and 3 negative terms; each term is an accumulator overflow that can assume a value of 1 or 0. OUT(k) can assume all integer values from -3 to $+4$.

The fractional-N order can be increased by generalizing the schematic of Fig. 3.15. The key block is the one inside the dashed box; it consists of one accumulator, one discrete-time differentiator, and one adder. This block has to be recursively replicated as many times (in increasing order) as needed.

Now, the output signal of the third-order Σ-Δ converter $Y(k)$ (see Fig. 3.8) is a pseudo-random signal whose average of power spectrum is given by Eq. (3.14), so the majority of noise energy is pushed toward the high-frequency range and can be filtered out by using a lowpass filter. In the same way, the frequency division modulating signal OUT(k) is a pseudo-random signal whose average is the fractional frequency and with a power spectrum given by Eq. (3.14). Still noise energy is pushed toward high frequencies; it can be filtered out with a lowpass filter. In the case of the PLL synthesizer, the lowpass function is made by the PLL closed-loop response. Its bandwidth[†] has to be $\ll f_s/6$. The loop filter has to be designed to meet that specification. The $Y(k)$ amplitude is within $[0; q]$ while OUT(k) is within [0; 1] and correspondent synthesizer output angular frequency is modulated by a factor OUT(k)$2\pi f_{\text{ref}}$. Thus we can replace q with $2\pi f_{\text{ref}}$ and f_s with f_{ref} and obtain the fractional-N generated angular frequency noise power density:

$$|\Omega_{\text{noise}}(f)|^2 = \left[2\sin\left(\pi\frac{f}{f_{\text{ref}}}\right)\right]^{2M}\frac{\pi^2}{3}f_{\text{ref}} \tag{3.17}$$

We are more interested in phase noise than in frequency noise. Anyway the latter can be calculated from the first by discrete-time derivation. This means that we have to multiply Eq. (3.17) by the squared amplitude of the discrete-time differentiator transfer function. That factor is already contained in Eq. (3.17) since the factor between the squared brackets is the transfer function of the discrete-time integrator which is the reciprocal of the one of the differentiator. Thus the phase noise power density due to an M-accumulator fractional-N synthesizer is given by

$$|\Phi_{\text{noise}}(f)|^2 = \left[2\sin\left(\pi\frac{f}{f_{\text{ref}}}\right)\right]^{2(M-1)}\frac{\pi^2}{3}f_{\text{ref}} \tag{3.18}$$

[†]At that offset, the frequency noise intercepts the value of the single accumulator which is not acceptable (see Fig. 3.10).

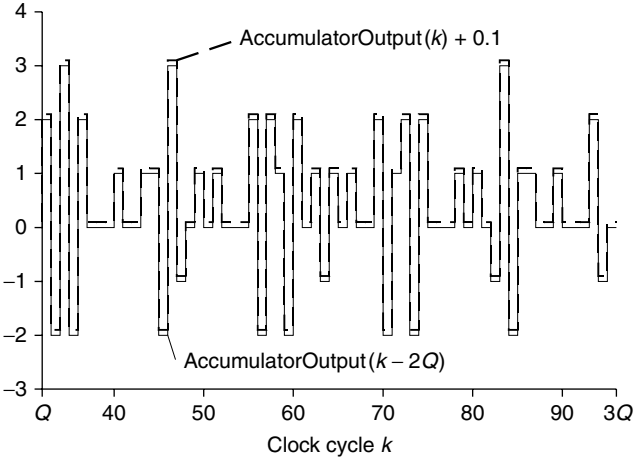

Figure 3.16 Normal and translated accumulator output $Q = 32$, $A = 11$.

For low-frequency values Eq. (3.18) can be approximated as

$$F_{\text{noise}}(f) \cong \frac{(2\pi)^{2M}}{12} f_{\text{ref}}^{-2(M-1)} f^{2(M-1)} \tag{3.18'}$$

which states that an M-accumulator fractional-N synthesizer phase noise slope is $20(M-1)$ dB/decade. Equation (3.18) relies on the flat distribution of quantization noise over frequency; or in other words, it needs the last accumulator's waveforms to be random signals. In real cases, the accumulator's waveforms are not truly (or perfectly) random signals. Because of this nonideality, it is difficult to find the multiaccumulator synthesizer phase noise analytically, but it is possible to find it by numerical calculation.[†] Figure 3.16 shows the resulting frequency control waveform OUT_k and the same curve translated by $2Q$ samples in the case of $Q = 32$, $A = 11$. Again, the translated curve is also y shifted by 0.1 in order to help distinguish the two. Note that $\text{OUT}_k = \text{OUT}_{k-2Q}$; the frequency division modulation waveform is periodic with a period of $2Q/f_{\text{ref}}$. Consequently the phase noise spectrum has Q spectral lines spaced by $f_{\text{ref}}/(2Q)$ (the maximum frequency is $f_{\text{ref}}/2$). In some particular cases, when Q is an integer multiple of A, the period becomes shorter, being multiplied by $1/A$, and the phase noise spectrum becomes made by Q/A spectral lines still with maximum frequency $f_{\text{ref}}/2$ and spaced by $f_{\text{ref}}A/(2Q)$. The output spectrum

[†]See the file 3AccumulatorsNfractional.MCD.

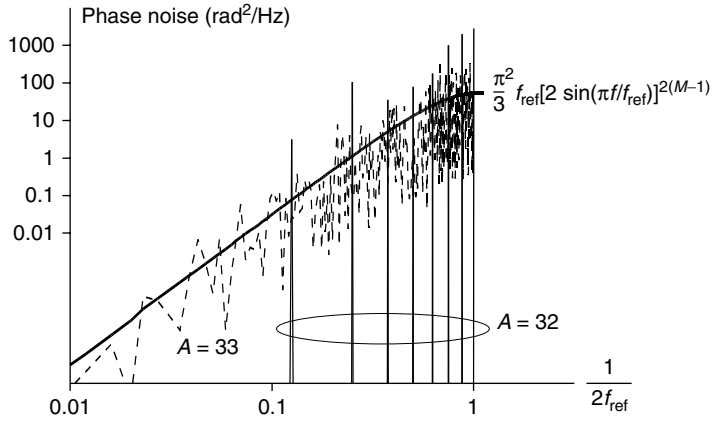

Figure 3.17 Fractional-N phase noise ($Q = 256$, $A = 33$).

is modulated by a signal which is more similar to a periodic signal than to random noise; the effectiveness of the spur reduction is compromised.

Figure 3.17 shows the result for accumulator size $Q = 256$ and the first accumulator inputs $A = 33$ and $A = 32$. On the same graph is also plotted the result coming from Eq. (3.18). It can be seen that the first case ($A = 33$) reasonably approximates the analytic expression derived for random sequences; in the second case ($A = 32$) $Q/A = 8$, and the phase noise spectrum contains only eight equally spaced lines (they don't look so, but remember the logarithmic scale). Spectra shown by Fig. 3.17 are calculated using the FFT. This calculation is not rigorous because the FFT needs samples that are equally time spaced by sampling time. The accumulator's waveforms are instead timed by $1/f_v$ which is not constant since it depends on the instant frequency division.

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Chapter

4

Synthesizer Performance Simulation

4.1 Introduction

This chapter is the core of the book. Many techniques for the prediction of PLL performances are described. Section 4.2 deals with the calculation of open-loop, closed-loop, and phase error responses. We show how to calculate these functions by using mathematical manipulation and circuit analysis programs. The methods described also allow for the calculation of global parameters like the unit gain bandwidth, response peak, and phase margin. Applying the methods of this section, it is possible to analyze PLLs without limitations on loop filter complexity.

Section 4.3 describes phase noise definition and analysis. Modeling of the noise from loop components together with the impact of this noise on the PLL phase noise is presented. The optimum closed-loop bandwidth to achieve minimum PLL phase noise is defined at the end of the section.

Angular modulated PLLs are described in Sec. 4.4 which gives a physical interpretation of closed-loop and phase error responses.

The analysis of dynamic performances of PLLs is presented in Sec. 4.5. Output frequency settling for linear and nonlinear operation of the phase detector are illustrated. Simulation techniques for these calculations are examined for both linear and nonlinear operation. An approximated linear analysis for the latter is also described.

A final comparison table for the mathematical manipulation and circuit analysis methods completes the chapter.

4.2 Simulation Techniques

Two techniques for simulation of a PLL are discussed in this chapter. The first one is based on the use of mathematical manipulation programs that perform all the complex number algebraic computations needed to manipulate PLL equations. The fundamental equations are open-loop, closed-loop, and phase error response [Eqs. (1.3), (1.5) and (1.6)]. All these functions can be easily calculated from the loop filter transfer function, and several loop filters were described in Sec. 2.3 together with their transfer functions. PLL performances can be calculated by analyzing the block diagrams of Fig. 1.2 by application of the above-mentioned equations. Sampling effects can be calculated using Eq. (2.10).

The other method of analysis is based on circuit simulators with the application of behavioral models. Calculation of the loop filter gain is one of the basic capabilities of circuit simulators. The remaining blocks of Fig. 1.2 are multipliers by a constant, one subtractor, and one integrator. The behavioral model analysis of block diagrams consists of representing quantities of each node in the block diagram with voltages and replacing each block with a corresponding circuit characterized by the same input-output relations. According to this definition, the blocks in the diagram of Fig. 1.2 are modeled as follows:

- The loop filter transfer function is modeled by the loop filter circuit itself.
- The multiplier by constant is modeled by the ideal voltage amplifier generally implemented with *voltage-controlled voltage sources* (VCVSs) that have input and output ports referred to ground and a gain equal to the multiplying constant. If the multiplying constant is less than 1, a two-resistor voltage divider can be used instead of a VCVS.
- The subtractor is modeled by the unit gain VCVS with the input port floating from ground and the output port referred to ground: The VCVS output voltage is equal to the difference between the voltages at the input terminals.
- The subtractor followed by the multiplier by constant is modeled by a VCVS like above but with the gain equal to the multiplying constant.
- The integrator is modeled by one circuit having an input-output gain of $1/(2\pi f)$.

In the case of the charge pump, the phase detector output is inherently a current rather than a voltage, so the output VCVS of the phase detector block is replaced by a *voltage-controlled current source* (VCCS).

In order to show the application of the two analysis methods, we will analyze one fourth-order type II PLL with the following parameters:

- Loop filter schematic as in Fig. 2.21 with feedback impedance as in Fig. 2.19*c*. Component values are $C_{\text{in}} = 2.2$ nF, $C_2 = 10$ nF, $C_3 = 1$ nF, $R_{1/2} = 3.3$ Kilo-ohms (kΩ), $R_2 = 5.6$ kΩ.
- PFD with Vdd = 5 V (ideal CMOS), $K_d = 5/(2\pi)$
- VCO modulation sensitivity of 10 MHz/V, $K_v = 2\pi(10 \times 10^6)$
- Output frequency of 1 GHz, reference frequency of 1 MHz, and thus frequency division factor $N = 10^3$.

This PLL will be analyzed using two approaches. Open-loop, closed-loop, and phase error responses will be calculated through analysis of the Fig. 1.2*a* block diagram. Two programs will be used: mathematical manipulation MATHCAD, and the SPICE-based simulator program SIMETRIX.[†] MATHCAD calculation is a straightforward application of loop equations and loop filter frequency responses. The loop filter frequency response can be calculated from Eq. (2.16):

Loop filter feedback impedance and gain:

$$Z2(f) := \left(C3 \cdot j \cdot 2 \cdot \pi \cdot f + \frac{1}{\frac{1}{C2 \cdot j \cdot 2 \cdot \pi \cdot f} + R2} \right)^{-1} \qquad F(f) := \frac{Z2(f)}{R1} \cdot \frac{1}{j \cdot 2 \cdot \pi \cdot f \cdot \frac{R1}{4} \cdot Cin + 1}$$

Phase detector gain: $Kd := 5 \cdot (2 \cdot \pi)^{-1}$

VCO tuning sensitivity: $Kv := 2 \cdot \pi \cdot 10 \cdot 10^6$

Frequency division factor: $N := 1000$

The open-loop gain, closed-loop frequency response, and phase error response are given by Eqs. (1.5), (1.3), and (1.6), respectively, as follows:

Open loop gain: $Hopen(f) := \frac{Kd \cdot Kv}{N} \cdot \frac{F(f)}{j \cdot 2 \cdot \pi \cdot f}$

Closed loop frequency response: $H(f) := \frac{\frac{Kd \cdot Kv}{N} \cdot \frac{F(f)}{j \cdot 2 \cdot \pi \cdot f}}{1 + \frac{Kd \cdot Kv}{N} \cdot \frac{F(f)}{j \cdot 2 \cdot \pi \cdot f}}$

Phase error response: $H1(f) := \frac{1}{1 + \frac{Kd \cdot Kv}{N} \cdot \frac{F(f)}{j \cdot 2 \cdot \pi \cdot f}}$

The program will calculate the preceding expressions as complex functions of frequency. Their amplitude and phase (real and imaginary

[†]See the files Mathcad_PLL_Analysis.MCD and Simetrix_PLL_Analysis.sxsch.

parts) can be plotted versus frequency obtaining the Bode plot, Nyquist plot, etc. A frequency stimulus expression has to be defined in order to plot the functions. This can be done through definition of an integer index to sweep the frequency variable:

frequency stimulus:

$$Kmax := 255 \quad k := 0..Kmax - 1 \quad f_{start} := 10 \quad f_{stop} := 1 \cdot 10^6$$

$$freq_k := f_{start} \cdot \left(\frac{f_{stop}}{f_{start}} \right)^{\frac{k}{Kmax-1}}$$

This way the frequency will be swept from 10 Hz to 1 MHz with 51 points per decade (255 total points). The phase margin, closed-loop unit gain bandwidth, and closed-loop gain peak can be easily calculated by using the equation-solving capability of MATHCAD.

Phase margin calculation:

$$fzero := 10^4$$

$$\text{Given} \quad |Hopen(fzero)| = 1 \quad f_{UnitGain} := \text{find}(fzero) \quad f_{UnitGain} = 6.49 \cdot 10^3$$

$$PhaseMargin := \arg(Hopen(f_{UnitGain})) \cdot \frac{180}{\pi} + 180$$

$$PhaseMargin = 46.203$$

Closed loop unit gain bandwidth calculation:

$$fzero := 10^4$$

$$\text{Given} \quad |H(fzero)| = 1 \quad f_{ClosedLoopUnitGain} := \text{find}(fzero)$$

$$f_{ClosedLoopUnitGain} = 8.614 \cdot 10^3$$

Closed loop gain peak:

$$D(f) := \frac{d}{df} |H(f)|$$

$$fguess := 5 \cdot 10^3$$

$$\text{Given} \quad D(fguess) = 0 \quad f_{ClosedLoopPeak} := \text{find}(fguess)$$

$$f_{ClosedLoopPeak} = 4.412 \cdot 10^3$$

$$ClosedLoopPeak_{dB} := 20 \cdot \log(|H(f_{ClosedLoopPeak})|)$$

$$ClosedLoopPeak_{dB} = 3.19$$

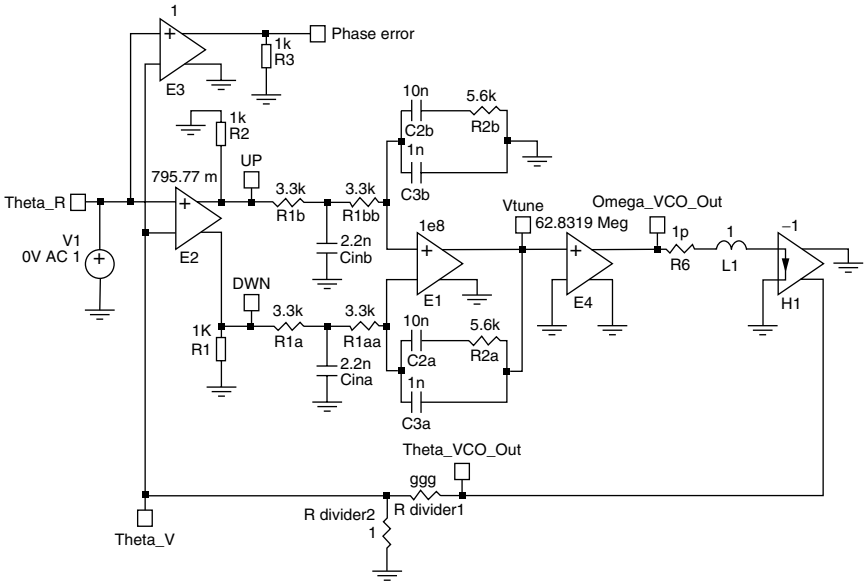


Figure 4.1 Behavioral model circuit of type II fourth-order PLL.

More or less of the same calculations can be performed by using behavioral model concepts. The SIMETRIX schematic of Fig. 4.1 is a behavioral model representation of a PLL block diagram as in Fig. 1.2a. Some significant nodes of the schematic are marked with terminals.

The voltages on terminals represent the quantities on the nodes of the block diagram.

- The PFD is represented by VCVS $E2$; its gain equals $K_d = 5/(2\pi)$. Terminals marked with Up and Dwn correspond to PFD output terminals. This component supplies a differential output voltage between the nodes equal to the average PFD. Two resistors $R1$ and $R2$, ensure a DC path to ground, which is needed for initial DC analysis of the circuit performed by the simulator. If a charge pump is used, $E2$ has to be replaced with a VCCS with gain $K_d = Icp/(2\pi)$, negative output terminal connected to ground, and a positive one connected to the loop filter input (which will be a transimpedance).
- Loop filter components are $R1a$, $R1aa$, $R2a$, $Cina$, $C2a$, $C3a$, $R1b$, $R1bb$, $R2b$, $Cinb$, $C2b$, $C3b$, and $E1$. The operational amplifier is simply modeled with a high gain VCVS (gain of $E1$ is 10^8).
- The VCO block consists of components $E4$, $R6$, $L1$, and $H1$. Component $E4$ is a VCVS whose gain equals K_v; its input is connected to the node marked V_{tune}, representing the tuning voltage (node a_4 in

Fig. 1.2), while the output is connected to node Omega_VCO_Out, whose voltage represents the VCO output angular frequency (node a_5 in Fig. 1.2). The integrator is realized with R6 $= 10^{-12}\Omega$, $L1 = 1$H, and the current-controlled voltage source $H1 = 1$ V/A. The gain from node Omega_VCO_Out to node Theta_VCO_Out is given by $1/(10^{-12} + j2\pi f)$. For frequencies sufficiently higher than 10^{-12} (which really is a very low value), that gain can be approximated with $1/(j2\pi f)$, which is perfect integrator transfer function. The approximation could be eliminated by replacing $R6$ with a short circuit, but this is not allowed because this way the voltage generator $E4$ output would be DC grounded from the $L1$ and $H1$ input.

- The frequency divider is a simple two-resistor (Rdivider1 and Rdivider2) voltage divider. Gain from node Theta_VCO_Out to Theta_V (node a_7 in Fig. 1.2a) is given by Rdivider1/(Rdivider1 + Rdivider2) $= 1/1000 = 1/N$, which is the reciprocal of the frequency division factor as needed.
- Nodes Theta_R and Theta_V represent the reference phase of the reference signal and of the divided VCO (nodes a_1 and a_7 of Fig. 1.2a). The difference between those two node voltages corresponds to the phase error; $E3$ presents that voltage to its output PhaseError.

Summarizing, voltages on the marked node of the schematic in Fig. 4.1 represent corresponding (phases, angular frequencies, voltages) quantities of the block in Fig. 1.2a so all frequency responses can be calculated applying one alternating current (AC) voltage source stimulus at the input (reference input of phase detector) and performing AC analysis of the circuit. AC analysis is one of the basic capabilities of SPICE.

From definitions of the closed-loop frequency response [Eq. (1.3)] and the transfer function from the reference phase to the output phase [Eq. (1.1)], it follows that the loop response is equal to the PLL input-output transfer function divided by N. The closed-loop response is then the gain from the reference input to the frequency divider output. This is the gain from the AC source to node Theta_V in the schematic of Fig. 4.1. The AC source has a unit amplitude; thus the Theta_V voltage equals the closed-loop frequency response. The phase error response is given by the voltage on the PhaseError node. The open-loop gain can be calculated by opening the connection between the frequency divider output and phase detector input, but this requires analysis of two circuits. A smarter solution is found by recognizing that the open-loop gain can be written in terms of the closed-loop response and phase error response. This can be done by combining Eqs. (1.3), (1.5),

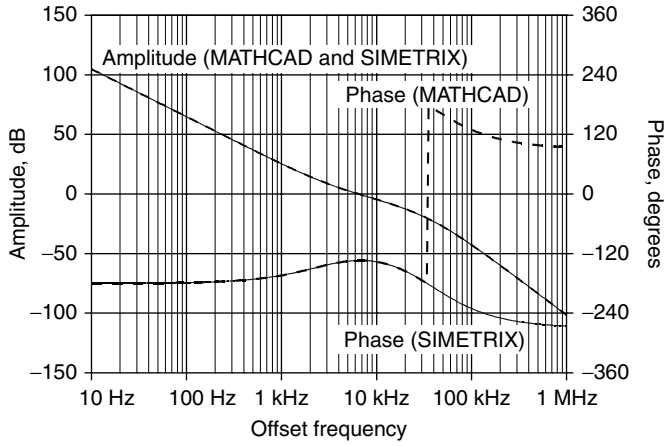


Figure 4.2 Type II fourth-order PLL Bode diagram.

and (1.6):

$$H_{\text{OpenLoop}}(f) = \frac{H(f)}{1 - H(f)} = \frac{H(f)}{\text{PhaseErrorResponse}(f)} \tag{4.1}$$

The open-loop gain is the ratio between the closed-loop and phase error frequency responses; therefore, its amplitude and phase can be plotted by using SIMETRIX capability to plot relative voltages. Use the instruction

Probe AC/Noise \dB-Relative Voltage \dB(V1/V2)

For the amplitude, and the instruction

Probe AC/Noise \Phase-Relative Voltage \Phase(V1/V2)

for the phase.

The frequency responses calculated with MATHCAD and SIMETRIX are plotted in Fig. 4.2 (open-loop gain) and in Fig. 4.3 (closed-loop response and phase error response). These two methods give almost identical results; the difference is less than 0.00055 dB for amplitude and 0.00056° for phase in all three functions and all over the frequency range. Looking at Fig. 4.2 it is possible to observe that the phase calculated with MATHCAD is in the range [−180°; +180°], while SIMETRIX removes the apparent discontinuities that occur when the phase magnitude approaches 180°.

The Nyquist diagram can be easily plotted with MATHCAD by using the polar plot. SIMETRIX can plot the Nyquist diagram of a given node voltage with the instruction:

Probe AC/Noise \Nyquist-Voltage

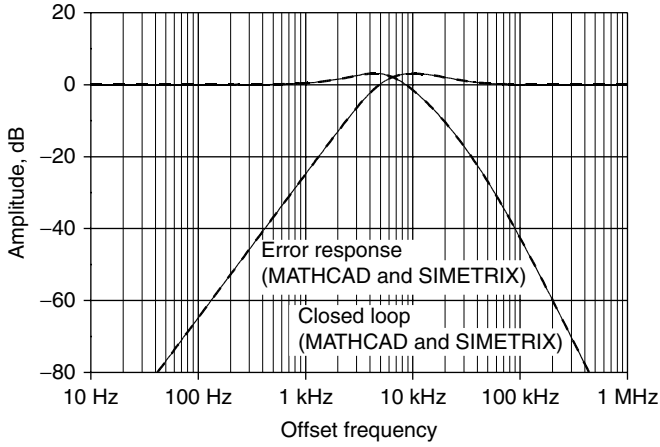


Figure 4.3 Type II fourth-order PLL response. Closed-loop frequency response with (*A*) SIMETRIX and (*A′*) MATHCAD. Phase error response magnitude with (*B*) SIMETRIX and (*B′*) MATHCAD.

In this case, the procedure is a little bit more complicated because the open-loop gain is obtained as the ratio of two voltages. The following procedure has to be used:

Probe \Add Curve

setting

y=Im(:Theta_V/:PhaseError) and x=Re(:Theta_V/:PhaseError).

MATHCAD Nyquist diagrams have a better aspect than those plotted by SIMETRIX. MATHCAD polar plots have a unitary aspect ratio; thus mathematically defined circles are plotted like circles. Differently from that, the aspect ratio of SIMETRIX graphs can be made approximately unitary only by manual resizing of the graph window. Without resizing, the unitary circle curve looks like an ellipse. Moreover the unit circle isn't automatically drawn by SIMETRIX; it has to be plotted applying the following procedure:

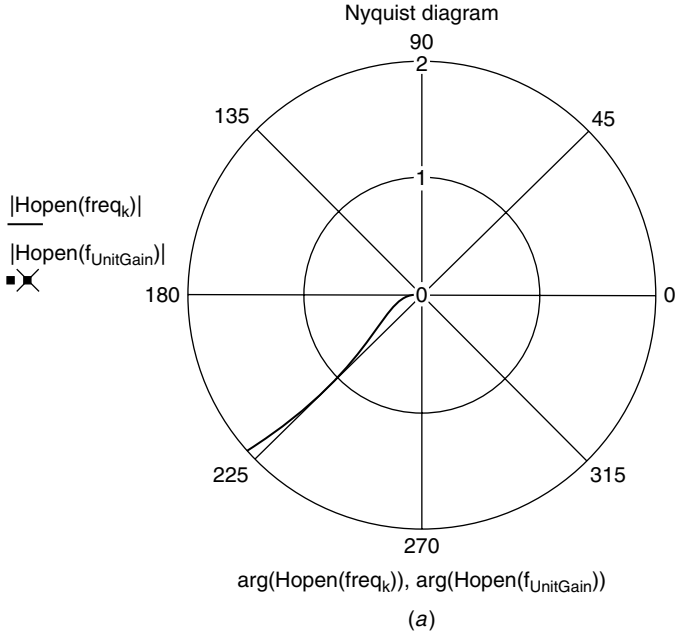
Probe \Add Curve

and setting

y=−(((abs(1-Im(:Theta_V/:PhaseError)^2)+1−(Im(:Theta_V/:PhaseError)^2))/2)^0.5)

x=Im(:Theta_V/:PhaseError)

Anyway, some other SPICE-based analysis programs have polar plot capability, eliminating that difficulty. Figure 4.4 shows the results obtained with the two approaches.



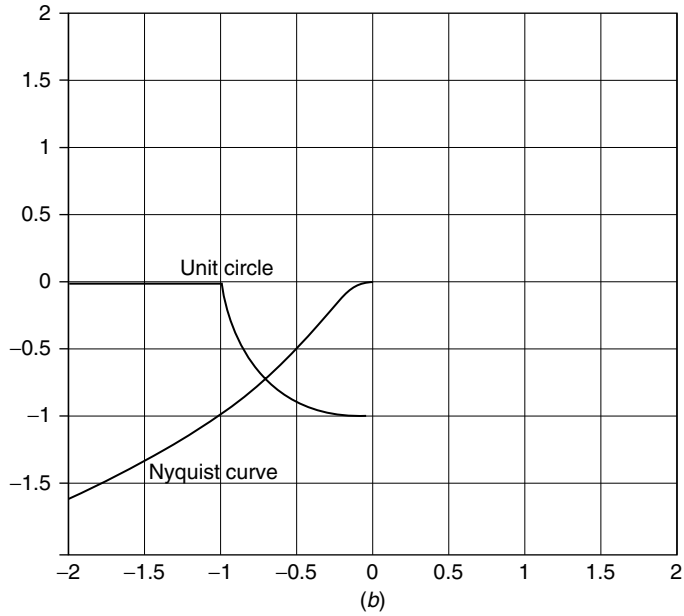


Figure 4.4 Type II fourth-order PLL Nyquist diagrams. (*a*) MATHCAD, and (*b*) SIMETRIX.

TABLE 4.1 Comparison of PLL Analysis Methods

	Mathematical	Behavioral circuits
Loop filter complexity	Moderate (−) Analytic expression of the response is needed.	Very high (+) Simulator can handle very complex circuits.
Calculation of phase margin	Easy (+) By using the equation-solving feature to find the solution of $\|H\text{open}(f)\| = 1$ and finding the open-loop phase at that frequency.	Relatively easy (−) By placing the cursor on the curve of the open-loop phase curve at the unit gain frequency.
Calculation of closed-loop unit bandwidth	Easy (+) By using the equation-solving feature to find the solution of $\|H(f)\| = 1$.	Relatively easy (−) By placing the cursor on the curve of the closed-loop frequency response at the unit gain.
Calculation of closed-loop peak	Easy (−) By using the equation-solving feature to find the solution of $D[\|H(f)\|] = 0$.	Very easy (+) Built in.
Statistical analysis	Possible (−) By manually generating multiple analyses.	Easy (+) By using Monte Carlo analysis.
Calculation of sampling effects	Easy (+) By writing Eq. (2.10).	Very difficult (−)

NOTE: (+) = advantage (more powerful or easier to use).
(−) = disadvantage (less powerful or more difficult to use).

The mathematical program-based method and the behavioral circuit method are more or less equivalent for basic calculations. Advantages and disadvantages of both methods are listed in Table. 4.1. This table will be updated in later sections, where the description of PLL analysis will be completed discovering further advantages and disadvantages.

4.3 Phase Noise

4.3.1 Definitions

Any oscillator and synthesizer output signal can be written as

$$V_{\text{out}}(t) = V(t)\cos\left[\int_0^t \omega(\tau)\,d\tau\right]$$

$V(t)$ is the amplitude of the signal and can be written as the sum of the nominal amplitude and the AM noise: $V(t) = V_o + V_{\text{AM}}(t)$. $\omega(t)$ is the instantaneous angular frequency. The argument of the cosine function

can be written in terms of the average (or nominal) frequency $\omega_o = 2\pi f_o$ and phase deviations $\theta_n(t)$:

$$V_{\text{out}}(t) = [V_o + V_{\text{AM}}(t)] \cos [\omega_o t + \theta_n(t)]$$

Defining the bilateral power density of phase deviations as

$$\left| \int_{-\infty}^{\infty} \theta_n(t) \exp(-j\,2\pi f\, t)\, d\,t \right|^2 = |\Theta_n(f)|^2$$

Θ_n is defined for both positive and negative values of frequency. $\theta_n(t)$ is a real function. It follows that $|\Theta_n(f)|^2 = |\Theta_n(-f)|^2$.

The *spectral density of phase deviation* is defined as the unilateral power density of the phase deviation:

$$S_\phi(f) = |\Theta_n(f)|^2 + |\Theta_n(-f)|^2 = 2\,|\Theta_n(f)|^2 \tag{4.2}$$

Neglecting AM noise, the oscillator output signal is: $V_{\text{out}}(t) = V_o \cos [\omega_o t + \theta_n(t)]$. If the phase deviation amplitude is $\ll 1$, the oscillator output signal can be approximated as

$$\begin{aligned} V_{\text{out}}(t) &= V_o\{\cos(\omega_o t) \cos[\theta_n(t)] - \sin(\omega_o t) \sin[\theta_n(t)]\} \\ &\cong V_o[\cos(\omega_o t) - \sin(\omega_o t)\theta_n(t)] \end{aligned}$$

The output spectrum is given by

$$\mathcal{F}[V_{\text{out}}(t)] \cong V_o \frac{\delta(f - f_o) + \delta(f + f_o)}{2} - V_o \frac{\Theta_n(f - f_o) - \Theta_n(f + f_o)}{2j} \tag{4.3}$$

That spectrum consists of two symmetrical parts. Each part includes one carrier at f_o and two symmetrical noise sideband spectra. The distance of each part from the origin is equal to the carrier frequency. The oscillator output spectrum is shown in Fig. 4.5. The oscillator phase noise at a given frequency f_m is defined as the ratio between noise in a 1-Hz bandwidth f_m offset from f_o and the carrier. From Eq. (4.3) the phase noise is given by

$$\text{PhaseNoise}(f_m) = \frac{(V_o/2)^2\,|\Theta_n(f_m)|^2}{(V_o/2)^2} = |\Theta_n(f_m)|^2 \tag{4.4}$$

The phase noise is usually expressed in logarithmic units (dBc/Hz):

$$\mathcal{L}(f_m) = 10\,\log_{10}\left\{|\Theta_n(f_m)|^2\right\} \tag{4.4′}$$

Comparing the definition of the phase deviation spectral density given in Eq. (4.2) and that of the phase noise given in Eq. (4.4), it can be

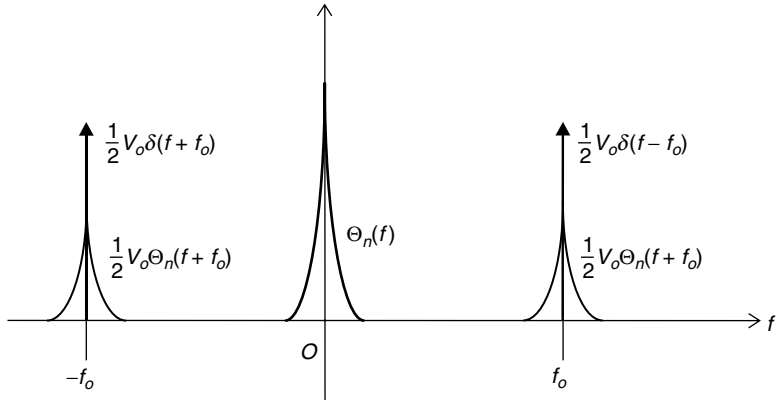


Figure 4.5 Phase deviation spectrum and oscillator output spectrum.

found that $S_\phi(f) = 2\text{PhaseNoise}(f)$. In the next sections we will use lowercase Greek letter θ to denote the time-domain phase noise, uppercase Greek letter Θ to denote its Fourier transform, and uppercase letter $\mathscr{L}$ to denote the phase noise expressed in dB: $\Theta(f) = F[\theta(t)]$, $\mathscr{L}(f) = 10\log_{10}[|\Theta(f)|^2]$.

4.3.2 Phase noise of PLL synthesizer

All electronic components generate noise, and loop components are no exception. Phase noise produced by the VCO, reference source, and frequency divider was discussed in Secs. 2.4.3, 2.5, and 2.6.1. The noise voltage produced by the loop filter originates from the resistor thermal noise and operational amplifier noise. Commonly used models for noise on resistors and operational amplifiers are shown in Fig. 4.6. The resistor noise is modeled by adding a noise voltage source in series with a noiseless resistor. The voltage noise density is given by $|v_r|^2 = 4\,KTR$ where K is the Boltzmann constant, T is the absolute temperature, and R is the resistance of the resistor. The voltage noise in series can be replaced by a shunt noise current with a density of $|i_r|^2 = 4KT(1/R)$, passing from a Thevenin to a Norton circuit.

The operational amplifier noise model includes one voltage noise generator and two equal-amplitude current noise generators connected to inputs. Voltage and current noise densities are given by opamp manufacturers.

The noise voltage at the loop filter output can be calculated by considering all noise sources on the circuit, multiplying them by their own gain to the output node, and summing the square magnitude of all these terms. This operation can be quite tedious even using a mathematical

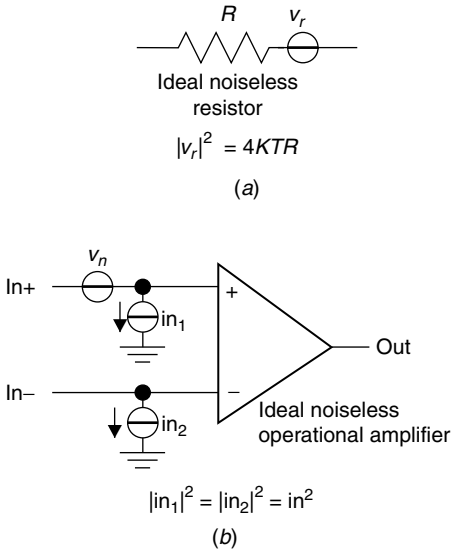


Figure 4.6 Noise models for loop filter components. (*a*) Resistor, and (*b*) operational amplifier.

manipulation program, but it is automatically performed by SPICE through AC noise analysis.

However, noise generated by resistors can be minimized by noting that the frequency responses of all loop filters for the PFD described in Sec. 2.3.2 don't change if all impedances are scaled by a constant factor (i.e., all resistance and inductance divided and all capacitance multiplied by an arbitrary constant). The noise voltage amplitude on resistors is proportional to the square root of resistance; thus the resistance of the loop filter has to be minimized compatibly with the current driving capability of the phase detector and operational amplifiers. Minimization of loop filter output noise also requires the use of low-noise operational amplifiers.

The phase noise of the PFD is usually assumed to be proportional to the reference frequency due to the increased rate of flip-flop switching. Expressing the phase frequency detector noise in logarithmic units we have

$$\mathscr{L}_{\mathrm{DET}}(f_r) = \mathscr{L}_{\mathrm{DET}}(f_r = 1\ \mathrm{Hz}) + 10\ \log_{10}(f_r) \tag{4.5}$$

where f_r is the reference frequency expressed in hertz and $\mathscr{L}_{\mathrm{DET}}(f_r = 1\ \mathrm{Hz})$ is on the order of –200 dBc/Hz.

Each loop component can be represented as an ideal block with one noise source added to its output. The diagram of Fig. 1.2*a* is transformed

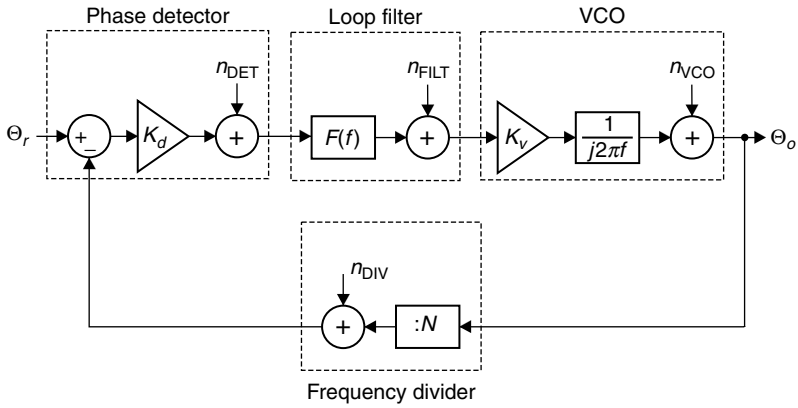


Figure 4.7 PLL block diagram with noise sources.

to that of Fig. 4.7. The diagram of Fig. 4.7 includes five different noise sources:

1. Reference phase noise
2. Phase detector noise
3. Loop filter output noise voltage
4. VCO phase noise
5. Frequency divider phase noise

The PLL output phase noise is given by a linear combination of five terms. Each term is given by one of these listed noise sources multiplied by a weighting function of the frequency. The weighting functions are the gains from the noise injection point to the output and can be calculated by application of Mason's rule.

The phase of the output signal is given by

$$\Theta_o = \frac{K_d K_v \frac{F(f)}{j2\pi f}}{1 + \frac{K_d K_v}{N}\frac{F(f)}{j2\pi f}}\Theta_r + \frac{K_v \frac{F(f)}{j2\pi f}}{1 + \frac{K_d K_v}{N}\frac{F(f)}{j2\pi f}} n_{\text{DET}} + \frac{\frac{K_v}{j2\pi f}}{1 + \frac{K_d K_v}{N}\frac{F(f)}{j2\pi f}} n_{\text{FILT}}$$
$$+ \frac{1}{1 + \frac{K_d K_v}{N}\frac{F(f)}{j2\pi f}} n_{\text{VCO}} - \frac{K_d K_v \frac{F(f)}{j2\pi f}}{1 + \frac{K_d K_v}{N}\frac{F(f)}{j2\pi f}} n_{\text{DIV}}$$

We have five noise sources, each filtered by its own frequency response. These partial frequency responses can be rearranged in terms of the PLL closed-loop, phase error, and loop filter frequency responses as follows:

$$\Theta_o(f) = NH(f)\Theta_r + \frac{N}{K_d}H(f)n_{\text{DET}} + \frac{N}{K_d}\frac{H(f)}{F(f)}n_{\text{FILT}}$$
$$+ \left[1 - H(f)\right] n_{\text{VCO}} - NH(f)n_{\text{DIV}} \tag{4.6}$$

All noise sources are uncorrelated, so the output phase noise is given by the sum of the squared amplitude of each term in Eq. (4.6) as follows:

$$|\Theta_o(f)|^2 = N^2 |H(f)|^2 |\Theta_r(f)|^2 + \frac{N^2}{K_d^2} |H(f)|^2 |n_{\mathrm{DET}}(f)|^2 + \frac{N^2}{K_d^2} \frac{|H(f)|^2}{|F(f)|^2} |n_{\mathrm{FILT}}(f)|^2 + [1 - H(f)]^2 |n_{\mathrm{VCO}}(f)|^2 + N^2 |H(f)|^2 |n_{\mathrm{DIV}}(f)|^2 \tag{4.7}$$

The loop filter noise can usually be minimized by minimizing the impedance of passive elements and choosing low-noise operational amplifiers. Under this condition the third term of Eq. (4.7) can be neglected. The output noise includes three terms which depend on frequency and whose weighting function is the closed-loop frequency response $H(f)$. The VCO phase noise also depends on frequency, but its weighting function is the phase error response $[1 - H(f)]$. Equation (4.7) can be rearranged and approximated as

$$|\Theta_o(f)|^2 = N^2 \left[|\Theta_r(f)|^2 + \frac{|n_{\mathrm{DET}}(f)|^2}{K_d^2} + |n_{\mathrm{DIV}}(f)|^2 \right] |H(f)|^2 + [1 - H(f)]^2 |n_{\mathrm{VCO}}(f)|^2 \tag{4.7'}$$

The synthesizer output phase noise is the sum of two terms. The first one is given by a linear combination of the reference signal, phase detector, and frequency detector noise. It is filtered by the closed-loop response which is lowpass; for this reason it is sometimes called *in-band noise*. The second is the VCO phase noise and is filtered by the highpass phase error response. The closed-loop and phase error responses cross close to the unit gain line (see Figs. 1.7, 2.36, and 4.3), so increasing the loop bandwidth will increase the contribution of in-band noise and will decrease the contribution of the VCO to the output phase noise, and vice versa. Call f_1 the crossover frequency between the PLL closed-loop and phase error responses and f_2 the crossover frequency of the VCO phase noise with in-band noise: The best compromise is normally obtained when $f_1 \approx f_2$. Moreover the magnitude of both the closed-loop and phase error frequency responses is higher than 1 at offset frequencies close to the cutoff. Those peaks are added to in-band noise and VCO filtered noise, respectively, increasing the PLL phase noise. For this reason the closed-loop response and phase error peaks have to be minimized. Peaks can be minimized but not eliminated, usually increasing the phase margin. Thus the PLL phase noise at the offset frequency close to crossover is always higher than that of the VCO

only or the reference source increased by $20 \log_{10}(N)$ only† even if all remaining components are noiseless.

4.3.2.1 MATHCAD analysis of PLL phase noise. Let's analyze the phase noise of a PLL synthesizer with 8-GHz output frequency and 1-MHz reference frequency employing the following components:

- VCO with $K_v = 2\pi(277 \times 10^7)$ as in Fig. 2.35 for $f_{\text{out}} = 8$ GHz and with phase noise as plotted in Fig. 2.39, which can be modeled by Eq. (2.33):

$$\mathscr{L}_{\text{VCO}}(f_m) = 10 \log_{10}\left[(9.8 \times 10^{-15}) + \frac{21.7}{f_m^2} + \frac{7.6 \times 10^6}{f_m^3}\right]$$

- Reference oscillator with the same resonator Q as in Fig. 2.41 (curve 1) but with an output frequency 10 times lower (1 MHz instead of 10 MHz). The sloped portion of the phase noise will decrease by $20 \log_{10}(10 \text{ MHz}/1 \text{ MHz}) = 20$ dB, while the noise floor (flat portion of the curve) will remain unchanged according to the Leeson equation. The reference phase noise can be expressed as

$$\mathscr{L}_{\text{REF}}(f_m) = 10 \log_{10}\left(10^{-15} + \frac{8 \times 10^{-13}}{f_m^2} + \frac{8 \times 10^{-11}}{f_m^3}\right)$$

- Frequency divider whose output phase noise is assumed to be like the transistor-transistor logic (TTL) divider of Fig. 2.50 (remember that the phase noise of a frequency divider is mainly determined by the last divider of the chain as stated in Sec. 2.6.1). Frequency divider noise can be approximated by the following formula:

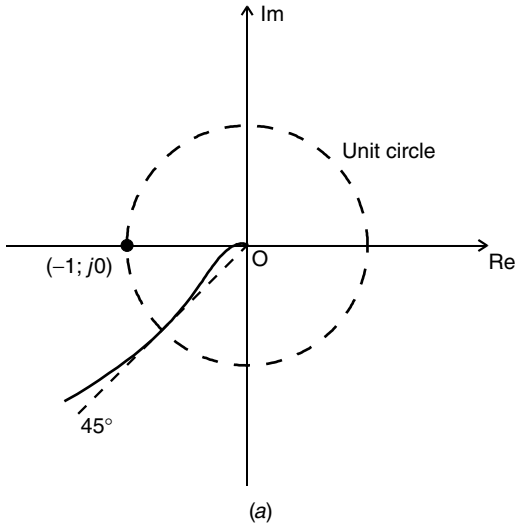
$$\mathscr{L}_{\text{DIV}}(f_m) = 10 \log_{10}\left(10^{-16.5} + \frac{3 \times 10^{-13}}{f_m}\right)$$

- Phase detector with phase noise given by Eq. (4.5):

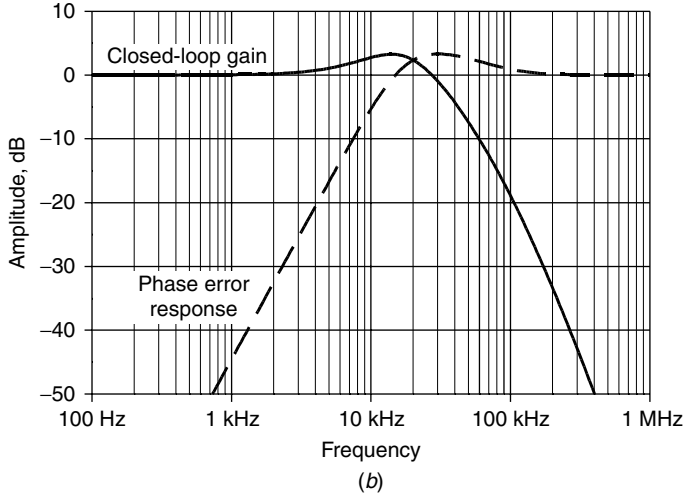
$$\mathscr{L}_{\text{DET}} = -200 + 10 \log_{10}(10^6) = -140$$

- Loop filter circuit like that in Fig. 2.21 with a feedback impedance as in Fig. 2.19*c*. The component values are $C_{\text{in}} = 270$ pF, $C_2 = 1$ nF, $C_3 = 82$ pF, $R_1/2 = 12$ kΩ, $R_2 = 18$ kΩ.

†The phase noise of the reference oscillator followed by an ideal frequency multiplier by N. This ideal source generates the same PLL frequency with a frequency division factor of N.



(*a*)



(*b*)

Figure 4.8 Type II, fourth-order PLL. (*a*) Nyquist diagram and the (*b*) closed-loop and phase error responses.

Equations for noise sources and the loop frequency response had be implemented inside a MATHCAD worksheet.† The Nyquist diagram is shown in Fig. 4.8*a*. It can be seen that the phase margin is about 44.9°: more or less like in the example of Sec. 4.2.

†See the file Mathcad_PLL_PhaseNoise_Analysis.MCD.

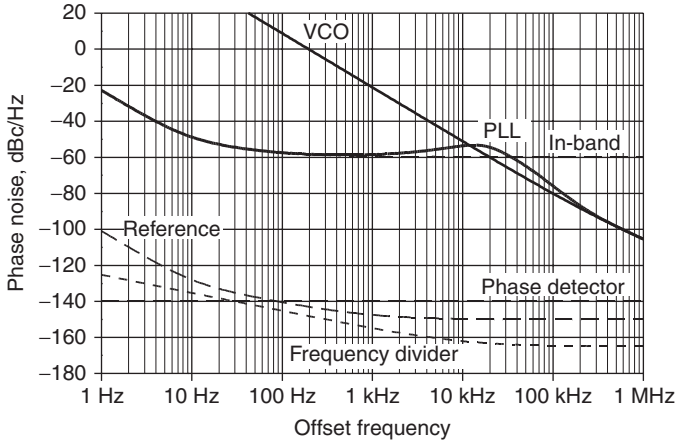


Figure 4.9 PLL phase noise and its partial terms.

Figure 4.8*b* shows the closed-loop and the phase error responses. Both curves exhibit a peak response of about 3.3 dB, a closed-loop unit gain bandwidth of 27.4 kHz, and an error response unit gain cutoff frequency of 14.9 KHz.

The in-band phase noise is calculated by a combination of the reference, PFD, and frequency divider phase noises using Eq. (4.7′):

$$L_{\text{InBand}}(f) = 10 \cdot \log\left[\left(10^{\frac{L_{REF}(f)}{10}} + 10^{\frac{L_{DIV}(f)}{10}} + 10^{\frac{L_{DET}}{10}} \cdot \frac{1}{kd^2}\right) \cdot N^2\right]$$

The PLL phase noise had been calculated by applying Eq. (4.7′) and is plotted in Fig. 4.9 together with the VCO, in-band, and all component phase noises. The in-band and VCO phase noises cross at 19.5 kHz. Phase noise minimization suggests that the closed-loop and phase error responses have to cross more or less at the same frequency; two curves cross at about 20 kHz as Fig. 4.8*b* shows, very closed to the requested value.

In order to show the effectiveness of the phase noise minimization criterion, the loop filter was scaled by factors 0.1, 1, and 10 by applying the scaling rules described in Sec. 2.3.4. Loop filter scaling changes the cutoff frequency but doesn't affect the shape of the response, in particular the phase margin and response peak. A scaling factor of 1 corresponds to not scaling the filter; scaling factors of 0.1 or 10 correspond, respectively, to reducing or increasing the closed-loop bandwidth by 10. PLL phase noise curves for the nominal loop filter and the two scaled loop filters are plotted in Fig. 4.10. The nominal (not scaled) filter gives the lowest phase noise; the narrower band PLL has a higher phase noise below 20 kHz; the wider band one has a higher noise above 30 kHz.

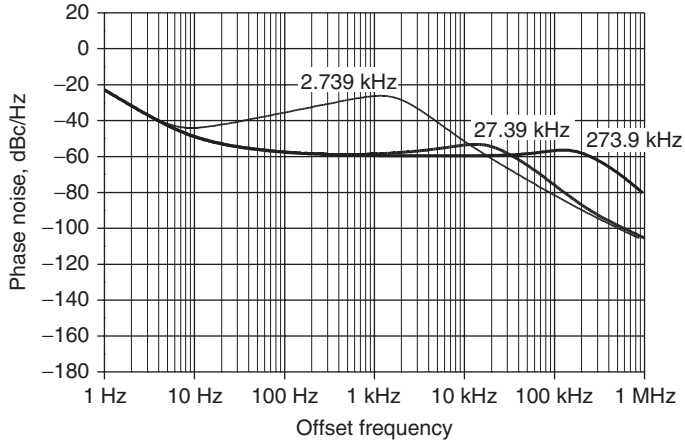


Figure 4.10 PLL phase noise with different values of the closed-loop unit gain bandwidth.

The optimum PLL bandwidth is not always achievable. An important limiting factor is reference spur filtering. When a small frequency step is needed, a low reference frequency has to be used and the maximum closed-loop bandwidth is limited because it has to be a small fraction of the reference frequency (as explained in Sec. 2.2). In our case the optimum loop bandwidth is a little bit smaller than 30 kHz, while the reference frequency is 1 MHz, which is 36.5 times bigger, keeping a reasonable margin for reference spur filtering. Sometimes the PLL bandwidth has to be wider than the optimum value because fast settling is required (see Sec. 4.5).

If an M-accumulator fractional-N divider is used, its phase noise is given by Eq. (3.18) which states that the M-accumulator fractional-N synthesizer phase noise slope is $20(M-1)$ dB/decade. The slope of the PLL frequency response has to be not less than that value; otherwise the in-band noise is not sufficiently filtered and will affect the PLL phase noise even at high offset frequencies. In Sec. 2.3.1 it was found that the PLL lowpass slope is $20(\text{PLL}_{\text{order}}-1)$ dB/decade, and it has to be not less than the fractional-N phase noise slope. Thus it has to be $20(\text{PLL}_{\text{order}}-1) \geq 20(M-1) \Rightarrow \text{PLL}_{\text{order}} \geq M$. The PLL minimum order equals the number of accumulators.

4.3.2.2 SIMETRIX analysis of PLL phase noise. The same calculation of the synthesizer output phase noise can be performed with circuit analysis by inserting noise sources inside the behavioral model of the loop. In other words the block diagram of Fig. 4.7 has to be implemented by applying the method of the behavioral model. In Sec. 4.2 we described

how to build up the equivalent circuit of the block diagram of Fig. 1.2*a*. The block diagram of Fig. 4.7 is derived from the one of Fig. 1.2*a*, including the phase noise of the loop components. The equivalent circuit for the block diagram of Fig. 4.1 has to be built up by applying the method described in Sec. 4.2 and summing the noise voltages at the output of all the loop components. According to the principle of behavioral modeling, all quantities of the block diagram are represented by voltages or currents (more usually voltages). Consequently phase noise sources will be represented by noise sources whose voltage density is equal to the corresponding phase noise. The square magnitude of the output noise voltage equals the synthesizer output phase noise. Now, the dependence on the frequency of the reference signal, phase detector, VCO, and frequency divider phase noise can be expressed as

$$|\Theta(f)|^2 = \sum_{k=0}^{3} A_k f^{-k}$$

where in some cases the coefficients A_k can be zero. Thus the loop components' phase noise curves have portions with slope over frequency of 30, 20, 10, and 0 dB/decade, and their corresponding noise voltage sources have the same slope. It is quite easy to model a flat noise source with a resistor followed by a VCVS[†]: One 6033.01-Ω resistor followed by a voltage gain of 100K gives a noise voltage density of 1 mV/Hz$^{0.5}$ (-60 dB below 1 V/Hz$^{0.5}$) when the temperature of the resistor is 27°C. Figure 4.11*a* shows the circuit. The noise voltage is available between nodes Vnp and Vnn, modifying the gain of the VCVC output level accordingly. Sloped noise sources can be obtained by filtering the flat noise generated by the circuit of Fig. 4.11*a*. The simplest filter is a first-order *RC* lowpass filter which has an asymptotic slope of 20 dB/decade. The circuit of Fig. 4.11*a* can be slightly complicated by placing a capacitor in the shunt with the resistor. The 20-dB/decade slope noise source is obtained providing that the cutoff frequency $1/(2\pi RC)$ is $\ll$ than the minimum frequency of interest. The resulting circuit is shown in Fig. 4.11*b*.[‡] The output noise between nodes Vnp and Vnn has a voltage density of 1 mV/Hz$^{1/2}$ at 1 Hz and depends on frequency as $1/f$. Noise generators with a slope that is not an integer multiple of 20 dB/decade are impossible[§] to obtain by applying the above described approach because lowpass filters have an asymptotic slope of 20 multiplied by the

[†]See the SIMETRIX file FlatNoise.

[‡]See the SIMETRIX file 20dB_decade_Noise.sxsch.

[§]The impedance of inductors and capacitors is sloped by 20 dB/decade, and there is no slower sloped element.

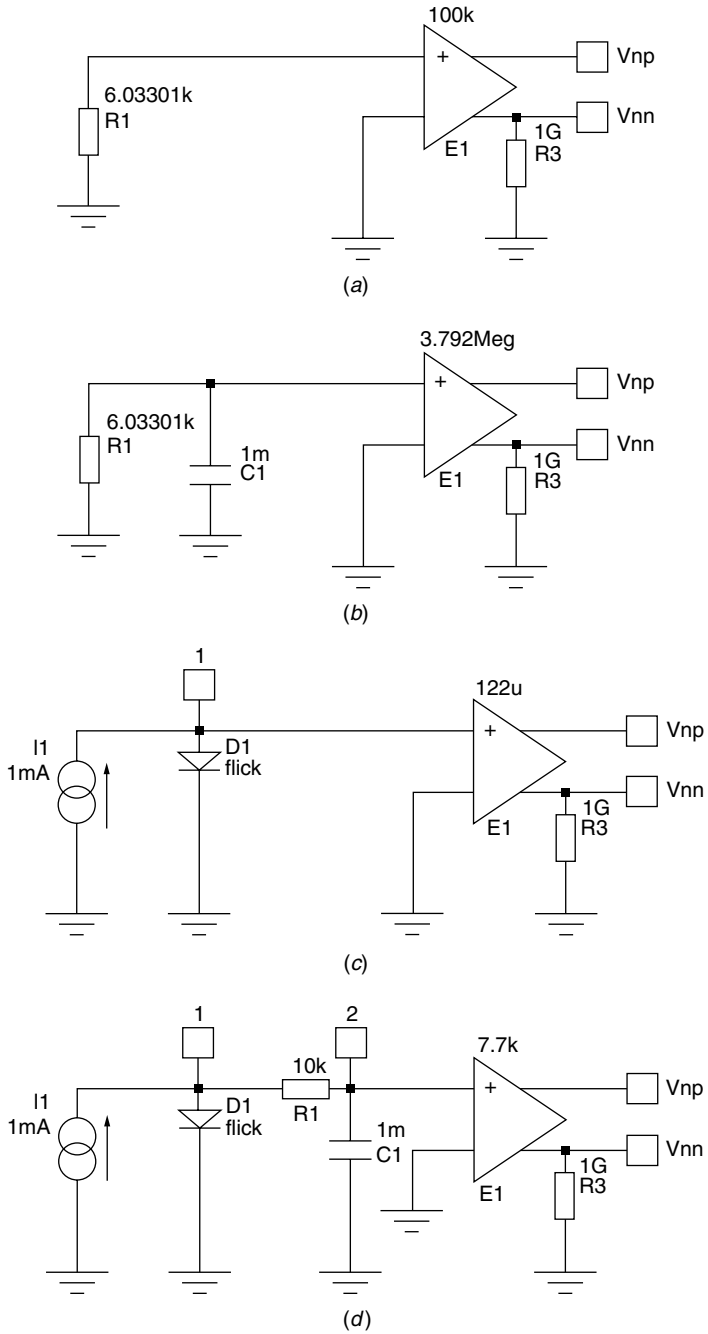


Figure 4.11 Noise generators. (*a*) Flat noise generator, (*b*) 20-dB/decade noise generator, (*c*) 10-dB/decade noise generator, and (*d*) 30-dB/decade noise generator.

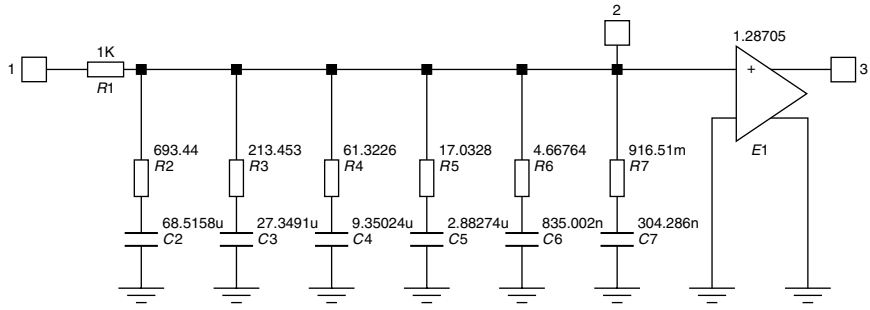


Figure 4.12 Ten-dB/decade filter.

filter order (which is an integer of course) dB/decade. A 10-dB/decade sloped filter can be synthesized by inserting many alternating poles and zeros in the transfer function. In this way the zeros partially cancel the filtering action of the poles and the filter slope is reduced to the desired value. Physical realization of the filter consists of a modified version of the *RC* lowpass filter where the capacitor is replaced by many series *RC* networks in parallel: This way the slope around the cutoff is used instead of the asymptotic slope. Figure 4.12 shows one possible realization of that filter.[†] It consists of one series resistor (R1), six series *RC* (R2, C2, R3, C3, . . . , R6, C6), and one ideal amplifier (E1) that adjusts the gain of the filter and provides zero output impedance.

Poles and zeros of a transfer function are approximately given by $P_k = R_1 C_{k+1}$ and $Z_k = R_{k+1} C_{k+1}$ with $k \in [1; 6]$. The frequency response magnitude (in dB) of the filter together with the magnitude of function $f^{-0.5}$ are plotted in Fig. 4.13. The maximum amplitude error is less than 0.4 dB from 1 Hz to 1 MHz. The filter of Fig. 4.12 can be cascaded with the generators of Fig. 4.11*a* and *b* obtaining the output voltage noise density of $f^{-0.5}$ and $f^{-1.5}$ (10 and 30 dB/decade), respectively.

Another approach can be used to model a $f^{-0.5}$ voltage noise density. This consists of taking flicker noise coming out from a forward-biased diode. SPICE models diode noise with the equation:

$$i_n^2(f) = \frac{4KT}{\mathrm{RS}} + 2qI_d + \mathrm{KF}I_d \frac{1}{f} \tag{4.8}$$

[†]See the SIMETRIX file Half_Slope.sxsch.

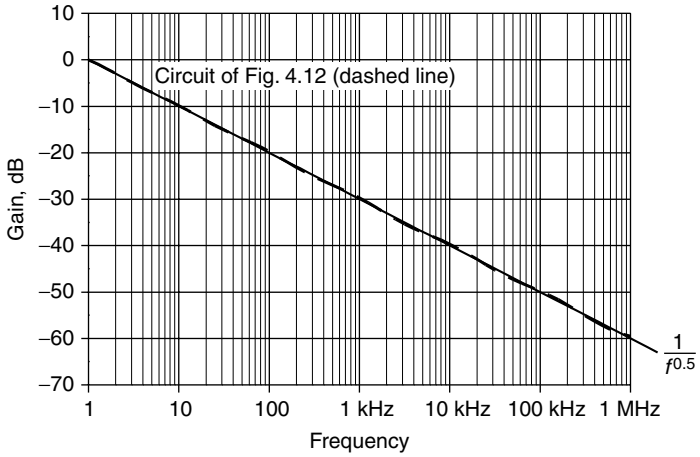


Figure 4.13 Magnitude frequency response of the circuit of Fig. 4.12.

where RS, KF = two parameters of the diode SPICE model (series resistance and flicker noise coefficient, respectively)
q = electron charge
T = absolute temperature
I_d = forward current

The square magnitude of the current noise density given by Eq. (4.8) contains three terms:

1. Thermal noise density due to series resistance of the diode (R_S)
2. Shot noise
3. Flicker noise

The first two terms have a flat distribution over frequency, while the third is 10 dB/decade sloped over frequency. For high values of the forward current and the flicker noise coefficient, the third term dominates over the other two and Eq. (4.8) can be approximated as

$$i_n^2(f) \cong K_F I_d \frac{1}{f} \tag{4.8′}$$

A forward-biased diode followed by a VCVS gives a noise generator sloped by 10 dB/decade. Figure 4.11*c* shows the schematic of such a generator† with an output voltage noise density of 1 mV/Hz$^{0.5}$ at 1 Hz.

†See the SIMETRIX file 10dB_decade_Noise.sxsch.

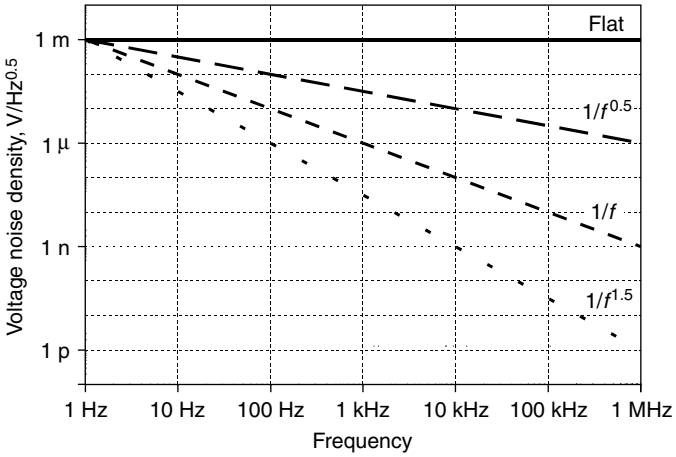


Figure 4.14 Output voltage noise density of the circuits in Fig. 4.11*a*, *b*, *c*, *d*.

The diode SPICE model is

```
.MODEL flick D IS=1n N=1 RS=0.1 KF=100
```

Inserting a 20-dB/decade lowpass filter within the above circuit, we will obtain a 30-dB/decade noise source (voltage noise proportional to $f^{-1.5}$). Figure 4.11*d* shows the schematic.† The output voltage noise density is still 1 mV/Hz$^{0.5}$ at 1 Hz.

Figure 4.14 shows the output voltage noise density of the circuits of Fig. 4.11*a*, *b*, *c*, and *d*. The output voltage noise density is 1 mV/Hz$^{0.5}$ at 1 Hz for all four circuits. The slope is 0, 20, 10, 30 dB/decade, respectively, for the circuits in Fig. 4.11*a*, *b*, *c*, and *d*.

Noise coming out from circuits can be summed up (by a series connection of the output ports) to obtain any noise spectrum in the form $|\Theta(f)|^2 = \sum_{k=0}^{3} A_k f^{-k}$. The gain of the output of the VCVS has to be set according to the corresponding coefficient A_k. In order to show this modeling technique, consider the VCO phase noise. In Sec. 4.3.2.1 it was assumed that the VCO phase noise is given by

$$\mathscr{L}_{\text{VCO}}(f_m) = 10 \log_{10}\left(9.8 \times 10^{-15} + \frac{21.7}{f_m^2} + \frac{7.6 \times 10^6}{f_m^3}\right)$$

†See the SIMETRIX file 30dB_decade_Noise.sxsch.

The corresponding equivalent noise voltage density is given by

$$v_{n,\mathrm{VCO}}(f_m) = \sqrt{9.8 \times 10^{-15}} + \frac{\sqrt{21.7}}{f_m} + \frac{\sqrt{7.6 \times 10^6}}{f_m^{1.5}}$$

The equivalent voltage noise has three terms sloped by 0, 20, and 30 dB/decade, respectively. The circuits of Fig. 4.11*a*, *b*, and *d* are required to model that. Summing the outputs of those circuits, we will have the following noise spectrum:

$$v_n'(f_m) = 10^{-3} + \frac{10^{-3}}{f_m} + \frac{10^{-3}}{f_m^{1.5}}$$

which has the same form of required noise but different coefficients. To make those coefficients equal, too, it is sufficient to multiply the gains of the circuits in Fig. 4.11*a*, *b*, and *d* by the coefficients $\frac{\sqrt{9.8\times10^{-15}}}{10^{-3}}$, $\frac{\sqrt{21.7}}{10^{-3}}$, $\frac{\sqrt{7.6\times10^6}}{10^{-3}}$. The resulting circuit is shown in Fig. 4.15.[†]

The noise voltage generated by the circuit of Fig. 4.15 (representing the VCO phase noise) can be added to the phase output of the VCO behavioral model by series connection of the noise generator output ports (Vnp, Vnn) to the VCO output: this way the noisy VCO block of Fig. 4.1 is implemented. The circuit[‡] is shown in Fig. 4.16. It is very similar to the one in Fig. 4.7 except for the component values and the presence of the VCO phase noise model given by components E5, E6, E7, R4, R5, R8, C1, C2, and I1.

Performing an AC analysis of the schematic of Fig. 4.16, it is possible to calculate the PLL closed-loop and phase error responses (the voltages on nodes Theta_V and PhaseError, respectively). Performing noise analysis it is possible to calculate the VCO contribution to the PLL output phase noise which is given by the output noise at node V_{nn}.

The procedure described for the VCO can be applied to all remaining loop components in order to model their noise. More precisely the user needs to model the noise of the following components: the phase detector, VCO, and frequency divider. Noise coming out of the loop filter is automatically computed by SPICE. Although the circuit obtained from the application of this procedure can be quite complicated, an interesting simplification can be achieved by applying a trick. The block diagram of Fig. 4.7 can be simplified into the one of Fig. 4.17, where the phase detector and frequency divider are noiseless. Two diagrams have the same output phase noise if the relation between the equivalent

[†]See the SIMETRIX file VCO_Noise.sxsch.

[‡]See the SIMETRIX file PLL_VCO_Phase_Noise.sxsch.

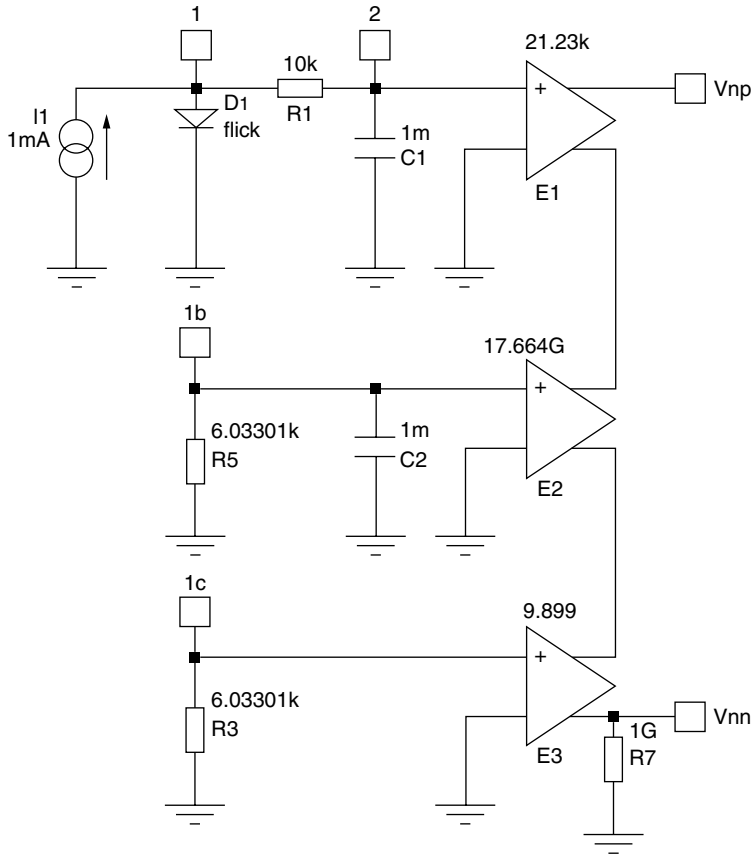


Figure 4.15 Model for the VCO phase noise.

phase noise of Fig. 4.17 and the noise sources of Fig. 4.7 is given by

$$\left|\text{InputEquivalentNoise}(f)\right|^2 = |\Theta_r(f)|^2 + \frac{|n_{\text{DET}}(f)|^2}{K_d^2} + |n_{\text{DIV}}(f)|^2 \tag{4.9}$$

In Sec. 4.3.2.1, it was assumed that the reference signal, phase detector, and frequency divider phase noise are, respectively, given by

$$\mathscr{L}_{\text{DET}} = -200 + 10\log_{10}(10^6) = -140$$

$$\mathscr{L}_{\text{DIV}}(f_m) = 10\log_{10}\left(10^{-16.5} + \frac{3\times 10^{-13}}{f_m}\right)$$

$$\mathscr{L}_{\text{REF}}(f_m) = 10\log_{10}\left(10^{-15} + \frac{8\times 10^{-13}}{f_m^2} + \frac{8\times 10^{-11}}{f_m^3}\right)$$

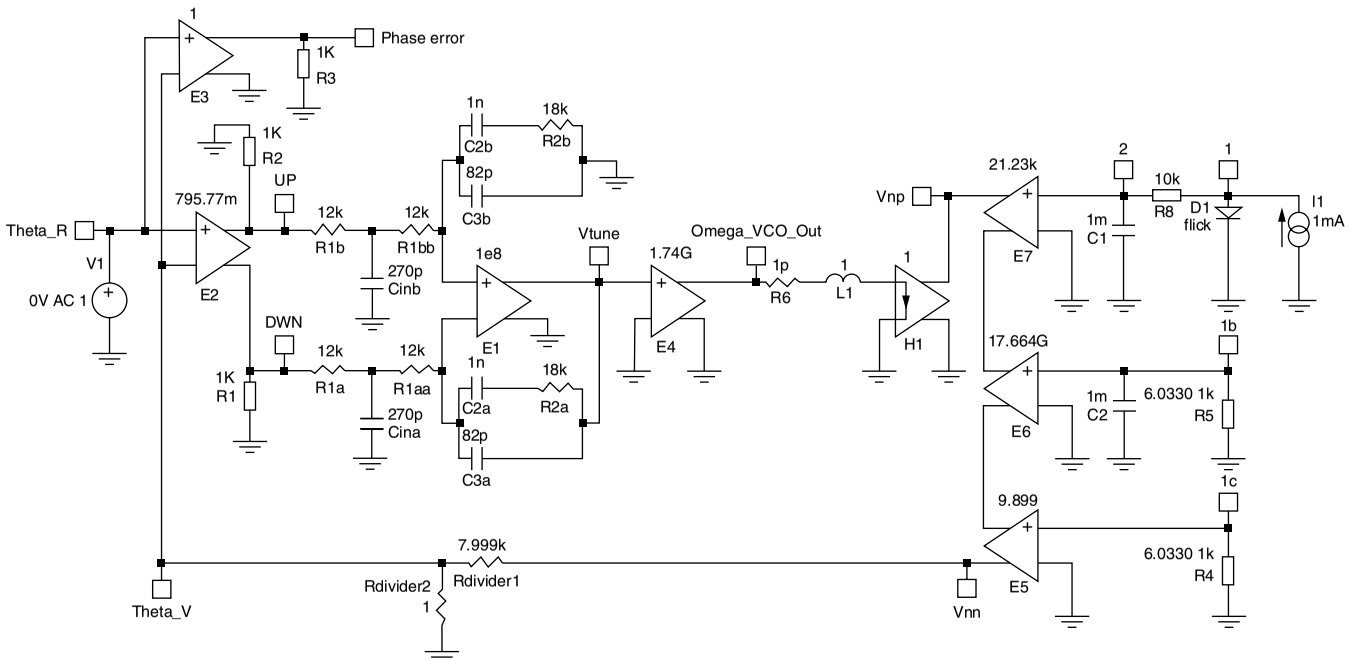


Figure 4.16 PLL behavioral model including VCO phase noise.

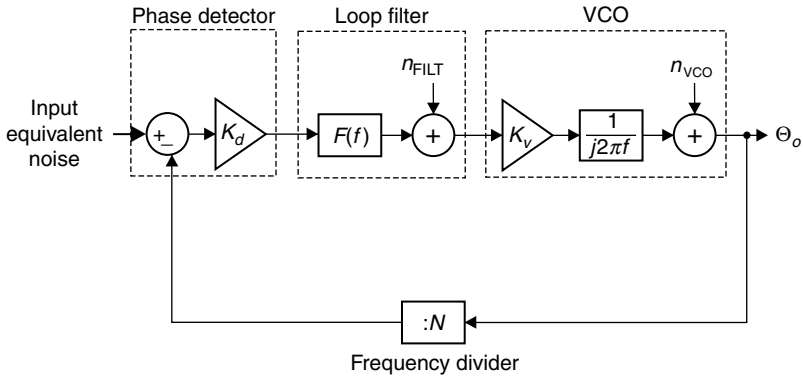


Figure 4.17 Simplified block diagram of Fig. 4.7.

These three terms can be combined according to Eq. (4.9) obtaining:

$$\text{EquivalentInputNoise}(f_m) = \sqrt{1.682 \times 10^{-14}} + \frac{\sqrt{11 \times 10^{-13}}}{f_m^{0.5}} + \frac{\sqrt{8 \times 10^{-11}}}{f_m^{1.5}}$$

The noise voltage corresponding to the equivalent input noise contains three terms with slopes of 0, 10, and 30 dB/decade. Synthesis of the voltage noise generator can be performed by applying the method described for VCO phase noise. The resulting network† is shown in Fig. 4.18.

The circuit of Fig. 4.18 can be inserted in series with the reference input of the schematic of Fig. 4.16, as shown‡ in Fig. 4.19. The noise and AC analyses of that circuit give all the noise contributions and frequency responses:

- The output noise at node PLL_{out} is the total PLL phase noise.
- The differential output noise between the nodes PLL_{out} and V_{np} is the VCO phase noise.
- The noise on node V_{np2} is the equivalent input noise.
- The noise voltage on node InBandNoise is the in-band noise given by the first term of Eq. (4.7′) (in-band noise equals equivalent input noise multiplied by the frequency division factor).

†See the SIMETRIX file Input_Equivalent_Noise.sxsch.

‡See the SIMETRIX file PLL_Phase_Noise.sxsch.

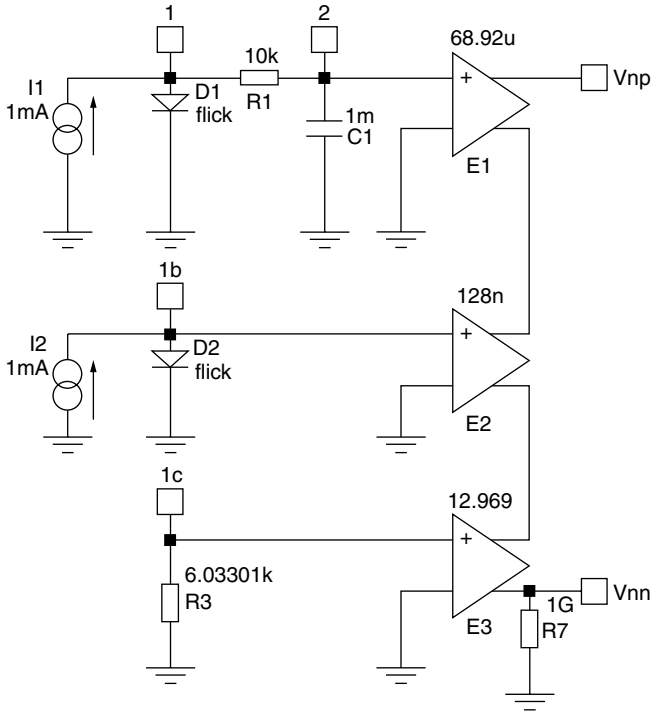


Figure 4.18 Equivalent input noise generator.

- The AC voltage on node Theta_V is the closed-loop frequency response.
- The AC voltage on node PhaseError is the phase error response.
- The ratio Theta_V/ PhaseError is the open-loop response.

Figure 4.20 shows these quantities.

Figure 4.21 shows the result of the Monte Carlo analysis (50 iterations) on the circuit of Fig. 4.19. A 10 percent tolerance was assumed for loop filter components and the VCO modulation sensitivity while all remaining components' parameters were considered as constant. The PLL output total phase noise is given by the voltage noise density. The black line is the nominal case (no tolerance), and the dashed lines surrounding the black one are the statistical results.

Figure 4.22 shows PLL output phase noise computations made with MATHCAD and SIMETRIX. The two curves are quite close, with the maximum difference being less than 1.2 dB. This is probably due to the fact that loop filter noise effects are not computed in MATHCAD (the phase noise calculated by SIMETRIX is higher), although values

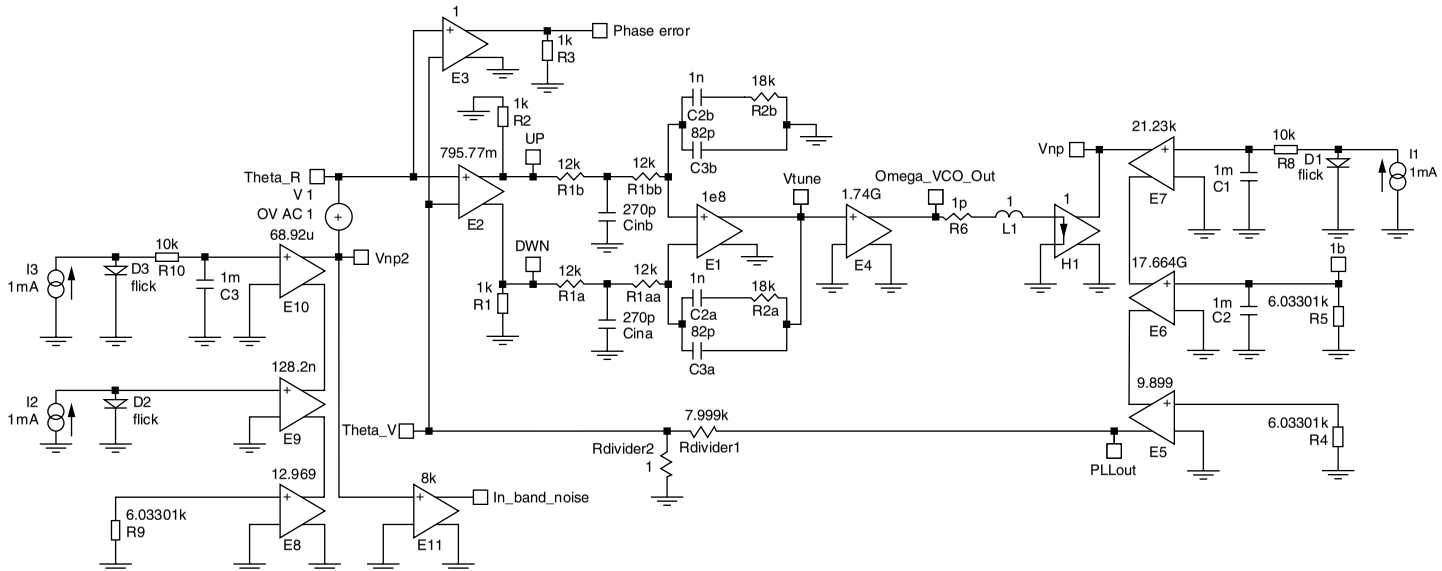


Figure 4.19 PLL behavioral model including components' phase noise.

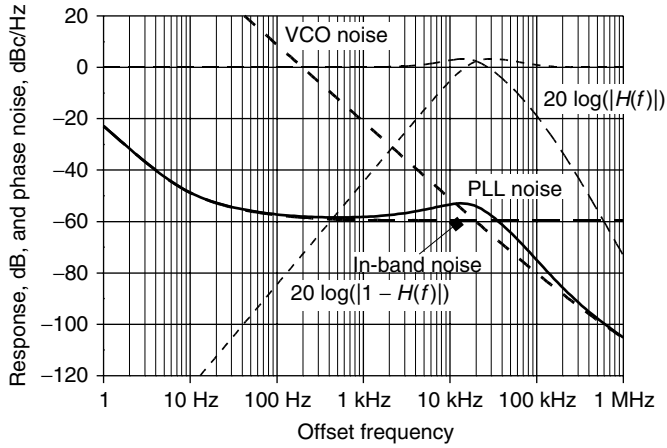


Figure 4.20 Results of analysis on schematic of Fig. 4.19.

of the noise parameters can be slightly different in the two circuits due to numerical rounding.

Table 4.1 can be updated considering the lesson learned in the discussions of Secs. 4.3.2.1 and 4.3.2.2. Table 4.2 provides a more complete list of pros and cons of the mathematical and behavioral model methods of analysis.

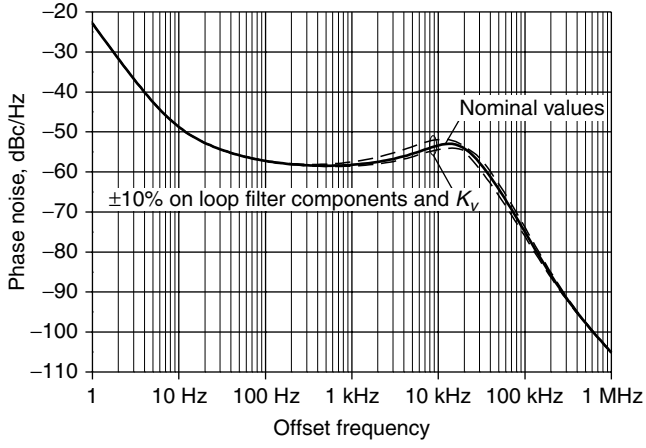


Figure 4.21 Monte Carlo phase noise analysis of the schematic in Fig. 4.19.

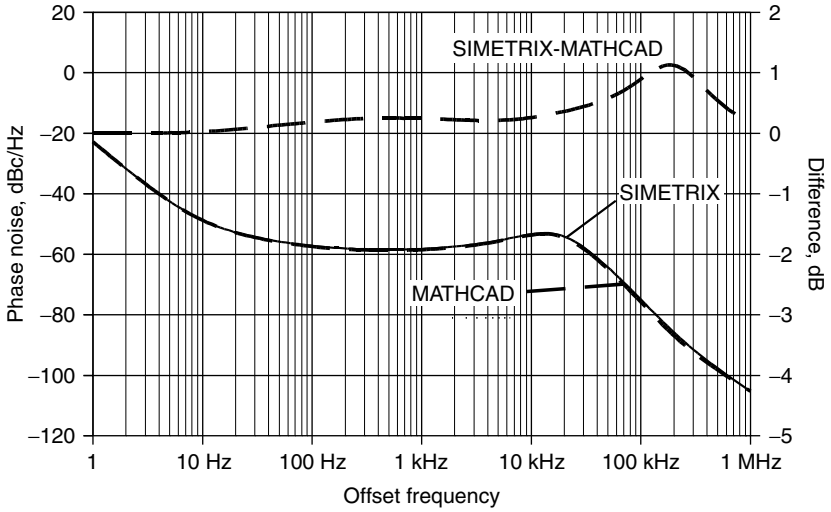


Figure 4.22 PLL output phase noise computations with SIMETRIX and MATHCAD.

4.4 Modulation of the PLL

Frequency modulation of the PLL output signal will be discussed in this section. Phase modulation with a modulating signal $m(t)$ corresponds to frequency modulation with the integral of $m(t)$. Therefore all the concepts of this section will also apply to phase modulation just considering $m(t)$ as the integral of the phase modulating signal.

There are two possible methods for output frequency modulation:

1. Frequency modulation of the reference oscillator (which has to be a tunable crystal oscillator, i.e., a crystal oscillator with a varactor in series or in shunt with the resonator).

TABLE 4.2 Comparison of PLL Analysis Methods (Update 1)

	Mathematical	Behavioral circuits
Loop components' phase noise modeling	Easy (+) By writing their expressions.	Relatively difficult (−) Frequency shaped voltage noise sources have to be synthesized.
Loop filter output noise calculation	Difficult (−) Relatively complicated expressions have to be written even for simple loop filter circuits.	Very easy (+) Automatically computed.

NOTE: (+) = advantage (more powerful or easier to use).
(−) = disadvantage (less powerful or more difficult to use).

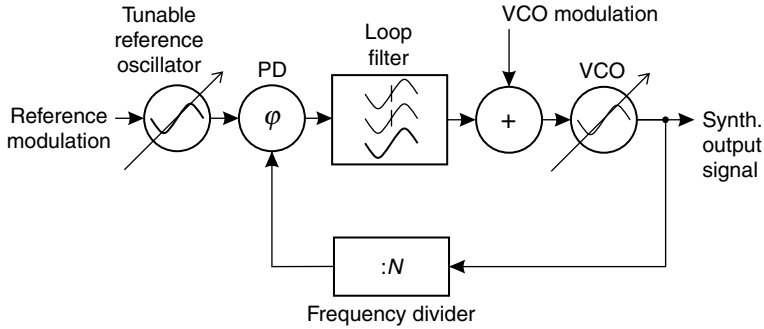


Figure 4.23 PLL with two frequency modulation points.

2. Frequency modulation of the VCO by adding the modulating voltage to the loop filter output.

Both of these possibilities are shown in Fig. 4.23.

In the remaining part of this section, it will be assumed that the PLL is locked before application of the modulating signals and that the amplitudes of the modulating signals are sufficiently small to maintain the lock condition. Once that condition is satisfied, linearity of the frequency versus tuning voltage characteristic of both the reference oscillator and VCO will be guaranteed as well.

Since the observed output quantity is the frequency (more precisely the angular frequency), the block diagram of Fig. 1.2*b* will be used as a reference and will be modified in order to insert modulation points; the resulting diagram is shown in Fig. 4.24.

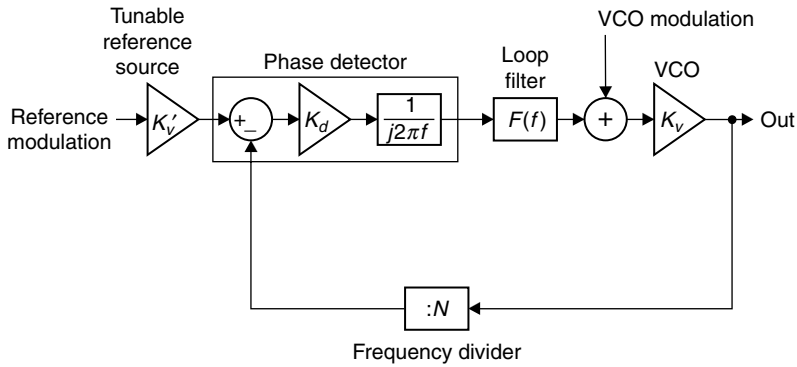


Figure 4.24 Block diagram of frequency modulated PLL.

4.4.1 Modulation of the reference oscillator only

Assume that the VCO modulation signal (indicated with "VCO modulation" in the schematic of Fig. 4.24) is zero. Let $mr(t)$ be the modulating signal of the reference oscillator signal (indicated with "Reference modulation" in the schematic of Fig. 4.24). The frequency response from "Reference modulation" to "Out" is given by the ratio of Fourier transforms of the PLL output angular frequency and $m(t)$. The reference modulation frequency response can be calculated by application of Mason's rule to the schematic of Fig. 4.24.

$$\frac{\Omega_{\text{out}}(f)}{M_R(f)} = \frac{\mathcal{F}[\omega_{\text{Out}}(t)]}{\mathcal{F}[m_r(t)]} = \frac{K_{vr}\frac{1}{j2\pi f}K_d F(f)K_v}{1+\frac{1}{j2\pi f}K_d F(f)K_v\frac{1}{N}}$$

This can be rearranged as

$$\underline{\underline{\text{RefMod}(f)}} = K_{vr}N\frac{\frac{1}{j2\pi f}K_d F(f)K_v\frac{1}{N}}{1+\frac{1}{j2\pi f}K_d F(f)K_v\frac{1}{N}} = \underline{\underline{K_{vr}NH(f)}} \qquad (4.10)$$

where K_{vr} is the reference oscillator gain expressed in $\text{rad}\cdot\text{s}^{-1}\cdot\text{V}^{-1}$. Equation (4.10) shows that the modulating signal affects the output signal through the filtering action of the PLL closed-loop frequency response.

Assuming a sinusoidal modulating signal

$$m_r(t) = A_r\cos(2\pi f_{mr}t)$$

the reference output signal is

$$\text{Ref}_{\text{out}}(t) = V_r\cos\left[2\pi f_{\text{ref}}t + \frac{K_{vr}}{2\pi f_{mr}}A_r\sin(2\pi f_{mr}t)\right]$$

and the PLL output signal is

$$\text{PLL}_{\text{out}}(t) = V_o\cos\left[2\pi N f_{\text{ref}}t + N\frac{K_{vr'}}{2\pi f_{mr}}A_r\sin(2\pi f_{mr}t+\varphi_r)\right]$$

where

$$K_{vr'} = K_{vr}\,|H(f_{mr})| \qquad \varphi_r = \arg[H(f_{mr})]$$

Summarizing, the frequency modulation of the PLL due to the reference modulation is the same as an ideal VCO tuned at Nf_{ref} with the gain equal to NK_{vr} and with the modulating signal filtered by PLL response $H(f)$ (see Fig. 4.25). $H(f)$ is a lowpass function; thus the PLL will keep the low-frequency components of the reference modulating signal and will cancel the high-frequency ones.

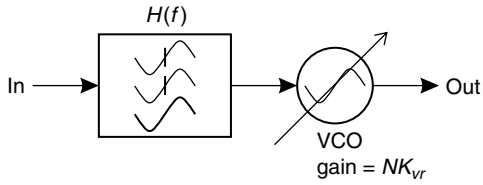


Figure 4.25 Equivalent circuit of reference modulated PLL.

4.4.2 Modulation of the VCO only

Assume now that the VCO modulation signal only is present [call it $m_v(t)$] while the modulating signal of the reference oscillator is zero. The VCO modulation frequency response can be calculated by application of the Mason rule to the schematic of Fig. 4.24 assuming "VCO modulation" as the input and "Out" as the output:

$$\underline{\underline{\mathrm{VCO_{Mod}}(f)}} = \frac{K_v}{1 + \frac{1}{j2\pi f} K_d F(f) K_v \frac{1}{N}} = \underline{\underline{K_v[1 - H(f)]}} \qquad (4.11)$$

where K_v is the VCO gain expressed in $\mathrm{rad \cdot s^{-1} \cdot V^{-1}}$. Equation (4.11) shows that the modulating signal affects the output signal as filtered by the PLL phase error response.

Assuming a sinusoidal modulating signal

$$m_r(t) = A_r \cos(2\pi f_{mv} t)$$

the PLL output signal is

$$\mathrm{PLL_{out}}(t) = V_o \cos\left[2\pi N f_{\mathrm{ref}} t + \frac{K_{v'}}{2\pi f_{mv}} A_v \sin(2\pi f_{mv} t + \varphi_v)\right]$$

where

$$K_{v'} = K_v \left|1 - H(f_{mv})\right| \qquad \varphi_v = \arg[1 - H(f_{mv})]$$

The frequency modulation of the PLL due to the VCO modulation is the same as that of an ideal VCO tuned at $N f_{\mathrm{ref}}$ with the same gain and with the modulating signal filtered by PLL error response $1 - H(f)$ (see Fig. 4.26). The function $1 - H(f)$ is highpass; therefore, the PLL will keep the high-frequency components of the VCO modulating signal and will cancel the low-frequency ones.

4.4.3 Dual-point modulation

The conclusions of Secs. 4.4.1 and 4.4.2 suggest that by feeding both the reference and VCO modulation points with the same signal, it is possible to modulate the PLL with both the low- and high-frequency components of the modulating signal. This can be done with the arrangement

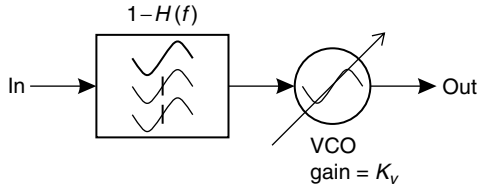


Figure 4.26 Equivalent circuit of VCO modulated PLL.

of Fig. 4.27 where the gain K_2 is needed to match the reference and VCO gain.

The frequency response from the "dual-point modulation" input to the "Out" output is given by a linear combination of Eqs. (4.10) and (4.11).

$$\text{DualPointMod}(f) = K_{vr}NH(f) + K_2K_v[1 - H(f)] \tag{4.12}$$

If $K_2 = \frac{K_{vr}N}{K_v}$, Eq. (4.12) becomes

$$\text{DualPointMod}(f) = K_{vr}N \tag{4.12'}$$

which is a constant: A perfectly balanced dual-point modulated PLL ideally has an infinite modulation bandwidth. For practical applications the infinite modulation bandwidth is too large because it allows transmission of high-frequency noise and spur components of the modulating signal. Some prefiltering of the modulating signal has to be provided. Anyway, the dual-point modulation scheme allows greater flexibility in the choice of the PLL bandwidth because of the virtual independence of the modulation bandwidth from that of the PLL.

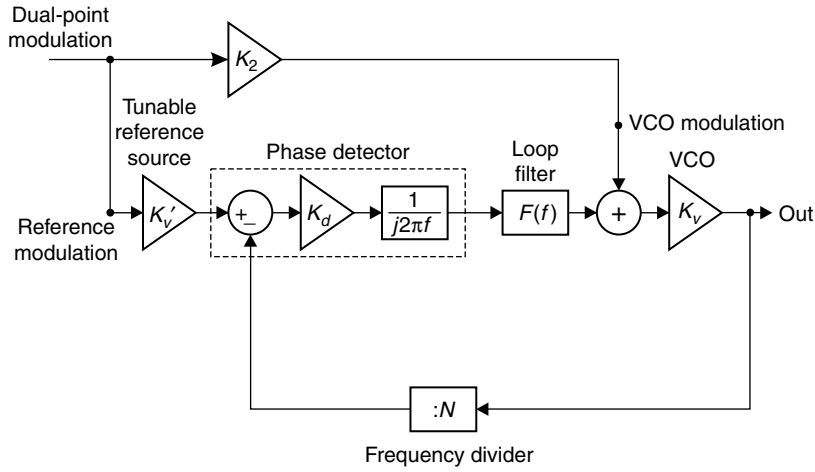


Figure 4.27 Dual-point modulated PLL.

4.5 Settling Time

In this section we will analyze the dynamics of the PLL when its output frequency is changed. Assume that the frequency division factor is initially set to $N = N_1$ and holds that value for a very long time (ideally infinite). The PLL is locked and its output frequency reaches its very stable value of $f_{\text{out1}} = N_1 f_{\text{ref}}$ where f_{ref} is the reference frequency. Now assume that N is changed to a new value $N_2 \neq N_1$. If the PLL is stable,† its output frequency will tend to its new value $f_{\text{out2}} = N_2 f_{\text{ref}}$ with a transient that will be analyzed in this section. In Sec. 2.2, it was shown that a real phase detector output is linear for limited values of phase error only. Let's assume that the frequency step $f_{\text{out1}} - f_{\text{out2}}$ is small enough to ensure small phase error values (and thus linear operation of the phase detector) during the transient. Under these conditions, it can be demonstrated that the output frequency of the PLL under analysis is the same as that of one PLL having a fixed frequency division factor $N = N_2$ (final value) and whose reference frequency has a step from $f_{\text{ref}} N_1/N_2$ to f_{ref}. To understand this, begin considering that two PLLs have the same initial and final steady-state output frequency. Furthermore, the output frequency of the second PLL in the frequency domain is given by

$$F_{\text{out}}(f) = F_{\text{in}}(f) N_2 H(f) \tag{4.13}$$

The PLL closed-loop frequency response can be written in a compact form derived from Eq. (1.8):

$$H(f) = \frac{\sum_{k=0}^{N_A} A_k (j2\pi f)^k}{\sum_{k=0}^{N_B+1} b_k (j2\pi f)^k} \qquad \text{where } N_B + 1 > N_A \quad \text{and} \quad A_0, b_0 > 0$$

Equation (4.13) can be rewritten as

$$F_{\text{out}}(f) = F_{\text{in}}(f) N_2 \frac{\sum_{k=0}^{N_A} A_k (j2\pi f)^k}{\sum_{k=0}^{N_B+1} b_k (j2\pi f)^k} \tag{4.13′}$$

†See Sec. 1.4.1 for stability definition.

or

$$F_{\text{out}}(f) = F_{\text{in}}(f)\frac{\sum_{k=0}^{N_A} a_k (j2\pi f)^k}{\sum_{k=0}^{N_B+1} b_k (j2\pi f)^k} \qquad \text{with} \quad a_k = N_2 A_k \tag{4.13''}$$

Introducing the auxiliary quantity Γ,

$$\begin{cases} \sum_{k=0}^{N_B+1} b_k (j2\pi f)^k \Gamma(f) = F_{\text{in}}(f) \\ F_{\text{out}}(f) = \sum_{k=0}^{N_A} a_k (j2\pi f)^k \Gamma(f) \end{cases} \tag{4.13'''}$$

Factor $j2\pi f$ in the Fourier domain corresponds to the derivation on the time domain, so the system of equations (4.13‴) can be written in the time domain as

$$\begin{cases} \sum_{k=0}^{N_B+1} b_k \dfrac{d^k[\gamma(t)]}{d_t^k} = f_{\text{in}}(t) \\ f_{\text{out}}(t) = \sum_{k=0}^{N_A} a_k \dfrac{d^k[\gamma(t)]}{d_t^k} \end{cases} \tag{4.14}$$

For transient calculations we are interested in solving the system of differential equations (4.14) for $t > 0$ assuming that the change of frequency division factor happens at $t = 0$. For $t > 0$ $f_{\text{in}}(t) = f_{\text{ref}}$ by hypothesis and Eq. (4.14) becomes

$$\begin{cases} \sum_{k=0}^{N_B+1} b_k \dfrac{d^k[\gamma(t)]}{d_t^k} = f_{\text{ref}} \\ f_{\text{out}}(t) = \sum_{k=0}^{N_A} a_k \dfrac{d^k[\gamma(t)]}{d_t^k} \end{cases} \tag{4.14'}$$

and initial conditions are that before changing (at $t < 0$), the output frequency is constant and equal to $f_{\text{out}}(t < 0) = f_{\text{out1}} = N_1 f_{\text{ref}}$ and all its derivatives are zero. System (4.14′) with these initial conditions is exactly the system of differential equations with the same initial conditions as that for the frequency division switching PLL. For $t < 0$ the PLL output frequency is constant (all derivatives are zero) and equal to $N_1 f_{\text{ref}}$. For $t > 0$ the output frequency evolves according to the PLL parameters' values at that time (i.e., $N = N_2$) for both frequency division and reference frequency switching PLL.

The PLL transient due to frequency switching (change of frequency division factor) can be calculated by the step response of PLL. Since we are assuming linear operation of the phase detector (remaining loop components are linear as well), it will be sufficient to calculate the unit step response. The Fourier transform of reference (input) frequency is given by the Fourier transform of the unit step:

$$F_{\text{in}}(f) = \frac{1}{j2\pi f}$$

Consider a second-order type II PLL. Its closed-loop frequency response is given by Eq. (1.13):

$$H_{\text{Active}}^{\text{2ndOrder}}(f) = \frac{j\frac{1}{Q}\frac{f}{f_n} + 1}{\left(j\frac{f}{f_n}\right)^2 + j\frac{1}{Q}\frac{f}{f_n} + 1}$$

The output response to the reference frequency unit step is given by the inverse Fourier transform of

$$\text{OutStep}(f) = N\frac{j\frac{1}{Q}\frac{f}{f_n} + 1}{\left(j\frac{f}{f_n}\right)^2 + j\frac{1}{Q}\frac{f}{f_n} + 1}\frac{1}{j2\pi f}$$

which is given by Eq. (4.15) for $Q \neq 0.5$ and by Eq. (4.15′) for $Q = 0.5$.

$$\frac{\text{outstep}(t)}{N} = 1 + \left[\frac{\sin\left(\pi\frac{\sqrt{4Q^2-1}}{Q}f_n t\right)}{\sqrt{4Q^2-1}} - \cos\left(\pi\frac{\sqrt{4Q^2-1}}{Q}f_n t\right)\right] \times \exp\left(-\pi\frac{f_n}{Q}t\right) \tag{4.15}$$

$$\left.\frac{\text{outstep}(t)}{N}\right|_{Q=\frac{1}{2}} = 1 + (2t-1)\exp(-2\pi f_n t) \tag{4.15′}$$

Equations (4.15) and (4.15′) give a normalized output angular frequency response to the reference unit step. They are plotted in Fig. 4.28 where the abscissa is time multiplied by $2\pi f_n$. For $Q > 0.5$ the second-order type II PLL step response presents damped oscillations with a frequency of $(2Q)^{-1}\sqrt{4Q^2-1}\,f_n$. This is close to the natural frequency and then to the closed-loop unit bandwidth. This concept is more general in that PLL transients, due to the output frequency switching, present damped oscillations with a frequency close to the unit gain bandwidth. Hence, the wider the bandwidth, the shorter the period of oscillations

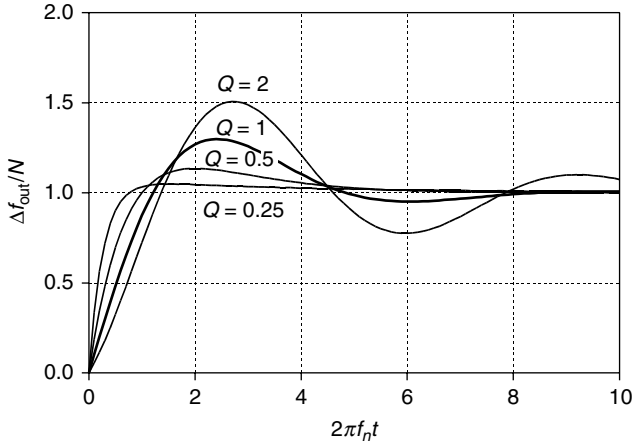


Figure 4.28 Second-order type II PLL transient response to the reference frequency unit step. Normalized output frequency = output frequency/N. Normalized time = $2\pi f_n t$.

and the faster the settling of output frequency. Wider-bandwidth PLLs have a shorter settling time,† and vice versa.

Note that the output frequency versus time has an overshoot increasing with the damping factor Q. Fig. 4.29 shows overshoot versus Q for a second-order type II PLL.

In Sec. 1.7 it was shown that the second-order type II PLL phase margin decreases and the closed-loop frequency response peak increases with the damping factor. Again, this trend is present in all PLLs with any order. The higher the phase margin, the lower the closed-loop peak and the transient overshoot.

4.5.1 Lock-in

PLL locking with linear operation of the phase detector is defined as a *lock-in*. Now we will calculate the lock-in range. To do that we will calculate the phase error which is node b_3 in the block diagram of Fig. 1.2*b*. The frequency response from the reference input (node b_1) to node b_3 is given by

$$\text{Ref\_}\Theta_e(f) = \frac{\frac{1}{j2\pi f}}{1 + \frac{1}{j2\pi f} K_d F(f) K_v \frac{1}{N}} = \frac{1 - H(f)}{j2\pi f} \tag{4.16}$$

†A wider bandwidth also gives a wider lock-in range. See Sec. 4.5.1.

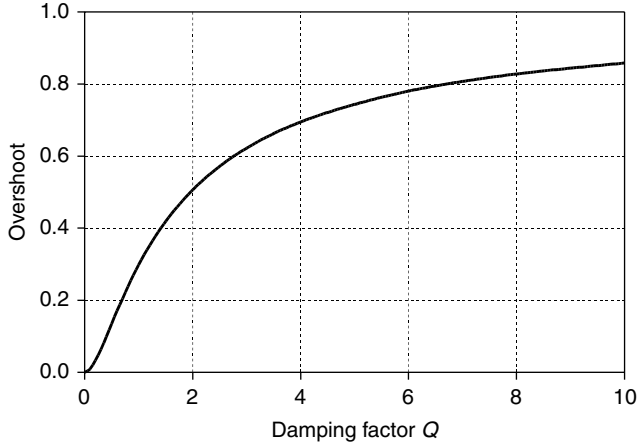


Figure 4.29 Overshoot versus Q for second-order type II PLL.

For a second-order type II PLL, Eq. (4.16) can be written as

$$\text{Ref\_}\Theta_e(f) = \frac{\left(j\frac{f}{f_n}\right)^2}{\left(j\frac{f}{f_n}\right)^2 + j\frac{1}{Q}\frac{f}{f_n} + 1}\frac{1}{j2\pi f} = \frac{\frac{jf}{f_n^2}}{\left(j\frac{f}{f_n}\right)^2 + j\frac{1}{Q}\frac{f}{f_n} + 1}\frac{1}{2\pi} \tag{4.16'}$$

The phase error due to the unit reference angular frequency step is given by the inverse Fourier transform of

$$\Theta_e\text{\_refstep}(f) = \frac{\frac{jf}{f_n^2}}{\left(j\frac{f}{f_n}\right)^2 + j\frac{1}{Q}\frac{f}{f_n} + 1}\frac{1}{2\pi}\frac{1}{j2\pi f} = \frac{\frac{1}{(2\pi f_n)^2}}{\left(j\frac{f}{f_n}\right)^2 + j\frac{1}{Q}\frac{f}{f_n} + 1}$$

which is given by Eq. (4.17) for $Q \neq 0.5$ and by Eq. (4.17′) for $Q = 0.5$

$$\theta_e\text{\_refstep}(t) = \frac{Q}{\pi f_n}\frac{\sin\left(\pi\frac{\sqrt{4Q^2-1}}{Q}f_n t\right)}{\sqrt{4Q^2-1}}\exp\left(-\pi\frac{f_n}{Q}t\right) \tag{4.17}$$

$$\theta_e\text{\_refstep}(t) = t\exp(-2\pi f_n t) \tag{4.17'}$$

The phase error due to the unit step on the reference angular frequency is plotted in Fig. 4.30 where the phase error is normalized by multiplying it by the natural angular frequency $2\pi f_n$ and time is normalized by multiplying the time by $2\pi f_n$ as well. Note that the phase error has a peak increasing with the damping factor Q; Fig. 4.31 shows that peak versus Q.

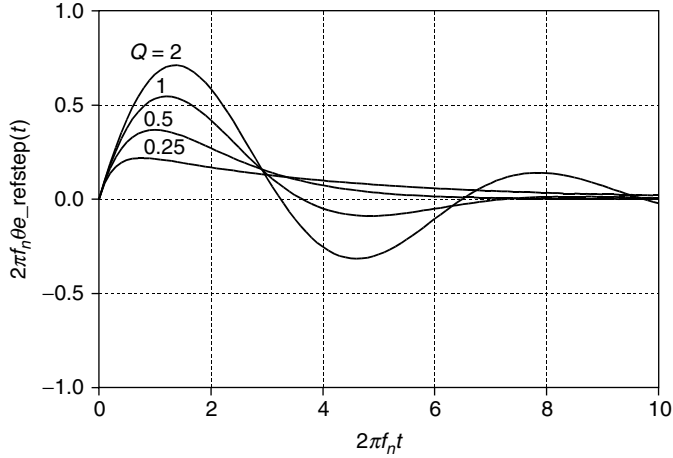


Figure 4.30 Second-order type II PLL phase error for the reference angular frequency unit step. Normalized phase error = (phase error) $2\pi f_n t$. Normalized time = $2\pi f_n t$.

The phase detector linear range depends on its type. Looking at Fig. 2.6 it can be seen that the multiplier is approximately linear[†] if the phase error magnitude is less than $\pi/4(\pm 45^\circ)$, while the PFD has a linear range of $\pm 2\pi(\pm 360^\circ)$.

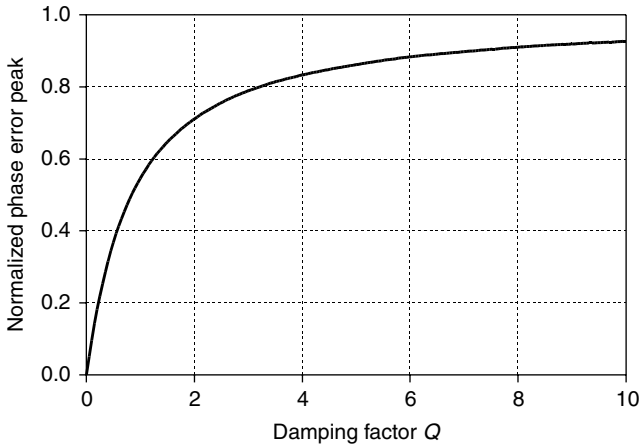


Figure 4.31 Normalized peak phase error versus Q for second-order type II PLL.

[†]The multiplier output characteristic is sinusoidal, so it is truly linear for zero phase error only. The linear range definition depends on specified nonlinearity.

The second-order type II PLL lock-in range can be computed as follows:

1. Given the damping factor Q, calculate the normalized peak phase error from the graph of Fig. 4.31. Call it NormalizedPhaseError(Q).
2. Given the PLL natural frequency f_n, calculate the peak phase error for the unit step on the angular reference frequency PeakPhaseError = NormalizedPhaseError(Q)/($2\pi f_n$).
3. If the peak phase error is less than the phase detector linear range, then the maximum amplitude of the angular reference frequency step is more than one, and vice versa. More precisely, MaxInputStep = PhaseDetectorLinearRange/PeakPhaseError.
4. The lock-in maximum output angular frequency step is MaxInputStep $\cdot N$ (where N is the final value of the frequency division factor).
5. Finally, the maximum output frequency step is MaxInputStep $\cdot N/(2\pi)$.

The phase error response of the second-order type II PLL to the input step is inversely proportional to the natural frequency and thus decreases with the unit gain bandwidth [see Eqs. (4.17) and (4.17′)]. This means that keeping the maximum phase error constant, the input step amplitude can be increased if the PLL bandwidth increases, or that the lock-in range increases with PLL bandwidth. This concept is more general: For any PLL the lock-in range increases with the closed-loop bandwidth.

Analytical calculation of the lock-in range can be quite difficult or even impossible as the loop filter complexity increases. Numerical methods can be used to circumvent this difficulty. Section 4.5.1.1 will address this.

4.5.1.1 Settling time calculation within the lock-in range. Five methods of analysis will be described, three of them are mathematical methods; the remaining two are based on behavioral model circuit analysis. All these methods will be applied to a second-order type II PLL similar to that of the previous sections with the following more detailed specifications:

- Phase detector gain: $K_d = 5/(2\pi)$
- VCO gain: $K_v = 2\pi(277 \times 10^6)$
- Frequency division factor: $N = 8000$
- Natural frequency: $f_n = 10$ kHz
- Damping factor: $Q = 1$

- Loop filter schematic like the one of Fig. 2.19 with the following components: $R_1 = 4385\ \Omega$, $R_2 = 1592\ \Omega$, $C_2 = 10$ nF.
- Reference frequency = 1 MHz

All the analysis methods that will be described will be applied to this case, and the results will be compared. A second-order PLL was chosen to make all presented methods applicable.

Method A: Analytic calculation of inverse Laplace transform. This method was essentially explained in previous sections. It consists of calculating the inverse Laplace or Fourier response of the out angular frequency response and phase error response to the unit step on the reference angular frequency. The only clarification to be added is that the Laplace transform expression coincides with the Fourier transform (setting $s = j2\pi f$) if the time domain transformed function is zero for negative values of time. This is not rigorous from a mathematical point of view since the Laplace variable s is complex while the Fourier variable $j2\pi f$ is purely imaginary. In any event it gives exact results in our case. The main drawback of this method is that it is quite difficult (if not impossible) to find inverse Laplace transforms for PLLs with an order higher than 2. That's why a second-order PLL is used as a benchmark.

Method B: Inverse Laplace transform calculation by expansion in series of Laurent. The normalized output step response is given by the inverse Fourier transform of

$$\text{OutStep}(f) = H(f)\frac{1}{j2\pi f}$$

The first step consists of calculating the poles of function OutStep(f). That function obviously has a pole in the origin due to factor $1/(2\pi f_n)$. In order to calculate the remaining poles, the closed-loop frequency response has to be written as a ratio between two polynomials:

$$H(f) = \frac{\text{Num}(f)}{\text{Den}(f)}$$

The poles to calculate are the roots of polynomial Den(f) and can be calculated by function "polyroots" (a built in MATHCAD function). Function OutStep(f) can be written as (expansion in series of Laurent)

$$\text{OutStep}(f) = \sum_{k=0}^{n} \frac{R_k}{(j2\pi f - P_k)}$$

where the P_k are the poles of the function (they are one more than the PLL order n due to the pole in the origin), and R_k is the residual in the

pole P_k. Residuals are found by calculating the limits:

$$R_k = \lim_{j2\pi f \to P_k} \text{OutStep}(f)(j2\pi f - P_k)$$

Particularly, the residual of the pole in the origin equals 1:

$$R_0 = \lim_{j2\pi f \to 0} \text{OutStep}(f)(j2\pi f_k) = H(0) = 1$$

Now the function OutStep(f) is written as the sum of $n + 1$ terms having a simple inverse Fourier transform. The normalized output step response is given by

$$\text{OutStep}(f) = 1 + \sum_{k=1}^{n} R_k \exp(-P_k t)$$

The phase error can be calculated by applying the same procedure, because it has the same poles P_k with different residuals that have to be recalculated.

Method C: FFT. If poles and/or residual calculation is impossible [because of a high PLL order, or because the analytic expression of $H(f)$ is not available since it is defined on discrete points only and interpolated], it is still possible to numerically calculate the Fourier transform and its inverse with the fast Fourier transform (FFT). The FFT is a fast algorithm for calculation of the DFT. From our practical point of view, the main difference between the Fourier transform and the FFT is that the first deals with continuous functions defined for $t \in (-\infty; +\infty)$, while the latter deals with functions defined in a discrete and finite number of points equally spaced and distributed over a finite time interval $t \in [0; T_{\text{FFT}}]$. The number of sampling points has to be an integer power of 2, so they are defined as

$$t_k = T_{\text{FFT}} \frac{k}{2^{N_{\text{FFT}}} - 1} \qquad \text{with} \qquad k = 0, \ldots, 2^{N_{\text{FFT}}} - 1$$

Furthermore the FFT works as a sampled function that is periodic with period T_{FFT}, so its resolution frequency is $1/T_{\text{FFT}}$ and the maximum frequency is half of the sampling frequency:

$$f_{\text{MAX}} = \frac{1}{T_{\text{FFT}}} 2^{N_{\text{FFT}}-1}$$

Because of this periodicity the chosen time interval has to be sufficiently large to allow a significant reduction of the switching transient at the end of the interval. The step stimulus will no longer be located in $t = 0$, but it will be located in the center of the sampling interval $T_{\text{FFT}}/2$.

The out frequency response to the reference step will be calculated as follows:

- Define a time interval T_{FFT} many times as the reciprocal of the PLL unit gain bandwidth.
- Define an integer power for sampling points N_{FFT} (usually around 10).
- Define the input step as

$$\eta(t) = \mathrm{if}\left(t < \frac{T_{\mathrm{FFT}}}{2}, 0, 1\right)$$

- The sample input step is

$$u_k = \eta(t_k) \qquad \text{with} \qquad t_k = T_{\mathrm{FFT}} \frac{k}{2^{N_{\mathrm{FFT}}} - 1}$$

- Calculate the FFT of the input step:

$$U = \mathrm{FFT}(u)$$

- The filter U with the PLL frequency response is

$$V = UH\left(\frac{k}{T_{\mathrm{FFT}}}\right) \qquad \text{with} \qquad k = 0, \ldots, 2^{N_{\mathrm{FFT}}-1}$$

- Calculate the inverse FFT of V:

$$v = \mathrm{IFFT}(V)$$

- Interpolate v to generate a continuous time response.

The same procedure has to be followed for the phase error calculation by simply replacing the frequency response $H(f)$ with $\mathrm{Ref\_}\Theta_e(f) = \frac{1-H(f)}{j2\pi f}$.

The FFT method is always applicable. The only requirement is the availability of a complex expression for the loop filter frequency response (magnitude and phase or real and imaginary part). That expression can be analytic or an interpolating function from discrete points.

Methods A, B, and C can be implemented[†] in MATHCAD and give almost coincident results.

Method D: Behavioral model of reference switching PLL. The analyzed circuit has to model the block diagram[‡] of Fig. 1.2b as shown in Fig. 4.32. The phase detector is modeled by components $E3$, $H1$, $E2$, $R6$, $L1$, $R1$,

[†]See the MATHCAD file Second_Order_PLL_Step_Response.MCD.

[‡]See the SIMETRIX file PLL_2nd_Order_Step.sxsch.

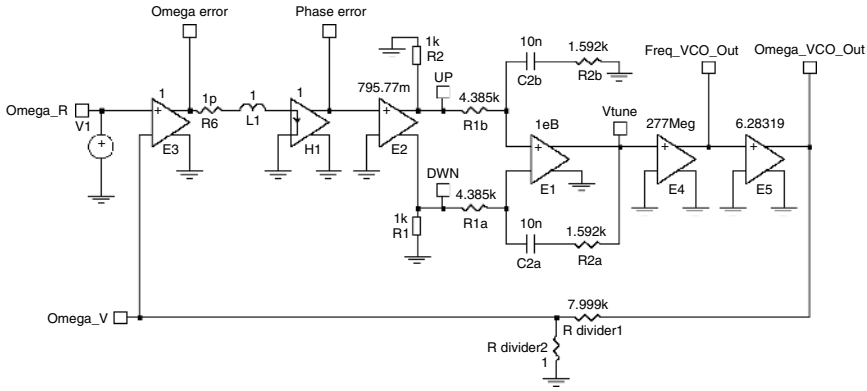


Figure 4.32 Circuit for PLL settling time simulation.

and $R2$. The integrator consists of $R6$, $L1$, and $H1$. The loop filter is modeled by components $E1$ (opamp) $R1a$, $R1b$, $R2a$, $R2b$, $C2a$, and $C2b$. The VCO is modeled by components $E4$ and $E5$; the latter transforms the output frequency into an angular frequency by multiplying it by 2π. The voltage divider made by resistors Rdivider1 and Rdivider2 models the frequency divider. The reference and divided VCO angular frequency are voltages on nodes Omega_R and Omega_V, the angular frequency and phase error are voltages on nodes OmegaError and PhaseError, the tuning voltage is the voltage on node V_{tune}, and the VCO output frequency and angular frequency are the voltages on nodes Freq_VCO_Out and Omega_VCO_Out.

The circuit of Fig. 4.32 can still be used for closed-loop and phase error responses simply by performing an AC analysis (input generator V1 has to be an AC source) and probing AC voltages on nodes Omega_V and OmegaError. Switching of the transient calculation is straightforward as well: Input generator V1 has to be a voltage step, the transient analysis has to be performed, and interested quantities are picked by probing the voltage on the corresponding node. The normalized output step response is the voltage on node Omega_V.

Method E: Behavioral model of frequency divider switching PLL. This method is the closest one to the physical representation of the frequency switching PLL. Indeed the output frequency of the PLL synthesizer is usually changed by changing the frequency division factor rather than by changing the reference frequency. Nevertheless we found in Sec. 4.5 that two operations are equivalent and analysis methods A, B, C, and D are based on the time-varying reference frequency. The circuit used for application of this method is very similar to the one of Fig. 4.32 with two changes:

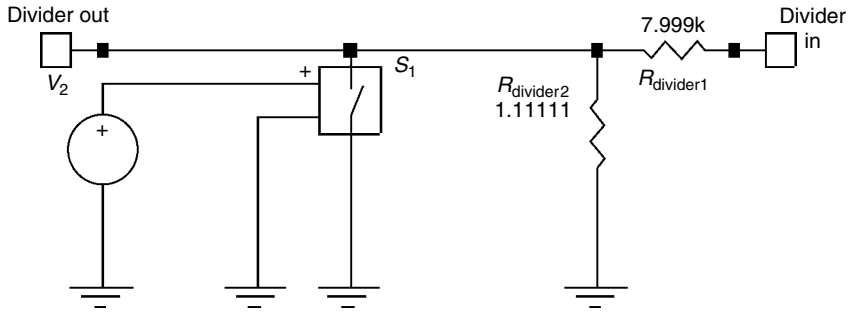


Figure 4.33 Behavioral model for time-varying frequency divider.

1. The input generator V1, which originally was a voltage step is replaced by a fixed voltage whose amplitude is the reference angular frequency $= 2\pi \times 10^6$.
2. The fixed voltage divider made by Rdivider1 and Rdivider2 is replaced by a time-varying voltage divider. It is shown in Fig. 4.33. $S1$ is a voltage-controlled switch. When the input voltage is lower than $V_{\text{off}} = 0.49$ V, its output resistance is $R_{\text{off}} = 10\ M\Omega$. For an input voltage higher than $V_{\text{on}} = 0.51$ V, the output resistance is $R_{\text{on}} = 10\ \Omega$. The voltage generator V_2 is a unit voltage step at $t = 0$.

Thus for $t < 0$ the voltage division factor is given by

$$N1 = \left(\frac{R\text{divider2}//R\text{off}}{R\text{divider2}//R\text{off} + R\text{divider1}} \right)^{-1} \cong 7200.1152$$

For t > 0 $S1$ switches on and the voltage division factor becomes

$$N2 = \left(\frac{R\text{divider2}//R\text{on}}{R\text{divider2}//R\text{on} + R\text{divider1}} \right)^{-1} \cong 8000$$

Consequently the output frequency switches from about $F_{\text{start}} = 7.2$ GHz to $F_{\text{stop}} = 8$ GHz. Normalization can only be applied to this circuit by plotting the following expressions:

$$\begin{aligned} \text{NormalizedOutputFrequency} &= \frac{\text{FreqVCO\_Out} - \text{F}_{\text{start}}}{\text{F}_{\text{start}} - \text{F}_{\text{stop}}} \\ &= \frac{\text{FreqVCO\_Out} - (7.2 \times 10^9)}{(8 \times 10^9) - (7.2 \times 10^9)} \end{aligned}$$

$$\begin{aligned} \text{NormalizedPhaseError} &= \frac{\text{PhaseError}}{\Delta\omega_{\text{in}}} = \frac{\text{PhaseError}}{\frac{2\pi\,\Delta f_{\text{out}}}{N_2}} \\ &= \frac{\text{PhaseError}}{\frac{2\pi(F_{\text{stop}} - F_{\text{start}})}{N_2}} = \frac{\text{PhaseError}}{2\pi\,10^5} \end{aligned}$$

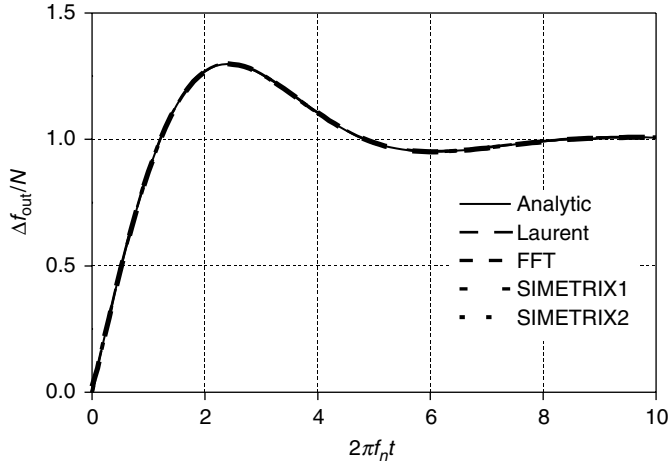


Figure 4.34 Calculations of the normalized output frequency step response.

Results from applications of methods A, B, C, D, and E are plotted in Fig. 4.34 which shows the normalized output angular frequency (ω_{out}/N) versus the normalized time ($t2\pi f_n$) and in Fig. 4.35 which shows the phase error versus normalized time. All the curves refer to the unit step on the reference angular frequency. It can be seen that all five methods are very consistent and give quite close results.

All the above described methods allow for calculation of the maximum output frequency step lock-in range. This can be done by increasing

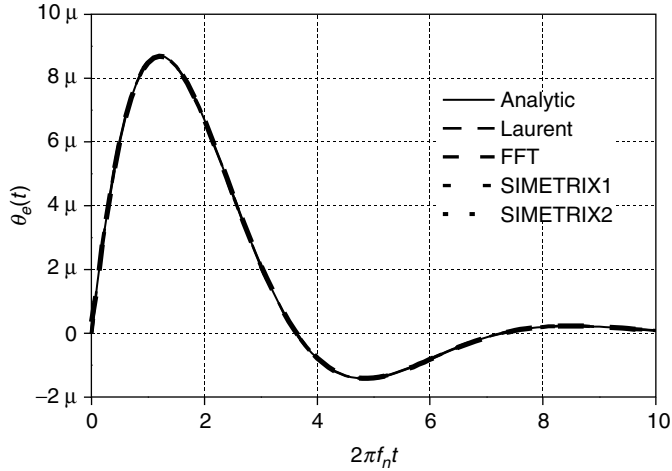


Figure 4.35 Calculations of the phase error step response.

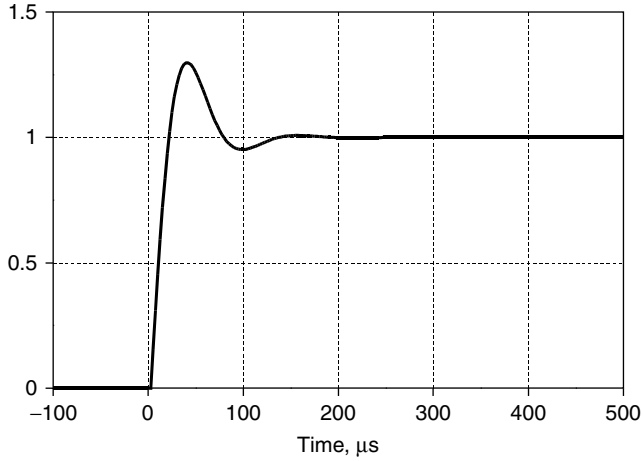


Figure 4.36 Second-order type II PLL ($f_n = 10$ kHz, $Q = 1$) output normalized step response.

the input step amplitude (all outputs will increase proportionally since the system is assumed to be linear) up to where the peak phase error exceeds the phase detector linear range and displaying the output frequency step corresponding to this limited case.

A final observation has to be made about the output frequency step response. Figure 4.36 shows the same curve of Fig. 4.34 but with time on a larger interval, and not normalized. Looking at that picture it is really difficult to say if the PLL is locked after 200, 300, 400, or 500 μs. To answer the question whether or not the PLL is locked, a frequency error has to be specified. More precisely Fig. 4.36 shows a normalized output frequency. Thus the frequency error relative to the frequency step has to be specified. The PLL is locked at a given time t_{lock} if and only if the normalized output frequency is definitely within specified limits at that time (i.e., for all $t > t_{\text{lock}}$). One way to check for this is to expand the y scale around 1, as Fig. 4.37 shows, but it is not possible to simultaneously see the initial part of the transient with this method. Another solution is to plot the magnitude of the relative frequency error on a logarithmic y scale: Large and small values of the frequency error can simultaneously be displayed.

$$\text{RelativeError}(t) = \left| \frac{\text{OutputFrequency}(t) - \text{InitialOutputFrequency}}{\text{FinalOutputFrequency} - \text{InitialOutputFrequency}} \right|$$

Figure 4.38 shows a log plot of the frequency error.

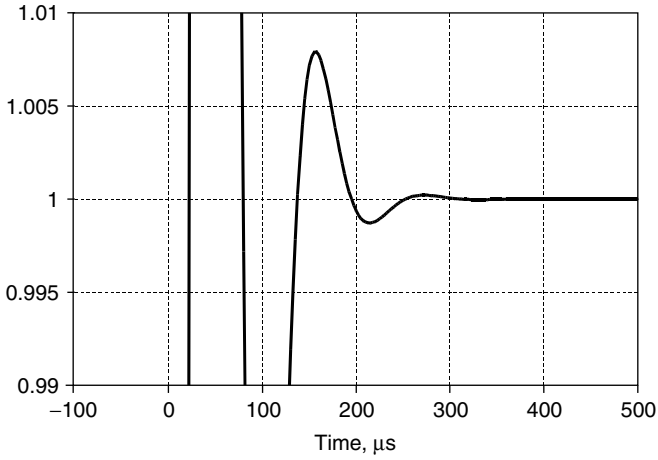


Figure 4.37 Graph of Fig. 4.36 with expanded y axis.

4.5.2 Pull-in

The PLL transient when the phase detector works outside of its linear region will be discussed in this section. Linear differential equations (4.14) and (4.14′) are no longer valid because of the phase detector nonlinearity. Consequently mathematical methods A, B, and C described in Sec. 4.5.1.1 are no longer valid. Thus nonlinear differential equations have to be solved: This is what the SPICE transient analysis does. Methods D and E are still valid; the first will be used in this section since it is

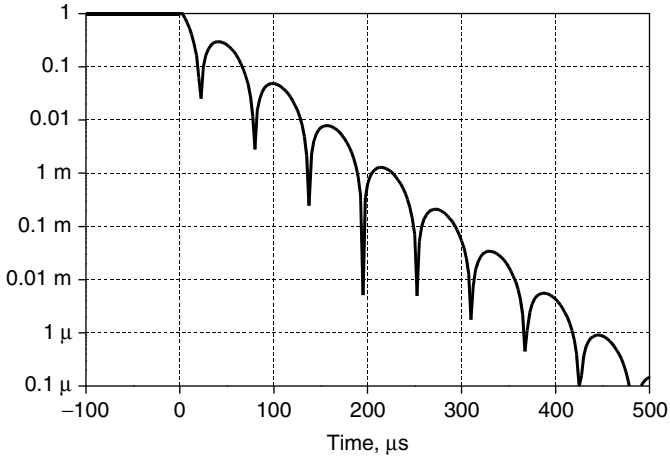


Figure 4.38 Second-order type II PLL ($f_n = 10$ kHz, $Q = 1$) frequency error log plot.

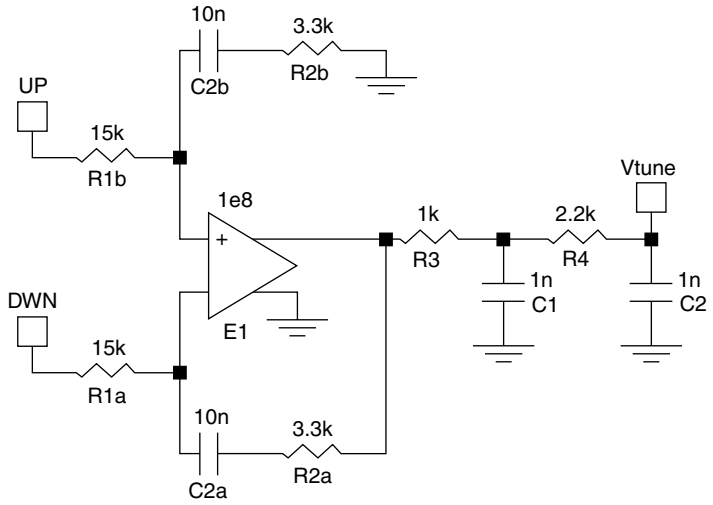


Figure 4.39 Schematic of third-order loop filter for pull-in analysis.

equivalent to the other and is more flexible. When the phase detector is operating nonlinearly, two situations are possible: For relatively small frequency division steps, the PLL still locks; for higher steps, it doesn't. The maximum output frequency step that allows the PLL to lock is defined as the *pull-in range*. The pull-in process involves by definition nonlinear operation of the phase detector; thus it depends on the used phase detector. Although some approximated formulas are available for pull-in of some particular PLL (usually of low order), this section will describe methods for accurate numerical calculation in more general cases. Two cases will be considered: multiplier and PFD. A fourth-order PLL will be analyzed with the same parameters as the one in Sec. 4.5.1.1 (which is second-order) but with a different loop filter, the schematic of which is shown in Fig. 4.39.

The PLL loop filter of Fig. 4.32 was replaced with the filter of Fig. 4.39 and AC analysis has been performed[†] in order to calculate the closed-loop $H(f)$ and phase error response $1 - H(f)$. The results are shown in Fig. 4.40. The basic linear performances of PLL were found to be

- Phase margin = 49°
- Closed-loop unit gain bandwidth = 8.97 kHz
- Closed-loop response peak = 3.75 dB

[†]See the SIMETRIX file PLL_4th_Order_Step.sxsch.

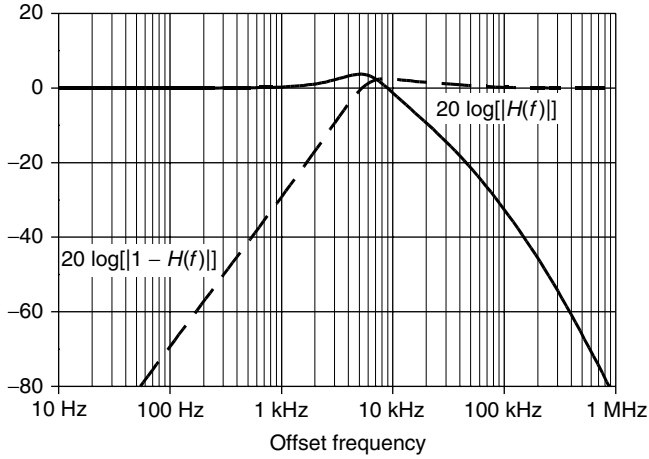


Figure 4.40 Response of type II fourth-order PLL with the loop filter of Fig. 4.39.

Assuming that the phase detector is a PFD, the linear phase error range is clearly defined as $\pm 2\pi$, the input step amplitude was increased up to where the phase error peak reaches the value of 2π, and the output frequency is displayed finding a lock-in range of 466.35 MHz (amplitude of output frequency step after the transient). If a multiplier is used as the phase detector, determination of the linear operating range is more difficult, and a linear analysis approach is not sufficient to delimit between the lock-in and pull-in range.

4.5.2.1 Pull-in for the PLL with a multiplier phase detector. The multiplier phase detector has a sinusoidal characteristic. The model for the phase detector has to be changed in the above used circuit. The phase detector model has to be complicated in order to introduce the sinusoidal output characteristic. This can be done with the circuit of Fig. 4.41. The voltage on nodes Omega_R and Omega_V corresponds to the reference and divided VCO angular frequencies. The voltage on node OmegaError is the angular frequency error; its integral (voltage on node PhaseError) is the phase error. The nonlinear voltage-controlled generator ARB2 has an output voltage equal to the sine of the phase error and models the sinusoidal characteristic of the multiplier. The VCVS E2 models the phase detector gain: It is assumed to be the same small signal gain $K_d = 5/(2\pi)$ of the linear case. Moreover the multiplier is modeled with a differential output. Differently from PFDs, multipliers usually have single-ended output, but this can easily be simulated by connecting node Up to ground and simplifying the loop filter of Fig. 4.39 by removing R1b, R2b, and C2b and connecting the opamp noninverting input to ground: Two circuits are perfectly equivalent and give the same result.

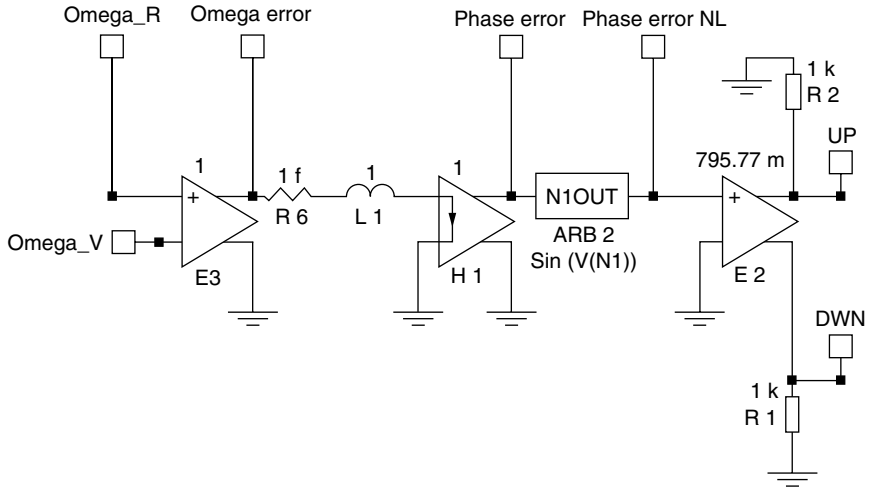


Figure 4.41 Behavioral model for the multiplier phase detector.

In the schematic of Fig. 4.41 (used for lock-in calculation), the phase detector (components E3, R6, L1, and H1) had a linear input-output characteristic. Here, the phase detector (see Fig. 4.41) has a sinusoidal input-output characteristic.[†] The input voltage step is delayed by 100 μs to make switching transients beginning at that time. Four meaningful cases were found:

1. Quasi-linear operation:

   Phase error over time within the range [−0.113; 0.713]
   Output frequency step = 51 MHz

2. Moderate nonlinear operation:

   Phase error over time within the range [−0.376; 1.729]
   Output frequency step = 102 MHz

3. Strong nonlinear operation:

   Phase error over time within the range [0; 70.31]
   Output frequency step = 204 MHz

4. Very strong nonlinear operation:

   Phase error over time within the range [0; ∞] linearly increasing about 600 V/ms
   Output frequency step = 800 MHz (PLL does not lock)

[†]See the SIMETRIX file PLL_4th_Order_Step_NonLinear_Sine.sxsch.

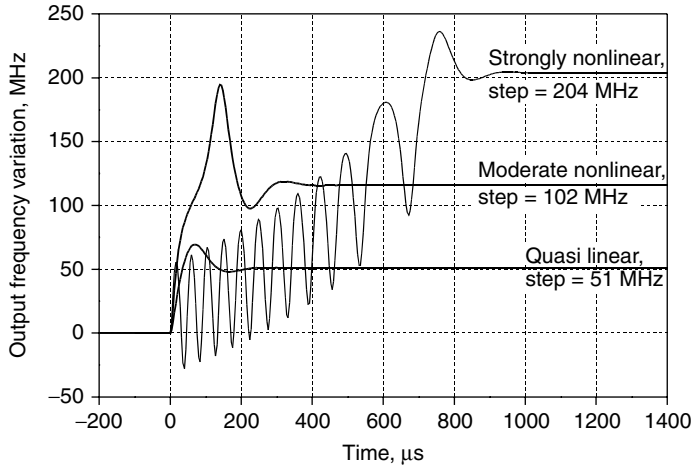


Figure 4.42 Pull-in process for type II fourth-order PLL with a multiplier as the phase detector.

Note that the multiplier phase detector characteristic (see Fig. 2.2) has a monotonic phase error range of $\pm\pi/2 \cong 1.571$, so case 3 only exceeds the monotonic (which does not mean linear) range. Results of the three different cases 1, 2, and 3 are shown in Fig. 4.42, while curve 4 is plotted in Fig. 4.43.

It can be seen that for small values of the frequency step (case 1), the switching transient is very close to that calculated with the linear model. As the frequency step increases, the transient waveform is distorted with increased overshoot percentage and lock time (case 2).

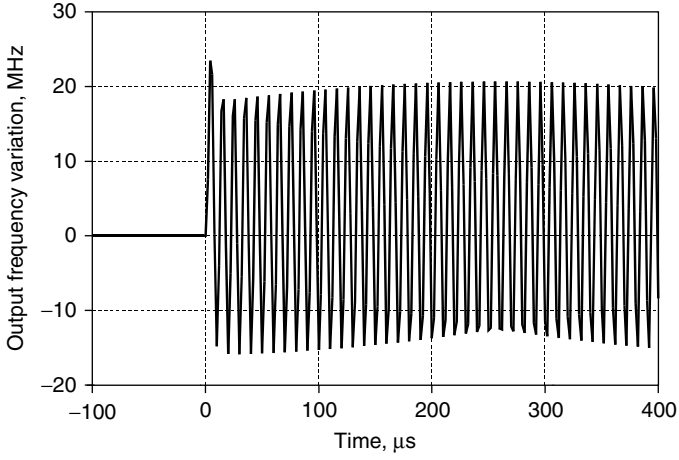


Figure 4.43 Pull-out process for type II fourth-order PLL with a multiplier as the phase detector.

Further increasing the output frequency step (case 3) creates undulations in the beginning part of the switching transient (portion of curve 3 from 100 to about 800 μs). This shape of the output frequency versus time curve is very typical of the pull-in process. In cases 2 and 3 after the initial distorted or rippled initial transient, the output frequency tends to its final value with the same shape as that of the linear operation. Pull-in is slower than lock-in because of this added portion of the switching transient. For a fast PLL, the lock difference between the initial and final output frequency has to be less than the lock-in range.

The pull-in range is calculated by increasing the input step amplitude up to the condition shown in Fig. 4.43 when the output frequency oscillates around zero without tending to any value, and the phase error continues to increase quite linearly over time without any apparent limit. The pull-in range is given by

$$\text{PullInRange}\,[Hz] = \text{InputVoltageStep}(\text{FrequencyDivisionFactor})\frac{1}{2\pi}$$

The analyzed PLL pull-in range is about 800 MHz.

The pull-in range has to be wider than the VCO output frequency excursion with the minimum and maximum possible tuning voltages which correspond to the saturated low and high output voltages of the operational amplifier. If this condition is not reached, switching on the PLL power supply may generate a transient that pushes the opamp out voltage to its saturated minimum or maximum voltage; in this case the VCO output frequency may go far from the needed value, and the PLL may not lock. When that requirement is not achievable, acquisition lock circuits have to be used:

- Coarse VCO pretuning. A DAC tunes the VCO at the required output frequency. The PLL only has to correct the output frequency error due to the open-loop VCO tuning, temperature drift, aging, etc. This way a narrower pull-in range is required and/or pull-in occurs for a smaller output frequency step, and the PLL locks faster due to the reduced output frequency step.
- Ramp added on tuning voltage. A slow voltage ramp is added to the VCO tuning voltage. The frequency sweeps from its minimum to its maximum value, when it passes close to its lock value (the wanted final frequency of the PLL), the loop locks it. Sometimes lock indication circuits are added which disable the ramp when the PLL is locked. Several solutions are possible for the lock indication circuit. The simpler solution is an AC detector on the loop filter output: When the PLL is locked, the tuning voltage is a stable DC.
- Discriminator-aided lock. The PLL output frequency is measured with a frequency discriminator, and an error signal is generated

proportional to the difference between the measured and required frequencies and feeds back the tuning voltage. This circuit is more properly known as the frequency and phase-locked loop (FPLL).

- Dual-band PLL. At the end of Sec. 4.5 it was stated that wider-band PLLs have a wider lock-in range; this is true also for pull-in. Two loop filters are used with two different PLL bandwidths: A wideband filter (with a wider pull-in range) is used during the output frequency switching; a narrowband filter is used in the lock condition. A lock indicator is used to select the proper filter.

4.5.2.2 Pull-in for the PLL with a Phase Frequency Detector. From the discussion about PFDs in Sec. 2.2.2 we know that the PFD has a clearly defined linear phase error range of $\pm 2\pi$. The lock-in range can be exactly calculated with linear simulation as explained in Sec. 4.5.2. Section 2.2.2 also states (see Fig. 2.7) that for large phase error values due to input signals with different frequencies, the PFD output voltage becomes about +Vdd/2 (or −Vdd/2) if the divided VCO frequency is lower (or higher) than the reference frequency. This characteristic of the PFD will push the VCO frequency in the right direction: Reducing or increasing the VCO frequency whether it is higher or lower than the set value. The PLL with phase frequency detector locks for any value of the output frequency step. The pull-in range of a PLL employing a PFD is infinite.

The first attempt to simulate the pull-in process for the PLL with the PFD was to replace the nonlinear voltage-controlled voltage source ARB2 (whose output is the sine of the input voltage) with another one implementing the PFD characteristic given by Eq. (2.4), which can be rewritten in terms of input and output voltages as

$$V_{\text{out}} = \left\{ \frac{1}{\pi} \text{atan} \left[\tan \left(\frac{V_{\text{in}} - \pi}{2} \right) \right] + \text{if}(V_{\text{in}} > 0, 0.5, -0.5) \right\} V_{\text{in}}$$

Unfortunately, that simulation does not work, maybe because of the many discontinuities present in the preceding equation. The behavioral model approach has to be abandoned if the pull-in process for the PLL with the PFD has to be simulated.

This new circuit[†] is more a high-level physical PLL model rather than a behavioral model. It describes all components of a PLL: reference source, PFD, loop filter, and VCO. The PFD circuit is shown in Fig. 4.44. It describes exactly the circuit of Fig. 2.3. Two resistors R1 and R2 were added for simulator needs coming from the interface between the digital components of PFD and the analog components of the loop filter. The

[†]See the SIMETRIX file PLL_4th_Order_Step_NonLinear_PFD.sxsch.

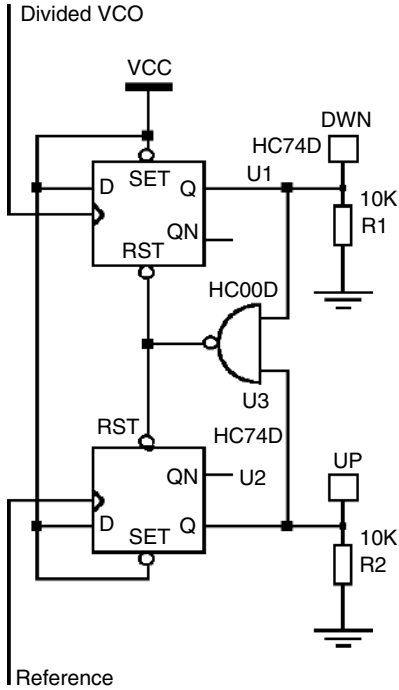


Figure 4.44 Phase frequency detector circuit used for pull-in simulation.

loop filter schematic is still that of Fig. 4.39 since the behavioral model of the loop filter coincides with the physical model; in other words, the output voltage models itself.

A physical model of the VCO is shown in Fig. 4.45. The voltage on node 3 is zero at the beginning of the simulation time ($t = 0$), For $t > 0$ the voltage on node 3 is given by the solution of the differential equation:

$$\mathrm{V2}(t) = \mathrm{V3}(t) + \mathrm{R5} \cdot \mathrm{C4} \frac{d\,\mathrm{V3}(t)}{d\,t} \tag{4.18}$$

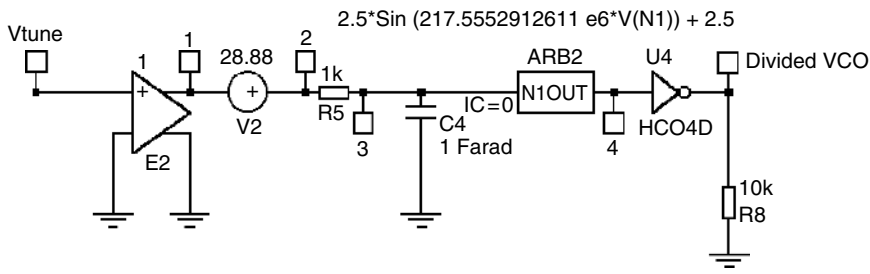


Figure 4.45 VCO circuit used for pull-in simulation.

Now, for small values of t it can be assumed[†] that V3 $\ll$ V2. Then Eq. (4.18) can be well approximated as

$$\mathrm{V2}(t) \cong \mathrm{R5}\cdot\mathrm{C4}\frac{d\,\mathrm{V3}(t)}{d\,t} \Rightarrow \mathrm{V3}(t) \cong \frac{1}{\mathrm{R5}\cdot\mathrm{C4}}\int_0^t \mathrm{V2}(\tau)\,d\,\tau$$

$$= 10^{-3}\int_0^t \mathrm{V2}(\tau)\,d\,\tau \qquad (4.18')$$

The node on voltage 4 is given by

$$\mathrm{V4}(t) = v_p \sin\left[a\mathrm{V3}(t)\right] + v_o \quad \text{with} \quad v_p = v_o = 2.5,\ a \cong 217.55\times 10^6 \qquad (4.19)$$

Substituting Eq. (4.18′) into Eq. (4.19) we obtain

$$\mathrm{V4}(t) \cong v_p \sin\left[a10^{-3}\int_0^t \mathrm{V2}(\tau)\,d\,\tau\right] + v_o \qquad (4.20)$$

The relation between the VCO tuning voltage and the output signal is given by

$$\mathrm{VCO}_{\mathrm{out}}(t) \cong \mathrm{VCO}_{\mathrm{amplitude}} \sin\left[K_v\int_0^t \mathrm{V}_{\mathrm{tuning}}(\tau)\,d\,\tau\right] \qquad (4.21)$$

Comparing Eq. (4.20) with (4.21), we see that components R5, C4, and ARB2 create a VCO with gain $K_v = a\times 10^{-3}$, amplitude v_p, and out offset voltage v_o, so the VCO's output voltage (node 4) swings between $v_o - v_p = 0$ and $v_o + v_p = 5$ V. The CMOS inverter U4 converts the sinusoidal output from node 4 into a square wave with CMOS levels. The circuit of Fig. 4.45 models a VCO cascaded with a frequency divider; node 5 is the frequency divider output. Insertion of a frequency divider is not impossible; it only needs some flip-flops and some combinatory logic, but note the following:

1. A frequency divider is not essential because the phase detector deals with the frequency divider output and no other loop component uses the VCO output signal (apart from the frequency divider, of course). The VCO output signal is simply the divider output signal with time divided by the frequency division factor.
2. Adding a frequency divider will greatly increase the computation time because the time step has to be a small fraction of the shorter

[†]The PLL lock time is on the order of milliseconds, while the time constant $\mathrm{R5}\cdot\mathrm{C4} = 10^3$ seconds.

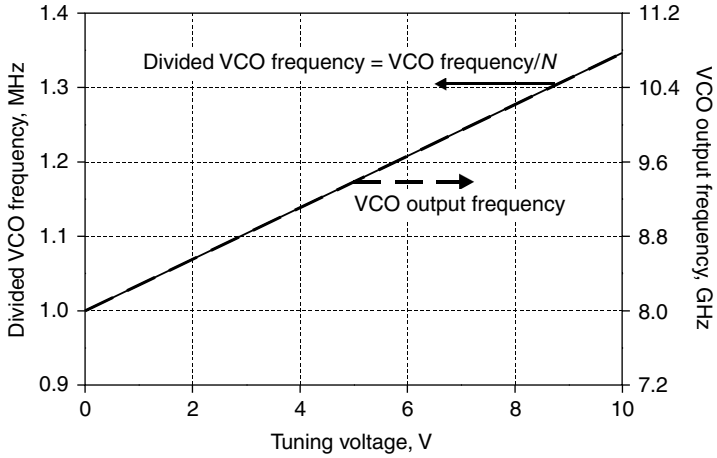


Figure 4.46 Tuning characteristic of the VCO of Fig. 4.46.

period of the faster signal in the circuit. Elimination of the frequency divider makes the highest frequency in the circuit $N = 8000$ times lower than the VCO output frequency; the simulation time is decreased by the same factor.

Now $K_v = a \times 10^{-3} \cong 2\pi(277 \times 10^6)/8000$; thus the VCO modeled by the circuit of Fig. 4.45 has a gain equal to that used for calculations in the other sections of this chapter divided by the frequency division factor of 8000.

The unit gain buffer E_2 and the fixed voltage generator V2 add an offset to the tuning voltage (node V_{tune}) making the output frequency assume a value of 1 MHz (VCO frequency of 8 GHz) for a tuning voltage of approximately 0 V. The output frequency of the circuit[†] in Fig. 4.45 is plotted in Fig. 4.46 versus the tuning voltage; this is the divided VCO frequency. We obtain the not-divided frequency by multiplying the divided VCO frequency by the frequency division factor.

The frequency divider is not explicitly present in the simulation circuit; therefore, only the reference frequency step approach can be implemented. Pull-in simulation is performed by stepping the reference frequency. The circuit of Fig. 4.45 is also used to generate the reference signal. Here a voltage step generator is connected between the tuning input and ground and has a zero initial value. Transient analyses are performed with some increasing step values, and the VCO output frequency is plotted versus time. The PLL output frequency is not directly available, but it can be picked by probing the tuning voltage and keeping in mind that the VCO output frequency versus the tuning frequency

[†]See the SIMETRIX file VCO_PullIn.sxsch.

is given by

$$\text{VCOfrequency}_{\text{MHz}}(\text{TuningVoltage}_{\text{Volt}}) = 277(\text{TuningVoltage}_{\text{Volt}} + 28.88) \tag{4.22}$$

The choice of the offset voltage is somewhat arbitrary. Different assumptions cause translation of the VCO tuning characteristic without affecting the gain. The chosen offset makes the reference frequency 1 MHz (and thus the output steady-state frequency is 1 MHz corresponding to the PLL output frequency of 8 GHz) before application of the voltage step. However what really matters is the frequency step and not the initial and final frequencies. In Sec. 4.5.2 it was found that a lock-in range of 466.35 MHz corresponds to a tuning voltage step of $466.35/277 = 1.68$ V. Two cases have been analyzed:

1. Output frequency step of 400 MHz, a little bit less than the lock-in range.
2. Output frequency step of about 888 MHz, about twice the lock-in range, corresponding to a voltage step of 3.2 V.

The resulting output frequency transients (beginning at $t = 100\ \mu$s) are shown in Fig. 4.47. Curve (c) comes from the linear calculation of case 1. Linear simulation with behavioral models and nonlinear simulation with the physical model give consistent results.

The physical model simulation is inherently discrete time; sampling effects are automatically taken into account by the PFD model.

The pull-in process on the PLL with the PFD is characterized by the presence of undulations superimposed on the output frequency ramp-up. This can be observed in Fig. 4.47 by looking at the initial portion of curve (b), the one delimited by point (f). These undulations look like double-wave-rectified sinusoids with increasing amplitude, while those of Fig. 4.42 look like sinusoids with increasing amplitude: Both these two shapes are characteristic of a used phase detector (PFD or multiplier). An interesting approximate calculation of the pull-in process can be performed based on analysis of curve (b). Let f_r and f_v be the reference and divided VCO frequencies. It is $f_v < f_r$ from the transient beginning at $t = 100\ \mu$s up to about $t = 240\ \mu$s: that region is delimited by points marked with (e). Below 100 μs the PLL is locked. Therefore, for $t < 100\ \mu$s the phase detector output is zero, and for $100\ \mu\text{s} < t < 240\ \mu$s the phase detector output is a nonperiodic pseudo square wave with a mean value of Vdd/2 as described in Sec. 2.2.2. When input signals have a slightly different frequency, the PFD average output plotted in Fig. 2.7 can be approximated with the following formula:

$$V_{\text{det,pull-in}} \cong \frac{\text{Vdd}}{2} \quad \text{if}(f_r > f_v, 1, -1) \tag{4.23}$$

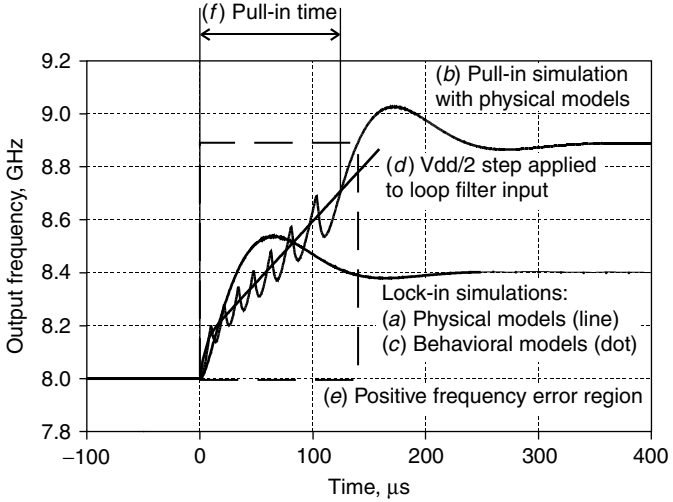


Figure 4.47 Pull-in process for type II fourth-order PLL with phase frequency detector. (*a*) Transient simulation with physical nonlinear model within lock-in range, (*b*) transient simulation with physical nonlinear model out of lock-in range, (*c*) transient simulation of case (*a*) with behavioral linear model, (*d*) response of loop filter cascaded with VCO to a Vdd/2 voltage step, (*e*) region of positive frequency error, (*f*) pull-in time.

Consequently for $t < 240$ μs the tuning voltage can be approximated by the loop filter response† to an input voltage step with an amplitude of Vdd/2 differentially applied between the Up and Dwn inputs. That waveform can be transformed into the PLL output frequency by application of the VCO characteristic, which is given by Eq. (4.22) in our case. The result is curve (*d*) of Fig. 4.47. It can be considered as a good approximation of the pull-in part of the tuning transient for the practical purpose of the settling time calculation. Approximate evaluation of the lock time taking the pull-in time into account, can be done for the PLL with a PFD considering that the output frequency follows curve (*d*) until the frequency error becomes lower than the lock-in range. From that point, the residual error tends to zero with the shape of the linear calculated step response being like curve (*a*) but with different initial and final values. Curves (*a*) and (*d*) can be calculated with any of methods B, C, D, and E described in Sec. 4.5.1.1.

The pull-in process is then approximated by a ramp on the tuning voltage which pushes the output frequency toward its final steady-state value. This ramp acts as a tuning aid; therefore, the PLL with the PFD always locks no matter what the output frequency step is. The infinite

†See the SIMETRIX file PLL_4th_Order_Step_NonLinear_PFD_Approx.sxsch.

pull-in range is the main advantage of using a PFD over a multiplier and most of the other phase detectors. A PLL with a PFD does not need an external acquisition aid. However, application of the VCO pretuning makes the PLL operate closer to lock-in, thus reducing the lock time.

At this point we can complete the comparison table of the mathematical and circuit-based simulation methods. This is done in Table 4.3.

TABLE 4.3 Comparison of the PLL Analysis Methods (update 2)

	MATHCAD	SIMETRIX
Loop filter complexity	Moderate (−) Analytic expression of transfer function is needed.	Very high (+) Simulator can handle very complex circuits.
Calculation of phase margin	Easy (+) By using the equation-solving feature to find the solution of $\|H\text{open}(f_o)\| = 1$ and finding the open-loop phase at f_o.	Relatively easy (−) By placing the cursor on the curve of the open-loop phase curve at the unit gain frequency.
Calculation of closed-loop gain unit BW	Easy (+) By using the equation-solving feature to find the solution of $\|H(f)\| = 1$.	Relatively easy (−) By placing the cursor on the curve of the closed-loop frequency response at the unit gain.
Calculation of closed-loop peak	Easy (−) By using the equation-solving feature to find the solution of $D[\|H(f)\|] = 0$.	Very easy (+) Built in.
Statistical analysis	Possible (−) By manual perform of multiple analyses.	Easy (+) By using Monte Carlo analysis.
Calculation of sampling effects	Easy (+) By writing Eq. (2.10).	(−) On settling time only, with physical models.
Loop components' phase noise modeling	Easy (+) By writing their expressions.	Possible (−) Frequency shaped voltage noise sources have to be synthesized.
Loop filter output noise calculation	Difficult (−) Relatively complicated expressions have to be written even for simple loop filter circuits.	Very easy (+) Automatically computed.
Lock-in transient calculation	Easy, There are 3 methods. FFT is the more general method.	Easy. There are 2 methods. The switching reference is the more flexible method.
Pull-in transient calculation	(−) Provides only an approximate solution of a PLL with a PFD.	(+) Possible in most cases, different methods available.

NOTE: (+) = advantage (more powerful or easier to use).
(−) = disadvantage (less powerful or more difficult to use).

Summarizing, most of the calculations are possible with both the methods.

4.6 Final Note on Circuit-Based Simulation

SPICE transient simulation (here implemented with SIMETRIX) allows for the modeling of other nonlinearities eventually present within the PLL. The operational amplifier nonlinearity is modeled by the SPICE macromodel. The VCO nonlinear tuning characteristic can be modeled with an arbitrary voltage-controlled voltage source inserted between the loop filter output and the VCO tuning input.

References

1. Dean Banerjee, "PLL Performance, Simulation, and Design," *National Semiconductor*, 1998.
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Chapter

5

Miscellaneous

5.1 Introduction

This chapter illustrates some circuits and systems correlated with the PLL. Section 5.2 describes a practical PLL design, which shows the use of modern integrated circuits. The simulation concepts discussed in Chap. 4 have been applied. The results of simulations have been compared with measurements demonstrating the effectiveness of simulations.

Section 5.3 describes the sampling phase detector, a useful circuit for the design of a microwave synthesizer which does not use the high-frequency prescaler. It also discusses some ideas about its application and the related problems.

Section 5.4 describes the multiple-loop architecture which is widely used when high resolution is needed. In this section the analysis of the multiple loop is reduced to the analyses of the single-loop PLL. Thus applicability of the techniques discussed in Chap. 4 is extended to the multiple-loop PLL.

The final section examines the newest synthesizer architecture known as direct digital synthesizer. Using that architecture it is possible to generate signals with high resolution and a fast settling time. This section discusses the working principles and effects of nonideal components. It also includes some basic ideas on the design of the output lowpass filter.

5.2 PLL Performance Verification

Figure 5.1 shows the simplified electrical diagram of a PLL, which uses a VCO, a crystal oscillator, a single chip synthesizer LMX2353, and a passive loop filter. The LMX2353 chip needs only six bypass or DC-block

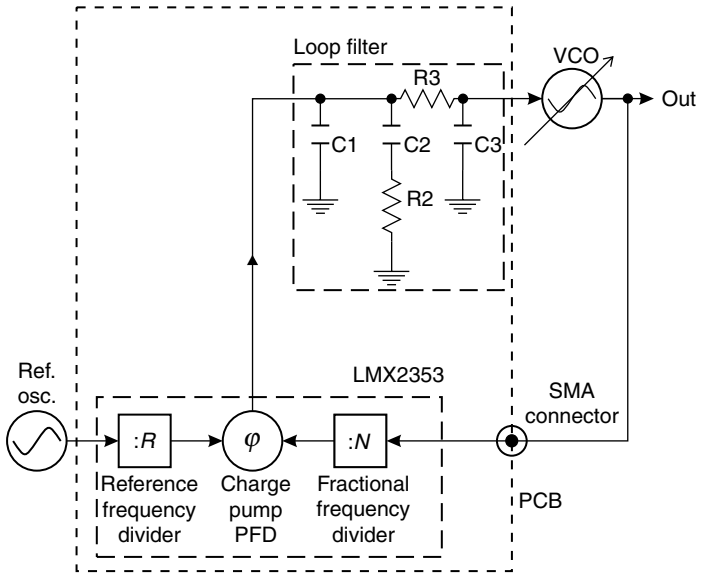


Figure 5.1 Simplified schematic of an experimental PLL.

capacitors. The following description is taken from the LMX2353 data sheet.[†]

> Reference and feedback frequency dividers, and phase frequency detector with charge pump are contained in a single chip LMX2353 manufactured by National Semiconductors.
>
> LMX2353 includes a reference divider with maximum input frequency of 50 MHz and programmable divider ratio from 3 to $2^{15} - 1 = 32767$.
>
> The feedback is a fractional-N with a single 4 bit accumulator. The divider is 19 bits with 15 bits integer divide and 4 bits fractional. The integer part is configured as a 5 bit A counter and a 10 bit M counter. Prescaler ratio can be selected between 16/17 and 32/33. The LMX2353 is capable of operating from 0.5 to 1.2 GHz with the 16/17 prescaler offering a continuous integer divide range from 272 to 16399, and 1.2 to 2.5 GHz with the 32/33 prescaler offering a continuous integer divide range from 1056 to 32767. The fractional part of the divider ratio is programmable in either 1/15 or 1/16 modes. A variable phase delay stage compensates for the accumulated integer phase error, minimizing the charge pump duty cycle, and reducing spurious levels. This technique eliminates the need for compensation current injection into the loop filter. The LMX2353 has a 16 level

[†]Reproduced with permission of National Semiconductor Corporation. The full data sheet is downloadable at *www.national.com*.

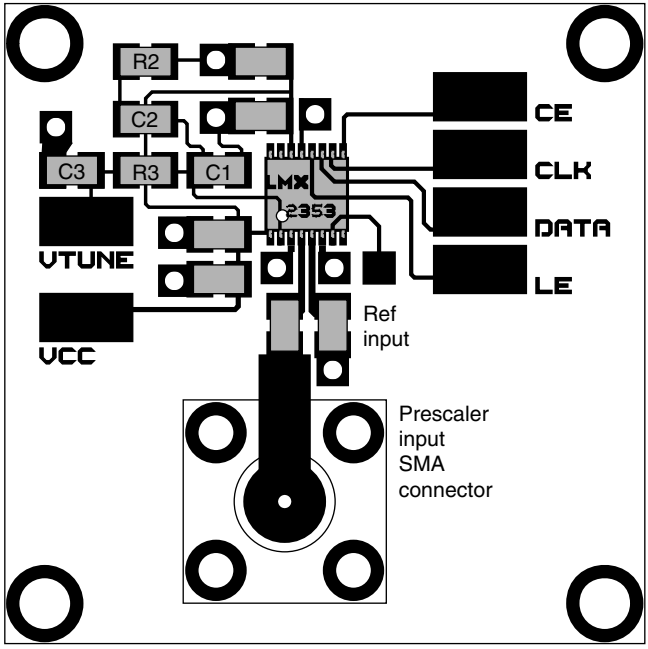


Figure 5.2 Layout of an experimental PLL.

programmable charge pump which supplies output current magnitudes from 100 to 1600 μA.

Reference divider, feedback divider, and charge pump current are programmable writing internal registers. The serial data is transferred into the LMX2353 via a three wire interface (Data, LE, Clock).

National Semiconductor also provides a PC program downloadable at *www.national.com* to drive the IC.

The LMX2353 and related passive components were placed on a printed circuit board 40 $\times$ 40 mm wide. The layout is shown in Fig. 5.2: The loop filter components C_1, C_2, C_3, R_2, and R_3 are placed in the upper left corner of the board. The PLL values are

- External reference frequency: 15.36 MHz
- Reference divider ratio: $4 \Rightarrow f_{\text{ref}} = 15.36/4 = 3.84$ MHz
- Output frequency range: 1098.24 – 1198.08 MHz
- Frequency resolution: $f_{\text{ref}}/16 = 240$ kHz
- VCO modulation sensitivity: 32.2 MHz/V
- Charge pump current: 1.6 mA

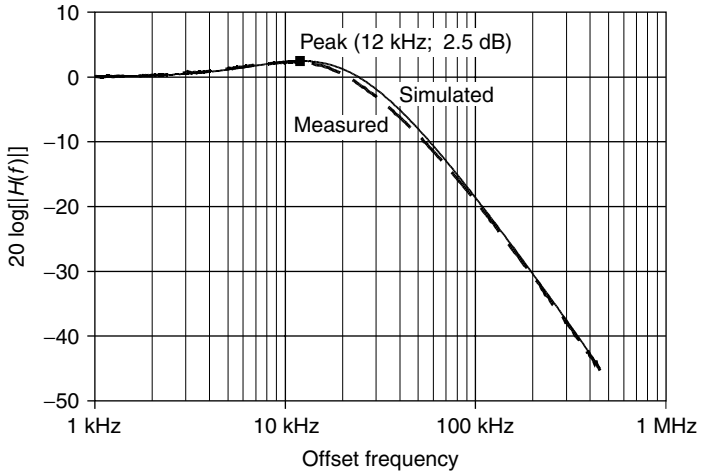


Figure 5.3 Simulated and measured closed-loop magnitude frequency response.

- Loop filter components
  Capacitors: C1 = 2.7 nF, C2 = 27 nF, C3 = 680 pF//30 pF[†]
  Resistors: R2 = 820 Ω, R3 = 270 Ω,
- In-band noise: −85 dBc/Hz flat over offset frequency

The same result can be obtained by reducing the charge pump current and increasing all the impedances of the loop filter by the same factor. The loop filter resistance would be increased, consequently increasing the loop filter noise. The current of the charge pump has to be set at its maximum in order to minimize the loop filter noise.

The PLL can be analyzed[‡] using the methods described in Chap. 4. The following parameters have been calculated:

- Phase margin = 51.6°.
- Closed-loop unit gain bandwidth = 20.4 kHz.
- Closed-loop peak = 2.5 dB at 12.5 kHz.
- Closed-loop frequency response. It is plotted in Fig. 5.3.
- PLL phase noise. It is plotted in Fig. 5.4 together with its terms.[§] Note that the in-band noise crosses the VCO noise at about 5 kHz, while

[†]30 pF is the input capacitance of the VCO tuning port including the connection shielded cable.

[‡]See the MATHCAD file Example1.MCD and the SIMETRIX file Example1.sxsch.

[§]In-band and VCO noise.

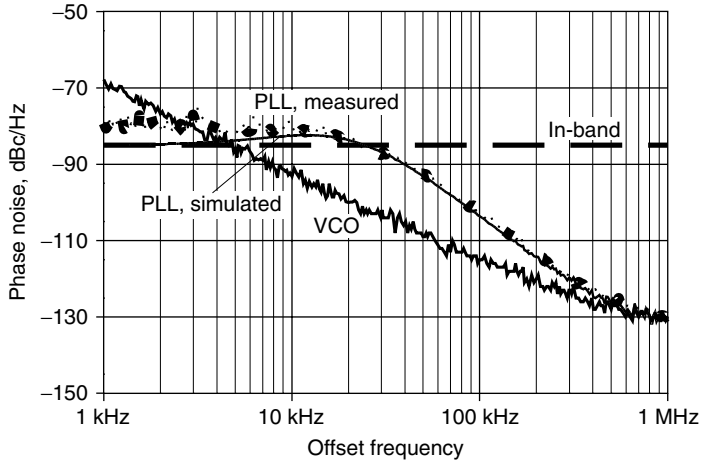


Figure 5.4 Simulated and measured phase noise.

the closed-loop response crosses the phase error response at about 20 kHz. The PLL bandwidth is four times higher than the optimum value for the phase noise described in Sec. 4.3.2. The loop bandwidth was increased in order to reduce settling time.

- Lock-in transient for the output frequency stepping from 1152 to 1156.2 MHz. It is plotted in Fig. 5.5.

The graphs of Figs. 5.3, 5.4, and 5.5 also show the measured curves.

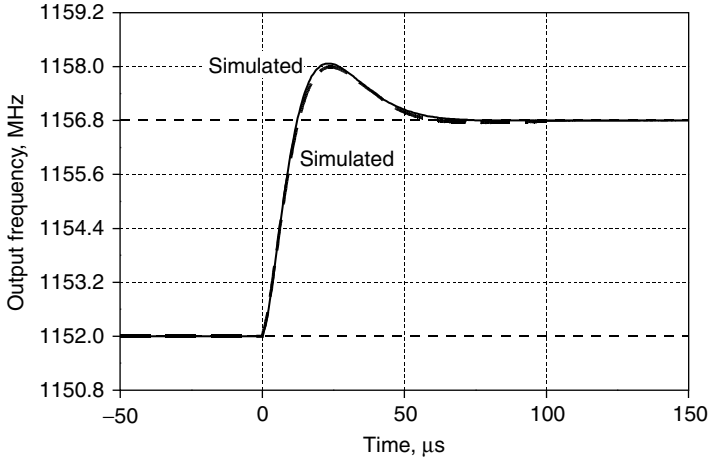


Figure 5.5 Simulated and measured lock-in transient.

The phase noise and the frequency settling curve were measured with the Agilent VCO analyzer 4352S. The test methods and procedure are described in the manual of the instrument.

5.2.1 Measurement of PLL frequency response magnitude

The closed-loop frequency response can be measured by frequency modulation of the reference source and by the measure of the reference and output spectra. The measurement technique is based on the theory of the modulated PLL described in Sec. 4.4. The time-domain expression for the frequency modulated reference source was found in Sec. 4.4:

$$\text{RefOut}(t) = V_r \cos\left[2\pi f_{\text{ref}} t + \frac{K_{vr}}{2\pi f_{mr}} A_r \sin(2\pi f_{mr} t)\right] \tag{5.1}$$

In order to find the spectrum of the frequency modulated wave, Eq. (5.1) can be expanded in series as

$$\text{RefOut}(t) = V_r \sum_{k=-\infty}^{+\infty} J_k\left(\frac{K_{vr} A_r}{2\pi f_{mr}}\right) \cos[2\pi(f_{\text{ref}} + k f_{mr})t] \tag{5.1′}$$

where $J_k(\beta)$ is Bessel's function of the first kind and the kth order of the variable β. For small values of the variable, Bessel's functions can be approximated as

$$J_0(\beta) \cong 1 \qquad -J_{-1}(\beta) = J_1(\beta) \cong \frac{\beta}{2} \qquad J_{-k}(\beta) = J_k(\beta) \cong 0 \qquad \forall k > 1$$

Let's define the modulation index as

$$\beta = \frac{K_{vr} A_r}{2\pi f_{mr}}$$

For small values of the modulation index $\beta = \frac{K_{vr} A_r}{2\pi f_{mr}}$, Eq. (5.1′) can be approximated as

$$\begin{aligned}\text{RefOut}(t) = {} & V_r \cos(2\pi f_{\text{ref}} t) \\ & + V_r \frac{\beta}{2} \cos[2\pi(f_{\text{ref}} + f_{mr})t] - V_r \frac{\beta}{2} \cos[2\pi(f_{\text{ref}} - f_{mr})t]\end{aligned} \tag{5.1″}$$

The general expression (5.1′) of the frequency modulated signal spectrum consists of one carrier at frequency f_{ref} and infinitely extended lower and upper sidebands. Each of them has an infinite number of spectral components. Those components are spaced by integer multiples of

f_{mr}[†] far from the carrier. In the simplified case of a low modulation index, the spectrum has only two side tones $\pm f_{mr}$ far from the carrier. Their relative amplitude is given by

$$\begin{aligned}\text{ReferenceSidebandLevel} &= 20\ \log_{10}\left(\frac{\text{SidebandAmplitude}}{\text{CarrierAmplitude}}\right)\\ &= 20\ \log_{10}\left(\frac{\beta}{2}\right)\quad \text{dBc}\end{aligned} \tag{5.2}$$

As calculated in Sec. 4.4, the modulation index of the PLL output signal is

$$\beta' = \frac{K_{vr}A_r}{2\pi f_{mr}} N\ |H(f_{mr})| = \beta N\ |H(f_{mr})|$$

Hence the sideband level of the PLL output signal is

$$\text{SynthesizerSidebandLevel} = 20\ \log_{10}\left(\frac{\beta'}{2}\right)\quad \text{dBc} \tag{5.3}$$

Subtraction of Eq. (5.2) from (5.3) gives

$$\begin{aligned}&\text{SynthesizerSidebandLevel} - \text{ReferenceSidebandLevel}\\ &\quad = 20\log_{10}[N\cdot|H(f_{mr})|]\quad \text{dB}\end{aligned} \tag{5.4}$$

Now, N is the frequency divider ratio and is known, constant, and does not depend on the modulating frequency f_{mr}. Equation (5.4) states that the difference between the output and the reference sideband level is given by the amplitude of the PLL closed-loop gain. This result can be applied to measure the amplitude of the closed-loop frequency response. The following operations have to be performed:

1. Replace the reference oscillator with one having the same frequency and the frequency modulation (FM) capability. Connect a low-frequency sinusoidal oscillator with the modulation input of the FM oscillator.
2. Set the modulating oscillator frequency at a low value, i.e., about 0.5–1 kHz.
3. Connect a spectrum analyzer with the synthesizer output. Set the center frequency equal to the PLL output frequency ($= N f_{\text{ref}}$) and the span a little bit wider than $6 f_{mr}$. Adjust the modulating signal amplitude to have $\pm f_{mr}$ side tones at the level of about −30 dBc (the remaining side tones should be lower than –65 dBc). Take note of the measured level.

[†] f_{mr} is the modulating frequency.

4. Connect a spectrum analyzer with the FM generator output. Set the center frequency equal to the reference frequency $= f_{\text{ref}}$ and the span a little bit wider than $6f_{mr}$. The level of side tones at $\pm f_{mr}$ should be slightly less than -30 dBc. If so, take note of the measured level; if not, reduce the modulating amplitude and repeat step 3.
5. According to Eq. (5.4) the PLL closed-loop frequency response amplitude at offset frequency f_{mr} is the difference between levels 3 and 4 decreased by $20 \log_{10}(N)$
6. The closed-loop response at frequency f_{mr} is given by

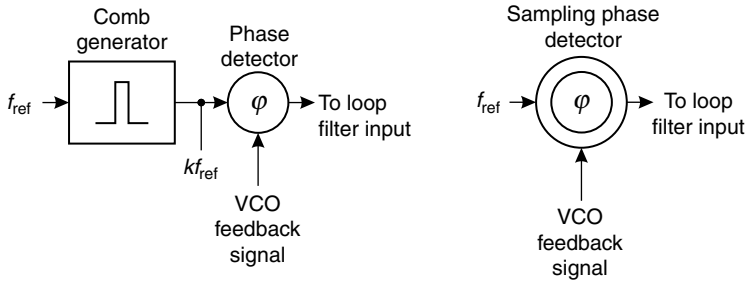
$$\text{dB}[|H(f_{mr})|] = \text{SynthesizerSidebandLevel (step 3)} - \text{ReferenceSidebandLevel (step 4)} - 20 \log_{10}(N)$$

7. Increase the modulating frequency and repeat steps 3 to 6 up to the maximum offset frequency of interest, say up to a frequency response amplitude of about -50 dB.

The measurement of the closed-loop frequency response is not essential since what really matters in a PLL synthesizer is the phase noise and the settling time. Anyway, the measurement of the frequency response can be helpful for debugging or troubleshooting.

5.3 Sampling Phase Detector

The sampling phase detector (SPD) can be used in a PLL to lock a microwave frequency VCO to an integer multiple of a lower frequency (about some hundreds of megahertz) without using a microwave frequency divider. The SPD block diagram is shown in Fig. 5.6*a*. It basically consists of a phase detector (usually a multiplier) whose reference signal is supplied by a pulse generator rather than a sinusoidal one for standard multiplier phase detectors. The symbol of the SPD is shown in Fig. 5.6*b*.



(*a*) Functional diagram (*b*) Symbol

Figure 5.6 Sampling phase detector.

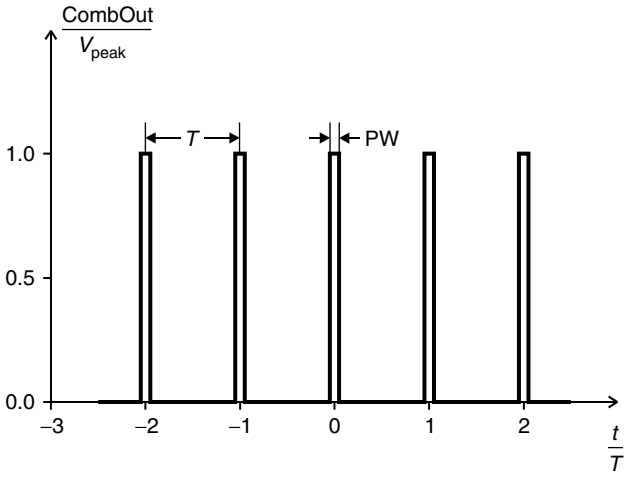


Figure 5.7 Pulse generator output waveform.

The pulse generator output signal is a rectangular wave with period T, pulse width PW, and amplitude V_{peak}. That signal can be written as a sum of unit rectangular pulses defined a little bit differently† from that in Sec. 1.3.3.

$$\text{RectangularPulse}_{\Delta T}(t) = \begin{cases} 1 & |t| < \frac{\Delta T}{2} \\ 0 & \text{elsewhere} \end{cases}$$

$$\text{CombOut}(t) = \sum_{n=-\infty}^{+\infty} \text{RectangularPulse}_{\Delta T}(t - nT) \tag{5.5}$$

The pulse generator output waveform is plotted in Fig. 5.7 where time is normalized to the period, and amplitude is normalized to V_{peak}.

The pulse generator output signal can be expanded in Fourier series as

$$\text{CombOut}(t) = V_{\text{peak}} \frac{\text{PW}}{T} + V_{\text{peak}} \frac{2}{\pi} \sum_{k=1}^{\infty} \frac{\sin\left(k\pi \frac{\text{PW}}{T}\right)}{k} \cos\left(2\pi k \frac{t}{T}\right) \tag{5.6}$$

†The rectangular pulse as defined in this chapter is translated in time and has unit amplitude. Thus the comb output signal Fourier series is simplified by having only cosine terms, and the waveform amplitude is controlled by a multiplying factor V_{peak}.

The first term of Eq. (5.6) is a DC voltage that is eliminated by the output capacitor and will not be considered. Equation (5.6) can be replaced by Eq. (5.6′) where the DC component is removed.

$$\text{CombOut}(t) = V_{\text{peak}} \frac{2}{\pi} \sum_{k=1}^{\infty} \frac{\sin\left(k\pi \frac{\text{PW}}{T}\right)}{k} \cos\left(2\pi k \frac{t}{T}\right) \tag{5.6′}$$

The pulse generator output signal is a "comb" (that is why it is called a *comb generator*) of harmonics of its fundamental frequency $1/T$. The amplitude of the kth harmonic is given by

$$\text{Harmonic}_k = V_{\text{peak}} \frac{2}{\pi} \frac{\sin\left(k\pi \frac{\text{PW}}{T}\right)}{k} \tag{5.6″}$$

The harmonic level envelope is shaped as $\sin(x)/x$. The level of the fundamental frequency is found by setting $k = 1$ in the expression (5.6″). The harmonic level normalized to the fundamental versus the harmonic order is plotted in Fig. 5.8. Let's define $K_{3\text{dB}}$ as the index of the harmonic whose power is half of that of the fundamental. The $K_{3\text{dB}}$th harmonic is 3 dB below the fundamental if

$$\frac{\sin\left(K_{3\text{dB}}\pi \frac{\text{PW}}{T}\right)}{K_{3\text{dB}}} = \frac{1}{\sqrt{2}} \sin\left(\pi \frac{\text{PW}}{T}\right)$$

$K_{3\text{dB}}$ can be found by solving the above-written transcendental equation once PW and T are known.

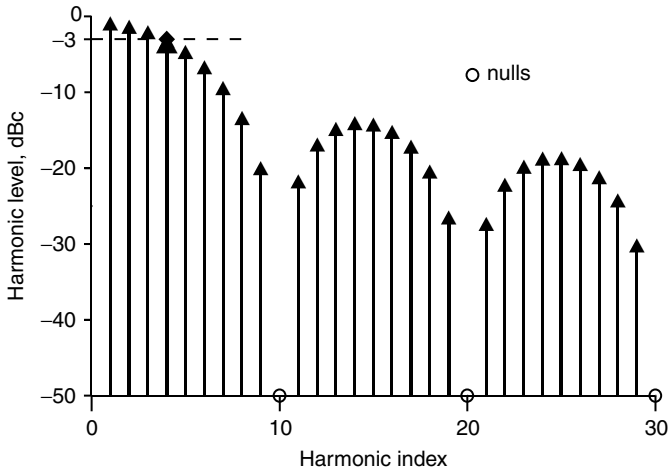


Figure 5.8 Comb generator output spectrum.

The comb generator output spectrum presents nulls at indices k_z given by

$$\text{Harmonic}_k = 0 \Rightarrow \frac{\sin\left(k_z \pi \frac{\text{PW}}{T}\right)}{kz} = 0 \Rightarrow k_z \pi \frac{\text{PW}}{T} = m\pi \Rightarrow \underline{\underline{k_z = m\frac{T}{PW}}}$$

where m is an arbitrary integer number. The first null occurs at $k_z = T/\text{PW}$. It follows that the smaller the duty cycle PW/T, the wider the output spectrum. Figure 5.8 also shows the position of the first three nulls and the -3 dB harmonic.

The rectangular waveform is generated from a sinusoidal input by a step recovery diode. The input frequency $1/T$ is on the order of hundreds of megahertz, and the input power is around half a watt. Comb generators usually incorporate output matching and equalizing networks which flatten the output spectrum. The output spectra have significant energy up to about 20 GHz with total conversion efficiency of some percents. Here are some typical numbers:

- Input frequency: $1/T = 1$ GHz
- Input power: $P_{\text{in}} = 100$ mW
- Efficiency: $\eta = 2\%$
- Total output power: $P_o = \eta P_{\text{in}} = 2$ mW
- Maximum output frequency: $F_{\max} = 20$ GHz
- Number of output spectral components: $N_{\text{harm}} = F_{\max} T = 20$
- Level of each[†] harmonic component: $L_{\text{harm}} = P_o / N_{\text{harm}} = 0.1$ mW

Now, assuming that the output pulses are very short and that the multiplier in Fig. 5.6*a* is ideal, the output of the SPD is the VCO signal sampled at the sampling frequency $f_{\text{ref}} = 1/T$. This is how the name *sampling phase detector* came to be.

Figure 5.9 shows a PLL with a PFD. Let us assume that the VCO frequency is close to one of the harmonics of the reference frequency. We will denote the index of that harmonic as K^*. Let the VCO and the comb generator output signals respectively be

$$\text{VCO}_{\text{out}}(t) = V_{\text{VCO}} \cos(2\pi f_{\text{VCO}} t)$$

$$\text{Comb}_{\text{out}}(t) = \sum_{\substack{k=1 \\ k \neq K^*}}^{\infty} a_k \cos(2\pi k f_{\text{ref}} t) + a_{K^*} \cos(2\pi K^* f_{\text{ref}} t)$$

[†]In this simple calculation a flat spectrum is assumed up to 20 GHz. In a real case the spectrum amplitude is decreasing at higher frequencies.

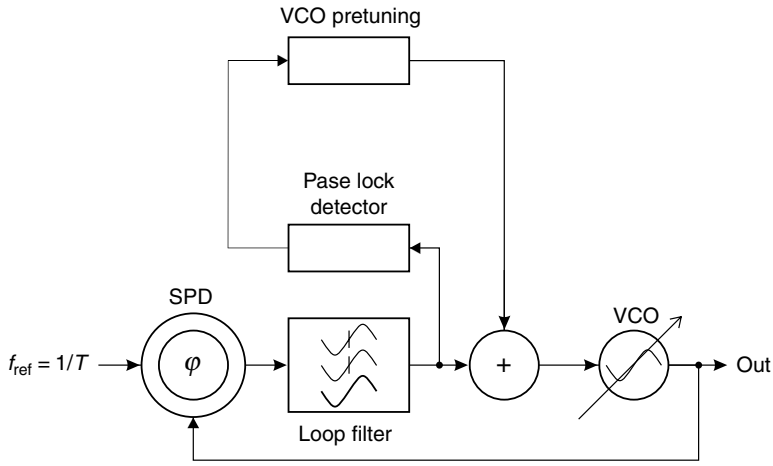


Figure 5.9 SPLL basic schematic.

The SPD output is the product of these two signals:

$$\mathrm{SPD}_{\mathrm{out}}(t) = V_{\mathrm{VCO}} \cos(2\pi f_{\mathrm{VCO}} t) \sum_{\substack{k=1 \\ k \neq K^*}}^{\infty} a_k \cos(2\pi k f_{\mathrm{ref}} t) + V_{\mathrm{VCO}} \cos(2\pi f_{\mathrm{VCO}} t) a_{K^*} \cos(2\pi K^* f_{\mathrm{ref}} t) \qquad (5.7)$$

The SPD output signal, given by Eq. (5.7), is the sum of infinite sinusoidal signals. Each sinusoidal signal has a frequency that is the sum or the difference between the VCO frequency and one of the harmonics of the reference frequency. Equation (5.7) can be expanded as

$$\mathrm{SPD}_{\mathrm{out}}(t) = \sum_{k=1}^{\infty} \frac{V_{\mathrm{VCO}} a_k}{2} \cos[2\pi(f_{\mathrm{VCO}} + k f_{\mathrm{ref}}) t] + \sum_{\substack{k=1 \\ k \neq K^*}}^{\infty} \frac{V_{\mathrm{VCO}} a_k}{2} \cos[2\pi(f_{\mathrm{VCO}} - k f_{\mathrm{ref}}) t] + \frac{V_{\mathrm{VCO}} a_{K^*}}{2} \cos[2\pi(f_{\mathrm{VCO}} - K^* f_{\mathrm{ref}}) t] \qquad (5.7')$$

Equation (5.7′) has three terms. The first one has spectral components whose frequency is the sum of the VCO and the reference harmonics. The second term has spectral components whose frequency is the difference between the VCO one and the reference harmonics far from it. The smallest of these frequencies is comparable with the reference one; the remaining frequencies are higher. Therefore, all the above-mentioned mixing products have frequencies close to and higher than that of the

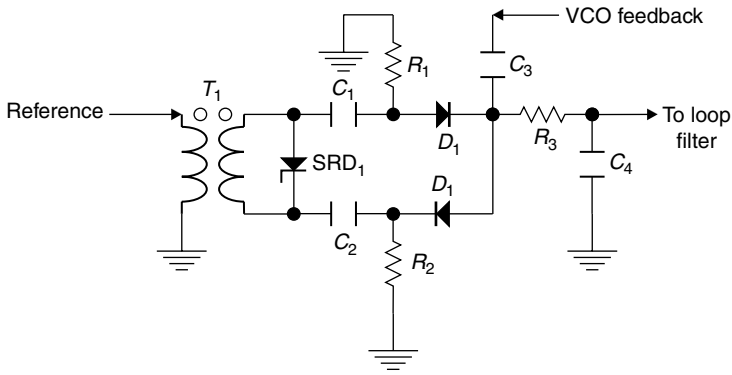


Figure 5.10 Integrated SPD.

VCO and are thus filtered out by the PLL. The only useful signal for the PLL is the third term of Eq. (5.7′):

$$\mathrm{SPD}'_{\mathrm{out}}(t) = \frac{V_{\mathrm{VCO}} a_{K^*}}{2} \cos[2\pi(K^* f_{\mathrm{ref}} - f_{\mathrm{VCO}})\, t] \qquad (5.7'')$$

Thus if the difference between the VCO frequency and the closest reference harmonic is smaller than the pull-in range, the PLL will lock the VCO to that harmonic. The PLL using the SPD is also known as a sampled phase-locked loop (SPLL). Its basic schematic is shown in Fig. 5.9.

The circuit in Fig. 5.9 includes a VCO pretuning circuit. It has to set the VCO output frequency close to the required reference harmonic. Driving the pretuning circuit allows the VCO to be locked on the different harmonics of the reference signal. However, if the VCO frequency excursion covers more than one harmonic and the pretuning is not sufficiently accurate, there is the risk of a false lock; i.e., the PLL locks the wrong harmonic. The circuit in Fig. 5.9 is commonly used with a voltage-controlled dielectric resonator oscillator (VCDRO). These oscillators use a high Q dielectric resonator with a varactor somehow coupled to it. The output frequency excursion is of a few megahertz and false lock is avoided. The pretuning circuit is a slow ramp generator, disabled when the phase lock is detected.

However, the phase detector gain of the mixer changes over frequency and depends on the amplitude of the used harmonic and on the amplitude of the VCO signal (which depends on the output frequency). Hence, one SPLL, generating more than one output frequency,[†] will have a different phase detector gain at a different output frequency and consequently a different bandwidth and settling time.

The comb generator and phase detector can be integrated into a single component as shown in Fig. 5.10. The comb generator has balanced

[†]Locking to different reference harmonics.

output and consists of transformer T_1, step recovery diode SRD_1, and coupling capacitors C_1 and C_2. The phase detector is a single balanced mixer using diodes D_1 and D_2, resistors R_1 and R_2 for DC return, capacitors C_3 and C_4 and resistor R_3 for VCO and output signal decoupling.

5.4 Multiple-Loop PLL

The single-loop microwave PLL has to use one high-frequency prescaler as the first stage of the frequency divider. These prescalers have a fixed module and have to divide the VCO frequency down to a value below 2 GHz. The most common fixed microwave divider ratios are 4 and 8. The frequency resolution of such a PLL is the reference frequency multiplied by the fixed divider ratio. The reference frequency has to be decreased by that factor in order to save the resolution. This implies the reduction of the maximum closed loop and the increase of in-band noise[†] by the same factor. The narrowband PLL also has a limited VCO phase noise reduction. Fractional-N[‡] is an architecture that allows for a small frequency resolution combined with a relatively high-reference frequency. Another possible architecture is the dual-loop synthesizer whose block diagram is shown in Fig. 5.11. It consists of two loops: the internal loop with the components inside the rectangle marked as PLL_2 (phase detector PD_2, loop filter LF_2, VCO_2, and frequency divider FD_2), and the external loop with the components PD_1, LF_1, VCO_1, MIXER, IF filter, and FD_1.

The external loop is a standard single-loop PLL with a reference frequency f_{ref2} and a frequency division N_2; its output frequency is $\text{FPLL}_2 = N_2 f_{\text{ref2}}$. FPLL_2 is below 2 GHz; thus the frequency divider ND_2 has no fixed prescaler and the frequency resolution is f_{ref2}. The signals at the RF and LO inputs of the mixer have frequencies of F_{out} and FPLL_2, respectively. The output IF signal has two sinusoidal components, one having a frequency of $F_{\text{out}} + \text{FPLL}_2$, and the other having a frequency of $F_{\text{out}} - \text{FPLL}_2$. The sum product is high frequency and is filtered out from the IF filter together with the mixer spurs and leakage.[§] The difference signal feeds the input of the frequency divider ND_1 whose output frequency is $(F_{\text{out}} - \text{FPLL}_2)/N_1$. The phase detector PD_1 compares the phases of the ND_1 output signal with that of the

[†]Equation (4.7′) states that the in-band noise is proportional to the frequency division factor-N

$$\left|\text{InBand}(f)\right|^2 = N^2 \left\lfloor |\Theta_r(f)|^2 + |n_{\text{DET}}(f)|^2 K_d^{-2} + |n_{\text{DIV}}(f)|^2 \right\rfloor$$

[‡]See Chap. 3.

[§]Having frequency $\pm m f_{RF} \pm n f_{lo}$ with $n, m = 0, 1, 2, \ldots$.

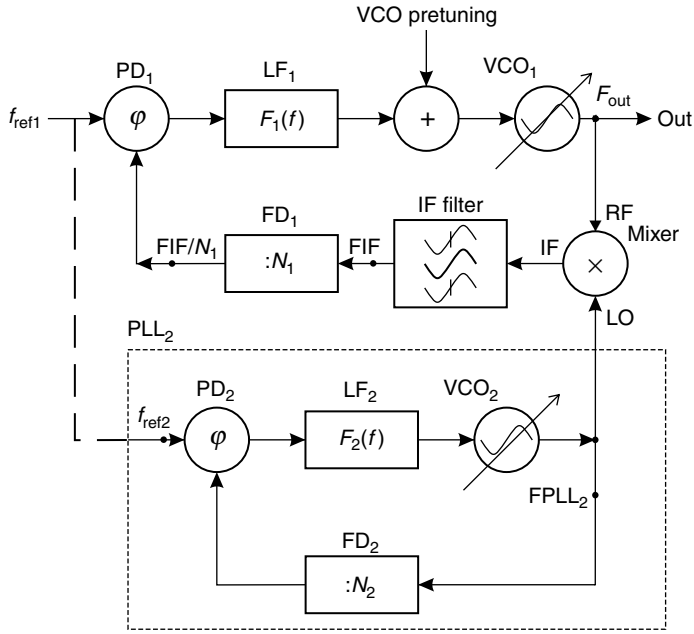


Figure 5.11 Dual-loop PLL synthesizer.

reference signal. If the PLL is stable, it will lock and the two phases will be equal. Consequently the two corresponding frequencies will be equal as well:

$$f_{\text{ref}1} = \frac{F_{\text{out}} - N_2 f_{\text{ref}2}}{N_1} \tag{5.8}$$

The output frequency is then

$$F_{\text{out}} = N_1 f_{\text{ref}1} + N_2 f_{\text{ref}2} \tag{5.8′}$$

We assumed that VCO_1 is a microwave oscillator and the VCO_2 output frequency is below 2 GHz. Therefore, the IF frequency $F_{\text{out}} - \text{FPLL}_2$ is still within the microwave range. Consequently the first stage of the frequency divider is a fixed microwave prescaler and the frequency division factor N_1 is the product of one fixed factor by one variable factor:

$$N_1 = N_{1,\text{fixed}} \cdot N_{1,\text{variable}}$$

Equation (5.8′) can be written as

$$F_{\text{out}} = N_{1,\text{fixed}} \cdot N_{1,\text{variable}} f_{\text{ref}1} + N_2 \cdot f_{\text{ref}2} \tag{5.8″}$$

From Eq. (5.8″) it follows that

- Unitary increasing (decreasing) of $N_{1,\text{variable}}$ implies F_{out} is decreasing (increasing) by $N_{1,\text{fixed}} \cdot f_{\text{ref}1}$.
- Unitary increasing (decreasing) of N_2 implies F_{out} is decreasing (increasing) by $f_{\text{ref}1}$.

The PLL_2 output frequency range has to be equal to a variation of F_{out} when $N_{1,\text{variable}}$ is increased by 1. Thus;

$$\text{FPLL}_{2,\max} - \text{FPLL}_{2,\min} = N_{1,\text{fixed}} f_{\text{ref}1} \Rightarrow N_{2,\max} - N_{2,\min} = N_{1,\text{fixed}} \frac{f_{\text{ref}1}}{f_{\text{ref}2}}$$

If the initial frequency of VCO_1 is very far from its steady-state value [given by Eq. (5.8′)], the frequency of the IF signal may be out of the IF filter passband. In that case no signal will clock the frequency divider FD_1, and the external PLL will not lock regardless of its pull-in range. Thus, a pretuning circuit is needed with sufficient precision to avoid that risk.

5.4.1 Phase noise of multiple-loop PLL

The phase noise of PLL_2 is given by Eq. (4.7′) and can be calculated with any of the methods described in Sec. 4.3.

$$\left|\Theta_o 2(f)\right|^2 = N_2^2 \left[|\Theta_{r2}(f)|^2 + \frac{|n_{\text{DET2}}(f)|^2}{K_{d2}^2} + |n_{\text{DIV2}}(f)|^2 \right] |H_2(f)|^2 + [1 - H_2(f)]^2 \left|n_{\text{VCO}_2}(f)\right|^2$$

where index 2 denotes values of PLL_2, whose frequency response is given by

$$H_2(f) = \frac{\frac{K_{d2}K_{v2}}{N_2} \frac{F_2(f)}{j2\pi f}}{1 + \frac{K_{d2}K_{v2}}{N_2} \frac{F_2(f)}{j2\pi f}}$$

The output phase noise of PLL_2 is a component of the in-band noise of the external loop:

$$|\Theta_o(f)|^2 = \left\{ N_1^2 \left[|\Theta_{r1}(f)|^2 + \frac{|n_{\text{DET1}}(f)|^2}{K_{d1}^2} + |n_{\text{DIV2}}(f)|^2 \right] + |\Theta_{o2}(f)|^2 \right\} |H_1(f)|^2 + [1 - H_1(f)]^2 |n_{\text{VCO1}}(f)|^2 \quad (5.9)$$

where index 1 denotes values of the external loop with the frequency response given by

$$H_1(f) = \frac{\frac{K_{d1}K_{v1}}{N_1}\frac{F_1(f)}{j2\pi f}}{1 + \frac{K_{d1}K_{v1}}{N_1}\frac{F_1(f)}{j2\pi f}}$$

The phase noise of VCO_1, $n_{VCO1}(f)$, includes degradation due to noise injection from the pretuning network. The methods of phase noise analysis described in Sec. 4.3 can easily be applied to calculate the phase noise of the dual-loop PLL given by Eq. (5.9).

For small values of offset frequency, it can be assumed that

$$|H_1(f)|^2 \cong |H_2(f)|^2 \cong 1 \Rightarrow \left|1 - H_1(f)\right|^2 \cong \left|1 - H_2(f)\right|^2 \cong 0$$

Close-to-carrier phase noise is then given by Eq. (5.9) where the closed-loop response is replaced by 1 and the error response by 0:

$$|\Theta_o(f)|^2_{\text{Close-In}} = N_1^2\left[|\Theta_{r1}(f)|^2 + \frac{|n_{\text{DET1}}(f)|^2}{K_{d1}^2} + |n_{\text{DIV2}}(f)|^2\right] + N_2^2\left[|\Theta_{r2}(f)|^2 + \frac{|n_{\text{DET2}}(f)|^2}{K_{d2}^2} + |n_{\text{DIV2}}(f)|^2\right] \tag{5.10}$$

In the simplified case of noiseless phase detectors and frequency dividers, the close-to-carrier phase noise becomes

$$|\Theta_o(f)|^2_{\text{Close-In}} = N_1^2\,|\Theta_{r1}(f)|^2 + N_2^2\,|\Theta_{r2}(f)|^2 \tag{5.10′}$$

Very often reference signals of the internal and external loops are generated by the same reference source with two frequency dividers:

$$f_{\text{ref}1} = \frac{1}{R_1} f_{\text{ref}} \qquad f_{\text{ref}2} = \frac{1}{R_2} f_{\text{ref}}$$

If two reference dividers are noiseless, it follows that

$$\Theta_{r1}(f) = \frac{\Theta_r(f)}{R_1} \qquad \Theta_{r2}(f) = \frac{\Theta_r(f)}{R_2}$$

which means that the two reference signals are coherent and their contributions are summed as voltage rather than as power like in Eq. (5.10′). Close-to-carrier noise becomes

$$|\Theta_o(f)|^2_{\text{Close-In}} = |N_1\Theta_{r1}(f) + N_2\Theta_{r2}(f)|^2 = \left(\frac{N_1}{R_1} + \frac{N_2}{R_2}\right)^2 |\Theta_r(f)|^2 \tag{5.11}$$

Assuming the two reference signals come from the same signal, the output frequency given by Eq. (5.8′) becomes

$$F_{\text{out}} = \left(\frac{N_1}{R_1} + \frac{N_2}{R_2}\right) f_{\text{ref}} \tag{5.12}$$

Comparing Eq. (5.11) with (5.12), it can be seen that the close-to-carrier phase noise of the dual-loop synthesizer is the same as that of a single-loop synthesizer with the same reference signal and output frequency. Leeson's Eq. (2.31) states that close-to-carrier noise of the reference oscillator is proportional to $f_{\text{ref}}/(Q_L f^2)$ where Q_L is the resonator's loaded Q and f is the offset frequency. Substituting reference close-to-carrier noise given by Leeson's equation into Eq. (5.11), we obtain

$$|\Theta_o(f)|^2_{\text{Close-In}} = \left(\frac{N_1}{R_1} + \frac{N_2}{R_2}\right)^2 \left(\frac{f_{\text{ref}}}{2Q_L f^2}\right)^2 \left(\frac{f_c}{f}\right) \frac{NFKT}{2P_s}$$

From Eq. (5.11),

$$\left(\frac{N_1}{R_1} + \frac{N_2}{R_2}\right)^2 = \left(\frac{F_{\text{out}}}{f_{\text{ref}}}\right)^2$$

Then,

$$|\Theta_o(f)|^2_{\text{Close-In}} = \left(\frac{F_{\text{out}}}{2Q_L f^2}\right)^2 \left(\frac{f_c}{f}\right) \frac{NFKT}{2P_s} \tag{5.13}$$

The close-to-carrier phase noise of any PLL with a single or double-loop depends only on the output frequency and on the parameters of the reference oscillator: loaded Q of the resonator, noise figure and flicker noise of the active device, and power on the resonator. Double-loop architecture can be generalized to multiple loop: if PLL_2 itself is a double-loop PLL, a triple-loop synthesizer is obtained, and so on. In any case Eq. (5.13) remains valid.

5.4.2 Transients in Multiple-Loop PLL

The synthesizer of Fig. 5.11 has three possible transients on the output frequency. The first is excited by changing the divider ratio of the external loop, the second by changing the divider ratio of the internal loop, and the third by variations of the pretuning voltage. As shown in Sec. 4.5, the first two transients can be calculated in response to steps in the reference angular frequency. Changes in pretuning voltage are ideally simultaneous with changes in FD_1. In this chapter linear transient analysis will be described based on the equivalent block diagram of the dual-loop PLL of Fig. 5.11. That block diagram is shown in Fig. 5.12. The observed magnitude is the angular frequency like in Fig. 1.2*b*.

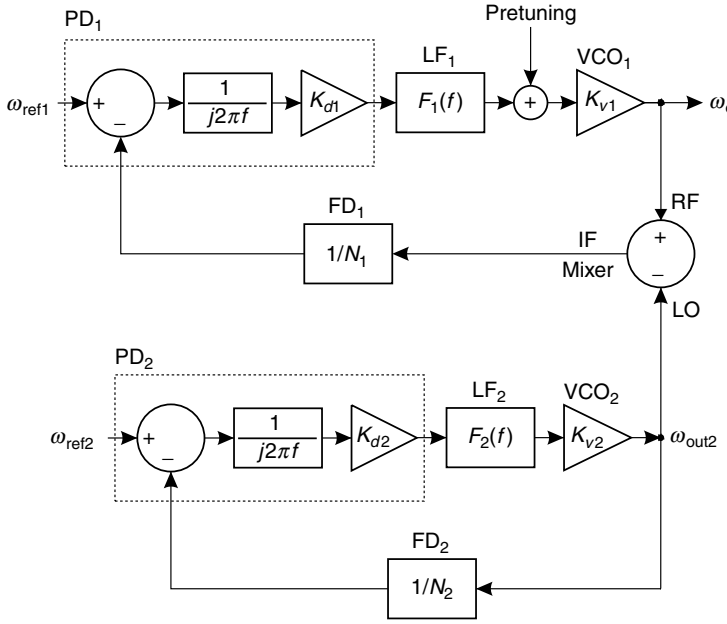


Figure 5.12 Block diagram of dual-loop PLL synthesizer.

The mixer is the only new block; it is modeled with a subtractor since the mixer IF output frequency is the difference between the RF and LO input frequencies, and the IF angular frequency is the difference between the RF and LO angular frequencies as well.

Linear calculations of frequency settling transients consist of calculations of some frequency responses. The inputs are the two reference frequencies of the two phase detectors and the pretuning input. The outputs are the synthesizer output, phase errors on two phase detectors (for validation of linear analysis), and the mixer output (to check if the IF filter passband limits are exceeded during the transient). All these frequency responses are calculated with Mason's rule.

5.4.2.1 Step on the angular frequency of the external-loop reference. Suppose we want to apply a step of amplitude $\Delta\omega_2$ on the reference angular frequency. The variation on the PLL_2 output angular frequency will be

$$\Delta\omega_{\text{out2,2}}(t) = \mathscr{F}^{-1}\left[N_2 H_2(f)\frac{\Delta\omega_2}{j2\pi f}\right] \tag{5.14}$$

The phase error on PD_2 is

$$\Delta\theta_{2,2}(t) = \mathscr{F}^{-1}\left[\frac{1-H_2(f)}{j2\pi f}\frac{\Delta\omega_2}{j2\pi f}\right] \tag{5.15}$$

The variation on the synthesizer output angular frequency is

$$\Delta\omega_{\text{out1,2}}(t) = \mathscr{F}^{-1}\left[N_2 \cdot H_2(j2\pi f)H_1(j2\pi f)\frac{\Delta\omega_2}{j2\pi f}\right] \tag{5.16}$$

The phase error on phase detector PD_1 is

$$\Delta\theta_{1,2}(t) = \mathscr{F}^{-1}\left[N_2 \cdot H_2(j2\pi f)\frac{1}{N_1}\frac{1 - H_1(j2\pi f)}{j2\pi f}\frac{\Delta\omega_2}{j2\pi f}\right] \tag{5.17}$$

The inverse Fourier transforms (5.15) to (5.17) can be calculated with any of the methods described in Sec. 4.5. The transient on the output frequency can be calculated together with the phase error on two phase detectors. It is possible to check whether or not the linear limits have been exceeded.

5.4.2.2 Step on the angular frequency of the internal-loop reference. Suppose we want to apply a step of amplitude $\Delta\omega_1$ on an angular frequency of $\theta_{ref\,1}$. PLL_2 is not affected by any variation of the external loop. The variation on the synthesizer output angular frequency is

$$\Delta\omega_{\text{out1,1}}(t) = \mathscr{F}^{-1}\left[N_1 \cdot H_1(j2\pi f)\frac{\Delta\omega_1}{j2\pi f}\right] \tag{5.18}$$

The phase error on phase detector PD_1 is

$$\Delta\theta_{1,1}(t) = \mathscr{F}^{-1}\left[\frac{1 - H_1(j2\pi f)}{j2\pi f}\frac{\Delta\omega_1}{j2\pi f}\right] \tag{5.19}$$

Equations (5.18) and (5.19) are the same as those for the single loop. The methods of Sec. 4.5 can be applied as they are, including the check of the phase detector linear operation.

5.4.2.3 Step on the pretuning voltage. Suppose we want to apply a step of amplitude ΔV_1 on a pretuning voltage of the external loop. Again, this perturbation doesn't affect PLL_2. The variation on the synthesizer output angular frequency is

$$\Delta\omega_{\text{out1,3}}(t) = \mathscr{F}^{-1}\left\{K_{v1}[1 - H_1(j2\pi f)]\frac{\Delta V_1}{j2\pi f}\right\} \tag{5.20}$$

The phase error on phase detector PD_1 is

$$\Delta\theta_{1,3}(t) = \mathscr{F}^{-1}\left[-\frac{K_{v1}}{N_1}\frac{1 - H_1(j2\pi f)}{j2\pi f}\frac{\Delta V_1}{j2\pi f}\right] \tag{5.21}$$

Equations (5.20) and (5.21) are similar to Eqs. (5.18) and (5.19). There are two differences: There is a different multiplying constant and the

closed-loop response is replaced by the phase error frequency response. The methods of Sec. 4.5 can be applied with minor changes.

5.4.2.4 Simultaneous application of different excitations. Different excitations can be applied simultaneously. Their effect can be calculated by superimposition of effects since the system is linear. One particularly interesting combination is one step on the eternal loop reference frequency and one step on the pretuning voltage. Summing Eq. (5.18) with (5.20) gives

$$\Delta\omega_{\text{out1,1}} + 3(t) = \mathscr{F}^{-1}\left\{\frac{H_1(j2\pi f)N_1\Delta\omega_1 + [1 - H_1(j2\pi f)]K_{v1}\,\Delta V_1}{j2\pi f}\right\} \tag{5.22}$$

if $\Delta V_1 = \frac{N_1}{K_{v1}}\Delta\omega_1$ Eq. (5.22) becomes

$$\Delta\omega_{\text{out1,1}} + 3(t) = \mathscr{F}^{-1}\left\{\frac{N_1\Delta\omega}{j2\pi f}\right\} = N_1\Delta\omega\,\eta(t) \tag{5.22'}$$

which is an ideal step. This result was also found in Sec. 4.4.3 where it was demonstrated that a perfectly balanced dual-point modulated PLL ideally has an infinite modulation bandwidth. Note that synchronous and balanced variations on the reference (modeling variations on the frequency divider) and on pretuning are exactly a perfectly balanced dual-point modulated PLL. Under the same condition, the phase error given by the sum of Eqs. (5.19) and (5.21) becomes zero.

5.4.3 Variations on Double-Loop Architecture

Many variations on the theme of the multiple-loop synthesizer are possible. Some of them will be described in this section.

1. PLL_2 of Fig. 5.11 can be replaced by one high-frequency PLL (sometimes an SPLL) with an output frequency close to that of VCO_1. This way the IF frequency becomes quite lower than the output frequency and the high-frequency fixed prescaler is no longer needed in the frequency divider FD_1. This configuration is still given by Eq. (5.8′), but N_1 can be changed with the unit step. Thus the output frequency resolution becomes the smaller of f_{ref1} and f_{ref2}. If PLL_2 is an SPLL, f_{ref2} is the input frequency of the comb generator, and N_2 is the index of the locked harmonic.
2. The same result of case 1 can be obtained by swapping the comb generator between the reference input and the VCO output of PLL_2. In this case the PLL_2 output (frequency around some hundreds of

megahertz) feeds the comb generator input whose output is the LO signal of the mixer. The combination of comb generator and mixer is analogous to the SPD described in Sec. 5.3 and is also known as the harmonic mixer or sampling mixer. The only difference is that the SPD output is a baseband signal, while the harmonic mixer IF output is an RF signal. The harmonic mixer generates many mixing products, but only one will fall within the passband of the IF filter. The external loop will lock that mixing product, making its frequency equal to $N_1 \cdot f_{\text{ref}1}$. The output frequency is given by Eq. (5.8′) where $f_{\text{ref}2}$ is the PLL_2 output frequency and N_2 is such that the result of Eq. (5.8′) is closest to the VCO_1 pretuned frequency. A configuration with a harmonic mixer eliminates the risk of false lock on PLL_2 but moves that risk to the external loop, making pretuning accuracy more critical.

3. PLL_2 can be replaced by a DDS generator.† In this case very high resolution is achieved because the DDS resolution is on the order of 1 Hz.

All considerations on phase noise and the settling time of the dual-loop PLL made in Secs. 5.4.1 and 5.4.2 are still applicable with the following changes for the above-mentioned cases.

The PLL_2 output frequency in case 1 and the N_2th harmonic in case 2 are close to the output frequency. The system can work with the PLL_2 frequency lower or higher than that of VCO_1. In the latter condition, the IF output frequency will decrease if the VCO_1 frequency increases. From an external loop point of view, a block from the VCO_1 tuning port to the mixer IF port behaves like a VCO with a negative gain: i.e., increasing the on tuning voltage decreases the output frequency. A 180° phase shift is added to the loop gain making it unstable. An additional phase shift can be removed by inverting the output characteristic of the loop filter or of the phase detector. The latter solution is easily implemented with PFD by the swapping f_v and f_r inputs.‡ In case 3, calculations on PLL_2 need to be replaced by calculations on DDS (see Sec. 5.5).

5.5 Direct Digital Synthesizer

A direct digital synthesizer (DDS) is a full digital architecture synthesizer characterized by high tuning speed and high frequency resolution. The DDS basic block diagram is shown in Fig. 5.13. The DDS includes four basic blocks: one accumulator, one read-only memory (ROM)

†See Sec. 5.5.

‡As an example, the phase detector polarity of LMX2353 (LMX2353 is used in Sec. 5.2), has a polarity that can be programmed via the three-wire interface.

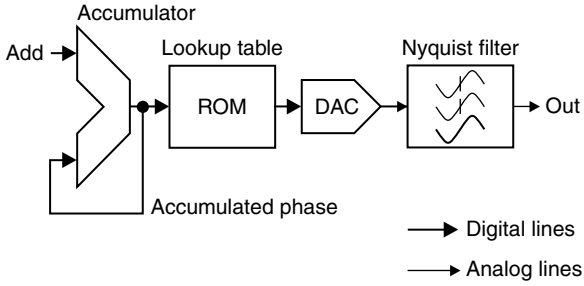


Figure 5.13 DDS basic diagram.

implementing a lookup table, one digital-to-analog converter (DAC), and one lowpass filter.

5.5.1 Principle of DDS operation

Operation of the accumulator was already described in Sec. 3.2. The accumulator is clocked by a reference frequency that can be considered as the sampling frequency of the system. Denote the size of the accumulator with Q, the input addendum with A, the output with $\mathrm{DDS}_{\mathrm{out}}$, and the accumulator clock frequency with f_{CLK}. At each clock cycle the accumulator output is increased by A until overflow is reached. Assuming $\mathrm{DDS}_{\mathrm{out}} = 0$ as the initial condition, it is

$$\mathrm{DDS}_{\mathrm{out},_k} = (kA) \mod Q \tag{5.23}$$

where index k indicates the kth clock cycle.

Equation (5.23) can be interpreted as the phase of a periodic signal with frequency $f_{\mathrm{CLK}}A/Q$. The lookup table address bus is connected to the accumulator output, and the data ideally are the sine of the corresponding address:

$$\mathrm{idealDATA}(i) = \sin\left[2\pi \frac{\mathrm{ADDRESS}(i)}{Q}\right] \tag{5.24}$$

where the variable i denotes the ith cell of the ROM.

The sine function assumes all real values between -1 and $+1$, while the ROM output can only assume discrete values, so Eq. (5.24) has to be rounded as

$$\mathrm{DATA}(i) = \mathrm{int}\left\{\frac{1 + \sin\left[2\pi \frac{\mathrm{ADDRESS}(i)}{Q}\right]}{2}(2^L - 1)\right\} \tag{5.24'}$$

The ROM output given by Eq. (5.24′) assumes all integer values between 0 and $2^L - 1$ where L is the number of bits of ROM data.

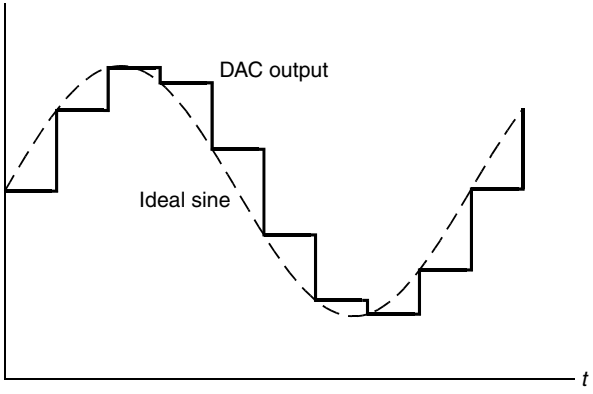


Figure 5.14 DDS DAC output waveform.

The accumulator output can be $0, 1, 2, \ldots, Q-1$, which is a digital word with length $\log_2(Q)$ bits corresponding to the size of the ROM. Q usually is an integer power of 2, and the ROM size is of course an integer number. The ROM output is a digital sequence that can be considered a staircase waveform approximating a sinusoidal waveform with frequency $f_{\mathrm{CLK}}A/Q$. That waveform which changes at each clock cycle, is affected by the quantization error due to the finite length of the ROM output. The ROM output digital sequence can be transformed into an analog waveform with a DAC. Figure 5.14 shows the DAC output and the corresponding sinusoidal waveform.

The DAC output waveform is an approximation of the sine wave with frequency

$$f_o = f_{\mathrm{CLK}}\frac{A}{Q} \tag{5.25}$$

sampled at a frequency equal to that of the accumulator clock, but the waveform of Fig. 5.14 is a sequence of rectangular pulses having width $T_{\mathrm{CLOCK}} = 1/f_{\mathrm{CLK}}$ instead of Dirac pulses. We want to make the DDS generate a sinusoidal signal with unit[†] amplitude and frequency $f_o = f_{\mathrm{CLK}}A/Q$. Denote that signal with $s(t)$:

$$s(t) = \sin(2\pi f_o t)$$

Its spectrum is

$$S(f) = \frac{\delta(f - f_o) - \delta(f + f_o)}{2j}$$

[†]This assumption implies no lack of generality.

Ideal sampling of a signal $s(t)$ with sampling frequency f_{CLK} consists of multiplying $s(t)$ by a periodic sequence of Dirac pulses with a period of $1/f_{\mathrm{CLK}}$. Sampling of $s(t)$ with frequency f_{CLK} gives the following signal:

$$s(t)^* = \sin(2\pi f_o t) \sum_{k=-\infty}^{+\infty} \delta\left(t - \frac{k}{f_{\mathrm{CLK}}}\right)$$

with the spectrum

$$S(f)^* = f_{\mathrm{CLK}} \sum_{k=-\infty}^{+\infty} \frac{\delta(f + f_o - kf_{\mathrm{CLK}}) - \delta(f + f_o - kf_{\mathrm{CLK}})}{2j}$$

Sampled signal $s(t)^*$ consists of a sequence of Dirac pulses placed at discrete equal-spaced time $t_k = k/f_{\mathrm{CLK}}$ with area equal to $s(t_k)$. The DAC output is a sequence of rectangular pulses with amplitudes equal to $s(t_k)$ and widths equal to $1/f_{\mathrm{CLK}}$. Its spectrum can be calculated by multiplying $S(f)^*$ by the response of the filter having a pulse response equal to the rectangular pulse with unit amplitude and width $1/f_{\mathrm{CLK}}$. The frequency response of that filter is given by the inverse Fourier transform of its pulse response:

$$T(f) = \int_0^{\frac{1}{f_{\mathrm{CLK}}}} \exp(j2\pi f t)\, dt = \frac{1}{f_{\mathrm{CLK}}} \frac{\sin\left(\pi \frac{f}{f_{\mathrm{CLK}}}\right)}{\pi \frac{f}{f_{\mathrm{CLK}}}} \exp\left(j\pi \frac{f}{f_{\mathrm{CLK}}}\right)$$

The spectrum of the DAC output signal is given by $S(f)^*$ multiplied by $T(f)$:

$$S_{\mathrm{DAC}}(f) = \sum_{k=-\infty}^{+\infty} \frac{\delta(f + f_o - kf_{\mathrm{CLK}}) - \delta(f + f_o - kf_{\mathrm{CLK}})}{2j} \times \frac{\sin\left(\pi \frac{f}{f_{\mathrm{CLK}}}\right)}{\pi \frac{f}{f_{\mathrm{CLK}}}} \exp\left(j\pi \frac{f}{f_{\mathrm{CLK}}}\right) \tag{5.26}$$

The magnitude of the DAC output spectrum is

$$|S_{\mathrm{DAC}}(f)| = \sum_{k=-\infty}^{+\infty} \frac{\delta(f + f_o - kf_{\mathrm{CLK}}) - \delta(f + f_o - kf_{\mathrm{CLK}})}{2} \times \left| \frac{\sin\left(\pi \frac{f}{f_{\mathrm{CLK}}}\right)}{\pi \frac{f}{f_{\mathrm{CLK}}}} \right| \tag{5.26′}$$

The DAC output spectrum has one spectral line with the same frequency of signal $s(t)$ and infinite spectral components at frequencies of

$kf_{\mathrm{CLK}} \pm f_o$ with k assuming all integer values. A useful spectral component has frequency f_o, and the closest unwanted spectral component has frequency $f_{\mathrm{CLK}} - f_o$. The original signal $s(t)$ can be reconstructed by filtering out all unwanted spectral components. This can be done only if

$$f_o < f_{\mathrm{CLK}} - f_o \Rightarrow \underline{\underline{f_o < \frac{f_{\mathrm{CLK}}}{2}}} \tag{5.27}$$

Equation (5.27) is the well-known condition on the sampling frequency given by the Shannon theorem. The maximum frequency given by Eq. (5.27) is also known as the *Nyquist frequency*. The output lowpass filter of Fig. 5.13 should be an ideal lowpass filter with a cutoff frequency of f_{CLK}. It filters out all unwanted spectral components presenting at its output the pure sine we want to generate. Anyway Eq. (5.26′) states that the amplitude of the output signal depends on its frequency with the factor

$$T'(f_o) = \sin\left(\pi \frac{f_o}{f_{\mathrm{CLK}}}\right)\left(\pi \frac{f_o}{f_{\mathrm{CLK}}}\right)^{-1} = \mathrm{sinc}\left(\pi \frac{f_o}{f_{\mathrm{CLK}}}\right) \tag{5.28}$$

which is close to unity for very low frequencies. It monotonically decreases with f_o for a minimum value of $2/\pi$ (about -3.9 dB) at maximum frequency $f_{o,\mathrm{MAX}} = 0.5 f_{\mathrm{CLK}}$. The spectrum of the DAC output with the *sinc* filter $T'(f)$ and the ideal lowpass output characteristics are shown in Fig. 5.15 where the x axis is frequency normalized to the sampling frequency f_{CLK}. The output ideal lowpass cutoff frequency is half of the sampling frequency. At this frequency the output filter gain crosses $T'(f)$ at the value $T'(f_{\mathrm{CLK}}/2) = 2/\pi$.

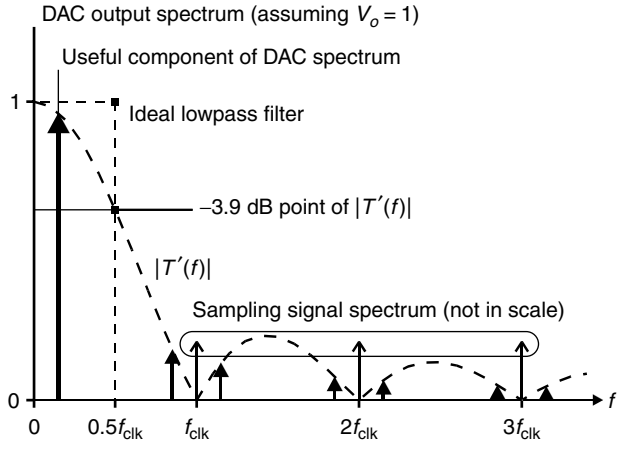


Figure 5.15 DDS output.

The signal at the output of the lowpass filter is a sinusoid with a frequency given by Eq. (5.25) with the limitation of the Shannon theorem given by Eq. (5.27):

$$f_o = f_{\text{CLK}}\frac{A}{Q} \qquad f_o < \frac{f_{\text{CLK}}}{2} \Rightarrow A < \frac{Q}{2} \tag{5.29}$$

The DDS output frequency is changed by changing the input addendum of the accumulator. The output frequency resolution is

$$f_{\text{RES}} = \frac{f_{\text{CLK}}}{Q} \tag{5.30}$$

Here are some typical numbers:

- Clock frequency: $f_{\text{CLK}} = 20$ MHz
- Accumulator size: 24 bits $\Rightarrow Q = 2^{24} - 1$
- Maximum theoretical output frequency: $f_{o,\text{MAX}} = f_{\text{CLK}}/2 = 10$ MHz
- Output frequency resolution: $f_{\text{RES}} = f_{\text{CLK}}/Q \cong 1.2$ Hz

DDS integrated circuits are available on the market with an accumulator, lookup table, and DAC in a single chip; the clock frequencies exceed 1 GHz and frequency resolutions reach values well below 1 Hz.

5.5.2 Effects of nonideal components on DDS performance

The discussion in Sec. 5.5.1 was based on ideal DDS components. It was found that the DDS output signal is a pure sine, ideally sampled at frequency f_{CLK}, filtered by the sinc filter, processed by a DAC (which is inherently nonlinear), and filtered by an ideal lowpass filter. Based on these conclusions, the DDS schematic of Fig. 5.13 can be modeled with the functional block diagram of Fig. 5.16.

The signal at the input of the DDS functional block diagram (node n_1) is a pure sine. The ideal sampler consists of one multiplier by sampling the sequence of Dirac pulses with period $1/f_{\text{CLK}}$; the sampled input is at node n_2. The sinc filter transforms an ideally sampled signal into a rectangular pulse sequence of DAC output (node n_3). The nonlinear transfer characteristic models the DAC staircase characteristic and other nonlinearities that can be present. The DAC output is the signal on node n_4. A reconstruction filter removes all unwanted spectral components. The DDS output signal is at node n_5.

5.5.2.1 Reconstruction filter. An ideal lowpass filter like that considered in Sec. 5.5.1 is not physically realizable as known. Practical filters have finite selectivity. One widely used lowpass filter topology is the

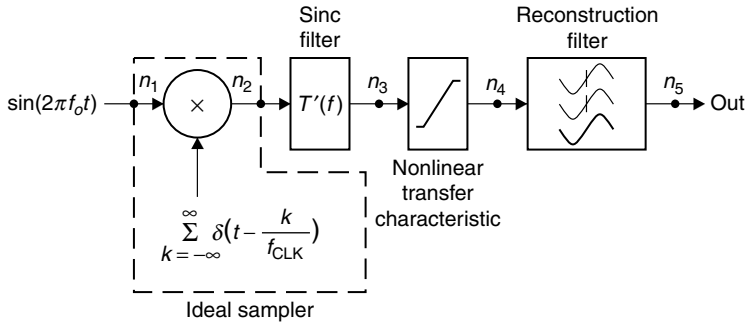


Figure 5.16 DDS functional block diagram.

lumped passive *LC* ladder network of Fig. 5.17. The most common configuration is with equal source and load resistance,[†] symmetrical structure, and Chebysheff response with odd order. The order of the filter equals the number of reactive elements. Design formulas for that filter can be found in the literature and can be easily implemented into a MATHCAD worksheet.[‡]

The passband attenuation of Chebysheff filters varies between 0 and RP, where RP is a defined design parameter named *ripple* and is usually expressed in decibels. For this reason Chebysheff filters are also known as *equal ripple* filters. Figure 5.18 shows the frequency response of three Chebysheff filters with a ripple of 0.1 dB and three different orders ($N = 7$, 9, and 13). The cutoff frequency of these filters is chosen to have 60 dB of attenuation at the Nyquist frequency. Because of the nonideal response of the filters, the maximum DDS output frequency (the cutoff frequency of the filter) is quite lower than the theoretical Nyquist frequency ($0.5 f_{\mathrm{CLK}}$) being $0.242 f_{\mathrm{CLK}}$, $0.311 f_{\mathrm{CLK}}$, and $0.391 f_{\mathrm{CLK}}$, respectively, for $N = 7$, 9, 13.

Selectivity of the reconstruction filter is then a limiting factor for the maximum DDS output frequency: It will approach its theoretical limit

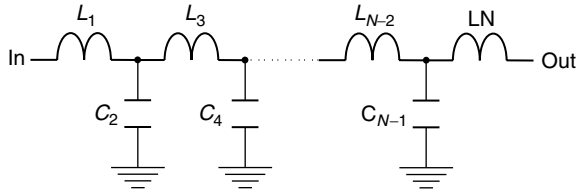


Figure 5.17 Lumped passive *LC* ladder lowpass filter.

[†]Defined as doubly terminated filters.

[‡]See the MATHCAD file LowPassFilter.MCD.

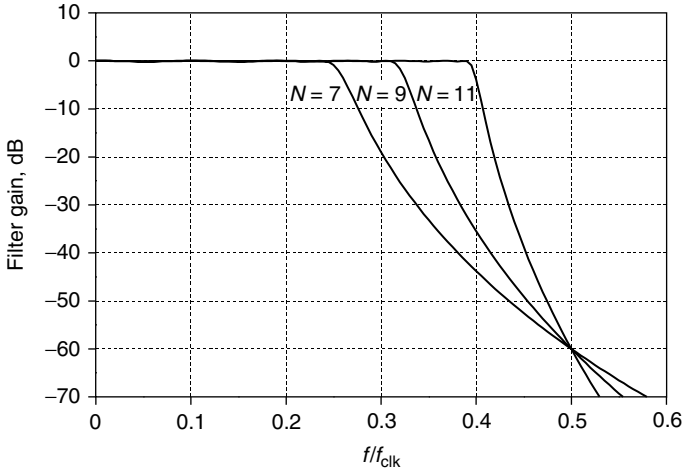


Figure 5.18 Response of Chebysheff filters with 0.1-dB ripple and different order.

of the Nyquist frequency as the filter selectivity (i.e., order of the filter) is increased. The maximum DDS output frequency for spur (unwanted spectral components above Nyquist frequency) attenuation of 50 dB and 60 dB is plotted in Fig. 5.19 versus filter order. It is assumed that the filters have 0.1 dB of ripple.

In any case, the filter order cannot be arbitrarily increased because high-order filters are very critical and sensitive to the tolerance of components' values. Moreover real capacitors and inductors are not purely

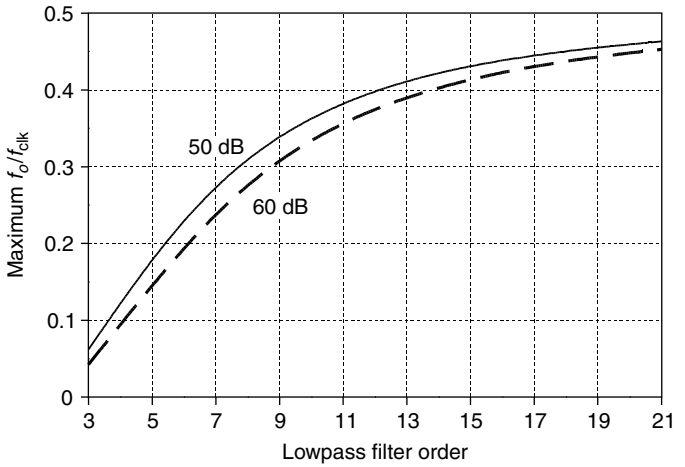


Figure 5.19 Maximum DDS output frequency for spur attenuation of 50 and 60 dB.

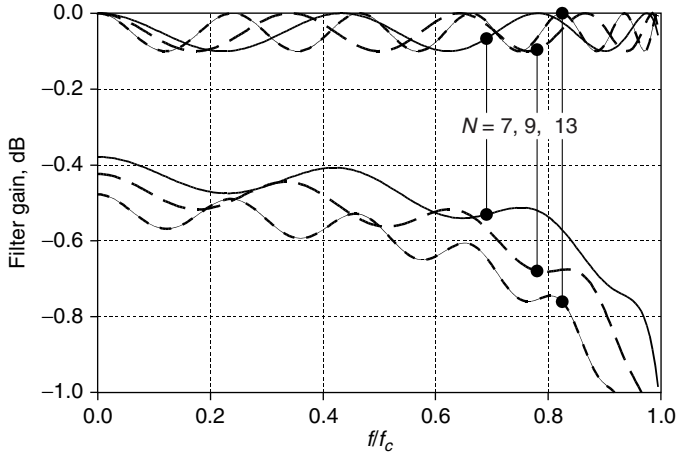


Figure 5.20 Chebysheff filters of different order with (lower traces) and without (upper traces) dissipation loss.

reactive elements but present power dissipation that can be taken into account with parasitic shunt or series resistors or with the Q factor. The effects of the finite Q factor of reactive elements are shown in Fig. 5.20 where the frequency responses of three Chebysheff filters are plotted with and without taking into account the dissipation. All filters have the same ripple and cutoff frequency. The dissipation loss smoothes the filter response as the frequency approaches the cutoff, making the response less sharp. This reduction of filter selectivity increases with the filter order. In any case the DDS maximum output frequency has to be even lower than the value taken from Fig. 5.19 because of the margins needed for filter tolerance and smoothing of the response close to cutoff.

Chebysheff filters have all their poles of attenuation at infinite frequency, where series inductors become open circuits and shunt capacitors become short circuits. Filter selectivity can be increased without increasing the order by introducing poles of attenuation at finite frequencies with the use of elliptic filters (also known as Cauer filters). They approximately are Chebysheff filters with series inductors (or shunt capacitors) replaced by parallel (or series) LC. This way poles of attenuation at infinite frequency are translated toward the resonant frequency of LC elements.

Figure 5.21 shows one Chebysheff filter and one elliptic filter,[†] together with their frequency responses. Both filters are seventh order with 0.1 dB ripple and 8 MHz cutoff frequency. The values of their

[†]See the SIMETRIX file DDS1_Lowpass3.sxsch.

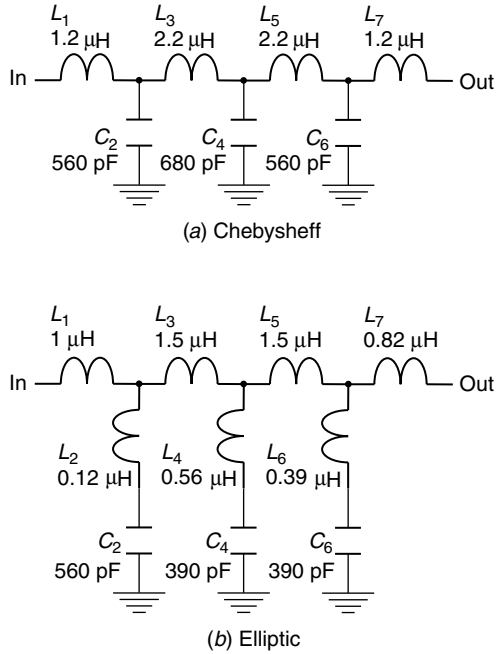


Figure 5.21 Chebysheff and elliptic filters with a cutoff frequency of 8 MHz.

components are approximated to the closest standard value. The response of Fig. 5.21*c* clearly shows how a shift of attenuation poles from infinite to a frequency close to cutoff improves selectivity. Elliptic filters have higher selectivity than Chebysheff filters with the same order.

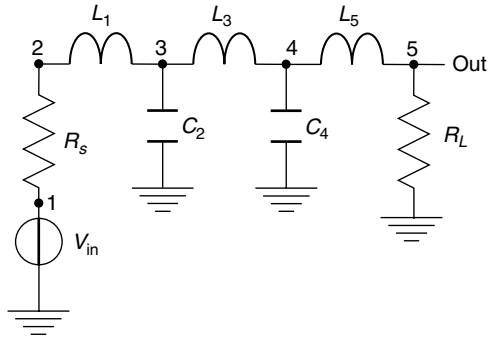


Figure 5.22 Fifth-order lowpass filter.

A given selectivity can be obtained with a lower order if an elliptic filter is used. A lower order implies less smoothing of the frequency response close to the cutoff and a lower sensitivity of the frequency response to the tolerance of the component values.

Calculation of the effects of the tolerance on components' values, and the effects of using nonexact values for the filter elements (due to the use of standard values) can be done with both mathematical and circuit analysis programs. The latter case is quite straightforward and consists of performing AC and Monte Carlo analyses of the filter. Filter analysis can also be performed with mathematical programs.[†] The basic procedure for ladder filter analysis will be illustrated with the circuit of Fig. 5.22 representing a fifth-order lowpass filter including the source and load. The procedure is based on the assumption of unitary output voltage and deducing all voltages and currents of the circuit beginning from the output and recursively going back to the input.
Let the output voltage be 1. Then

Current flowing through the output load and inductor L_5 is

$$I_1(f) = \frac{1}{R_1}$$

Voltage on node 4 is

$$V_4(f) = 1 + I_1(f)\, j 2\pi f\, L_5$$

Current through capacitor C_4 is

$$I_4(f) = j 2\pi f\, C_4 V_4(f)$$

[†]See the MATHCAD file LowPassFilter_Synthesis_Analysis.MCD and the SIMETRIX file LowPassFilter_Synthesis_Analysis.sxsch for comparison.

Voltage on node 3 is

$$V_3(f) = V_4(f) + [I_1(f) + I_4(f)]j2\pi f L_3$$

Current through capacitor C_2 is

$$I_2(f) = j2\pi f C_2 V_3(f)$$

Voltage on node 1 is

$$V_1(f) = V_3(f) + [I_1(f) + I_2(f) + I_4(f)](j2\pi f L_1 + R_s)$$

Available power from source V_{in} is

$$P_{\text{in}}(f) = \frac{V_1(f)^2}{4R_s}$$

Filter gain is

$$\text{Gain}(f) = 10\log_{10}\left[\frac{P_{\text{out}}(f)}{P_{\text{in}}(f)}\right] = -10\log_{10}[P_{\text{in}}(f)]$$

The above procedure can be generalized for filters of any order. More complicated impedance expressions than inductors and capacitors can also be used to give a more realistic description of real components. Component values can be modified displaying the resulting response.

5.5.2.2 Nonlinearities. A sampled signal generated by a DAC is distorted by the quantization error generated by a combination of finite length of ROM output word and DAC resolution. Thus even in the ideal case, the sampled signal passes through a nonlinear transfer characteristic which is the block after the sinc filter in Fig. 5.16. Moreover real DACs present additional nonlinearity due to deviation from the nominal staircase characteristic. The signal on node n_3 of Fig. 5.16 has the spectrum given by Eq. (5.26′). The spectrum has infinite components with frequencies given by

$$f_o \qquad \text{and} \qquad kf_{\text{CLK}} \pm f_o \qquad \text{with} \qquad k = 1, 2, 3, \ldots$$

At nonlinear transfer output all the above spectral components intermodulate generating even more spectral components with frequencies of

$$f_o \qquad \text{and} \qquad kf_{\text{CLK}} \pm mf_o \qquad \text{with} \qquad k, m = 1, 2, 3, \ldots$$

Some of these products have frequencies lower than the output lowpass cutoff and will not be filtered: They are known as DDS output spurs. Their level normally is in the range from -45 to -70 dBc. DAC nonlinearity is often generated by internal crosstalk due to parasitic coupling.

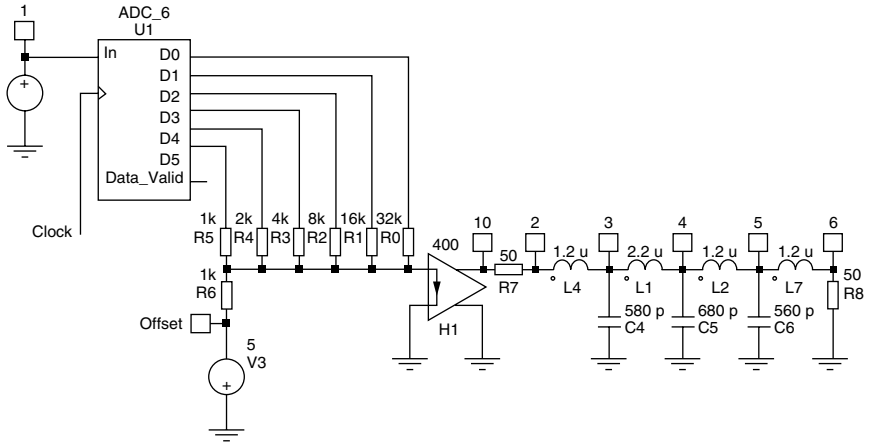


Figure 5.23 SIMETRIX schematic of DDS.

These effects increase with the clock frequency. Consequently the general trend is that higher clock frequency DDSs have the higher spur level.

Some calculations of a DDS output spectrum can be performed[†] with both MATHCAD and SIMETRIX. The first method is quite straightforward: Accumulator output is calculated with Eq. (5.23), ROM ideal (no quantization) with Eq. (5.24), DAC ideal output (only quantization, no further nonlinearity) with Eq. (5.24′). Additional nonlinearity is modeled with a third-order polynomial and spectra are calculated with the FFT. The SIMETRIX simulation circuit is shown in Fig. 5.23. The accumulator output is the digital output of the analog to digital converter (ADC), U1 has a 2.3-MHz sinusoidal signal as its input (node 1), and the clock is a digital pulse generator with a period of 50 ns and 50% of duty cycle (20-MHz square wave). Digital outputs $D_0, D_1, \ldots, D_5$ exactly model the ROM output ($D0$ is LSB, $D5$ is MSB). The circuit of Fig. 5.25 includes one 6-bit weighted resistor DAC with 50-Ω output resistance, consisting of

- Resistors R0, R1, . . . , R5
- Resistor R6 and DC source V3 (the offset compensation network)
- CCVS[‡] H1 with R7 (the output matching network)

[†]See files DDS1.mcd and DDS1.sxsch.

[‡]Current-controlled voltage source.

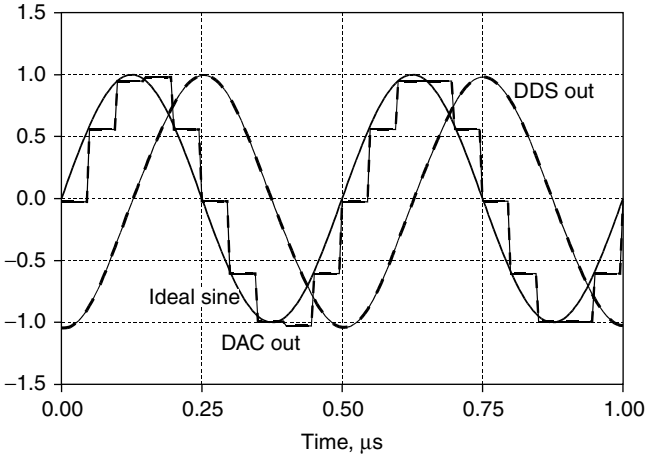


Figure 5.24 Output waveforms of circuit of Fig. 5.23. Node 1—ideal sine, node 10—DAC output (multiplied by 2), node 6—DDS output.

The *LC* ladder network between nodes 2 and 6 is the output lowpass filter (same circuit as in Fig. 5.21*a*), and the output filter load is R_8.

Output waveforms are simulated with a transient simulation and are plotted in Fig. 5.24. The output signal is delayed with respect to the input. This is due in part to the conversion time of the ADC and in part to the group delay of the output filter.

The output spectrum (node 6) of the circuit in Fig. 5.23 is plotted in Fig. 5.25. Figure 5.25*a* shows the DDS output spectrum for an output frequency of 2.3 MHz. Note the many spectral lines around the fundamental frequency. These are the DDS spurs, and they have a maximum level of about −43 dBc. Above 8 MHz the spur level is attenuated by the output lowpass filter. Figure 5.25*b* shows the DDS output spectrum when the output frequency is 2 MHz. Note that the spur energy is concentrated around the harmonies of the output frequency. This is because the output frequency (2 MHz) and the clock frequency (20 MHz) are both integer multiples of the same frequency. Such a condition usually involves a reduced accuracy of the simulation.

A simulation was performed with a simple 6-bit ADC in order to give prominence to spurs. The number of ADC bits and numbers of weighted resistors of the DAC can be increased in order to reduce the spur level. The circuit of Fig. 5.23 allows some interesting analyses on the DDS, for example:

- Impairment can be introduced into a DAC in order to model some nonlinearity and to study its effect on the output spectrum.

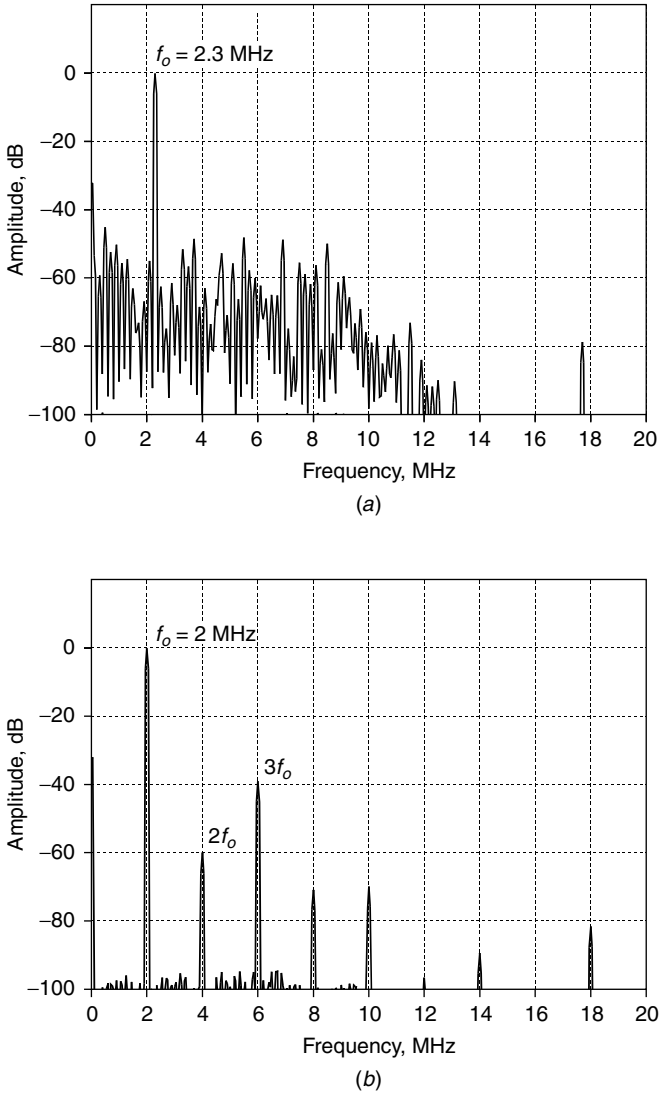


Figure 5.25 DDS output spectrum from the circuit of Fig. 5.23.

- Time-domain noise can be added to the ADC clock in order to study the effect of jitter.
- The output filter can be changed with less or more selective ones.

The DDS synthesizer has a high-frequency resolution, fast frequency settling (just the time needed to change the input addendum register),

and low phase noise (about that of a clock signal with some degradation due to the noise of digital circuits). Two drawbacks of a DDS are output spurs and a maximum output frequency that is about 1 GHz for faster DDSs on the market.

Frequency multiplication is needed for generation of microwave signals. Calculation of effects of frequency multiplication on DDS spurs is interesting in this regard.
Let $s(t)$ be the signal generated by a DDS and affected by a spur:

$$s(t) = \sin(2\pi f_o t) + \Delta v \sin[2\pi(f_o + \Delta f)t]$$

where the first term is the carrier and the second term is the unwanted spur with amplitude $\Delta_v \ll 1$. Moreover the spur frequency is lower than the maximum DDS output frequency: thus $\Delta f < f_{\mathrm{CLK}}/2f_o$. Consider now a frequency doubler consisting of a nonlinear two-port device with an output voltage equal to twice the square of the input voltage. Assume that $s(t)$ is the input voltage and $s_2(t)$ is the corresponding output:

$$s_2(t) = 2s(t)^2 = 2\{\sin(2\pi f_o t) + \Delta v \sin[2\pi(f_o + \Delta f)t]\}^2$$

$$s_2(t) \cong 2\sin^2(2\pi f_o t) + 4\Delta v \sin(2\pi f_o t)\sin[2\pi(f_o + \Delta f)t]$$

$$s_2(t) \cong 1 - \cos[2\pi(2f_o)t] + 2\Delta v \cos(2\pi \Delta f t) - 2\Delta v \cos[2\pi(2f_o + \Delta f)t]$$

The doubler output signal is the sum of four terms: the first is a DC component, the second is a cosine with a frequency double that of the input, the third has a frequency below the DDS Nyquist frequency, and the fourth has a frequency close to that of the second term. Low-frequency components can be easily eliminated with a bandpass filter, so the only important terms are the second and the fourth. Let $s_2'(t)$ be the filtered signal containing those two terms only (with the sign changed for simplicity):

$$s_2'(t) \cong \cos[2\pi(2f_o)t] + 2\Delta v \cos[2\pi(2f_o + \Delta f)t]$$

The filtered frequency doubler output has two spectral components:

- The carrier, a cosine with the same amplitude as the input carrier and double frequency.
- The spur having the same distance Δf from the carrier as the input signal but with double the amplitude.

In other words a frequency duplication increases the spur level by a factor of 2(+6.02 dB). This result can be generalized to any frequency

multiplication factor.

$$\text{OutSpurLevel[dBc]} = \text{InputSpurLevel[dBc]} + 20\log_{10}(N) \qquad (5.31)$$

where N is the frequency multiplication factor.

Equation (5.31) was derived assuming a low spur level and is valid until the predicted output spur level is below -10 dBc. This assertion coincides with that of Sec. 2.6.1 about phase noise increasing (or decreasing) due to frequency multiplication (or division): In fact phase noise can be considered as the sum of many low-level spurs whose frequencies are distributed around the carrier.

5.5.2.3 Compensation of sinc filter. One of the results of Sec. 5.5.1 is that the amplitude of the DDS output signal is decreasing in frequency by the sinc factor $T'(f_o)$ given by Eq. (5.28). Many techniques can be used to obtain flat power across the frequency. The first is to connect a voltage-controlled amplifier (or attenuator) at the lowpass filter output and modify the gain (or the attenuation) frequency by frequency to flatten the output power. This gain control can be done by

1. Open-loop mode. Control voltage is generated by a DAC driven by a ROM correction table whose input is the output frequency.
2. Closed-loop mode. Output power is measured with a detector and compared with a reference voltage; the difference between them generates the control voltage.

A simpler solution is to use an equalizer[†] like that shown in Fig. 5.26. It is designed to operate with a 50-Ω source and load impedance and for a clock frequency of 20 MHz. A different design for a different clock frequency can be obtained by dividing all reactive elements by the ratio between the desired clock frequency and 20 MHz (frequency scaling). The circuit is symmetric and presents about 6 dB of insertion loss in DC, gain can be restored with a 6-dB amplifier. The input is node 2; the output is node 6.

The response of the equalizer together with the sinc factor and their combination are plotted in Fig. 5.27. The resulting equalized output power flatness is better than ± 0.4 dB.

5.5.3 Enhancements of DDS architecture

The full digital structure of a DDS is very flexible. Important additional capabilities can easily be added.

[†]See the SIMETRIX file DDS_SINC_Compensation.

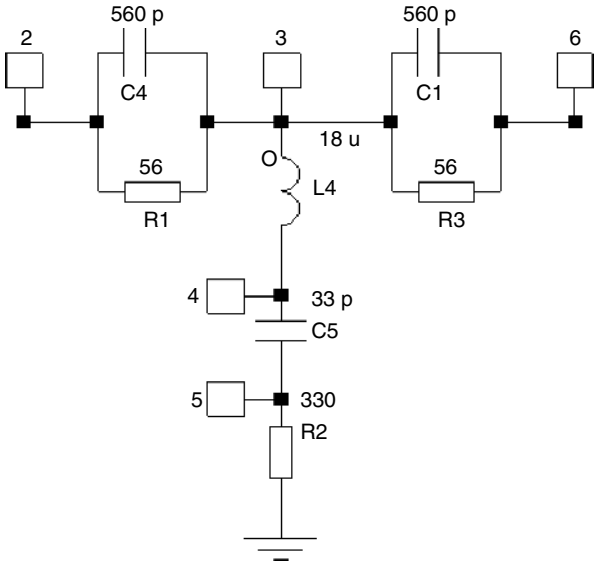


Figure 5.26 Equalizer of DDS output level (20-MHz clock frequency).

Different waveforms can be generated by a DDS simply by changing the relation between the address and data of the lookup table (sawtooth, triangular, square waves, and even noise). A phase modulation port can be added by inserting an adder between the accumulator output (which

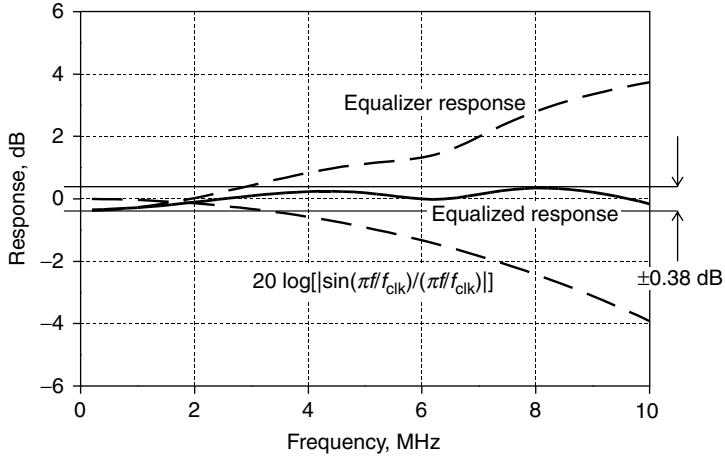


Figure 5.27 Sinc equalizer response. (*a*) Sinc filter $T'(f)$, (*b*) equalizer response, and (*c*) equalized sinc response, (flatness better than ±0.4 dB).

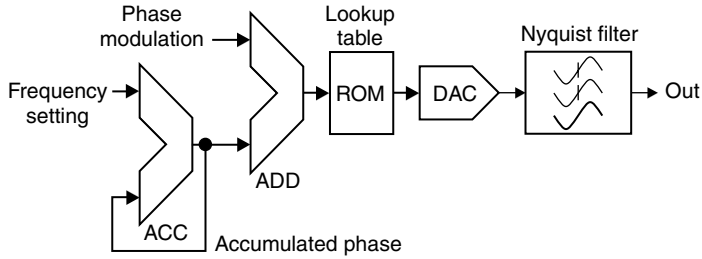


Figure 5.28 DDS with phase modulation capability.

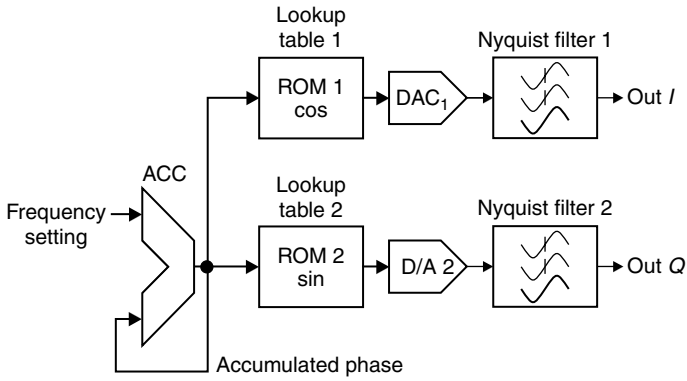


Figure 5.29 DDS with quadrature generation capability.

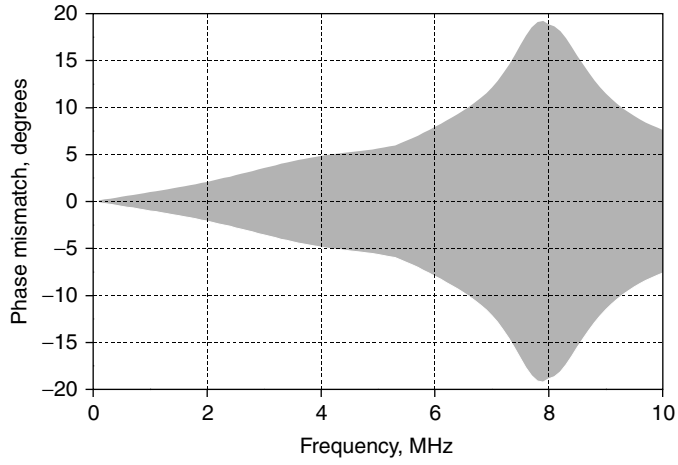


Figure 5.30 Phase mismatch of the Fig. 5.21*a* filter for 10% component tolerance.

represents the phase of the synthesized signal) and the PROM address input as shown in Fig. 5.28.

A DDS can generate in-phase and quadrature (I and Q) signals, i.e., two coherent sinusoidal signals with the same frequency and 90° out of phase. This can be done by duplicating the ROM, DAC, and output filter. Two ROMs share the same address coming from accumulator output. The data of the first ROM contain the cosine, while the data of the second ROM contain the sine of the address. An arrangement for I and Q generation is shown in Fig. 5.29.

However, the quadrature relation between output signals is conserved only if two output filters are phase matched, and this requirement can be difficult to achieve because of the high order of the filter and then the large group delay. Figure 5.30 shows phase matching between two filters like that of Fig. 5.21*a*, one with nominal components and the other with capacitors and inductors statistically varying ±10 percent. The maximum possible phase mismatch is about ±20° close-to-cutoff frequency of 8 MHz. Phase mismatch was calculated performing 200 iterations of the Monte Carlo analysis.†

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Giovanni Bianchi is a senior microwave engineer at SDS Technology in Rome, Italy, and a frequent speaker at professional gatherings such as the European Microwave Conference and IEEE MTT symposia. He was previously a principal staff engineer with Motorola PCS where he disclosed six PLL-related circuits. A reviewer of the *IEEE Microwave and Guided Wave Letter* since 1995, Mr. Bianchi is also a reviewer for *IEEE Microwave Magazine*.

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