HIGH - LEVEL SYNTHESIS
Introduction to
Chip and System Design

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by

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Preface

Rationale

Computer-aided design (CAD) research, and the CAD industry in particular, has been very successful and has enjoyed exceptional growth, paralleled only by the advances in IC fabrication. Since problems at lower levels of design became humanly intractable and time consuming earlier than on higher abstraction levels, CAD researchers and the industry first turned to problems such as circuit simulation, placement, routing and floorplanning. CAD tools for logic simulation and synthesis came later. As design complexities grew and time-to-market requirements shrank drastically, industry and academia started focusing on even higher levels of design than logic and layout. A higher level of abstraction reduces the number of objects that a designer needs to consider by an order of magnitude, which in turn allows the design and manufacture of larger systems in shorter periods of time. High-level synthesis is thus the natural next step in the design methodology of VLSI systems.

Another reason for the emphasis on high-level design methodologies is that high-level abstractions are closer to a designer's way of thinking. It is difficult to imagine a designer specifying, documenting and communicating a chip design in terms of a circuit schematic with 100,000 gates, or a logic description with 100,000 Boolean expressions. With increasing design complexity, it becomes impossible for a designer to comprehend the functionality of a chip or a system specified completely with circuit or logic schematics. A system described in terms of higher level components (e.g., memories, registers, ALUs and buses) and specified using higher level operations on data values over time exposes the design's functionality and allows a designer to consider alternative implementations with

ease.

Research on high-level synthesis started over twenty years ago, but did not come into focus since lower level tools were not available to seriously support the insertion of high-level synthesis into the mainstream design methodology. Since then, substantial progress has been made in formulating and understanding the basic concepts in high-level synthesis. Although many open problems remain, the two most important problems are the lack of a universally accepted theoretical framework and a CAD environment supporting both automatic and manual high-level synthesis. In spite of these deficiencies, high-level synthesis has matured to the point that a book is necessary to summarize the basic concepts and results developed so far and to define the remaining open problems. Such a reference text will allow the high-level synthesis community to grow and prosper in the future.

Audience

This book in intended for three different groups in the CAD community.

First, it is intended for CAD managers and system designers who may be interested in the methodology of chip and system design and in the capabilities and limitations of high-level synthesis tools.

Second, this book can be used by CAD tool developers who may want to implement or modify algorithms for high-level synthesis. Complementary books by Camposano and Wolf [CaWo91] and Walker and Camposano [WaCa91] discuss specific research approaches to high-level synthesis.

Finally, since this book surveys basic concepts in high-level design and algorithms for automatic synthesis, it is also intended for graduate students and seniors specializing in design automation and system design.

Textbook Organization

The book is organized into nine chapters that can be divided into five parts. Chapters 1 and 2 present the basic concepts and the system design process. Chapters 2 and 3 deal with design models and quality

metrics for those models. Chapters 4 and 5 deal with design description languages and design representation. Chapters 6, 7 and 8 provide a survey of algorithms for partitioning, scheduling and allocation, while Chapter 9 covers the issues of design methodology and frameworks for high-level synthesis.

Given an understanding of the concepts defined in Chapters 1 and 2, each chapter is self-contained and can be read independently. We used the same writing style and organization in each chapter of the book. A typical chapter starts with an introductory example, defines the basic concepts and describes the main problems to be solved. It follows with a description of several well known algorithms or solutions to the posed problems and explains the advantages and disadvantages of each approach. Each chapter ends with a short survey of other work in the field and some open problems.

The book is designed for use in two different courses. One course would be on system design and methodology, omitting the synthesis algorithms in Chapters 6, 7 and 8; a second course would emphasize high-level synthesis techniques and omit the material on languages and frameworks in Chapters 4 and 9.

We have included several exercises at the end of each chapter. These exercises are divided into three categories: homework problems, project problems and thesis problems. Homework problems test the understanding of the basic material in the chapter. Project problems, indicated by an asterisk, require some literature research and a good understanding of the topic; they may require several weeks of student work. Thesis problems, indicated by a double asterisk are open problems that may result in an M.S. or even a Ph.D. thesis if researched thoroughly.

We hope that this book fills the need for a unifying body of material on high-level synthesis; we welcome your comments and corrections.

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