Technology Processes Options and mmwave Reference Circuits for 5G Communication

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Outline

• Overview and Globalfoundries process options
• 45RFSOI Technology Introduction
• FEM Demonstrator Design with 45RFSOI
  – Ka band Switch Design
  – Ka Band Power Amplifier Design
  – Ka Band Low-Noise-Amplifier Design
• Summary
Mobile Data Usage Exploding

General Mobile Data Traffic Growth / Top Line

- 2016: 6.8 EB
- 2017: 10.7 EB
- 2018: 16.1 EB
- 2019: 24.3 EB
- 2020: 35.0 EB
- 2021: 49.0 EB

38% CAGR
600X growth

Device Data Consumption

- M2M Module = 3 X
- Wearable Device = 6 X
- Smartphone = 37 X
- Tablet = 94 X
- Laptop = 119 X

Source: Adapted from Cisco VNI Mobile Report, 2017

IEEE CICC, Austin, TX, 2017
One technology doesn’t fit all…architecture and partitioning plays a role in choice

Must evaluate based on key merits, alignment and benefits to the end market
GLOBALFOUNDRIES process options

<table>
<thead>
<tr>
<th>Offering</th>
<th>Target Applications</th>
</tr>
</thead>
<tbody>
<tr>
<td>7RF SOI</td>
<td>1st switch/LNA applications, etc</td>
</tr>
<tr>
<td>7SW</td>
<td>2nd switch/LNA applications, etc</td>
</tr>
<tr>
<td>130RFSOI</td>
<td></td>
</tr>
<tr>
<td>8SW</td>
<td>3rd switch/LNA applications, etc</td>
</tr>
<tr>
<td>45RFSOI</td>
<td>mmWave applications, 5G, etc</td>
</tr>
<tr>
<td>5PAe / 1KW5PAe</td>
<td>2nd WiFi applications, PA</td>
</tr>
<tr>
<td>5PAX / 1K5PAXe</td>
<td>3rd WiFi applications, PA</td>
</tr>
<tr>
<td>7PA</td>
<td>Cellular PA applications</td>
</tr>
<tr>
<td>8HP/XP</td>
<td>High performance mmWave, etc</td>
</tr>
<tr>
<td>8uW</td>
<td>High performance mmWave, etc</td>
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<tr>
<td>9HP</td>
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Various mmWave Applications

Low Earth Orbit (LEO) satellites for broadband communications
Ka Band (26-40 GHz)

Advanced Driver Assistance System (ADAS) auto radar
24 & 77-81 GHz

Future 5G handset, CPE & small cell
24-86 GHz (proposed allocations based on WRC 15)

Millimeterwave backhaul
E Band (71-76 & 81-86 GHz)

Common system blocks: **Phased array antennas**, mmWave up & down converters, mmWave LO generation, mmWave LNA & power amplifiers, mmWave switches, phase shifters, power combiners/splitters

Frequency range: 24–100 GHz

- Depending on Tx output power level, number of phased array antenna and frequency band, chip partitioning and integration for radio interface (FEM, TRx) will vary
- Opportunity for mmWave silicon technologies for user equipment (UE), access points (AP) and infrastructure
- Other applications: augmented reality, virtual reality, optical communications, IoT, machine-based communications, etc.
Case Study: 5G / WiGig mmWave Handset Architecture with 45RFSOI FEM

45RFSOI

14nm/12FDX/7nm CMOS
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  – Ka Band Power Amplifier Design
  – Ka Band Low-Noise-Amplifier Design
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45RFSOI Introduction (1/2)

- **SOI process:**
  - Transistors are built on a top layer of silicon isolated by a buried oxide layer from the substrate
  - Transistors in SOI have low parasitic junction capacitance, which results in higher performance ($F_t/F_{\text{max}}$)
  - SOI transistors can be stacked, which enables higher voltage and power handling
  - SOI substrate engineering provides additional RF benefits
    - Reduced parasitics, higher Q and lower loss
    - Increased isolation and linearity

- **45RFSOI provides high $F_t/F_{\text{max}}$ FETs:**
  - NFET: $F_t > 300\text{GHz}$; $F_{\text{max}} > 350\text{GHz}$
  - PFET: $F_t > 250\text{GHz}$; $F_{\text{max}} > 300\text{GHz}$

- **PDK:**
  - RF model
  - EM tool
  - Reliability tool

IEEE CICC, Austin, TX, 2017
45RFSOI Introduction (2/2)

• High resistivity handle wafer improves back-end-of-line (BEOL) loss and reduces harmonics
• Dual thick metal option provides high quality inductors, mmWave transformer
• 3-4 layers thin metal for digital block routing
• High Q or high density MIM cap
• Economical vertical natural capacitor
• High density resistors for RF isolation and low harmonics

BEOL IL comparison with different substrates
Inductor Q Improvement with Chamfering

- Chamfering improves Q for inductors used in mmWave blocks
- Smaller inductors have greater Q improvement with chamfering
- Chamfering at both inner and outer corners gives optimal performance
- Chamfer factor ~0.7 to 0.8 is the optimized number
- For 300pH inductor, Q factor can be improved up to 10%
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- 22FDX
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mmWave Switch Topology Options

• Switch topologies:
  – RF electromechanical switches
    • Not compatible with CMOS process
  – PIN diode switch:
    • DC power consumption
    • High power handling capability
  – Quarter wavelength transmission line:
    • Large area in 28/39GHz
    • Suitable for 60GHz or above
  – FET switch:
    • Series shunt topology: Smaller area
    • Tuned shunt topology: Low isolation
mmWave Switch Design/Optimization Strategies

• Series shunt topology is described in this evaluation (no series inductive matching to avoid matching network loss in this frequency)

• Optimize stack height number to trade off isolation versus insertion loss (IL)
  \[ |IL|^2 = 1 - |RL_{input}|^2 - |Iso|^2 \]
  Assume lossless case

• 45RF-FET provides good Ron, device level Ron*Coff < 90fs
  – Because of tight pitch, traditional metal wiring causes additional coupling
  – At mmWave frequency, higher Coff has larger impact to IL due to worsening RL and isolation

\[ Iso = -20 \log \left( \frac{2 \times Z_0//R_{on}}{\frac{2}{\omega C_{off}} + Z_0 + Z_0//R_{on}} \right) \]

  – Improved metal wiring coupling is very important to switch RF performance
Ku band SPDT Design

X/Ku band SPDT switch sizing

Tapered FET layout to reduce the drain to source coupling

Source: C Li, G Freeman, M Boenke, N Cahoon, U Kodak, G Rebeiz, “1W < 0.9dB IL DC-20GHz T/R Switch Design with 45nm SOI Process”, IEEE SiRF, 2017.
Small Signal Measurement Results

- Applications: Satcom, 5G
- Ron:
  - 0.4 ohm-mm @ <6GHz
  - <0.8ohm-mm @ 30GHz including wiring
- IL:
  - <0.5dB @ 10GHz
  - <0.9 dB @ 20GHz
Large Signal Measurement Results

- **P1dB**: 31.5dBm
- **Pmax (soft breakdown)**: >25dBm
- **IIP3 (one-tone measurement)**: 63.8dBm
- **Harmonics**: IMD2/3>90dBc

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*Measured by UCSD (courtesy of Professor Gabriel Rebeiz)*
Ka band SPDT
Hardware Results vs. Simulation

- **Applications**: Targeted for 5G UE FEM applications
- **Insertion loss**: 
  - 0.8dB IL < 30GHz
  - Good model to hardware correlation with 45RFSOI PDK
- **Nonlinearity**: P1dB is 30dBm (25dBm 0.1dBm compression)
- **Harmonics**: 
  - 2nd harmonic model to hardware correlation <3dB
  - 3rd harmonics, hardware is better than model

*Measured by UCSD (Courtesy of Professor Gabriel Rebeiz)*
Ku band SPDT NFET and PFET Comparison

- **Design sizing**
  - Choose the same topology and also same sizing
- **Insertion loss:**
  - 0.65dB IL @28GHz with PFET
  - 0.76dB IL @28GHz with NFET
- **Nonlinearity:** PFET should be better than NFET
- **Isolation**
  - SPDT with PFET shows about 1-2dB better than SPDT with NFET.
PA Design: Single-Ended PA

- **Design target:**
  - $\text{PAE}_{\text{max}} > 40\%$
  - $\text{PAE}_{9\text{dB}, \text{BO}} > 15\%$

- **FET sizing:**
  - $W/L = 2.7\mu m \times 10 \times 8/40\text{nm}$

- **DC bias conditions:**
  - $\text{VDD} = 2.9\text{ V}$
  - $V_{g1} = 0.25\text{ V}$
  - $V_{g2} = 1.15\text{ V}$
  - $V_{g3} = 2.15\text{ V}$

*Source: C Li, etc, “A High-Efficiency 5G K/Ka-Band Stacked Power Amplifier in 45nm CMOS SOI Process Supporting 9Gb/s 64-QAM Modulation with 22.4% Average PAE”, IEEE TXWMCS, 2017.*
PA Design / Optimization Strategies

• Determine the optimal number of stacked power transistors
  – 1 stack: Has high PAE, but low Psat
  – 4 stack: PAE drops below 40% based on schematic level evaluation

• Size the device so that the real part of the optimum load impedance is close to 50 ohm
  – Reduce output matching network loss
  – 1dB passives loss is equal to 20% PAE reduction
  – With matching network, difficult to meet >40% PAE target

• Use gate RC network to tune the phase

• Use Lm and Cm to improve PAE
  – Based on our evaluation, this improves PAE ~6%
Small Signal Measurement Results

Wide 1dB bandwidth, 18GHz - 29GHz
Summary

- 16dB Psat and 41% peak PAE achieved
- 9.6dB back-off PAE is 15%
- Reasonable model to hardware correlation in large signal behavior
- Design can meet 8X8 array PA power requirement
Large Signal Measurement (2/2)

• Very wide bandwidth
  – Psat 1dB bandwidth is 18-29GHz, similar to small signal bandwidth

• PAE > 35% in 1dB bandwidth range
  – Good for single carrier high data rate transmission scenario

• 9.6dB back off PAE >15%
  – Good for multi-carrier high PAPR modulated signal too

Measured in Georgia Tech GEMS Lab (Courtesy of Professor Hua Wang)
Modulation Measurement: 1.5Gsym/s (9Gb/s) 64-QAM

High data rate single carrier measurement:
• 9Gbps data rate
• 9.9dBm average power
• High average PAE: 22.4%
• Reasonable EVM: 5.5%

-25.1 dB EVM

Measured in Georgia Tech GEMS Lab (Courtesy of Professor Hua Wang)
Modulation Measurement: 160Msym/s (960Mb/s) 64-QAM

Low data rate single carrier measurement:

- 960Mb/s data rate
- 9.5dBm average power
- High average PAE: 22.4%
- Very good EVM: 3.3%

Measured in Georgia Tech GEMS Lab (Courtesy of Professor Hua Wang)
PA Design: Differential PA

- Higher per element output power required for 4x4 array
- Differential topology is one option to achieve higher output power and maintain high PAE
- Neutralizing capacitors are added in this design
- For differential topology, transformer baluns are used
  - The thick metal option is helpful, especially for output baluns
Transformers Design

- High efficiency output transformer is key to PA $P_{\text{out}}$ and PAE:
  - Dual thick metal and high resistivity substrate can reduce the loss
  - Top thick Al and one thick Cu is used in the primary; the other thick Cu and medium thick Cu is used in the secondary
  - $Q$ is about 24 at 28GHz

- Transformer design options:

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<th>Frlan</th>
<th>Overlay</th>
<th>Concentric</th>
<th>Nested</th>
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<tr>
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<td>Low</td>
<td>Med</td>
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<tr>
<td>Self-Resonant</td>
<td>Med</td>
<td>Low</td>
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<td>Inductance</td>
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<tr>
<td>Type</td>
<td>Non-sym</td>
<td>Depends</td>
<td>Depends</td>
<td>Sym</td>
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Differential PA Layout Extraction Results

- Input balun has about 2% impact to the peak PAE
- Output balun has about 0.5dB impact to Psat and 5% impact to the peak PAE
- PA performance (simulated)
  - 10.5dB power gain
  - 23dBm Psat
  - 34% PAEmax
- Future work:
  - Advanced topologies such as harmonics tuning, Doherty topology can further improve the peak PAE > 40%

![S-Parameter Response](image)

![Harmonic Balance Response](image)
28GHz LNA Design

- Topologies of 1 stage
  - CS
    - Low noise
    - Sensitive to variation, especially $C_{gd}$
  - Cascode
    - High gain
    - Robust to process variation
    - Higher OIP3

- Low noise figure in LNA can extend the communication range, or reduce the PA output power requirement for given range
  - Source degeneration inductor is about 100pH based on matching conditions and also FET $F_t$.
    Limited noise contribution to NF
  - Gate matching inductor (about 700pH in 28GHz LNA design) is a major noise contributor to the LNA:
    about 0.8dB NF
LNA Comparison

- Single stage cascode LNA is evaluated in this study
- Inductors on low resistivity vs high resistivity substrate are compared
  - limited impact on LNA input and output return loss
  - LNA with inductors on low resistivity substrate has lower gain
  - High resistivity substrate has a significant improvement to NF 0.3-0.4dB NF
Summary

• GLOBALFOUNDRIES process options for next wave of mobile data
  • SOI advantages for phased array front end
    – 45nm RFSOI technology with Ft/Fmax > 300GHz/350GHz for mmWave applications
    – FET stacking for improved switch and PA voltage and power handling
    – High resistivity substrate and thick metals for high Q and low loss transmission lines and inductors

• Switch, PA, LNA design examples
  – SPDT switch:
    • Ku band SPDT can provide GaAs comparable performance for satcom/5G applications
    • Ka band SPDT <1dB IL, >1W OP1dB SPDT can meet the 5G UE application requirements
  – Ka band PA:
    • Single-ended PA: Psat > 16dBm, PAE > 40%, >1Gbps data rate single-ended PA is demonstrated which can meet 8X8 or 4X8 phased array requirements
    • Differential PA design: Psat > 23dBm, PAEmax > 34% can meet 2X2, 4X4 array requirements
  – LNA
    • Ka band LNA with < 2dB NF is shown
    • Substrate resistivity shows major impact to LNA NF
    • High resistivity substrate improves NF about 0.3-0.4dB compared with low resistivity substrate
Thank you

Questions?
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