This year’s session on Analog Techniques continues to defy simple categories. This session illustrates the diversity and vigor of modern analog circuitry. The rise of wearable devices and Internet of Things (IoT) leads to the emergence of nano-power designs of references, oscillators and many other blocks. New frontiers of precision, power, and performance are established.

5.1 A 60V Auto-zero and Chopper Operational Amplifier with 800kHz Interleaved Clocks and Input Bias-Current Trimming
Y. Kusuda, Analog Devices, San Jose, CA

Paper 5.1 from Analog Devices presents an auto-zero and chopper operational amplifier with 6.8nV/√Hz PSD in 0.18μm BCDMOS. The chopper op-amp employs 800kHz interleaved clocks, moving the majority of the switching PSD up to 4.8MHz, above the op-amp’s unity gain frequency of 3.2MHz. The maximum input bias current is 200pA. It achieves 152dB CMRR and 1.2V/μs slew rate.

5.2 A 110dB SNR ADC with ±30V Input Common-Mode Range and 8µV Offset for Current Sensing Applications
L. Xu, Delft University of Technology, Delft, The Netherlands

Paper 5.2 by Delft University of Technology presents a ΔΣ ADC with an improved capacitively-coupled high voltage chopper. It achieves ±30V input common-mode voltage range, 110dB SNR and 8µV maximum offset. The sensing AFE consumes 505μW from a 5V supply.

5.3 A 2-Channel -83.2dB Crosstalk 0.061mm^2 CCIA with an Orthogonal Frequency Chopping Technique
Y-L. Tsai, National Taiwan University, Taipei, Taiwan

Paper 5.3 by National Taiwan University presents a continuous two-channel capacitively-coupled instrumentation amplifier using an orthogonal frequency chopping technique and only one active amplifier. It achieves 26nV/√Hz input-referred noise, -83.2dB crosstalk and consumes 27μA from a 3V supply.

5.4 A 32nW Bandgap Reference Voltage Operational from 0.5V Supply for Ultra-Low Power Systems
A. Shrivastava, PsiKick, Charlottesville, VA

Paper 5.4 by PsiKick Inc. presents a 32nW bandgap reference from a 0.5V supply voltage. It achieves 75 ppm/°C over a temperature range of 0 to 80°C and 2% untrimmed 3σ process variation.
5.5 A Forward-Body-Bias Tuned 450MHz Gm-C 3rd-Order Low-Pass Filter in 28nm UTBB FD-SOI with >1dBp IIP3 over a 0.7-to-1V Supply
J. Lechevallier, University of Twente, Enschede, The Netherlands and STMicroelectronics, Crolles, France

Paper 5.5 by University of Twente presents a 450MHz inverter based, 3rd-order Butterworth Gm-C filter in 28nm UTBB FD-SOI technology. The cut-off frequency and filter shape are kept constant over a supply ranging from 0.7V-to-1V, while maintaining linearity above 1dBV without any requirement for Q-tuning and supply voltage tuning. It achieves 6.1nV/√Hz input noise, and dissipates less than 5.6mW.

5.6 A 0.13µm Fully Digital Low-Dropout Regulator with Adaptive Control and Reduced Dynamic Stability for Ultra-Wide Dynamic Range
A. Raychowdhury, Georgia Institute of Technology, Atlanta, GA

Paper 5.6 by Georgia Institute of Technology presents a fully digital LDO that uses adaptive control and fine grained clock gating to enable >90% current efficiency across a 50× load current range. The design also introduces a technique to enable 8× reduction in transient time in response to large voltage droops.

5.7 A 29nW Bandgap Reference Circuit
J. M. Lee, Pohang University of Science and Technology, Pohang, Korea

Paper 5.7 by Pohang University of Science and Technology presents a bandgap reference circuit with a PTAT generated by leakage current. No start-up circuit is needed. The BGR is fabricated in 0.35µm CMOS and consumes 29nW from a 1.4V supply.

5.8 A Digitally Assisted Single-Point-Calibration CMOS Bandgap Voltage Reference with a 3σ Inaccuracy of ±0.08% for Fuel-Gauge Applications
G. Maderbacher, Infineon Technologies, Villach, Austria

Paper 5.8 by Infineon Technology presents a digitally assisted single-point-trim CMOS bandgap reference. The key idea is to keep the analog bandgap core simple and only compensate non-PTAT related effects by using chopping techniques. A 3σ inaccuracy of ±0.08% from -40°C to +120°C is achieved. The temperature drift is 7ppm/°C.

5.9 A 37µW Dual-Mode Crystal Oscillator for Single-Crystal Radios
D. Griffith, Texas Instruments, Dallas, TX

Paper 5.9 by Texas Instruments presents a 24MHz crystal oscillator and a 31.25kHz derived sleep timer for a single crystal wireless node application. A dedicated state machine enables mode transitions without losing clock pulses. It achieves 9ppm/V of frequency variation with voltage and consumes 37µW in sleep mode.

5.10 A 4.7MHz 53µW Fully Differential CMOS Reference Clock Oscillator with -22dB Worst-Case PSNR for Miniaturized SoCs
J. Lee, Institute of Microelectronics, Singapore, Singapore

Paper 5.10 by Institute of Microelectronics Singapore presents a 4.7MHz CMOS reference clock oscillator for SoCs with severely digital noise contaminated supply and ground. It employs a fully differential supply- and ground-regulating frequency-locked loop architecture, a differential period detector with a supply-insensitive period reference, and a differential integrator generating a virtual 0V reference. It achieves a worst-case power supply noise rejection of -22dB and consumes 53µW from a 1.4V supply.
5.1 A 60V Auto-zero and Chopper Operational Amplifier with 800kHz Interleaved Clocks and Input Bias-Current Trimming

Yoshinori Kusuda
Analog Devices, San Jose, CA

Precision operational amplifiers (opamp) with 30V supply operation have been widely used to support industrial, instrumentation, and other applications [1]. Most of them have been realized with BJTs or JFET processes [1] to offer voltage noise PSD better than 10nV/√Hz and offset voltage drift better than 1μV/°C. Recently, opamps with similar specifications have become available using CMOS based processes [2-4], which can offer a cheaper wafer price. Auto-zeroing and/or chopping are used as essential techniques to reduce offset voltage drift and 1/f noise associated with CMOS input differential pairs. The switching action of those techniques, however, results in unwanted output ripples and glitches, which requires a post-filter and limits usable signal bandwidth. Increasing the switching frequency can extend the usable signal bandwidth, though it introduces DC errors such as offset voltage drift and input bias current. Maximum offset voltage drift of 0.025μV/°C and an input bias current of 600pA have been achieved [3], although the switching frequency at 60kHz limits the usable signal bandwidth. A high switching frequency of 333kHz has been achieved [2], while the maximum offset voltage drift and input bias current are 0.085μV/°C and 850pA, respectively.

This paper presents an auto-zeroed and chopped opamp operating in the 4.5 to 60V supply range using a BCDMOS process based on 0.18μm CMOS technology. It achieves a maximum offset voltage drift of 0.015μV/°C, a noise PSD of 6.8nV/√Hz, and a 3.2MHz unity gain frequency, while dissipating 840μA of current. In addition to reducing modulated chopping ripples by combining auto-zeroing and chopping [5], glitches from the charge injection of input switches are mitigated by employing six parallel input stages with 800kHz interleaved clocks. It moves the majority of switching spectral energy up to 4.8MHz while leaving little spectral energy at 800kHz. Maximum input bias current is reduced from 2nA to 200pA by trimming during post-production testing, using an on-chip charge mismatch compensation circuit.

The auto-zeroed and chopped input transconductance amplifier, Gmmain, is shown in Fig. 5.1.1, together with the timing diagram. It is composed of six identical channels in parallel, each of which is driven by individual and interleaved timing clocks. Each channel goes through pre-charging (PC), auto-zeroing (AZ), chopping (CHOP), and inverting-chop (CHOPB) phases as shown in the timing diagram. In the PC phase, two common mode level shift capacitors, CCM, are connected in between the INP terminal and common mode buffer, CMBUF. The two CCM capacitors become floating voltage sources to provide the main transconductance amplifier, Gmmain, with a 1.6V common mode voltage in later phases, without creating a notch in the signal transfer function discussed in [6]. The AZ phase, the input offset voltage of Gmmain is sampled by auto-zero capacitors, CZA, and nulled by the auto-zero transconductance amplifier, GmAZ, which otherwise results in modulated chopping ripples [5]. The differential output of Gmmain gets connected to the signal path in the CHOP and CHOPB phases, and residual offset error and sampled noise from the AZ phase will be modulated by chopping. In contrast to two ping-pong channels [5], the proposed GmAZ with six channels reduces the power dissipated by auto-zeroing relative to that used for amplifying input signals. Four out of the six channels are in either CHOP or CHOPB phases, and contribute to amplifying the input signals. Meeting target 4.5V and 60V supply and signal bandwidth, the required transconductance value of Gmmain and switch sizes in SWIN be four times smaller than those in [5]. The smaller input switches will create less glitch energy per switching event, but require a post-filter and limits usable signal bandwidth. Increasing the switching frequency at 60kHz limits the usable signal bandwidth. A high switching frequency of 333kHz has been achieved [2], while the maximum offset voltage drift and input bias current are 0.085μV/°C and 850pA, respectively.

Figure 5.1.2 shows the proposed input switching circuit, SWIN, incorporating a charge mismatch compensation circuit. The four input switches (SW+, SW-, SW+I, and SW-I) have unwanted coupling capacitors with mismatch (C1, C2, and C3) that have been intentionally added and are driven by additional inverters and adjustable supply voltages (CVDD_DACP and CVDD_DACN). The compensating input bias current is controlled to be 2(C1+C2+CVDD_DACP-CVDD_DACN), where C1, C2, C3, and C4 are assumed to be equal to C0. The CVDD_DACP and CVDD_DACN are generated based on the CVDD and on 8b trimming code, DTRIM. To determine the polarity, either CVDD_DACP or CVDD_DACN deviates from the CVDD according to the MSB of DTRIM. The magnitude of the deviation is linearly changed with the rest of the bits, and the compensating input bias current will change by about 50pA with one LSB.

The overall opamp diagram is presented in Fig. 5.1.3, including the proposed input switching circuit, SWIN, and the proposed input transconductance amplifier, GmAZ, followed by second and output transconductance amplifiers, Gm2 and Gm3. The DTRIM is provided through a digital interface at post-production testing, after measuring the initial input bias current externally. The code of DTRIM is stored in on-chip fuse memory, which is read at power up. The input common mode regulator, CM-Reg, generates the CVDD and CVSS tracking to input common mode voltage (VCM+1.5V and VCM), to maintain constant charge injection in SWIN. Thanks to input common mode level shifting with the Cap, the Gmmain and GmAZ can be supplied by a regulated 4.2V supply (AVDD). Under those internally regulated supplies, the SWIN, Gmmain, SWOUT, and Gm3 can be made of 5V CMOS devices, which offer better performance and smaller area than 60V DMOS devices. The input RC filter and clamping diodes are added to protect the devices in SWIN and Gmmain against high voltage input transients. The clocks are generated under a regulated 3.6V supply voltage (DVDD), and a clock level shifter is used before the SWIN.

The proposed design is fabricated as a standalone dual opamp in a die size of 1.5x2.1mm2. The opamps are specified and tested under a supply voltage range from 4.5 to 60V, an input common mode range from negative supply rail up to 1.5V below positive supply rail, and temperature range from -40 to 125°C. Tested voltage noise PSD with unity gain configuration is shown in Fig. 5.1.4, achieving a flat 6.8nV/√Hz PSD at lower frequencies. The majority of the switching PSD is moved up to 4.8MHz above the opamp unity gain frequency of 3.2MHz, with the use of the interleaved clocks. A narrow PSD is left at 800kHz due to mismatches among the six channels in GmAZ. The level of this PSD varies for different opamp units as shown in the histogram. Additionally the PSD increases around 1.2MHz due to modulated auto-zero sampling noise. Lastly, noise from the output stage GmAZ shows up around 6.5MHz when the gain of GmAZ decreases, which hides the switching PSD at 4.8MHz. In Fig. 5.1.5, measured input bias current versus input common mode voltage, VCM is shown for 20 opamp units under 30V supply. The two figures are given to compare before and after the trimming, which is done at a single bias condition with 5.5V supply, 2.75V input common mode, and at room temperature. Looking at VCM equal to 15V in the figures, the trimming reduces the maximum input bias current from 500pA to 40pA. It increases up to 110pA when VCM approaches 0V or 28.5V, due to the lack of voltage headroom in the CM-Reg circuit. Raising the temperature to 85°C increases the input bias current to 130pA, mostly due to leakage current from ESD protection devices. Considering the spread in mass production and test error guard band, the maximum specified input bias current will be 200pA, which would have been 2nA without trimming. Other performance metrics are compared with previous work in Fig. 5.1.6.

Acknowledgement: The author gratefully acknowledges the engineering support by the Analog Devices Linear Product Group, including design discussions, verification, chip layout, bench test, and ATE development.

References:
Figure 5.1.1: Input transconductance amplifier, $G_m$, and timing diagram.

Figure 5.1.2: Input switching circuit, $SW_{in}$.

Figure 5.1.3: Overall operational amplifier diagram.

Figure 5.1.4: Voltage noise PSD and histogram of 800kHz noise PSD.

Figure 5.1.5: Input bias current vs. input common mode (before and after trimming).

Figure 5.1.6: Performance comparison with previous work.
Figure 5.1.7: Die micrograph of the proposed 1.5x2.1mm² dual opamp.
5.2 A 110dB SNR ADC with ±30V Input Common-Mode Range and 8µV Offset for Current Sensing Applications

Long Xu1, Burak Gönen1, Qinwen Fan2, Johan H. Huijsing1, Kofi A. A. Makinwa1

1Delft University of Technology, Delft, The Netherlands, 2Maxim Integrated Products, Delft, The Netherlands

This paper presents a high-resolution 110dB SNR ΔΣ ADC that achieves a ±30V input common-mode voltage range (CMVR) while powered from a single 5V supply. This beyond-the-rails capability is obtained by employing a capacitively coupled high-voltage (HV) chopper at the input of a switched-capacitor (SC) ΔΣ ADC. Furthermore, the use of correlated double sampling and system-level chopping results in a maximum offset of 8µV over the full CMVR. In contrast to a recent HV ADC [1], the ADC exhibits 30dB more resolution, while its CMVR extends below the negative rail.

The ADC is intended for current monitoring applications, in which a small voltage drop across a shunt resistor must be digitized. In battery monitoring applications, or when inductive loads are involved, the differential voltage across the shunt will often be accompanied by beyond-the-rails common-mode (CM) voltages. Conventionally, current monitoring systems consist of a precision current sensing amplifier (CSA) with a wide CMVR, whose output is then digitized by an ΔΣ ADC [2]. The CSA thus isolates the ADC from large CM voltages, while its gain relaxes the ADC noise requirements. Since the presented ADC itself has beyond-the-rails CM capability together with high resolution, low offset and high gain accuracy, it obviates the need for the CSA, thus reducing the power consumption and the silicon area of the resulting current monitoring system.

Figure 5.2.1 shows the block diagram of the ADC. It consists of a single-loop single-bit 3rd-order SC ΔΣ ADC with a feed-forward architecture based on three OTAs and a SC summing network. An inner set of HV choppers, CH in, together with switches Φ1 and Φ2, implement a correlated double sampling (CDS) scheme that mitigates the offset effect of Φ1 and Φ2. Further offset reduction is obtained with the help of an outer set of HV choppers, CH sys, which, together with a digital chopper at the output of the modulator, implement a system-level chopping scheme. During Φ1, the input signal, \( V_{\text{inp}} \), and the OTA offset are sampled on the 5pF input capacitors, \( C_{\text{in}} \). During Φ2, the HV chopper, \( V_{\text{hvp}} \), reverses the input and thus transfers a charge packet proportional to \( 2C_{\text{in}} \) to the integrator capacitors, \( C_{\text{int}} \). This cross-coupled sampling scheme [3] ensures that the only components exposed to the input CM voltage are the capacitors \( C_{\text{in}} \) and two capacitively coupled HV choppers. The input capacitors are implemented as HV fringe capacitors with a breakdown voltage of 80V. The feedback capacitors are also implemented with the same type of capacitors, to ensure good matching and hence, good gain accuracy.

Figure 5.2.2 shows the schematic of the capacitively-coupled HV chopper, which consists of 4 sampling switches \( MN_{\text{h}} \), one dynamic latch \( MN_{\text{e}} \), three coupling capacitors \( C_{\text{c1}} \) and a minimum selector \( MN_{\text{e2}} \). All the transistors are 5V NMOS devices located in an isolated HV N-Epi pocket (Fig. 5.2.2). The N-Epi pocket is capable of floating up to 65V with regard to the grounded P-Substrate, while the local P-wells can float down to -60V with respect to the N-Epi pocket. Potential latch-up issues associated with the parasitic NPNP structure of the NMOS transistors are circumvented by two measures: 1) The minimum selector prevents the upper NP-diode from conducting, and 2) An HV clamping diode between the positive supply and the floating N-Epi prevents the N-Epi pocket from dropping below the P-Substrate, which means that the lower NP-diode cannot turn on. Protection devices \( MN_{\text{e1}} \) and \( D_{\text{h}} \) restrict the maximum voltage drop across \( MN_{\text{e}} \) to less than 5V, even during fast CM transients. In this way, the HV chopper switches can withstand ±60V input CMVR. In the end, the ADC input CMVR is limited to ±30V by the ESD diodes at the input terminals.

In a previous floating HV chopper [4], the sources of the 4 switches were connected to their P-wells. As a result, the parasitic drain/P-well diodes, \( D_{\text{p1-4}} \), limited the input differential voltage range (DVR) of the chopper to several hundred millivolts. To extend the DVR, a minimum selector, \( MN_{\text{e2}} \), is connected to the chopper input terminals. The circuit ensures that the P-wells of the switches are connected to the input terminal with the lowest input voltage, \( V_{\text{min}} \), thus ensuring that parasitic diodes \( D_{\text{p1-4}} \) are not forward biased.

Each HV chopper is controlled by non-overlapping clock signals Clkp and Clkn, generated by standard 5V logic, which are capacitively coupled to the gates of transistors \( MN_{\text{e1}} \) via capacitors \( C_{\text{c1}} \). In [4], the initial gate voltages of \( MN_{\text{h}} \) are defined by connecting the sources of the latch \( MN_{\text{h}} \) (node A) to one of the input terminals, say \( V_{\text{min}} \). If \( V_{\text{min}} \) is higher than \( V_{\text{hvp}} \) and the differential switch input voltages are larger than the threshold voltages, the switches \( MN_{\text{h}} \) connected to the terminal \( V_{\text{min}} \) will never turn off. To avoid this, node A is connected to the output of a minimum selector so that the clock signals are always superimposed on \( V_{\text{min}} \) (the lower of \( V_{\text{min}} \) and \( V_{\text{hvp}} \)). Due to the cross-coupled sampling scheme, the 4 switches of the HV chopper can share one set of coupling capacitors. Compared to other HV switches [5], this capacitively coupled HV chopper is 3x smaller, occupying only 0.012mm².

Since the coupled clock signals are superimposed on \( V_{\text{min}} \), their amplitude determines the maximum DVR of the chopper switches. This is because the switches can only be turned on if the amplitude of the differential input signal is less than their overdrive voltage. However, it should be noted that the coupled signals at the gates of the switches are slightly attenuated by the parasitic capacitors at nodes B, C. As a result, with 0-to-5V clock signals, the measured linear differential input range of the chopper is about 4.4Vpp.

The first integrator is implemented around a folded-cascode gain-boosting OTA, which achieves 120dB DC gain and draws 40µA. The second and third integrators are scaled down to improve power efficiency. They are built around single-stage folded-cascode OTAs, each of them has a gain of 90dB and draws 5µA. The comparator is composed of a pre-amplifier and a dynamic latch. For flexibility, the decimation is performed by an off-chip 512-tap sinc² filter.

The ΔΣ modulator is realized in an HV 0.18µm CMOS process (Fig. 5.2.7). It has an active area of 0.8mm² and draws 101µA from a 5V supply. The sampling frequency is 150kHz and the signal bandwidth is 100Hz. Figure 5.2.3 gives the 2μs-point output spectrum for a -6.2dB input signal (relative to the 2.8V peak) with an input offset of ±100μV. The first-stage filter has a 15× larger DVR, while maintaining the same input CMVR.

The ADC performance is summarized in Fig. 5.2.6. Compared with [1], the proposed ADC extends the input CM voltage below the negative rail, and achieves a 30dB higher SNR. Furthermore, compared to [4], the improved HV chopper exhibits a 15x larger DVR, while maintaining the same input CMVR.

Acknowledgment:
The authors would like to thank Paul Crolla, Patrick Coady and Rahim Chowdhury from Maxim Integrated Products for their support in the characterization and fabrication of the chips.

References:
Figure 5.2.1: Block and timing diagrams of the 3rd-order ΔΣ ADC.

Figure 5.2.2: Schematic of the HV input chopper and a cross-section of the NMOS devices.

Figure 5.2.3: Measured 222-point FFT of the ΔΣ modulator output (V_{CM}=25V).

Figure 5.2.4: SNR and SNDR versus input amplitude.

Figure 5.2.5: Histograms (15 samples) of the measured offset (with and without system-level chopping) and the relative gain accuracy.

Figure 5.2.6: Performance summary and comparison table.

<table>
<thead>
<tr>
<th></th>
<th>This work</th>
<th>[1]</th>
<th>[2]</th>
</tr>
</thead>
<tbody>
<tr>
<td>Supply voltage</td>
<td>5V</td>
<td>3.3V</td>
<td>2.7V-5.5V</td>
</tr>
<tr>
<td>Input CM range</td>
<td>±30V</td>
<td>0-50V</td>
<td>0-60V</td>
</tr>
<tr>
<td>Input DM range</td>
<td>4.4V_{pp}</td>
<td>30V_{pp}</td>
<td>440mV_{pp}</td>
</tr>
<tr>
<td>SNR</td>
<td>110.1dB</td>
<td>81dB</td>
<td>73.9dB</td>
</tr>
<tr>
<td>SFDR</td>
<td>100.8dB</td>
<td>97.8dB</td>
<td>--</td>
</tr>
<tr>
<td>BW</td>
<td>100Hz</td>
<td>125kHz</td>
<td>500Hz</td>
</tr>
<tr>
<td>Offset</td>
<td>8µV</td>
<td>--</td>
<td>500µV</td>
</tr>
<tr>
<td>CMRR (@DC)</td>
<td>140dB</td>
<td>--</td>
<td>120dB</td>
</tr>
<tr>
<td>PSRR (@DC)</td>
<td>80dB</td>
<td>--</td>
<td>77dB</td>
</tr>
<tr>
<td>Gain accuracy</td>
<td>0.6%</td>
<td>--</td>
<td>--</td>
</tr>
<tr>
<td>Chip area</td>
<td>0.8mm²</td>
<td>0.98 mm²</td>
<td>--</td>
</tr>
<tr>
<td>Power</td>
<td>505µW</td>
<td>4.29mW</td>
<td>4.32mW</td>
</tr>
<tr>
<td>FOM*</td>
<td>163dB</td>
<td>155.6dB</td>
<td>124.6dB</td>
</tr>
</tbody>
</table>

* FOM = SNR + 10 log_{10}(\frac{1}{FOM})
Figure 5.2.7: Chip micrograph.
5.3  A 2-Channel -83.2dB Crosstalk 0.061mm² CCIA with an Orthogonal Frequency Chopping Technique

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Area-efficient low-noise instrumentation amplifiers (IAs) are required in various multi-channel sensing and monitoring applications. These IAs must be designed to achieve low noise and low power, good noise efficiency factor (NEF), good gain matching and low crosstalk among multiple channels [1]. For a continuous sensor array application, each sensor unit is conventionally connected to an individual amplifier for analog signal processing. This configuration consumes large chip area and high power. Furthermore, the quality of gain matching among channels is limited due to the independence of each channel. In [2-3], several multi-channel schemes addressing some of these difficulties are reported. This paper demonstrates a prototype capacitively-coupled IA (CCIA) that adopts an orthogonal frequency chopping (OFC) technique to realize a continuous two-channel CCIA with only one active amplifier, thus saving chip area and power. The whole two-channel CCIA, realized in 0.35μm CMOS, occupies an active area of 0.061mm² (area per channel is 0.0305mm²). This 2-channel IA draws 27μA with channel consuming an equivalent current of 13.5μA.

To verify the effectiveness of the OFC technique, the crosstalk between channels is measured by applying a sinusoidal input signal to channel 1 of the CCIA while the input of channel 2 is kept at the common mode. 10 samples were measured with the input frequency varying from 100Hz to 1kHz. The measured crosstalk (upper left of Fig. 5.3.3) ranges from -79dB to -89dB, with an average of -83.2dB. The upper-right plot of Fig. 5.3.3 shows the measured outputs (overlay plot) when 2 signals at 500Hz and 550Hz are applied to channel 1 and channel 2, respectively. When monitoring channel 2 alone (lower-left of Fig. 5.3.3), the small signal leakage from channel 1 at 500Hz is observed. Comparing these two plots indicates that the crosstalk from channel 1 is -83dB. Similarly, the signal leaking from channel 2 to channel 1 (lower-right of Fig. 5.3.3) is at -92dB, while the signal magnitude is at -11dB; the crosstalk is around -81dB.

The 2-channel CCIA employing the OFC scheme is fabricated in 0.35μm CMOS process technology. The total active area is 0.061mm²; the effective area per channel is 0.0305mm². Operated from a 3V supply, this 2-channel CCIA draws 27μA with each channel consuming an equivalent current of 13.5μA. To verify the effectiveness of the OFC technique, the crosstalk between channels is measured by applying a sinusoidal input signal to channel 1 of the CCIA while the input of channel 2 is kept at the common mode. 10 samples were measured with the input frequency varying from 100Hz to 1kHz. The measured crosstalk (upper left of Fig. 5.3.3) ranges from -79dB to -89dB, with an average of -83.2dB. The upper-right plot of Fig. 5.3.3 shows the measured outputs (overlay plot) when 2 signals at 500Hz and 550Hz are applied to channel 1 and channel 2, respectively. When monitoring channel 2 alone (lower-left of Fig. 5.3.3), the small signal leakage from channel 1 at 500Hz is observed. Comparing these two plots indicates that the crosstalk from channel 1 is -83dB. Similarly, the signal leaking from channel 2 to channel 1 (lower-right of Fig. 5.3.3) is at -92dB, while the signal magnitude is at -11dB; the crosstalk is around -81dB.

The total harmonic distortion (THD) of the CCIA at an input magnitude of 4mVp is dominated by the 3rd harmonic, which is at -67.2dB, as shown in Fig. 5.3.4. Tones at 60Hz with harmonics at 180Hz and 300Hz result from supply line noise. The output noise density, measured by an Agilent 35670A dynamic signal analyzer, is 2.6μV/√Hz (Fig. 5.3.5). With a CCIA gain of 40dB, the input-referred noise density is 26 nV/√Hz. The NEF of the proposed IA is calculated to be 3.74. The measured gain mismatch between channels for a sinusoidal input signal is around 0.55%. CMRR is higher than 110dB and PSRR is better than 103dB up to 1kHz. The experimental results are summarized and compared with state-of-the-art IAs in Fig. 5.3.6. The chip micrograph is shown in Fig. 5.3.7.

Acknowledgement:
The authors thank Y.-Y. Lin and Y.-F. Kuo for valuable discussion, and CIC, Taiwan for chip fabrication. This work is supported by MOST, Taiwan.

References:
Figure 5.3.1: Overall architecture and the concept of the orthogonal frequency chopping technique.

Figure 5.3.2: CCIA with the operational amplifier.

Figure 5.3.3: Crosstalk performance between two channels.

Figure 5.3.4: Measured output harmonic distortion (input magnitude=4mVpp); THD is dominated by the 3rd harmonic tone (-67.2dB). Tones at 180Hz and 300Hz are due to supply line noise.

Figure 5.3.5: Measured output noise PSD and input-referred noise PSD.

Figure 5.3.6: Performance summary and comparison table.

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<tr>
<td>Cheaper (Y/N)</td>
<td>Y</td>
<td>Y</td>
<td>N</td>
<td>Y</td>
<td>Y</td>
</tr>
<tr>
<td>f1 (kHz)</td>
<td>10</td>
<td>200 (100*)</td>
<td>-</td>
<td>500</td>
<td>25</td>
</tr>
<tr>
<td>f2 (kHz)</td>
<td>20</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>-</td>
</tr>
<tr>
<td>Supply Voltage (V)</td>
<td>3</td>
<td>1.8</td>
<td>1.5</td>
<td>1.5</td>
<td>1.2</td>
</tr>
<tr>
<td>Current (µA)</td>
<td>13.5</td>
<td>320</td>
<td>2.6</td>
<td>194</td>
<td>31</td>
</tr>
<tr>
<td>Input Noise PSD (nV/Hz)</td>
<td>25</td>
<td>18.7</td>
<td>26.2**</td>
<td>13.5</td>
<td>40</td>
</tr>
<tr>
<td>CMRR (dB)</td>
<td>110</td>
<td>&gt;99</td>
<td>78</td>
<td>102</td>
<td>116</td>
</tr>
<tr>
<td>PSRR (dB)</td>
<td>103</td>
<td>&gt;102</td>
<td>80</td>
<td>101</td>
<td>108</td>
</tr>
<tr>
<td>Crosstalk (dB)</td>
<td>85.2</td>
<td>73</td>
<td>50</td>
<td>-</td>
<td>-</td>
</tr>
<tr>
<td>Gain Matching (%)</td>
<td>0.55</td>
<td>0.1</td>
<td>7</td>
<td>-</td>
<td>10.7</td>
</tr>
<tr>
<td>NEF</td>
<td>3.74</td>
<td>12.9</td>
<td>1.64</td>
<td>7.2</td>
<td>7.5</td>
</tr>
<tr>
<td>Number of Samples</td>
<td>10</td>
<td>40</td>
<td>N/A</td>
<td>12</td>
<td>8</td>
</tr>
<tr>
<td>Area (mm²)</td>
<td>0.0305</td>
<td>0.035</td>
<td>0.03125</td>
<td>0.06</td>
<td>0.465</td>
</tr>
</tbody>
</table>

*Additional 100Hz clock for DEM
**Equivalent number is calculated from NEF in [3]
Figure 5.3.7: Chip micrograph.
Figure 5.4.1 shows the circuit diagram of the proposed BGR comprising 2× charge pump cells. BJTs transistors Q1 and Q2, capacitors Ca1 and Ca2, and a SC to generate VREF. The output of one 2× charge-pump cell drives Q1 and C1. In the absence of Q2, Vout will charge to 2V in, but Q1 clamps the output voltage to VBE1, which is complementary to absolute temperature (CTAT). Similarly, VEB2 is generated using Q3 and C3, where Q3 is M times Q1. The difference in voltage between VEB1 and VEB2 is ∆VBE, which is proportional to absolute temperature (PTAT) and is stored on C1 (Fig. 5.4.1). The SC scales VEB and ∆VBE by constants a and b to generate the temperature independent BGR voltage, VREF (Fig. 5.4.1). The charge pump circuit configuration with the BJTs enables the low voltage operation of the BGR. The minimum Vref required to generate VEB and ∆VBE is Vref/2 in the circuit of Fig. 5.4.1, which is approximately 375mV, 2× lower than [3].

Figure 5.4.2 shows the switched-capacitor network (SCN) of the BGR circuit. It generates constants for scaling VEB and ∆VBE and then generates VREF using non-overlapping phases of the clock (CLK), φ1 and φ2. In phase φ2 (Fig. 5.4.2), C1 is discharged to ground while the top plates of C2, C3, C4, and C5 are connected to VEB1. The bottom plate of C2 is connected to ground, while the bottom plates of C3, C4, and C5 are connected to VEB1. The voltage across C2 is VEB1, while the voltage across C3, C4, and C5 is ∆VBE. Nodes 3 and 4 are charged to VEB1 in phase φ1, and C1 and C2 are connected together. As C1 was charged to ground and C2 was discharged to VEB1 in phase φ1, the voltage at node 3 in phase φ2 is VEB1-C1/C2+C3. Further, C1, C2, and C3 are connected in series in phase φ2 to generate ∆VBE. The voltage node 4 discharges C1 to a voltage VREF=3∆VBE+VREF+CTAT, where C1 is the capacitor value. The capacitors are selected to set a temperature dependent VREF, accounting for bottom plate parasitics. The load capacitors for VREF generation and the SCN circuit use NMOS capacitors, and the bandgap output and the ∆VBE tripler circuit use MIM capacitors to reduce bottom plate parasitics. Further, C1 has 4× trimming to control process drift.

Figure 5.4.3 shows the clock generation and switching control circuit for the BGR, which must produce dual phase clock signals at a voltage over VREF from a lower VREF. A PTAT current source with high power supply rejection gives a current controlled ring oscillator clock (CLK) of approximately 30kHz at a VREF of 0.5V at approximately 2nW. A clock doubler circuit doubles the swing of the output clocks to enable the SCN switches to pass a VREF voltage level. The output frequency of CLK is 3fV/2VREF, which is inversely proportional to VREF (Fig. 5.4.3), with fV being almost constant with VREF. Since the BGR power consumption increases with VREF, the decreasing frequency of the clock source with increasing VREF keeps the power consumption low. An increase of VREF from 0.5V to 1.5V decreases the period of CLK and the power of the BGR by 2×. CLK is used to generate two non-overlapping clock phases, p and p, that swing from 0 to VREF. Phases p and p are used in the clock doubler circuit to generate signals that swing from 0 to 2VREF (Fig. 5.4.3). The bottom plates of C10 and C11 are connected to the output of inverters driven by p and p, and their top plates are driven by diode connected LFB NMOS devices whose leakage will charge the top plate to VREF in the absence of switching. The bottom plate of C12 and C13 swing from 0 to VREF when switching, and the top plate swings from VREF to 2VREF (Fig. 5.4.3). Next, we convert these signals to full 0-to-2VREF, swing. When p is high, X1 is also high, so φ2 is pulled down to ground. When p is low, X2 is pulled up to VREF and X2 is at 2VREF. The PMOS transistor will turn off and pass the X1 level to φ2, which swings from 0 to 2VREF. Similarly φ2 also swings from 0 to 2VREF with a non-overlapping phase (Fig. 5.4.3).

The proposed BGR targets an output voltage of 500mV. Figure 5.4.4 shows the measured VREF across process, temperature (0°C to 80°C), and VREF (0.5V to 1.5V). The BGR should operate to below 0.4V VREF, but limitations of unrelated circuits on the chip prevent measurement below 0.5V. The measured output voltage from 0°C to 80°C for 6 chips varies from 492mV to 504mV in the absence of trimming (Fig. 5.4.4). After applying one time trimming by changing C11 (Fig. 5.4.2), the output voltage changes from 499.5mV to 504mV. The temperature stability of the BGR circuit varies from 75ppm/°C to 125ppm/°C across 6 chips. The untrimmed output of the BGR achieves a 3× variation of approximately 2% across process at 0.5V VREF and 20°C (Fig. 5.4.4), which can be reduced by trimming C11. Figure 5.4.4 shows that the output varies by approximately 2% for a VREF variation from 0.5V to 1.5V for 6 chips, showing a PSR of -40dB at DC. Clocking two bandgap references, as shown in Fig. 5.4.5, can further reduce the PSR of the BGR. A voltage follower stage buffers the output of the first stage BGR and drives a 2× stage BGR circuit. The lower current consumption of the proposed BGR circuit enables the operation from a lower quiescent current voltage follower stage. The output of the 2× stage BGR, VREF varies by 0.5% for the variation of VREF from 0.55V to 1.5V, showing a PSR of -52dB at DC.

Figure 5.4.5 also shows the BGR power consumption, which is 32nW at 0.5V VREF and 27°C. The current source and ring oscillator consume 10.5nW, so the BGR power consumption could be reduced to 21.5nW with an external clock, if already available in a system. The BGR circuit should function to 0.4V, where it consumes 19.2nW. The power consumption of the cascaded BGR circuit to generate VREF is 71nW, or 52nW with an external clock source. Figure 5.4.5 shows the settling time of the BGR circuit at different VREF to be below 5ms. The ripple on VREF is 50μV at a VREF of 0.5V.

Figure 5.4.6 compares this work with previously reported state-of-the-art low power BGR circuits. The BGR in this work operates at 0.5V, over 1.4× lower than in [2], and the design supports even lower VREF. The BGR consumes 32nW at 0.5V VREF, which is over 1.6× lower than [2]. Further, [3] uses a switched-capacitor BGR circuit to reduce area and achieves lower power by duty cycling, which results in a ripple of 20mV. The ripple of our BGR is due to clock feedthrough and is measured at 50μV at 0.5V VREF. The temperature stability of our BGR is 75ppm/°C from 0°C to 80°C. References [4] and [5] achieve higher temperature stability but consume 600× more power. The PSR of our circuit is -40dB or -52dB at DC in the two design options. Further, conventional lower voltage BGRs [1] require large resistors for low power, which increases area. Our BGR does not use resistors and has an area of 0.0264mm².

The proposed bandgap circuit is implemented in 0.13μm CMOS (Fig. 5.4.7). It improves the power consumption by 1.6× and minimum operating voltage by 1.4× compared to similar work. References:

Figure 5.4.1: Circuit diagram and $V_{BE}$, $\Delta V_{BE}$, and $V_{REF}$ simulations for the bandgap reference circuit.

Figure 5.4.2: Switched-capacitor network circuit used by the BGR to generate a ratio and sum to obtain $V_{REF}$.

Figure 5.4.3: Clock generation and switch control signals used to enable switching for the BGR core circuit.

Figure 5.4.4: Measurement of the variation of BGR circuit across temperature, $V_{IN}$, and process.

Figure 5.4.5: Variation of the BGR voltage, power consumption and settling time with $V_{IN}$.

Figure 5.4.6: Comparison of BGR metrics with other low power, low $V_{IN}$ designs.
Figure 5.4.7: Die micrograph of the bandgap reference circuit.

<table>
<thead>
<tr>
<th>Block</th>
<th>Current [μA]</th>
<th>Power [μW]</th>
</tr>
</thead>
<tbody>
<tr>
<td>Current Source</td>
<td>17.6</td>
<td>86.4</td>
</tr>
<tr>
<td>Ring Oscillator</td>
<td>3.0</td>
<td>1.8</td>
</tr>
<tr>
<td>Clock Doubler</td>
<td>3.0</td>
<td>1.8</td>
</tr>
<tr>
<td>Bandgap Core</td>
<td>9.4</td>
<td>19.0</td>
</tr>
</tbody>
</table>

Area Breakdown

<table>
<thead>
<tr>
<th>Block</th>
<th>Area (μm²)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Current Source</td>
<td>80 x 60</td>
</tr>
<tr>
<td>BJT Q1 and Q2</td>
<td>59 x 90</td>
</tr>
<tr>
<td>SCN</td>
<td>60 x 60</td>
</tr>
</tbody>
</table>
5.5 A Forward-Body-Bias Tuned 450MHz Gm-C 3rd-Order Low-Pass Filter in 28nm UTBB FD-SOI with >1dBVp IIP3 over a 0.7-to-1V Supply

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1University of Twente, Enschede, The Netherlands,
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Due to the absence of internal nodes, inverter-based Gm-C filters [1,2] allow achieving bandwidths beyond what is possible with opamp-RC techniques. The class-AB behavior of the inverter, together with the high transconductance for a given quiescent current, results in a high dynamic range for a given power consumption when optimally biased [3]. The major disadvantage of traditional inverter-based Gm-C filters is that they are tuned with the supply voltage, $V_{DD}$, and hence require a finely controllable supply. Voltage regulators used to accomplish this require a voltage headroom (including margin for tuning) and degrade total power efficiency by tens of percent. In this paper, we show that by exploiting body biasing in an ultra-thin buried oxide (BOX) and body, fully-depleted SOI (UTBB FD-SOI) CMOS technology, we overcome the requirement for a tunable $V_{DS}$ in inverter-based Gm-C filters, while achieving high linearity over a wide supply voltage range.

A cross-section of an UTBB FD-SOI CMOS inverter is shown in Fig. 5.5.1 [4]. The BOX underneath the active devices isolates the drain and sources from the bulk, allowing the transistor body to be used as a back-gate, hence enabling significant threshold voltage ($V_T$) shifts. Low-$V_T$ (LVT) devices in this technology are implemented as ‘flip-well’ transistors, where the NMOS and PMOS devices lay above n- and p-wells, respectively. Due to the BOX isolation, there are no drain- and source-to-bulk parasitic diodes, which limit the maximum forward body bias (FBB) range in bulk technology. For 28nm UTBB FD-SOI LVT transistors, a FBB of up to 3V is allowed. Combined with a higher sensitivity to body bias ($V_{BBB}$) range in bulk technology. For 28nm UTBB FD-SOI LVT transistors, a FBB of up to 3V is allowed. Combined with a higher sensitivity to body bias ($V_{BBB}$) range in bulk technology. For 28nm UTBB FD-SOI LVT transistors, a FBB of up to 3V is allowed. Combined with a higher sensitivity to body bias ($V_{BBB}$), the NMOS and PMOS devices can be kept constant over hundreds of mV supply range, hence compensating for supply voltage variations. Alternatively, FBB can be used to tune the transconductors. Body biasing requires negligible current (<1nA), consisting only of leakage currents of reverse-biased diodes.

Illustrated in the bottom left plot of Fig. 5.5.1 is the change in the Gm curve of a differential CMOS inverter over $V_{DS}$ variations. Without body biasing, Gm changes and linearity is degraded. For high $V_{DS}$, the inverter behavior is compressive (mobility reduction), while for low $V_{DS}$ it is expansive (exponential range). Only one $V_{DS}$ results in a flat Gm-curve, which means that it produces little 3rd-order distortion. Body biasing can be applied to tune Gm back to its nominal value over different $V_{DS}$, without linearity degradation, as illustrated in the bottom right plot of Fig. 5.5.1. We apply this technique to a low-pass (LP) Gm-C filter to keep the cut-off frequency ($f_c$) constant and to guarantee high linearity over a 300nm supply voltage range. Local supply decoupling is still required, but the separate voltage regulator can be omitted. Without this technique, the same supply variation would have shifted the cut-off frequency between 110 and 650MHz and degraded IIP3 by more than 10dB.

The LP filter topology shown in Fig. 5.5.2 is derived from a 3rd-order, doubly terminated Butterworth LC ladder prototype using gyrator synthesis [1]. The transconductors and MOM capacitors are sized for a nominal $V_{DD}$ of 450MHz. The use of 110nm gate lengths in 28nm UTBB FD-SOI technology makes the transconductor output resistance sufficiently constant to be compensated by a fixed negative resistance, eliminating the need for $Q$-tuning as used in previous designs [1,2,5]. The increased MOSFET parasitic capacitors are absorbed in the filter capacitances. The common-mode loop gain must be kept below unity, which is accomplished by inverters gm1 and gm2 [1]. We choose $gm_1 = 0.350gm_0$ and $gm_2 = 0.325gm$, to minimize noise and power consumption, while still ensuring common-mode stability and output resistance cancellation [2].

As shown in Fig. 5.5.2, all NMOS and PMOS devices are body biased by VBBN (biased from 0 to 3V) and VBBP (biased from 0 to -3V) respectively. Impedance up-scaling by a factor of 2 is applied to the last nodes (N3) to achieve unity gain overall, while reducing power consumption. To measure the filter in a 50Ω environment, inverter buffers are added at the filter output, and 50Ω resistors terminate the input and output. A reference path is integrated on chip to enable de-embedding of the filter core [1]. The chip, of which a micrograph is shown in Fig. 5.5.7, is integrated in STMicroelectronics 28nm UTBB FD-SOI technology. The filter core occupies 0.04mm², of which 0.03mm² are filter capacitors.

The S-parameters of the filter path, reference path and PCB crosstalk were measured, from which the transfer function of the filter core was de-embedded. Using FBB tuning, the filter Fc is kept constant at 450MHz for a $V_{BBB}$, varying from 0.7 to 1V. Figure 5.5.3 shows the measured filter transfer function. This figure also shows another tuning strategy where $V_{BBB}$ is fixed at 0.9V, and Fc is varied between 190MHz and 900MHz using FBB tuning between 0 and 3V.

The 3rd-order intermodulation distortion of the filter path, including output buffers, is measured with 2 in-band tones at 300±0.5MHz. Figure 5.5.4 shows the IIP3 for different $V_{DD}$, where VBBP and VBBN are varied, showing that the IIP3 can be maximized for every supply level. Figure 5.5.5 shows the IM3 and fundamental against input power when Fc is tuned to 450MHz, for different $V_{DD}$ values. These curves extrapolate to an IIP3 above 1.2dBVp. The 1dB compression point was measured by sweeping the power of a single 300MHz tone, and varies between -10.3 and -4.8dBVp. The input noise power spectral density (PSD) of the de-embedded filter core is approximately 6nV/√Hz, and power consumption varies between 4mW and 6.5mW over the 0.7–1V supply range.

The filter performance is summarized and compared to four other recent Gm-C filters with a cut-off frequency above 100MHz in Fig. 5.5.6. Three key performance figures (noise, linearity and power consumption) can be easily traded against each other; the noise PSD can be reduced by impedance scaling at the expense of a proportional increase in power consumption [3], while linearity can be improved at the expense of noise by attenuating the input, keeping the dynamic range the same. To allow comparison of the different circuits, taking these design freedoms into account, we calculate their normalized signal-to-noise ratio (NSNR) in the last row of Fig. 5.5.6 [3]. Compared to previous work this design achieves a higher linearity, or a lower noise level and lower power consumption. Compared to the most similar filter in [2] this work obtains over 3dB higher SFDR at lower power consumption, while not needing a regulated supply. The SFDR of this design is 3dB lower than [7], yet consumes 12 times less power. This performance is maintained over a 0.7–1V supply range.

This paper has demonstrated that the extended body biasing range in UTBB FD-SOI, applied to an inverter-based Gm-C filter, can save a significant amount of power while accommodating supply voltage variations, without performance degradation and with competitive linearity.

Acknowledgments:
The authors thank Nicolas Rolland and Pierre Dautriche from ST Microelectronics for enabling this research.

References:
Figure 5.5.1: Inverter cross section with typical Gm curves.

Figure 5.5.2: Chip schematic.

Figure 5.5.3: De-embedded transfer function.

Figure 5.5.4: IIP3 versus forward body bias, for different supplies.

Figure 5.5.5: IIP3 and gain compression.

Figure 5.5.6: Performance summary and comparison.
Figure 5.5.7: Chip micrograph.
A 0.13µm Fully Digital Low-Dropout Regulator with Adaptive Control and Reduced Dynamic Stability for Ultra-Wide Dynamic Range

Saad Bin Nasir, Samantak Gangopadhyay, Arijit Raychowdhury

Georgia Institute of Technology, Atlanta, GA

An increasing number of power domains and of power states per domain, as well as decreasing decoupling capacitance per local grid and ultra-wide current dynamic range of digital load circuits (for low power on one end while maintaining performance at another) necessitate the design of high-efficiency, compact on-die voltage regulators providing ultra-fine grained spatio-temporal voltage distribution [1,2]. Digitally implementable linear regulators operated in low-dropout (LDO) mode, based on continuous time or discrete time control, exhibit process and voltage scalability [3-5], thus supplementing their analog counterparts [6].

This paper presents a discrete-time, fully digital, scan-programmable LDO macro in 0.13µm technology featuring greater than 90% current efficiency across a 50× current range, and 8× improvement in transient response time in response to large load steps. The baseline design (Fig. 5.6.1) features a 128b barrel shifter that digitally controls 128 identical power PMOS devices to provide load and line regulation at the node VREF for a scan-programmable fine-grained synthetic load. A clocked comparator, which eliminates the need for any bias current, controls the direction of shift, D. The programmable mux-select signals, MUX1 and MUX2, provide controllable closed loop gains, KBARREL, of 1 to 3×. Since at any clock edge only 1, 2 or 3 shifts can occur (depending on the gain setting), fine-grained clock gating is enabled by dividing the 128b shifter into four sections and only enabling the clock to the section(s) where the shift occurs (Fig. 5.6.1).

A linearized hybrid control model of the LDO (Fig. 5.6.2) reveals two open loop poles: 1) An integrator pole at z=1, and 2) At z=e\(^{-FLOAD/FS}\) where FLOAD is the equivalent output pole (FLOAD = 1/(RCLOAD(RS+LDS(CLOAD+G))). For a given sampling frequency of the discrete time controller. With ultra-wide dynamic ranges of the load current, RLOAD changes, often over two orders of magnitude; hence the open loop poles (and equivalent closed loop poles) of the regulator span a large range (Fig. 5.6.2). Consequently at iso-Fp heavy load conditions show an over-damped response, whereas light load conditions become under-damped and even oscillatory. To cater to a wide load range, we provide adaptive control such that FLOAD/Fp is bounded. This results in a more consistent transient response and, by scaling Fp with FLOAD (and hence ILOAD), the current efficiency of the LDO is vastly improved. In the present design, a slower control loop checks for the status of bit-45, and bit-85 of the barrel shifter. Bit-45=1 and bit-85=1 indicates that both PMOS devices are off and hence light load conditions exist. Similarly, 01 and 00 represent nominal and heavy load conditions. When the Q-point point of the load changes and a heavy, nominal or light load condition is identified, an adaptive controller waits for an incubation period (which eliminates chattering between multiple frequency-modes) and sets Fp to FHIGH, FLOW or FLOW. The incubation period is programmable and is realized using an externally clocked binary counter, enabling Fp adjustment only when the counter saturates. When operating in regulation, with small load transients, the autonomous choice of Fp results in decreased ringing, faster settling and close tracking of the controller current, Ic, with ILOAD.

Along with adaptive control for efficient regulation across a wide dynamic range, we propose a programmable and digitally implementable “variable structure control” that facilitates fast recovery from large voltage droops, in response to large load steps. These are infrequent, often triggered by changes in the power state of the system. This design principle, referred to as Reduced Dynamic Stability (RDS) and borrowed from the control design of military aircrafts, exhibits an ultra-fast transient response without compromising static stability. This is accomplished by retiming the baseline design with overshoot and droop detectors that compare VR and VREF+Δ (Fig. 5.6.3). Once such a droop/overshoot is detected, the regulator selects a fast clock (FTRANSIENT=400MHz), which will instantaneously render the loop marginally stable by moving the open (and hence closed) loop poles very close to |z|=1. Further, the barrel shifter gain can be simultaneously increased to further reduce the stability margin of the loop. This enables a faster recovery from load transients. As soon as VR returns close to regulation (VR > VREF > VREF+Δ), the RDS logic switches back to the sampling clock Fp, allowing a stable return to regulation without any ringing. The current design supports externally programmable Δ and measurements support a provably stable response for Δ = 50 or 100mV.

The LDO macro is measured across a wide range of operating conditions and the Shmoo plot (Fig. 5.6.4) illustrates VR at 0.45 to 1.15V with the line voltage, VLOAD, from 0.5 to 1.2V, thus revealing (a) a minimum dropout of 50mV and (b) near threshold operation (process Vt ∼ 300mV). Oscilloscope capture of a transient measurement shows: 1) Regulation under Q-point changes; 2) Ripple of less than 3%, and 3) Autonomous adaptation of Fp in response to load changes. Scope captures also show baseline design (RDS off) vs. proposed design (RDS on) and reveal decreased settling time (TS) when RDS is enabled.

The settling time for small current transients (Fig. 5.6.5) reveals a strong dependence of Fp on ILOAD and hence FLOAD, further motivating the use of dynamically adaptive Fp under different load conditions to meet a Ts specification. A color-map provides the autonomous and dynamic allocation of FHIGH, FLOW and FLOW for varying ILOAD, ILOAD and VLOAD to meet a target Ts. Measurements are carried out on the baseline and proposed design (with RDS) for voltage droops >100mV. The baseline design, with ILOAD = 0.7mA and ΔLOAD=1.2mA, shows an initial decrease in Ts with Fp as the system becomes critically damped, and an eventual increase in Ts with Fs as the system becomes under-damped and exhibits ringing and slower settling. The proposed design with RDS enabled (for FBARREL=1 and 3) shows >8× improvement in Ts. Faster response also reduces Vd but in response to the same load step and 36% (60%) reduction of Vd is observed for Ts of 2.1mA (0.7mA). Load regulation for a range of VLOAD voltages shows an average of 6mV/mA and a worst case of 10mV/mA. We also note a 50× load range, which can be further scaled if a larger barrel-shifter and power MOSFETs are used. By enabling fine-grained clock gating, 34% reduction of controller power, Pctl, is measured. As adaptation to Q-point, due to dc changes in ILOAD, is enabled for the wide load current range, we note Fp adjusting for high, nominal and light loads, thereby providing high current efficiency across the entire load range while meeting a target Ts specification. A 4× improvement in current efficiency is measured at light load conditions when compared to the baseline design (Fig. 5.6.6). A comparative study with recently published data establishes that the current design (Fig. 5.6.7) is competitive in both power efficiency and performance. Adaptive control enables an energy-efficient wide dynamic range. A power efficiency figure of merit (FOM1), defined as the average current efficiency across a load range from FLOW to FHIGH, is 90%, compared to the FOM2 for a proportional design (with RDS) which enables a dynamic trade-off between instantaneous stability and transient response, provides ultra-fast Ts with a discrete time digital loop without compromising the runtime stability. FOM2 [2], normalized to the process node, shows that the performance is comparable to its analog counterpart [6].

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References:


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Figure 5.6.1: Fully digital low-dropout regulator with digitally programmable loop gain and fine-grained clock gating.

Figure 5.6.2: Autonomous adaptation of sampling frequency (F_s) across a wide dynamic range.

Figure 5.6.3: Droop and overshoot detectors detect large load transients. In response, a faster sampling clock and higher loop gain are enabled for faster recovery from droops and overshoots.

Figure 5.6.4: Measured operating range of the LDO with representative scope captures.

Figure 5.6.5: Measured settling time, T_s, for small droops with adaptation for autonomous choice of F_s. RDS allows 8× improvement in T_s for large load transients and 36% to 60% reduction in V_DROP.

Figure 5.6.6: Measured load regulation, current efficiency and performance summary.
Figure 5.6.7: Chip micrograph, process and design specifications.

<table>
<thead>
<tr>
<th>Specification</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Process</td>
<td>IBM 130nm CMOS 8-M</td>
</tr>
<tr>
<td>Total Area</td>
<td>2 mm²</td>
</tr>
<tr>
<td>Active Area</td>
<td>0.3552 mm²</td>
</tr>
<tr>
<td>LDO Area</td>
<td>0.114 mm²</td>
</tr>
<tr>
<td>Testing Interface</td>
<td>QFN Package</td>
</tr>
</tbody>
</table>
5.7 A 29nW Bandgap Reference Circuit

Jong Mi Lee¹, Youngwoo Ji², Seungnam Choi³, Young-Chul Cho³, Seong-Jin Jang⁴, Joo Sun Choi³, Byungsub Kim³, Hong-June Park⁴, Jae-Yoon Sim⁵

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Bandgap references (BGRs) are widely used to generate a temperature-insensitive reference voltage determined by the silicon bandgap. The BGR generally utilizes PN diodes to generate both of proportional-to-absolute-temperature (PTAT) and complementary-to-absolute-temperature (CTAT) quantities and combines them to eliminate the temperature dependence. Though the BGR provides a robust voltage or current reference with insensitivity to process, voltage and temperature variations that is superior to CMOS-only reference circuits, it has received little attention in ultra-low-power (ULP) sensor applications. While CMOS-only reference circuits have recently demonstrated nanowatt power consumption [1], BGR approaches still have two critical factors to preventing nanowatt consumption. One is that PTAT generation assumes sufficient forward bias, VS, of the PN junction to allow e(eV+VT)/kT which must always flow, to represent the ideality factor and the thermal voltage, respectively. In addition, the PTAT generation requires a start-up circuit to prevent the circuit from resting at the undesirable zero-bias condition. Since the start-up circuit utilizes a resistive voltage division between power rails, it consumes non-zero DC current, which must be larger than leakage current in order to ensure stable start-up operation. These two requirements for PTAT generation limit the use of BGRs in nanowatt ULP applications.

Recently, a sample-and-hold scheme with duty cycling was applied to a BGR circuit and achieved a power consumption of a few nanowatts [2]. However, it uses a traditional BGR core and does not reduce the power consumption of the BGR circuit itself when it is turned on. Therefore, further reduction of power consumption would be achieved if a similar sample-and-hold scheme were used to implement a PN diode, providing a CTAT voltage. The voltage reference, Vref, is copied by an opamp, drawing PTAT current through resistors. The opamp has a reasonable current level, which should be much larger than the gate leakage current, in order to ensure stable start-up operation.

This paper proposes a BGR with a leakage based PTAT. Without any start-up circuit, duty-cycling, or assumption of strong forward bias for the PTAT, the fabricated BGR in 0.35μm CMOS consumes 29nW at room temperature and shows a temperature coefficient of 12.75ppm/C with a line regulation of 0.198%/V. Figure 5.7.1 shows the proposed concept of two-diode PTAT generation. The two diodes are identical except for a multiplication factor, L, determined by the ratio of the numbers of identical diodes used at pull-up and pull-down sides. The diodes are connected in series between power rails with the upper diode reverse biased. Then, only leakage current, Igs, flows through the branch, where Is represents the reverse saturation current. The intermediate node voltage becomes PTAT, nV Tln(L+1), without the assumption of enough forward bias of the lower diode to guarantee that e(IV+V0)/kT is much larger than 1. In addition, since this circuit utilizes the leakage current, which always flows, there is no need of a start-up circuit. Therefore, the proposed scheme dramatically reduces the current consumption for PTAT generation which has been a major cause of power consumption in the conventional BGR. This concept of two-diode PTAT generation can be also extended to use other diodes if they are identical. Replacement of PN diodes with MOS diodes also results in PTAT generation. The MOS current equation in the sub-threshold region is Isub=μCox(W/L)(m-1)VT/V0m(VT+VGS/2m)1-m/2, where m is the inverse of the gate-to-surface coupling coefficient. The intermediate node voltage can be derived to be mVTln(L), resulting in a PTAT voltage. Recently, this MOS version of PTAT generation was adopted in the design of a temperature sensor [5]. This work generalizes the design of the PTAT with two identical diodes and extends it to form an ultra-low-power BGR circuit.

Note that conventional BGR circuits take the diode voltage for CTAT while the difference between two CTATs becomes PTAT. In the proposed scheme, the PTAT is directly taken from the diode voltage. Therefore, the current for PTAT generation increases exponentially as temperature changes and could range from 1A to nA. The PTAT generated by drawing too little current at low temperatures can be affected by unwanted gate leakage current from circuits to be connected to the PTAT node because the gate leakage has less dependence on temperature. Simulated current for PTAT generation is shown in Fig. 5.7.1. Assuming that the two versions are implemented in the same area, the PN and MOS diode versions consume 30A and 60A at room temperature, respectively, while they consume 2nA and 13nA at 120°C. The larger current variation in the PN version is due to stronger temperature dependency of Is. In this work, the MOS diode version is used considering the layout area and reasonable current level, which should be much larger than the gate leakage current given by the process technology.

Figure 5.7.2 shows the circuit schematic of the proposed BGR. The PTAT voltage is copied by an opamp, drawing PTAT current through resistors. The opamp has a source-follower-based level shifter followed by an NMOS differential pair at the input stage to receive low PTAT voltage. Total current consumption for the opamp is less than 1nA at room temperature. The total power consumption of the BGR is dominated (> 99% at room temperature) by the current through resistors, and can be reduced by increasing the resistance at the cost of area. A lateral NPN BJT (Fig. 5.7.3) with twin-well technology is stacked on the resistors to implement a PN diode, providing a CTAT voltage. The voltage reference, Vref, can be derived as (1+R2/R1)VPTAT+VCTAT, eliminating the temperature dependency by adjustment of the ratio between R1 and R2.

The designed BGR circuit is fabricated using a 0.35μm CMOS process. The measured temperature coefficient (TC) is 12.75ppm/C when temperature changes from -10°C to 110°C. Figure 5.7.4 shows measured reference voltages from 10 chips. The standard deviation is 2.36mV at 20°C, revealing a μσ of 0.2%. Figure 5.7.5 shows the measured reference voltage when supply voltage varies. The reference voltage increases by 2.3mV as the supply voltage increases by 1V, showing a line regulation of 0.198%/V. Current consumption is also measured as temperature changes. The total current linearly increases up to 60°C, revealing that the current through the resistors is dominant while the leakage current for PTAT generation and opamp operation is negligible. The BGR circuit consumes 28.7nW from a 1.4V supply voltage at room temperature. Above 60°C, the exponentially increasing leakage current starts to appear as a comparable contributor to the total power consumption. Figure 5.7.6 summarizes the performance and compares it with previously reported state-of-the-art BGR circuits.

Acknowledgements:
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References:
Figure 5.7.1: Proposed concept of two-diode PTAT generation using leakage current.

Figure 5.7.2: Proposed bandgap voltage reference circuit.

Figure 5.7.3: Structure of lateral NPN BJT for CTAT.

Figure 5.7.4: Measured reference voltage from 10 chips and distribution of the reference voltages at 20°C.

Figure 5.7.5: Measured line regulation and current consumption.

Figure 5.7.6: Performance summary and comparison with previous works.
Figure 5.7.7: Chip micrograph.
5.8 A Digitally Assisted Single-Point-Calibration CMOS Bandgap Voltage Reference with a 3σ Inaccuracy of ±0.08% for Fuel-Gauge Applications

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Accurate voltage references are key building blocks for almost all electronic systems. Specifically, fuel gauge applications benefit from very high precision references to allow for extremely precise measurement of battery voltage and current in order to provide an accurate measurement of the state of charge of the battery.

In this work a digitally assisted single-point-trimmed CMOS bandgap voltage reference is presented. Compared to previous art [1-4], this work achieves a low inaccuracy of ±0.08% (3σ) from -40°C to +120°C. The residual temperature drift is as low as 7 ppm/°C. The key idea is to keep the analog bandgap core simple and only compensate non-PTAT related effects (like offset) by using chopping techniques. The remaining PTAT and chip-to-chip variations can then be cancelled out using a single-point trim. Compared to [1], this work avoids the need for a bulky analog notch filter by minimizing offset using a DAC and a simple digital calibration loop. Finally, the remaining curvature, temperature drift, and stress effects are compensated in the digital domain by means of a temperature sensor, a stress sensor and a lookup table (LUT). In summary, the high precision of the reference voltage is achieved by reducing the analog portion to a minimum and combining this with digital compensation. As a consequence, the analog output voltage of the reference is not fully compensated (but also not needed in our system).

Figure 5.8.1 shows a system overview of the voltage reference in the context of a fuel gauge system. The core of the reference is a CMOS bandgap circuit providing an analog reference voltage, $V_{BG}$. This voltage is used as reference for the high accuracy ΣΔ-ADC [5], which measures the battery cell voltage (or current via a shunt resistor). Since $V_{BG}$ is compensated for non-PTAT errors only, the remaining error also affects the uncorrected ADC result in the digital domain. Here the remaining errors are compensated using a LUT, which is based on correction values from the measured $V_{BG}$ at room temperature (single-point trim). In addition, the LUT is used to provide curvature correction, since this effect is quite stable for devices in a given technology [7]. During calibration, the analog $V_{BG}$ output is passed via a 1-σ order lowpass filter to an on-chip chopped buffer (not shown) to provide a low impedance signal source to the tester. The temperature is measured by an on-chip temperature sensor with ±0.5°C accuracy. Finally, stress effects caused by packaging or aging are compensated for by using a stress sensor [6] and calculating the final corrected ADC result used by the fuel gauge algorithms. Combining all of these techniques, a single-point calibration at wafer level is sufficient to achieve the required accuracy of the overall system.

Figure 5.8.2 shows a block diagram of the used bandgap subsystem. PNP transistors Q1 and Q2 and resistors R1, R2, and R3 form a classical bandgap structure. The common node of the core is driven by $V_{th}$, which is in common source configuration. With this simple topology the bandgap voltage errors caused by mismatch in the core are of 1st-order PTAT type (excluding curvature, corrected afterwards in the LUT). Therefore the error can be removed by a single room temperature trim, since PTAT errors rotate $V_{BG}$ around 0 Kelvin. Only the base resistance mismatch and the current gain mismatch of the bipolar transistors Q1 and Q2 are not PTAT type but their error contribution is quite low [1].

A chopped system is used to remove the offset of the error OTA. This is very important since such an offset would contribute significant error, which would be non-PTAT type. Additionally, the voltage ripple in the loop is used to get the information about the offset of the error OTA. An auto-zeroing comparator with 3 gain stages detects the polarity of the voltage ripple. The comparator is designed to detect voltage ripples down to 100μV. The output information of the comparator is used in a state machine to drive a DAC with current output that compensates for the offset in the error OTA. Once the voltage ripple has been minimized it is possible to disable the comparator in order to reduce power consumption. Additionally this concept also allows chopping to be disabled since the offset of the error OTA is already minimized. The benefit is that the voltage ripple at the reference voltage, $V_{BG}$, is not increased by the chopping process (only short-term during calibration). The chopped error OTA with offset tuning capability is shown in Fig. 5.8.3. The offset of the OTA caused by the differential input pair $M_{h}$ and $M_{l}$ and the current mirror $M_{h}$ and $M_{l}$ can be compensated by the digitally programmable currents $I_{trim1}$ and $I_{trim2}$. For instance if $V_{thM1} > V_{thM2}$, the generated offset can be reduced by setting $I_{trim1}$ larger than $I_{trim2}$. Then, the voltage drop on the resistor $R_{v}$ would be larger than the drop on $R_{w}$, which will change the current mirror ratio of $M_{h}$ and $M_{l}$ due to different source node voltages of the transistors. The trimmed currents are generated by the digitally controlled differential pair $M_{h}$ and $M_{l}$.

Figure 5.8.4 shows the simulation results of 120 transient Monte Carlo runs. There is high correlation between $V_{BG}$ at 25°C and the temperature coefficient (TC) over process variations, which means that the major remaining errors are clearly PTAT type. Therefore, the result of the bandgap voltage measurement at 25°C can be used to predict the TC of the bandgap. For example, if the measured $V_{BG}$ at 25°C is 1.225V, the resulting TC equals 48ppm/°C. This value can be stored in a LUT and can be used to compensate the digital reference voltage. After obtaining the PTAT correction factor, the remaining error is dominated by bandgap curvature and nonlinear temperature dependence. Since at 1st-order these effects are stable for a given technology, they also can be corrected digitally by adapting the LUT values accordingly.

A third step in the correction process is to handle mechanical stress effects. Plastic packaging can be a significant source of stress, causing additional error between wafer-level and package measurements. Therefore a stress sensor is implemented to allow calibration at wafer-level, which is much less time consuming than in packaged samples, thus significantly saving production cost [6].

The reference circuit is fabricated as part of a fuel gauge chip of the Infineon Oria™ product family in a 0.13μm CMOS technology. The active area of the bandgap (excluding the ADC, digital core, temperature sensor and stress sensor) is 0.034mm². All resistors are of standard polysilicon type, transistors are standard 1.5V core devices.

Lab measurements on ceramic samples are shown in Fig. 5.8.5. The upper graph shows the relative bandgap voltage after single-point trim. The typical bandgap curvature, as well as PTAT mismatch between the samples is clearly visible. After applying the PTAT and curvature correction, the residual error is shown in the lower graph. The temperature drift (box method) is 7ppm/°C over the -40 to 120°C temperature range.

Figure 5.8.6 shows production tester (wafer level) results of $V_{BG}$ after digital correction for two different temperatures (0°C for 100 samples, 60°C for 4500 samples). The inaccuracy is below ±0.055% (3σ). The reduced temperature range of 0 to 60°C is chosen to fit the fuel gauge application. The stress sensor was measured in the lab on plastic packaged samples. The results show a high correlation between the stress sensor output voltage and $V_{BG}$ voltage under stress conditions over different samples. Consequently, an additional trim at the package level is no longer needed.

The resulting inaccuracy corresponds to a state of charge error of below 1% for a typical LiPo battery, which is well within requirements and allows accurate calculation of battery lifetime parameters.

References:
Figure 5.8.1: Overview of fuel gauge voltage reference system.

Figure 5.8.2: Bandgap subsystem, including bandgap core, chopped OTA, and offset cancellation loop.

Figure 5.8.3: Chopped OTA with offset tuning capability.

Figure 5.8.4: Simulated PTAT behavior (transient monte carlo, 120 runs) shows high correlation between $V_{BG}$ at 25°C and temperature coefficient (TC) over process variation, thus allowing accurate single-point trim.

Figure 5.8.5: Lab measurements on 13 packaged ceramic samples of relative bandgap voltage after single point trim (upper) and residual error after digital correction (lower graph). Inaccuracy is below $\pm 0.08\%$ ($3\sigma$). Temperature drift (box method) is 7ppm/°C.

Figure 5.8.6: Measured inaccuracy on production tester (wafer level) for 2 different temperatures (0°C for 100 samples, 60°C for 4500 samples) is below $\pm 0.055\%$ ($3\sigma$). This temperature range is the specified range for the fuel gauge application.
Figure 5.8.7: Testchip micrograph.
A 37µW Dual-Mode Crystal Oscillator for Single-Crystal Radios

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The emerging Internet of Things (IoT) market is fueled by reductions in power, cost and size of wireless sensors. Wireless nodes reduce average power by using intermittent data transmission, which is synchronized by a continuously operating sleep timer in each node. In some applications, such as disposable sensors, low cost and small physical size are more important than achieving the lowest possible power consumption. Crystal cost and size is a limitation, particularly because each node requires two crystals. The first crystal, in the MHz range, is used to generate the PLL reference clock. The second crystal, usually 32.768kHz, is used to generate an accurate sleep timer used for synchronizing data transmission. A radio SoC may occupy 4x4mm² board area while a standard size for each crystal is 3.2x2.5mm². Therefore, the size of the crystals can be larger than the SoC itself, limiting the applications.

The power profile for a wireless node with synchronized data transmission is shown in Fig. 5.9.1. The node spends the majority of time in sleep, TS. To ensure that the wireless link is maintained, a guard time of duration TSVS is required, where VS is the maximum frequency variation of the sleep timer due to temperature and voltage shifts. During this guard time, the radio circuits are operational with power Ps, waiting for data to be received. Therefore, the energy required that is not directly used for data transmission or reception is limited by the sleep power and the sleep timer frequency stability, and is approximately TSVS(Ps + PAVS(Vs)). The term Ps+PAVS should be minimized for maximum efficiency. Crystal oscillators have low frequency variation and low power consumption at the cost of increased board area and cost.

Recent literature has proposed alternatives to external 32kHz crystals for sleep timers. In [1], an integrated RC oscillator with self-chopping is used and excellent stability results are achieved. However, temperature compensation is required to meet the ±500ppm sleep timer requirement in the Bluetooth Smart standard. In both [2] and [3], a poly resistor with a dedicated temperature coefficient implant is used in the oscillator, which increases the process cost. In [2], frequency variation with supply is also large. Wireless nodes often have supplies that droop while in sleep; so improved frequency stability over supply variation is desired. In [4], a Pierce oscillator is operated in a low power mode (LPM) or high performance mode (HPM) and a 32kHz clock is generated with a divider. This cellular design switches modes without maintaining the time base because a base station is available as the master time reference, unlike for wireless connectivity standards such as Bluetooth Smart or Zigbee. In this work, a dual mode crystal oscillator is presented which maintains the time base when switching between modes, and therefore can be used as a sleep timer as well as a PLL reference clock.

The dual mode system block diagram is shown in Fig. 5.9.2. A Pierce oscillator is implemented with transistor M1, feedback resistor Rb and tuning capacitors C1 and C2. C1 and C2 are row- and column-encoded arrays, each with 64 independently controlled capacitors, to ensure monotonic frequency tuning. Bias current is generated with a 14b thermometer coded resistor array, Rb, and PMOS current mirror with ratio 1:R1. The ratio M is implemented with a 7b binary weighted array. The oscillator amplitude is sensed, converted to a 6b word and provided to a state machine, which adjusts Rb and M to keep the amplitude between programmed upper and lower thresholds. In HPM, the bias resistor is near minimum, the current mirror ratio is near mid-code to obtain the desired phase noise, and the tuning capacitors are configured to create the required crystal load capacitance. In LPM, C1 and C2 are set to minimum, bias resistor Rb is increased to maximum, and the ratio M is increased to maximum. This increases the bias noise contribution to the oscillator phase noise but minimizes the total power consumption. Figure 5.9.3 shows the control waveforms from the state machine used to transition the crystal oscillator between HPM and LPM. When the state machine receives a request to transition from HPM to LPM, the four parameters Rb, M, C1, and C2 are changed in an interleaved fashion, one unit at a time, such that the energy in the crystal, and therefore the amplitude, is kept nearly constant. This ensures that no clocks are malformed or lost. When the capacitor arrays C1 and C2 reach minimum in LPM, the oscillator frequency has increased by 230ppm, as expected from the pulling equation

\[
\frac{\Delta f}{f_c} = \frac{C_m}{2(C_c + C_p)}
\]

where \(C_m\) is the crystal motional capacitance, \(C_c\) is the parasitic capacitance, and \(C_p\) is the effective load capacitance provided by the series combination of C1 and C2. The oscillator negative resistance is proportional to \(1/C_c\), and can be sustained with much lower bias current when the load capacitance is decreased to minimum. Figure 5.9.4 shows the measured 24MHz clock frequency versus time during transitions between modes. The transitions occur smoothly with no lost or malformed clocks, and the frequency settles to ±40ppm within 130μs. Crystal oscillator startup time is long and increases the average node power consumption because circuitry is on, consuming power while waiting for the clock to be available. In this implementation, this inefficiency is eliminated because the 24MHz crystal oscillator is always on. The 24MHz clock is divided by 768 to derive 31.25kHz which is used as the sleep timer. During transitions, the state machine is locked with 24MHz derived from the crystal oscillator. After reaching LPM, the state machine clock is gated. The fixed offset of 230ppm in LPM is compensated in the synchronization algorithm. The frequency variation around the fixed offset as a function of part-to-part variation and supply and temperature changes determines the sleep clock variation, \(\Delta V\), and required guard time, TS. Power and stability tradeoffs of real time clock sources can be compared if the active power value is known. A sleep timer figure of merit (FOM) can be written as FOM\(\left(\Delta f/P_s, \Delta T\right) = P_s + P_{AVS}(\Delta f, \Delta T)\). Supply voltage may drop during sleep, so \(V_s\) needs to account for frequency variation with voltage \(\Delta f/V_s\) as well as with temperature \(\Delta T\). For the comparison shown in Fig. 5.9.6, \(P_s\) is assumed to be 10mW, supply variation is 300mV, and temperature is assumed to vary over the entire range quoted in the figure. With these conditions, the dual mode oscillator has a FOM of 37.3μW, which is competitive since the implementation is low cost, requiring no special mask layers and no calibration to maintain the ±500ppm sleep timer accuracy required by Bluetooth Smart.

Figure 5.9.5 shows the measured Allan deviation of the 31.25kHz clock in LPM. Beyond a 2s averaging time, the Allan deviation floor is less than 0.008ppm. Figure 5.9.6 summarizes the dual mode oscillator performance measured on 6 parts and compares it to previously published works. The frequency variation with voltage is 6.8ppm/V for HPM and 9ppm/V for LPM. The oscillator and state machine are fabricated in a low leakage 65nm CMOS process. A micrograph is shown in Fig. 5.9.7. The dual mode oscillator and amplitude detector occupy 0.08mm², the ADC occupies 0.019mm², and the state machine occupies 0.036mm² for a total 0.13mm². The ADC is used for other purposes in the SoC, and the 24MHz crystal oscillator and state machine are required to create the PLL reference clock. Therefore, the only extra area needed to create the dual oscillator is due to an incremental increase in the state machine complexity.

In conclusion, a dual mode crystal oscillator has been implemented that can be used both as the reference clock for the radio PLL in a high performance mode and the sleep timer in a low power mode. The oscillator can switch seamlessly between the high performance and low power modes without losing the time base so that synchronization can be maintained among wireless nodes. This allows the wireless node to be implemented with a single crystal, enabling a low cost and small form factor design.

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The authors would like to acknowledge V. Pirahk for the first generation state machine design and R. Smith for mixed signal verification.

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Figure 5.9.1: Simplified power profile of a wireless node with synchronized data transmission.

Figure 5.9.2: Block diagram of the dual mode crystal oscillator and state machine.

Figure 5.9.3: Amplitude, frequency, and control signals in HPM to LPM to HPM transition.

Figure 5.9.4: Measured 24MHz clock frequency versus time showing transitions between operating modes.

Figure 5.9.5: Measured Allan deviation of the 31.25kHz sleep timer in low power mode.

Figure 5.9.6: Summary of measured results and comparison to previous work.
Figure 5.9.7: Die micrograph of the dual mode crystal oscillator on a 65nm CMOS radio SoC.
5.10 A 4.7MHz 53µW Fully Differential CMOS Reference Clock Oscillator with –22dB Worst-Case PSNR for Miniaturized SoCs

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Low-power CMOS reference clock oscillators have been widely used in miniaturized SoCs for emerging microsystems such as implantable biomedical devices and smart sensors [1-3]. In such SoCs, as the supply voltage shrinks the level of analog and digital circuit integration increases to meet rigorous power and area constraints, the noise from other blocks (especially digital blocks) couples through supply and ground lines and poses a serious threat to the performance of CMOS reference clock oscillators.

Although relaxation oscillators can provide high frequency stability as well as low noise [1-3], they have poor tolerance to supply and ground noise due to supply-sensitive building blocks such as reference voltage generators and single-ended comparators. One way of making them immune to the supply noise is to regulate the supply using a bandgap voltage regulator [4]. However, the regulator consumes large power and area and, moreover, requires large external decoupling capacitors of several hundreds of nF to remove high frequency noise, because the supply noise rejection of the regulator starts to deteriorate from around tens of kHz. This approach is therefore not suitable for more area- and power-restricted applications. In this paper, a low-power CMOS reference clock oscillator with high supply and ground noise rejection is presented, which achieves a worst-case power supply noise rejection (PSNR) of –22 dB without any help of decoupling capacitors and bandgap regulators by employing: 1) A fully differential supply- and ground-regulating frequency-locked loop (FLL) architecture; 2) A differential period detector (PD) with a supply-insensitive period reference, and 3) A differential integrator generating a virtual 0V reference. In addition, to achieve higher frequency stability and lower noise, the oscillator uses a chopping technique.

In order for the CMOS oscillators to achieve high immunity against supply and ground noise, it is important to secure a supply-insensitive period (or frequency) reference based on a differential topology. Such requirements can be achieved through a simple differential RC circuit shown in Fig. 5.10.1. To investigate the circuit, transient results of a capacitor voltage, Vc, after switching off, observed with various supply voltages are shown together. It can be seen that the 0V-crossing time, t0V, is independent of supply variation and determined solely by the resistance, Rref, and the capacitance, Cref. Therefore, the supply insensitivity can be naturally obtained by using t0V as the period reference. Since the voltage, VREF, sampled at t0V, indicates the difference between VREF and VDC, the circuit acts like a PD with a supply-insensitive period reference.

The proposed CMOS reference clock oscillator is shown in Fig. 5.10.2, which is composed of a differential PD, a differential integrator, a ring VCO and control logic. As the oscillator is based on a fully differential architecture, it is essentially robust to common-mode interruptions such as supply and ground noise. The key idea is to employ a FLL around the ring VCO so that its output frequency, fCLK, is locked to the supply-insensitive t0V. In order to compare fCLK with t0V and convert their difference into t0V, the oscillator uses the differential PD based on the RC circuit shown in Fig. 5.10.1. In the differential integrator, VREF is compared to 0V, which is inherently generated by a virtual short of the differential integrator, and the comparison result changes the VCO supply VREF. The VCO then updates fCLK and generates an additional 4 phases of the clock signal used to control the simple logic circuit. Note that the virtual 0V replaces a supply-sensitive physical reference voltage, and both the supply and ground of the VCO are regulated by the FLL, making the proposed oscillator robust against not only supply noise but also ground noise. Since the DC-offset and flicker noise of the integrator degrade the frequency stability against supply variation and the noise performance of the oscillator, a chopper stabilization is employed and a low-pass filter composed of CREG and RREG is added to filter out the noise from chopping switches.

The timing diagram and important waveforms of the proposed oscillator are shown in Fig. 5.10.3. The period detection phase consists of a reset phase, a period-detection phase and a charge-transfer phase. During the reset phase, RST is low and CSEG is discharged to –VDD (i.e., Vc = –VDD). Next, in the period-detection phase, Q is low and CSEG is charged through the two RSEG resistors. Note that since Q is the output of the oscillator divided by two, Vc at the end of this phase represents the period difference between 1/fCLK and t0V. After that, when SW goes low, VREF is updated by sampling Vc and compared with 0V through the differential integrator, which transfers the charge on CSEG to CREF and changes VREF. Due to the negative feedback formed by the FLL, VREF at the charge-transfer phase reaches 0V and the output clock is finally locked at fCLK. Therefore, the output frequency after locking is expressed as fCLK = 1/T0V = 1/2ln(2)RSEG/CSEG, which is independent of supply variation, as desired.

To investigate the supply-noise sensitivity of the proposed oscillator, transfer functions from Vc to VREF have been simulated and the results are shown in Fig. 5.10.4(a). In the oscillator, the PD is the only block sensitive to supply noise that has high-pass characteristics (VREF/VDD) due to the first-order noise shaping. The high-frequency noise from the PD is strongly suppressed by the FLL action, which shows low-pass characteristics (VREF/VDCB). Consequently, the overall transfer function has a band-pass characteristic (VREF/VDCB) with a peak gain at around 100kHz, which is the bandwidth of the FLL. In order to quantify the dynamic supply-noise sensitivity, the PSNR performance has been measured with a sinusoidal tone of 200mVp, as shown in Fig. 5.10.4(b). The oscillator achieves a worst-case PSNR of –22dB at 100kHz without any internal or external decoupling capacitors. For comparison, the measurement results of the commercial silicon oscillator [4] are shown together. The proposed oscillator shows 31dB and 43dB lower PSNR compared to the commercial one, with and without a decoupling capacitor of 100nF, respectively.

The proposed oscillator is fabricated in a 0.18μm standard CMOS process and occupies an overall area of about 430×200μm², as shown in Fig. 5.10.7. Note that the oscillator includes neither internal decoupling capacitors nor bandgap regulators. The oscillator consumes 53µW from a 1.4V supply at the output frequency of 4.7MHz. Figure 5.10.5(a) shows the measured period jitter and accumulated jitter performances for the cases with and without chopping. The use of the chopping technique improves the long-term jitter by approximately a factor of two at the 10¹⁴ cycles due to the flicker noise suppression, while degrading the period jitter by only 4ps. The inclining slope of ανN for the first 1000 cycles is clearly observed from the measured accumulated jitter. Figure 5.10.5(b) shows the measured frequency stability of the proposed oscillator. By removing the DC-offset of the integrator through the chopper stabilization so that the oscillator can be more precisely locked at T0V, the frequency stability over supply variation is improved by more than 2.5 times and the oscillator achieves the frequency variation of less than ±0.2% for the supply change from 1.4 to 3.3V. For the temperature change from –40 to 125°C, the oscillator frequency varies by less than ±0.35%. The performance of the oscillator is summarized and compared with other state-of-the-art designs in Fig. 5.10.6. The proposed reference clock oscillator achieves a worst-case PSNR of –22dB without using decoupling capacitors or bandgap regulators, while providing the frequency stability comparable to that of other state-of-the-art works. Moreover, the lowest period jitter is achieved.

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Figure 5.10.1: A differential RC circuit and its transient results under various supply voltages.

Figure 5.10.2: Structure of the proposed reference clock oscillator and schematics of the supply- and ground-regulated VCO and control logic circuit.

Figure 5.10.3: Timing diagram and waveforms of the reference clock oscillator.

Figure 5.10.4: (a) Supply-noise transfer function of the oscillator. (b) Measured PSNR performance for the commercial [4] and proposed oscillators.

Figure 5.10.5: (a) Measured period jitter and accumulated jitter performances. (b) Frequency variations over supply and temperature measured for 5 samples.

Figure 5.10.6: Performance summary and comparison.
Figure 5.10.7: Die micrograph of the proposed reference clock oscillator.