Basic Mechanisms and Modeling of Single-Event Upset in Digital Microelectronics

Paul E. Dodd, *Senior Member, IEEE*, and Lloyd W. Massengill, *Senior Member, IEEE*

***Abstract*—Physical mechanisms responsible for nondestructive single-event effects in digital microelectronics are reviewed, concentrating on silicon MOS devices and integrated circuits. A brief historical overview of single-event effects in space and terrestrial systems is given, and upset mechanisms in dynamic random access memories, static random access memories, and combinational logic are detailed. Techniques for mitigating single-event upset are described, as well as methods for predicting device and circuit single-event response using computer simulations. The impact of technology trends on single-event susceptibility and future areas of concern are explored.**

***Index Terms*—Charge collection, heavy ion irradiation, radiation effects, radiation hardening, single-event effects, single-event upset, soft errors, terrestrial cosmic rays.**

I. Introduction

SINGLE-EVENT effects (SEE) in microelectronics are caused when highly energetic particles present in the natural space environment (e.g., protons, neutrons, alpha particles, or other heavy ions) strike sensitive regions of a microelectronic circuit. Depending on several factors, the particle strike may cause no observable effect, a transient disruption of circuit operation, a change of logic state, or even permanent damage to the device or integrated circuit (IC).

In this paper, we will examine the basic physical mechanisms causing SEE in digital microelectronics for spaceborne applications. Reflecting their relative importance in the commercial marketplace, we will concentrate on silicon MOS devices and digital ICs. Our focus is limited to nondestructive SEEs; destructive SEEs are covered elsewhere in this issue. We begin with a brief historical overview of the discovery of single-event upset (SEU) in space and terrestrial systems. We will then discuss the mechanisms and characteristics of nondestructive SEE in detail, with particular emphasis on SEU in dynamic random access memories (DRAM) and static random access memories (SRAM) and single-event transients (SET) in logic. We discuss various techniques that have been used to mitigate SEU at the device, circuit, and system levels. Next, we review modeling and simulation methods that have proved useful for gaining physical insight and predicting SEE in microelectronics. Finally, we conclude with a look into technology trends that may affect future device susceptibility to SEE and areas of emerging concern, including upsets in terrestrial microelectronics.

Manuscript received February 26, 2003. Sandia National Laboratories is a multiprogram laboratory operated by Sandia Corporation, a Lockheed Martin Company, for the U.S. Department of Energy's National Nuclear Security Administration under Contract DE-AC04-94AL85000.

P. E. Dodd is with Sandia National Laboratories, Albuquerque, NM 87185 USA (e-mail: pedodd@sandia.gov).

L. W. Massengill is with the Department of Electrical Engineering and Computer Science, Vanderbilt University, Nashville, TN 37235 USA (e-mail: lloyd.massengill@vanderbilt.edu).

Digital Object Identifier 10.1109/TNS.2003.813129

II. SEE: A Brief History

Oddly enough, the first paper to ever deal with the issue of SEU was not a paper on the use of electronics in the space environment, but a paper assessing scaling trends in terrestrial microelectronics [1]. In this paper, the authors forecast the eventual occurrence of SEU in microelectronics due to terrestrial cosmic rays and further predicted that the minimum volume of semiconductor devices would be limited to about 10 μm on a side due to these upsets! In fact, the authors wrote in 1962 that "already at the present time the essential part of semiconductor devices, the active region, is close to the minimum size possible" [1]. The first confirmed report of cosmic-ray-induced upsets in space was presented at the NSREC in 1975 by Binder *et al.* [2]. In this paper, four upsets in 17 years of satellite operation were observed in bipolar J–K flip–flops operating in a communications satellite. The authors used scanning electron microscope (SEM) exposures to determine the sensitive transistors and, using a diffusion model, calculated a predicted upset rate within a factor of two of the observed rate. Perhaps because the numbers of errors observed was so small, it was a few years before the importance of SEU was fully recognized, with significant numbers of SEU-related papers not appearing at the NSREC until 1978–1979.

The occurrence of soft errors in terrestrial microelectronics manifested itself shortly after the first observations of SEU in space [3]. This watershed paper from authors at Intel found a significant error rate in DRAMs as integration density increased to 16 and 64K, spurring a flurry of terrestrial SEU-related work in the late 1970s [4]. The primary cause of soft errors at the ground level was quickly diagnosed as alpha-particle contaminants in packaging materials [3]. For example, according to Ziegler, the Intel problem was traced to a new LSI ceramic packaging plant that had just been built downstream from the tailings of an abandoned uranium mine [5]. Radioactive contaminants in the water used by the factory were contaminating the ceramic packages they manufactured. By using low-activity materials for IC fabrication and on-chip shielding coatings [5], [6], the terrestrial soft error problem essentially disappeared for several years and has only recently become a serious concern again, as will be discussed in detail in Section VIII.

In the late 1970s, evidence continued to mount that cosmic-ray-induced upsets were indeed responsible for errors observed in satellite memory subsystems, and the first models for predicting system error rates were formulated [7]. By this time satellite memory systems had increased in size, and on-orbit error rates of one per day could not be ignored as a fluke. In combination with the reports of soft errors in terrestrial systems, the evidence was compelling that an important new radiation effect had arrived.

Although the first papers attributed memory upsets to direct ionization by heavy ions such as those in the iron group [2], [7], by 1979 two groups reported at the NSREC on errors caused by proton and neutron indirect ionization effects [8], [9] (explained in Section III). This was a very important discovery because of the much higher abundance of protons relative to heavy ions in the natural space environment. In addition, it meant that not only would SEE be caused by galactic cosmic rays, but also by solar event protons and protons trapped in the Earth's radiation belts. In fact, proton-induced SEE often dominate the single-event response of commercial parts operating in low earth orbits. The paper by Guenzer *et al.* [9] was the first to use the term "single-event upset," and this term was immediately adopted by the community to describe upsets caused by both direct and indirect ionization. The year 1979 also brought the first report of single-event latchup (SEL), an important discovery given the potentially destructive nature of the failure mode [10].

In the early 1980s, research on SEU continued to increase, and by 1980, single-event phenomena had become a dedicated session of the NSREC. Methods for hardening ICs to SEU were widely developed and used throughout this decade [11], [12]. At the same time, research into the fundamental mechanisms behind SEEs was paying dividends in increased scientific understanding of the problem. Much of the single-event research of the 1980s focused on errors observed in latched circuitry, such as DRAMs, SRAMs, nonvolatile memories, latches, and registers. An understanding of this phenomenon, and its mitigation for reliable data storage, proved critical to successful military and space deployments of that decade. The flurry of work to address the extremely significant problem of soft errors in memories shaped the early single-event research landscape, especially within the NSRE conference community.

There were, however, a few studies in the 1980s addressing another emerging and potentially troubling single-event issue: errors due to single events in combinational or imbedded core logic. In 1984, May and his coauthors from Intel were awarded "Best Paper" at the International Reliability Physics Symposium for a very revealing single-event experiment on an Intel microprocessor under dynamic operation [13]. Using an experimental technique of dynamic fault imaging, May demonstrated the temporal progression of a single-event disturbance from a local perturbation to a massive fault condition encompassing most of the microprocessor circuitry. Other studies of combinational logic appeared in the late 1980s (e.g., [14]–[16]), but were often overshadowed by the volume of work addressing memory upset.

The 1990s saw two major developments that continued to increase the importance of SEEs. One was the dramatic decrease in the number of manufacturers offering radiation-hardened (or more particularly to our purposes here, SEU-hardened) digital ICs. This (among other factors) led to the increased usage of commercial electronics in spacecraft systems. While many system designers embraced the use of modern commercial ICs because of the increased functionality and performance they provide, their relative sensitivity to SEE presented significant challenges to maintaining system reliability. The second development was the continued advance in fabrication technologies toward smaller IC feature sizes and the higher speeds and more complex circuitry that scaling enables. These advances typically increase sensitivity to SEE, even to the point of terrestrial errors in a benign desktop environment, and may also lead to new failure mechanisms. Absent new mechanisms, Ronen *et al.* have shown that simple scaling rules predict an increase in soft error susceptibility of about 40% per technology generation node [17].

These two developments of the past decade have led to an interesting convergence of mission from two historically disparate communities within the integrated circuit field: space and military vendors driven toward commercial (nonradiation-hardened) circuits and commercial vendors driven toward a very real concern about SEE in the everyday consumer environment.

In the late 1990s, a renewed interest in SEE in combinational (or core) logic emerged. This resurgence was fueled by several factors including: 1) a perception that the memory soft error situation was controllable with advanced technologies (e.g., SOI, ^{10}B-free materials, reduced-emission packaging) and the effectiveness of error detection and correction (EDAC) techniques [18], [19]; 2) a growing concern, based on extrapolated empirical and theoretical data, that technology scaling could lead to an inversion between the relative significance of memory-generated and core-logic-generated faults on observed soft error rates [20]–[22]; and 3) observations that clock speeds were driving up core-logic error rates [23], [24].

As we enter the 21st century, increasing sensitivity to SEU is expected to continue, both in memories and core logic. Upsets in terrestrial electronics are a serious reliability concern for commercial manufacturers. In fact, single-event vulnerability has become a mainstream product reliability metric for all facets of the integrated circuit industry, as outlined by the SEMATECH National Industry Association Roadmap [25]. A recent all-day tutorial at the International Reliability Physics Symposium was devoted entirely to soft errors in commercial semiconductor technologies [26] and in 2003 this topic became a regular technical session of that conference. At the same time, the feasibility of traditional SEU-hardening techniques is becoming questionable, especially in a paradigm where we see fewer dedicated rad-hard foundries to implement them. Circuit designs that are inherently radiation resistant [known as hardening by design (HBD)] are receiving considerable attention [27], [28]. Another current subject of interest is charge collection and SEU in silicon-on-insulator (SOI) and SiGe bipolar technologies [29], [30]. As these become mainstream fabrication technologies, their radiation response is of interest to spacecraft designers ready to insert the latest technologies into their systems.

III. Physical Origins of SEU

A. Charge Deposition

There are two primary methods by which ionizing radiation releases charge in a semiconductor device: direct ionization by the incident particle itself and ionization by secondary particles created by nuclear reactions between the incident particle and the struck device. Both mechanisms can lead to integrated circuit malfunction.

1) Direct Ionization: When an energetic charged particle passes through a semiconductor material it frees electron-hole pairs along its path as it loses energy. When all of its energy is lost, the particle comes to rest in the semiconductor, having traveled a total path length referred to as the particle's *range*. We frequently use the term *linear energy transfer* (LET) to describe the energy loss per unit path length of a particle as it passes through a material. LET has units of MeV/cm^2/mg, because the energy loss per unit path length (in MeV/cm) is normalized by the density of the target material (in mg/cm^3), so that LET may be quoted roughly independent of the target. We can easily relate the LET of a particle to its charge deposition per unit path length. In silicon, an LET of 97 MeV-cm^2/mg corresponds to a charge deposition of 1 pC/μm. This conversion factor of about 100 is handy to keep in mind to convert between LET and charge deposition.

A curve of particular interest for understanding the interaction of a given energetic particle with matter is the LET of the particle versus depth as it travels through the target material. Fig. 1 shows such a curve for a 210-MeV chlorine ion traveling through silicon. Such curves are readily obtained using computer codes derived from the work of Ziegler *et al.* (e.g., the TRIM and SRIM family of codes, [31]). This figure shows the basic characteristics of ion-induced charge deposition as a function of depth. The peak in charge deposition is referred to as the *Bragg peak* and in general occurs as the particle reaches an energy near 1 MeV/nucleon. A useful rule of thumb is that the maximum LET (in MeV-cm^2/mg) of an ion is roughly equal to its atomic number Z. A more rigorous discussion of the Bragg curve and the Bragg peak is found in [32].

Direct ionization is the primary charge deposition mechanism for upsets caused by heavy ions, where we define a heavy ion as any ion with atomic number greater than or equal to two (i.e., particles other than protons, electrons, neutrons, or pions). Lighter particles such as protons do not usually produce enough charge by direct ionization to cause upsets in memory circuits, but recent research has suggested that as devices become ever more susceptible, upsets in digital ICs due to direct ionization by protons may occur [33], [34].

2) Indirect Ionization: Although direct ionization by light particles does not usually produce enough charge to cause upsets, this does not mean that we can ignore these particles. Protons and neutrons can both produce significant upset rates due to indirect mechanisms. As a high-energy proton or neutron enters the semiconductor lattice it may undergo an inelastic collision with a target nucleus. Any one of several nuclear reactions may occur; examples for protons and neutrons can be found in [35] and [36]. Possible reactions include: 1) elastic collisions that produce Si recoils; 2) the emission of alpha or gamma particles and the recoil of a daughter nucleus (e.g., Si emits alpha-particle and a recoiling Mg nucleus); and 3) spallation reactions, in which the target nucleus is broken into two fragments (e.g., Si breaks into C and O ions), each of which can recoil. Any of these reaction products can now deposit energy along their paths by

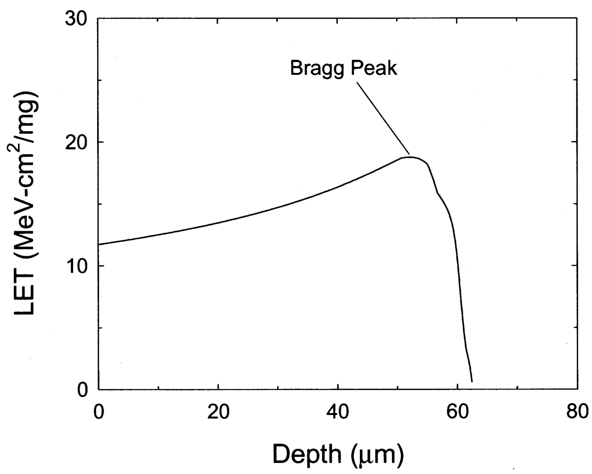


Fig. 1. Linear energy transfer (LET) versus depth curve for 210-MeV chlorine ions in silicon.

direct ionization. Because these particles are much heavier than the original proton or neutron, they deposit higher charge densities as they travel and therefore may be capable of causing an SEU.

Inelastic collision products typically have fairly low energies and do not travel far from the particle impact site. They also tend to be forward-scattered in the direction of the original particle; this has consequences for the SEU sensitivity as a function of the angle of incidence [37], [38]. Once a nuclear reaction has occurred, the charge deposition by secondary charged particles is the same as from a directly ionizing heavy ion strike.

B. Charge Collection

The basic properties of charge collection following a particle strike have been studied using a variety of experimental and theoretical methods. Broadbeam charge collection spectroscopy measurements have been used to determine SEU-sensitive volumes in SRAMs [39]–[41], and ion microbeams and lasers have been used with high-speed sampling oscilloscopes to measure charge-collection transients in Si devices [42]–[44]. Ion microbeams and lasers have also been used to map integrated charge collection as a function of position in ICs [45], [46] and more recently as a function of both time and position [47]. The physics of charge collection have also been studied in detail through the use of two-dimensional (2-D) and three-dimensional (3-D) numerical simulation [48], [49]. It is beyond the scope of this paper to comprehensively review the massive literature on charge collection; we seek to cover the main highlights and recent developments only.

1) Basic Physics of Charge Transport: When a particle strikes a microelectronic device, the most sensitive regions are usually reverse-biased p/n junctions. The high field present in a reverse-biased junction depletion region can very efficiently collect the particle-induced charge through drift processes, leading to a transient current at the junction contact. Strikes near a depletion region can also result in significant transient currents as carriers diffuse into the vicinity of the depletion region field where they can be efficiently collected. Even for

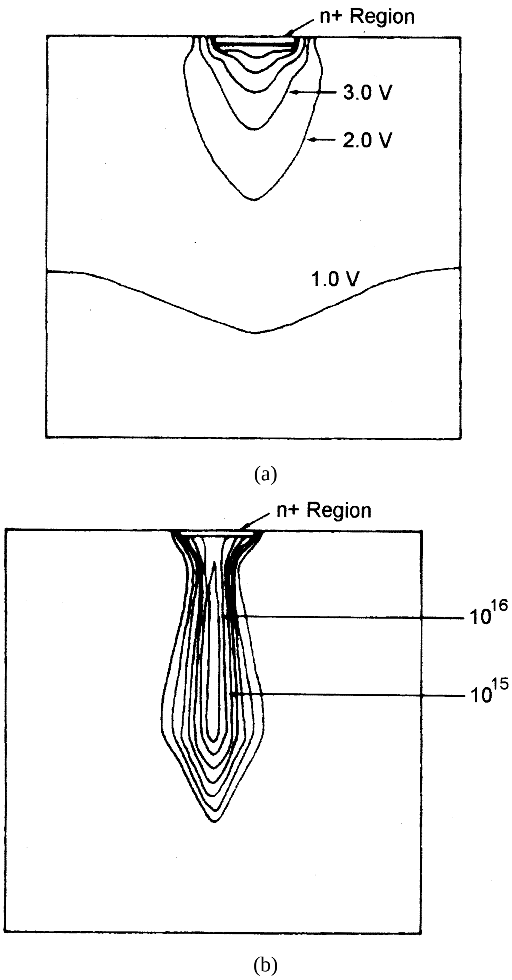


Fig. 2. Illustration of funneling in an n^+/p silicon junction following an ion strike: (a) electrostatic potential and (b) electron concentration. Note that contours of electrostatic potential are distorted along the path of the ion [51].

direct strikes, diffusion plays a role as carriers generated beyond the depletion region can diffuse back toward the junction.

Shortly following the discovery of SEU, researchers at IBM used numerical device simulators to compute the response of reverse-biased p/n junctions to alpha-particle strikes [48], [50]. An important insight gained from these early charge-collection simulations was the existence of a transient disturbance in the junction electrostatic potential, which was termed the "field funnel." Charge generated along the particle track can locally collapse the junction electric field due to the highly conductive nature of the charge track and separation of charge by the depletion region field, as shown in Fig. 2 [51]. This funneling effect can increase charge collection at the struck node by extending the junction electric field away from the junction and deep into the substrate, such that charge deposited some distance from the junction can be collected through the efficient drift process.

The funnel effect has been investigated in further detail by later researchers [52], [53], with the analytical models for funneling developed by McLean and Oldham [52] being an important early contribution to understanding several characteristics of funneling. Later research studied the influence of epitaxial substrates on the transient charge-collection characteristics [54]–[56]. Several important additional insights have been gained from these studies, and the reader is referred to [54]–[57] for comprehensive discussions of funneling.

While in some cases important to charge collection in isolated p/n junctions with constant applied bias, the role of the funnel is less significant in the case of static circuits such as SRAMs, where reverse-biased transistor junctions are connected to active external circuitry. In this scenario, the applied voltage at the struck junction is not constant, and in fact very often the struck node may switch from being reverse-biased to zero-biased. This loss of bias at the struck node tends to lessen the importance of drift collection (and hence the funnel) as the transient proceeds [58]. In such cases, funneling may play a role in the early-time response of the circuit by helping to initially flip the node voltage, but it is late-time collection by diffusion that ensures the bit stays flipped (see Section IV for further details about the upset process in SRAM circuits).

2) Charge-Collection Mechanisms in Submicron Devices: The charge-collection response of a single p/n junction is generally presumed to accurately depict the response of the sensitive junction of a transistor, typically a reverse-biased drain region. Studies have indicated that a new charge-collection mechanism may exist for submicron MOS transistors that requires considering the entire transistor [59]. Termed the alpha-particle source-drain penetration effect (ALPEN), this charge-collection mechanism results from a disturbance in the channel potential that the authors referred to as a funneling effect. The effect is triggered by a particle strike that passes through both the source and the drain at near-grazing incidence. Immediately following the strike, the electrostatic potential in the channel region is perturbed, leading to a significant (but short-lived) source-drain conduction current that mimics the "on" state of the transistor. This mechanism was revealed by 3-D alpha-particle simulations and has been experimentally verified. The experiments indicate that source charge injection due to this mechanism increases rapidly for effective gate lengths below about 0.5 μm. Later work predicted the same direct channel conduction mechanism can occur in 0.3-μm gate length MOSFETs even for normal incidence strikes and can lead to charge multiplication [60]. This mechanism may forebode a serious vulnerability to SEU for deep submicron MOSFETs.

A somewhat similar, but distinct mechanism exists when electrons or holes released by a particle strike are confined to a well or body region in which a transistor is located. For example, for an n-channel MOS transistor located in a p-well, electrons induced by a particle strike can be collected at either the drain/well junction or the well/substrate junction. However, as illustrated in Fig. 3, holes left in the well raise the well potential and lower the source/well potential barrier, and the source injects electrons into the channel [61]–[63]. These electrons can be collected at the drain, where they add to the original particle-induced current and can cause an increased SEU sensitivity. Because the electrons are injected over the source/well barrier, this is referred to as a bipolar transistor effect, where the source acts as the emitter, the channel as the base region, and the drain as the collector. Reducing the channel length effectively decreases the base width, and the effect becomes more pronounced [63].

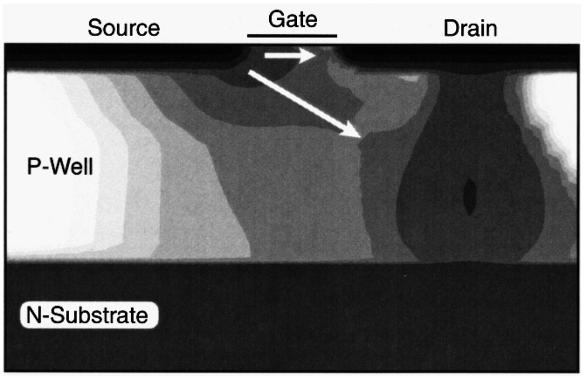


Fig. 3. Electron concentration contours inside an n-channel MOS transistor following a heavy ion strike [63]. Bipolar effect is evidenced by the contours emanating from the source, showing that the source is injecting electrons into the p-well, where they may be collected at the substrate or at the drain.

3) Charge Collection in Silicon-on-Insulator Devices: Charge collection mechanisms in SOI devices are covered in detail elsewhere in this issue, but essentially the same bipolar effect discussed above occurs in SOI devices [64], [65]. Following a particle strike to the body of an n-channel SOI transistor, electrons can be collected at the source and drain electrodes. Holes can only escape through the body tie contact, if there is one, or slowly through recombination if there are no body ties. Residual holes left in the body raise the body potential and trigger the lateral parasitic bipolar transistor inherent to the SOI transistor. This bipolar current considerably lowers the SEU hardness of SOI. In some cases, bipolar amplification in concert with impact ionization can lead to snapback, a sustained high-current condition similar to latchup [29]. Even in devices with body ties, the bipolar effect results in significant charge amplification, especially for ion strikes far from the body ties [66]–[67].

IV. SEU IN MEMORY CIRCUITS

A. SEU Mechanisms in DRAMs

DRAM technology refers to the broad class of information storage devices, usually one-transistor designs, which passively store packets of charge to represent binary information. The key to DRAM upset is that the information storage is passive (no active regeneration path), and any (no matter how small) disturbance of the stored information by a particle strike is persistent until corrected by external circuitry [19]. There is no inherent refreshing of this charge packet (e.g., charge resupply through a load device) and no active regenerative feedback as one observes in latches and SRAM cells. What is so often referred to as a bit flip, the transition from one stable binary state to the other, is not required in DRAMs for an SEU to occur. A degradation of the stored signal to a level outside the noise margin of the supporting circuitry is sufficient to lead to erroneous interpretation and a resultant error.

There are two key parameters related to DRAM upsets: the noise margin associated with a bit signal and a critical time window (because of the dynamic operation of the circuit, the vulnerability to upset is not constant with time). The noise margin is closely linked with the concept of critical charge,

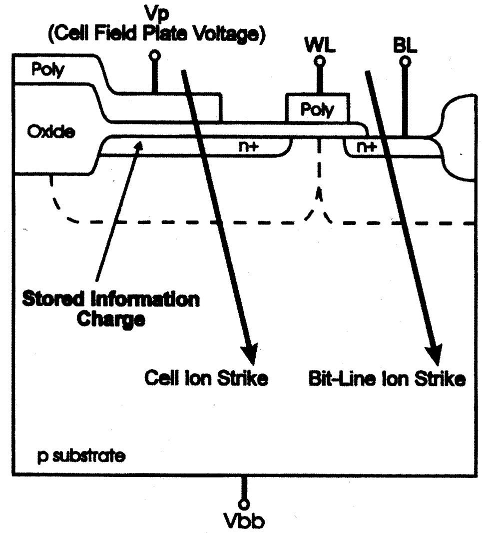


Fig. 4. One-transistor DRAM cell physical layout, illustrating ion strikes to the storage cell and bit-line.

Q_{crit}. Q_{crit} is usually defined as the minimum amount of charge collected at a sensitive node necessary to cause a circuit upset. This definition is somewhat limited and is not totally appropriate in all circuit cases [68]. For example, Q_{crit} may not be a circuit constant, but can vary with the timing of the strike relative to the dynamics of the circuit. The temporal characteristics of the ion strike in relation to the dynamic clocking of the cell are also important.

The most prevalent soft error source in DRAM arrays is single-event charge collection within each binary cell. These cell errors, as first described by May and Woods [3], are caused by a single-event strike in or near either the storage capacitor or the source of the access transistor, as illustrated in Fig. 4. Such a strike directly affects the stored charge and the information integrity by the collection of the ion-induced charge. A cell upset due to charge collection is usually observed as a $1 \rightarrow 0$ transition; the collected charge relaxes a stored charge state [3]. This upset mechanism has been the primary concern and focus of study since the early investigations of SEU in DRAMs.

In the late 1980s, Takeda *et al.* reported the ALPEN source-drain penetration effect discussed in Section III [59]. While the normal effect of an ion strike is to deplete charge from a DRAM cell storage capacitance, the ALPEN mechanism causes the opposite result: the shunting of charge onto the storage node. Thus, $0 \rightarrow 1$ transitions can also be introduced by ion strikes. A similar phenomenon has been found to occur between adjacent trench storage capacitors in trench-type DRAMs [69].

Upsets can also occur in DRAMs due to bit-line strikes. When the bit lines are in a floating voltage state (e.g., during a read cycle), DRAMs are sensitive to the collection of charge into diffusion regions that are electrically connected to the bit access lines [70]. This collection could arise from any of the access-transistor drains along the bit-line length or from a direct strike to the differential sense amplifier [71]. The bit-line SEU mechanism is the reduction of the sensing signal due to a charge imbalance introduced on the precharged bit lines, either prior to or during the sensing operation.

Bit-line strikes are only possible during the floating precharge and sensing stages of operation, and therefore temporal characteristics of the strike in relation to the clocking signals are critical. Because the duty cycle of these stages to the overall cycle time increases with increasing overall clock frequency, the bit-line soft error rate is inversely proportional to DRAM cycle time [71]. In contrast, cell upsets are independent of the DRAM cycle time. Bit-line errors also show a strong inverse correlation with the signal charge [71]. As chip densities and speeds grow, bit-line errors are expected to be increasingly important.

In 1988, Rajeevakumar *et al.* observed a new failure mode in DRAMs due to a synergistic effect of bit-line and storage cell charge collection [72]. Both processes individually resulted in less charge collection than Q_{crit}, but the combined effect during a read operation caused an error. This effect, termed the combined cell-bit line (CCB) failure mode, was shown to dominate both the cell and bit-line error components at very low cycle times.

Another very important factor in determining the SEU susceptibility of DRAMs is the storage cell technology [19]. Many different physical storage structures are used in DRAM manufacture, ranging from various stacked capacitor designs to buried trench capacitors. These different physical structures have been shown to have a dramatic effect on the observed soft error rate [73].

B. SEU Mechanisms in SRAMs

The upset process in SRAMs is quite different from DRAMs, due to the active feedback in the cross-coupled inverter pair that forms a typical SRAM memory cell as shown in Fig. 5. When an energetic particle strikes a sensitive location in a SRAM (typically the reverse-biased drain junction of a transistor biased in the "off" state [63], [74], for example the "off" n-channel transistor shown in Fig. 5), charge collected by the junction results in a transient current in the struck transistor. As this current flows through the struck transistor, the restoring transistor ("on" p-channel transistor in Fig. 5) sources current in an attempt to balance the particle-induced current. Unfortunately, the restoring transistor has a finite amount of current drive, and equally importantly, a finite channel conductance. Current flow through the restoring transistor therefore induces a voltage drop at its drain. This *voltage* transient in response to the single-event current transient is actually the mechanism that can cause upset in SRAM cells. The voltage transient is essentially similar to a write pulse and can cause the wrong memory state to be locked into the memory cell.

In SRAM cells, there are four possible sensitive strike locations, namely the four transistor drains interior to the SRAM circuit. An important consideration for charge collection is whether the junction is located inside a well or in the substrate [63], [74], because the well-substrate junction provides a potential barrier that prevents charge deposited deep within the substrate from diffusing back to the struck drain junction. For example, in the familiar outside-the-well "off" strike, because the struck drain is not located in a well, charge deposited deep in the substrate can diffuse back to the drain junction. This is the most sensitive strike location for most technologies [74].

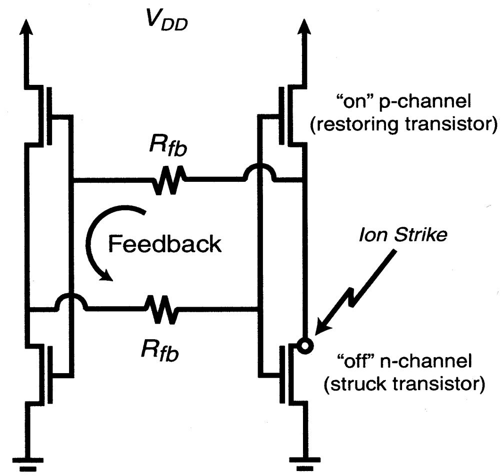


Fig. 5. Competition between the feedback process and the recovery process governs the SEU response of SRAM cells.

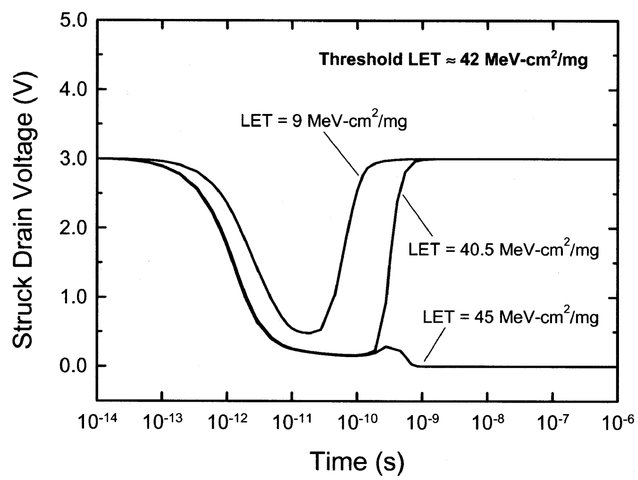


Fig. 6. SRAM struck drain voltage transients for ion strikes with LET well below, just below, and just above the SEU threshold. Even the ion strike with LET well below the actual SEU threshold is sufficiently ionizing to momentarily flip the struck node voltage.

Inside-the-well strikes are particularly interesting because of shunt and bipolar effects that can occur in multilayer structures [61]. For the inside-the-well "off" strike, the initial drift current pulls down the struck node potential, initiating the upset process. As the transient proceeds, holes deposited in the p-well are collected at the p-well ties, raising the well potential and leading to injection of electrons by the source [61], [62], [75]. This initiates the inside-the-well bipolar effect discussed in Section III and illustrated in Fig. 3. Electrons collected by the substrate do not contribute to upset because the substrate is attached to V_{DD}. However, electrons collected by the n-drain constitute a bipolar current in the same direction as the initial photocurrent and do contribute to the upset process [63]. For small geometries, the inside-the-well "off" strike can become an important mechanism.

Interestingly, incident particles far below the upset threshold are often sufficiently ionizing to induce a momentary voltage "flip" at the struck node of an SRAM. For example, Fig. 6 shows drain voltage transients in an SRAM for a particle strike with LET well below the upset threshold, just below the upset threshold, and just above the upset threshold. Even the particle with LET well below the upset threshold causes a significant voltage transient on SET at the struck drain. Whether an observable SEU occurs depends on which happens faster: the feedback of the voltage transient through the opposite inverter, or recovery of the struck node voltage as the single-event current dies out [58], [76], [77]. Note that drift (including funneling effects) is responsible for the rapid initial flip of the cell, while long-term charge collection by diffusion prolongs the recovery process; both mechanisms are critical to the upset process.

The recovery time of an SRAM cell to a particle strike depends on many factors, such as the particle LET, the strike location, etc. From a technology standpoint, the recovery time depends on the restoring transistor current drive and minority carrier lifetimes in the substrate [76], [77]. The cell feedback time is simply the time required for the disturbed node voltage to feed back through the cross-coupled inverters and latch the struck device in its disturbed state. This time is related to the cell write time and in its simplest form can be thought of as the RC delay in the inverter pair. This RC time constant is thus a critical parameter for determining SEU sensitivity in SRAMs—*the smaller the RC delay, the faster the cell can respond to voltage transients (including write pulses) and the more susceptible the SRAM is to SEU*. Obviously, this has implications for the sensitivity of future, higher speed technologies, as discussed in Section VIII.

C. *Single-Event Multiple Bit Upset*

Single-event multiple-bit upsets (MBUs) occur when a single particle strike causes more than one error in an IC. For example, diffusion of charge to closely spaced junctions can upset more than one bit in both SRAM and DRAM cells [56], [78]. For a particle striking an IC at a grazing angle of incidence, the charge track may intersect several sensitive regions and cause multiple upsets [79]. The effects of MBU are typically alleviated by a combination of error-correcting codes that work on a word-by-word basis (see Section VI) and layout rules that prevent physically adjacent bits from belonging to the same word of memory. Still, single-word multiple-bit upsets (SMUs) can occur and pose a substantial threat to system integrity [80]. MBUs have been observed in on-orbit spacecraft data [81], [82]. As advanced technologies pack ever more bits into small areas, MBU may become more prevalent.

D. *Functional Interrupts*

Single-event functional interrupts (SEFIs) are a complex failure mode whereby an ion strike triggers an IC test mode, a reset mode, or some other mode that causes the IC to temporarily lose functionality [83]. As devices become increasingly complex, they may be more likely to exhibit SEFIs. For example, synchronous DRAMs are very complicated ICs that incorporate built-in self-test (BIST) modes and self-repairing boot sequences that remap nonfunctional bits in the memory with redundant bits on the chip. An ion strike to a SDRAM with such circuits may initiate a BIST mode, cause a chip reset to occur, or throw the IC into an idle state [84]. These events can have serious consequences on system operation, sometimes requiring device reset to clear the condition [85].

V. SEE Mechanisms in Logic

The quantification of SEU effects in combinational logic circuits (e.g., core logic of a microprocessor or microcontroller) is quite different than in memories. Whether or not an erroneous data signal caused by a single-event ion strike is captured by a storage element (latch or register) depends on the existence of active paths from the struck node to latches, the arrival time of the erroneous signal at the latches, and the erroneous pulse time profile at the latch input. Even if the erroneous signal is captured (stored) by one or more latches, there is still no guarantee that it will propagate to the output. The erroneous information may be blocked by superseding logic during the following clock cycles—i.e., the corrupted latch may become a "don't care" member of a subsequent state of the logic. In core logic, the concepts of "faults" and "errors" are distinct from memory circuits and require precise definition.

A. *Combinational Soft Faults*

In a logic circuit, charge collection due to a single-event strike on a particular node will generate a low-to-high or high-to-low voltage transition or a transient noise pulse. If this pulse is larger than the input noise margin of a subsequent gate, it will compete with the legitimate digital pulses propagating through the circuit. The ability of the noise pulse to propagate depends not only on its magnitude, but also on the active logic paths from the node existing at that instant in time. An example of this is shown in Fig. 7 [86].

In Fig. 7, a single-event strike generates a voltage transition on node F of this circuit. The possible propagation of this pulse to a latch (storage) element depends on several factors. First, the active combinational paths at that instant in time. Two such distinct paths (one for an input vector of 000 and one for an input vector of 100) are shown by the arrows in Fig. 7. The active combinational paths depend on the dynamic state of the logic as determined by the particular code vectors executed with time (the present "state" of the logic). Second, assuming that an active path exists for the propagation of the noise pulse, the pulse will be shaped and phase delayed as it propagates through the intervening gates en route to a latch. Third, the temporal characteristics of the noise pulse as it arrives at a latch are important. The pulse must arrive within the setup and hold (S/H) time of the latch element to be captured (to be stored by the latch element). The clocking characteristics of the latch and the previous state of the latch contribute to this mechanism. If all three of the above conditions are properly met, then the SE-generated noise pulse will be captured by the latch as erroneous information—we define this as the generation of a *soft fault* (SF).

SFs may also be generated by direct single-event strikes to the latch nodes, where the latch information is corrupted via a bit flip. This effect is analogous to SEUs in memory circuits and can be modeled in a similar way [6].

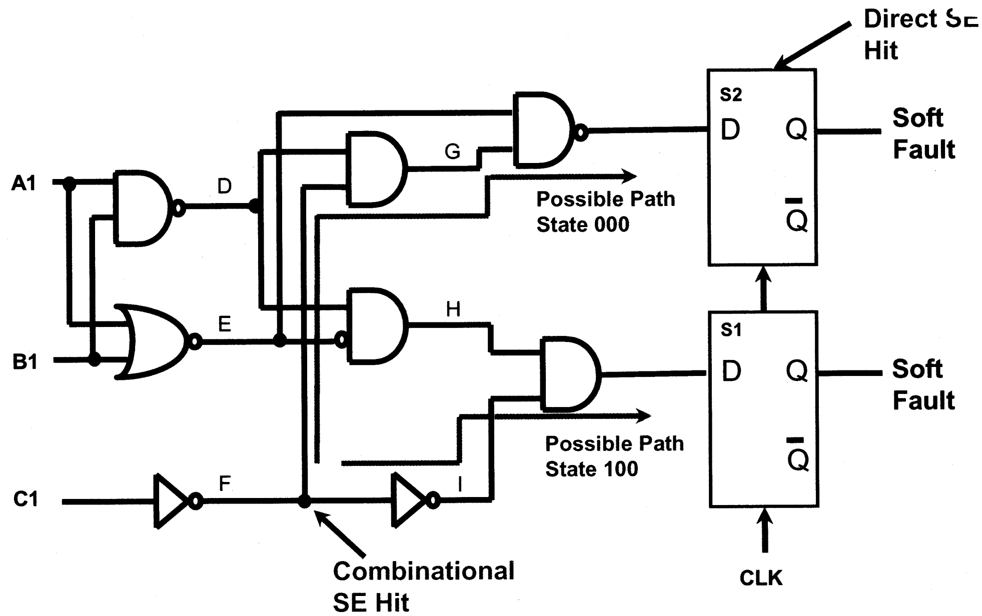


Fig. 7. Example of a SET impulse propagating through a combinational logic system, taking various paths as a function of the system state, and creating a latch soft fault [151].

B. Observable Error Events

Once an SF has been identified, or a soft fault probability has been calculated, information is known about the vulnerability of a circuit to single events and/or critical paths which may contribute a weak link for single-event tolerance. However, actual upset metrics which map to the observable operation of a particular circuit on orbit or in a beam experiment are not delivered by knowledge of SFs. Internal SFs may not be observable at the interface pins of a circuit (or the I/O ports of a subcircuit). For example, the particular latch affected by the soft fault may be part of a "don't care" state of the finite state machine; the change of state has no effect on subsequent operation of the circuit. Or, the erroneous latch data may be part of a data register that is scrubbed in a subsequent clock cycle. Thus, no observable error actually occurs.

However, if the soft fault eventually propagates to one or more of the I/O ports of the circuit, then an externally observed error exists; we define this and only this event as an *error event*. It is clear that one soft fault may cause erroneous information at many I/O ports and that this erroneous information may appear during many clock cycles.

VI. Mitigation of SEU

SEU mitigation techniques can be roughly classified into three distinct categories. System-level techniques deal with SEU at the system architecture level. Circuit-level techniques rely on changes in the circuit design to reduce SEU sensitivity. Technology- or device-level hardening requires fundamental changes to the underlying fabrication technology used to manufacture ICs. In this section, we will briefly present all three levels of hardening techniques. A review of several hardening techniques is also found in [87].

A. Technology Hardening

The most fundamental method for hardening against SEU is to reduce charge collection at sensitive nodes. This can be accomplished in DRAMs and SRAMs by introducing extra doping layers to limit substrate charge collection [88]. In advanced SRAMs, triple-well [89] and even quadruple-well [90] structures have been proposed to decrease SEU sensitivity. In this case, all strikes are basically "inside-the-well" strikes. Retrograde wells and buried layers can also be used to provide an internal electric field that opposes collection of charge deposited in the substrate [91], [92]. Even the simple use of an epitaxial substrate instead of a bulk substrate affords some level of reduced charge collection [56].

Another effective technique for reducing charge collection in silicon devices is the use of SOI substrates [65]. In this case, the collection volume is reduced by the fact that the active device is fabricated in a thin silicon layer that is dielectrically isolated from the substrate. In a typical thin-film SOI device, the source and drain penetrate all the way to the buried isolation oxide (BOX). This substantially reduces the SEU-sensitive area because the reverse-biased drain junction area is limited to the depletion region between the drain and the body of the transistor. Charge deposited in the silicon substrate underneath the BOX cannot be collected at the drain due to the dielectric isolation, although recent research indicates that capacitive coupling across the BOX can lead to unexpected charge collection in SOI structures [93], [94]. Unfortunately, as briefly mentioned in Section III, charge deposited in the body region (for example, by a particle strike to the gate region) can trigger a bipolar mechanism that limits the SEU hardness of SOI circuits [64], [65]. Body ties are sometimes used commercially to reduce floating-body effects under dc operation, and careful attention to body tie design is crucial to maintaining good SEU performance [64], [95], [96]. Even in body-tied SOI designs, manufacturers have found it necessary to incorporate other hardening methods for applications where very high upset thresholds are desired [93], [97], [98]. Fully depleted SOI transistors exhibit reduced floating-body effects and in some (but not all) cases have shown excellent SEU performance [99].

B. Circuit- and System-Level Hardening

Because of the invasive nature of device-level hardening (i.e., the requirement for fundamental changes in the manufacturing process), methods to improved single-event tolerance at the circuit level have been a frequent topic of research.

Given an understanding of the upset mechanism in SRAMs, we can immediately understand a typical technique used to harden SRAMs against SEU. We have discussed (Section IV) how the SEU process in an SRAM is essentially a race condition between the feedback and recovery processes. To harden an SRAM, we need to either slow the feedback process or decrease the recovery time. The feedback process can be slowed by adding either resistance or capacitance to the feedback loop [11]. Cross-coupled feedback resistors (R_{fb} in Fig. 5) are the classical method of increasing the cell feedback time by increasing the RC delay in the feedback loop. This technique is very effective, as illustrated in Fig. 8. This figure shows the measured SEU cross section (area of the chip sensitive to SEU) as a function of LET for a microprocessor before and after hardening by resistive decoupling [100]. The predicted upset rate in a geosynchronous orbit for the unhardened microprocessor is about once a day, while in the resistively hardened part it is about once per century.

Unfortunately, because the SEU process in SRAMs looks just like the write process, this same RC delay directly impacts the write pulse width of the SRAM. Thus, the effectiveness of resistive hardening does not come without a price. In addition to the speed penalty incurred by adding feedback resistors, increased process complexity results from adding feedback resistors. These resistors are typically implemented in the cell layout as lightly doped polysilicon regions. Because the resistivity of polysilicon is very sensitive to the doping concentration and numerous other factors, it is very difficult to control the resistor value [101]. To add to this problem, polysilicon resistivity has a negative temperature dependence. This leads to a temperature dependence of both the write speed and the SEU response and makes it challenging to optimize a resistively hardened technology so that it will operate within specifications across a wide temperature range.

Other decoupling techniques have been proposed that place resistors, diodes, or transistors in different locations within the feedback path [102]–[106], usually for the purpose of reducing the impact of the resistors on timing parameters or increasing manufacturability. For the most part, these techniques have not been widely used (if at all) and have their own associated tradeoffs. Capacitors have been successfully used as a feedback element in SOI SRAMs [65], [97], [98] and very recently as a means to improve the soft-error performance of deep-submicron CMOS SRAMs for terrestrial applications [107]. While adding capacitance still degrades timing parameters, one advantage is reduced temperature-dependence compared to resistive hardening.

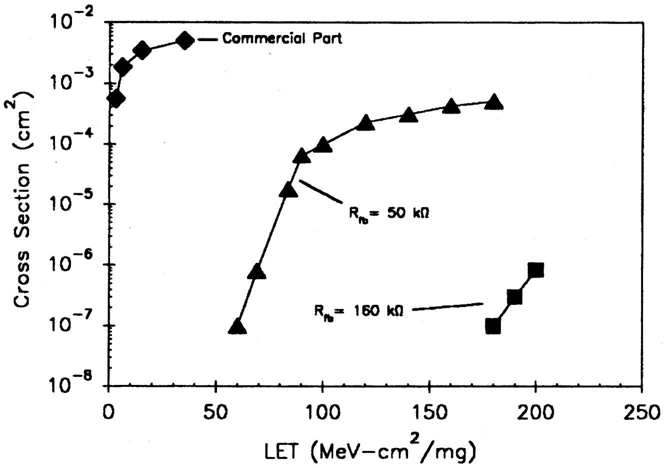


Fig. 8. Measured SEU cross section of a 16-bit commercial microprocessor showing the effectiveness of resistive hardening for mitigating SEU [100].

Another important technique for hardening circuits, especially in a manner portable across any commercial fabrication process, is sometimes referred to as HBD [108]. Several design-hardened SRAM and latch circuits have been proposed and fabricated [109]–[114]. These memory cells typically rely on redundant circuit elements (usually 12–16 transistors per memory cell as opposed to six in a standard unhardened cell) to protect against SEU. Because of the large number of transistors per cell, these designs consume more area (and consequently more power) than six transistor cells. Other latch/memory cell designs employ spatial and/or temporal redundancy relative to the localized single-event charge deposition in a way that does not require a 2× increase in transistor count [115], but sacrifice performance in other ways (usually speed). While these cells can be appropriate for protecting critical data paths, they have not usually been suitable for very highly integrated circuits. Still, as the gap widens between state-of-the-art commercial fabrication processes and radiation-hardened processes, HBD techniques are becoming increasingly attractive. These circuit-hardening approaches are likely to be very important for future high-performance radiation-hardened ICs.

Mitigation of SEEs in combinational (or core) logic can involve redundant data paths (as described above) or the enhancement of data paths with proper choices of circuit types. An example is the elimination of all dynamic logic [116]. Because of its passive and highly charge-sensitive mode of operation, dynamic logic is highly vulnerable to SEEs, both space and terrestrial. Another method includes the choice of data path latches to include static or keeper-based designs [117].

System-level hardening approaches include the use of error detection and correction (EDAC) circuitry to monitor and correct memory errors as they occur [118]–[120]. This approach requires that extra bits of information be stored with the data to reconstruct the original data in the event of an upset. System overhead can be nonnegligible, but this is sometimes the only method available if relatively susceptible parts must be used. Another important technique is triple-modular redundancy (TMR), which can be implemented at the circuit, system board, or module level. Cruder methods such as watchdog timers, lockstep operation, majority voting, etc., are commonly used to detect control system errors [121]. While simple in concept, overhead can again be significant, but in many cases this is the only option available to the spacecraft engineer.

VII. Modeling Single-Event Mechanisms

From the earliest history of numerical device modeling, the radiation effects community has recognized the value of computational modeling for providing insight into the effects of ionizing radiation on microelectronic devices. In fact, pioneering work on one-dimensional drift-diffusion numerical modeling was presented at the NSREC as early as 1967 [122], [123], winning the Best Paper award for that year [122]. This early work focused on transient radiation response, as SEU would not be observed experimentally until several years later [2]. The development and use of numerical models for radiation effects has proceeded on many levels: the interaction of ionizing particles with matter, physical device simulators that predict the response of devices to incident radiation, circuit simulators that model circuit response to a single event, and codes that predict the error rate that will be observed for a specific part flying in particular orbit. In this paper, we will only review the models that most directly pertain to the actual upset process itself, namely device and circuit models that predict the response of devices and circuits to the ion track. Models for predicting error rates are covered elsewhere in this issue.

A. Physics-Based Device Models

The most commonly used formalism for device simulation is that of drift-diffusion models. In a drift-diffusion model, the semiconductor device equations are derived from the Boltzmann transport equation using numerous approximations. The equations to be solved are the Poisson equation and the current continuity equations, together with the constitutive relationships for current density (the actual drift-diffusion equations [124]). These equations are discretized and solved on a mesh using finite-difference or finite-element techniques [125]. Drift-diffusion models are highly evolved, and relatively speaking, not terribly computationally intensive, except in the case of 3-D models. Because of the assumptions they are based on, however, they are ill suited to treat many effects becoming important in small-geometry devices, such as velocity overshoot, carrier heating, and quasiballistic transport [124]. Nevertheless, due to their computational efficiency, they remain the workhorse simulation tool, even for deep submicron devices.

The next step up the device-simulation hierarchy is hydrodynamic and energy balance codes. Based on fewer assumptions, these codes begin to treat nonlocal effects, but are correspondingly more computer-intensive, based on five or six equations of state rather than the three of the drift-diffusion method [124].

The top rung of the device simulation ladder is Monte Carlo simulation, which makes the fewest assumptions and approximations [124]. Rather than being based on approximations to complicated macroscopic equations, Monte Carlo methods describe carrier transport on a fundamental, microscopic scale using classical equations of motion (e.g., Newton's first law). The motion of individual carriers is followed as they drift in fields and interact with scattering centers until statistical significance is achieved. Few assumptions are involved other than transport is described using classical physics. The penalty is very high computational intensity as the trajectories of many thousands of particles must be tracked to attain meaningful statistics.

B. Multidimensional Device Simulations

One of the many challenges of device simulation of radiation effects is the need for advanced 3-D modeling tools. The inherently 3-D nature of an ion passing through a microelectronic device is difficult to address with the 2-D simulation programs that are routinely used in the semiconductor industry for device analysis. The development of full 3-D tools has been fairly recent, however, and much insight has been gained in the past through the use of 2-D programs [48], [50], [61], [74], [76], [77], [126]–[133].

In a 2-D rectangular simulation, all quantities are assumed to be extruded into the third dimension, and hence *either* the correct generated charge density *or* the correct total charge can be simulated, not both. Scaling schemes have been proposed that adjust the Auger recombination rate in an attempt to correct for geometry effects [129]. Another method is to use *quasi*-3-D versions of the popular PISCES-II code, based on cylindrical symmetry and coordinate transformations [134]. Many charge collection and SEU studies have been performed using these modified 2-D codes [53], [135]–[138]. Unfortunately, there are few devices that exhibit circular symmetry, although through clever use of geometrical approximations, cylindrically symmetric simulations have proven revealing and surprisingly accurate in some cases [78]. Full 3-D device codes are necessary to model the effects of angled ion strikes [62], [139].

Fully 3-D device simulators were first reported in the literature in the early 1980s [140], and some of the early work on 3-D device simulation was motivated by alpha-particle reliability issues [141], [142]. An early comparison of 2-D and 3-D charge-collection simulations showed that while the transient responses were qualitatively similar, significant quantitative differences existed, both in the magnitude of the current response and the time scale over which collection was observed [143]. The implication of these results is that while 2-D simulations may provide basic insight, 3-D simulation is necessary if truly *predictive* results are to be obtained. Throughout the 1980s, companies developed internal 3-D device simulators, but most of these were proprietary and optimized for supercomputers. Only in the 1990s did numerical techniques and microprocessor speeds improve sufficiently to bring such tools to the desktop workstation. In the last several years fully 3-D device simulators have become commercially available [144]–[147]. Optimized for high-end workstations, a fairly large 3-D simulation can generally be performed in a few hours.

C. Circuit Simulations

In the previous sections, we discussed physics-based device models that simulate the charge collection in a device following an ion strike. Stepping up in a hierarchical view, these models can be incorporated into macro-models of the devices interconnected in a subcircuit. The macro view of the circuit will relate the collection of charge in individual device junctions to changes in the circuit currents and voltages.

A common circuit model for the charge collection at a junction due to direct funneling or diffusion is a double-exponential, time-dependent current pulse [148]. Typical parameters of this pulse are a rise time on the order of tens of picoseconds and a fall time on the order of 200 to 300 ps [68]. The actual magnitude and time profile of the current model depend on material parameters, the ion species, the ion energy, device dimensions, and the hit location relative to the junction. If the time profile of the collection current is not important to the circuit response to the hit, then analytical current models such as these usually adequately describe the induced current pulse. If, however, the time profile is critical to the circuit response, more accurate models for the current pulse are necessary, such as those from a device simulation.

Historically, it has become common practice to use the total charge delivered by the current waveform as a single descriptor of the particle strike's impact on the affected circuit node. This can be an extremely dangerous simplification, since it assumes the time profile of the charge delivery to a sensitive node is unimportant to its response [58]. From this simplification comes the concept of critical charge, $Q_{\rm crit}$. $Q_{\rm crit}$ is a property of the particular circuit (not the ion or environment) and is defined as the minimum charge delivered by the transient current waveform that causes that circuit to be upset. Of course, $Q_{\rm crit}$ tells nothing about the time profile of the delivery of that charge. Critical charge is commonly used as a figure of merit in the comparison of circuit design types and technologies. The quantity describes the relative vulnerability of a circuit to single events without the complications of ion species, ion energies, LET, or type of charge collection.

The importance (or lack thereof) of the precise time profile of SE current models depends entirely on the dominant high-frequency pole associated with the circuit's hit node, given by the open-circuit time constant (total node capacitance and equivalent ac resistance) seen by the current source. That is, the hit node acts as a low-pass filter, integrating the charge delivered to the node by the SE current pulse. If the response of the circuit at the collecting node is much slower than the characteristic time constant of the SE pulse, then the pulse is effectively integrated by the nodal capacitance and only the total charge delivered by the pulse is important to the circuit response. If, however, the time constant at the node is much shorter than the time constant of the SE pulse, then the circuit responds to the delivered charge faster than the pulse can deliver it, so the pulse shape is critically important to the circuit response. These concepts are essential to the accurate modeling of SEUs at the circuit level, since they define the boundary between valid modeling using only the collected charge and modeling requiring a more accurate description of the time profile of the charge collection.

Deterministic circuit simulation of both memory elements and logic circuitry has been effectively performed in the circuit domain using industry standard analysis codes such as Berkeley SPICE, Synopsys HSPICE, Orcad PSPICE, Cadence Spectre, and others. Using these techniques, hardened memory designs have been explored and the propagation of SETs in core logic has been studied. However, as circuits grow exponentially in density and complexity, comprehensive circuit simulation is impractical. Over the past decade, other methods to track radiation vulnerability at the circuit level have emerged, primarily in the realm of core logic.

In the mid 1990s, Baze and Buchner performed a series of circuit simulations and laser experiments on combinational logic to extract general properties of single-event propagation [23], [149]. They concluded that: 1) the soft error rate is independent of the frequency in latch circuits when the setup and hold time is much less than clock period; 2) the soft error rate increases linearly with the operating clock frequency in the combinational circuits; and 3) soft errors in latch circuits dominate in present day technologies, but the errors in the combinational circuits will dominate in future technologies.

In 1997, Massengill *et al.* [150] presented a probabilistic description of single-event fault generation, propagation, and logic error events using a high-level VHDL circuit description. This method was demonstrated in simulation code at NSREC in 2000 [151]. Seifert *et al.* [24], [117] have presented an analytical description of core logic soft error vulnerability based on the "window of vulnerability" of in-data-path static and dynamic latch elements, the synchronous clock, and other deterministic elements.

D. Mixed Device/Circuit Simulations

It should be obvious from the preceding sections that the tight coupling of device and circuit response to incident particle strikes significantly complicates SEU modeling. In SRAMs, for example, device modeling of the struck transistor with typical constant boundary conditions (or even including passive, lumped elements) will never result in an upset being observed in the simulation—by construction the device will always return to its prestrike state. The best that can be done in this situation is to study the charge-collection characteristics of the struck device and compare the collected charge to some critical charge to upset. However, the usefulness of this approach is extremely limited for SRAMs, since the charge-collection characteristics are greatly influenced by external loading and the feedback mechanism in latches [58]. Nevertheless, unloaded device simulation has been useful for studying the basic physical properties of charge collection, and for studying DRAMs, where loading effects are not as prevalent and critical charge is well defined by noise margins [19].

As discussed in the previous section, for studying the upset process itself in SRAMs, circuit simulation has been a useful tool. One strength of this approach is the large scale of the circuit in question that can be modeled; another is its computational efficiency. A drawback is the accuracy of the transient current used as the input stimulus. For example, if the current is based on device simulations of a struck, unloaded device [152], then the circuit simulation inherits the inaccuracy of the improperly loaded device simulation. Still, circuit simulations have provided considerable insight into SEU in memories and have resulted in improvements to hardening techniques for a variety of circuits [12], [87], [103], [153], [154].

Recently, the simultaneous solution of device and circuit equations has been increasingly used. This technique, known as *mixed-mode* or *mixed-level* simulation, was developed by Rollins at USC/Aerospace in the late 1980s [155]. The term "mixed-level" is probably less confusing and more descriptive than "mixed-mode." In a mixed-level simulation of SEU, the struck device is modeled in the "device domain" (i.e., using multi-dimensional device simulation), while the rest of the memory cell is represented by SPICE-like compact circuit models, as illustrated in Fig. 9 [58]. The two domains are tied together by the boundary conditions at contacts, and the solution to both sets of equations is rolled into one matrix solution [155], [156]. The advantage is that only the struck device is modeled in multiple dimensions, while the rest of the circuit consists of computationally efficient SPICE models. This decreases simulation times and greatly increases the complexity of the external circuitry that can be modeled. Mixed-level capability has been incorporated into most of the commercially-available 3-D device codes [144]–[147]. These codes were first used to study SEU in CMOS SRAMs in 1991 [157] and since then have received a great deal of continued use for this purpose [49].

E. Recent Enhancements

A drawback of the mixed-level method is that coupling effects between adjacent transistors have been shown to exist at the device level using 2-D simulations [129]. These effects cannot be taken into account when only the struck device is modeled at the device level. To address this difficulty, it is necessary to simulate the entire SRAM cell in the 3-D device domain [158]. An illustration of the technique is shown in Fig. 10 [93]. Fig. 10(a) shows a top-down view of the SRAM cell layout, while Fig. 10(b) shows the actual computational mesh used for simulations. When compared to the results of standard mixed-level simulations, it has been found that in cases where no coupling effects between transistors exist, mixed-level simulations are adequate to reproduce the full SRAM cell results. For some strike locations, however, coupling effects between adjacent transistors are observed [158], [159]. Mixed-level simulations are incapable of predicting such effects. As interdevice spacing decreases with increasing integration levels, coupling effects can be expected to become more important, and simulating the entire SRAM cell in the device domain may become routinely necessary [158].

Standard single-point (i.e., one ion strike location) 3-D mixed-level simulations are known to predict upset thresholds in very good agreement with measured thresholds [63]. In these simulations, the most sensitive strike location is assumed based on past experience. However, error rates in ICs are dependent not only on the threshold LET, but also on the sensitive area, which cannot be obtained from a single-point simulation. Researchers have generated simplified step-function cross-section curves from theoretical and simulation results by making assumptions about the sensitive area [160], [161]. Charge-collection contours in an SOI transistor have also been calculated using 2-D simulations [162]. Using a customized version of a commercial 3-D device simulator running on a large parallel computer, researchers have recently demonstrated the ability

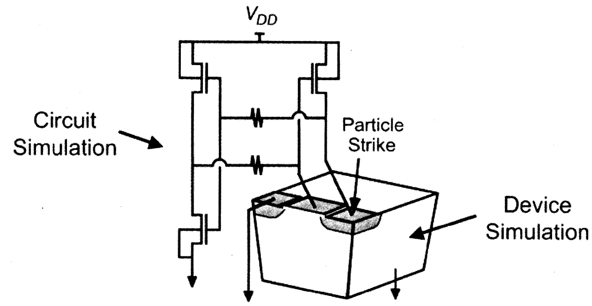


Fig. 9. Mixed-mode simulation structure for SRAM cells. Iillustration is of an n-channel "off" drain strike [58].

to directly compute the upset cross section of an SRAM [93]. These simulations were based on full-cell simulations, but separate simulations were performed for ion strikes incident every 0.5 μm throughout an SRAM unit cell. One set of simulations gave a map of the SEU-sensitive area of the SRAM unit cell for a given ion and energy. By repeating the simulations for several ion/energy combinations, the authors generated the evolution of the sensitive area as a function of ion LET, as shown in Fig. 11. Combining the information in the individual upset maps, the full upset cross-section curve was predicted and found to be in excellent agreement with experimental results [93]. The simulated cross section curve was based on nearly 7000 individual soft error simulations and took about 3 months to perform on 30 nodes of a parallel computer. Continued advances in computational power may make such simulations more feasible in the future.

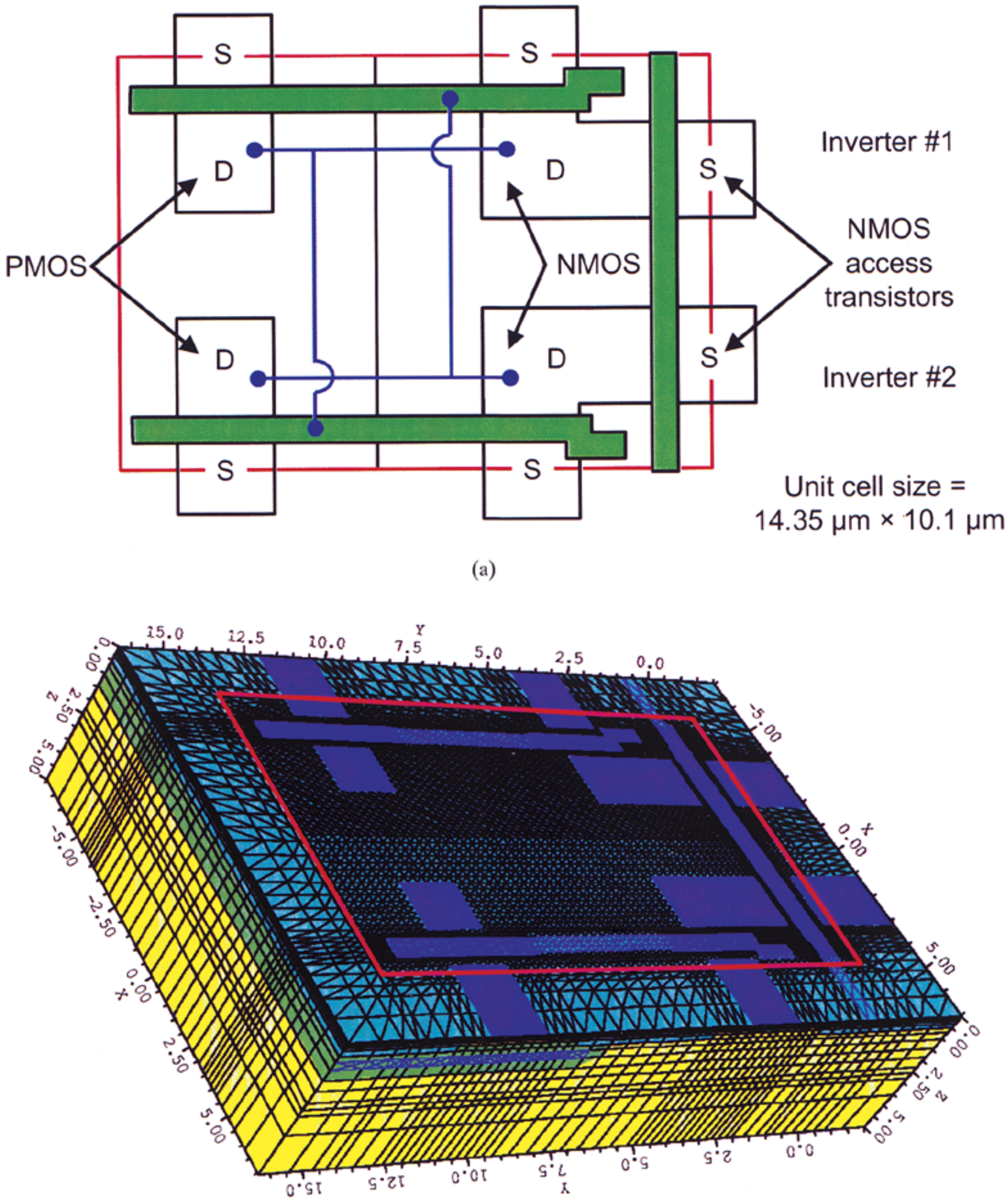
Techniques like mixed-level simulation are useful for in-depth studies of SEU in specific small-scale circuits and for given ion strikes. A system designer, however, is more likely to be interested in the total error rate for a large circuit containing many transistors and operating in some particular environment of interest. Because this is a very difficult problem, requiring detailed environmental models, the probability that a given ion strike causes an SEU is usually treated using analytical methods such as the rectangular parallelepiped (RPP) model. Typical methods of solution are covered elsewhere in this issue. Two groups have recently reported on large-scale SEU simulation systems that are aimed at predicting system error rates using a more first-principles basis of the interaction of ions with devices [163]–[165].

VIII. Future Trends

One of the biggest concerns for SEU is how technology trends will impact device susceptibility in the future. In this section, we discuss key technology drivers, how technology trends may affect hardening strategies, and the phenomenon of SEEs in ground-based and aircraft microelectronics, a topic of growing concern as devices become more susceptible to SEU.

A. Technology Drivers Impacting SEEs

Key technology parameters that influence SEU sensitivity include gate length, gate and drain area, and power supply voltage. If all parameters are taken into account, the overall trend is a general increase in SEU susceptibility with each



(a)

(b)

Fig. 10. (a) Layout of 256K six-transistor SRAM unit cell (D = drain and S = source). Red box indicates the boundaries of the unit cell, green regions are the gate polysilicon lines, and blue lines show the interconnections within the unit cell. (b) View of 3-D unit cell as laid out in device simulator. Mesh size is approximately 100 000 points [93].

technology generation. This trend is shown in Fig. 12, which is a plot of the simulated and experimentally measured SEU threshold for SRAMs without feedback resistors in three recent Sandia CMOS technologies [63]. A factor that is at least as important as the fundamental changes to the physics is simply the reduction in total capacitance as technologies shrink. Remember that the feedback time for the SRAM cell is to first order related to the RC delay in the inverter pair. As device areas shrink, the gate and drain capacitance shrinks, making the device faster but consequently much more susceptible to SEU. SEU is therefore a grave concern for scaled technologies.

Another area that is becoming increasingly important is the propagation of SETs in digital logic circuits. The problem here is that as circuit speeds rise, the probability that a momentary glitch will be clocked as valid data and propagated through the logic path increases. For example, in Fig. 6 we saw that even a particle well below the upset threshold can cause a momentary flip in the state of an SRAM cell. Consider the case where this memory cell is actually a latch circuit in a microprocessor. In the example of Fig. 6, if this latch value is read 10 ps after an ion strike and the value is clocked down the line, it matters little that the struck latch eventually returns to its original state, because the corrupt value has already been passed on to the next stage of the circuit. These types of errors are likely to become a pervasive problem as clock speeds continue to increase and will be difficult to protect against, especially in commercial mi-

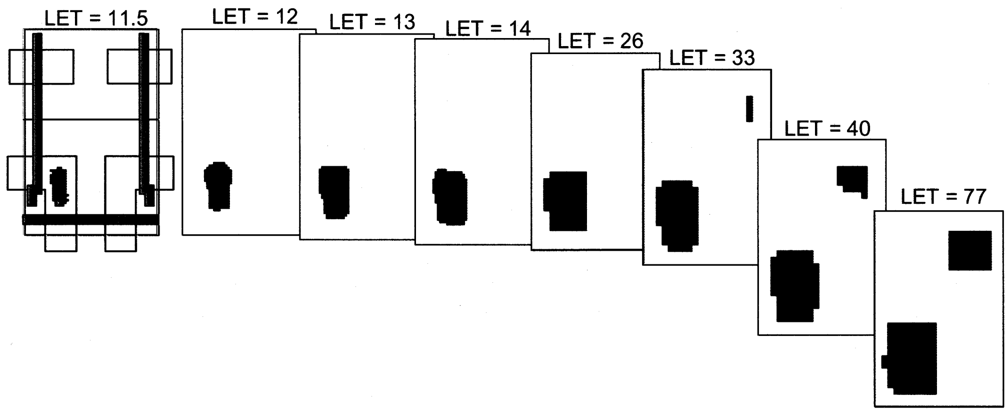


Fig. 11. Evolution of the soft-error sensitive area (black regions) of a 256K SRAM unit cell without feedback resistors as a function of increasing ion LET. Note increasing sensitive area of reverse-biased NMOS drain. At an LET of 33 MeV-cm^2/mg, the reverse-biased PMOS drain also becomes SEU-susceptible.

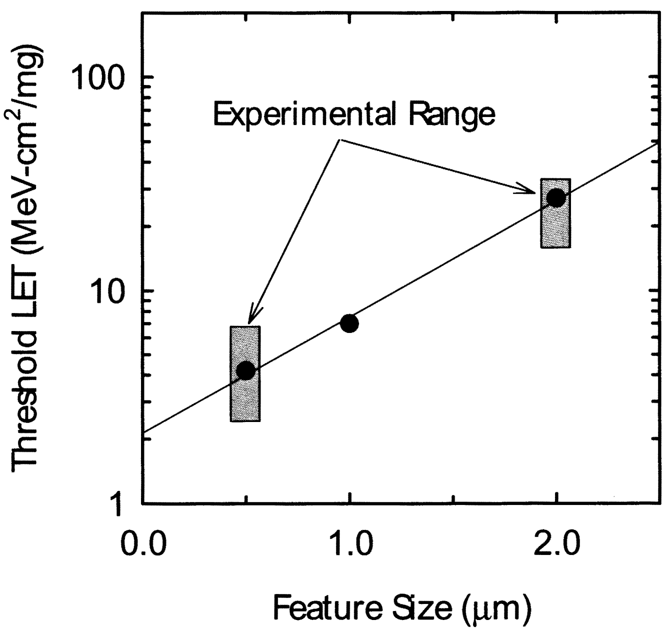


Fig. 12. Overall SEU threshold LET technology trend for three generations of Sandia CMOS SRAMs without feedback resistors [63]. Points are the results of 3-D mixed-level simulations, and shaded regions are the measured range.

croprocessors where speed is paramount. It has been predicted that for circuits built in technologies below 0.35 μm, propagated SETs will be a primary SE failure mode [115]. Temporal sampling circuit approaches have been developed that prevent the propagation of SETs and also provide the equivalent of triple spatial redundancy [115].

B. Hardening Design Strategies

A considerable concern for SRAMs requiring SEU hardness in the future is whether traditional resistive hardening techniques will remain a viable option. The resistive decoupling technique is fundamentally incompatible with high speed because it relies on slowing the cell down so that it cannot respond quickly to SEU voltage transients. This tends to mean that the write performance of hardened SRAM cells has to be kept at a nearly constant level to maintain a constant level of SEU hardness. Also, because a smaller, faster SRAM cell has lower capacitance, the feedback resistance required to harden the cell has to be raised to compensate. Such large resistors are very difficult to controllably manufacture and show a significant temperature dependence [101]. Because of this problem and stagnant performance levels, it is likely that for applications requiring a high level of SEU hardness, devices below about 0.5-μm will utilize other hardening techniques, such as SOI, active feedback elements, or circuit hardening.

C. Terrestrial and High-Altitude SEEs

Much of this review has concentrated on the natural space radiation environment and its effect on microelectronics. A radiation environment also exists in the Earth's atmosphere and, although less harsh than the space environment, it can also give rise to SEE. The terrestrial radiation environment is covered elsewhere in this issue and will not be described here; in this section, we briefly discuss the interaction of this environment with microelectronics in aircraft systems and at ground level.

As discussed in Section II, SEU in terrestrial electronics was discovered in the late 1970s and was recognized as a significant reliability concern. However, after considerable early activity, the terrestrial soft error problem was effectively alleviated by using low-activity materials and on-chip shielding coatings [5], [6]. Occasionally, changes in suppliers or procedures have caused semiconductor manufacturers temporary but considerable headaches due to raised radioactive contaminant levels in materials such as nitric and phosphoric acid [5], [166]. The march toward higher integration densities has made soft-error concerns a continual design consideration for advanced DRAM and SRAM development in the last decade. A particular area of recent concern is flip-chip packaging technologies that place a source of alpha particles (Pb-Sn solder bumps) right on the die itself, where they cannot be shielded by coating layers [167]. Elimination of materials rich in ^{10}B, such as BPSG dielectric layers, has been shown to reduce the thermal neutron soft error rate (SER) by several orders of magnitude [168], [169].

Even in the absence of on-chip sources of radiation, recent studies have conclusively proved that terrestrial cosmic rays (primarily neutrons) are a significant source of soft errors in both DRAMs and SRAMs [170]–[172]. Upsets have been observed both at ground level and in aircraft and have been convincingly correlated to the altitude and latitude variation of the neutron flux [173], [170], [172]. Lage *et al.* have shown that even without alpha particles, a baseline of cosmic-ray upsets still exists for high-density SRAMs [171]. O'Gorman has shown that neutron upsets disappear for DRAMs placed 200 m underground in a salt mine, while they increase dramatically for systems operated above 10 000 feet in Leadville, CO [170]. In addition to SEU observed in memories used in large computer systems and aircraft, upsets have been observed in SRAMs used in implantable medical devices such as cardiac defibrillators [174].

Fig. 13 shows the measured cosmic-ray neutron SER versus power supply voltage in several generations of SRAMs from a variety of vendors [175]. Terrestrial soft error failure rate specifications are usually given in terms of FIT rates, where FIT = Failure in Time = 1 error in 10^9 device hours. In this figure, SER is reported in FIT/Mb of memory to allow comparison between memories of different sizes. For reference, an uncorrected SER of 1000/Mb would lead to one error every three weeks in a system with 256 MB of memory. From this figure, it is clear that low-voltage SRAMs exhibit unacceptably high SER without error correction and that different IC technologies can have SER varying by two orders of magnitude at a given voltage.

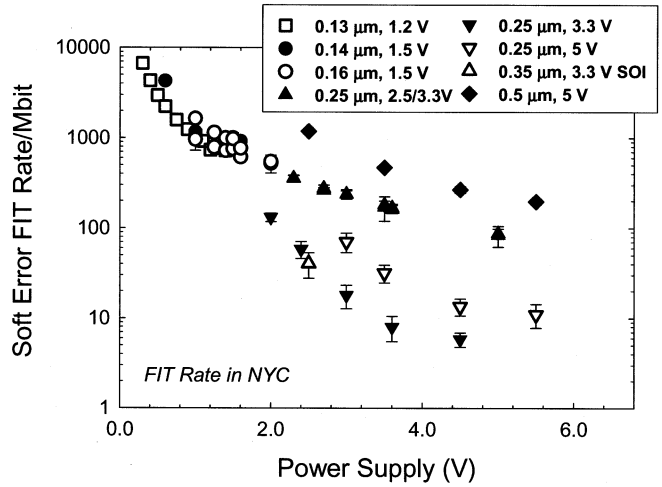


Fig. 13. Soft error failure rate as a function of power supply voltage for SRAMs manufactured in several different technologies by several vendors [175].

Destructive SEEs can also occur in ground-based systems. For example, neutron-induced single-event burnout has caused destructive failures in large-area high-voltage power diodes used for railroad applications in Europe [176]. It has recently been experimentally demonstrated that significant neutron-induced latchup rates can occur in high-density SRAMs at ground level [175].

Revelations such as these have significant implications for manufacturers of commercial memory chips and computer systems, because systems cannot realistically be shielded against incident neutrons. Meeting specified failure rates is expected to be a significant challenge for commercial semiconductor manufacturers. A typical specification is to maintain a FIT rate less than 1000 [171]. A complicating factor is that since FIT rates are often specified *per device*, meeting a constant FIT rate specification actually requires reducing the error rate *per bit* as the number of bits per device is increased.

It has been suggested that because manufacturers of commercial microelectronics for terrestrial applications have had to deal with alpha-particle-induced upsets from packaging materials, commercial parts will by design remain hard to at least the alpha-particle threshold [177]. Indeed, there is historical evidence supporting this view as data from more than ten years of microprocessor evolution show a constant upset threshold just above the threshold for alpha particle upset [177]. However, it is also known that many manufacturers have specific soft-error driven design rules for placement of devices relative to on-chip solder bumps and/or use hardened circuit designs for I/O circuitry that must be in the vicinity of such on-chip alpha sources [178]. This clearly implies that many devices being manufactured are in fact already below the alpha-particle threshold for upset.

Many of the techniques traditionally used in the radiation effects community to SEU-harden devices are of such a nature that they are unlikely to be adopted by commercial manufacturers. They tend to consume more power, reduce manufacturability, and severely impact IC performance. Commercial DRAMs have generally exhibited a fairly constant SEU performance because DRAM manufacturers have intentionally maintained the unit cell capacitance through the use of clever modifications to the storage cell [19], [22]. The nodal capacitance for SRAMs, however, has been steadily shrinking [171]. To counteract increased terrestrial SERs, manufacturers may find it necessary to explicitly add capacitance to high-density SRAMs [107], [171]. Lage has predicted that this will be necessary for the 4 Mb generation of SRAMs and beyond [171]. Design-hardened circuits may be useful for critical logic paths or circuitry, but because of area penalties will likely not be adopted on a large scale except as a last resort. The use of error-correcting memory architectures is already becoming more common again and this trend will likely continue. Mitigating soft errors in high-speed digital logic circuits will be especially challenging. Fault-tolerant systems are routinely used in aircraft mechanical systems and seem a natural choice for preventing neutron-induced SEU in avionics [179]. SOI is a possible solution to the terrestrial SEU problem, although as noted previously SOI is not automatically upset immune. In any event, the fact that commercial manufacturers will be studying SEU should prove beneficial to the radiation effects community inasmuch as it brings new resources to bear on the problem.

D. Effects of Technology Node Advancement

Rarely is modern technology scaling manifest as simple lithography shrinks; concomitant changes in materials, designs, and circuit topologies accompany any movement from one technology node to the next. Thus, future progress of integrated circuit technologies impacts SEE tolerance on a variety of levels—potential new material particle emissions, reduced noise margins due to scaling, increased sensitivity due to new circuit topologies, increased operational speed, and the increased probability for errors due to ever-increasing density of information storage and processing. It is because of this uncertainty that SE vulnerability has been, and continues to be, a significant reliability concern across the industry.

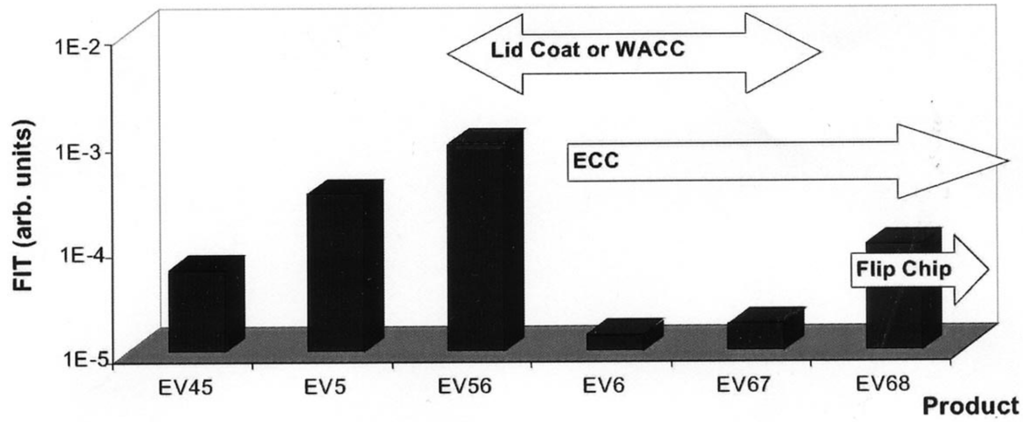


Fig. 14. Experimentally observed FIT rates for the DEC/Compaq Alpha microprocessor exposed to alpha-particles as a function of technology generation node as defined in the text [20].

One modern integrated circuit that has seen significant soft error analysis and design throughout its developmental life is the DEC Alpha microprocessor. The historical trend in alpha-particle induced soft error rates of the Alpha microprocessor has not been monotonic as the device has matured, both in design and fabrication technology, from one generation to the next. This example illustrates the synergistic effects impacting single-event vulnerability as a design surmounts several technology generations.

As an example of this point, Fig. 14 shows the measured soft error FIT rate for Alpha microprocessors as a function of technology node, starting with a 0.5-μm, 3.3-V technology (EV45) with 32 kB of on-chip cache, and maturing to a 0.18-μm, 1.6-V technology with 128 kB of on-chip cache (EV68) [20].

Before the implementation of ECC protection, the chip-level SER had steadily increased from EV45 to EV5 (0.5-μm, 3.3-V, 112-kB cache) to EV56 (0.35-μm, 2.5-V, 120-kB cache) as would be expected with increased cache (a dominant contributor to SEE), reduced feature size, and reduced power supply voltage. However, the increase in vulnerability between EV5 and EV56 (a technology shrink) is not as pronounced as would be expected based on simple scaling calculations. This is due to the addition of a lid coating and a wirebond-attached chip capacitor (WACC) between the package and the surface of the chip, thus diminishing particle interactions from the packaging material. The bulk of the remaining SEEs in the EV56 design have been attributed to alpha-particle emissions from the interconnect stack.

Following the implementation of ECC in the EV6 (0.35-μm, 2.2-V, 128-kB cache), a dramatic reduction in SEE vulnerability is seen, even though process scaling continues. This reduction is enhanced by design modifications of the EV6, including the incorporation of new data-path latch designs that are static rather than dynamic in operation [20].

Scaling to the EV67 (0.25-μm, 2.0-V, 128-kB cache) shows an increase in vulnerability, clearly due to process scaling. However, as in previous cases, this increase is not as high as would be expected due to simple scaling rules. It has been determined that the increase in sensitivity due to lowered power supply voltage and nodal capacitances has been moderated by the reduced charge collection efficiency of the 0.25-μm technology [20].

Finally, the evolution of the Alpha processor to the EV68 (0.18-μm, 1.6-V, 128-kB cache) shows a striking increase in SEE vulnerability. This has been attributed to the introduction of flip-chip packaging due to the particulate emissions from the lead bump material.

IX. Summary

Nondestructive SEE are caused by charge deposition by direct ionization from heavy ions and indirect ionization from protons and neutrons. The deposited charge can be collected by drift and diffusion in semiconductor devices, causing current transients that can result in circuit malfunction. Funneling can increase the charge collected due to drift processes and is especially important for DRAMs and devices not fabricated on epitaxial substrates. In SRAMs, voltage transients can cause upsets by mimicking the write process. In complex and high-speed circuits such as microprocessors, even a momentary glitch can propagate through an IC to cause upsets. Multiple-bit upsets occur when more than one bit in a digital circuit is upset by a single particle strike.

Mitigation techniques for SEU include system-level methods such as error detection and correction, lockstep execution, and redundant systems using voting. Circuit-level methods are also effective, and several SEU-hardened latch designs have been proposed. These techniques have the advantage of allowing the use of commercial fabrication technologies but usually lead to greatly increased transistor counts and area penalties. Traditional radiation-hardened circuits use process techniques such as lightly doped polysilicon feedback resistors to provide SEU immunity. While very effective, passive feedback elements reduce circuit performance and degrade IC manufacturability.

Simulations of SEE have been crucial to developing an understanding of the mechanisms behind SEE and for suggesting methods for hardening devices. As devices continue to evolve to smaller dimensions, device-level modeling will encounter new challenges such as the ion strike affecting more than a single transistor at a time. A greater level of usefulness can be reached when simulation tools prove to be validated and predictive. At this level, simulations become essential during the design process for reducing the number of "fab-and-test" cycles that must be completed to develop radiation-hardened technologies.

Technology trends are unfortunately such that SEE are likely to become even more of a concern for the future. Decreasing feature sizes, lower operating voltage, and higher speeds all conspire to increase susceptibility to SEU. Upset in avionics is an established concern. Upset at the ground level will continue to be an increasing concern for manufacturers of microelectronics for terrestrial applications. The use of flip-chip packaging and multiple levels of metals will further exacerbate the problem. Typical methods of mitigation that either increase the transistor count or reduce IC performance will likely not be acceptable to commercial manufacturers, and new methods will need to be developed. SOI technology may help in this regard, but is not a magic bullet to end all SEE concerns. Hopefully, the fact that commercial manufacturers must deal with SEE concerns will provide a collateral benefit to the radiation effects community as more resources are brought to bear on the problem.

ACKNOWLEDGMENT

The first author is grateful for the continuing support, encouragement, and camaraderie of the Radiation Physics, Simulation and Technology Department at Sandia National Laboratories. Were it not for the accumulated expertise in the department, the understanding of basic mechanisms of single-event effects represented in this paper would not have been possible. The second author is grateful to the Radiation Effects Research Group, Vanderbilt University, for providing such a rewarding place to collaborate. The frequent technical discussions, joint technical ventures, and friendship have made many things possible.

REFERENCES

[1] J. T. Wallmark and S. M. Marcus, "Minimum size and maximum packing density of nonredundant semiconductor devices," *Proc. IRE*, vol. 50, pp. 286–298, 1962.

[2] D. Binder, E. C. Smith, and A. B. Holman, "Satellite anomalies from galactic cosmic rays," *IEEE Trans. Nucl. Sci.*, vol. 22, pp. 2675–2680, Dec. 1975.

[3] T. C. May and M. H. Woods, "Alpha-particle-induced soft errors in dynamic memories," *IEEE Trans. Electron. Devices*, vol. 26, pp. 2–9, Feb. 1979.

[4] *IEEE Int. Reliability Physics Symp.*, numerous papers in the 1978-1980 proc..

[5] J. F. Ziegler, H. W. Curtis, H. P. Muhlfeld, C. J. Montrose, B. Chin, M. Nicewicz, C. A. Russell, W. Y. Yang, L. B. Freeman, P. Hosier, L. E. LaFave, J. L. Walsh, J. M. Orro, G. J. Unger, J. M. Ross, T. J. O'Gorman, B. Messina, T. D. Sullivan, A. J. Sykes, H. Yourke, T. A. Enger, V. Tolat, T. S. Scott, A. H. Taber, R. J. Sussman, W. A. Klein, and C. W. Wahaus, "IBM experiments in soft fails in computer electronics (1978–1994)," *IBM J. Res. Develop.*, vol. 40, no. 1, pp. 3–18, 1996.

[6] T. C. May, "Soft errors in VLSI: Present and future," *IEEE Trans. Components, Hybrids, Manuf. Tech.*, vol. 2, pp. 377–387, Dec. 1979.

[7] J. C. Pickel and J. T. Blandford, Jr., "Cosmic ray induced errors in MOS memory cells," *IEEE Trans. Nucl. Sci.*, vol. 25, pp. 1166–1171, Dec. 1978.

[8] R. C. Wyatt, P. J. McNulty, P. Toumbas, P. L. Rothwell, and R. C. Filz, "Soft errors induced by energetic protons," *IEEE Trans. Nucl. Sci.*, vol. 26, pp. 4905–4910, Dec. 1979.

[9] C. S. Guenzer, E. A. Wolicki, and R. G. Allas, "Single event upset of dynamic RAM's by neutrons and protons," *IEEE Trans. Nucl. Sci.*, vol. 26, pp. 5048–5053, Dec. 1979.

[10] W. A. Kolasinski, J. B. Blake, J. K. Anthony, W. E. Price, and E. C. Smith, "Simulation of cosmic-ray induced soft errors and latchup in integrated-circuit computer memories," *IEEE Trans. Nucl. Sci.*, vol. 26, pp. 5087–5091, Dec. 1979.

[11] J. L. Andrews, J. E. Schroeder, B. L. Gingerich, W. A. Kolasinski, R. Koga, and S. E. Diehl, "Single event error immune CMOS RAM," *IEEE Trans. Nucl. Sci.*, vol. 29, pp. 2040–2043, Dec. 1982.

[12] A. E. Giddings, F. W. Hewlett, R. K. Treece, D. K. Nichols, L. S. Smith, and J. A. Zoutendyk, "Single event upset immune integrated circuits for Project Galileo," *IEEE Trans. Nucl. Sci.*, vol. 32, pp. 4159–4163, Dec. 1985.

[13] T. C. May, G. L. Scott, E. S. Meieran, P. Winer, and V. R. Rao, "Dynamic fault imaging of VLSI random logic devices," in *Proc. Int. Reliability Physics Symp.*, Las Vegas, NV, 1984.

[14] S. E. Diehl-Nagle, J. E. Vinson, and E. L. Peterson, "Single event upset rate predictions for complex logic systems," *IEEE Trans. Nucl. Sci.*, vol. 31, pp. 1132–1138, Dec. 1984.

[15] A. L. Friedman, B. Lawton, K. R. Hotelling, J. C. Pickel, V. H. Strahan, and K. Loree, "Single event upset in combinational and sequential current mode logic," *IEEE Trans. Nucl. Sci.*, vol. 32, pp. 4216–4217, Dec. 1985.

[16] K. J. Hass, R. K. Treece, and A. E. Giddings, "A radiation-hardened 16/32-bit microprocessor," *IEEE Trans. Nucl. Sci.*, vol. 36, pp. 2252–2257, Dec. 1989.

[17] R. Ronen, A. Mendelson, K. Lai, L. Shih-Lien, F. Pollack, and J. P. Shen, "Coming challenges in microarchitecture and architecture," *Proc. IEEE*, vol. 89, p. 325, Mar. 2001.

[18] C. Dai, N. Hakim, S. Hareland, J. Maiz, and S. W. Lee, "Alpha-SER modeling and simulation for sub-0.24μm CMOS technology," in *Proc. Symp. VLSI Tech.*, 1999, p. 81.

[19] L. W. Massengill, "Cosmic and terrestrial single-event radiation effects in dynamic random access memories," *IEEE Trans. Nucl. Sci.*, vol. 43, pp. 576–593, Apr. 1996.

[20] N. Seifert, D. Moyer, N. Leland, and R. Hokinson, "Historical trends in alpha-particle induced soft error rates of the Alpha microprocessor," in *Proc. Int. Reliability Physics Symp.*, 2000, pp. 259–265.

[21] S. Hareland, J. Maiz, M. Alavi, K. Mistry, S. Walsta, and C. Dai, "Impact of CMOS process scaling and SOI on soft error rates of logic processors," in *Proc. Symp. VLSI Tech.*, 2001, pp. 73–74.

[22] R. Baumann, "The impact of technology scaling on soft error rate performance and limits to the efficacy of error correction," in *IEDM Tech. Dig.*, 2002, pp. 329–332.

[23] S. Buchner, M. Baze, D. Brown, D. McMorrow, and J. Melinger, "Comparison of error rates in combinational and sequential logic," *IEEE Trans. Nucl. Sci.*, vol. 44, pp. 2209–2216, Dec. 1997.

[24] N. Seifert, X. Zhu, D. Moyer, R. Mueller, N. Leland, R. Hokinson, M. Shade, and L. Massengill, "Frequency dependence of soft error rates for sub-micron CMOS technologies," in *IEDM Tech. Dig.*, 2001.

[25] *Semiconductor Research Corp. Nat. Technology Roadmap*, 1999.

[26] J. Maiz and R. Baumann, "Radiation induced soft errors in silicon components and computer systems," in *Tutorial, Int. Reliability Physics Symp.*, Dallas, April 2002.

[27] F. Faccio, K. Kloukinas, A. Marchioro, T. Calin, J. Cosculluela, M. Nicolaidis, and R. Velazco, "Single event effects in static and dynamic registers in an a 0.25 μm CMOS technology," *IEEE Trans. Nucl. Sci.*, vol. 46, pp. 1434–1439, Dec. 1999.

[28] M. P. Baze, S. P. Buchner, and D. McMorrow, "A digital CMOS design technique for SEU hardening," *IEEE Trans. Nucl. Sci.*, vol. 47, pp. 2603–2608, Dec. 2000.

[29] P. E. Dodd, M. R. Shaneyfelt, D. S. Walsh, J. R. Schwank, G. L. Hash, R. A. Loemker, B. L. Draper, and P. S. Winokur, "Single-event upset and snapback in silicon-on-insulator devices and integrated circuits," *IEEE Trans. Nucl. Sci.*, vol. 47, pp. 2165–2174, Dec. 2000.

[30] G. Niu, R. Krithivasan, J. D. Cressler, P. A. Riggs, B. A. Randall, P. W. Marshall, R. A. Reed, and B. Gilbert, "A comparison of SEU tolerance in high-speed SiGe HBT digital logic designed with multiple circuit architectures," *IEEE Trans. Nucl. Sci.*, vol. 49, pp. 3107–3114, Dec. 2002.

[31] J. F. Ziegler, J. P. Biersack, and U. Littmark, *The Stopping and Range of Ions in Solids*. New York: Pergamon, 1985.

[32] E. L. Petersen, "Single event analysis and prediction," in *1997 IEEE NSREC Short Course*, Snowmass, CO.

[33] J. Barak, J. Levinson, M. Victoria, and W. Hajdas, "Direct processes in the energy deposition of protons in silicon," *IEEE Trans. Nucl. Sci.*, vol. 43, pp. 2820–2826, Dec. 1996.

[34] S. Duzellier, R. Ecoffet, D. Falguère, T. Nuns, L. Guibert, W. Hajdas, and M. C. Calvet, "Low energy proton induced SEE in memories," *IEEE Trans. Nucl. Sci.*, vol. 44, pp. 2306–2310, Dec. 1997.

[35] E. Petersen, "Soft errors due to protons in the radiation belt," *IEEE Trans. Nucl. Sci.*, vol. 28, pp. 3981–3986, Dec. 1981.

[36] F. Wrobel, J.-M. Palau, M. C. Calvet, O. Bersillon, and H. Duarte, "Incidence of multi-particle events on soft error rates caused by n-Si nuclear reactions," *IEEE Trans. Nucl. Sci.*, vol. 47, pp. 2580–2585, Dec. 2000.

[37] R. A. Reed, P. J. McNulty, and W. G. Abdel-Kader, "Implications of angle of incidence in SEU testing of modern circuits," *IEEE Trans. Nucl. Sci.*, vol. 41, pp. 2049–2054, Dec. 1994.
[38] R. A. Reed, P. W. Marshall, H. S. Kim, P. J. McNulty, B. Fodness, T. M. Jordan, R. Reedy, C. Tabbert, M. S. T. Liu, W. Heikkila, S. Buchner, R. Ladbury, and K. A. LaBel, "Evidence for angular effects in proton-induced single-event upsets," *IEEE Trans. Nucl. Sci.*, vol. 49, pp. 3038–3044, Dec. 2002.
[39] P. J. McNulty, W. J. Beauvais, and D. R. Roth, "Determination of SEU parameters of NMOS and CMOS SRAMs," *IEEE Trans. Nucl. Sci.*, vol. 38, pp. 1463–1470, Dec. 1991.
[40] R. A. Reed, P. J. McNulty, W. J. Beauvais, and D. R. Roth, "Charge collection spectroscopy," *IEEE Trans. Nucl. Sci.*, vol. 40, pp. 1880–1887, Dec. 1993.
[41] P. J. McNulty, "Single-event effects experienced by astronauts and microelectronic circuits flown in space," *IEEE Trans. Nucl. Sci.*, vol. 43, pp. 475–482, Feb. 1996.
[42] R. S. Wagner, J. M. Bradley, C. J. Maggiore, J. G. Beery, and R. B. Hammond, "An approach to measure ultrafast-funneling-current transients," *IEEE Trans. Nucl. Sci.*, vol. 33, pp. 1651–1656, Dec. 1986.
[43] S. J. Heileman, W. R. Eisenstadt, R. M. Fox, R. S. Wagner, N. Bordes, and J. M. Bradley, "CMOS VLSI single event transient characterization," *IEEE Trans. Nucl. Sci.*, vol. 36, pp. 2287–2291, Dec. 1989.
[44] I. Nashiyama, T. Hirao, T. Kamiya, H. Yutoh, T. Nishijima, and H. Sekiguti, "Single-event current transients induced by high energy ion microbeams," *IEEE Trans. Nucl. Sci.*, vol. 40, pp. 1935–1940, Dec. 1993.
[45] F. W. Sexton, "Microbeam studies of single-event effects," *IEEE Trans. Nucl. Sci.*, vol. 43, pp. 687–695, Feb. 1996.
[46] S. Buchner, J. B. Langworthy, W. J. Stapor, A. B. Campbell, and S. Rivet, "Implications of the spatial dependence of the single-event upset threshold in SRAM's measured with a pulsed laser," *IEEE Trans. Nucl. Sci.*, vol. 41, pp. 2195–2202, Dec. 1994.
[47] H. Schöne, D. S. Walsh, F. W. Sexton, B. L. Doyle, P. E. Dodd, J. F. Aurand, R. S. Flores, and N. Wing, "Time-resolved ion beam induced charge collection (TRIBICC) in microelectronics," *IEEE Trans. Nucl. Sci.*, vol. 45, pp. 2544–2549, Dec. 1998.
[48] C. M. Hsieh, P. C. Murley, and R. R. O'Brien, "A field-funneling effect on the collection of alpha-particle-generated carriers in silicon devices," *IEEE Electron. Device Lett.*, vol. 2, pp. 103–105, Dec. 1981.
[49] P. E. Dodd, "Device simulation of charge collection and single-event upset," *IEEE Trans. Nucl. Sci.*, vol. 43, pp. 561–575, Feb. 1996.
[50] C. M. Hsieh, P. C. Murley, and R. R. O'Brien, "Collection of charge from alpha-particle tracks in silicon devices," *IEEE Trans. Electron. Devices*, vol. 30, pp. 686–693, Dec. 1983.
[51] C. M. Hsieh, P. C. Murley, and R. R. O'Brien, "Dynamics of charge collection from alpha-particle tracks in integrated circuits," in *Proc. IEEE Int. Reliability Phys. Symp.*, 1981, pp. 38–42.
[52] F. B. McLean and T. R. Oldham, "Charge funneling in n and p-type Si substrates," *IEEE Trans. Nucl. Sci.*, vol. 29, pp. 2018–2023, Dec. 1982.
[53] L. D. Edmonds, "A simple estimate of funneling-assisted charge collection," *IEEE Trans. Nucl. Sci.*, vol. 38, pp. 828–833, Feb. 1991.
[54] P. E. Dodd, F. W. Sexton, and P. S. Winokur, "Three-dimensional simulation of charge collection and multiple-bit upset in Si devices," *IEEE Trans. Nucl. Sci.*, vol. 41, pp. 2005–2017, Dec. 1994.
[55] L. D. Edmonds, "Charge collection from ion tracks in simple EPI diodes," *IEEE Trans. Nucl. Sci.*, vol. 44, pp. 1448–1463, June 1997.
[56] ——, "Electric currents through ion tracks in silicon devices," *IEEE Trans. Nucl. Sci.*, vol. 45, pp. 3153–3164, Dec. 1998.
[57] ——, "A time-dependent charge-collection efficiency for diffusion," *IEEE Trans. Nucl. Sci.*, vol. 48, pp. 1609–1622, Oct. 2001.
[58] P. E. Dodd and F. W. Sexton, "Critical charge concepts for CMOS SRAMs," *IEEE Trans. Nucl. Sci.*, vol. 42, pp. 1764–1771, Dec. 1995.
[59] E. Takeda, K. Takeuchi, D. Hisamoto, T. Toyabe, K. Ohshima, and K. Itoh, "A cross section of α-particle-induced soft-error phenomena in VLSIs," *IEEE Trans. Electron. Devices*, vol. 36, pp. 2567–2575, Nov. 1989.
[60] S. Velacheri, L. W. Massengill, and S. E. Kerns, "Single-event-induced charge collection and direct channel conduction in submicron MOSFETs," *IEEE Trans. Nucl. Sci.*, vol. 41, pp. 2103–2111, Dec. 1994.
[61] J. S. Fu, C. L. Axness, and H. T. Weaver, "Memory SEU simulations using 2-D transport calculations," *IEEE Electron. Device Lett.*, vol. 6, pp. 422–424, Aug. 1985.
[62] R. L. Woodruff and P. J. Rudeck, "Three-dimensional numerical simulation of single event upset of an SRAM cell," *IEEE Trans. Nucl. Sci.*, vol. 40, pp. 1795–1803, Dec. 1993.
[63] P. E. Dodd, F. W. Sexton, G. L. Hash, M. R. Shaneyfelt, B. L. Draper, A. J. Farino, and R. S. Flores, "Impact of technology trends on SEU in CMOS SRAMs," *IEEE Trans. Nucl. Sci.*, vol. 43, pp. 2797–2804, Dec. 1996.
[64] S. E. Kerns, L. W. Massengill, D. V. Kerns, Jr., M. L. Alles, T. W. Houston, H. Lu, and L. R. Hite, "Model for CMOS/SOI single-event vulnerability," *IEEE Trans. Nucl. Sci.*, vol. 36, pp. 2305–2310, Dec. 1989.
[65] O. Musseau, "Single-event effects in SOI technologies and devices," *IEEE Trans. Nucl. Sci.*, vol. 43, pp. 603–613, Feb. 1996.
[66] L. W. Massengill, D. V. Kerns, S. E. Kerns, and M. L. Alles, "Single event charge enhancement in SOI devices," *IEEE Electron. Device Lett.*, vol. 11, pp. 98–99, Feb. 1990.
[67] O. Musseau, V. Ferlet-Cavrois, J. L. Pelloie, S. Buchner, D. McMorrow, and A. B. Campbell, "Laser probing of bipolar amplification in 0.25-μm MOS/SOI transistors," *IEEE Trans. Nucl. Sci.*, vol. 47, pp. 2196–2203, Dec. 2000.
[68] L. W. Massengill, "SEU modeling and prediction techniques," in *IEEE NSREC Short Course*, 1993, pp. III-1–III-93.
[69] J.-S. Chern, P. Yang, P. Pattnaik, and J. A. Seitchik, "Alpha-particle-induced charge transfer between closely spaced memory cells," *IEEE Trans. Electron. Devices*, vol. 33, pp. 822–834, June 1986.
[70] R. J. McPartland, "Circuit simulations of alpha-particle-induced soft errors in MOS dynamic RAMs," *IEEE J. Solid-State Circuits*, vol. 16, pp. 31–34, Feb. 1981.
[71] T. Toyabe, T. Shinoda, M. Aoki, H. Kawamoto, K. Mitsusada, T. Masuhara, and S. Asai, "A soft error rate model for MOS dynamic RAM's," *IEEE J. Solid-State Circuits*, vol. 17, pp. 362–367, Feb. 1982.
[72] T. V. Rajeevakumar, N. Lu, W. Henkels, W. Hwang, and R. Franch, "A new failure mode of radiation-induced soft errors in dynamic memories," *IEEE Electron. Device Lett.*, vol. 9, pp. 644–646, Dec. 1988.
[73] J. F. Ziegler, M. E. Nelson, J. D. Shell, R. J. Peterson, C. J. Gelderloos, H. P. Muhlfeld, and C. J. Montrose, "Cosmic ray soft error rates of 16-Mb DRAM memory chips," *IEEE J. Solid-State Circuits*, vol. 33, pp. 246–252, Apr.. 1998.
[74] H. T. Weaver, "Soft error stability of p-well versus n-well CMOS latches derived from 2D, transient simulations," in *IEDM Tech. Dig.*, 1988, pp. 512–515.
[75] C. Detcheverry, C. Dachs, E. Lorfèvre, C. Sudre, G. Bruguier, J. M. Palau, J. Gasiot, and R. Ecoffet, "SEU critical charge and sensitive area in a submicron CMOS technology," *IEEE Trans. Nucl. Sci.*, vol. 44, pp. 2266–2273, Dec. 1997.
[76] C. L. Axness, H. T. Weaver, J. S. Fu, R. Koga, and W. A. Kolasinski, "Mechanisms leading to single event upset," *IEEE Trans. Nucl. Sci.*, vol. 33, pp. 1577–1580, Dec. 1986.
[77] H. T. Weaver, C. L. Axness, J. S. Fu, J. S. Binkley, and J. Mansfield, "RAM cell recovery mechanisms following high-energy ion strikes," *IEEE Electron. Device Lett.*, vol. 8, pp. 7–9, Jan. 1987.
[78] J. A. Zoutendyk, L. D. Edmonds, and L. S. Smith, "Characterization of multiple-bit errors from single-ion tracks in integrated circuits," *IEEE Trans. Nucl. Sci.*, vol. 36, pp. 2267–2274, Dec. 1989.
[79] O. Musseau, F. Gardic, P. Roche, T. Corbière, R. A. Reed, S. Buchner, P. McDonald, J. Melinger, L. Tran, and A. B. Campbell, "Analysis of multiple bit upsets (MBU) in a CMOS SRAM," *IEEE Trans. Nucl. Sci.*, vol. 43, pp. 2879–2888, Dec. 1996.
[80] R. Koga, S. D. Pinkerton, T. J. Lie, and K. B. Crawford, "Single-word multiple-bit upsets in static random access devices," *IEEE Trans. Nucl. Sci.*, vol. 40, pp. 1941–1946, Dec. 1993.
[81] J. B. Blake and R. Mandel, "On-orbit observations of single event upset in Harris HB-6508 1K RAMs," *IEEE Trans. Nucl. Sci.*, vol. 33, pp. 1616–1619, Dec. 1986.
[82] C. I. Underwood, J. W. Ward, C. S. Dyer, and A. J. Sims, "Observations of single-event upsets in nonhardened high-density SRAM's in Sun-synchronous orbit," *IEEE Trans. Nucl. Sci.*, vol. 39, pp. 1817–1827, Dec. 1992.
[83] R. Koga, S. H. Penzin, K. B. Crawford, and W. R. Crain, "Single event functional interrupt (SEFI) sensitivity in microcircuits," in *Proc. 4th RADECS*, 1997, pp. 311–318.
[84] R. Koga, S. H. Crain, P. Yu, and K. B. Crawford, "SEE sensitivity determination of high-density DRAM's with limited-range heavy ions," in *2001 IEEE Radiation Effects Data Workshop Rec.*, 2001, pp. 182–189.
[85] R. Koga, P. Yu, K. B. Crawford, S. H. Crain, and V. T. Tran, "Permanent single event functional interrupts (SEFI's) in 128- and 256-megabit synchronous dynamic random access memories (SDRAM's),".
[86] L. W. Massengill, M. S. Reza, B. L. Bhuva, and T. L. Turflinger, "Single-event upset cross-section modeling in combinational CMOS logic circuits," *J. Radiation Effects, Res. Eng.*, vol. 16, no. 1, 1998.

[87] "The design of radiation-hardened IC's for space: A compendium of approaches," in *Proc. IEEE*, vol. 76, S. E. Kerns and B. D. Shafer, Eds., Nov. 1988, pp. 1470–1509.

[88] S.-W. Fu, A. M. Mohsen, and T. C. May, "Alpha-particle-induced charge collection measurements and the effectiveness of a novel p-well protection barrier on VLSI memories," *IEEE Trans. Electron. Devices*, vol. 32, pp. 49–54, Feb. 1985.

[89] D. Burnett, C. Lage, and A. Bormann, "Soft-error-rate improvement in advanced BiCMOS SRAMs," in *Proc. IEEE Int. Reliability Phys. Symp.*, 1993, pp. 156–160.

[90] J. D. Hayden, R. C. Taft, P. Kenkare, C. Mazur, C. Gunderson, B. Y. Nguyen, M. Woo, C. Lage, B. J. Roman, S. Radhakrishna, R. Subrahmanyan, A. R. Sitaram, P. Pelley, J. H. Lin, K. Kemp, and H. Kirsch, "A quadruple well, quadruple polysilicon BiCMOS process for fast 16 Mb SRAMs," *IEEE Trans. Electron. Devices*, vol. 41, pp. 2318–2325, Dec. 1994.

[91] T. Kishimoto, M. Takai, Y. Ohno, T. Nishimura, and M. Inuishi, "Control of carrier collection efficiency in n+p diode with retrograde well and epitaxial layers," *Jpn. J. Appl. Phys.*, pt. 1, vol. 36, no. 6A, pp. 3460–3462, 1997.

[92] M. Takai, T. Kishimoto, Y. Ohno, H. Sayama, K. Sonoda, S. Satoh, T. Nishimura, H. Miyoshi, A. Kinomura, Y. Horino, and K. Fujii, "Soft error susceptibility and immune structures in dynamic random access memories (DRAM's) investigated by nuclear microprobes," *IEEE Trans. Nucl. Sci.*, vol. 43, pp. 696–704, Feb. 1996.

[93] P. E. Dodd, M. R. Shaneyfelt, K. M. Horn, D. S. Walsh, G. L. Hash, T. A. Hill, B. L. Draper, J. R. Schwank, F. W. Sexton, and P. S. Winokur, "SEU-sensitive volumes in bulk and SOI SRAM's from first-principles calculations and experiments," *IEEE Trans. Nucl. Sci.*, vol. 48, pp. 1893–1903, Dec. 2001.

[94] J. R. Schwank, P. E. Dodd, M. R. Shaneyfelt, G. Vizkelethy, B. L. Draper, T. A. Hill, D. S. Walsh, G. L. Hash, B. L. Doyle, and F. D. McDaniel, "Charge collection in SOI capacitors and circuits and its effect on SEU hardness," *IEEE Trans. Nucl. Sci.*, vol. 49, pp. 2937–2947, Dec. 2002.

[95] G. E. Davis, L. R. Hite, T. G. W. Blake, C. E. Chen, H. W. Lam, and R. DeMoyer, "Transient radiation effects in SOI memories," *IEEE Trans. Nucl. Sci.*, vol. 32, pp. 4432–4437, Dec. 1985.

[96] M. L. Alles, S. E. Kerns, L. W. Massengill, J. E. Clark, K. L. Jones, and R. E. Lowther, "Body tie placement in CMOS/SOI digital circuits for transient radiation environments," *IEEE Trans. Nucl. Sci.*, vol. 38, pp. 1259–1264, Dec. 1991.

[97] L. R. Hite, H. Lu, T. W. Houston, D. S. Hurta, and W. E. Bailey, "An SEU resistant 256k SOI SRAM," *IEEE Trans. Nucl. Sci.*, vol. 39, pp. 2121–2125, Dec. 1992.

[98] N. van Vonno and B. R. Doyle, "A 256k SRAM implemented in SOI technology," in *Proc. RADECS-93*, 1993, pp. 392–395.

[99] P. Francis, J.-P. Colinge, and G. Berger, "Temporal analysis of SEU in SOI/GAA SRAMs," *IEEE Trans. Nucl. Sci.*, vol. 42, pp. 2127–2137, Dec. 1995.

[100] F. W. Sexton, W. T. Corbett, R. K. Treece, K. J. Hass, K. L. Hughes, C. L. Axness, G. L. Hash, M. R. Shaneyfelt, and T. F. Wunsch, "SEU simulation and testing of resistor hardened D-latches in the SA3300 microprocessor," *IEEE Trans. Nucl. Sci.*, vol. 38, pp. 1521–1528, Dec. 1991.

[101] P. S. Winokur, F. W. Sexton, D. M. Fleetwood, M. D. Terry, M. R. Shaneyfelt, P. V. Dressendorfer, and J. R. Schwank, "Implementing QML for radiation hardness assurance," *IEEE Trans. Nucl. Sci.*, vol. 37, pp. 1794–1805, Dec. 1990.

[102] H. T. Weaver, C. L. Axness, J. D. McBrayer, J. S. Browning, J. S. Fu, A. Ochoa, and R. Koga, "An SEU tolerant memory cell derived from fundamental studies of SEU mechanisms in SRAM," *IEEE Trans. Nucl. Sci.*, vol. 34, pp. 1281–1286, Dec. 1987.

[103] R. L. Johnson, Jr. and S. E. Diehl, "An improved single event resistive-hardening technique for CMOS static RAMs," *IEEE Trans. Nucl. Sci.*, vol. 33, pp. 1730–1733, Dec. 1986.

[104] A. Ochoa, Jr., C. L. Axness, H. T. Weaver, and J. S. Fu, "A proposed new structure for SEU immunity in SRAM employing drain resistance," *IEEE Electron. Device Lett.*, vol. 8, pp. 537–539, Nov. 1987.

[105] S. Verghese, J. J. Wortman, and S. E. Kerns, "A novel CMOS SRAM feedback element for SEU environments," *IEEE Trans. Nucl. Sci.*, vol. 34, pp. 1641–1646, Dec. 1987.

[106] L. R. Rockett, Jr., "Simulated SEU hardened scaled CMOS SRAM cell design using gated resistors," *IEEE Trans. Nucl. Sci.*, vol. 39, pp. 1532–1541, Oct. 1992.

[107] F. Ootsuka, M. Nakamura, T. Miyake, S. Iwahashi, Y. Ohira, T. Tamaru, K. Kikushima, and K. Yamaguchi, "A novel 0.20 μm full CMOS SRAM cell using stacked cross couple with enhanced soft error immunity," in *IEDM Tech. Dig.*, 1998, pp. 205–208.

[108] D. R. Alexander, "Design issues for radiation tolerant microcircuits for space," in *1996 IEEE NSREC Short Course*, Indian Wells, CA.

[109] L. R. Rockett, Jr., "An SEU hardened CMOS data latch design," *IEEE Trans. Nucl. Sci.*, vol. 35, pp. 1682–1687, Dec. 1988.

[110] H. T. Weaver, W. T. Corbett, and J. M. Pimbley, "Soft error protection using asymmetric response latches," *IEEE Trans. Electron Dev.*, vol. 38, pp. 1555–1557, Dec. 1991.

[111] M. N. Liu and S. Whitaker, "Low power SEU immune CMOS memory circuits," *IEEE Trans. Nucl. Sci.*, vol. 39, pp. 1679–1684, Dec. 1992.

[112] D. Wiseman, J. Canaris, S. Whitaker, J. Venbrux, K. Cameron, K. Arave, L. Arave, M. N. Liu, and K. Liu, "Design and testing of SEU/SEL immune memory and logic circuits in a commercial CMOS process," in *IEEE NSREC Data Workshop Rec.*, 1993, pp. 51–55.

[113] R. Velazco, D. Bessot, S. Duzellier, R. Ecoffet, and R. Koga, "Two CMOS memory cells suitable for the design of SEU-tolerant VLSI circuits," *IEEE Trans. Nucl. Sci.*, vol. 41, pp. 2229–2234, Dec. 1994.

[114] T. Calin, M. Nicolaidis, and R. Velazco, "Upset hardened memory design for submicron CMOS technology," *IEEE Trans. Nucl. Sci.*, vol. 43, pp. 2874–2878, Dec. 1996.

[115] D. G. Mavis and P. H. Eaton, "Soft error rate mitigation techniques for modern microcircuits," in *Proc. Int. Reliability Phys. Symp.*, 2002, pp. 216–225.

[116] R. W. Berger, D. Bayles, R. Brown, S. Doyle, A. Kazemzadeh, K. Knowles, D. Boser, J. Rodgers, B. Saari, D. Stanley, and B. Grant, "The RAD750—A radiation hardened power PC processor for high performance spaceborne applications," in *IEEE Proc. Aerospace Conf.*, vol. 5, 2001, pp. 2263–2272.

[117] N. Seifert, X. Zhu, and L. W. Massengill, "Impact of scaling on soft-error rates in commercial microprocessors," *IEEE Trans. Nucl. Sci.*, vol. 49, pp. 3100–3106, Dec. 2002.

[118] D. C. Bossen and M. Y. Hsaio, "A system solution to the memory soft error problem," *IBM J. Res. Develop.*, vol. 24, pp. 390–397, Mar. 1980.

[119] C. L. Chen and M. Y. Hsiao, "Error-correcting codes for semiconductor memory applications: A state-of-the-art review," *IBM J. Res. Develop.*, vol. 28, no. 2, pp. 124–134, 1984.

[120] P. M. O'Neill and G. D. Badhwar, "Single event upsets for space shuttle flights of new general purpose computer memory devices," *IEEE Trans. Nucl. Sci.*, vol. 41, pp. 1755–1764, Oct. 1994.

[121] J. D. Kinnison, "Achieving reliable, affordable systems," in *1998 IEEE NSREC Short Course*, Newport Beach, CA.

[122] C. W. Gwyn, D. L. Scharfetter, and J. L. Wirth, "The analysis of radiation effects in semiconductor junction devices," *IEEE Trans. Nucl. Sci.*, vol. 14, pp. 153–169, Dec. 1967.

[123] V. A. J. van Lint, J. H. Alexander, D. K. Nichols, and P. R. Ward, "Computerized model for response of transistors to a pulse of ionizing radiation," *IEEE Trans. Nucl. Sci.*, vol. 14, pp. 170–178, Dec. 1967.

[124] M. S. Lundstrom, *Fundamentals of Carrier Transport*, ser. Modular Series on Solid State Devices. Reading, MA: Addison-Wesley, 1990, vol. X.

[125] S. Selberherr, *Analysis and Simulation of Semiconductor Devices*. Vienna, Austria: Springer-Verlag, 1984.

[126] J. G. Rollins, W. A. Kolasinski, D. C. Marvin, and R. Koga, "Numerical simulation of SEU induced latch-up," *IEEE Trans. Nucl. Sci.*, vol. 33, pp. 1565–1570, Dec. 1986.

[127] J. P. Kreskovsky and H. L. Grubin, "Simulation of charge collection in a multilayer device," *IEEE Trans. Nucl. Sci.*, vol. 32, pp. 4140–4144, Dec. 1985.

[128] J. S. Fu, C. L. Axness, and H. T. Weaver, "Two-dimensional simulation of single event induced bipolar current in CMOS structures," *IEEE Trans. Nucl. Sci.*, vol. 31, pp. 1155–1159, Dec. 1984.

[129] J. S. Fu, H. T. Weaver, R. Koga, and W. A. Kolasinski, "Comparison of 2D memory SEU transport simulation with experiments," *IEEE Trans. Nucl. Sci.*, vol. 32, pp. 4145–4149, Dec. 1985.

[130] J. S. Fu, K. H. Lee, R. Koga, W. A. Kolasinski, H. T. Weaver, and J. S. Browning, "Processing enhanced SEU tolerance in high density SRAMs," *IEEE Trans. Nucl. Sci.*, vol. 34, pp. 1322–1325, Dec. 1987.

[131] J. S. Fu, K. H. Lee, R. Koga, F. W. Hewlett, R. Flores, R. E. Anderson, J. C. Desko, W. J. Nagy, J. A. Shimer, R. A. Kohler, and S. D. Steenwyk, "Scaling studies of CMOS SRAM soft-error tolerances—From 16k to 256k," in *IEDM Tech. Dig.*, 1987, pp. 540–543.

[132] J. G. Rollins, J. Choma, Jr., and W. A. Kolasinski, "Single event upset in SOS integrated circuits," *IEEE Trans. Nucl. Sci.*, vol. 34, pp. 1713–1717, Dec. 1987.

[133] J. H. Chern, J. A. Seitchik, and P. Yang, "Single event charge collection modeling in CMOS multi-junctions structure," in *IEDM Tech. Dig.*, 1986, pp. 538–541.

[134] J. G. Rollins, T. K. Tsubota, W. A. Kolasinski, N. F. Haddad, L. Rockett, M. Cerrila, and W. B. Hennley, "Cost-effective numerical simulation of SEU," *IEEE Trans. Nucl. Sci.*, vol. 35, pp. 1608–1612, Dec. 1988.

[135] J. A. Zoutendyk, L. S. Smith, G. A. Soli, and R. Y. Lo, "Experimental evidence for a new single-event upset (SEU) model in a CMOS SRAM obtained from model verification," *IEEE Trans. Nucl. Sci.*, vol. 34, pp. 1292–1299, Dec. 1987.

[136] J. A. Zoutendyk, E. C. Secrest, and D. F. Berndt, "Investigation of single-event upset (SEU) in an advanced bipolar process," *IEEE Trans. Nucl. Sci.*, vol. 35, pp. 1573–1577, Dec. 1988.

[137] A. R. Knudson and A. B. Campbell, "Comparison of experimental charge collection waveforms with PISCES calculations," *IEEE Trans. Nucl. Sci.*, vol. 38, pp. 1540–1545, Dec. 1991.

[138] E. Worley, R. Williams, A. Waskiewicz, and J. Groninger, "Experimental and simulation study of the effects of cosmic particles on CMOS/SOS RAMs," *IEEE Trans. Nucl. Sci.*, vol. 37, pp. 1855–1860, Dec. 1990.

[139] P. E. Dodd, M. R. Shaneyfelt, and F. W. Sexton, "Charge collection and SEU from angled ion strikes," *IEEE Trans. Nucl. Sci.*, vol. 44, pp. 2256–2265, Dec. 1997.

[140] E. M. Buturla, P. E. Cottrell, B. M. Grossman, and K. A. Salsburg, "Finite-element analysis of semiconductor devices: The FIELDAY Program," *IBM J. Res. Develop.*, vol. 25, no. 4, pp. 218–231, 1981.

[141] E. Takeda, K. Takeuchi, E. Yamasaki, T. Toyabe, K. Ohshima, and K. Itoh, "The scaling law of alpha-particle induced soft errors for VLSI's," in *IEDM Tech. Dig.*, 1986, pp. 542–545.

[142] J. H. Chern, J. T. Maeda, L. A. Arledge, Jr., and P. Yang, "SIERRA: A 3-D device simulator for reliability modeling," *IEEE Trans. Computer-Aided Design*, vol. 8, pp. 516–527, May 1989.

[143] J. P. Kreskovsky and H. L. Grubin, "Numerical simulation of charge collection in two- and three-dimensional silicon diodes—A comparison," *Solid-State Electron.*, vol. 29, no. 5, pp. 505–518, 1986.

[144] *Davinci Three-Dimensional Device Simulation Program Manual*: Synopsys, Inc., 2003.

[145] *Taurus Process/Device User's Manual*: Synopsys, Inc., 2003.

[146] *Athena/Atlas User's Manual*: Silvaco Int., 1997.

[147] "DESSIS user's manual," ISE Integrated Systems Engineering AG, Release 4, vol. 5, 1997.

[148] G. C. Messenger, "Collection of charge on junction nodes from ion tracks," *IEEE Trans. Nucl. Sci.*, vol. 29, pp. 2024–2031, Dec. 1982.

[149] M. P. Baze and S. P. Buchner, "Attenuation of single event induced pulses in CMOS combinational logic," *IEEE Trans. Nucl. Sci.*, vol. 44, pp. 2217–2222, Dec. 1997.

[150] L. W. Massengill, "Challenges of modeling SEE's in complex sequential logic," in *First NASA/SEMATECH/SRC Symposium on Soft Errors, Radiation Effects, and Reliability*, Washington, DC, Oct. 1997.

[151] L. W. Massengill, A. E. Baranski, D. O. van Nort, J. Meng, and B. L. Bhuva, "Analysis of single event effects in combinational logic—Simulation of the AM2901 bitslice processor," *IEEE Trans. Nucl. Sci.*, vol. 47, pp. 2609–2615, Dec. 2000.

[152] Y. Song, K. N. Vu, J. S. Cable, A. A. Witteles, W. A. Kolasinski, R. Koga, J. H. Elder, J. V. Osborn, R. C. Martin, and N. M. Ghoniem, "Experimental and analytical investigation of single event, multiple bit upsets in poly-silicon load, 64K $\times$ 1 NMOS SRAMs," *IEEE Trans. Nucl. Sci.*, vol. 35, pp. 1673–1677, Dec. 1988.

[153] D. D. Tang and C. Chuang, "A circuit concept for reducing soft error in high-speed memory cells," *IEEE J. Solid-State Circuits*, vol. 23, pp. 201–203, Jan. 1988.

[154] K. Gulati, L. W. Massengill, and G. R. Agrawal, "Single event mirroring and DRAM sense amplifier designs for improved single-event-upset performance," *IEEE Trans. Nucl. Sci.*, vol. 41, pp. 2026–2034, Dec. 1994.

[155] J. G. Rollins and J. Choma, Jr., "Mixed-mode PISCES-SPICE coupled circuit and device solver," *IEEE. Trans. Computer-Aided Design*, vol. 7, pp. 862–867, Aug. 1988.

[156] K. Mayaram, J. H. Chern, and P. Yang, "Algorithms for transient three-dimensional mixed-level circuit and device simulation," *IEEE Trans. Computer-Aided Design*, vol. 12, pp. 1726–1733, Nov. 1993.

[157] K. Mayaram, P. Yang, and J. H. Chern, "Transient three-dimensional mixed-level circuit and device simulation: Algorithm and applications," in *Proc. ICCAD-91*, 1991, pp. 112–115.

[158] Ph. Roche, J. M. Palau, K. Belhaddad, G. Bruguier, R. Ecoffet, and J. Gasiot, "SEU response of an entire SRAM cell simulated as one contiguous three dimensional device domain," *IEEE Trans. Nucl. Sci.*, vol. 45, pp. 2534–2543, Dec. 1998.

[159] K. Castellani-Coulie, J.-M. Palau, G. Hubert, M.-C. Calvet, P. E. Dodd, and F. W. Sexton, "Various SEU conditions in SRAM studied by 3-D device simulation," *IEEE Trans. Nucl. Sci.*, vol. 48, pp. 1931–1936, Dec. 2001.

[160] V. Ferlet-Cavrois, O. Musseau, J. L. Leray, Y. M. Coïc, G. Lecarval, and E. Guichard, "Comparison of the sensitivity to heavy ions of SRAM's in different SIMOX technologies," *IEEE Electron. Device Lett.*, vol. 15, pp. 82–84, Mar. 1994.

[161] C. Detcheverry, C. Dachs, E. Lorfévre, C. Sudre, G. Bruguier, J.-M. Palau, J. Gasiot, and R. Ecoffet, "SEU critical charge and sensitive area in a submicron CMOS technology," *IEEE Trans. Nucl. Sci.*, vol. 44, pp. 2266–2273, Dec. 1997.

[162] K. Warren, L. Massengill, R. Schrimpf, and H. Barnaby, "Analysis of the influence of MOS device geometry on predicted SEU cross sections," *IEEE Trans. Nucl. Sci.*, vol. 46, pp. 1363–1369, Dec. 1999.

[163] S. Satoh, R. Sudo, H. Tashiro, N. Higaki, and N. Nakayama, "CMOS-SRAM soft-error simulation system," in *Proc. IEEE Int. Reliability Phys. Symp.*, 1994, pp. 339–343.

[164] G. R. Srinivasan, H. K. Tang, and P. C. Murley, "Parameter-free, predictive modeling of single event upsets due to protons, neutrons, and pions in terrestrial cosmic rays," *IEEE Trans. Nucl. Sci.*, vol. 41, pp. 2063–2070, Dec. 1994.

[165] P. C. Murley and G. R. Srinivasan, "Soft-error Monte Carlo modeling program, SEMM," *IBM J. Res. Develop.*, vol. 40, no. 1, pp. 109–118, 1996.

[166] Z. Hasnain and A. Ditali, "Building-in reliability: Soft errors—A case study," in *Proc. IEEE Int. Reliability Phys. Symp.*, 1992, pp. 276–280.

[167] Y. Tosaka, S. Satoh, T. Itakura, H. Ehara, T. Ueda, G. Woffinden, and S. A. Wender, "Measurement and analysis of neutron-induced soft errors in sub-half-micron CMOS circuits," *IEEE Trans. Electron. Devices*, vol. 45, pp. 1453–1458, July 1998.

[168] R. C. Baumann and E. B. Smith, "Neutron-induced boron fission as a major source of soft errors in high density SRAMs," *Microelectronics Reliability*, vol. 41, pp. 211–218, 2001.

[169] H. Kobayashi, K. Shiraishi, H. Tsuchiya, M. Motoyoshi, H. Usuki, Y. Nagai, K. Takahisa, T. Yoshiie, Y. Sakurai, and T. Ishizaki, "Soft errors in SRAM devices induced by high energy neutrons, thermal neutrons, and alpha particles," in *IEDM Tech. Dig.*, 2002, pp. 337–340.

[170] T. J. O'Gorman, "The effect of cosmic rays on the soft error rate of a DRAM at ground level," *IEEE Trans. Electron. Devices*, vol. 41, pp. 553–557, Apr. 1994.

[171] C. Lage, D. Burnett, T. McNelly, K. Baker, A. Bormann, D. Dreier, and V. Soorholtz, "Soft error rate and stored charge requirements in advanced high-density SRAMs," in *IEDM Tech. Dig.*, 1993, pp. 821–824.

[172] E. Normand, "Single event upset at ground level," *IEEE Trans. Nucl. Sci.*, vol. 43, pp. 2742–2750, Dec. 1996.

[173] ——, "Single-event effects in avionics," *IEEE Trans. Nucl. Sci.*, vol. 43, pp. 461–474, Apr. 1996.

[174] P. D. Bradley and E. Normand, "Single event upsets in implantable cardioverter defibrillators," *IEEE Trans. Nucl. Sci.*, vol. 45, pp. 2929–2940, Dec. 1998.

[175] P. E. Dodd, M. R. Shaneyfelt, J. R. Schwank, and G. L. Hash, "Neutron-induced latchup in SRAM's at ground level," in *Proc. Int. Reliability Phys. Symp.*, 2003, pp. 51–55.

[176] E. Normand, J. L. Wert, D. L. Oberg, P. P. Majewski, P. Voss, and S. A. Wender, "Neutron-induced single event burnout in high voltage electronics," *IEEE Trans. Nucl. Sci.*, vol. 44, pp. 2358–2366, Dec. 1997.

[177] A. H. Johnston, "Radiation effects in advanced microelectronics technologies," *IEEE Trans. Nucl. Sci.*, vol. 45, pp. 1339–1354, June 1998.

[178] private communication numerous U.S. semiconductor and computer manufacturers.

[179] A. H. Taber and E. Normand, "Investigation and characterization of SEU effects and hardening strategies in avionics,", DNA Tech. Rep. DNA-TR-94-123, 1995.