CMOS VOLTAGE REFERENCES

CMOS VOLTAGE REFERENCES

AN ANALYTICAL AND PRACTICAL PERSPECTIVE

Chi-Wah Kok and Wing-Shan Tam

Canaan Microelectronics Corporation Ltd, Hong Kong

This edition first published 2013

Registered office
John Wiley & Sons Singapore Pte. Ltd., 1 Fusionopolis Walk, #07-01 Solaris South Tower, Singapore 138628

Library of Congress Cataloging-in-Publication Data

CMOS voltage references : an analytical and practical perspective / Chi-Wah Kok, Wing-Shan Tam. – First edition.
pages cm
Includes bibliographical references and index.
ISBN 978-1-118-27568-9 (hardback)
1. Voltage references. 2. Electric circuit analysis. 3. Electric circuits–Design and construction. I. Kok, Chi-Wah. II. Tam, Wing-Shan. III. Title: Voltage reference.
TK454.C628 2013
621.3815′28–dc23

2012030274

ISBN: 9781118275689

Set in 10/12 pt Times by Aptara Inc., New Delhi, India

CONTENTS

About the Authors **ix**

Preface **xi**

Acknowledgements **xiii**

Nomenclature **xv**

1 Warm Up **1**
1.1 Bipolar Junction Transistors 2
1.1.1 Differential V_{BE} 5
1.2 Metal-Oxide Semiconductor Field-Effect Transistor 7
1.2.1 Cutoff Region 11
1.2.2 Subthreshold Conduction 11
1.2.3 Triode Region 14
1.2.4 Saturation Region 16
1.2.5 Thermal Properties 19
1.2.6 Channel Length Modulation Effect 23
1.3 Diode 23
1.4 Resistor 25
1.4.1 Dummy Element 27
1.4.2 Guard Ring 27
1.4.3 Sheet Resistance 27
1.5 Device Matching 28
1.5.1 Application of Statistics to Circuit Design 28
1.5.2 Systematic Variation 30
1.6 Simulation Models for Circuit Design 31
1.6.1 Process Variation and Typical Design 32
1.6.2 Process Corners 34
1.7 Noise 36
1.7.1 Types of Noises 36
1.7.2 Sums and Multiplications of Noises 38
1.8 Fabrication Technology 39
1.9 Book Organization 40
1.10 Exercises 42
References 46

2 Voltage Reference **49**
2.1 Performance Measures 49
2.1.1 Line Regulation 51
2.1.2 Temperature Coefficient 54
2.1.3 Power Supply Rejection Ratio 56
2.1.4 Quiescent Current 59
2.1.5 Output Noise 60
2.2 Other Design Considerations 62
2.3 Summary 63
2.4 Exercises 65
References 70

3 Bandgap Voltage Reference **71**
3.1 Widlar Bandgap Voltage Reference Circuit 71
3.2 Drain Voltage Equalization Current Mirror 74
3.2.1 Opamp Based β-Multiplier Bandgap Voltage Reference Circuit 76
3.2.2 Bandgap Voltage Reference Circuit 77
3.3 Major Circuit Elements 81
3.3.1 Operational Amplifier 81
3.3.2 Current Mirror 86
3.3.3 Startup Circuit 88
3.3.4 Resistor Network 93
3.3.5 Bipolar Transistor 94
3.4 Complete Layout 95
3.5 Summary 95
3.6 Exercises 96
References 101

4 Error Sources in Bandgap Voltage Reference Circuit **103**
4.1 Non-Ideal Opamp 103
4.1.1 Input Offset Voltage 104
4.1.2 Limited Gain and Power Supply Rejection Ratio 112
4.1.3 Noise 113
4.2 Current Mirror Mismatch 114
4.2.1 Channel Length Modulation Effect Compensation 116
4.2.2 Cascode Current Mirror 117
4.3 Bipolar Transistor 122
4.3.1 Size Variation 122
4.3.2 Series Base Resistance 122
4.3.3 β Variation 125
4.4 Resistor Variation 126
4.5 Power Supply Variation 127
4.5.1 Pre-Regulation 132
4.6 Output Loading 135
4.7 Output Noise 138
4.8 Voltage Reference Circuit Trimming 140

4.8.1 Linked Fuse Resistor Trimming 141
4.8.2 Resistor Trimming Circuit Analysis 142
4.8.3 Modulated Trimming 146
4.8.4 Voltage Domain Trimming 148
4.8.5 Current Domain Trimming 149
4.9 Summary 149
4.10 Exercises 151
References 161

ADVANCED VOLTAGE REFERENCE CIRCUITS

5 Temperature Compensation Techniques 165
5.1 $V_{BE} - \Delta V_{BE}$ Compensation 166
5.1.1 Brokaw Bandgap Voltage Reference 168
5.1.2 β-Multiplier $V_{BE} - \Delta V_{BE}$ Compensation 170
5.2 Widlar PTAT Current Source and V_{BE} Compensation 175
5.3 V_{GS} Based Temperature Compensation 177
5.3.1 V_{GS} Current Source 178
5.4 Summary 182
5.5 Exercises 183
References 189

6 Sub-1V Voltage Reference Circuit 191
6.1 Sub-1V Output Stage 193
6.2 Voltage Headroom in Opamp based β-multiplier Voltage Reference Circuit 195
6.2.1 Opamp with NMOS Input Stage 197
6.2.2 Local Voltage Boosting 198
6.2.3 Low V_{th} Transistor 198
6.2.4 Bulk-Driven Transistors 199
6.3 Sub-1V Bandgap Voltage Reference by Resistive Division 199
6.3.1 Resistive Divided V_{BE} 202
6.3.2 Independent Biased Resistive Divided V_{BE} 206
6.4 Peaking Current Source and V_{BE} Compensation 209
6.5 Weighted ΔV_{GS} Compensation 211
6.6 Summary 214
6.7 Exercises 215
References 222

7 High Order Curvature Correction 223
7.1 Compensation Order 224
7.2 Second Order Temperature Compensation 228
7.2.1 Second Order Current Source 229
7.2.2 Current Subtraction 232
7.2.3 Current Addition 236
7.3 BJT Current Subtraction 238
7.4 Piecewise Linear Compensation 240

7.5 Sum and Difference of Sources with Similar Temperature Dependence 243
7.5.1 Difference of Voltages with Similar Temperature Dependence 244
7.5.2 Sum of Voltages with Inverted Temperature Dependence 245
7.5.3 Multi-threshold Voltages Curvature Compensated Voltage Reference 247
7.6 Summary 252
7.7 Exercises 253
References 257

8 CMOS Voltage Reference without Resistors 259
8.1 Generation of Weighted PTAT Source By Inverse Functions 260
8.1.1 Weighted Differential Circuit 260
8.1.2 Negative Impedance Converter 262
8.2 Resistorless Voltage and Current Sources 265
8.2.1 Resistorless Voltage Source 265
8.2.2 Resistorless Current Source 266
8.3 First Order Compensated Resistorless Bandgap Voltage Reference Circuit 268
8.3.1 Voltage Summation Based Resistorless Reference Circuit 269
8.3.2 Current Summation Based Resistorless Reference Circuit 270
8.4 Resistorless Sub-Bandgap Reference Circuit 270
8.4.1 The Voltage Summation Approach 271
8.4.2 CTAT Voltage Reduction 273
8.5 Summary 279
8.6 Exercises 280
References 281

A SPICE Model File 283

B SPICE Netlist of Voltage Reference Circuit 287

Index 289

ABOUT THE AUTHORS

Chi-Wah Kok was born in Hong Kong. He was granted a PhD degree from the University of Wisconsin Madison. Since 1992, he has been working with various semiconductor companies, research institutions, and universities, which include AT&T Labs Research, Holmdel, SONY U.S. Research Labs, Stanford University, Hong Kong University of Science and Technology, Hong Kong Polytechnic University, City University of Hong Kong, Lattice Semiconductor, etc. In 2006, he founded Canaan Microelectronics Corp Ltd., a fabless IC company with products in mixed signal IC for consumer electronics. Dr. Kok embraces new technologies to meet the fast changing market requirements. He has extensively applied signal processing techniques to improve the circuit topologies, designs, and fabrication technologies within Canaan. This includes the application of semidefinite programming to circuit design optimization, abstract algebra in switched capacitor circuit topologies improvement, and nonlinear optimization methods to optimize high voltage MOSFET layout and fabrication.

Wing-Shan Tam was born in Hong Kong. She received her BEng degree in electronic engineering from The Chinese University of Hong Kong, MSc degree in electronic and information engineering from The Hong Kong Polytechnic University, and PhD degree in electronic engineering from the City University of Hong Kong in 2004, 2007, and 2011, respectively. Currently, she is the Engineering Manager of Canaan Microelectronics Corp Ltd. Her research interests include mixed-signal integrated circuit design for data conversion and power-management.

PREFACE

This book has a genesis: It started as internal training material for engineers working in Canaan Microelectronics Corp. Ltd. It is also a monograph because it presents the outcome of our research and teaching activities in the field of temperature independent circuit design at both the Canaan Microelectronics Corp. Ltd. and the City University of Hong Kong. Many unpublished works are included in this book. Numerous design examples are also presented together with detailed discussions on design principles, performance analysis, and the potential problems of each circuit topology. This book is intended to be course material for senior and graduate level courses, training material for engineers, and also a reference text for readers who are working in the field of temperature independent circuit design.

The book is divided into eight chapters. The first chapter offers an introduction of device physics focusing on the temperature properties of individual devices, which introduces just enough material for voltage reference circuit design and analysis. Details of general device physics may be gathered from existing literature, such as the textbooks by Chenming C. Hu, (*Modern Semiconductor Devices for Integrated Circuits*, Prentice Hall, 2010), and S.M. Sze, (*Physics of Semiconductor Devices*, Wiley, 1969) that offer detailed discussions on the device physics for bipolar transistors, MOS transistors, and other passive components manufactured in the CMOS process. Besides the physics, towards the end of Chapter 1, we also discuss practical issues in CMOS circuit design. The device matching problem is introduced. Computer simulation for circuit design with process variations is discussed. Finally, the device noise models that describe the noises associated with CMOS devices are presented. Chapter 2 presents the performance characterization of voltage reference circuits. The presented characterization will be used throughout the book in the analytical discussions and performance comparisons of individual voltage reference circuits. A general voltage reference circuit framework of opamp based β-multiplier bandgap voltage reference is presented in Chapter 3. The presented voltage reference circuit is silicon proven, and has been applied to a power management IC of Canaan Microelectronics Corp. Ltd.: the micrograph of the die is shown on the front page of this book. Every building block within the voltage reference circuit is discussed analytically together with layout details. Various error sources of the circuit are identified, and analyzed in Chapter 4. Methods to remedy each problem together with their pros and cons are discussed in detail in Chapter 4. The basic PTAT-CTAT temperature compensation technique discussed in Chapter 4 will be extended to voltage reference circuits using various temperature dependent devices and topologies in Chapter 5. Analytical derivation to determine the component values of each device within the voltage reference circuit, together with the important design considerations of each circuit and topology will be discussed. Chapter 6 discusses the design of voltage

reference circuits with sub-1V supply, and voltage reference circuits with sub-1V reference voltage. Notice that the design of the voltage reference circuit with a sub-1V reference voltage is different from that of the voltage reference circuit with a sub-1V supply voltage. A voltage reference circuit with a sub-1V supply voltage is also a voltage reference circuit with a sub-1V reference voltage. The voltage reference circuit with sub-1V reference voltage being able to operate with a sub-1V supply voltage is important in modern CMOS circuit design where the supply voltage keeps reducing for power reduction and silicon size shrinkage. A number of sub-1V voltage reference circuits will be discussed in this chapter.

High order curvature compensated voltage reference circuits are presented in Chapter 7, which are important to applications that require a reference voltage with low temperature sensitivity. A number of high accuracy voltage reference circuit topologies, including high order curvature compensation, inverted temperature compensation, and piecewise temperature compensation etc. are discussed. This book concludes in Chapter 8 with a discussion on a type of special voltage reference circuit that does not require resistors. Such a voltage reference circuit has the advantage of compact layout. The performance of a resistor free voltage reference circuit can be further optimized with applications of piecewise temperature compensation technique to lower the temperature sensitivity of the circuit. Post-fabrication trimming circuits are discussed to reduce the reference voltage variation.

A detailed summary of the state of the art development with respect to the topic of each chapter is presented in the "*Summary*" section of each chapter. Homework problems are presented in the "*Exercise*" section in individual chapter. The homework includes both analytic problems, and SPICE based computer simulation exercises. While the process parameters used in this book and also in developing the exercises may not be the same as those in your institution, it is our hope that the exercises will provide you with general guidelines, analysis, design and layout experience for the design of the voltage reference circuits with the help of SPICE. The experience will further address the performance evaluation of the voltage reference circuit which will help you to achieve a thorough consideration of the voltage reference circuit before the actual design.

The development of voltage reference circuits is still continuing and therefore a book, such as this one, cannot be definitive or complete. It is hoped, however, that this book will fill an important gap; students embarking upon mixed-signal circuit design should be able to learn sufficient basics before tackling journal papers, researchers and engineers in the field of temperature independent/dependent circuit design should be able to use it as reference to assist their circuit design tasks, and current researchers in the field should be able to get a broad perspective on what has been achieved. The subject area is introduced, some major developments are recorded, and enough successes as well as challenges are noted here for readers to look into other voltage independent/dependent circuit design problems and generate solutions for their own problems.

Chi-Wah Kok and Wing-Shan Tam
February 2012

ACKNOWLEDGEMENTS

We are in debt to many people, too numerous to mention. To all the scholars who have influenced us, both in person or through their works, we acknowledge our indebtedness and express our great appreciation. Perhaps the most noteworthy was Prof. Hei Wong of the City University of Hong Kong whose knowledge, enthusiasm in advanced microelectronics research and development, and generous support in the course of the development of this book has surely inspired and greatly assisted us. We are proud to say that Prof. Wong is one of our greatest role models.

Dr. Kok would like to take this chance to claim victory in the competition with his wife Dr. Annie Ko on who will be the first to complete his/her second textbook. It was this competition that provided Dr. Kok with the extra boost to get this book finished with his best effort. Dr. Kok is also very happy to collaborate with Dr. Tam on this book project, who has always been his best collaborator in both the academic and business spheres. Dr. Tam is truly indebted and grateful to her parents, Simon Tam and Gloria Lee, for their love, encouragement, and their constant support in all her pursuits, including her PhD study and the completion of this book. Dr. Tam would also like to thank her beloved family, especially her sister and grandmother, who are always willing to share her stress and happiness. Finally, Dr. Tam would like to express her sincere gratitude to Dr. Kok, who introduced her into the world of IC design. Dr. Tam is very grateful for the opportunity to coauthor this book and treasures other aspects of her partnership with Dr. Kok too. Coauthoring a book is never easy. In the course of the development of this book, the authors have learned a lot from each other, and adapted to each others' working and learning styles. We are looking forward to seeing our excellent partnership extend to future book and other research and development projects.

Despite the assistance, review, overseeing, and editing of so many people, we have no doubt that errors still lurk undetected. These are ours alone, and it is our hope that the reader of this book will discover them and bring them to our attention, so that they all may be eradicated.

Chi-Wah Kok and Wing-Shan Tam

NOMENCLATURE

SoC	System-On-Chip
ATE	Automatic test equipment
J	Joule
Col	Coulomb
K	Kelvin
$^{\circ}$**C**	degree Celsius
V_T	Thermal voltage, kT/q
V_{DD}	Positive supply voltage
V_{SS}	Negative supply voltage
BJT	Bipolar Junction Transistor
I_B	Base Current of Bipolar Transistor
I_C	Collector Current of Bipolar Transistor
I_E	Emitter Current of Bipolar Transistor
I_S	Saturation Current of Bipolar Transistor
J_C	Collector Current Density of Bipolar Transistor
J_S	Saturation Current Density of Bipolar Transistor
V_{BE}	Base-Emitter Voltage of a BJT
V_{CE}	Collector-Emitter Voltage of a BJT
R_B	Zero-bias base ohmic resistance
R_E	Emitter resistance
R_C	Collector resistance
V_{G0}	Silicon Bandgap Voltage Extrapolated at 0 K
A_E	Emitter Area of Bipolar Transistor
W_B	BJT base width
β	Forward current gain
V_D	Forward-bias diode voltage
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
NMOS	N-Channel MOSFET
PMOS	P-Channel MOSFET
CMOS	Complementary Metal Oxide Semiconductor
W	MOSFET Gate Width
L	MOSFET Gate Length
S	Channel Width to Length Ratio (W/L) of a MOSFET
I_{DS}	Drain to Source Current of a MOSFET

$I_{D,sub}$	Drain to Source Current of a MOSFET biased in subthreshold mode
$I_{D,lin}$	Drain to Source Current of a MOSFET biased in triode mode
$I_{D,sat}$	Drain to Source Current of a MOSFET biased in saturation mode
$I_{D,leak}$	Drain to Source Leakage Current or Off Current of a MOSFET in cutoff mode
$\hat{I}_{leak}$	Unit Drain to Source Current Normalized by S
ζ	Subthreshold Slope
ζ_n	Subthreshold Slope of a n-channel MOSFET
ζ_p	Subthreshold Slope p-channel MOSFET
C_D	Depletion capacitance of a MOSFET
C_{ox}	Gate oxide capacitance per unit area of a MOSFET
t_{ox}	Thickness of gate oxide
V_{th}	Threshold voltage of a MOSFET
V_{GS}	Gate source voltage of a MOSFET
V_{DS}	Drain source voltage of a MOSFET
$R_{DS,sub}$	Drain source resistance of a MOSFET in subthreshold mode
$V_{DS,sub}$	Drain source voltage of a MOSFET in subthreshold mode
$V_{DS,lin}$	Drain source voltage of a MOSFET in linear mode
$V_{DS,sat}$	Drain source voltage of a MOSFET in saturation mode
R_{DS}	Drain source resistance of a MOSFET
$R_{DS,lin}$	Drain source resistance of a MOSFET in linear mode
g_m	Transconductance of a MOSFET
$R_{DS,sat}$	Drain source resistance of a MOSFET in saturation mode
μ	Mobility of the charge carrier
CTAT	Complementary to Absolute Temperature
PTAT	Proportional to Absolute Temperature
V_{CTAT}	CTAT Voltage
I_{CTAT}	CTAT Current
V_{PTAT}	PTAT Voltage
I_{PTAT}	PTAT Current
V_{IN}	Input voltage to the voltage reference circuit
$V_{IN(nom)}$	Nominal input voltage to the voltage reference circuit
$V_{IN(min)}$	Minimum input voltage for proper operation of the voltage reference circuit
$V_{IN(max)}$	Maximum input voltage for proper operation of the voltage reference circuit
V_{REF}	Output voltage of the voltage reference circuit
$V_{DD(min)}$	Minimum operating supply voltage
$V_{DD(nom)}$	Nominal supply voltage
$V_{REF(nom),T}$	Output voltage of the voltage reference circuit at specific temperature T with respect to a range of input voltages
$V_{REF(min),T}$	Output voltage of the voltage reference circuit at $V_{IN(min)}$ and temperature T
$V_{REF(max),T}$	Output voltage of the voltage reference circuit at $V_{IN(max)}$ and temperature T
V_{η}	Noise source

$V_{REF_{CONV}}$	Reference voltage generated by conventional $V_{BE} - V_T$ temperature compensation voltage reference circuit
V_{DROP}	Dropout voltage defined as the voltage difference between the input and output voltage
T_{nom}	Nominal temperature
$V_\eta(f)$	Noise voltage at frequency f
T_{min}	Minimum temperature for proper operation of the voltage reference circuit
T_{max}	Maximum temperature for proper operation of the voltage reference circuit
$V_{REF(nom),V_{IN(nom)}}$	Output voltage of the voltage reference circuit at nominal input voltage with respect to a temperature range $[T_{min}, T_{max}]$
$V_{REF(max),V_{IN(nom)}}$	The maximum output voltage of the voltage reference circuit at nominal input voltage in the temperature range $[T_{min}, T_{max}]$
$V_{REF(min),V_{IN(nom)}}$	The maximum output voltage of the voltage reference circuit at nominal input voltage in the temperature range $[T_{min}, T_{max}]$
I_q	The quiescent current of the voltage reference circuit
TC	Temperature Coefficient
$PSRR$	Power supply rejection ratio
BW	System bandwidth of the voltage reference circuit
V_{OS}	Offset voltage
$\mathcal{S}_{PSRR}$	Power-supply rejection ratio that the variation of the reference voltage with a particular frequency in the input voltage
$\mathcal{S}_x^y$	Sensitivity of parameter y with respect to a change in parameter x
$\mathcal{S}_{LR}$	Linear regulation measure of variation of reference voltage with respect to a charge in input voltage to the voltage reference circuit
$\mathcal{S}_{TC}$	Temperature coefficient measure of variation of reference voltage with respect to a change in operation temperature of the voltage reference circuit

Table 1 Physical Constant

Parameter	Description	Typical Values
k	Boltzmann's Constant	1.38×10^2 J/K
q	Electron's Charge	1.62×10^{-19} Col
V_T	Thermal Voltage	$kT/q = 26$ mV at 300 K
B_{G0}	Silicon Bandgap Voltage Extrapolated at 0 K	1.206 V
V_{BE}	Base Emitter Voltage of NPN	0.73 mV at 300 K
V_{BE}	Base Emitter Voltage of PNP	0.76 mV at 300 K

1

Warm Up

The voltage reference circuits discussed in this book require you to work on electron devices by connecting together transistors, resistors, and capacitors. Therefore you need to understand the properties and limitations of each device in some detail. The easiest way to learn about electron devices is to study their physical models, although they are usually very complex. For example, the Gummel and Poon model of a bipolar transistor lists 45 parameters (Gummel and Poon, 1970) and yet still is not accurate enough to simulate the saturation or junction breakdown behaviors. The BSIM 3.3 model of a MOS transistor has more than 50 coefficients (Liu, 2001) not counting noise and gate leakage parameters. Although all of these variables are useful for the design of voltage reference circuits, only very few numbers and equations have to be remembered for creative work, and the shapes of a few dependencies and some qualitative relationships (not how much, but more or less, increasing or decreasing) of these parameters are much more important.

The following sections will present, from the authors' point of view, the most important electron device parameters necessary for voltage reference circuit design. Detailed descriptions of the operations of individual electron device can be found in textbooks on analog circuit design or device modeling (Hu, 2010; Sze, 1969). In particular, a large part of this book presents the design and analysis of a special kind of voltage reference circuit, the bandgap voltage reference. It is useful to know which parameters of the practical model dominate the behavior of each electron devices in the case of bandgap reference circuit design.

The well-known Gummel and Poon model for bipolar transistors, and BSIM 3.3 model for MOSFETs used in SPICE, will form the basis for the design and analysis of bandgap references. In particular HSPICE (*HSPICE® Simulation and Analysis User Guide* 2006), a typical SPICE simulator, will be used to produce all the simulation results presented in this book based on a 0.18 μm mixed signal CMOS process SPICE model. However, instead of going through SPICE, a minimum set of key parameters will be presented in the following sections which allow us to analytically describe the relation between various electron devices behaviors and their application to temperature insensitive circuit design. We shall start our discussions with the active components first, which include the bipolar transistors, MOSFETs, and diode, and then the passive components, which are the resistors made by different CMOS processes.

CMOS Voltage References: An Analytical and Practical Perspective, First Edition. Chi-Wah Kok and Wing-Shan Tam.
 Published 2013 by John Wiley & Sons Singapore Pte. Ltd.

1.1 Bipolar Junction Transistors

The bipolar junction transistor (BJT), is a vital component in the voltage reference circuit and is commonly used for the generation of temperature dependent voltage, whereas the generation of controllable temperature dependent voltage is the first step towards obtaining a temperature insensitive reference voltage. The BJTs can be implemented in a standard CMOS process. The simplified cross-view of a vertical NPN transistor and a vertical PNP transistor implemented in CMOS process are shown in Figure 1.1(a) and (b), respectively; while Figure 1.1(c) and (d) are the layouts of the transistors in Figure 1.1(a) and (b), respectively. In general, the NPN transistor is preferred because of its higher collector-current efficiency and the highly doped base region which can achieve a low series base resistance. The awkward effect of the base resistance will be discussed in Section 4.3.2. Besides, there are other limitations on the application of PNP transistor in voltage reference circuit. Consider the vertical PNP transistor illustrated in Figure 1.1(b), where the emitter is formed by a P-type region, the base is formed by a N-well, and the collector is formed by a P-type substrate. There are two limitations imposed on such BJT implementation. First, the collector is formed by the substrate, which is permanently tied to the lowest supply voltage. Second, the current gain of the transistor, β, is very low when compared to its NPN counterpart, which is defined as

$$\beta = \frac{I_C}{I_B}, \tag{1.1}$$

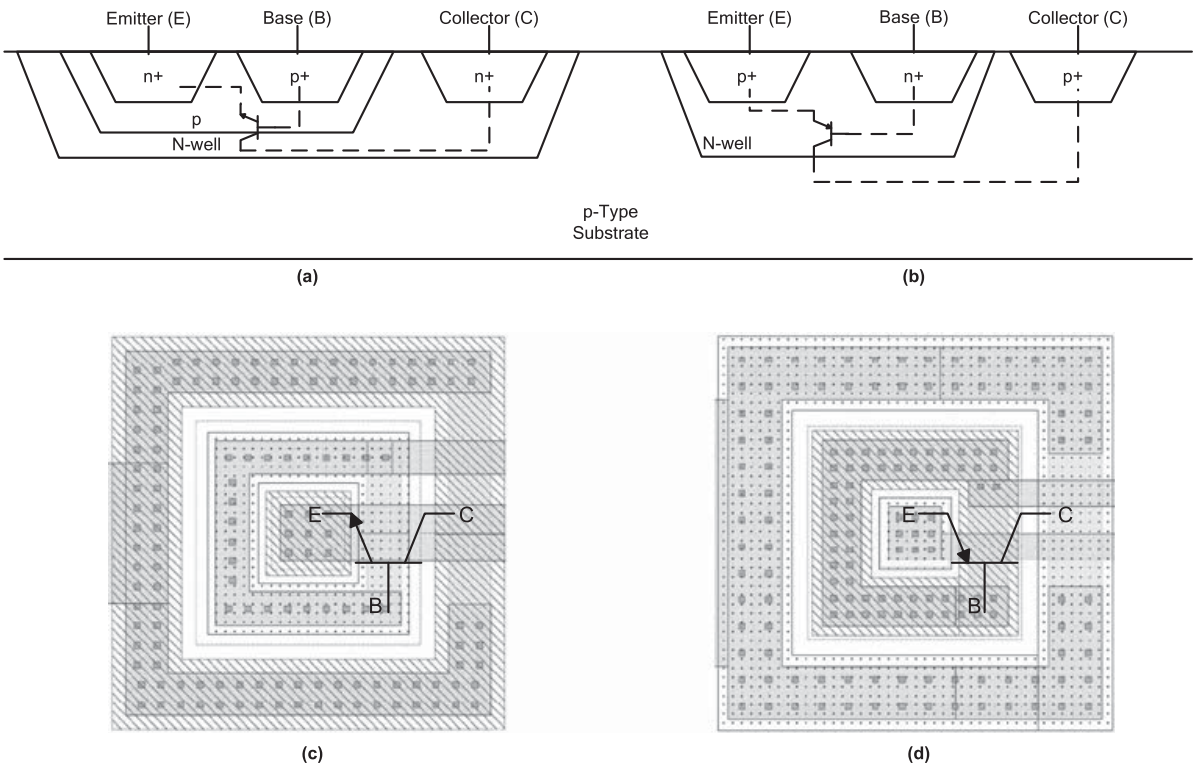


Figure 1.1 Integrated bipolar transistor in N-well CMOS processes: (a) a vertical NPN transistor and (b) a vertical PNP transistor. Layout examples of (c) NPN transistor in (a) and (d) PNP transistor in (b).

with I_C and I_B being the currents flowing into the collector and base of the BJT, respectively. To effectively alleviate the base resistance as a source of error in voltage reference circuit design, a high current gain ($\beta \geq 100$) is desired. As a result, the vertical PNP transistor is only applicable to voltage reference circuit design if we make it large to achieve a small base resistance. The last but not least, problem associated with the vertical PNP BJT is that it cannot be used in cascode structure because the collector is required to connect to the ground, and thus cannot be connected to the emitter of another BJT. Despite the above limitations, both the NPN and the PNP BJTs can be used in the voltage reference circuit.

The BJT applied in a voltage reference circuit is usually configured in a diode-connected structure (i.e., the base terminal and the collector terminal are connected together), such that the base-emitter voltage, V_{BE}, is used to provide a fixed junction voltage. However, the junction voltage is temperature sensitive, and thus cannot be used as reference voltage by itself. The thermal analysis of the BJT, and in particular the V_{BE}, has been widely discussed in the literature (Massobrio and Antognetti, 1993; Tsividis, 1980). The theory and notation of the NPN transistor are applicable to the PNP transistor with a few obvious modifications. Therefore, all the symbols and notations of these two types of BJTs are used interchangeably in our discussions.

If we neglect the Early effect, the collector current of a NPN transistor biased in the forward active region is given by

$$\begin{aligned} J_C(T)A_E &= J_S(T)A_E \exp\left(\frac{V_{BE}}{V_T}\right), \\ I_C(T) &= I_S(T) \exp\left(\frac{V_{BE}}{V_T}\right), \end{aligned} \tag{1.2}$$

where A_E is the base-emitter junction area, T is the absolute temperature in K, $I_C(T)$ is the temperature dependent collector current, $J_S(T)$ is the saturation current density, which relates to the temperature dependent saturation current $I_S(T)$ as $I_S(T) = J_S(T)A_E$. Finally, the thermal voltage V_T is given by

$$V_T = \frac{kT}{q}, \tag{1.3}$$

with $q = 1.6 \times 10^{-19}$ Col being the electron charge, and $k = 1.38 \times 10^{-23}$J/°C being the Boltzmann constant. As an example, at $T = 300$ K, $V_T(300) = 0.0259$ V. Without going into further details of the semiconductor physics of BJT, we shall quote the base-emitter voltage function of the BJT from (Johns and Martin 1997).

$$V_{BE}(T) = V_{G0}\left(1 - \frac{T}{T_r}\right) + V_{BE}(T_r)\frac{T}{T_r} - \frac{\rho kT}{q}\ln\left(\frac{T}{T_r}\right) + \frac{kT}{q}\ln\left(\frac{J_C(T)}{J_C(T_r)}\right), \tag{1.4}$$

where V_{G0} is the bandgap voltage of silicon at 0 K which equals 1.206 V, ρ is a process dependent temperature constant and equals 1.93 in the process concerned, and T_r is a reference temperature. Consider a temperature dependent collector current that can be modeled as

$$I_C(T) = a \times T^{\theta}, \tag{1.5}$$

where a is a constant and θ is the order of temperature dependency, $\theta = 0$ implies the collector current is independent with temperature, and $\theta = 1$ implies the collect current varies linearly with temperature, and so on. The collector current density at temperature T with respect to the collector current density at the reference temperature T_r is given by

$$\frac{J_C(T)}{J_C(T_r)} = \left(\frac{T}{T_r}\right)^{\theta}. \tag{1.6}$$

We can thus simplify $V_{BE}(T)$ as

$$V_{BE}(T) = V_{G0}\left(1 - \frac{T}{T_r}\right) + V_{BE}(T_r)\frac{T}{T_r} - (\rho - \theta)\frac{kT}{q}\ln\left(\frac{T}{T_r}\right). \tag{1.7}$$

It can be observed that $V_{BE}(T)$ is nonlinearly related to temperature. Furthermore, because of the $V_{BE}(T_r)$ term in the above equation, $V_{BE}(T)$ might vary with the biasing condition (which depends on the collector current) as well as the transistor size (which depends on the emitter area). Figure 1.2 shows the SPICE simulation of the temperature dependency of the V_{BE} of a NPN BJT with 25 μm^2 emitter area and biased with $I_C = 6$ μA. The V_{BE} is observed to be 0.73 V at $T = 300$ K, and it decreases with temperature almost linearly at a rate of -1.73 mV/K at 300 K. Such a temperature characteristic is known as *Complementary to Absolute Temperature* (CTAT), where the rate of change of V_{BE} against temperature is negative. When biased with different collector currents, the $V_{BE}(T)$ will vary as shown in the SPICE simulation result in Figure 1.2. To simplify our discussions in subsequent chapters, we shall assume that the BJTs are biased appropriately (with $I_C = 6$ μA), such that the $V_{BE}(T)$ can be approximated as a linear temperature function with high accuracy (unless otherwise

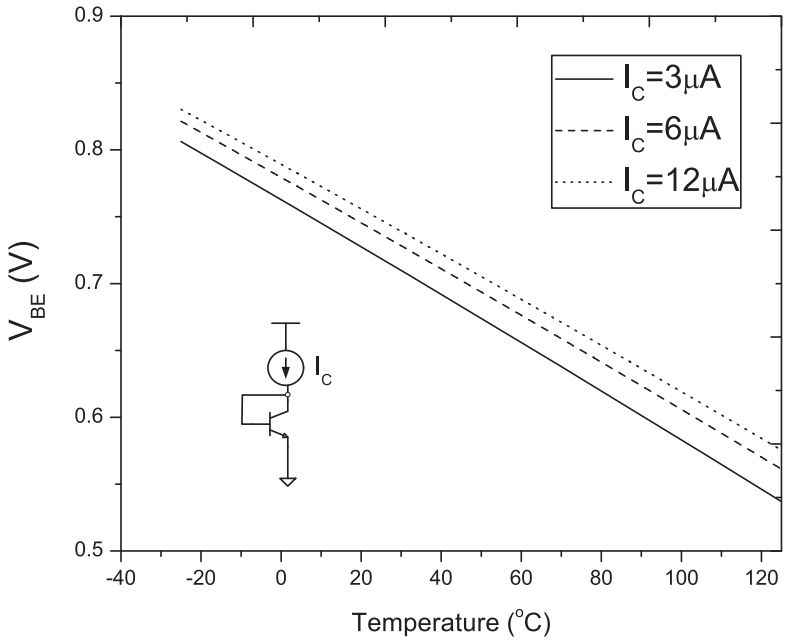


Figure 1.2 V_{BE} vs temperature of a NPN transistor with emitter area 25 μm^2 biased at $I_C = 3, 6, 12$ μA.

specified). In particular, the linear temperature dependency approximation of the V_{BE} for the NPN transistor is given by

$$\frac{\partial V_{BE}(T)}{\partial T} = -1.73 \text{ mV/K}. \tag{1.8}$$

Similarly, the $V_{EB}(T)$ of a PNP transistor has a linear temperature dependency given by

$$\frac{\partial V_{EB}(T)}{\partial T} = -1.39 \text{ mV/K}. \tag{1.9}$$

These two linearly approximated temperature characteristics of the $V_{BE}(T)$ and $V_{EB}(T)$ voltages will be applied in all our discussions unless stated otherwise. In reality, the CTAT characteristic of $V_{BE}(T)$ is not a linear temperature function as depicted in Equation 1.4, and $\partial V_{BE}(T)/\partial T$ is a high order temperature function that will cause curvature error as will be discussed in later chapters. Nevertheless, the $V_{BE}(T)$ is the PN junction voltage, which is a process independent parameter, and is one of the robust parameters in modern CMOS processes that can be used to construct a stable and precise reference voltage.

1.1.1 Differential V_{BE}

As derived in Equation 1.4, $V_{BE}(T)$ is a high order function of temperature T. However, the difference of the $V_{BE}(T)$ between two BJTs biased with different current densities can be well represented by a low order function or even as a linear function of the temperature T. Figure 1.3 illustrates a method to extract the differential V_{BE}, $\Delta V_{BE_{1,2}}$, from two BJTs Q_1 and Q_2 with emitter areas A_{E_1} and A_{E_2}, respectively (readers should note that $V_{BE}(T)$ and V_{BE} will both be used in this book and have exactly the same meaning). Assume $A_{E_1} : A_{E_2} = 1 : N$ and the

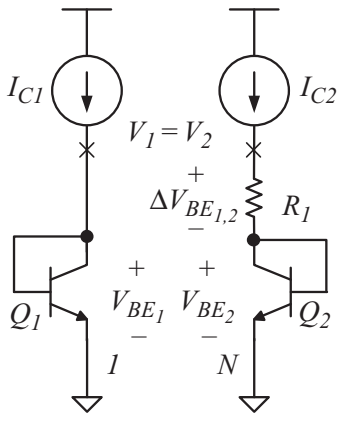


Figure 1.3 Extraction of $\Delta V_{BE_{1,2}}$ from *NPN* transistors.

current sources will provide $I_{C_1} = I_{C_2}$. As a result, the current density J_{C_1} of Q_1 is N times larger than the current density J_{C_2} of Q_2. This yields $\Delta V_{BE_{1,2}}$ as

$$\begin{aligned}\Delta V_{BE_{1,2}} &= V_{BE_1} - V_{BE_2} && (1.10)\\ &= V_T \ln\left(\frac{I_{C_1}}{J_S A_{E_1}}\right) - V_T \ln\left(\frac{I_{C_2}}{J_S A_{E_2}}\right) && (1.11)\\ &= V_T \ln\left(\frac{A_{E_2}}{A_{E_1}}\right) && (1.12)\\ &= V_T \ln(N), && (1.13)\end{aligned}$$

where V_{BE_1} and V_{BE_2} are the base-emitter voltage of BJTs Q_1 and Q_2, respectively. It can be observed that $\Delta V_{BE_{1,2}}$ is proportional to V_T, which is a linear function of T. If we rewrite Equation 1.13 with respect to V_T, we shall obtain

$$V_T = \frac{\Delta V_{BE_{1,2}}}{\ln(N)}, \tag{1.14}$$

which implies the $\Delta V_{BE_{1,2}}$ extraction circuit is actually a V_T extraction circuit as well. Note that

$$\begin{aligned}\frac{\partial V_T}{\partial T} &= \frac{\partial \frac{kT}{q}}{\partial T} = \frac{k}{q}\\ &\approx 0.09\ \text{mV/K} \ \text{ at 300 K.} && (1.15)\end{aligned}$$

It can be observed from Equation 1.15 that the thermal voltage is an intrinsic linear *Proportional to Absolute Temperature* (PTAT) voltage. Figure 1.4 shows the SPICE simulation result of the

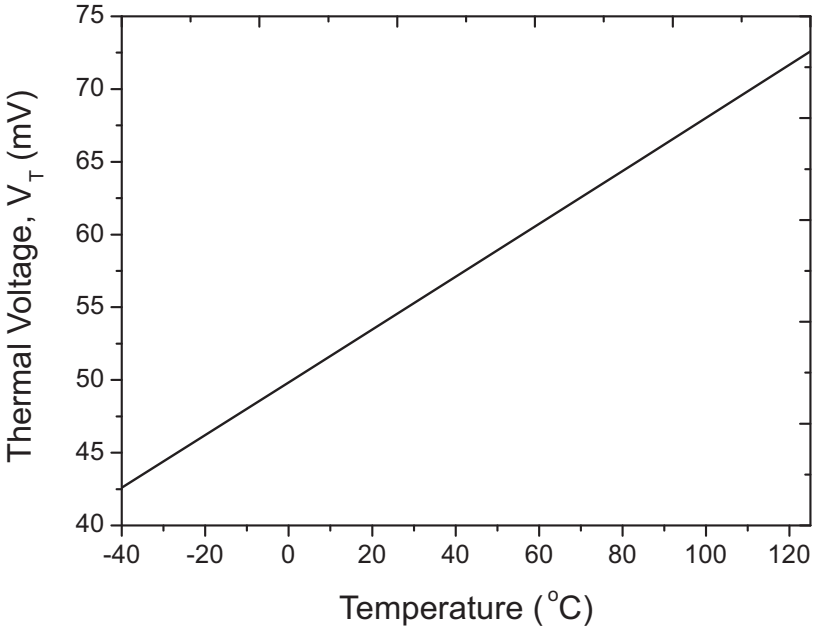


Figure 1.4 Thermal property of V_T extracted from $\Delta V_{BE_{1,2}}$ with emitter area ratio $N = 8$ using the circuit shown in Figure 1.3.

thermal property of V_T extracted from $\Delta V_{BE_{1,2}}$ using the circuit shown in Figure 1.3 with $N = 8$, which demonstrates the PTAT nature of V_T.

The PTAT voltage V_T and the CTAT voltage V_{BE} are commonly used as the thermal elements to generate a temperature insensitive reference voltage. A zero *Temperature Coefficient* (TC) reference voltage can be obtained by compensating the CTAT voltage V_{BE} with a weighted PTAT voltage V_T (The temperature coefficient will be formally defined in Section 2.1.2). The compensation obtained in the form of voltage sum can be easily implemented by the resistor network. However, the resistance of the resistor implemented in the CMOS process is process sensitive, thus imposing another adverse effect on the obtained reference voltage. The derivation of the weighting factor and the methods to compensate the adverse effects from the process variation problem will be discussed in Chapter 4.

1.2 Metal-Oxide Semiconductor Field-Effect Transistor

The metal-oxide semiconductor field-effect transistor, MOSFET, has proved extremely popular compared to the BJT. This is because of the compact layout and simple structure of the MOSFET. In this text, we shall mainly concentrate on the enhancement-mode MOSFET, including both the N-channel MOSFET (NMOS) and P-channel MOSFET (PMOS), since they are the most commonly available MOSFET devices in modern CMOS foundry services. Other types of MOS transistors will be discussed over the course of voltage reference circuit development in later chapters when such devices are applied. Showing in Figure 1.5 are the symbols of the MOSFETs that we shall use in this text. Physically, the MOSFET is a four-terminal device with a source, drain, gate, and substrate terminals. The substrate terminals of the NMOS and PMOS transistors are usually connected to GND and V_{DD}, respectively. We shall use the simplified three-terminal symbols as shown in Figure 1.5 throughout the book. The arrows beside the MOSFET symbols illustrate the direction of the current that is flowing through the drain and source terminals. The silicon layout of an NMOS transistor is shown in Figure 1.5(c). To understand the operation of the MOSFET device, let us consider the physical structure of a NMOS transistor as shown in Figure 1.6, where the NMOS transistor is fabricated directly on the P-type substrate, with N^+ regions forming the drain and source terminals, and with electrons as charge carriers. With the source terminal being grounded, and a positive voltage applied to the gate terminal, the positive voltage at the gate terminal attracts the negative electrons in the P-type substrate to accumulate under the gate terminal and repel the positive holes downwards, thus inverting the substrate surface from P-type to N-type. As a result, this layer is also known as the "*inversion*" layer, which connects the drain and source regions. This layer is also known as the N-channel in the NMOS transistor. The N-channel is completely formed when the NMOS transistor gate-to-source voltage, V_{GS}, is greater than its threshold voltage $V_{th,n}$, where the value of the threshold voltage is determined at device fabrication. Once the channel is created, there will be I_{DS} flows through the channel from the drain to the source terminals, where mobile electrons are the majority charge carriers. As a result, the NMOS transistor can be considered in three modes which depend on the channel condition, and in turn depend on the voltages across different terminals of the transistors. The details of different operation modes will be discussed in the next section. In contrast to the NMOS transistor, the PMOS transistor is fabricated on N-type substrate (in N-well CMOS process, the N-type substrate of a PMOS transistor is usually defined by the N-well), with P^+ regions forming the drain and source terminals, and uses holes as the majority charge carriers.

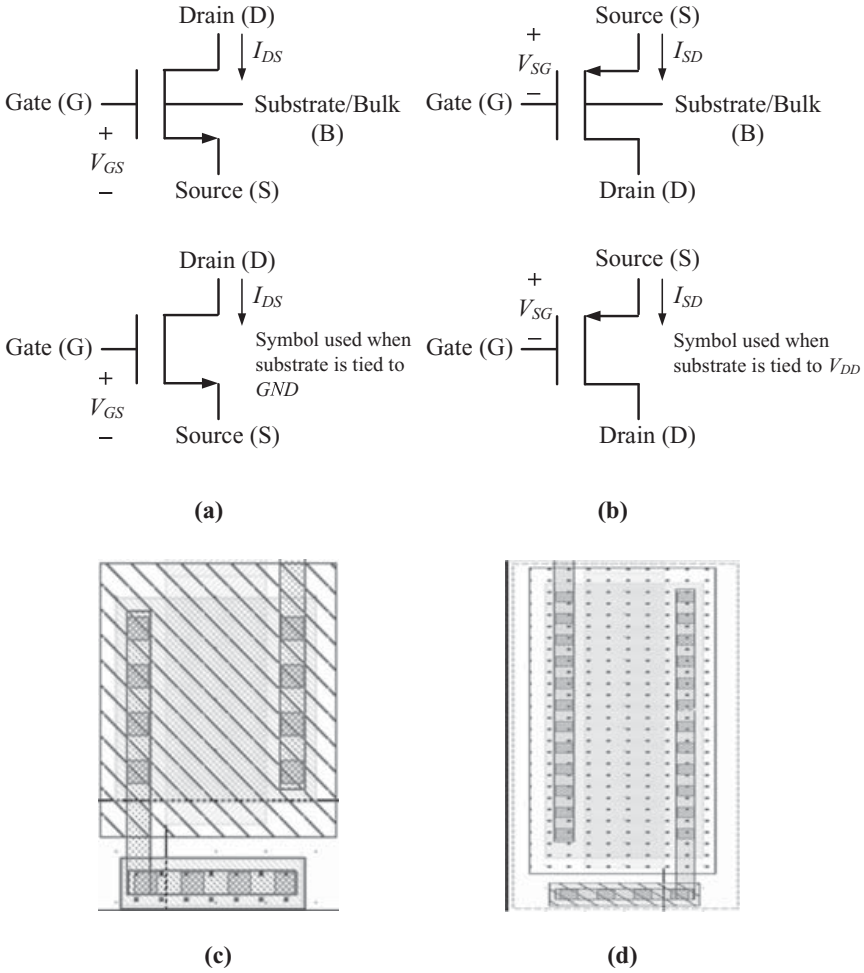


Figure 1.5 Symbols for (a) NMOS transistor and (b) PMOS transistor, and layouts of (c) NMOS transistor and (d) PMOS transistor.

An example layout of the PMOS transistor is shown in Figure 1.5(d). The PMOS transistor operates similarly as its NMOS transistor counterpart, except that V_{GS}, V_{DS}, and the threshold voltage $V_{th,p}$ are negative. Moreover, the current flowing through the channel enters from the source terminal and leaves through the drain terminal, and thus is known as I_{SD}.

As discussed, the threshold voltage V_{th}, particularly $V_{th,n}$ for the NMOS transistor and $V_{th,p}$ for the PMOS transistor, is an important parameter which defines the minimum gate voltage required to accumulate sufficient numbers of charge carriers to form the inversion channel in the MOSFET. Showing in Figure 1.7 is the relationship of I_{DS} and V_{GS} of a NMOS transistor obtained from SPICE simulation with 2 μm channel width and 1 μm channel length at $V_{DS} = 0.1$ V. It can be observed from Figure 1.7 that the positive gate voltage V_{GS} of the NMOS transistor must be larger than $V_{th,n}$ before a conducting channel is induced. In this case, the MOSFET is said to be biased at strong inversion. Similarly, a PMOS transistor requires a gate voltage that is more negative than $V_{th,p}$ to induce the conducting channel with holes as charge carriers. For the process under attention in this book

$$V_{th,n} = 0.48 \text{ V}, \tag{1.16}$$

$$V_{th,p} = -0.47 \text{ V}. \tag{1.17}$$

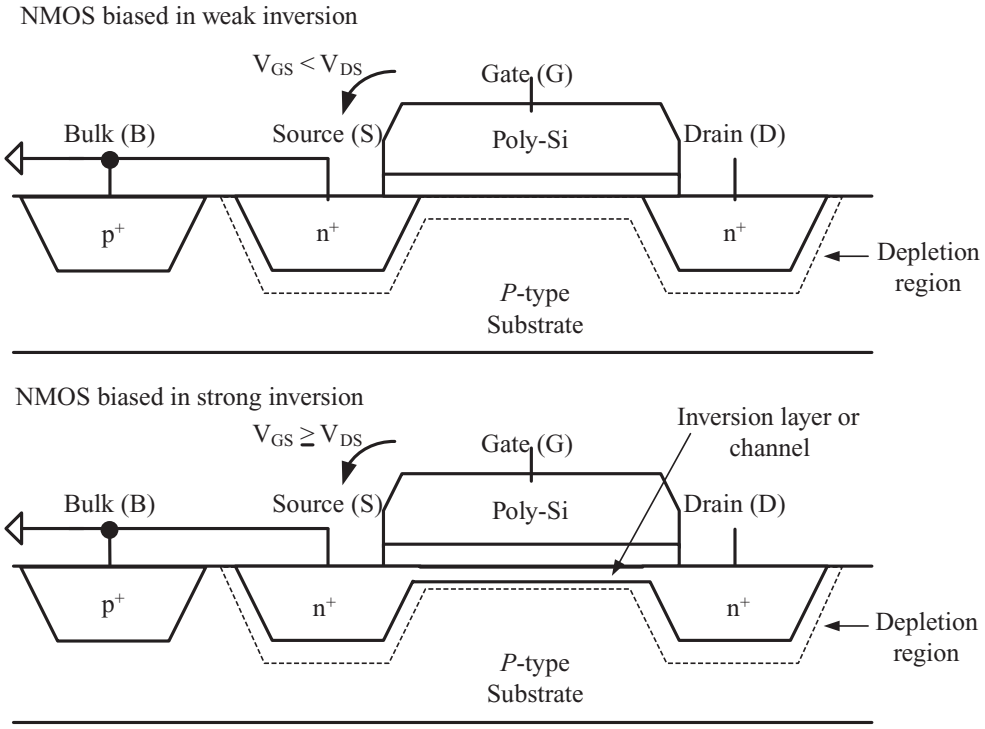


Figure 1.6 NMOS device structure biased in weak inversion and strong inversion.

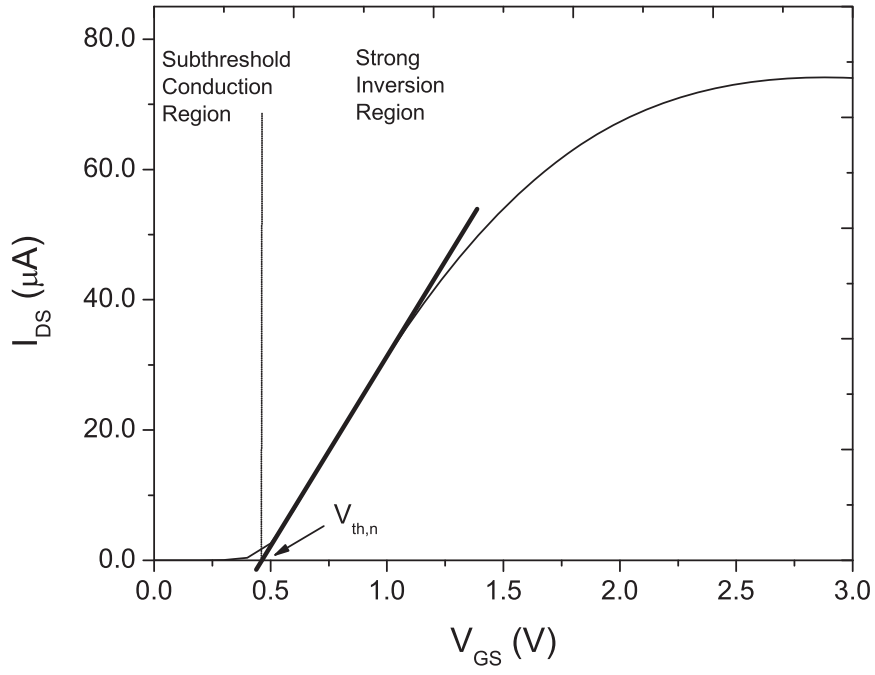


Figure 1.7 The I_{DS} versus V_{GS} of a NMOS transistor with $S = W/L = 2\ \mu m/1\ \mu m$.

Table 1.1 Summary of channel conditions and operation modes of NMOS transistor.

Voltage Condition	Channel Condition	MOS Operation Mode
$V_{GS} = 0$	No Inversion	Cutoff
$0 < V_{GS} < V_{th,n}$	Weak Inversion	Subthreshold
$0 < V_{GS} < V_{th,n}$ $V_{DS} < 4V_{th,n}$	Weak Inversion	Triode, Linear
$V_{GS} \geq V_{th,n}$ $V_{DS} < V_{GS} - V_{th,n}$	Strong Inversion	Triode, Linear
$V_{GS} \geq V_{th,n}$ $V_{DS} \geq V_{GS} - V_{th,n}$	Strong Inversion	Saturation

Note that subthreshold conduction is possible even though the current I_{DS} is very small. In this case the MOSFET is biased at weak inversion with $0 < V_{GS} < V_{th,n}$.

In addition to the inversion condition of the channel, the operation of the MOSFET is also classified into different operation regions with respect to the V_{GS} and V_{DS} voltage conditions. Table 1.1 and Table 1.2 summarize the operation modes and the corresponding channel conditions of the NMOS transistor and PMOS transistor, respectively. As discussed, the physical operation of the NMOS transistor and PMOS transistor are more or less the same with the only difference being that the voltage and current polarity are reversed. To avoid confusion, the use of notation in Table 1.1 and Table 1.2 is the same as the absolute values of the voltages under concern for the case of the PMOS device. In the following sections, we shall discuss the four operation modes of NMOS transistor in detail and in particular we shall emphasize its physical operation and thermal properties which are applicable to bandgap voltage reference circuit design. Since the PMOS transistor exhibits similar properties as that of the NMOS transistor, the physical operation details for PMOS transistor will be skipped. However, to complete our discussions, the relevant analytical relationship of the PMOS transistor will also be presented. In particular, the subscript "*sub*", "*lin*", and "*sat*" will be appended to V_{GS} and

Table 1.2 Summary of channel conditions and operation modes of PMOS transistor.

Voltage Condition	Channel Condition	MOS Operation Mode
$V_{GS} = 0$	No Inversion	Cutoff
$\lvert V_{GS}\rvert < \lvert V_{th,p}\rvert$	Weak Inversion	Subthreshold
$\lvert V_{GS}\rvert < \lvert V_{th,p}\rvert$ $\lvert V_{DS}\rvert < \lvert 4V_{th,p}\rvert$	Weak Inversion	Triode, Linear
$\lvert V_{GS}\rvert \geq \lvert V_{th,p}\rvert$ $\lvert V_{DS}\rvert < \lvert V_{GS} - V_{th,p}\rvert$	Strong Inversion	Triode, Linear
$\lvert V_{GS}\rvert \geq \lvert V_{th,p}\rvert$ $\lvert V_{DS}\rvert \geq \lvert V_{GS} - V_{th,p}\rvert$	Strong Inversion	Saturation

I_{DS} to indicate the operating mode of the MOSFET throughout this book, such that there will be no confusion about which equations are being referred to in the analytical analysis of the voltage reference circuit in later sections.

1.2.1 Cutoff Region

We start our discussions with the NMOS transistor working in the cutoff region, which is the case when $V_{GS} = 0$ with the source region tied to GND. Since there is no bias voltage applied to the gate terminal, the inversion layer is not formed. This is physically equivalent to having two back-to-back diodes connected in series between the drain and source regions. For the NMOS transistor, a diode is formed by the PN junction between the N^+ drain region and the P-type substrate, and another diode is formed by the PN junction between the P-type substrate and the N^+ source region. These back-to-back diodes prevent current conduction from drain to source when a voltage V_{DS} is applied. Theoretically, the $I_{DS} = 0$ when $V_{GS} = 0$. However, as observed in Figure 1.7, $I_{DS} \neq 0$ when $V_{GS} = 0$. This current is known as the leakage current or the "*off*" current, which takes the major part of the static power consumption of the CMOS circuits. However, the leakage current is very small, usually as small as 10^{-11}A as shown in Figure 1.8, therefore we shall assume $I_{DS} = 0$ for the NMOS transistor when it is working in the cutoff mode with $V_{GS} = 0$.

1.2.2 Subthreshold Conduction

As observed in Figure 1.7, the drain current I_{DS} is very close to zero until $V_{GS} > V_{th,n}$. To better understand the relationship between I_{DS} and V_{GS}, a semilog plot of Figure 1.7 is

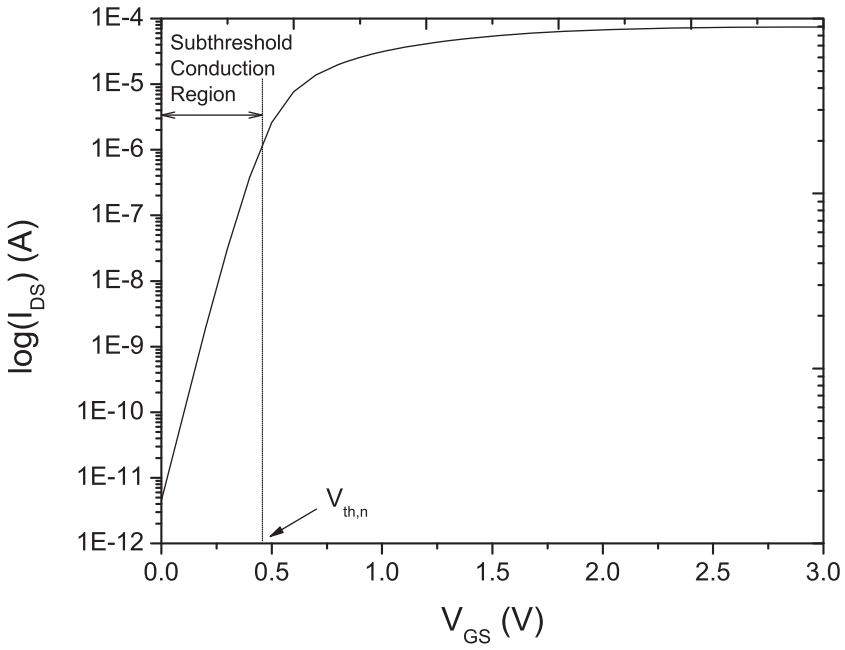


Figure 1.8 The semilog plot of (I_{DS}) versus V_{GS} of a NMOS transistor with $W/L = 2\ \mu\text{m}/1\ \mu\text{m}$.

shown in Figure 1.8, where it is very clear that a low level I_{DS} conduction is achieved with $0 < V_{GS} < V_{th,n}$. This kind of current conduction is known as subthreshold conduction where the inversion layer is not completely formed. As a result, the subthreshold conduction is not the consequence of the charge carrier flowing from the drain to the source through the inversion layer. The subthreshold conduction is mainly due to the existence of an electric field between the drain and source regions. The electrons travel from the drain to the source by direct tunneling under the effect of the electric field. The drain current of the NMOS transistor in the subthreshold mode is given by

$$I_{D,sub} = I_{D,leak} \exp \frac{V_{GS,sub}}{\zeta_n V_T} = \hat{I}_{D,leak} S \exp \frac{V_{GS,sub}}{\zeta_n V_T}, \tag{1.18}$$

where $I_{D,leak}$ is the drain-to-substrate leakage current, $S = W/L$ is the channel width to length ratio of the MOSFET, $\hat{I}_{D,leak}$ is the unit drain-to-substrate current normalized by S, such that $I_{D,leak} = S\hat{I}_{D,leak}$, and

$$\zeta_n = 1 + \frac{C_{D,n}}{C_{ox,n}}, \tag{1.19}$$

is a non-ideal factor, also known as the subthreshold slope, which depends on the depletion capacitance, $C_{D,n}$, and the gate oxide capacitance, $C_{ox,n}$. Since $C_{D,n}$ is always smaller than or equal to $C_{ox,n}$, as a result $1 \leq \zeta_n \leq 2$. The subthreshold current of the PMOS transistor has the same form as that in Equation 1.18 and is given by

$$I_{D,sub} = I_{D,leak} \exp \frac{V_{SG,sub}}{\zeta_n V_T} = \hat{I}_{D,leak} S \exp \frac{V_{SG,sub}}{\zeta_p V_T}, \tag{1.20}$$

where $V_{GS,sub}$ in Equation 1.18 for the NMOS transistor is now changed to $V_{SG,sub}$ for the PMOS transistor and ζ_p is same as that defined in Equation 1.19 with the subscript n replaced by p for the PMOS transistor. It can be observed that the subthreshold drain current of a MOSFET has a similar exponential current–voltage relationship as that of I_C versus V_{BE} relationship in BJT. As a result, this suggests that a controllable temperature dependent voltage can be implemented by MOSFET in the subthreshold mode in a similar manner to that of the BJT, and this will be demonstrated in later sections (Vittoz and Neyroud, 1979). Even though the above sentence is correct from a macro view of the temperature insensitive circuit design, there are important differences between the two. First, the subthreshold current is small. Even worse, the drain-to-source resistance $R_{DS,sub}$ in the subthreshold mode is large, which will induce large thermal noise in the circuit when compared to that of the BJT, as will be discussed in Section 1.4. Second, MOSFET has intrinsic matching problems. As a result, a larger output voltage variation may be observed from the CMOS constructed voltage reference circuit when compared to the bipolar counterpart unless special considerations are made in the design. This is especially true for the CMOS circuit with MOSFETs biased in subthreshold mode. Third, the coefficient $I_{D,sub}$ does not have the same temperature coefficient as that of the BJT, and thus will affect the temperature coefficient of the resulting voltage reference circuit.

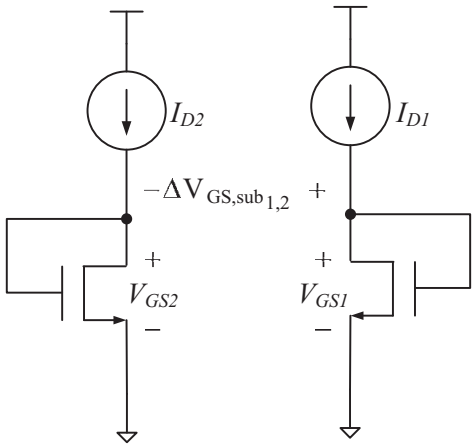


Figure 1.9 Extraction of $\Delta V_{GS_{1,2}}$ from two MOSFETs with the same size biased in subthreshold conduction region with $I_{D1} \neq I_{D2}$.

Finally, the exponential current characteristic of the subthreshold current in MOSFET contains a factor ζ, which further depends on the voltage-dependent depletion capacitance. Since it is difficult, if not impossible, to obtain a stable and known voltage when designing the voltage reference circuit using MOSFET in subthreshold mode (actually if a known and stable voltage is available, then the voltage reference design problem does not even exist), therefore great care has to be taken to use MOSFET in the subthreshold region to design voltage reference circuits that achieve the same precision as that obtained by the voltage reference circuit using BJTs.

1.2.2.1 Differential $V_{GS,sub}$

Similarly to the differential V_{BE} derived in Section 1.1.1, the difference of the V_{GS} between two MOSFETs of the same size biased in the subthreshold conduction mode with different current densities is a low order function of temperature T, which depends on V_T, and the subthreshold slope ζ. With reference to a pair of NMOS as shown in Figure 1.9,

$$\Delta V_{GS,sub_{1,2}} = V_{GS_1} - V_{GS_2}, \tag{1.21}$$

$$= \zeta_n V_T \ln\left(\frac{I_{D_1}}{I_{D_2}}\right). \tag{1.22}$$

This is a favorable property because all other higher order temperature characteristics of the device will cancel each other out. The SPICE simulation result of the $\Delta V_{GS,sub_{1,2}}$ voltage extracted from the schematic in Figure 1.9 with the two MOSFETs of the same size, where $S_1 = S_2 = 2\ \mu\text{m}/1\ \mu\text{m}$, biased in the subthreshold conduction region with $I_{D_1} = \frac{1}{8} I_{D_2} = 50\,\text{nA}$, is plotted in Figure 1.10. The result shows that $\Delta V_{GS,sub_{1,2}}$ is PTAT and is almost linearly proportional to temperature.

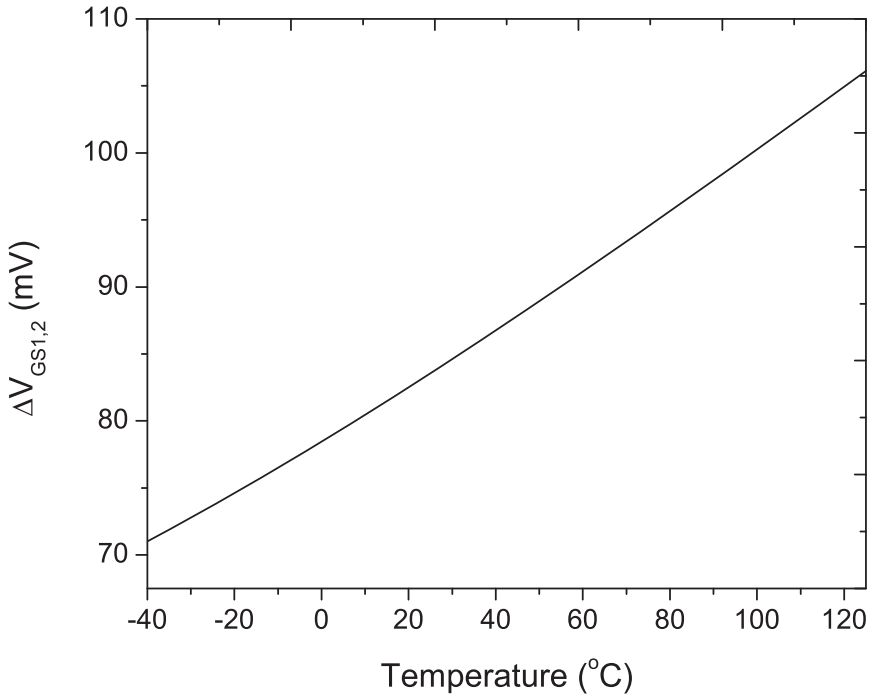


Figure 1.10 Thermal property of $\Delta V_{GS_{1,2}}$ extracted from MOSFET biased in the subthreshold conduction mode connected as shown in Figure 1.9 with $I_{D_1} = \frac{1}{8} I_{D_2} = 50$ nA.

1.2.3 Triode Region

Gradually increasing V_{GS}, the transistor will leave the weak inversion region and enter the strong inversion region, where more electrons (the majority charge carriers of the NMOS transistor) will be attracted and accumulated near the surface of the substrate under the gate terminal. The gate and substrate form a parallel-plate capacitor with the oxide layer acting as the dielectric layer of the capacitor. The positive gate voltage causes negative charges in the channel to accumulate on the top plate of the capacitor. The corresponding positive charges on the bottom plate will develop a uniform electric field in the vertical direction. The electric field induced by V_{DS} will control the amount of charge in the channel, and thus determine the channel conductivity, which in turn controls the magnitude of the I_{DS} flowing through the channel.

When $V_{GS} = V_{th,n}$, a N-channel is induced in the NMOS transistor. In this case, the magnitude of I_{DS} is still negligibly small irrespective of the value of V_{DS} because the N-channel has just enough charge carriers to make it conductive. When V_{GS} increases to be greater than $V_{th,n}$, more electrons are attracted to the channel, hence increasing the numbers of charge carriers in the channel and thus increasing the conductance of the N-channel. As a result, the channel contains sufficient numbers of charge carriers to achieve a conduction current I_{DS} when a small V_{DS} is applied. The conductance of the channel is proportional to the excess gate voltage $(V_{GS} - V_{th,n})$, also known as the *effective voltage*. It follows that the magnitude of the current I_D will be linearly proportional to $(V_{GS} - V_{th,n})$ when $V_{DS} > 0$, such that the NMOS transistor operates as a linear resistor with its resistance controlled by the effective voltage $(V_{GS} - V_{th,n})$. In this case, the NMOS transistor is said to be operating in the *linear region*,

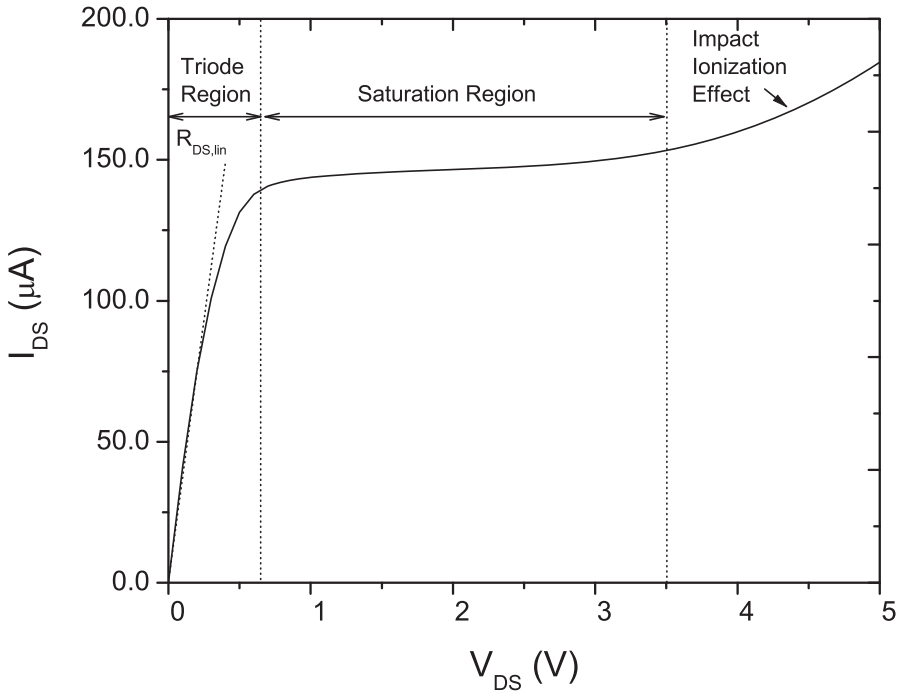


Figure 1.11 The I_{DS} versus V_{DS} of an NMOS transistor with $W/L = 2\ \mu\text{m}/1\ \mu\text{m}$ at $V_{GS} = 1.2\ \text{V} > V_{th,n}$.

which is also known as the *triode region*. The I_{DS} of the NMOS transistor in the linear region is related to V_{GS} by

$$I_{DS,lin} = \mu_n C_{ox,n} \left(\frac{W}{L}\right) \left(V_{GS,lin} - V_{th,n}\right) V_{DS}, \tag{1.23}$$

where μ_n is the carrier mobility in the N-channel and $C_{ox,n}$ is the gate oxide thickness of the NMOS transistor. Figure 1.11 shows the SPICE simulation result of $I_{DS,lin}$ versus V_{DS} of a NMOS transistor at $V_{GS} = 1.2$ V with $W/L = 2\ \mu\text{m}/1\ \mu\text{m}$. A linear relationship between $I_{DS,lin}$ and V_{DS} can be observed from the figure, where the slope is known as the on-resistance of the MOSFET in linear mode, and is given by

$$R_{DS,lin} = \frac{1}{\mu_n C_{ox,n}\left(\frac{W}{L}\right)\left(V_{GS,lin} - V_{th,n}\right)}. \tag{1.24}$$

The PMOS transistor operates similarly to the NMOS transistor where the $I_{DS,lin}$ relates to $V_{SG,lin}$ of the PMOS transistor biased in the linear region and is given by

$$I_{DS,lin} = \mu_p C_{ox,p} \left(\frac{W}{L}\right) \left(V_{SG,lin} - |V_{th,p}|\right) V_{SD}, \tag{1.25}$$

where μ_p is the carrier mobility of the P-channel and $C_{ox,p}$ is the gate oxide thickness of the PMOS transistor.

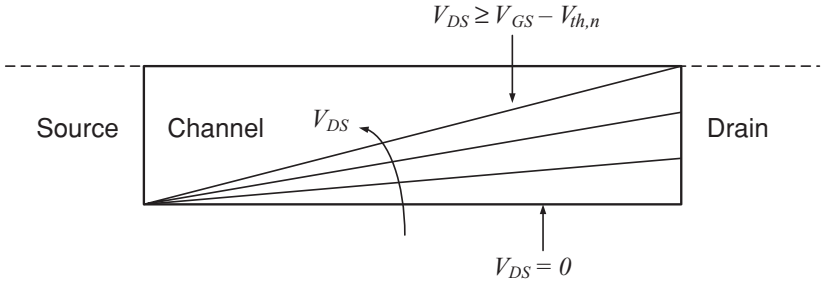


Figure 1.12 Change in channel shape with increasing V_{DS} of a NMOS transistor.

1.2.4 Saturation Region

If we further increase the V_{DS}, the NMOS transistor will enter the saturation region as shown in Figure 1.11. Let us first consider the case of $V_{DS} \leq (V_{GS} - V_{th,n})$, the voltage difference between the gate and the channel is not sufficient to form a uniform inversion layer between the source and drain region, due to the increasing electric field between the drain and the source regions. Figure 1.12 illustrates the channel tapering with increasing V_{DS} and it begins to become "*pinched-off*" when $V_{DS} = (V_{GS} - V_{th,n})$. Further increasing V_{DS} will not increase I_{DS}, and I_{DS} is no longer linearly proportional to V_{GS} as you can easily observe from Figure 1.11. In this case, the NMOS transistor is said to be operating in the saturation region. In the saturation region, the $I_{DS,sat}$ is independent of the drain-to-source voltage V_{DS}, but related to $V_{GS,sat}$ in a square-law relationship given by

$$I_{DS,sat} = \frac{1}{2}\mu_n C_{ox,n}\left(\frac{W}{L}\right)\left(V_{GS,sat} - V_{th,n}\right)^2. \tag{1.26}$$

The MOSFET biased in saturation mode behaves as an ideal current source with the current magnitude being controlled by the $V_{GS,sat}$ as shown in Figure 1.13. The PMOS transistor operates similarly with $I_{SD,sat}$ in the saturation mode given by

$$I_{SD,sat} = \frac{1}{2}\mu_p C_{ox,p}\left(\frac{W}{L}\right)\left(V_{SG,sat} - |V_{th,p}|\right)^2. \tag{1.27}$$

It can be observed from both Equations 1.26 and 1.27 that the drain current of the MOSFET in saturation mode depends only on V_{GS}, and this is useful in the design of current source and current mirrors. Without ambiguity, the rest of the book will use $I_{D,sat}$ for both NMOS and PMOS, where the direction of current flow can be understood from the transistor type, or otherwise the complete subscript will be used to indicate the direction of current flow.

1.2.4.1 Differential $V_{GS,sat}$

Similarly to the differential $V_{GS,sub}$ of the MOSFETs biased in the subthreshold mode derived in Section 1.2.2, the differential $V_{GS,sat}$ extracted from two NMOS transistors biased in the saturation region also demonstrates a low order temperature dependency. Figure 1.14 shows a block diagram to extract the differential V_{GS} from two NMOS transistors biased in saturation

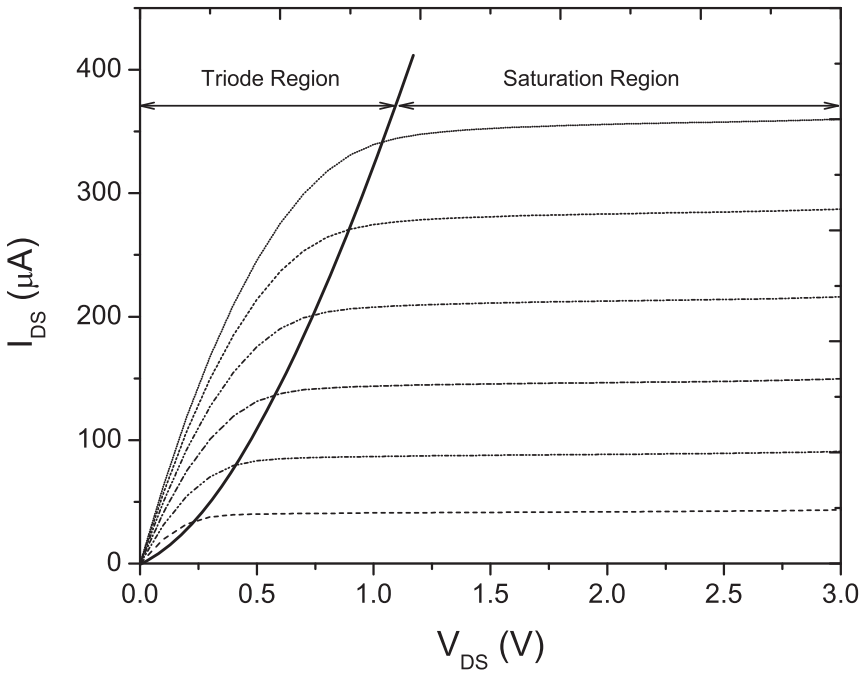


Figure 1.13 The I_{DS} versus V_{DS} characteristic of the NMOS transistor with $W/L = 2\ \mu m/1\ \mu m$ at different V_{GS}.

mode, which was first presented in (Yu and Geiger, 1994). Equation 1.26 can be rewritten in terms of $V_{GS,sat}$ as

$$V_{GS,sat} = \sqrt{\frac{2I_{DS,sat}}{\mu_n C_{ox,n} W/L}} + V_{th,n}. \tag{1.28}$$

If we consider V_{GS_1} and V_{GS_2} of the two NMOS transistors in Figure 1.14 with $S_1 = W_1/L_1$ and $S_2 = W_2/L_2$ being fed with drain currents I_1 and I_2, respectively. As a result both transistors

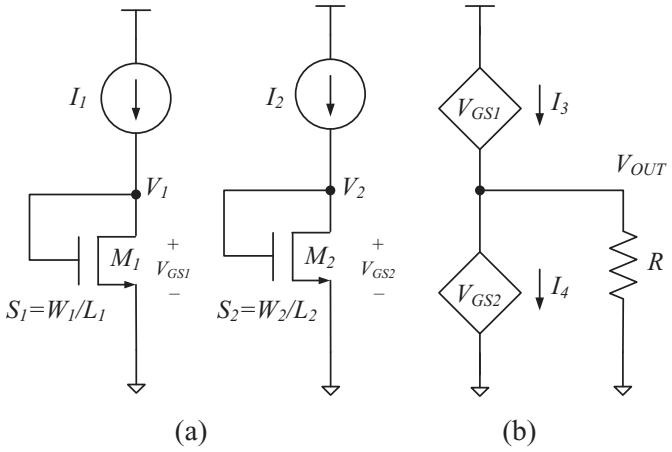


Figure 1.14 Extraction of $V_{th,n}$ from differential V_{GS} with both NMOS transistor biased in the saturation region.

are biased in saturation region. It is possible to obtain V_{OUT} as a function of $V_{th,n}$ by using two voltage controlled current sources as shown in Figure 1.14(b), where I_3 and I_4 are controlled by V_{GS_1} and V_{GS_2}, respectively. The differential current is converted to voltage through resistor R, such that $V_{OUT} = (I_3 - I_4)R$. Define the ratio of the biasing current to the transistor width to length ratio of the two transistors M_1 and M_2 as

$$r = \sqrt{\frac{I_1 S_2}{I_2 S_1}}. \tag{1.29}$$

As a result, $V_{th,n}$ can be obtained as

$$V_{th,n} = \frac{V_1 - r V_2}{1 - r}. \tag{1.30}$$

In other words, by constructing the voltage controlled current source I_3 and I_4 with current output proportional to $\frac{1}{1-r}$ and $\frac{r}{1-r}$ of the control voltages, respectively, the output voltage V_{OUT} in Figure 1.15 will equal the NMOS transistor threshold voltage scaled by R. As an example, by selecting $r = 2$, $S_1 = S_2$, and the proportional constants of the two voltage control current sources for I_3 and I_4 as r/R and $1/R$, respectively, the output voltage is $V_{OUT} = V_{th,n}$, and thus forms a threshold voltage extraction circuit.

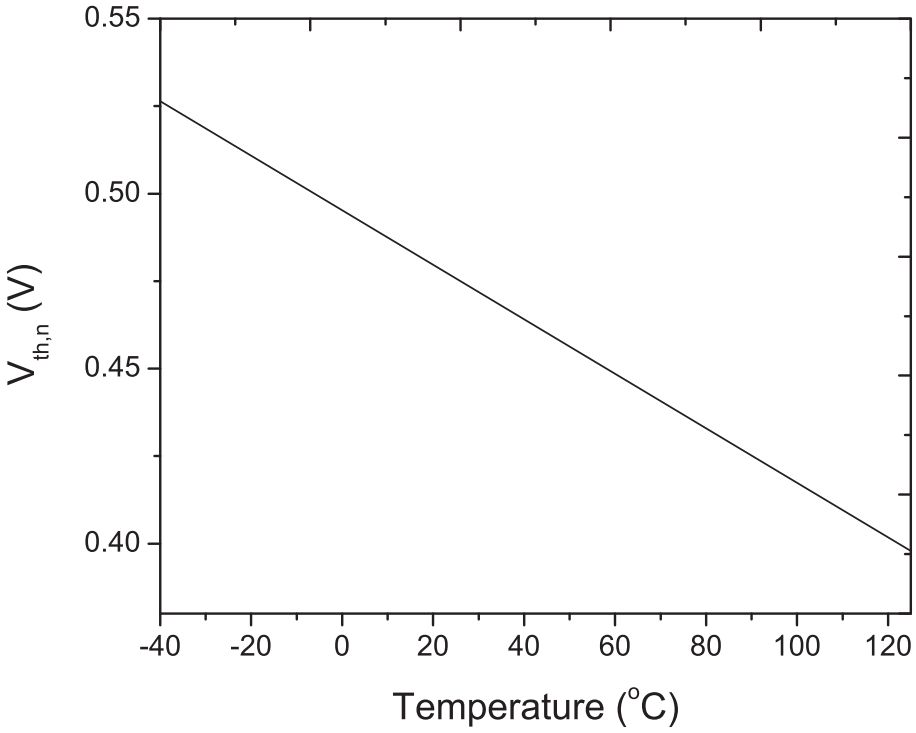


Figure 1.15 The $V_{th,n}$ versus temperature of a NMOS transistor with $W/L = 2\ \mu m/1\ \mu m$.

1.2.5 Thermal Properties

The successful application of any electron device to the temperature insensitive voltage reference circuit will depend on the designer's understanding of the thermal properties of that device. Thermal models of semiconductors exist in a variety of forms and complexities. It was shown that even the simplest thermal models of semiconductor devices can give satisfactory results if properly used. We have already reviewed the PTAT and CTAT properties of ΔV_{BE} and V_{BE} of BJTs, respectively. The previous section has also shown that the thermal property of $I_{DS,sub}$ is similar to its countepart in the BJT. In this section, we shall review the thermal properties of the threshold voltage $V_{th}(T)$, the carrier mobility in channel region $\mu(T)$, and the transconductance $g_m(T)$ of the MOSFETs.

1.2.5.1 The Threshold Voltage ($V_{th,n}$ and $V_{th,p}$)

The threshold voltages of the NMOS and PMOS transistors have similar thermal properties. It has been shown that the threshold voltage exhibits a linear property with respect to temperature variation. An effective and yet simple model for the temperature dependency of the threshold voltage of the MOSFET is given by (Liu 2001)

$$V_{th,n}(T) = V_{th,n}(T_r) - \beta_{th,n}(T - T_r), \tag{1.31}$$

$$|V_{th,p}(T)| = |V_{th,p}(T_r)| - \beta_{th,p}(T - T_r), \tag{1.32}$$

where $\beta_{th,n} = |\frac{\partial V_{th,n}}{\partial T}|$ and $\beta_{th,p} = |\frac{\partial V_{th,p}}{\partial T}|$ are the first order temperature coefficients of the threshold voltages of the NMOS and PMOS transistors, respectively. Figure 1.15 shows the relationship between the threshold voltage and temperature of a NMOS transistor obtained from the SPICE simulation of a NMOS transistor of size $W/L = 2\ \mu m/1\ \mu m$. It can be observed that $V_{th,n}$ is a CTAT term, where $\frac{\partial V_{th,n}}{\partial T} = -0.779\ mV/^{\circ}C$ at $T = 300$ K for the fabrication process under concern. In this case, we can derive $\beta_{th,n} = 0.779\ mV/^{\circ}C$, which is a positive coefficient. Similarly, the thermal coefficient of the $V_{th,p}$ of the PMOS transistor is given by $\beta_{th,p} = 0.802\ mV/^{\circ}C$ for the process under consideration in this book.

1.2.5.2 The Carrier Mobility (μ_n and μ_p)

The thermal property of the carrier mobility of the NMOS and PMOS transistors can be expressed by a simple equation with respect to the carrier mobility of NMOS and PMOS transistors at the reference temperature T_r, which is given by (Liu, 2001)

$$\mu_n(T) = \mu_n(T_r)\left(\frac{T}{T_r}\right)^{-\beta_{\mu n}}, \tag{1.33}$$

$$\mu_p(T) = \mu_p(T_r)\left(\frac{T}{T_r}\right)^{-\beta_{\mu p}}. \tag{1.34}$$

It is clear that the carrier mobility has a temperature coefficient with an exponential order β_μ temperature coefficient, and great care should be taken to apply it in the voltage reference

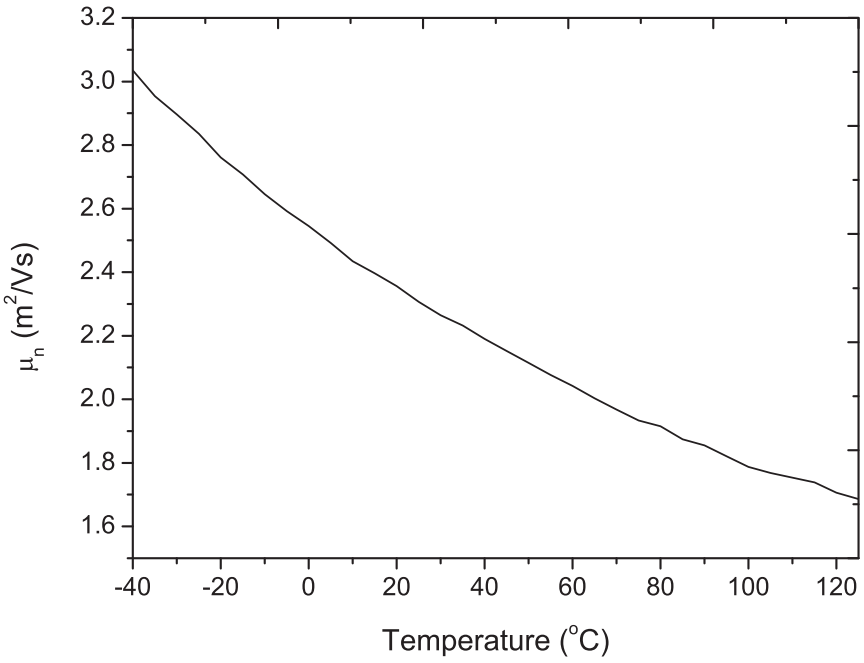


Figure 1.16 The carrier mobility μ_n versus temperature of a NMOS transistor with $W/L = 2\ \mu m/1\ \mu m$.

circuit. In Figure 1.16 the carrier mobility $\mu_n(T)$ obtained by the SPICE simulation of a NMOS transistor of size $W/L = 2\ \mu m/1\ \mu m$ at different temperatures is shown, which reveals that $\mu_n(T)$ has a CTAT property and exponential in nature.

1.2.5.3 The Transconductance (g_m)

Because of the temperature dependencies of the threshold voltage and carrier mobility, other MOSFET properties that depend on these physical parameters of the MOSFET will also be thermal dependent. One such parameter is the transconductance. The transconductance g_m governs the intrinsic gain A of a device with the help of the output impedance r_o (Hu, 2010) such that

$$A = g_m r_o. \tag{1.35}$$

This relationship will be used to analyze the performance of both the MOSFET devices and other circuit modules, such as the opamp, in later chapters.

To be specific, and as an example, the transconductance of a MOSFET defines the amount of drain current that changes with a slight change of voltage on its gate. This allows the computation of g_m at a stable operating point where V_{DS} is held constant and the device is assumed to be operating in saturation region. This is because among all operating modes of the MOSFET, the saturation mode is commonly applied to form the current source, and thus the transconductance has the greatest effect on the MOSFET operating in saturation mode.

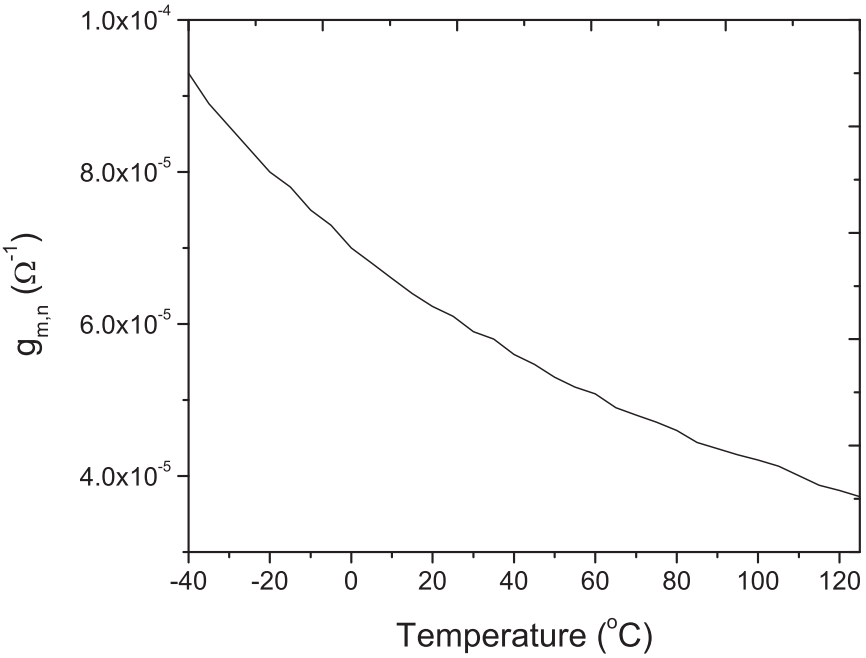


Figure 1.17 The $g_{m,n}$ versus temperature of a NMOS transistor with $W/L = 2\ \mu\text{m}/1\ \mu\text{m}$.

The $g_{m,n}$ of a NMOS transistor biased in the saturation region is given by

$$g_{m,n} = \frac{\partial I_{DS,sat}}{\partial V_{GS,sat}} = \mu_n C_{ox,n} \frac{W}{L}(V_{GS,sat} - V_{th,n}) = \frac{2I_{DS,sat}}{V_{GS,sat} - V_{th,n}}, \tag{1.36}$$

and that for a PMOS transistor is given by

$$g_{m,p} = \frac{\partial I_{DS,sat}}{\partial V_{SG,sat}} = \mu_p C_{ox,p} \frac{W}{L}(|V_{SG,sat}| - |V_{th,p}|) = \frac{2I_{DS,sat}}{|V_{SG,sat}| - |V_{th,p}|}. \tag{1.37}$$

It is clear that the thermal property of g_m is the combined result of the thermal properties of V_{th} and μ, which is further scaled by $C_{ox}\frac{W}{L}$. Since both V_{th} and μ have CTAT property, therefore, it is expected that the thermal property of g_m will also be CTAT. It can be observed from the SPICE simulation result of the $g_{m,n}$ from a NMOS transistor with size $S = W/L = 2\ \mu\text{m}/1\ \mu\text{m}$ plotted in Figure 1.17 that $g_{m,n}$ has a high order temperature coefficient. Moreover, it should be noted that this high order temperature coefficient is further subject to the geometric variation problem of the transistor. As a result, the application of transconductance to the design of a temperature insensitive voltage reference circuit is far more difficult than that of carrier mobility.

1.2.5.4 The Gate Source Voltage (V_{GS})

Similarly to g_m, the temperature dependency of V_{GS} is also affected by the thermal property of the threshold voltage and the carrier mobility. However, unlike the transconductance, the thermal property of V_{GS} is more complicated than it looks. Consider the ($I_{DS,sub}$, $V_{GS,sub}$)

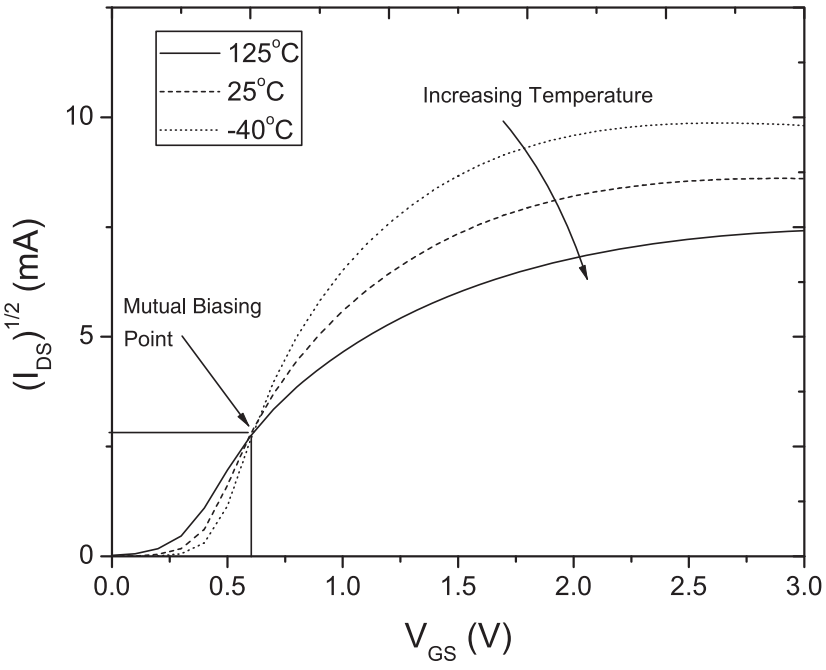


Figure 1.18 The $\sqrt{I_{DS}}$ versus V_{GS} characteristics of a NMOS transistor with $W/L = 2\ \mu m/1\ \mu m$ at different temperatures.

relationship of the subthreshold current in Equation 1.18. We can observe that $V_{GS,sub}$ is linearly proportional to V_T when $\frac{I_{DS,sub}}{I_{DS,leak}}$ is constant. As a result, it is easy to mistake $V_{GS,sub}$ for a PTAT voltage. However, it has been demonstrated in (Giustolisi *et al.*, 2003) that $V_{GS,sub}(T)$ is a CTAT voltage with

$$V_{GS,sub}(T) = V_{GS,sub}(T_r) - \beta_{gs,sub}(T - T_r), \tag{1.38}$$

where $\beta_{gs,sub}$ is the first order temperature coefficient of the MOSFET biased in subthreshold mode, and is a positive number.

If the I_{DS} and V_{GS} keep increasing, the transistor will enter saturation mode. The temperature dependency of $V_{GS,sat}(T)$ depends on μ and V_{th} as derived in Equation 1.28, and is shown to be a PTAT voltage. This dual temperature dependency of V_{GS} can be clearly observed in Figure 1.18, which plots the SPICE simulation of $\sqrt{I_{DS}}$ versus V_{GS} of a NMOS transistor with size $W/L = 2\ \mu m/1\ \mu m$ at various temperatures. It is clear from the curves plotted in the figure that the temperature dependency of (I_{DS}, V_{GS}) exhibits a strong CTAT property at low V_{GS}. The temperature coefficient reduces as V_{GS} increases until a point of mutual biasing where the temperature coefficient of (I_{DS}, V_{GS}) is zero. Then the temperature dependency of (I_{DS}, V_{GS}) will become PTAT as V_{GS} keeps increasing and enters saturation mode. Note that the zero temperature coefficient of (I_{DS}, V_{GS}) at the mutual biasing point is the result of the mutual compensation of the thermal property of the carrier mobility μ_n and the thermal property of the threshold voltage $V_{th,n}$. However, it should also be noted that it is difficult and complicated to bias the MOSFET in this mutual biasing point in order to obtain a temperature independent (I_{DS}, V_{GS}). As a result, great care should be taken with circuits that require a temperature insensitive $I_{DS,sat}$. Similar precautions should also be put in place when designing temperature sensitive circuits using $V_{GS,sub}$.

1.2.6 Channel Length Modulation Effect

As the MOSFET device geometry keeps shrinking, the depletion width of the source and drain regions will become a significant portion of the channel. Since the current that flows through the device is controlled by both the electric field from the gate and the electric field from the drain to the source, this will induce the *channel length modulation effect*. The channel length modulation effect of a MOSFET describes the increase in depletion width at the drain with an increasing drain voltage. As a result, the effective channel length becomes shorter, which leads to an increased drain current. An example is shown in Figure 1.19, where it is clear that the I_{DS} does not flatten with increasing V_{DS} while a small increase is still observed at high V_{DS} region. The channel length modulation effect of a NMOS transistor biased in saturation mode can be modeled by the Shichman–Hodges model (Shichman and Hodges, 1968), which modifies Equation 1.26 to

$$I_{D,sat} = \frac{1}{2}\mu_n C_{ox,n}\left(\frac{W}{L}\right)\left(V_{GS,sat} - V_{th,n}\right)^2(1 + \lambda V_{DS}), \tag{1.39}$$

where λ is the channel length modulation parameter. A similar model as that described by Equation 1.39 applies to the PMOS transistor.

1.3 Diode

All PN junctions in an integrated circuit can be used to form diodes. But only a few of them can actually be used by themselves without unpleasant side-effects. In modern CMOS

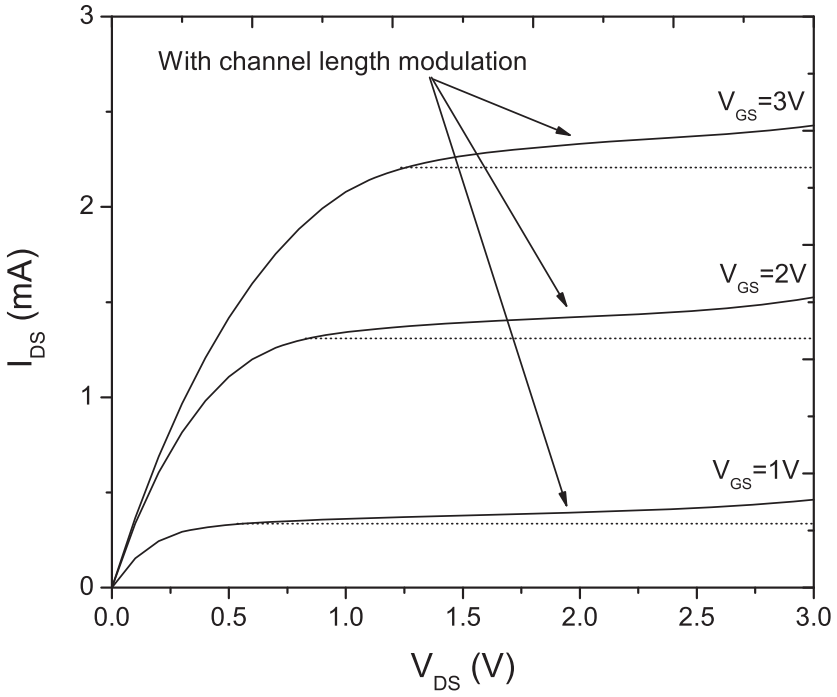


Figure 1.19 The I_{DS} versus V_{DS} characteristics of a MOSFET with increasing drain voltage at various V_{GS}.

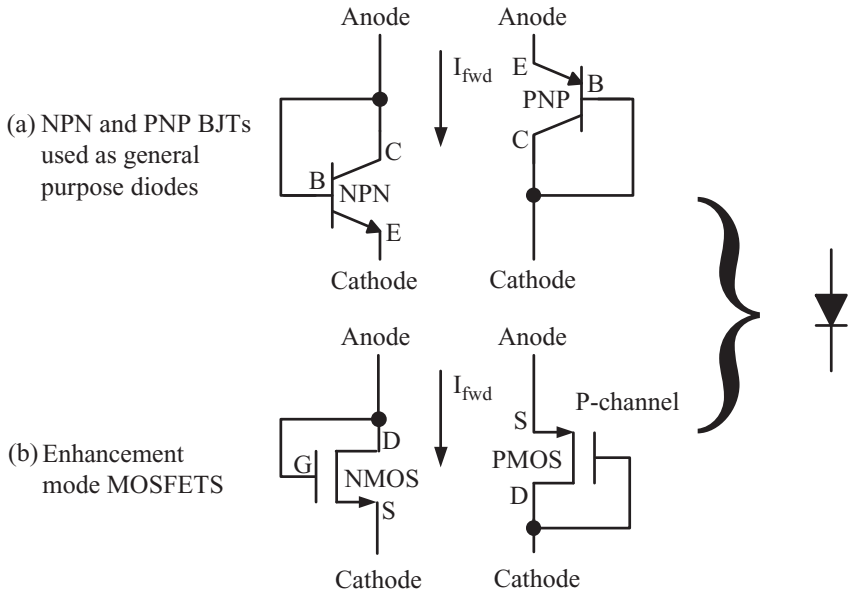


Figure 1.20 Diode connected (a) BJTs and (b) MOSFETs.

processes, there are two useful diode structures: diode connected BJT and diode connected MOSFET as shown in Figure 1.20.

Among all three types of in BJTs (base-emitter, base-collector, and collector-substrate), the base-emitter junction makes a good diode, but it has a fairly high series resistance associated with it. The surrounding collector of the PNP can be connected to the most negative supply voltage, whereas that of the NPN can be connected to the most positive supply voltage, to keep the base-collector and the collector-substrate junctions permanently reverse-biased. But a much better diode can be obtained if the collector and base are connected together, creating a diode-connected BJT as shown in Figure 1.20(a). Note that the transistor is actively biased and has gain. However, if β is large, the base current will only have a small effect on the diode current. In fact, this connection gives you an almost ideal diode.

Besides the diode connected BJT, PN junctions can be obtained from MOSFET, which are the free-floating junctions between the N-channel source-drain and the P-substrate or the P-channel source-drain and the N-well. The term "*diode connected*" MOSFET is used to describe a MOSFET with its gate and drain connected together to form a diode-like structure as shown in Figure 1.20(b). The forward diode voltage obtained from the SPICE simulation of a diode connected NPN BJT at different temperatures is shown in Figure 1.2, which is shown to exhibit a CTAT property. Similarly, the SPICE simulation of the diode connected MOSFET with $W/L = 2\ \mu m/1\ \mu m$ biased in subthreshold mode with $I_{DS,sub} = 400$ nA at different temperatures is shown in Figure 1.21, which is shown to have CTAT thermal characteristics similar to those of the diode connected BJT. Since the MOSFET has a more compact layout when compared to that of BJT, it seems that the MOSFET is a better choice for diode implementation. On the other hand, while the voltage-current property of both diode connected transistors are affected by the biasing current, the biasing current has a greater effect on the diode connected MOSFET than that of diode connected BJT. This is because the diode connected MOSFET is required to be biased at subthreshold mode to obtain a close to linear

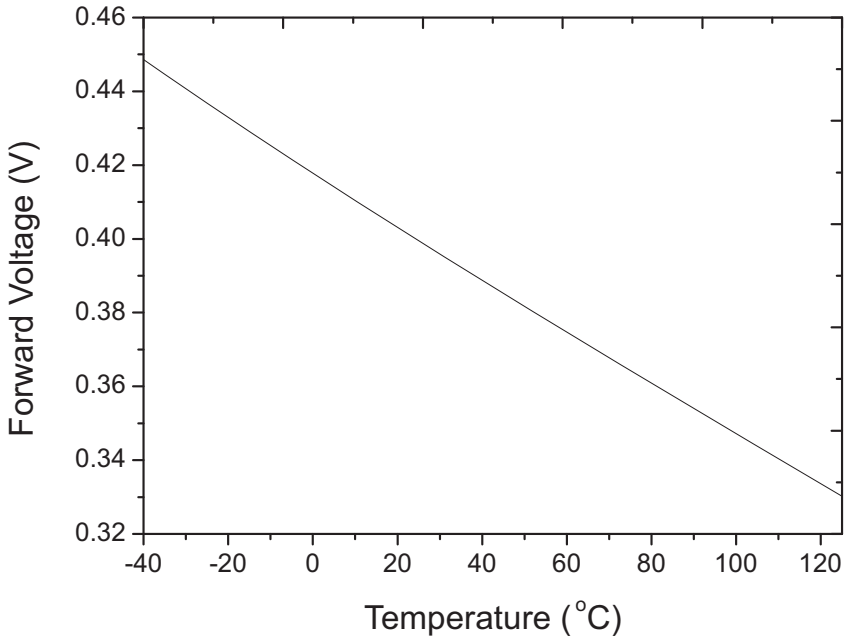


Figure 1.21 Forward voltage of a diode connected NMOS transistor versus temperature biased with 400 nA with W and L being 2 μm and 1 μm.

CTAT property. As a result, the robustness of the diode connected BJT under varying biasing conditions will become a good reason for choosing it for implementation.

1.4 Resistor

A resistor is not only an intrinsic voltage-to-current and current-to-voltage converter, by properly adjusting its value, different weighting can be placed on the converted current and voltage. As a result, it has been popularly deployed in voltage reference circuits. However, most CMOS fabrication processes do not provide a standard structure for the sole purpose of implementing resistors. Instead every free-floating layer in an integrated circuit can, when properly patterned, be used as a resistor. Among various parameters that characterize the integrated resistor, the parameters that are important to voltage reference circuit design are the sheet resistance, R_{sheet}, in $\Omega/\square$, which describes the resistance of a resistor in a unit square, and the temperature and voltage sensitivities (Razavi, 2001), such that

$$R(T) = R_{sheet}\left(1 + T_{CR1}(T - T_r) + T_{CR2}(T - T_r)^2 \cdots + \cdots + T_{CRn}(T - T_r)^n \cdots\right), \tag{1.40}$$

and

$$R(V) = R_{sheet}\left(1 + V_{CR1}(T - T_r) + V_{CR2}(T - T_r)^2 \cdots + \cdots + V_{CRn}(T - T_r)^n \cdots\right), \tag{1.41}$$

where $T_{CR\ell}$ and $V_{CR\ell}$ are the ℓ-th order temperature coefficient and voltage coefficient of the resistor, respectively. As an example, $T_{CR1} = 8.52 \times 10^{-4}$, $T_{CR2} = 3.01 \times 10^{-7}$, $V_{CR1} = 2.67 \times 10^{-4}$ and $V_{CR2} = -2.97 \times 10^{-5}$ in the $P+$ implanted poly-resistance, which is also known as the high resistance poly-resistor. Note that the $T_{CR\ell}$ and $V_{CR\ell}$ decay quietly as the order increases. As a result, the second-order $R(T)$ and $R(V)$ models are usually accurate enough for most of the voltage reference circuit design problems.

It should not be surprising to learn that the resistor value has a large variation on R_{sheet} due to geometric variation and large temperature coefficients (T_{CR1} and T_{CR2}). In order to fine tune the values of the resistors to achieve stable resistance for accurate circuit implementation, most circuits employ pairs of resistors, such that it is the ratio between the resistance of the resistor pair that is important, not the absolute resistances of the resistors. In this case, it is the matching of the resistor values that is the most important factor to lower the variation of the circuit performance. Luckily, the integrated resistors naturally match well. Whatever error may have occurred in making one applies to any other fabricated in close proximity. When you make a relatively large device, say ten times the minimum width of the device in the process under consideration, a mismatch of 0.5% or less can usually be achieved. Besides the width, there is another factor known as the "*end-effect*" that accounts for the enlargement of both ends of the resistor to accompany the contacts. Because of the end-effect, you cannot expect resistors of different lengths to match well. To achieve optimum matching, one should only use identical resistors. There are a number of resistor layout techniques to achieve well matched resistor pairs, which include inter-digitization and cross-couple layout techniques (Hastings 2001). An example of the resistor network layout using the inter-digitization technique for resistor pair R_1 and R_2 is shown in Figure 1.22. Instead of drawing two single resistors separately, the inter-digitization technique achieves a better matching result by dividing each resistor into many unit resistors. These unit resistors are inter-digitized to pursue an accurate resistor ratio R_2/R_1.

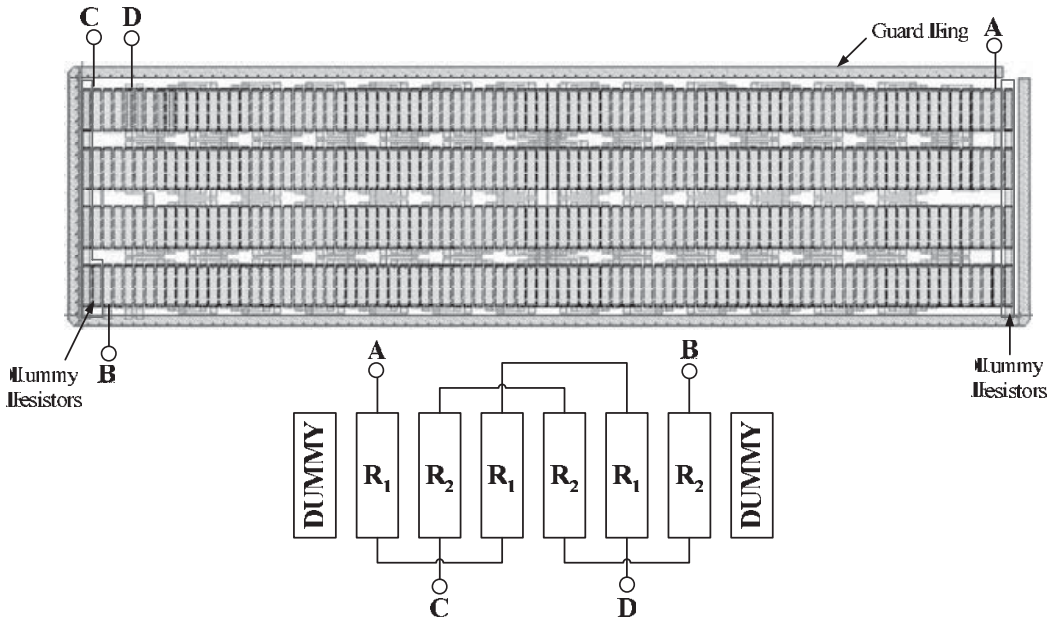


Figure 1.22 Layout example of the resistors R_1 and R_2 of the opamp-based β-multiplier bandgap reference in Figure 3.4 with consideration of the resistor ratio R_2/R_1.

1.4.1 Dummy Element

The amount of dopant diffusion between the inner and outer cells of any device is affected by the relative dopant concentrations between these two regions. It is clear that there will be different dopant diffusion between the unit resistor at the edges of the inter-digitized and the common-centroid layout. Hence this leads to mismatch and is known as the *end-effect* problem. This problem can be alleviated by placing dummy elements on the edge of the resistor layout to compensate the doping concentration difference by ensuring the unit resistors of the matched resistors have the same adjacent structures. Normally, these dummy elements are tied to either the ground or V_{DD} rather than left floating in order to avoid unpleasant electrical characteristics.

1.4.2 Guard Ring

To reduce the impact of substrate noise on the resistors, the resistor network can be surrounded by a guard ring as shown in Figure 1.22. The guard rings are usually connected to the ground or V_{DD} instead of leaving them floating in order to avoid unpleasant electrical characteristics that may affect the circuit.

1.4.3 Sheet Resistance

While the benefits of multiple matched sections inter-digitized layout will be discussed in the next section, we shall first list the sheet resistance and the first order temperature coefficients of various types of integrated resistors for the 0.18 μm mixed signal CMOS process considered throughout this book in Table 1.3.

It can be observed from Table 1.3 that the sheet resistance of the metal resistor is too low, which means it is not good for using in a voltage reference circuit because it will occupy too large a silicon area for any useful resistance. Furthermore, the temperature coefficients of the metal resistor and *N*-well resistor are too high to be applied in the voltage reference circuit. Not only do diffused resistors have high temperature dependency as noted from Table 1.3, they have high voltage dependency as well. Therefore, neither type of diffused resistor is good enough to be used in voltage reference circuit. In conclusion, the non-silicide

Table 1.3 Sheet resistance and temperature coefficients (T_{CR}) of different resistors.

Resistor Type	Sheet Resistance ($\Omega/\square$)	T_{CR} (ppm/°C)
Non-Silicide *N*+ Diffused	56.1	1510
Non-Silicide *P*+ Diffused	114	1410
Non-Silicide *N*+ Poly	290	−1350
Non-Silicide *P*+ Poly	319	−163
N-well	890	2730
High Resistance Poly	1030	−852
Metal	0.078	3600

$P+$ poly-resistor is the most suitable resistor type to be used for temperature and voltage variation robust circuits.

1.5 Device Matching

Device mismatch errors are the differences between two or more device parameters that are desired to be identical. Matching accuracy, to some extent, dominates the performance of the voltage reference circuits. For example, the matching characteristic of the current mirror plays a key role in the β-multiplier circuit which is widely applied in voltage reference circuits. As a result, applying layout techniques to handle mismatch errors has become more important to high performance voltage reference circuit design, because even a small amount of mismatch may easily damage the performance of a precise voltage reference circuit.

In order to design a voltage reference circuit with consideration of the device mismatch problem, some statistical description for parametric variation can be used to (a) estimate the characteristics or statistical distribution for the parameter of interest, and (b) understand or minimize the impact on circuit performance associated with those variations.

1.5.1 Application of Statistics to Circuit Design

The most basic approach to establish a statistical model for parametric variation is to characterize the distribution of the parameter of interest θ over some sample of devices or structures. The details of the physical sources of this variation are not considered; rather the combined set of underlying deterministic (but not understood) as well as random contributions are simply lumped together in a combined "*random*" statistical description. As a result, the simplest approach (although not very accurate as it is highly likely that different parameters are correlated) to make use of the statistical model for circuit design with device parameter random variation is to treat each variation independent, such that the statistical information can be applied to determine a particular device matching technique that can achieve a reference voltage within a given voltage variation margin due to the variation of parameter caused by device mismatch.

Previous studies have shown that the parameters of all devices fabricated by the CMOS process deviate from the nominal values randomly, and this random variation of device parameters can be modeled by a Gaussian random variable. As a result, the standard statistical tools that quantify the variation of parameters, such as the 3σ tolerance where σ is the standard variance of the parameter under consideration, can be applied. Traditionally, a 3σ mismatch of 2% over process and temperature variations is commonly acceptable for a voltage reference circuit. The following section will provide an analytical analysis of the application of putting multiple devices together to alleviate the device matching error due to random variations.

1.5.1.1 Random Variation

Consider the random variation of a device which is composed of unit cells. As a result, the parameter of the unit cell is the integral of the parameter value over the area of the unit cell. Since the area of the unit cell is usually small, the systematic error of the unit cell is negligible

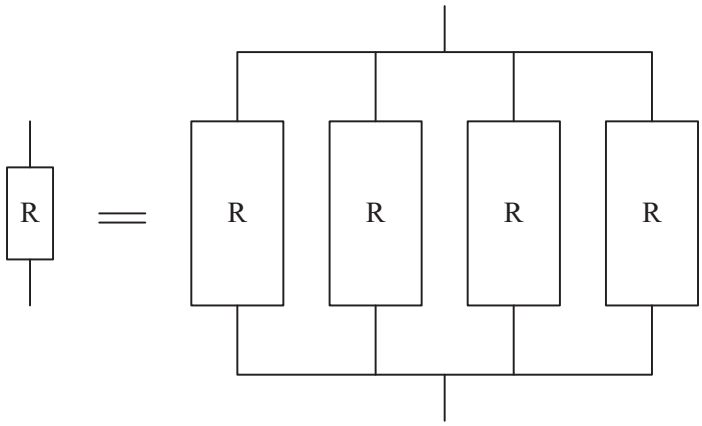


Figure 1.23 Resistors obtained by parallel connections of unit resistors (the size of the resistors drawn in this figure is proportional to the size of the resistors implemented on silicon).

and the parameter of the unit cell can be approximated by the parameter at a particular point in the unit cell plus random variations. Tradeoff can be made between area and matching accuracy. To simplify our discussions, let's consider the case of reducing the resistor value variations by putting together M unit resistors in parallel connection as shown in Figure 1.23 (where $M = 4$ in this example). The resistance of each unit resistor R can be written as $R = R_0(1 + \epsilon)$, where R_0 is the nominal resistance and ϵ is the relative error, which follows the Gaussian distribution ($\epsilon : \mathcal{N}(0, \sigma)$) (Pelgrom *et al.*, 1989). The total resistance of the four unit resistors connected in parallel is given by

$$\begin{aligned} R &= R_0(1+\epsilon_1)//R_0(1+\epsilon_2)//R_0(1+\epsilon_3)//R_0(1+\epsilon_4) \\ &= R_0 \frac{1}{\frac{1}{1+\epsilon_1}+\frac{1}{1+\epsilon_2}+\frac{1}{1+\epsilon_3}+\frac{1}{1+\epsilon_4}} \\ &\approx R_0 \frac{1}{1-\epsilon_1+1-\epsilon_2+1-\epsilon_3+1-\epsilon_4} \\ &\approx \frac{R_0}{4}\left(1+\frac{\epsilon_1+\epsilon_2+\epsilon_3+\epsilon_4}{4}\right), \end{aligned} \tag{1.42}$$

where we assume the variation $\epsilon_k << 1$ with $k = 1, \ldots, 4$. Since ϵ_k are iid Gaussian variables, therefore $\frac{\epsilon_1+\epsilon_2+\epsilon_3+\epsilon_4}{4} : \mathcal{N}(0, \frac{\sqrt{4}\sigma}{4}) = \mathcal{N}(0, \frac{\sigma}{2})$. As a result, by connecting four unit resistors in parallel, the accuracy of the resistor has been doubled. The increased accuracy has been traded for the silicon area, because the effective resistance of the parallel connected unit resistors equals R_0/M. As a result, M set of this parallel unit resistor connections are required to be connected in series to obtain the desired resistance R_0. These serial-parallel connections can be used to obtain the desired effective resistance while improving the accuracy. Actually this structure is similar to doubling both W and L of the resistor, but gives more freedom in layout. This characteristic is also useful for reducing gradient error as will be discussed in next section. The same area matching accuracy tradeoff can be achieved for almost all devices fabricated by

the CMOS process, and is commonly used by circuit designer to overcome design difficulties due to random variation in order to create high performance voltage reference circuits.

1.5.2 Systematic Variation

The systematic variations are process dependent and usually modeled as spatial gradients in device parameters. The magnitude mismatch error due to systematic variation can be compatible to that of random variations (Felt 1994). If the random mismatch is reduced by increasing the area, the systematic mismatch will dominate. Further reduction of the random variation will not achieve a significant reduction in the overall mismatch error, it will only make the systematic variation more significant. Since mismatch due to systematic variation can cause performance degradation, it should be carefully handled and minimized. Special layout techniques can be used to reduce the magnitude of these errors. Figure 1.24 shows the application of a centro-symmetric layout to reduce the systematic variation of a resistor that is being implemented with a serial-parallel connection of four resistors. This centro-symmetric layout can suppress the linear gradient error since it is symmetrical in both horizontal and vertical directions.

In Figure 1.22 another example of a matched layout of two resistors is shown. This layout technique is known as the inter-digit layout method. In this example, the layout is symmetrical along one direction only. As a result, it can suppress linear gradient error that aligns with the symmetrical direction of the unit resistors layout. The best layout of a match resistor pair should apply both centro-symmetric and inter-digit layout technique at the same time, such that inter-digit layout is applied to each *R* of the resistor implemented with centro-symmetric layout in Figure 1.24.

In summary, by dividing the device fabricated by the CMOS process into serial-parallel connections of unit cells, and employing special layout schemes, both the random and gradient

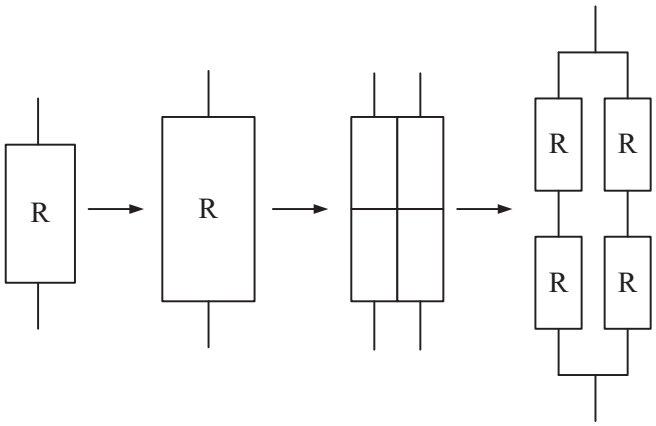


Figure 1.24 Resistor implemented with centro-symmetric layout structure by serial-parallel connection (with 2 resistors in parallel and 2 set of these parallel resistors in series, where the size of the resistors drawn in this figure is proportional to the size of the resistors implemented on silicon).

errors can be minimized, thus the accuracy of the device and hence the performance of the voltage reference circuit can be substantially improved.

1.6 Simulation Models for Circuit Design

The statistical models that characterize the device parameter variations can be incorporated into a circuit simulator which will enable us to obtain accurate circuit performance analysis under various parametric variation assumptions without going through tedious hand calculations. With the help of circuit simulator, a typical design process is shown in Figure 1.25. The simulation result of a typical design with parametric variation is checked against the performance limit under various process variations. The design is robust to process variation if it passes the performance limit test. Otherwise the design parameter is altered according to the failed performance parameter, such as to shift the performance of the typical design, until the designed circuit passes the performance analysis under parametric variations. It may take a few iterations of the above design process to achieve a robust design. This design path has become the *de facto* standard for robust circuit design to combat process variation problems. To enable parametric circuit simulation, the parameter of various devices are measured on a *golden wafer*. Note that the device models in the circuit simulator are simply analytically parameterized models. As an example, the SPICE parameters of the BJT are the model parameters of the physical model developed by Gummel and Poon (Gummel and Poon, 1970). Such model parameters can be extracted from the measurement data of the golden wafer, even though both the measurements under parametric/environmental variations and parametric extraction are very time

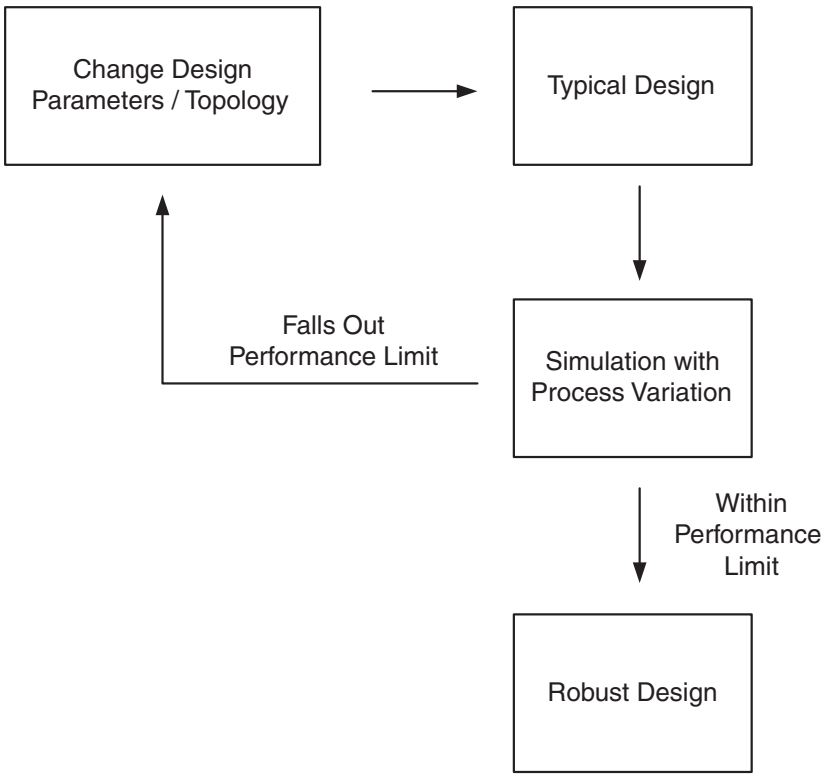


Figure 1.25 Robust design flow with process variation simulations.

consuming. The good news is such measurements and parameter extractions are required to be made only once. After the initial device parameter characterizations, also known as *process characterization*, a small set of important parameters will be selected for monitoring process variations, such a set of parameters will be measured on each fabricated wafer in a process monitor layout, which will be useful for yield analysis, adjustment of the statistical variations of the device models, and process parameter tuning. All the above are currently known as "*process control*" in modern CMOS foundries. The process control will test the parameters monitoring again under predefined process limits; such as the *Pass/Fail* limits to determine if the fabrication process is under control or if something has gone wrong. As an example, typical parameters that are monitored for an MOS transistor during fabrication are

1. oxide thickness
2. effective channel length
3. effective channel width
4. threshold voltage
5. mobility
6. substrate doping
7. sheet resistance.

The first six items in the typical parameter list have a direct effect on the thermal properties of the MOSFET while the last has an effect on the variation of the generated reference voltage on a voltage reference circuit. The following section will present a typical simulator based performance limit analysis.

1.6.1 Process Variation and Typical Design

When a circuit is designed without considering parametric variations, such a design is known as a "*typical*" design. It is highly probable that the performance parameter θ of the typical design will drift away due to the variation of process parameter Γ. In Figure 1.26(a) a typical

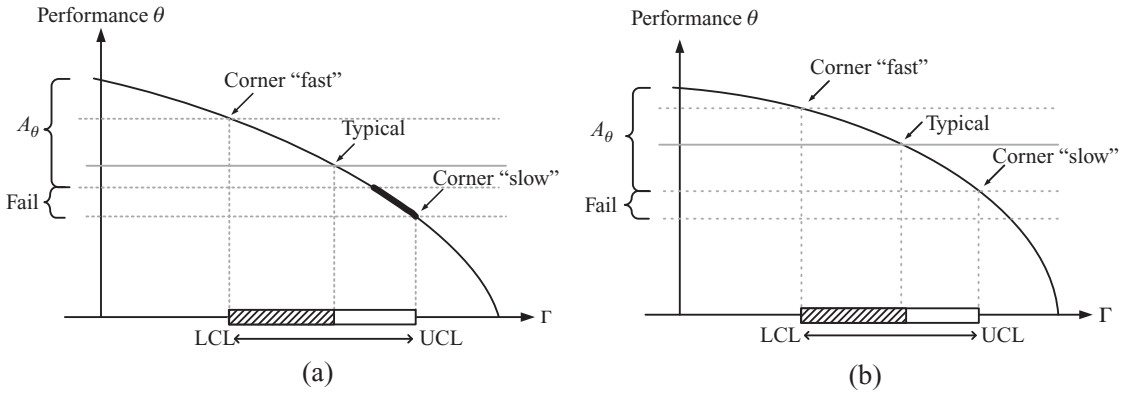


Figure 1.26 The variation of the device parameter θ resulting from process variation of process parameter Γ. (a) shows the process corner without the circuit performance information. (b) shows the process corner with consideration of circuit performance.

case of the drift of performance parameter θ caused by variation of process parameter Γ is shown. In the figure, the range indicated by A_θ is the acceptable circuit performance range for the performance parameter θ under a given quality control requirement. The variation of process parameter Γ under a predefined process control will achieve 3σ within LCL (Lower control limit) and UCL (Upper control limit), otherwise the yield of the fabricated device will be tremendously affected. The induced performance θ due to LCL and UCL are known as the "*fast*" and "*slow*" corners respectively. The drift of performance θ of the typical design is therefore limited to being within the "fast" and "slow" corners. In the case of Figure 1.26(a), it is clear that the UCL will induce a performance θ that lies outside A_θ. As a result, the circuits that are fabricated with a device having process parameter Γ in the slow corner will fail the given quality control requirement. In fact all the fabricated circuits that fall into the fail bin as indicated in Figure 1.26(a) will be unable to pass the quality control. This will have a tremendous effect on the production yield of the fabricated circuit. As a result, the process variation must be considered in the design phase to ensure that the designed circuit will function properly for all the possible process variations (corners).

The process parameter variations at different production levels (i.e., die, wafer, lot, and run) can have a strong impact on the voltage reference circuit performance: output voltage accuracy and temperature coefficient, possibly compromising the production of a precise voltage reference circuit due to a too low yield. To achieve an acceptable yield, the circuit has to be designed with respect to the (LCL,UCL) process variation for assessing expected performance figures. What we are aiming to do is to design a circuit that is robust to the variation of parameter Γ, such that the performance parameter θ induced by both fast and slow corners is within the acceptable range A_θ. As a result, the yield of the fabricated circuit should be better than 3σ theoretically. Ideally, this should be achieved by circuit techniques. However, in the case of wide parametric distribution for the parameter Γ, or when design complexity is under consideration, trimming methods can be applied to achieve a post-fabrication adjustment to improve the yield of the circuit. In this case, any fabricated circuits that do not pass the predefined quality control will be trimmed (on a particular selected devices within the circuit) to adjust the performance of the fabricated circuit with respect to the parameter Γ, such that the performance of the trimmed circuit will be well within the acceptable range A_θ. In other words, the trimming method helps to adjust the (LCL, UCL) spread such that the adjusted spread is well within that induced by A_θ.

Trivially, the overall yield of the voltage reference circuit is affected by both the parameter process variation and local variation (i.e., mismatch). As a result, both effects must be considered during the design phase. In many cases, it is assumed that within-die parameter variations are much lower than die-to-die parameter variations. As a result, the effect of within-die fluctuations are often neglected by voltage reference circuit designers. However, it should be pointed out that the effects of within-die fluctuations increase as the channel length decreases. Since the process parameter variations and mismatches are unavoidable and process dependent, most robust voltage reference circuit designs rely on post-fabrication device trimming to alleviate the problem. In this case, the parametric variation simulation results will help the designer to determine the initial accuracy of the untrimmed voltage reference circuit and determine the number of trimming bits (i.e., trimming fuses) that are required to achieve a given accuracy specification. Section 4.8 will provide a detailed discussion on the application of trimming to improve the yield of voltage reference circuits, while in the following we shall discuss the "*process corner*" that determines the variation extremes of the device parameters.

Table 1.4 Definition of process corner models in SPICE simulator.

Corner	MOSFET	Corner	BJT	Corner	R/C
tm	typical mean	*tm*	typical mean	*tm*	typical mean
wp	fast NMOS, fast PMOS	*hs*	high speed, high β	*wp*	worst power
ws	slow NMOS, slow PMOS	*lb*	low speed, low β	*ws*	worst speed
*wo*1	fast NMOS, slow PMOS	*hb*	low speed, high β		
wz	slow NMOS, fast PMOS				

1.6.2 Process Corners

There are a large number of definitions of process corners in the literature and commercial simulators. Two of the most typical process corners models (Pourchon *et al.*, 2007) are the

1. worst case corner
2. statistical corner.

The popular simulators, such as SPICE and BSIM, make use of the worst case corner model which defines the process corners for various devices as listed in Table 1.4. These process corners are assumed to be independent, and circuits simulated with worst case corner can have devices that are a mix of any of these conditions. As a result, there are a total of $5 \times 4 \times 3 \times 3 = 180$ corner combinations for typical CMOS circuits that are implemented with MOSFETs, BJTs, resistors, and capacitors. Furthermore, the within-die fluctuations are neglected in the worst case corner simulation. No matter the mixture of the device variations, all devices will have a guarantee device performance bounded by these 180 corners. In order to simplify the corner analysis, and to capture the largest range of parameter variation, only slow/fast corners of a specially made corner lot are characterized together with the typical case. The classical slow/fast corner lot of CMOS process is defined with varying *N*-well and *P*-well doping levels, such that higher than normal doping levels are applied in the case of the fast corner, and vice versa lower than normal doping levels are applied to the case of slow corner. Let us consider the case of the threshold voltage of the MOSFET alone. The process corners wo, ws, wp, and wz will define a box with the four corners drawn as gray circles as shown in Figure 1.27. All MOSFETs fabricated by this process will have the threshold voltage bounded inside the box defined by the worst case process corner (also known as the fast/slow corner). As a result, the application of process corner parameter in simulation allows accurate simulation results of the voltage reference circuit under extreme conditions, and thus will obtain the performance variation extremes to be induced by the process variations on the fabricated voltage reference circuit. In other words, the simulation results obtained by SPICE simulations with devices modeled by the worst case process corners will correspond

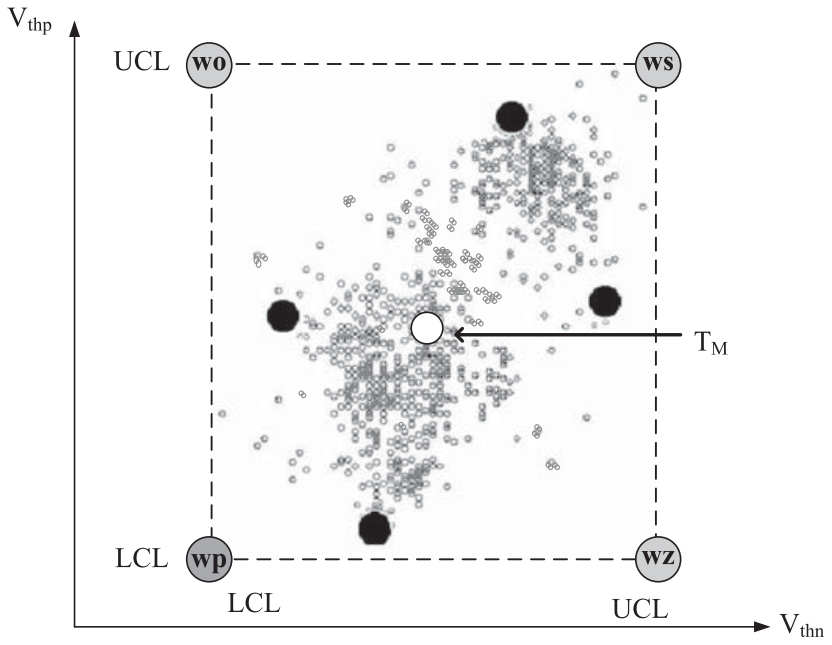


Figure 1.27 Threshold voltage variation of the NMOS and PMOS transistors and the associated process corners.

to the extreme performance, and thus allow us to evaluate the performance and stability of the voltage reference circuits. It is also clear from Figure 1.27 that corners collide with the UCL and LCL will allow us to perform the worst case yield analysis of the fabricated design as discussed in Section 1.6.1.

It is however, the extreme performance analysis that will result in a complicated and expensive (because it occupies a large silicon area) trimming circuit. Reducing the trimming circuit will reduce the yield of the trimmed voltage reference circuits. However, the reduction in yield is usually small for a large reduction of the trimming circuit complexity. This is particularly the case when the worst case corner is far from the statistical corner. As shown in Figure 1.27, a large percentage ("3σ") of the fabricated voltage reference circuits will have the parametric performance of the devices bound within the statistical corners (the quadrilateral with the black dots in Figure 1.27 as the statistical corners of the threshold voltage of the fabricated MOS transistors). Therefore, a better trimming circuit and procedure can be obtained if a design approach based on statistical corners is taken, instead of the worst case corner analysis (Pourchon *et al.*, 2007). Some of the modern simulators do support statistical corner simulations which not only consider parametric variations with statistical importance, but also the dependence of parametric variations between each parameter. However, not all foundries have characterized their technology and process dependent variations and developed a SPICE model to include the effect of statistical corners to enable the circuit designer to enjoy the benefits of statistical corners.

Since not all foundries and simulators support the statistical corner, the rest of the book will use the worst case corner in our analyses. However, readers should understand that the statistical corner can also be applied, and a better circuit may be obtained with statistical corner analysis.

1.7 Noise

Noise is an important factor that limits the performance of electronic circuits. Noise in a CMOS circuit is created by various physical phenomena and is due to the random motion of charge-carrying particles (electronics and holes). The charge-carrying particles are not stationary and move randomly through the lattice of the material even in the presence of an electric field. As a result, noise cannot be represented by a fixed amplitude since the amplitude varies randomly over time. A probability density function (pdf) of a random process is used to describe the probability of the occurrence of each noise amplitude in the random process. Most noise sources can be represented by their mean-square noise voltage given by

$$\overline{V_\eta^2} = E(V_\eta^2(t)), \tag{1.43}$$

where $E(\cdot)$ is the expectation operator and $V_\eta(t)$ is the noise signal. In noise analysis the noise power is usually represented by its power spectral density (PSD). In circuit analysis where the noise at one particular frequency is desired, the center frequency is usually taken as the frequency at which the device operates such as the fundamental frequency of a data signal. The PSD can be calculated over the range of the devices passband to determine the signal-to-noise ratio. The PSD is represented by the unit V^2/Hz, however, it is sometimes more intuitive to show noise as currents and voltages during calculations. In those cases, the square root of the PSD is used with the units of $\mathrm{V}/(\mathrm{Hz})^{1/2}$ or $\mathrm{A}/(\mathrm{Hz})^{1/2}$ which are the root-mean-square (RMS) noise voltage and the noise current respectively. The root-mean-square noise voltage is also equal to the standard deviation of the noise amplitude σ_{V_η}.

This section gives an overview of various sources of noise as well as the effects of different type of noise in circuits. The detailed noise analysis of a special voltage reference circuit, the opamp based β-multiplier bandgap voltage reference circuit, and various circuit techniques that can be applied to minimize the effects of various noise sources in the voltage reference circuit will be presented in Section 4.7.

1.7.1 Types of Noises

Noise in the CMOS circuit is classified in relation to the mechanism of how it is created. The types of noise include thermal noise, shot noise, and flicker noise. Thermal noise is the random motion of electrons due to thermal energy. Shot noise is created at junctions between two materials where an electric field exists. Flicker noise is due to imperfections in the material itself where the charge carriers may get trapped or slowed down. These noise types are explained in details in the following sections.

1.7.1.1 Thermal Noise

Each CMOS device is associated with all three noise sources, and some of them will be the dominant noise sources for each device. The resistors have just thermal noise as the most significant noise property. Thermal noise is created when carriers inside a conductor are "*thermally agitated*" and the random motion creates a random current and potential across the conductor. The amplitude of the noise voltage across the conductor has a Gaussian distribution

and the power spectral density of thermal noise is constant over all frequencies. We can define the mean-square noise voltage and current of a resistor as

$$\overline{V_{\eta_T,R}^2} = 4\,kTR, \qquad \overline{I_{\eta_T,R}^2} = \frac{4kT}{R}, \tag{1.44}$$

where k is the Boltzmann's constant, and R is the resistance. Note that the thermal noise is white noise, therefore, it is the noise bandwidth under consideration that is important, not the actual frequency region. The actual noise power is computed by integrating $\overline{V_{\eta_T,R}^2}$ or $\overline{I_{\eta_T,R}^2}$ in the frequency region under concern, which is equivalent to multiplying the noise bandwidth Δf to $\overline{V_{\eta_T,R}^2}$ and $\overline{I_{\eta_T,R}^2}$. It is clear that the noise power is proportional to temperature in both equations which is consistent with the idea that increasing temperature increases the energy of the carriers and thus increases the random motion.

The thermal noise of a MOSFET is mainly generated from the conducting channel. The noise spectral density of the thermal noise of an NMOS transistor can be modeled as a noise voltage source connected in series with the gate of the MOSFET (Razavi 2001), which is given by

$$\overline{V_{\eta_T,M}^2} = 4kT\gamma\frac{1}{g_m}, \qquad \overline{I_{\eta_T,M}^2} = 4kT\gamma g_m, \tag{1.45}$$

where γ is a process dependent parameter that equals to $\frac{2}{3}$ for MOSFETs with a long channel length. Note that the thermal noise of both resistor and MOSFET can be reduced by reducing the resistance of the devices. In particular, for the MOSFET, we can increase the transconductance to reduce the thermal noise.

The significant noise source in BJT is the thermal noise and shot noise, and a less significant flicker noise at low frequency. The flicker noise will become the dominant noise source at high frequency. The thermal noise of the diode connected BJT can be modeled as the thermal noise of an equivalent resistor, which is given by

$$\overline{V_{\eta_T,Q}^2} = 4\,kTR_Q, \tag{1.46}$$

where R_Q is the resistance between the base and emitter of the diode connected BJT.

1.7.1.2 Shot Noise

Shot noise results from the individual charges passing a potential barrier. In *PN* junctions, shot noise is generated when there is an electric field that forms a potential difference across the depletion regions. In MOSFET, an electric field exists between the gate and the channel of the device, resulting in a leakage current from the gate to the channel. The leakage current is the main source of shot noise and this current is usually very small. For this reason we can usually neglect shot noise during noise analysis.

1.7.1.3 Flicker ($1/f$) Noise

Flicker noise in MOSFETs occurs because of the imperfections in the channel. The charge carriers get trapped by these imperfections making the current fluctuate. The spectral density of the flicker noise decreases with increasing frequency at a rate of $1/f$ and is the greatest at DC. As a result, the higher the DC bias levels, the higher the flicker noise component. The flicker noise is observed to be lower in larger devices because of the larger gate capacitance helps in absorbing the "*fluctuations in the channel charge*." The flicker noise spectral density of a NMOS transistor is given by

$$\overline{V^2_{\eta_{1/f},M}} = \frac{K_n}{C_{ox,n}WLf}, \tag{1.47}$$

where K_n is a process dependent parameter and is a constant, and f is the frequency at which the charge carriers get trapped and released. If a PMOS transistor is under consideration, K_n and $C_{ox,n}$ in Equation 1.47 will be replaced with K_p and $C_{ox,p}$. As can be seen from the equation, a thinner oxide layer at the gate will lead to lower $1/f$ noise similar to the case of large gate area does (the gate area equals to the product WL). It can be observed that at low frequency ($f << 1$), the flicker noise is more significant, while at high frequency ($f >> 1$), the thermal noise becomes the dominate noise source.

1.7.2 Sums and Multiplications of Noises

Noisy signals behave in very different way when compared to their noise free partners. When two noisy DC signals are super-imposed, that is summed, the noise part and the noise free part of the signals have to be considered separately. If the intrinsic noise sources associated with the two signals are uncorrelated, those sources will be RMS summed, while the noise free DC signals will be added linearly. As an example, consider Figure 1.28, where the noisy voltage source is composed of a noise free DC voltage source of 1 V, and a white noise of RMS

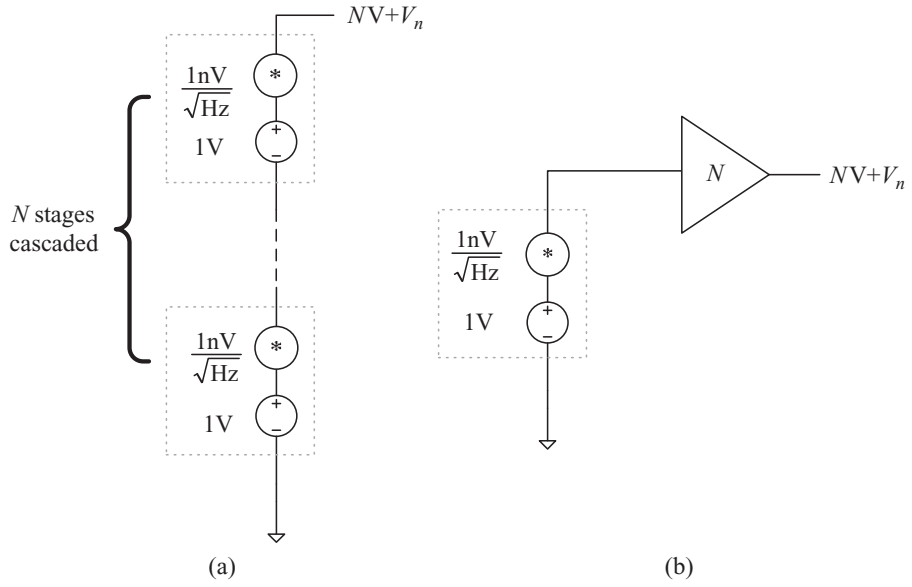


Figure 1.28 (a) Sum of N identical independent noisy signals, (b) multiplication of a noisy signal by a factor of N.

Table 1.5 BJT model parameters.

Parameter	Description	Typical Values
I_S	Transport saturation current	6.50×10^{-19} A
β	Forward current gain	3.4502
R_B	Zero-bias base ohmic resistance	122.98 Ω
R_E	Emitter ohmic resistance	2.16 Ω
R_C	Collector ohmic resistance	17.11 Ω
V_{G0}	Bandgap voltage of silicon at 0 K	1.206 V

voltage 1 nV/(Hz)$^{1/2}$. If we want to obtain a N V voltage from this voltage source, this can be accomplished by duplicating and super-imposing N copies of the voltage sources as shown in Figure 1.28(a); or by feeding the output of the voltage source into a noise free amplifier with gain N as in Figure 1.28(b). If all the N sources are uncorrelated, the output noise voltage in Figure 1.28(a) is given by $V_\eta = \sqrt{N}$ nV/(Hz)$^{1/2}$. While in the case of Figure 1.28(b) where an amplifier with gain N is used, the output noise voltage is given by $V_\eta = N$ nV/(Hz)$^{1/2}$. In reality, it will be impossible to construct a noise free amplifier, and thus the output voltage will be even higher than N nV/(Hz)$^{1/2}$ because of the noise contributed by the noisy amplifier. It is clear that stacking up N sources to obtain a higher voltage generates less output noise than amplifying the signal directly. The problem is the increase in silicon area because of the N copies of the voltage source circuits, where the situation is worse when N is large.

1.8 Fabrication Technology

Our discussions on the CMOS device characteristics conclude with a presentation of the technology parameters used in this book for both analytic computations and SPICE simulations. The technology under consideration with all the designs, analysis, simulations, and layouts is a 0.18 μm CMOS technology, and the BJT, and MOSFET model parameters are summarized in Table 1.5 and Table 1.6, respectively.

Table 1.6 MOSFET model parameters.

		Typical Values	
Parameter	Description	NMOS	PMOS
$V_{th,n}$, $V_{th,p}$	Zero-bias threshold voltage	0.48 V	−0.47 V
$t_{ox,n}$, $t_{ox,p}$	Thickness of gate oxide	3.87×10^{-9} m	3.74×10^{-9} m
μ_n, μ_p	Carrier mobility	3.4×10^{-2} cm^2/ Vs	8.661×10^{-3} cm^2/Vs
$C_{ox,n}$, $C_{ox,p}$	Gate oxide capacitance per unit area	9.04×10^{-15} F	9.36×10^{-15} F

1.9 Book Organization

This book concentrates exclusively on the design and analysis of CMOS voltage reference circuits. It is divided into eight chapters, including this one. A prerequisite for this book is a junior-level course in CMOS analog circuit design. A minimal review of CMOS device physics has been provided in this chapter. Readers should refer to (Hu, 2010) and (Sze, 1969) for an in-depth understanding of the CMOS devices and analog circuit designs.

Chapter 2 presents an introduction of reference voltage performance characterizations commonly encountered in describing voltage reference circuits. The design and analysis of the opamp based β-multiplier bandgap voltage reference circuit that is very suitable and also commonly found in today's integrated circuits fabricated with CMOS technology is presented in Chapter 3. The conditions required to achieve an output reference voltage with near-zero temperature coefficient under the assumptions of ideal devices and environment are discussed.

Note that voltage reference circuits with different properties can be constructed by interconnecting different basic building blocks. Therefore, studying these building blocks will be the first step in the design and analysis of the voltage reference circuits in general. These provide the relations between some pertinent internal variables with the inputs and the building blocks, which in turn provide the key to the design and implementation of high precision and low temperature coefficient voltage reference circuits.

Chapter 4 is devoted to the analysis of the stability, precision, and other performance limitations of the opamp based β-multiplier bandgap voltage reference circuit with various imperfections of the building blocks, and voltage reference circuit topology as a whole. The chapter will discuss building blocks, voltage reference circuit topologies, and design methodologies that help to reduce the reference voltage sensitivity to the respective sources of error. The effect on various process variation problems will also be discussed and possible solutions to alleviate these physical difficulties are presented.

Besides the opamp based β-multiplier bandgap voltage reference circuit discussed in Chapter 3, there are other forms of CMOS voltage reference circuit topologies, and some of the practical topological configurations will be reviewed in Chapter 5. We shall also discuss various sources of error associated with such circuits in real world applications and the possible methodologies to alleviate those problems.

Chapter 6 and 7 discuss advanced voltage reference circuits namely the low voltage and low temperature coefficient voltage reference circuits, respectively. The aspect of designing voltage reference circuits with an output voltage that is lower than 1 V and/or supply voltage lower than 1 V are discussed in Chapter 6. A few important sub-1V voltage reference circuits are reviewed to illustrate the design constraints. The techniques used to overcome those constraints, and their pros and cons will also be presented. Chapter 7 presents the application of high order curvature correction techniques to improve the temperature coefficient and hence the precision of the voltage reference circuit. Following the formal definition of the order of compensation, a number of important high order curvature correction techniques will be discussed.

This book concludes with a discussion of an advance CMOS voltage reference circuit in Chapter 8, where the design and analysis of a special CMOS voltage reference circuit that does not require any resistors in its implementation will be presented. Specifically discussed is the inclusion of a special voltage summing technique to achieve sub-1V reference voltage, a

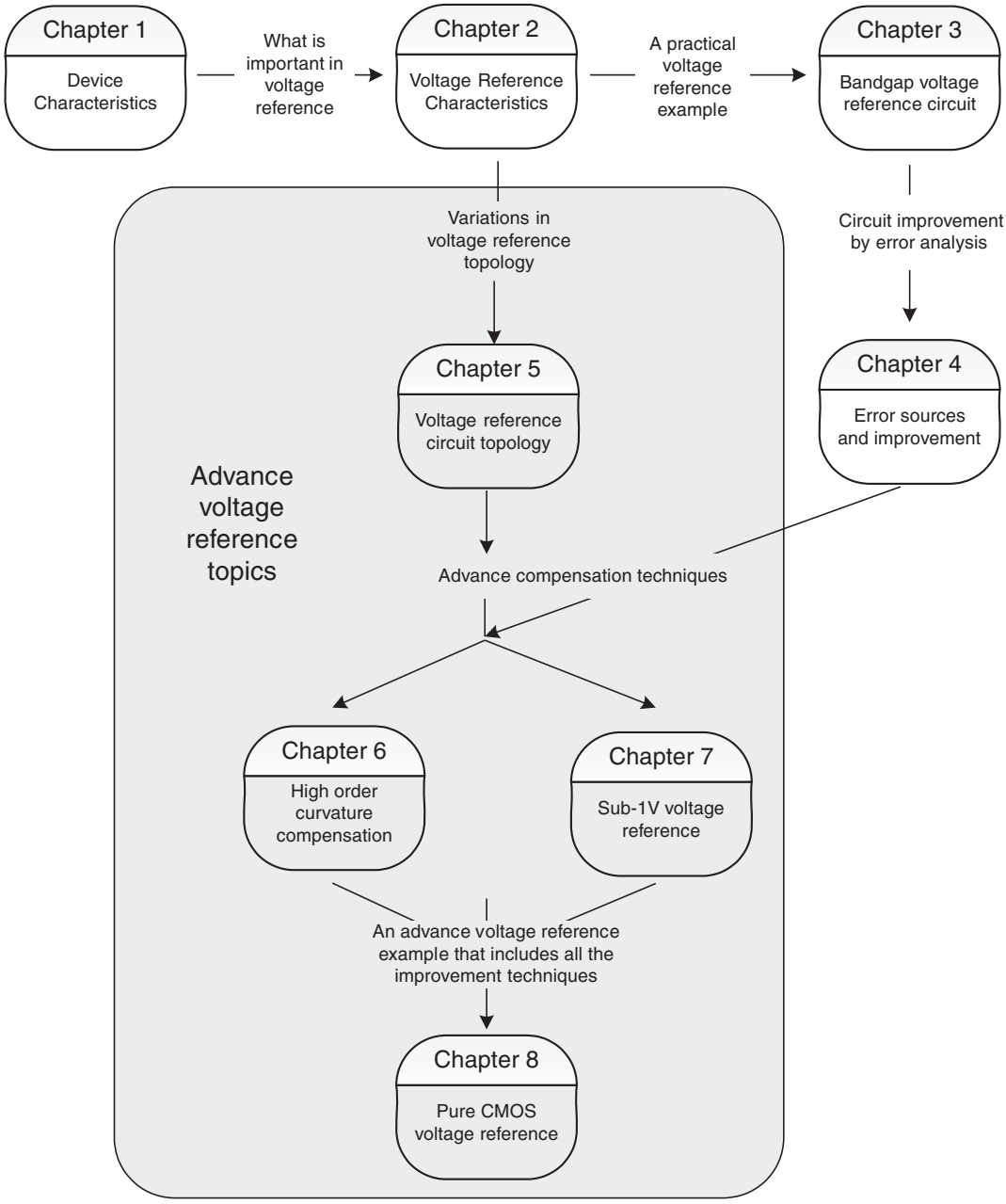


Figure 1.29 Book Organization.

bootstrap biasing technique to improve the power supply rejection ratio, and a piecewise temperature compensation circuit to generate a reference voltage with low temperature coefficient and high temperature stability.

Many topics included in this text can be omitted from class discussions, depending on the coverage required in the course. Figure 1.29 shows the suggested study sequence for each chapter. A useful approach for undergraduate teaching will be to cover the materials in Chapter 1 to 4, which will provide an understanding of the fundamental topics such as the PTAT, CTAT, and bandgap voltage reference circuit, and establish the benefits and applications of circuits with a near-zero temperature coefficient. Chapter 5 to 8 are advanced topics on voltage reference circuits which when combined with Chapter 2 will form a one semester graduate level course.

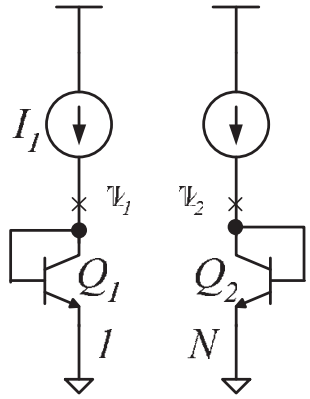


Figure 1.30 Schematic to extract $\Delta V_{BE_{1,2}}$ for Exercise 1.1.

In our experience, students learn more when they are given realistic assignments to practice. To this end we encourage substantial assignments on, for example, the simulation and layout of CMOS voltage reference circuits. This work should be designed to demonstrate and reinforce the techniques taught. It is important that students actually participate in, as well as attend, lectures.

1.10 Exercises

Exercise 1.1 *Showing in Figure 1.30, the emitter area ratio of the bipolar transistors Q_1 and Q_2 is 1 to N. Assume the bipolar transistors have the same reverse saturation current. Extract $\Delta V_{BE_{1,2}} = V_{BE_1} - V_{BE_2}$ by inserting a resistor R_1.*

Exercise 1.2 *Showing in Figure 1.31 shows the emitter area ratio of the bipolar transistors Q_1 and Q_2 is 1 to N. Assume the bipolar transistors have the same reverse saturation current. Find the current, I, and the voltage, V_R, across the resistor R_1.*

Exercise 1.3 A simple bandgap voltage reference circuit*: Consider the circuit in Figure 1.32, we have*

$$V_{REF} = V_{BE} + M\Delta V_{BE_{1,2}}. \tag{1.48}$$

Consider the V_T extraction circuit in Figure 1.3, which extracts V_T from $\Delta V_{BE_{1,2}}$ as in Equation 1.12

1. *Rewrite V_{REF} using Equation* 1.7*,* 1.12*, and* 1.48*.*
2. *Obtain the temperature dependency of V_{REF} by partially differentiating V_{REF} with T.*
3. *Derive M that achieves V_{REF} with zero temperature dependency at $T = T_r$, and derive the associated V_{REF}.*
4. *Derive the numeric value of V_{REF} with $\theta = 1$ and $T_r = 300$* K.

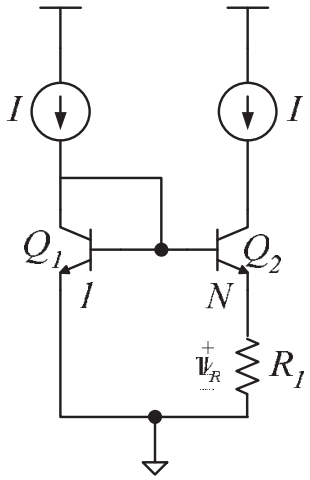


Figure 1.31 Schematic to extract $\Delta V_{BE_{1,2}}$ with BJTs arranged as a current mirror for Exercise 1.2.

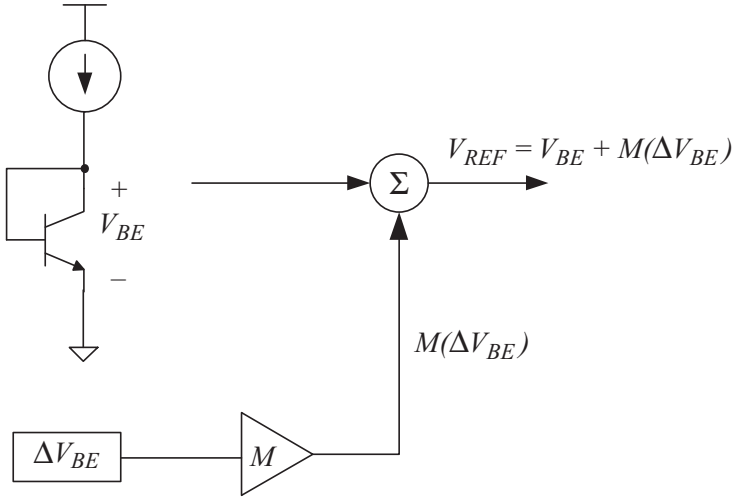


Figure 1.32 A simple bandgap voltage reference circuit for Exercise 1.3.

Exercise 1.4 *Consider the PMOS transistor in Figure 1.33 where* $\mu_p C_{ox,p} = 250\ \mu\text{A/V}^2$, $W = 10\ \mu\text{m}$, $L = 10\ \mu\text{m}$, *and* $V_{th,p} = -0.6\ \text{V}$. *Neglecting the channel length modulation effect, find* V_G.

Exercise 1.5 *Consider a NMOS transistor with* $\mu_n C_{ox,n} = 100\ \mu\text{A/V}^2$, $V_{th,n} = 0.7\ \text{V}$, *and* $\lambda = 0.01\text{V}^{-1}$. *If* $V_{GS} = 0.9\ \text{V}$, *and* $V_{DS} = 1\ \text{V}$, *find the proper* W/L *ratio required for a drain current of* 0.1 mA.

Exercise 1.6 *Assume* $|V_{th,p}| = 0.7\ \text{V}$, *and* $\mu_p C_{ox,p}(W/L) = 1\ \text{mA/V}^2$. *Find the drain current for each of the circuits in Figure 1.34.*

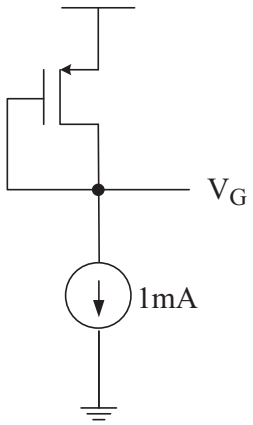


Figure 1.33
Finding the operating point of PMOS transistor for Exercise 1.4.

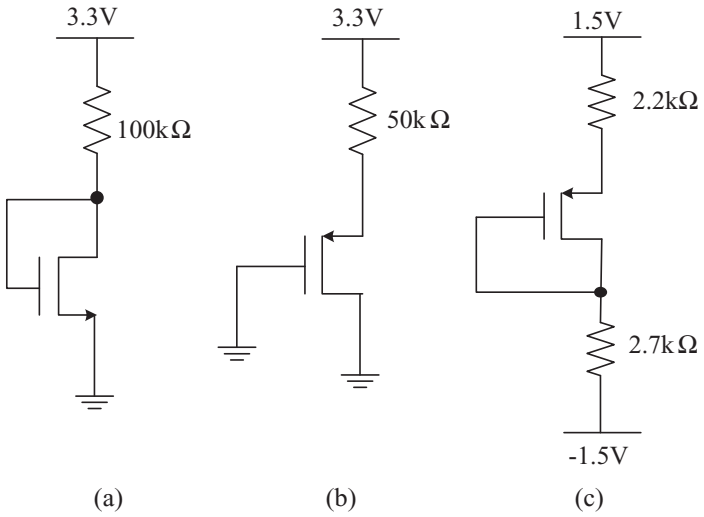


Figure 1.34 Finding the operating point of the transistors under different biasing conditions for Exercise 1.6.

Exercise 1.7 *Assume* $V_{th,n} = 0.7$ V, $\mu_n C_{ox,n} = 100\ \mu\text{A/V}^2$. *Find the values of the* W/L *ratio for each of the transistors in the circuit in Figure 1.35 required to achieve* $V_A = 2$ V *and* $V_B = 1$ V.

Exercise 1.8 *Assume* $V_{th,n} = 0.7$ V *and* $\mu_n C_{ox,n}(W/L) = 1\ \text{mA/V}^2$ *for each of the transistors used in Figure 1.36.*

1. *Find the operating point* (I_D, V_{DS}) *for* M_1 *in each of the circuits with* $V_{DD} = 5$ V.
2. *Reduce the power supply voltage by* 10% *and repeat part 1.*
3. *Calculate the sensitivity of* I_D *to* V_{DD} *in each of the circuits.*

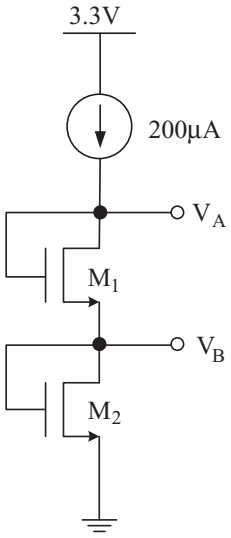


Figure 1.35
Finding the operating condition of NMOS transistors arranged in cascode structure for Exercise 1.7.

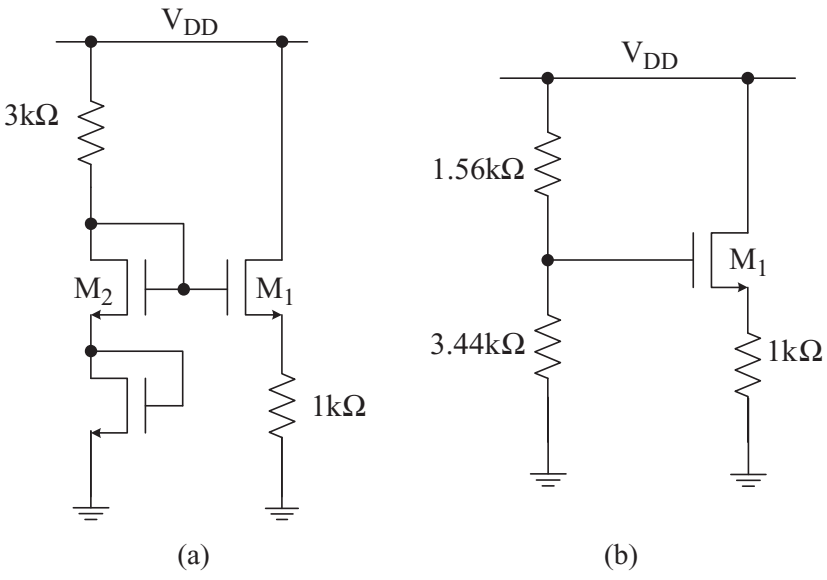


Figure 1.36 Finding the effect of V_{DD} variations on NMOS transistor with simple biasing circuit and active biasing circuit for Exercise 1.8.

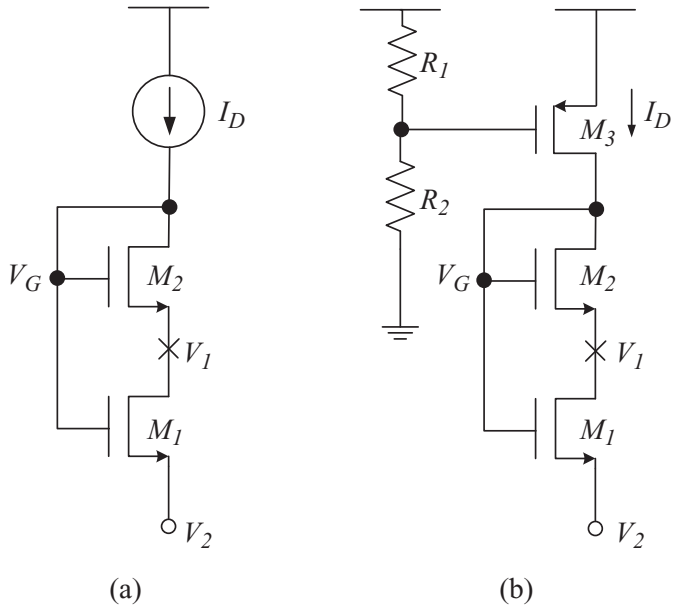


Figure 1.37 PTAT voltage generation by $\Delta V_{GS,\,sub}$ (a) with ideal current source I_D and (b) current source made up with M_3 at strong inversion for Exercise 1.10.

Exercise 1.9 *Compute $\Delta V_{GS,sub_{1,2}}$ in the circuit shown in Figure 1.9, with $S_1 \neq S_2$ operating in subthreshold mode.*

Exercise 1.10 *V_{PTAT} voltage generation:*

1. *Compute $\Delta V_{GS,sub_{1,2}}$ in the circuit shown in Figure 1.37(a) with I_D properly chosen to bias both NMOS transistors operating in subthreshold mode.*
2. *Consider the circuit with the current source made with PMOS M_3 biased on strong inversion as shown in Figure 1.37(b). Derive the minimum V_{DD} required to operate the circuit.*
3. *Simulation of the circuit in Figure 1.37(b) with a selected R_1 and R_2 that satisfy (1) and (2).*
   a. *Plot the simulation result of V_1 against T.*
   b. *Comment on the shape of the obtained curve when compared to what was expected to be obtained from the ideal circuit, and state the physical reason for this deviation.*

Exercise 1.11 *Estimate the minimum and maximum resistances of an N-well resistor with a nominal resistance of* 10 kΩ *at room temperature (*27 °C*) over a temperature range of (*0, 100 °C*).*

References

Felt, E. (1994) Measurement and modeling of MOS transistor current mismatch in analog IC's. *Proceedings of the IEEE/ACM International Conference on Computer-Aided Design*, pp. 272–7.

Giustolisi, G., Palumbo, G., Criscione, M. *et al.* (2003) A low-voltage low-power voltage reference based on subthreshold MOSFETs. *IEEE Journal of Solid-State Circuits*, **38** (1), 151–4.

Gummel, H. and Poon, H. (1970) An integral charge control models of bipolar transistors. *Bell Systems Technical Journal*, **49**, 827–52.

Hastings, A. (2001) *The Art of Analog Layout*. Prentice Hall.

Hu, C.C. (2010) *Modern Semiconductor Devices for Integrated Circuits*. Prentice Hall.

Johns, D.A. and Martin, K. (1997) *Analog Integrated Circuit Design*. Wiley & Sons.

Liu, W. (2001) *MOSFET Models for SPICE Simulation including BSIM3v3 and BSIM4*. John Wiley & Sons.

Massobrio, G. and Antognetti, P. (1993) *Semiconductor Device Modeling with SPICE*, 2nd edn. McGraw-Hill.

Pelgrom, M.J.M., Duinmaijer, A.C.J. and Welbers, A.P.G. (1989) Matching properties of MOS transistors. *IEEE Journal of Solid-State Circuits*, **24**, 1433–9.

Pourchon, F., Beckrich-Ros, H., Raya, C. *et al.* (2007) High accuracy temperature bipolar modeling for demanding bandgap application. *IEEE Bipolar/BiCMOS Circuits and Technology Meeting* pp. 180–83.

Razavi, B. (2001) *Design of Analog CMOS Integrated Circuits*. McGraw Hill.

Shichman, H. and Hodges, D.A. (1968) Modeling and simulation of insulated-gate field-effect transistor switching circuits. *IEEE Journal of Solid State Circuits*, **SC-3**, 285–9.

Sze, S.M. (1969) *Physics of Semiconductor Devices*. Wiley.

HSPICE® Simulation and Analysis User Guide 2006.

Tsividis, Y.P. (1980) Accurate analysis of temperature effects in $i_c - v_{BE}$ characteristics with application to bandgap reference sources. *IEEE Journal of Solid-State Circuits*, **15** (6), 1076–84.

Vittoz, E.A. and Neyroud, O. (1979) A low-voltage CMOS bandgap reference. *IEEE Journal of Solid-State Circuits*, **14** (3), 573–9.

Yu, G.G. and Geiger, R.L. (1994) An accurate and matching-free threshold voltage extraction scheme for mos transistors. *IEEE International Symposium on Circuits and Systems*, pp. 115–18.

2

Voltage Reference

A voltage reference circuit is a device that generates an exact output voltage which in theory does not depend on the operating voltage, load current, temperature, or the passage of time. Readers should not mistake voltage regulators for voltage reference circuits even though they are very similar, as both circuits generate regulated output voltages that are immune to the change in load current, input voltage, temperature, etc. A voltage regulator, however, is intended to provide a higher output current than that of a voltage reference circuit. As a result, the voltage regulator is much less accurate than a voltage reference circuit, the output noise is higher, and the long term stability is not specified. In fact, every voltage regulator requires a precise voltage reference circuit in its core.

Besides the voltage regulators, voltage reference circuits are used in all circuits that require a precise voltage for measurements to be made against. The accuracy of any measurement can be regarded as good as it is able to be compared against a known standard. High resolution A/D and D/A converters, digital meters, smart sensors, threshold detectors, servo systems, battery management systems, and many other precise industrial control systems require precise voltage reference circuits in their cores. Various circuits have been developed to provide accurate reference voltages, whereas their performance can be characterized by the objective measures detailed in the following sections. These objective measures not only allow us to specify the voltage reference circuits that have been implemented or are to be designed, they can also allow a fair and objective comparison between two voltage reference circuits.

2.1 Performance Measures

A variety of circuits require a fixed reference voltage to be compared to for the sake of reliability and accuracy. As an example, the A/D converter requires a stable reference voltage to achieve high conversion accuracy, which is independent of the supply voltage. A precise reference voltage is not only a temperature compensated voltage source but also a transiently stable circuit, where the output is impervious to sudden variations in supply voltage, load, noise, and manufacturing process. Therefore, the reference voltage circuits should have high static and dynamic performances. The static performance of a voltage reference circuit is

CMOS Voltage References: An Analytical and Practical Perspective, First Edition. Chi-Wah Kok and Wing-Shan Tam.
 Published 2013 by John Wiley & Sons Singapore Pte. Ltd.

affected by the limited line regulation, load regulation, process and manufacturing variations on the electron device characteristics and values, electron device mismatches, variation on electron device temperature coefficient, package shift effect, channel-length modulation, etc. The static performance influences the absolute accuracy of the output voltage, which can be improved through trimming of individual circuit components using techniques such as fusible links and laser trimming (Erdi, 1975; Huijsing *et al.*, 1996) etc. To simplify our discussions on the dynamic performance of the voltage reference circuit, we shall consider the nominal output voltage, known as $V_{REF(nom)}$, which is the desired voltage at nominal operating conditions. We assume that this output voltage is obtained through trimming techniques, where the nominal operating condition is regarded as the room temperature with a specified supply voltage known as the nominal input/supply voltage $V_{DD(nom)}$. The output voltage variations over the full range of operating conditions are considered, which is regarded as the dynamic performance. In general, the dynamic performance of the voltage reference circuit is dominated by four factors: (i) the temperature coefficient (TC) of the voltage reference circuit over the operating temperature range, (ii) the line regulation of the voltage reference circuit over the operating input voltage range, (iii) the power supply rejection ratio ($PSRR$) under maximum input ripple, and (iv) the peak-to-peak output noise of the voltage reference circuit over the operating frequency spectrum. Under nominal operating temperature conditions, the relative error caused by limited $PSRR$ is normally smaller than that caused by the intrinsic peak-to-peak output noise and the line regulation of the voltage reference circuit. When the operating temperature variation is limited, the temperature coefficient of the voltage reference circuit will usually become the dominant factor, which limits the dynamic performance of the reference voltage. The sensitivity parameter, or its *de facto* acronym, will be used throughout this book. The following sections will provide formal definitions of each of the voltage reference circuit performance measures using the sensitivity parameter $\mathcal{S}_x^y$ that measures the sensitivity of the parameter y with respect to a change in parameter x as defined by (Allen and Holberg, 2003)

$$\mathcal{S}_x^y = \frac{\lim}{\Delta x \to 0} \left\{ \frac{\Delta y / y}{\Delta x / x} \right\} = \frac{\partial y}{\partial x} \frac{x}{y}, \tag{2.1}$$

where Δx and Δy are the change in parameter y due to the change in parameter x with respect to the nominal values of x and y. For simplicity, a modified sensitivity measure $\mathcal{S}_y$ is used instead of the above conventional definition in some of the selected performance parameters in the rest of the book. Consider the case of defining the line regulation using Equation 2.1, where y is the output reference voltage and x is the supply voltage. It can be observed that $\mathcal{S}_x^y$ has a linear factor x. In other words, $\mathcal{S}_x^y$ will reward voltage reference circuits operating at low nominal supply voltage. In this case, it will be difficult to compare the performance of one voltage reference circuit to another. As a result, in some special cases of the sensitivity measure of the performance parameters for a voltage reference circuit, researchers and engineers in this field use the modified sensitivity measure, as will be defined for each performance measure in later sections to avoid unfair comparison. At the same time, in order to simplify our discussions and without loss of generality, we have chosen a specific set of nominal operation parameters as summarized in Table 2.1. All the voltage reference circuits will be characterized under the listed nominal conditions unless specified otherwise.

Table 2.1 Nominal condition for voltage reference circuit characterization.

Parameters	Symbol	Values
Nominal Supply Voltage	$V_{IN(nom)}$	1.8 V
Nominal Temperature	$T_{(nom)}$	Room Temperature (i.e., 300 K or 25 °C)

2.1.1 Line Regulation

The line regulation $\mathcal{S}_{LR,T(nom)}$ specifies the variation of the output of the voltage reference circuit $\Delta V_{REF,T(nom)}$ with respect to the input voltage variation ΔV_{IN} at the nominal temperature. Formally, line regulation is specified as μV/V or % of the following voltage ratio

$$\mathcal{S}_{LR,T(nom)} = \frac{\Delta V_{REF,T(nom)}(\Delta V_{IN})}{\Delta V_{IN}} (\mu\text{V/V}) \text{ [or } \times 100(\%)], \tag{2.2}$$

where $\Delta V_{REF,T(nom)}(\Delta V_{IN})$ is the variation of the reference voltage measured within the input voltage variation in the range of $[V_{IN(min)}, V_{IN(max)}]$, and $\Delta V_{IN} = V_{IN(max)} - V_{IN(min)}$. Note that in everyday application, the input supply voltage range is not required to be $V_{IN(nom)} \pm \frac{\Delta V_{IN}}{2}$, as will be elaborated in a sequel. Therefore, it is more desirable to specify $[V_{IN(min)}, V_{IN(max)}]$ instead. Figure 2.1 shows the test-bench used to measure the line regulation of a voltage reference circuit. The steady-state output current, output capacitive load, and output resistive load of the voltage reference circuit are enumerated as I_{OUT}, C_{LOAD}, and R_{LOAD}, respectively, where $I_{OUT} = V_{REF(nom)}/R_{LOAD}$. Note that the line regulation factor can be affected by I_{OUT} and C_{LOAD}. As a result, the measured line regulation should be specified together with the measurement environment which includes the operating temperature, C_{LOAD} and I_{OUT} or R_{LOAD}. The output voltage of the voltage reference circuit, $V_{REF,T(nom)}$, is measured with V_{IN} increased from 0 V to $V_{IN(max)}$ under nominal temperature $T_{(nom)}$ at a chosen C_{LOAD} and I_{OUT}. A typical waveform for $V_{REF,T(nom)}$ against V_{IN} is shown in Figure 2.2. Similar to all other engineering problems, the desired reference voltage is specified with some tolerance to reflect the inaccuracy in the real world. The output voltage of a voltage reference circuit is specified as $V_{REF(nom)} \pm \frac{\Delta V_{REF}}{2}$ at $T_{(nom)}$. As shown in Figure 2.2, the input voltage range that corresponds to such an output voltage range is specified as $[V_{IN(min)}, V_{IN(max)}]$. The input voltage variation is thus given by

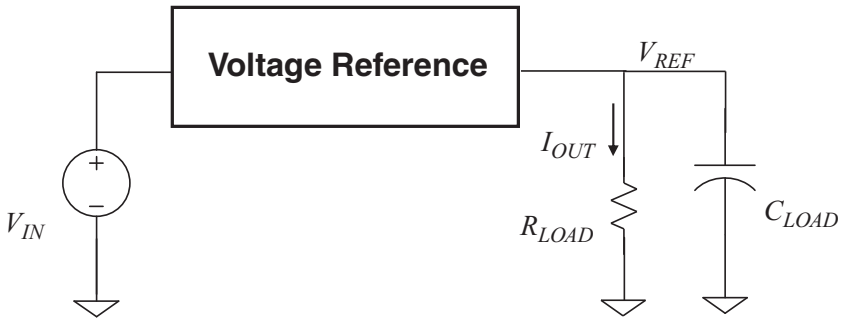


Figure 2.1 Test-bench of voltage reference circuit for line regulation and temperature coefficient measurement.

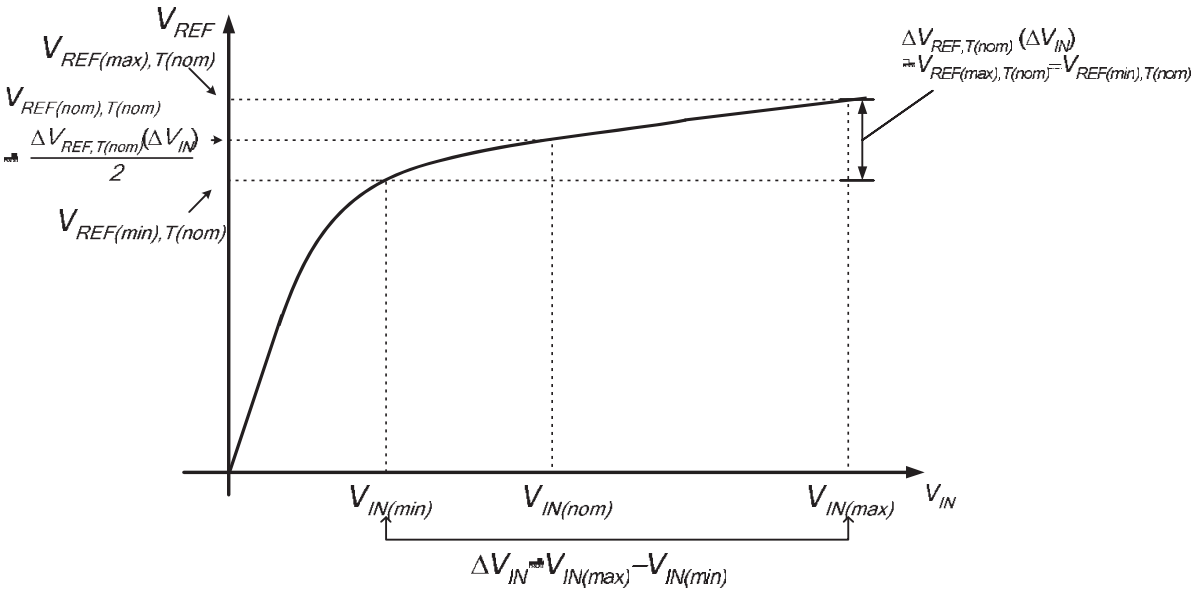


Figure 2.2 A typical waveform of V_{REF} measured from voltage reference circuit against using V_{IN} at $T_{(nom)}$ for the computation of line regulation.

$\Delta V_{IN} = V_{IN(max)} - V_{IN(min)}$. It is clear that the operating range of V_{IN} will affect the line regulation, therefore the operating range of V_{IN} should be specified during the line regulation measurement. The parameter $V_{IN(min)}$ denotes the minimum operating voltage of the voltage reference circuit. In particular, the parameter V_{DROP} specifies the dropout voltage of the voltage reference circuit, which is defined to be the difference between the input to output voltage of the voltage reference circuit. In particular, $V_{DROP(min)}$ is defined as the difference between the desired reference voltage $V_{REF(nom)}$ and $V_{IN(min)}$ (i.e., $V_{DROP(min)} = V_{IN(min)} - V_{REF(nom)}$). In some literature, $V_{DROP(min)}$ is used to specify the minimum operating voltage of the given voltage reference circuit, with a given $V_{REF(nom)}$. Another interesting property of the minimum dropout voltage is that a lower $V_{DROP(min)}$ helps to promote the power efficiency of the voltage reference circuit, as well as extending the operating voltage range, and hence prolongs the system life time for system driven by a limited power source. However, low dropout voltage also implies greater design complexity as will be discussed in later chapters. This design paradox is one of the obstacles for engineers to overcome to achieve a high performance voltage reference circuit. Let us address this fact once again. While $V_{REF(nom)} = \frac{\Delta V_{REF,T(nom)}(\Delta V_{IN})}{2}$, the reader should not get confused with $V_{IN(nom)}$, which does not necessarily equal $\frac{\Delta V_{IN}}{2}$ (i.e., it is possible that $V_{IN(nom)} \neq \frac{\Delta V_{IN}}{2}$). In other words, given $V_{IN(nom)}$, ΔV_{IN} and $V_{REF(nom)}$ do not tell you $V_{DROP(min)}$. You also need to know $V_{REF(nom)}$, $V_{IN(min)}$, and $V_{IN(max)}$ to obtain $V_{DROP(min)}$.

2.1.1.1 SPICE Setup

SPICE simulation is a powerful tool for circuit designers to verify the correctness and also the performance of a voltage reference circuit in the design phase. In particular, we have discussed in Section 1.6 that it is possible to apply SPICE to analyse the limiting performance of the

voltage reference circuit. The SPICE netlist 'ref.sp' of the voltage reference circuit is listed in Appendix B, which is applied in this section and subsequent sections to discuss how to set up the test-bench in SPICE for simulator based performance evaluation. Let's first take a look of the SPICE input file for the test-bench of the line regulation as shown in Figure 2.1. Before we move further to the details of the SPICE input file, we shall assume the reader has experience in using SPICE to simulate a circuit. Otherwise readers can go to other textbooks (Vladimirescu, 1994) to become familiar with the SPICE simulation tool.

Listing 2.1 SPICE input file for the characterization of line regulation of a voltage reference circuit.

```
* SPICE Input File for the Simulation of Line Regulation
.INCLUDE 'book.mdl'
.INCLUDE 'ref.sp'

VIN 1 0 DC 1.8
IBIAS 2 0 DC 20U
X1 2 1 VREF 0 REFCIR
RLOAD VREF 0 1MEG
CLOAD VREF 0 24F

.DC VIN 0 3 0.1
.PROBE DC V(RLOAD)
.END
```

The SPICE input file for simulating the line regulation of a voltage reference circuit is shown in Listing 2.1. The input file, also known as netlist, implements the circuit shown in the line regulation test-bench (see Figure 2.1), in which the voltage reference circuit 'REFCIR' is stored in the file 'ref.sp'. The process model used in this book is described in the technology model file 'book.mdl' listed in Appendix A, which contains the model parameters of a 0.18 μm CMOS technology. The contents of the files are listed in the appendices of this book. These two files are included for simulation with command .INCLUDE. The voltage reference circuit REFCIR is denoted as X1 with the pin assignment given by <bias input output ground>, where bias is the input current that biases the internal circuit of REFCIR, input is the supply voltage of the voltage reference circuit, output is the reference voltage generated by REFCIR, and ground is the supply ground input of the voltage reference circuit. The voltage reference circuit X1 is biased with IBIAS which is specified as a 20 μA constant current source in the SPICE script in Listing 2.1. A DC supply voltage 'VIN' at nominal voltage 1.8 V as defined in the SPICE script is coupled to the input of the voltage reference circuit. A resistive load 'RLOAD' and a capacitive load 'CLOAD' are coupled to the voltage reference circuit at the output of the voltage reference circuit. To simplify our discussions, the output node of the voltage reference circuit is denoted as VREF. A DC analysis, taking the supply voltage as the changing variable from 0 V to 3 V in a step of 0.1 V is performed according to the control statement '.DC VIN 0 3 0.1'. The plot of V_{REF} as a function of V_{IN} can be obtained from the data logged by the output control statement '.PROBE DC V(RLOAD)' as the V_{REF} builds up at the positive terminal of R_{LOAD}. Note that if I_{OUT} is under

investigation instead of V_{REF}, the output control statement can be modified to `'.PROBE DC I1(RLOAD)'`, where I_{OUT} is the current flow into the positive terminal of R_{LOAD}.

2.1.2 Temperature Coefficient

As discussed in Chapter 1, the physical characteristics of the circuit components vary with the operating temperature, and thus create a temperature dependent output of the voltage reference circuit. The temperature sensitivity of the circuit, $\mathcal{S}_{TC}$, also known as the temperature coefficient (TC), specifies the reference voltage drift over a given range of operating temperature $[T_{min}, T_{max}]$ with $V_{IN} = V_{IN(nom)}$. The parameter $\mathcal{S}_{TC}$ is defined as

$$TC = \mathcal{S}_{TC,V_{IN(nom)}} = \frac{\left(V_{REF(max),V_{IN(nom)}} - V_{REF(min),V_{IN(nom)}}\right)}{(T_{max} - T_{min}) \times V_{REF(nom)}} \times 10^6 \ (\text{ppm}/^\circ\text{C})$$

$$= \frac{\Delta V_{REF,V_{IN(nom)}}(\Delta T)}{\Delta T \times V_{REF(nom)}} \times 10^6 \ (\text{ppm}/^\circ\text{C}), \tag{2.3}$$

where $\Delta V_{REF,V_{IN(nom)}}(\Delta T)$ is the variation of the reference voltage within the temperature range $[T_{min}, T_{max}]$, and $\Delta T = T_{max} - T_{min}$ as specified on a typical waveform shown in Figure 2.3. This waveform can be obtained by the same test-bench used for the measurement of line regulation (see Figure 2.1) with V_{IN} fixed to be $V_{IN(nom)}$ and varying the operating temperature over $[T_{min}, T_{max}]$. The temperature variation is usually accomplished through putting the test chip into a hot/cold bath or inside an environmental chamber while all other

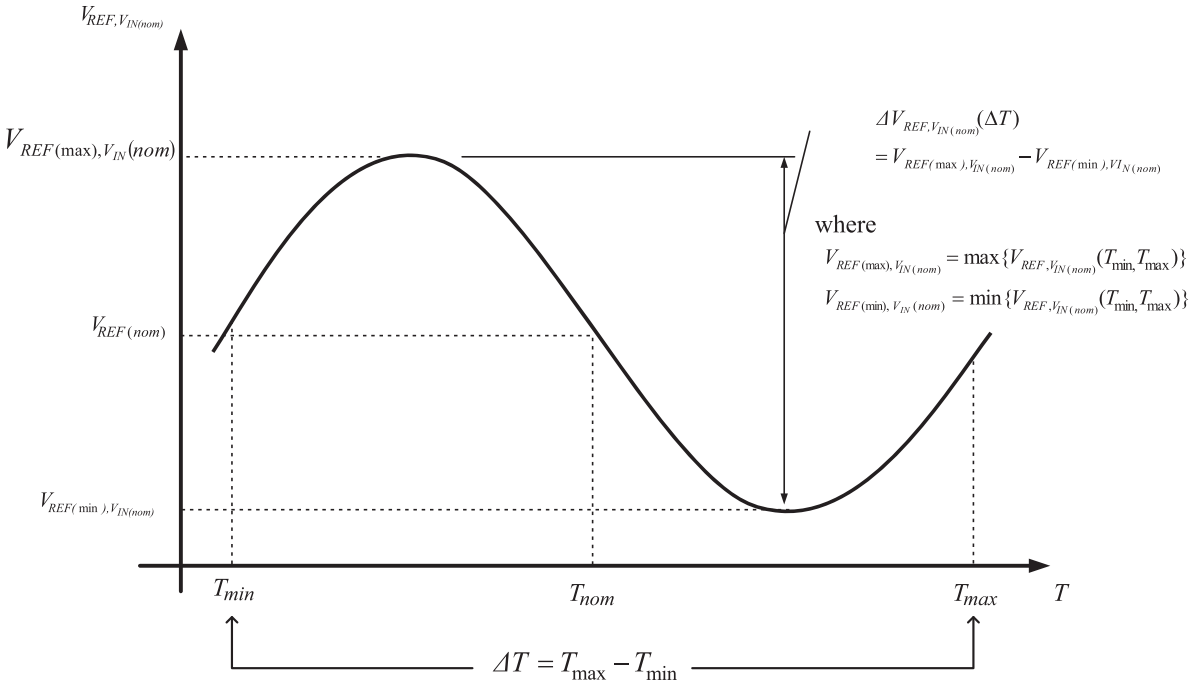


Figure 2.3 A typical waveform of temperature coefficient (TC) of the voltage reference under nominal input voltage ($V_{IN(nom)}$).

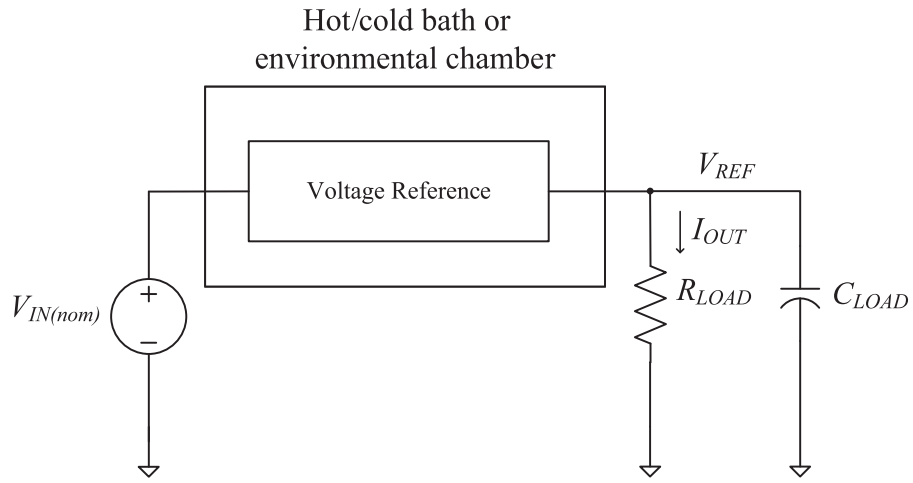


Figure 2.4 Hot/cold bath or environmental chamber.

input and output sources are maintained in the nominal environment as shown in Figure 2.4. The $V_{REF,V_{IN(nom)}}$ is being measured under the specified C_{LOAD} and R_{LOAD} over the pre-defined temperature range. The parameters, $V_{REF(max)}$, $V_{IN(nom)}$, $V_{REF(min)}$, and $\Delta V_{REF,V_{IN(nom)}}$, in Equation 2.3 can be obtained from the same measurement results with the specified operating temperature range. Hence, $\mathcal{S}_{TC}$ can be computed accordingly. Note that the $\mathcal{S}_{TC}$ varies with the variation in the operating temperature range.

As observed from Figure 2.3, the temperature dependency of most voltage reference circuits are high order functions of the operating temperature T. The consequence of the high order curvature implies that the $\mathcal{S}_{TC}$ can sometimes be misleading, since it can be made to look better by making the allowable temperature range smaller and centering it right at the point where $V_{REF,V_{IN(nom)}}(T)$ equals the average between $V_{REF(min),V_{IN(nom)}}$ and $V_{REF(max),V_{IN(nom)}}$. Since there are many different standard ranges that specify the practical operating temperature range, it will be difficult if not impossible to accurately compare these values unless the temperature ranges over which the references are measured are known *a priori.*

It is important to choose the temperature range suitable for the specific application to compute $\mathcal{S}_{TC}$. On the other hand, a small $\mathcal{S}_{TC}$ can always be obtained by choosing the smallest T_{min} and the largest T_{max} such that

$$V_{REF(max),V_{IN(nom)}} = V_{REF(nom)} + \frac{\Delta V_{REF,V_{IN(nom)}}(\Delta T)}{2}, \tag{2.4}$$

$$V_{REF(min),V_{IN(nom)}} = V_{REF(nom)} - \frac{\Delta V_{REF,V_{IN(nom)}}(\Delta T)}{2}. \tag{2.5}$$

Note that if we alter $V_{REF(nom)}$ to maximize the operating temperature range $[T_{min}, T_{max}]$ with a given $\Delta V_{REF,V_{IN(nom)}}$, the altered $V_{REF(nom)}$ will also affect the $\mathcal{S}_{LR}$, and all other performance parameters. Therefore, it is not that simple to alter the $\mathcal{S}_{TC}$ by changing a single design parameter, as all performance parameters are inter-related.

The $\mathcal{S}_{TC}$ required by different applications can range from a few parts per million per degree Celsius (ppm/°C) to hundreds of ppm/°C. The variation of the reference voltage over the operating temperature range will directly affect the accuracy of a system. For example, a N-bit

analog-to-digital converter that requires a reference voltage $V_{REF(nom)}$ under a temperature span ΔT would have a conversion accuracy ΔV_N that requires

$$\Delta V_N = \frac{V_{REF(nom)}}{2^{N+1}} \tag{2.6}$$

$$= \frac{\Delta V_{REF,V_{IN(nom)}}(\Delta T)}{\mathcal{S}_{TC} \times \Delta T} \frac{1}{2^{N+1}}, \tag{2.7}$$

where we assume the voltage reference circuit achieves the optimal S_{TC} with

$$V_{REF(nom)} = \frac{1}{2}\left[V_{REF(max),V_{IN(nom)}} - V_{REF(min),V_{IN(nom)}}\right]. \tag{2.8}$$

This illustrates the stringent requirements placed on the design of the voltage reference circuit for applications with a wide operating temperature range. Last but not least, after so many years of voltage reference circuit developments and applications, it has been customary for the engineer to use the acronym *TC* in place of $\mathcal{S}_{TC}$. The rest of the book will use both terms *TC* and $\mathcal{S}_{TC}$ interchangeably.

2.1.2.1 SPICE Setup

Listing 2.2 shows the SPICE input file for the simulation of the temperature coefficient of a voltage reference circuit, which implements the test-bench shown in Figure 2.4. Similar to the simulation of line regulation, a DC analysis is performed, and the environment parameter `TEMP` will be the changing variable and is given by the control statement `'.DC TEMP -40 125 165'` in place of the `'.DC VIN'` statement. This simulation script will obtain the reference voltage at different temperatures from −40 °C to 125 °C in 165 steps (i.e., one measurement per degree Celsius). A plot of the V_{REF} as a function of temperature can be obtained by further processing the simulation result captured by `'V(RLOAD)'`.

2.1.3 Power Supply Rejection Ratio

In real world implementation, the power rail on the silicon is corrupted by the high frequency noise due to signal coupling, feedback, power surge, and so on. The ability of the voltage reference circuit to reject the noise and other spurious signals at a particular frequency on the power rail, and to provide a stable reference voltage, is specified as the power supply rejection ratio ($PSRR$). The $PSRR$ is a function of frequency expressed in dB with the following definition

$$PSRR(f) = \mathcal{S}_{PSRR,f} = 20\log\frac{V_{REF,AC}(f)}{V_{IN,AC}(f)}(\text{dB}), \tag{2.9}$$

Listing 2.2 SPICE input file for the characterization of temperature coefficient of a voltage reference circuit.

```
* SPICE Input File For The
* Simulation of Temperature Coefficient
.INCLUDE 'book.mdl'
.INCLUDE 'ref.sp'

VIN 1 0 DC 1.8
IBIAS 2 0 DC 20U
X1 2 1 VREF 0 REFCIR
RLOAD VREF 0 1MEG
CLOAD VREF 0 24F

.DC TEMP -40 125 165
.PROBE DC V(RLOAD)
.END
```

where the power supply being corrupted with spurious noise at a particular frequency f is modeled as a DC voltage coupled with a sinusoidal signal at frequency f, and labeled as $V_{IN,AC}(f)$. As a result, $V_{IN} = V_{IN,AC} + V_{IN(nom)}$. The output voltage $V_{REF}(f)$ is an AC coupled reference voltage measured at the output of the voltage reference circuit, such that $V_{REF}(f) = V_{REF(nom)} + V_{REF,AC}(f)$. The $PSRR$ over a wide frequency range can be applied to describe the variation of the reference voltage corrupted by supply noise. The $PSRR$ can be measured with the test-bench in Figure 2.5. Similar to other test-benches being used to measure the line regulation and temperature coefficient, both I_{OUT} and C_{LOAD} have to be specified in the test-bench to measure $PSRR$. The amplitude of the AC signal $V_{IN,AC}(f)$ is usually chosen to be 1 V peak-to-peak, which is denoted as 1 V_{pp}, even though other amplitudes can also be

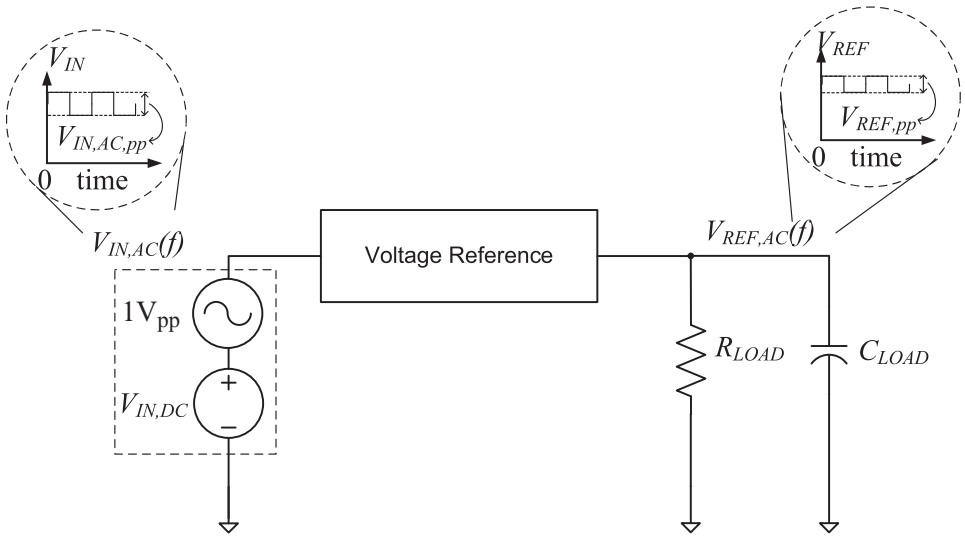


Figure 2.5 Test-bench of voltage reference circuit for power supply rejection ratio ($PSRR$) measurement.

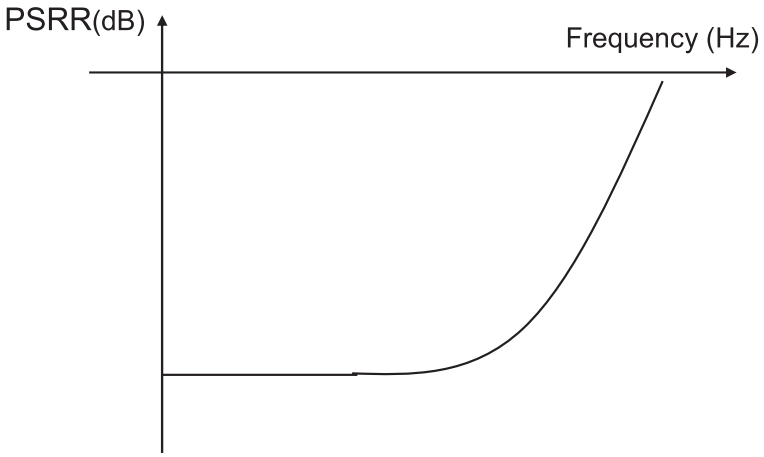


Figure 2.6 A typical waveform of power supply rejection ratio ($PSRR$) of the voltage reference circuit.

chosen, the 1 V_{pp} signal helps to simplify the extraction of $PSRR$ from the measurement result, because $PSRR(f) = 20\log V_{REF,AC}(f)$ in the case of $V_{IN,AC}(f) = 1$ V_{pp}. The $PSRR(f)$ can be computed from the measured $V_{REF}(f)$ with a frequency varying AC voltage source. Figure 2.6 shows a typical $PSRR$ waveform of a voltage reference circuit. The $PSRR(f)$ is lowpass shaped because of the limited frequency response of the CMOS devices used to implement the voltage reference circuit. A 1 kHz sinusoidal signal, $V_{IN,AC}(1000)$, is usually used in most specifications due to its popularity in both audio signals and control systems.

2.1.3.1 SPICE Setup

Listing 2.3 shows the SPICE input file for the simulation of the $PSRR$ of the voltage reference circuit. An AC source with amplitude of 1V is added onto the original input voltage source `'VIN'` to imitate the power supply noise, where the AC signal will be presented at the input voltage within the frequency range to be simulated. To simulate the $PSRR$ performance of the voltage reference circuit subject to input noise at different frequencies, AC analysis is performed as defined by the control statement `'.AC DEC 50 10 100MEG'`, which specifies the simulated frequency range spans from 10 Hz to 100 MHz, and a set of simulation results will be obtained with 50 data points per decade in the simulated frequency range. As mentioned, the $PSRR(f) = 20\log V_{REF,AC}(f)$ in the case of $V_{IN,AC}(f) = 1$ V_{pp}, therefore, the $PSRR$ is a function of frequency and can be plotted by the control statement `'.PROBE AC VDB(VREF)'` to allow an immediate result visualization.

Listing 2.3 SPICE input file for the characterization of the power supply rejection ratio of a voltage reference circuit.

```
* SPICE Input File For The
* Simulation of Power Supply Rejection Ratio
.INCLUDE 'book.mdl'
.INCLUDE 'ref.sp'
```

```
VIN 1 0 DC 1.8 AC 1
IBIAS 2 0 DC 20U
X1 2 1 VREF 0 REFCIR
RLOAD VREF 0 1MEG
CLOAD VREF 0 24F

.AC DEC 50 10 100MEG
.PROBE AC VDB(VREF)
.END
```

2.1.4 Quiescent Current

The quiescent current, I_q, also known as the supply current, is the current required to operate the voltage reference circuit at steady-state with no resistive load. In nominal condition, the quiescent current equals $I_{q(nom)}$ under $V_{IN(nom)}$ and $T_{(nom)}$ with $R_{LOAD} = \infty$ such that I_{LOAD} equals 0. As a result, $V_{IN(nom)} \times I_{q(nom)}$ is the steady-state power consumption of the reference circuit under nominal conditions. A voltage reference circuit with a low quiescent current is desirable for two reasons. First, a low quiescent current implies high power efficiency, and long working hours of the voltage reference circuit for applications with limited supply power, such as battery operated devices. Second, a low quiescent current voltage reference circuit has small power dissipation and hence a small self-heating effect which helps to maintain the accuracy and stability of the output voltage of the voltage reference circuit. The test-bench showing in Figure 2.7 measures $I_{q(nom)}$ as the current flows into the voltage reference circuit with supply voltage $V_{IN(nom)}$ at nominal temperature $T_{(nom)}$ and a capacitive load C_{LOAD} connected to V_{REF}. It should be noted that the value of I_q varies with V_{IN}, operating temperature T, and capacitive load C_{LOAD}. Therefore, I_q should be specified with respect to V_{IN}, T, and C_{LOAD}.

2.1.4.1 SPICE Setup

As aforementioned, the quiescent current equals $I_{q(nom)}$ under $V_{IN(nom)}$ and $T_{(nom)}$ with $R_{LOAD} = \infty$ such that I_{LOAD} equals 0. Thefore, the loading resistor `'RLOAD'` is removed in the SPICE

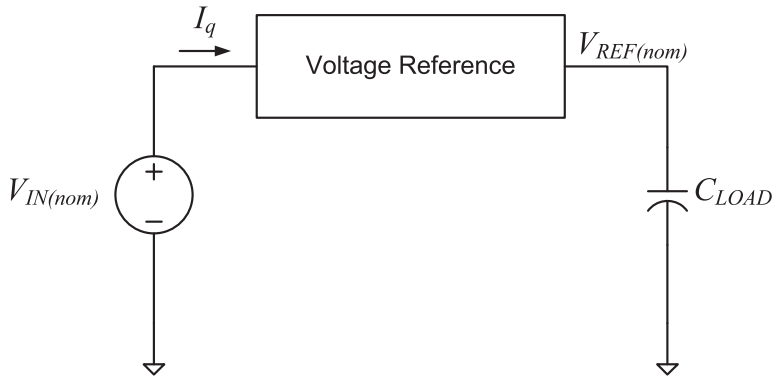


Figure 2.7 Test-bench of voltage reference circuit for quiescent current (I_q) measurement.

script listed in Listing 2.4, which is consistent with the test-bench shown in Figure 2.7. The input voltage is defined at the nominal condition of 1.8 V. A transient analysis is performed to simulate the quiescent current in steady state defined by the statement `'.TRAN 10U 300U'`. The quiescent current can be observed from the plotted $I_{q(nom)}$ current against time which is obtained by the control statement `'.PROBE TRAN I2(X1)'`.

Listing 2.4 SPICE input file for the characterization of the quiescent current of a voltage reference circuit.

```
* SPICE Input File For The
* Simulation of Quiescent Current
.INCLUDE 'book.mdl'
.INCLUDE 'ref.sp'

VIN 1 0 DC 1.8
IBIAS 2 0 DC 20U
X1 2 1 VREF 0 REFCIR
CLOAD VREF 0 24F

.TRAN 10U 300U
.PLOT TRAN I2(X1)
.END
```

2.1.5 Output Noise

Another frequency dependent performance parameter of the voltage reference circuit is the output noise. The output noise of a voltage reference circuit is generally specified as the peak-to-peak voltage in the $0.1 \sim 10$ Hz bandwidth which is useful for low frequency systems such as voltage regulators. The output noise can also be specified in a higher frequency bandwidth such as 10 Hz to 20 kHz. This type of specification is useful for noise in the broadband region which is also known as "*white noise*" or thermal noise. Applications that require such broadband noise consideration include A/D and D/A converters. Similar to the device noise discussed in Section 1.7, the output noise of the voltage reference circuit is measured with respect to its root mean square (RMS) value. Assuming the noise is truly random, the peak-to-peak noise voltage can be estimated by multiplying the RMS value by 6. For example, a voltage reference with 2 μV_{RMS} at 10 Hz to 20 kHz noise density will have a peak-to-peak noise voltage of approximately 12 μV.

In reality, the best way to specify high frequency noise is to show a graph of noise voltage spectral density versus frequency in $nV/\sqrt{Hz}$ as discussed in Section 1.7. This allows the design engineer to calculate the reference noise based on the desired bandwidth of their system. Consider the RMS noise voltage spectral density requirement of an analog-to-digital converter with N-bit. The noise density $V_{\eta,REF}(f)$ in $(V/\sqrt{Hz})$ has a peak-to-peak noise

voltage of $6V_{\eta,REF}\sqrt{BW}$, where BW is the system bandwidth. The peak-to-peak noise voltage is required to be smaller than half of the conversion voltage step size, and thus

$$V_{\eta,REF} < \frac{1}{2}\frac{V_{REF(nom)}}{(2^N \times 6 \times \sqrt{BW})}. \tag{2.10}$$

For example, a 12 bit analog-to-digital converter with $V_{REF(nom)} = 5$ V operating in an audio bandwidth of 100 Hz to 20 kHz would require

$$\begin{aligned} V_{\eta,REF} &< 5/(12 \times 2^{12} \times \sqrt{20\text{ kHz} - 100\text{ Hz}}) \\ &< 720\text{ nV}/\sqrt{\text{Hz}}. \end{aligned} \tag{2.11}$$

A typical noise measurement requires a bandpass filter to extract the noise spectrum in a desired bandwidth. Figure 2.8 shows a typical test-bench for the noise measurement of a voltage reference circuit. The output of the voltage reference circuit is bandpass filtered by cascading a highpass filter with a lowpass filter. An example of a 2 decade bandpass filter with bandwidth 10 Hz $\sim$ 1 kHz constructed with a 1 pole highpass filter and a 2 pole lowpass filter is shown in Figure 2.9, where Chebyshev filters are used because of its sharp transition. Note that the filter should be designed with respect to the input impedance of your measurement equipment. The schematic presented in Figure 2.8 is for reference only. Of course the most accurate measurement is to use a spectrum analyzer or noise analyzer to extract the output voltage noise power in a specified frequency band. However, for most applications, a simple $L - C$ filter can get the job done well.

In order to reduce the output noise of the voltage reference circuit, a simple $R - C$ filter can be applied to reduce the noise to an acceptable limit required by the system resolution and

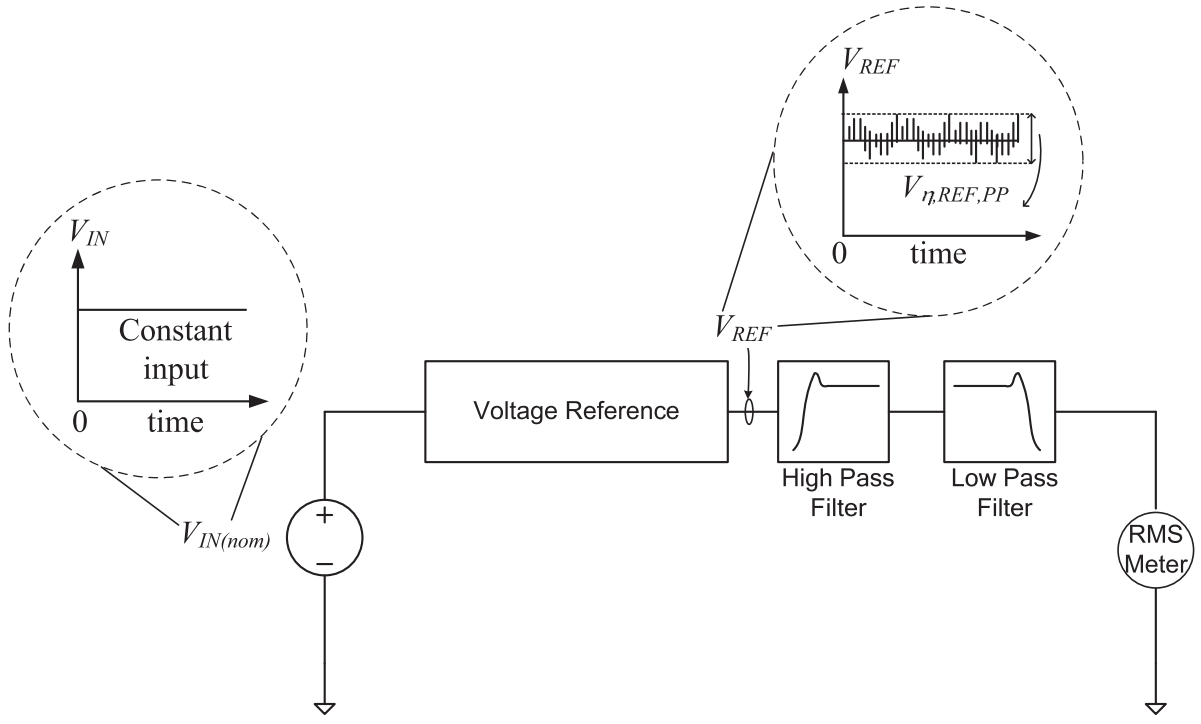


Figure 2.8 Test-bench of voltage reference circuit for noise measurement.

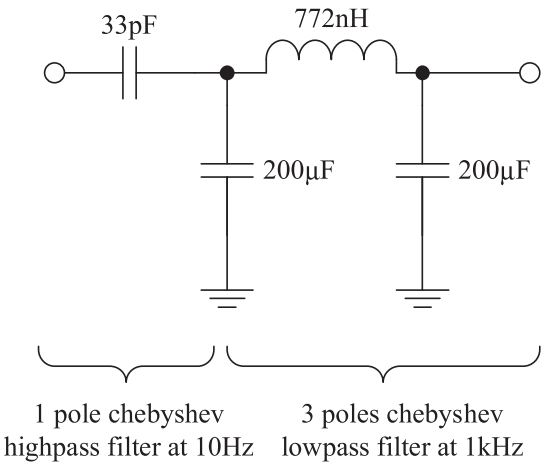


Figure 2.9 A bandpass filter for the measurement of low frequency noise with a bandwidth of 10 Hz $\sim$ 1 kHz.

accuracy. The wideband output noise in the 10 kHz to 1 MHz band can be reduced to about 50 μV_{pp} using a 0.001 μF capacitor at the output of the voltage reference circuit. Noise in the 1 kHz to 100 kHz band can be further reduced using a 0.1 μF capacitor on the output. However, most of the voltage reference circuits are constructed with low output drive capability which suffers from instability problems when driving a large capacitive load. As a result, a design paradox between system noise and stability results. The designer is thus required to determine the best compromise between these two factors to achieve the best voltage reference circuit performance.

2.2 Other Design Considerations

Besides the obvious design consideration that we've discussed for each performance parameter presented in previous sections, there are other design considerations in a voltage reference circuit that are important and that at the same time also affect the above performance parameters. Among these are

1. circuit size
2. power dissipation
3. device mismatch
4. ease of output trimming.

The designer will have to consider the above design parameters in order to fit the designed voltage reference circuit into the bigger picture of the final product. In particular the circuit size and power dissipation are related design constraints because of their importance to the market value of the final product. At the same time, they are also important for the output noise of the voltage reference circuit. Note that the intrinsic thermal noise is inversely dependent on the square root of the quiescent current and the total component size, while $1/f$ noise is inversely proportional to the sum of the square root of the gate area of the MOSFETs in the

circuit. Previous design experience tells us that when the opamp based β-multiplier bandgap voltage reference circuit to be presented in Chapter 3 is implemented with 0.5 μm technology with an area of 0.01 mm^2 and a quiescent current of 4 μA, it generates approximately 30 μV RMS output noise over the frequency range of DC to 10 kHz. If one were willing to apply brute force techniques to reduce white noise and $1/f$ noise by an order of magnitude, the circuit would require a quiescent current of 4 mA and an area of 1 mm^2. Clearly, these area and current requirements would be unacceptably large for an integrated circuit. Over the last decade, a feasible low noise voltage reference circuit for practical implementation has had a size limitation of 0.02 mm^2 and a less than 100 μA quiescent current. Recently, the design requirement has been tightened to 0.005 mm^2 circuit area and less than 1 μA quiescent current.

As discussed in Chapter 1, all devices are subject to process variations, which will induce parameter variation and device mismatch problems. Even though circuit trimming can be applied to alleviate the process variation problem, the device mismatch and circuit trimming must be considered in the voltage reference circuit design. A good voltage reference circuit should be relatively insensitive to device mismatches and effective in achieving the desired operating point through device parameter trimming. Device matching in integrated circuit technologies in general and voltage reference circuits in particular has been introduced in Chapter 1 and investigated in depth in (Allen and Holberg, 2003). The more important question in the design of a high performance voltage reference circuit is how does the topology of the circuit affect the circuit's sensitivity to component mismatches, and the accuracy of the trimmed nominal output voltage. Ideally, the circuit should have a broad trimming range such that very small changes in a trimming resistor (for example) do not drastically alter the output voltage and temperature coefficient of the circuit. The analysis in Section 3.2.1 will show that not all components in the opamp based β-multiplier bandgap voltage reference circuit have the same V_{REF} sensitivity. As a result, the voltage reference circuit topology must be chosen carefully, such that most of the circuit components have low V_{REF} sensitivity, while those with high sensitivity can be trimmed with an implementable trimming network. Last but not least, the trimming network usually takes up a large silicon area. As a result, it not only increases the manufacturing cost because of the added trimming step in the post-fabrication process of the voltage reference circuit, it also increases the intrinsic silicon cost. Furthermore, the larger the silicon size of the trimming network, the higher the noise injected into the voltage reference circuit from the trimming network, and thus the more degraded the performance of the voltage reference circuit.

The above design dilemma cannot be resolved with engineering decisions alone, the marketing decision that determines the final product price will also contribute in deciding the chip size and other performance parameters of the voltage reference circuit, and thus the final voltage reference circuit design.

2.3 Summary

A precise voltage reference circuit is extremely important for many applications. The performance of the voltage reference circuit can be characterized by a set of parameters, and the desirable design parameters are listed in Table 2.2, which will be used throughout this book to aid our discussions. Also listed in Table 2.2 are the implications for the performance of the voltage reference circuit when each individual parameter varies. The above design parameters

Table 2.2 A summary of the desirable design parameters of the voltage reference circuit.

Parameters	Desirable Values	Pros	Cons
$\mathcal{S}_{LR}$	$\downarrow$	less susceptible to supply voltage variation	complex design; large silicon area; difficult to work with low supply voltage
$\mathcal{S}_{TC}$	$\downarrow$	less susceptible to temperature variation	complex design; large silicon area requires high order temperature compensation
$\mathcal{S}_{PSRR}$	$\uparrow$	less susceptible to supply voltage high frequency noise	complex design; large silicon area
I_q	$\downarrow$	more power efficient	low output drive; more susceptible to stability problem; may not work well with large $\mathcal{S}_{PSRR}$
$V_{IN(nom)}$	$\downarrow$	more suitable for low voltage application; work well with low I_q; more power efficient	low voltage device operation; more susceptible to stability problem; may not work well with large $\mathcal{S}_{PSRR}$
V_{DROP}	$\downarrow$	more suitable for low voltage application; works well with low $V_{IN(nom)}$	complex design; large silicon area
$V_{\eta,REF}$	$\downarrow$	more accurate reference output	requires more power to drive the filtering circuits

are also applicable to temperature and voltage insensitive circuits with current output, where the observation on V_{REF} would be replaced by I_{REF}.

Among all the above performance parameters, the line regulation and the temperature coefficient are the most important for a wide variety of applications. The line regulation of the voltage reference circuit can be improved by better circuit topology, such as self-biased, thus achieving high supply voltage variation immunity. We can also make better use of the semiconductor device's supply voltage independent physical characteristics, such as the silicon bandgap voltage, threshold voltage of the MOSFET, and so on, to create a stable reference voltage that is insensitive to supply voltage variation. The temperature coefficient can be minimized by the mutual compensation between the PTAT and CTAT factors of the voltage reference circuit. In the next chapter, we shall discuss a well known voltage reference circuit known as the opamp-based β-multiplier bandgap voltage reference circuit, which makes use of the mutual compensation of PTAT and a CTAT voltages to generate a near-zero *TC* reference voltage equals to the silicon bandgap voltage. Our discussions are based on a silicon proven example. All the basic building blocks of the opamp based β-multiplier bandgap voltage reference circuit will be reviewed analytically in detail and the rationale of their layout structures will also be reviewed. The physical constraints and error sources of the opamp based β-multiplier bandgap voltage reference circuit will be discussed in Chapter 4. Then we shall discuss various kinds of advanced voltage reference circuits in subsequent chapters.

To assist readers in designing their own voltage reference circuits, SPICE simulation scripts for simulation based performance analysis have been discussed in this chapter. Modern foundries have accurate SPICE model files for us to obtain accurate simulations under nominal operating conditions. The reader should also perform the corner analysis to understand the performance limitation of the voltage reference circuits in the design phase, such that appropriate circuit techniques, such as trimming circuit or even change of circuit topology, can be adopted to design appropriate voltage reference circuits for their own applications.

2.4 Exercises

Exercise 2.1 *Determine the required $PSRR$ of a voltage reference circuit with $V_{REF(nom)} =$ 5V applied to a 12 bit ADC with a maximum peak-to-peak V_{DD} variation of 10 mV in the frequency range under consideration.*

Exercise 2.2 *Calculate the operating hours of a voltage reference circuit with $V_{REF(nom)} =$ 3V, $I_q = 1$ mA and $V_{DROP} = 200$ mV powered by a 5V battery with 100 mAh.*

Exercise 2.3 *Figure 2.10 shows a modified Widlar bandgap voltage reference circuit.*

1. *Simulate this circuit using the test-bench as shown in Figure 2.1 by DC sweep of the input voltage, V_{IN}, to obtain the waveform of V_{REF} as a function of V_{IN} as shown in Figure 2.11. Derive the line regulation.*
2. *Simulate the circuit using the test-bench as shown in Figure 2.1 by DC sweep of the temperature from $-40\,^{\circ}$C to $125\,^{\circ}$C to obtain the waveform of V_{REF} as a function of temperature under $V_{IN(nom)}$ and $V_{REF(nom)}$ as shown in Figure 2.12. Derive the temperature coefficient (TC).*

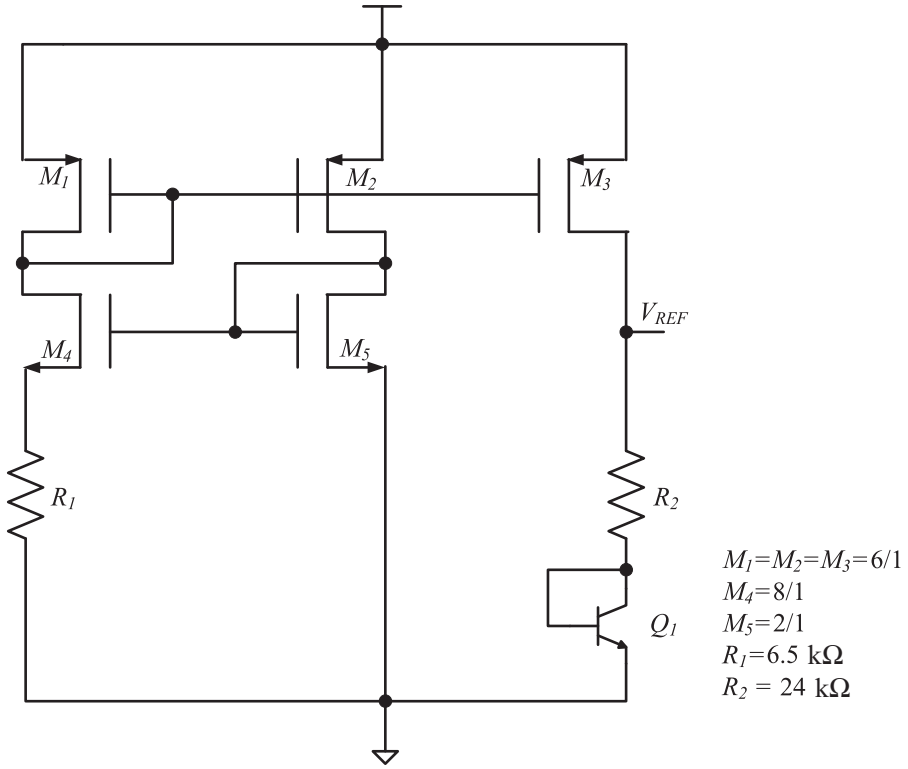


Figure 2.10 A modified Widlar bandgap voltage reference circuit for Exercise 2.3.

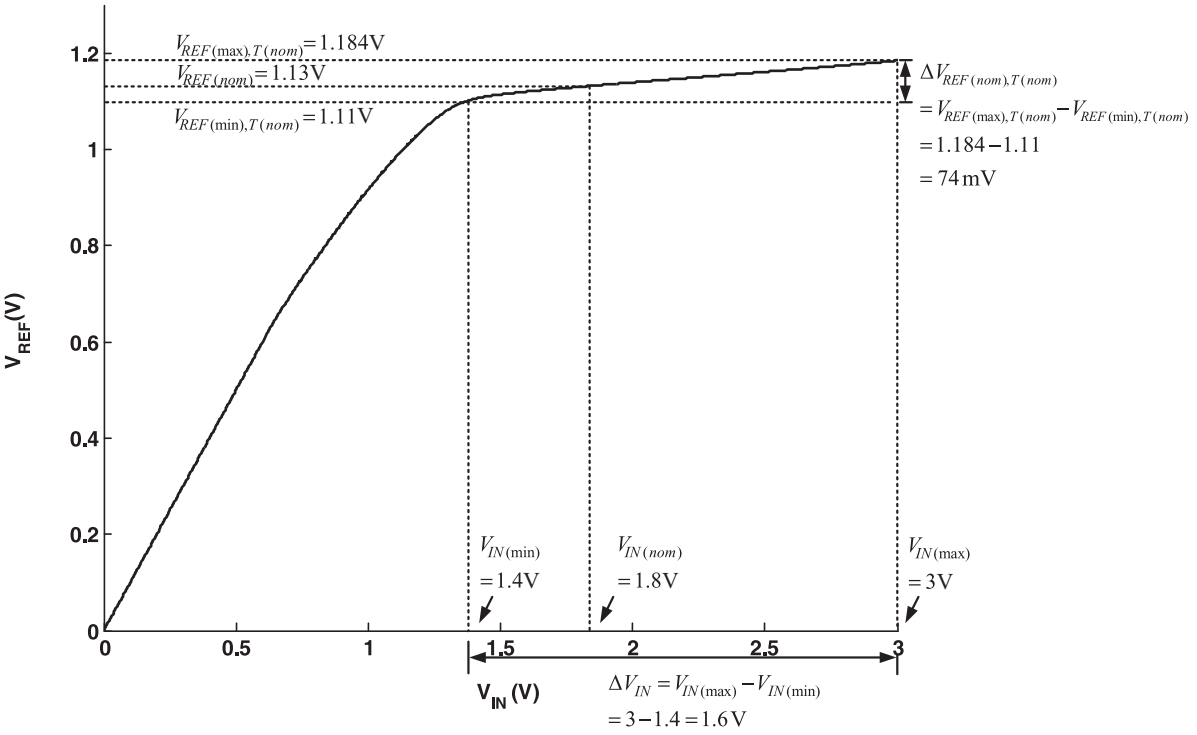


Figure 2.11 V_{REF} variation of the circuit in Figure 2.10 under V_{DD} variation for line regulation analysis in Exercise 2.3(a).

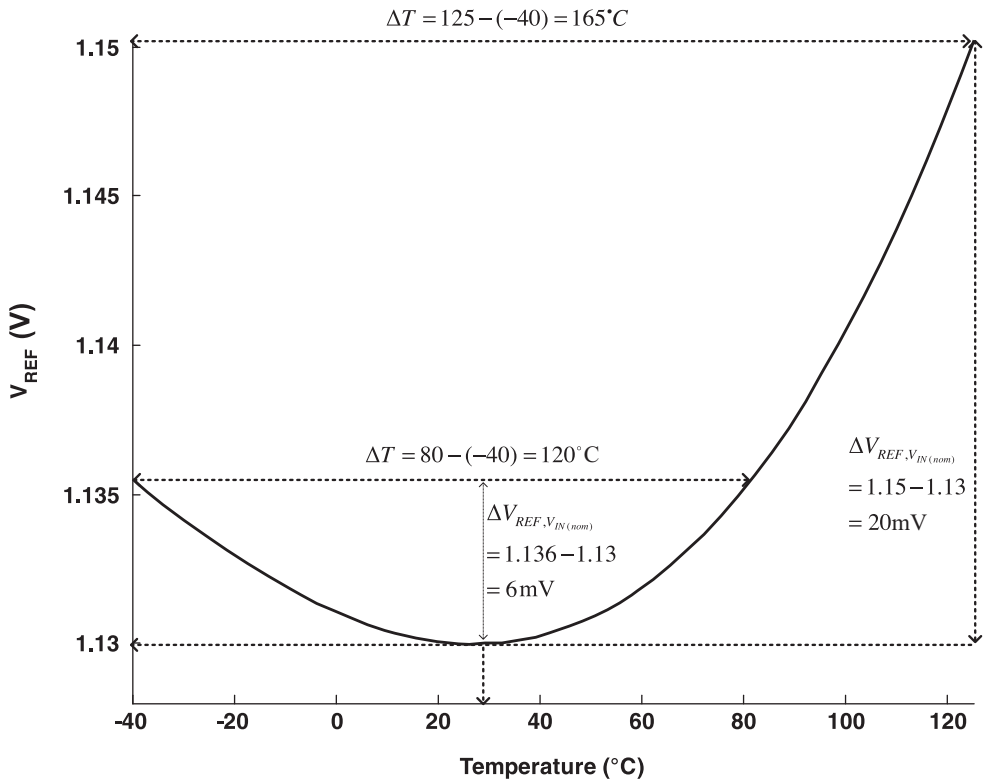


Figure 2.12 V_{REF} variation of the circuit in Figure 2.10 under temperature variation for temperature coefficient analysis in Exercise 2.3(b).

3. *Simulate the circuit using the test-bench shown in Figure 2.5 with AC sweep of frequencies from* 10 Hz *to* 10 MHz. *Obtain the waveform of* $20\log(\frac{V_{REF}}{V_{IN}})$ *as a function of frequency as shown in Figure 2.13. Derive the power supply rejection ratio (PSRR).*
4. *Simulate the circuit using the test-bench in Figure 2.7 by probing the current flowing into the circuit. Perform a DC sweep of the temperature in the simulation. Obtain the waveform of* I_q *as a function of temperature as shown in Figure 2.14. Derive the quiescent current* (I_q), *with* $V_{IN(nom)} = 1.8$ V *and* $T_{(nom)} = 300$ K.

Exercise 2.4 *Derive the output voltage, line regulation, and temperature sensitivity of the simple voltage reference in Figure 2.15 formed by (a) resistor-MOSFET voltage divider, and (b) MOSFET only voltage divider. Find the conditions on* M_1 *and* M_2 *of the MOSFET only voltage divider in Figure 2.15(b) to achieve a near-zero TC voltage reference.*

Exercise 2.5 *Consider a n-bit digital-to-analog (D/A) converter, which uses a reference voltage to generate a precision analog output voltage for a given digital input word. Assume the D/A converter is ideal in every aspect, the relative accuracy of the reference voltage will determine how many bits can effectively be converted. Determine the maximum conversion bit n if the D/A converter's reference voltage has a nominal value of* 1.2 V *with a maximum error of* ± 1.2 mV.

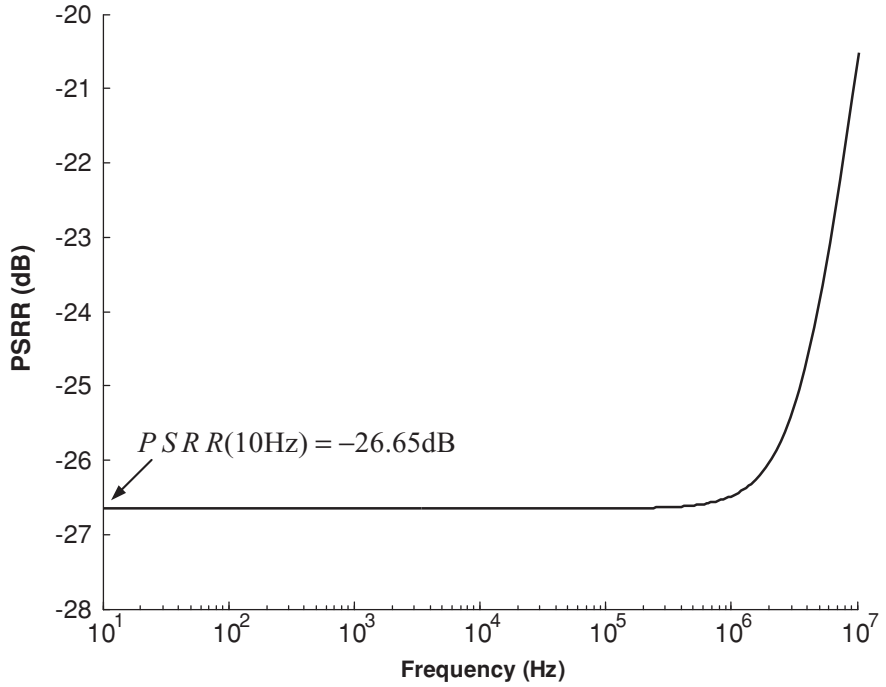


Figure 2.13 $PSRR$ of V_{REF} in the circuit shown in Figure 2.10 using the work-bench in Figure 2.5 for $PSRR$ analysis in Exercise 2.3(c).

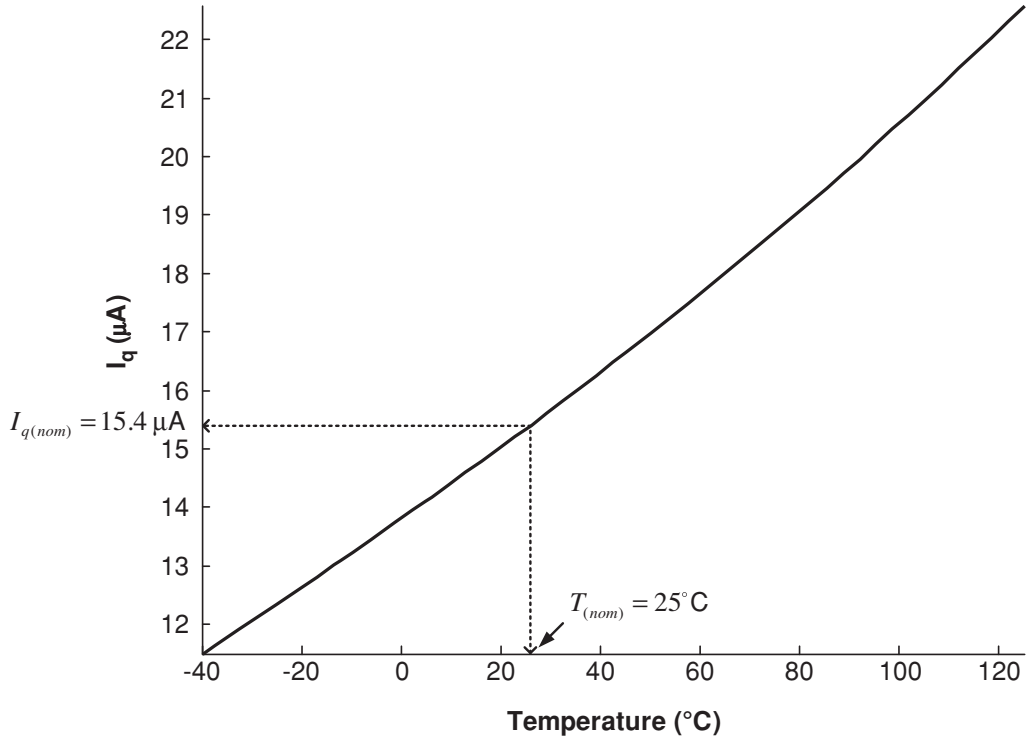


Figure 2.14 Quiescent current of the circuit in Figure 2.10 observed at different temperature for the analysis in Exercise 2.3(d).

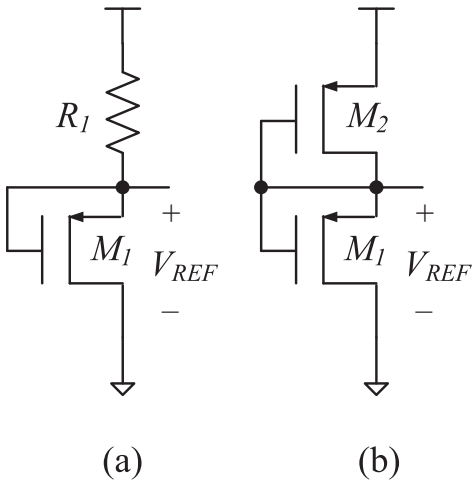


Figure 2.15 Simple voltage reference circuit implemented by (a) resistor-MOSFET voltage divider, and (b) MOSFET only voltage divider.

Exercise 2.6 *Figure 2.16 shows the schematic of a voltage regulator with V_{REF} as the reference voltage. Let the open loop gain of the error amplifier be A.*

1. *Derive V_{OUT} in terms of V_{REF}, R_1 and R_2.*
2. *Derive the load regulation of V_{OUT} of the voltage regulator.*
3. *Derive an approximation of the line regulation of V_{OUT} in terms of R_{DS_1}, R_L, A, g_{M_1}, R_1, and R_2 only. Discuss the design factors that can improve the line regulation.*
4. *Derive an approximation of $\mathcal{S}_{V_{REF}}^{V_{OUT}}$ in terms of V_{REF} and ΔV_{REF}.*

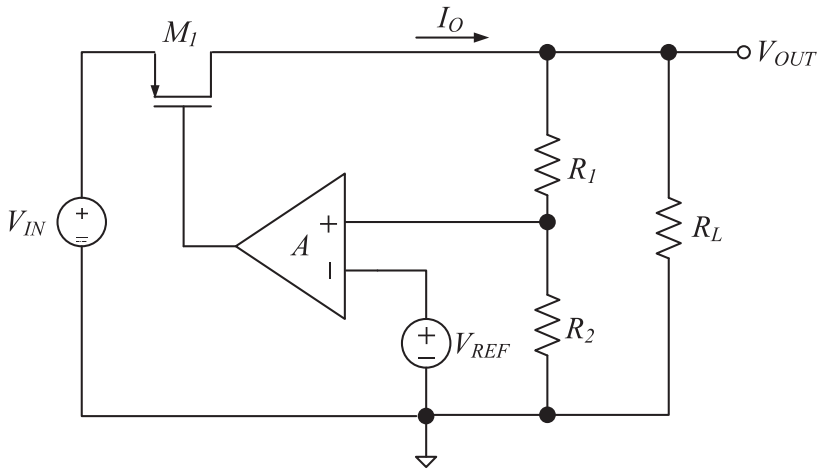


Figure 2.16 Schematic of a voltage regulator with V_{REF} as the reference voltage.

References

Allen, P.E. and Holberg, D.R. (2003) *CMOS Analog Circuit Design*. Oxford Press.

Erdi, G. (1975) A precision trim technique for monolithic analog circuits. *IEEE Journal of Solid-State Circuits*, **SC-10** (11), 412–16.

Huijsing, J., van de Plassche, R.J. and Sansen, W.M. (1996) *Analog Circuit Design: Low-noise, Low-power, Low-voltage: Mixed-mode Design with CAD Tools, Voltage, Current and Time Reference*. Kluwer Academic Publishers.

Vladimirescu, A. (1994) *The SPICE Book*. Wiley.

3

Bandgap Voltage Reference

The bandgap voltage reference circuit is one of the most commonly applied voltage reference circuit that theoretically outputs a voltage equal to the bandgap voltage of the semiconductor used. One of the first bandgap voltage reference circuits was presented by Robert Widlar of the National Semiconductor in 1971 (Widlar, 1971), and is known as the Widlar bandgap voltage reference circuit. The Widlar bandgap voltage reference circuit was implemented with the conventional junction isolated bipolar technology where the equivalent circuit is shown in Figure 5.1 in Chapter 5. The Widlar bandgap voltage reference circuit generates a stable low temperature coefficient reference voltage at 1.23 V (i.e., the bandgap voltage of silicon at room temperature derived in Exercise 1.3). This early implementation of a bandgap voltage reference circuit was successfully applied in the National Semiconductor's voltage regulator integrated circuit LM113, which proved capable of achieving an output voltage with low temperature coefficient. Since then, it has been applied in many voltage regulator integrated circuits to generate the internal reference voltage.

3.1 Widlar Bandgap Voltage Reference Circuit

The basic idea of bandgap voltage reference circuit topology is the mutual compensation of a PTAT term (V_{PTAT}) and a CTAT term (V_{CTAT}) to pursue a reference voltage with zero temperature coefficient. The compensation can be achieved by a simple weighted sum between these two voltages, such that

$$V_{sum}(T) = m_1 V_{PTAT}(T) + m_2 V_{CTAT}(T) \tag{3.1}$$

aims to achieve

$$\frac{\partial V_{sum}(T)}{\partial T} = m_1 \frac{\partial V_{PTAT}(T)}{\partial T} + m_2 \frac{\partial V_{CTAT}(T)}{\partial T} = 0. \tag{3.2}$$

Note that $\frac{\partial V_{PTAT}(T)}{\partial T} > 0$ and $\frac{\partial V_{CTAT}(T)}{\partial T} < 0$, with appropriate choice of m_1 and m_2, a zero TC $V_{sum}(T)$ can be obtained. In reality, $V_{sum}(T)$ can only achieve a near-zero TC as shown in

CMOS Voltage References: An Analytical and Practical Perspective, First Edition. Chi-Wah Kok and Wing-Shan Tam.
 Published 2013 by John Wiley & Sons Singapore Pte. Ltd.

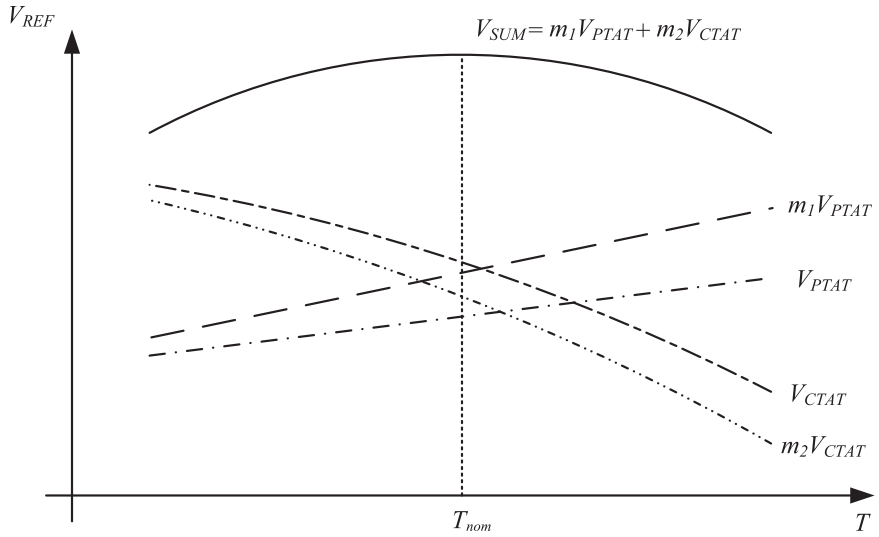


Figure 3.1 The temperature variation of reference voltage obtained as the voltage sum $V_{sum} = m_1 V_{PTAT} + m_2 V_{CTAT}$.

Figure 3.1. We shall say that the compensated voltage $V_{sum}(T)$ is a near-zero *TC* voltage, if $\frac{\partial V_{sum}(T)}{\partial T}|_{T=T_{(nom)}} = 0$ (in other books and papers, you may find this property described as zero temperature coefficient at $T_{(nom)}$. In this book, we shall adopt near-zero *TC* because we are actually describing the temperature coefficient of the voltage under consideration being close to zero in the temperature range of interest). The Widlar bandgap voltage reference circuit that adopted the above PTAT and CTAT voltages' mutual compensation topology can only achieve a near-zero *TC* voltage in a limited temperature range because both $V_{PTAT}(T)$ and $V_{CTAT}(T)$ are nonlinear functions of the temperature and thus result in a voltage sum $V_{sum}(T)$ being a nonlinear function of temperature. The CTAT voltage in the Widlar bandgap voltage reference circuit is formed by the V_{BE} of a BJT, while the PTAT voltage in the Widlar bandgap voltage reference circuit is formed by V_T extracted from ΔV_{BE} of two BJTs biased in the different current density. The block diagram of the Widlar bandgap voltage reference circuit is shown in Figure 3.2. Recall the temperature characteristics of V_{BE} and V_T in Section 1.1, which are given by Equation 1.8 as -1.73 mV/K, and Equation 1.15 as 0.09 mV/K, respectively at $T_{(nom)} = 300$ K. According to Equation 3.1, a near-zero *TC* reference voltage can be obtained by the weighted sum of V_{BE} and V_T as shown in Figure 3.2, where

$$V_{REF}(T) = V_{BE}(T) + MV_T(T). \tag{3.3}$$

Differentiating Equation 3.3 with respect to the temperature yields

$$\begin{aligned} \frac{\partial V_{REF}(T)}{\partial T} &= \frac{\partial (V_{BE}(T) + MV_T(T))}{\partial T} \\ &= \frac{\partial V_{BE}(T)}{\partial T} + M\frac{\partial V_T(T)}{\partial T}. \end{aligned} \tag{3.4}$$

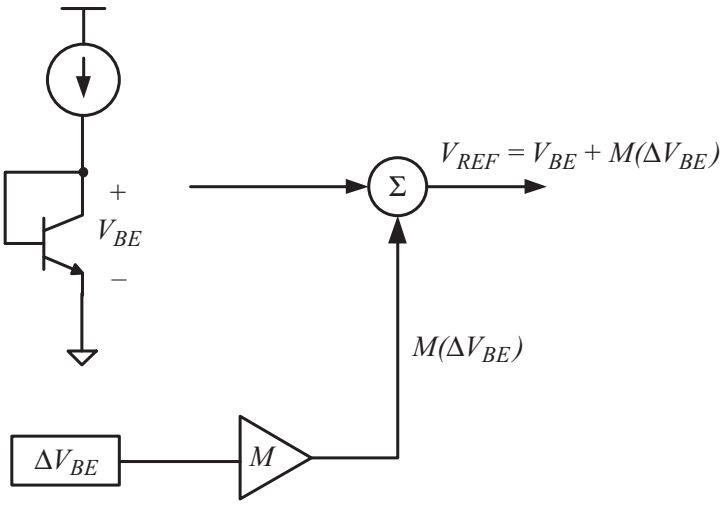


Figure 3.2 Topological block diagram of Widlar bandgap voltage reference circuit.

Noted that $\frac{\partial V_{BE}(T)}{\partial T} = -1.73$ mV/K and $\frac{\partial V_T(T)}{\partial T} = 0.09$ mV/K. Therefore, the optimal M at $T = T_{(nom)}$ obtained by evaluating $\frac{\partial V_{REF}(T)}{\partial T}|_{T=T_{(nom)}} = 0$ yields

$$M = -\frac{\partial V_{BE}(T)}{\partial T} \Big/ \frac{\partial V_T(T)}{\partial T}\Big|_{T=T_{(nom)}} = \frac{-1.73}{-0.09} = 19.22. \tag{3.5}$$

Substituting M into Equation 3.3 yields a near-zero TC reference voltage with value 1.23 V at $T = T_{(nom)}$. Since both V_{BE} and V_T are nonlinear functions with respect to temperature, Equation 3.3 with M given by Equation 3.5 can only generate a near-zero TC voltage within a limited temperature range closes to $T_{(nom)}$. To increase the operating temperature range of the voltage reference circuit while achieving a low TC reference voltage, other compensation techniques will have to be adopted to compensate the temperature effect of the nonlinear terms in Equation 3.1. There are a variety of compensation methods presented in the literature, and different combinations of precision elements have been presented to obtain reference voltages with different properties. The combination of different precision elements and the compensation methods that form different voltage reference circuit topologies will be the topic of later chapters.

In summary, the Widlar bandgap voltage reference circuit shows that if a CTAT voltage is summed with a PTAT voltage that has been scaled appropriately, such that both the CTAT voltage and the scaled PTAT voltage have the same temperature characteristic in magnitude, then a voltage equal to the silicon bandgap voltage V_{G0} will be obtained (again, please refer to Exercise 1.3). The obtained voltage reference voltage is almost independent of the operating temperature, where the temperature coefficient is around $10 \sim 100$ ppm/K. In the case of the Widlar bandgap voltage reference circuit, a small temperature coefficient reference voltage is conveniently achieved by proper scaling of the PTAT voltage V_T with the scaling factor M to produce a weighted voltage MV_T, which is then summed with the CTAT voltage V_{BE}, to produce a reference voltage V_{REF} with near-zero TC. In a similar manner, the mutual compensation of the PTAT and CTAT sources can be performed in the current domain. Both

the voltage summing reference circuit and current summing reference circuit will be discussed in later chapters.

The bandgap voltage reference circuit with output given by Equation 3.3 is known as the first order compensation circuit. The bandgap voltage reference circuit with a small temperature coefficient or a near-zero *TC* over a wide temperature range can be obtained by further compensating the nonlinear terms of the PTAT and CTAT voltages. The associated compensation error between the nonlinear terms of the PTAT and CTAT voltages is known as *curvature error*. The detailed causes of curvature error and the high order compensation methods that reduce the curvature errors will be discussed in later chapters. Besides the curvature error, the circuit component variation is another important factor that affects the accuracy of the voltage reference circuit. The circuit component value variation induced reference voltage accuracy problem can be alleviated by better layout and device matching, circuit topology, and post-processing trimming technique. Their application, and the pros and cons of each technique, will be detailed in the next chapters.

While the compensation methods of various reference circuits will be detailed in later chapters, in the meantime we shall review a popular voltage reference circuit, the opamp (operational amplifier) based β-multiplier bandgap voltage reference circuit. The opamp based β-multiplier bandgap voltage reference circuit is a first-order compensated voltage summing bandgap voltage reference circuit that implements the circuit topology in Figure 3.2.

3.2 Drain Voltage Equalization Current Mirror

It has been shown in Equation 1.14 that ΔV_{BE} is a PTAT voltage. To extract ΔV_{BE}, a resistor R_1 is inserted in series with Q_2 as shown in Figure 3.3. If $V_A = V_B$, the voltage across R_1 equals $\Delta V_{BE_{1,2}}$. The current flowing through the resistor equals $I_2 = \Delta V_{BE_{1,2}}/R_1 = V_T \ln N/R_1$. This PTAT current can be extracted by a current mirror and converted back to a PTAT voltage using another resistor. The PTAT voltage can then be combined with the CTAT voltage to generate a reference voltage with a low temperature coefficient. An added advantage of this circuit is the ability to increase the current flowing through R_1 by simply decreasing the resistance of R_1

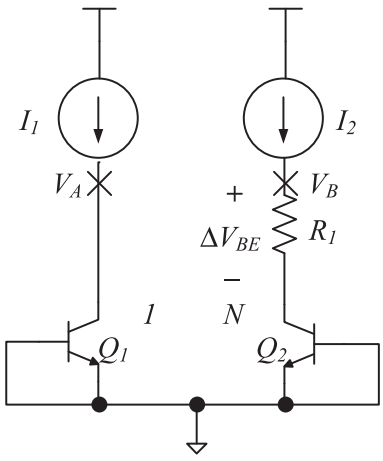


Figure 3.3 Extraction of ΔV_{BE}.

without having to scale the sizes of the bipolar transistors massively, as will be demonstrated in Section 4.1.1.2. Increasing the current across R_1 provides several advantages when the bandgap voltage reference circuit is implemented with non-ideal circuit components, such as reducing the effect of the component mismatch problem which will be discussed in Section 4.1.1.2.

The real challenge of the ΔV_{BE} extraction circuit in Figure 3.3 is the design of the matched current mirror to generate I_1 and I_2. The two current sources can be constructed by current mirror where the gate nodes and source nodes of the two transistors are connected. Let's consider the simple case where $I_1 = I_2$ obtained by a simple current mirror as shown in Figure 3.4. However, this simple current mirror architecture will suffer from the channel modulation problem due to the difference between the drain voltages (V_A and V_B) of the two transistors that form the current mirror (for details, please refer to Section 4.2.1) as shown in Figure 3.5. We can carefully select R_1 to make $V_A = V_B$, or we can use a drain voltage equalization technique (You *et al.*, 1997). The drain voltage equalization technique places an opamp in the feedback loop with its inputs connected to the drains of the mirror transistors, V_{D_1} and V_{D_2}, which are V_A and V_B respectively. The error amplifier output is connected to the gate node of the transistors. Due to the feedback configuration, $V_{D_1} = V_A$ and $V_{D_2} = V_B$ are forced to have the same potential and thus achieved equal drain voltages. As a result, the two mirror transistors will have the same drain, gate, source, and bulk node voltages. This forces the drain currents of the two transistors to be equal. The gain of the error amplifier will determine the accuracy of the drain voltages and the accuracy of the mirrored current. Figure 3.6 shows an example of the bandgap voltage reference circuit that makes use of the

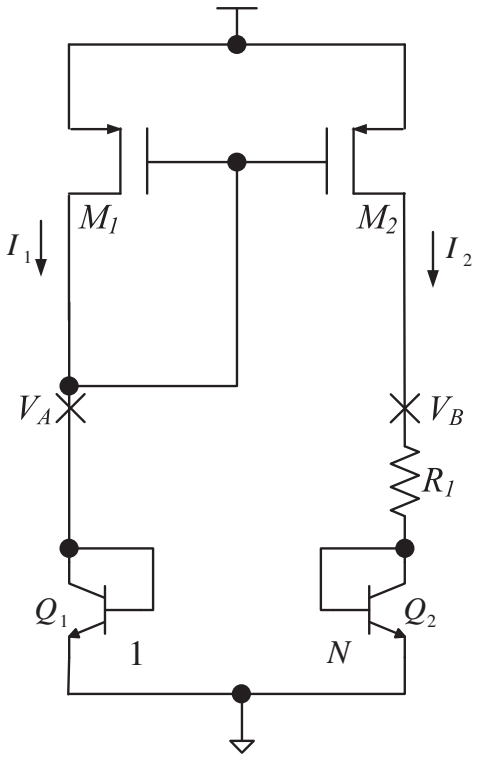


Figure 3.4 Schematic diagram of a drain voltage equalization current mirror based ΔV_{BE} extraction circuit.

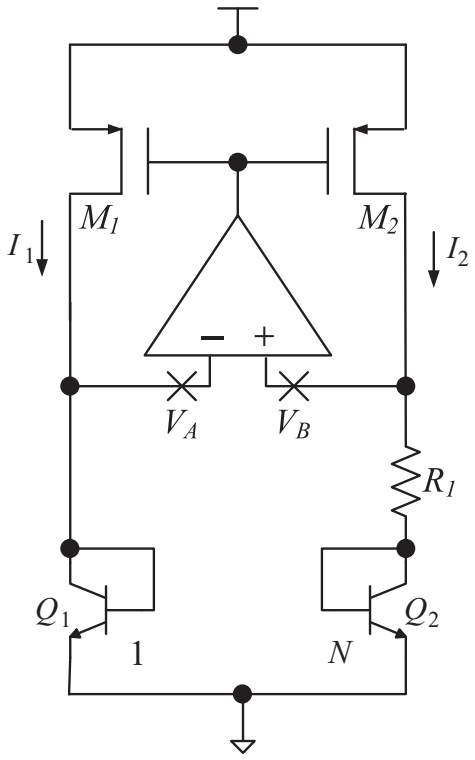


Figure 3.5 Schematic diagram of an opamp based drain voltage equalization current mirror to extract ΔV_{BE}.

drain voltage equalization technique. Such voltage reference circuits are well known in the community as opamp based β-multiplier bandgap voltage reference circuits, and we shall use the same naming convention in this book.

3.2.1 Opamp Based β-Multiplier Bandgap Voltage Reference Circuit

Figure 3.6 shows the schematic of the opamp based β-multiplier bandgap voltage reference circuit that follows the compensation method depicted in Figure 3.2. A simplified block diagram of the circuit is shown in Figure 3.7, where the whole system can be viewed as a feedback circuit composed of three main blocks, the opamp, feedback network which is also referred to as the bandgap core, and the output block. The amplifier gain is denoted as $\alpha(s)$, the loop gain is given by $\beta\alpha(s)$, and hence the notation β-multiplier. Different output sub-circuits can be applied to achieve different output voltage characteristics. As will be discussed in Section 6.1, bandgap voltage reference circuits with output voltage lower than 1 V can be achieved by using special output sub-circuits. In the meantime, we shall concentrate on the schematic and the equivalent block diagram as shown in Figure 3.6 and Figure 3.7, respectively, for our discussions on the design and operation of the opamp based β-multiplier bandgap voltage reference circuit, and in particular, the analysis of the $PSRR$ of the bandgap voltage reference circuit will be discussed in Section 4.5.

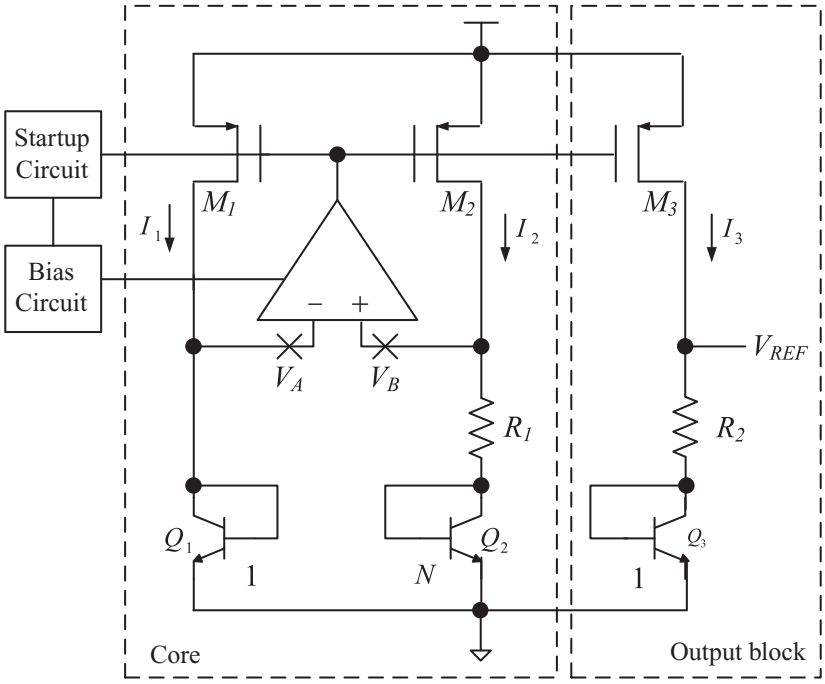


Figure 3.6 Schematic of an opamp based β-multiplier bandgap voltage reference circuit.

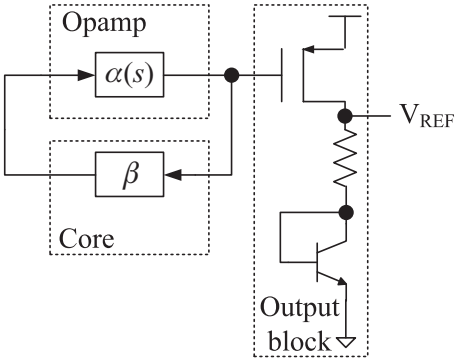


Figure 3.7 Block diagram of the opamp based β-multiplier bandgap voltage reference circuit.

3.2.2 Bandgap Voltage Reference Circuit

The opamp based β-multiplier bandgpap voltage reference circuit consists of four major sub-circuits, which are the current mirror pair and the opamp that form the β-multiplier (or drain voltage equalizer) to extract the $\Delta V_{BE_{1,2}}$, the V_{BE} voltage sources, and the startup circuit (which is not shown in Figure 3.6). A startup circuit is required because the β-multiplier circuit is a metastable system which can become stable in both equilibrium state and quasi-equilibrium state. When the circuit starts, it is at the quasi-equilibrium state with zero current in the β-multiplier circuit, that is $I_1 = I_2 = 0$. As a result $V_A = V_B = 0$, which keeps the opamp output unchanged, and thus maintains the bias of M_1 and M_2 to output $I_1 = I_2 = 0$. As a

result, the circuit is said to be in quasi-equilibrium state, and maintains the whole circuit in the startup condition. A startup circuit is therefore required to provide an external excitation to the quasi-equilibrium state, and brings the metastable system to the equilibrium state that produces a stable reference voltage. While the design of the startup circuit will be discussed later, it should be noted that the startup circuit will only be effective during the time before the system reaches the equilibrium state. When the bandgap voltage reference circuit is in equilibrium state, the startup circuit has a negligible effect on the reference voltage of the voltage reference circuit, and hence all the performance parameters of the circuit.

The current mirror pair is formed by transistors M_1, M_2, and M_3 having identical size, such that the currents flowing through the three transistors are the same as $I_1 = I_2 = I_3 = I$. The β-multiplier consists of three diode connected NPN transistors Q_1, Q_2, and Q_3, with their emitter area ratios being $1 : N : 1$ to provide the required temperature dependent voltages to construct the voltage reference circuit. Let V_{BE_1}, V_{BE_2} and V_{BE_3} be the base-emitter voltages of Q_1, Q_2, and Q_3, respectively. The voltages V_A and V_B are thus given by

$$V_A = V_{BE_1}, \tag{3.6}$$
$$V_B = I R_1 + V_{BE_2}. \tag{3.7}$$

The infinite input impedance of the opamp clamps V_A and V_B to the same voltage level. As a result, equating Equations 3.6 and 3.7 yields

$$V_A = V_{BE_1} = I R_1 + V_{BE_2} = V_B, \tag{3.8}$$
$$V_{BE_1} - V_{BE_2} = I R_1, \tag{3.9}$$
$$\Delta V_{BE_{1,2}} = V_T \ln(N) = I R_1, \tag{3.10}$$

where the term $\Delta V_{BE_{1,2}}{=}V_T \ln(N)$ is obtained by Equation 1.14. Hence, the voltage across R_1 equals the PTAT voltage V_T scaled by $\ln(N)$. Therefore, the current I that flows through the current mirror of the β-multiplier is a PTAT current and is given by

$$I = V_T \frac{\ln(N)}{R_1}. \tag{3.11}$$

The current mirror ensures that $I_3 = I$, thus the PTAT current I will induce a PTAT voltage across R_2. The reference voltage V_{REF} is the sum of the voltage across R_2 and V_{BE_3},

$$\begin{aligned} V_{REF} &= I R_2 + V_{BE_3} \\ &= \frac{R_2}{R_1} \Delta V_{BE_{1,2}} + V_{BE_3} \\ &= \frac{R_2 \ln(N)}{R_1} V_T + V_{BE_3}. \end{aligned} \tag{3.12}$$

Comparing Equations 3.12 and 3.3 reveals that the opamp based β-multiplier bandgap voltage reference circuit is a first-order compensated bandgap voltage reference circuit, where the

weighting factor $M = \frac{R_2 \ln(N)}{R_1}$ scales the PTAT voltage V_T, which is summed with the CTAT voltage V_{BE_3}. We shall define $V_{REF\text{-}CONV}$ as

$$V_{REF\text{-}CONV} = MV_T + V_{BE}, \tag{3.13}$$

which is regarded as the reference voltage obtained from "*conventional*" opamp based β-multiplier bandgap voltage reference circuits. At room temperature $T = T_{(nom)}$, the first order approximation given by Equations 1.8 and 1.15 (i.e., $\frac{\partial V_{BE}}{\partial T} = -1.73$ mV/K and $\frac{\partial V_T}{\partial T} = 0.09$ mV/K) yields $M = 19.22$ as derived in Equation 3.5. The weighting factor M is linearly proportional to the transistor ratio $\ln(N)$, and the resistor ratio R_2/R_1. Consider the case of $N = 8$, the resistor ratio that achieves zero $TC\ V_{REF}$ at $T = T_{(nom)}$ is obtained as

$$\begin{aligned} \left.\frac{\partial V_{REF}}{\partial T}\right|_{T=T_{(nom)}} &= \frac{R_2 \ln(N)}{R_1}\frac{\partial V_T}{\partial T} + \frac{\partial V_{BE_3}}{\partial T} = 0 \\ \frac{R_2}{R_1}\ln(8)\cdot 0.09 \times 10^{-3} - 1.73 \times 10^{-3} &= 0 \\ \frac{R_2}{R_1} &\approx 9.24 \end{aligned} \tag{3.14}$$

The bipolar transistor will be biased to work in the active region with a 6 μA collector-current, as discussed in Section 1.1, to obtain the smallest quiescent current. This collector-current can be obtained by adjusting the resistance of R_1. At $T = T_{(nom)}$, the resistance of R_1 can be obtained from Equation 3.11 with $I = 6$ μA.

$$\begin{aligned} R_1 &= \frac{V_T \ln(N)}{I} \\ &= \frac{kT}{q}\frac{\ln(N)}{I} \\ &= \frac{1.38 \times 10^{-23}\cdot 300\cdot \ln(8)}{6 \times 10^{-6} \times 1.6 \times 10^{-19}} \\ &= 8.97\ \text{k}\Omega. \end{aligned} \tag{3.15}$$

The resistor ratio in Equation 3.14 with $R_1 = 8.97$ kΩ will yield $R_2 = 9.24 \cdot R_1 = 82.9$ kΩ. Substituting $T = T_{(nom)}$, $I = 6$ μ A, $R_2 = 82.9$ kΩ and $V_{BE_3} = 0.73$ V into Equation 3.12 will yield $V_{REF} = 1.23$ V with $\frac{\partial V_{REF}}{\partial T}|_{T=T_{(nom)}} = 0$, where the resistors R_1 and R_2 of the circuit are set to the values obtained above. Figures 3.8 and 3.9 plot the SPICE simulation results of the output voltage of the circuit in Figure 3.6 with varying temperature and input voltage, respectively. It can be observed from Figure 3.8 that the circuit starts working and generates a stable output voltage at $V_{DD} = 1.4$ V. This is the minimum operating voltage of the circuit, and in Chapter 4 we shall discuss the physical constraint that affects the minimum operating voltage of the circuit in Figure 3.6. The curvature error of the output voltage of the voltage reference circuit in Figure 3.6 can be observed from Figure 3.9. We further observe that the curvature error is linearly dependent on the input voltage. Due to the fact that the output voltage increases with increasing input voltage, the output voltage versus temperature curve is also observed to

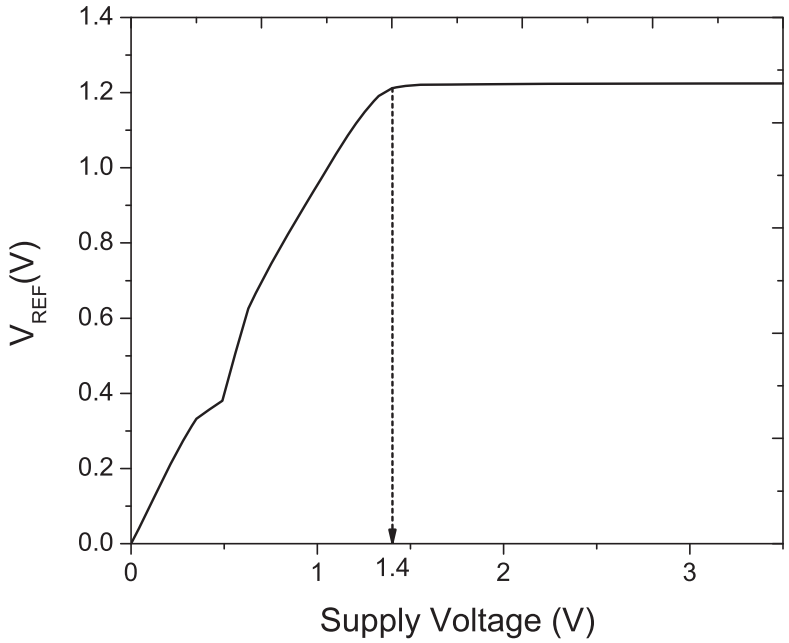


Figure 3.8 Reference voltage obtained from the opamp based β-multiplier bandgap voltage reference circuit with varying supply voltage.

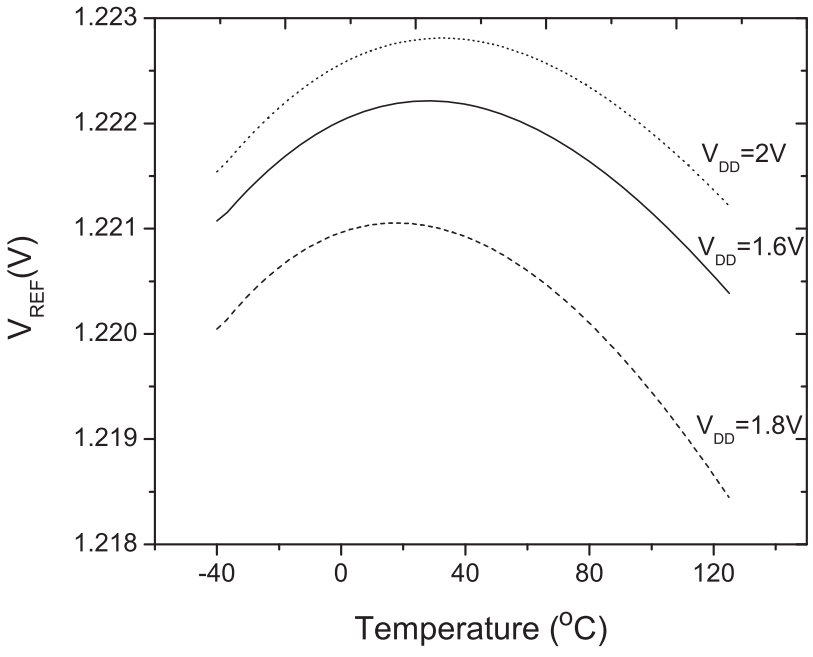


Figure 3.9 Reference voltage obtained from the opamp based β-multiplier bandgap voltage reference circuit at various input voltages with varying temperature.

be shifted up with increasing input voltage. The curvature error will therefore be the smallest at a particular input voltage. In the case of operating temperatures between $-25\,^{\circ}\text{C} \sim 75\,^{\circ}\text{C}$, the temperature coefficient will achieve its smallest value at $V_{DD} = 1.8$ V. The variation of the output voltage with different input voltage is measured as the line regulation of the voltage reference circuit. The line regulation of the circuit in Figure 3.6 can be measured from Figure 3.8, which is found to be 3.5 mV/V or 0.35%. The line regulation of the reference circuit is small and exhibits an almost linear property across the observed temperature range as shown by the shifting curve property in Figure 3.9. The temperature coefficient of the voltage reference circuit measured from Figure 3.9 at $V_{DD} = 1.8$ V is 6.67 ppm/K with a temperature range $[-40\,^{\circ}\text{C}, 125\,^{\circ}\text{C}]$.

Clearly, the temperature coefficient of V_{REF} obtained by the circuit in Figure 3.6 is derived with ideal circuit elements. Even though it is almost impossible to implement a circuit with ideal circuit elements, we shall discuss the design and silicon layout of the major sub-circuits in Figure 3.6 assuming they are ideal. While the problem of the circuit element variations on V_{REF} will be discussed in next chapter.

3.3 Major Circuit Elements

The functions and design requirements of various circuit elements in the opamp based β-multiplier bandgap voltage reference circuit will be discussed in the following sections. The design parameters listed in these sections are obtained from proven silicon samples of opamp based β-multiplier bandgap voltage reference circuits, which can be used as a design reference for readers to design their own bandgap voltage reference circuits. The same set of design parameters will be used throughout all simulation results presented in this book, so as not to create any ambiguity between the descriptions in the text and the presented simulation results obtained from SPICE.

3.3.1 Operational Amplifier (opamp)

A high gain opamp is desirable for maintaining a virtual short circuit at the two inputs of the opamp in the close-loop construction of the β-multiplier circuit. High gain is also desirable to maintain the stability of the close-loop β-multiplier. Figure 3.10 shows the schematic of a one-stage differential amplifier, which is used for the ease of explanation and performing analytical analysis of various opamp characteristics that affect the performance of the voltage reference circuit. The silicon proven voltage reference circuit presented in this book, and applied in SPICE simulations, is a two-stage differential amplifier, which has very high gain for high performance voltage reference circuits and fast convergence in SPICE simulations. The SPICE netlist of the two-stage opamp is listed in Appendix B. The W/L of each MOSFET in the schematic in Figure 3.10 are listed on the side of individual MOSFETs within the figure. Listed in Table 3.1 are the performance parameters of the opamp in Figure 3.10. When this amplifier is applied to the schematic in Figure 3.6, the complete transistor level schematic of the opamp based β-multiplier bandgap voltage reference circuit is shown in Figure 3.11. The application of this simple opamp in the bandgap voltage reference circuit does limit the performance of the voltage reference circuit. Some of these limits can be immediately observed

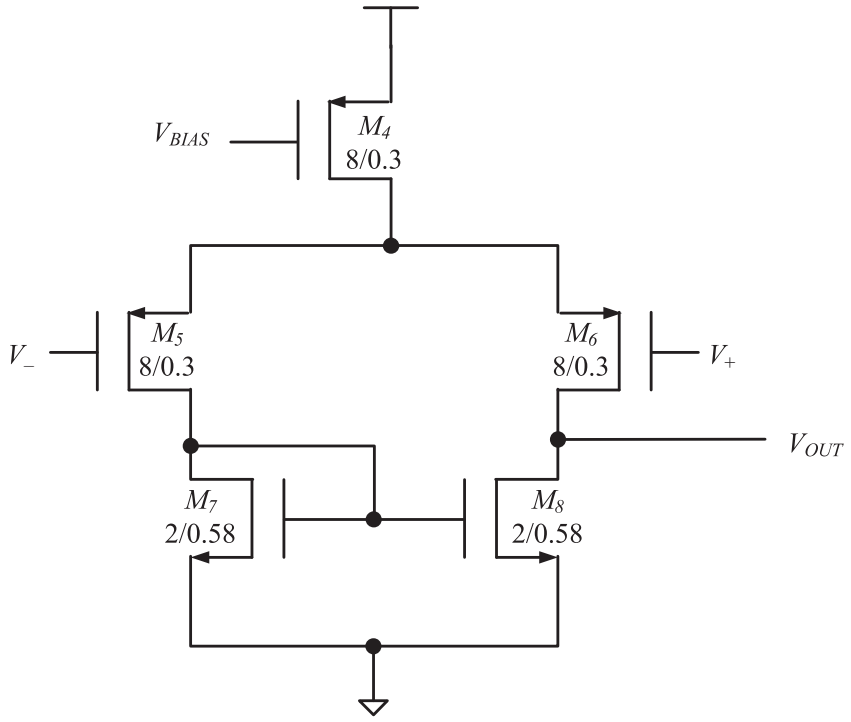


Figure 3.10 Schematic of a single stage opamp used in this book.

from the opamp performance listed in Table 3.1. It is clear from the performance parameters that the opamp suffers from the input offset problem. When the negative input terminal V_- is connected to the output terminal V_{OUT}, the opamp is configured to form an inverted feedback loop. The output voltage of an ideal opamp in the inverted feedback loop should follow that of the positive input terminal V_+. However, due to the input offset problem, the output voltage of a real world implementation of the opamp can deviate from that voltage. A potential difference is required to add onto the positive input terminal V_+, which equals the input offset voltage, to bring the output voltage of the opamp equals to the input voltage V_+. This input offset problem

Table 3.1 Specification of opamp used in this book with 1.8 V supply voltage and 18 fF output capacitive load.

Parameter	Values
DC Gain (A_v)	74.52 dB
Corner Frequency	2.03 kHz
Unity Gain Bandwidth	106 MHz
Phase Margin	46.7 °
Offset	10 mV
Current	20 μA
Slew Rate (Rise)	123×10^6 V/s
Slew Rate (Fall)	151×10^6 V/s
Input Common Mode Range	0.1 V ∼ 1.2 V
$PSRR$	94.97 dB
CMRR	73.7 dB

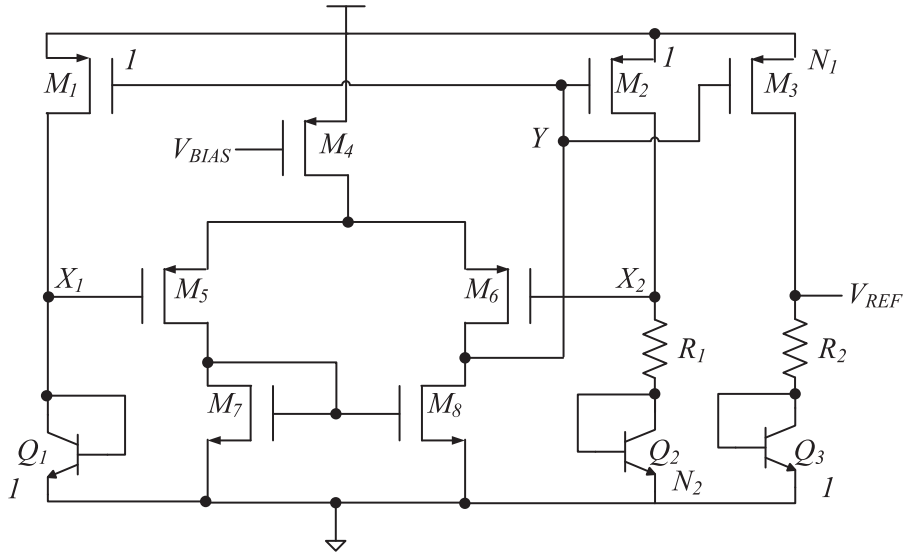


Figure 3.11 MOSFET transistor level schematic of the opamp based β-multiplier bandgap voltage reference circuit.

is caused by many factors, the channel length modulation problem of the input MOSFET and the matching problem of the input transistor are the greatest contributors. The input offset voltage can be estimated from SPICE simulation and corner analysis in particular can be used to observe the voltage applied to V_+ bringing the output voltage of the inverted feedback loop to be equal to the input voltage.

When the opamp is connected to form a β-multiplier circuit, it requires the voltages at the two input terminals to be the same. In the case of the opamp based β-multiplier, the opamp will bias the current mirror according to the voltage difference between its two input terminals, such as to force the voltages at the two input terminals to be the same. This is theoretically possible when the opamp has high enough gain. The open loop gain (A_v) of the opamp is defined as

$$A_v(\text{dB}) = 20\log\left(\frac{V_{OUT}}{(V_+ - V_-)}\right), \tag{3.16}$$

which is also known as the DC gain. A high A_v is desirable for stable operation of the voltage reference circuit and a typical A_v larger than 60 dB should be adopted. Furthermore, an opamp with a large open loop gain and high $PSRR$ can help to reduce the noise induced on the reference voltage.

As a result, among all the design parameters of the opamp, the open loop gain, the offset voltage, and the $PSRR$ are the particular parameters that have the greatest impact on the performance of the opamp based β-multiplier bandgap voltage reference circuit. Other AC performance parameters of the opamp have their own effects on the performance of the opamp based β-multiplier bandgap voltage reference circuit. However, their effects are less important because the voltage reference circuit mostly operates in DC condition. The voltage reference circuit problem of applying an opamp with small A_v, narrow unity gain bandwidth, low $PSRR$, and large offset will be discussed in Section 4.1.

Another performance limitation of the opamp circuit in Figure 3.10 is the minimum V_{DD} required to operate the opamp properly. When $V_{DD} < 1.7$ V, M_1 will be working in the linear region and thus tremendously reducing the biasing current, which leads to a decrease in the common mode gain. If the V_{DD} keeps dropping, M_1 will work in the weak inversion region, which means the opamp is unable to achieve enough gain to maintain normal operation. As a result, it posts a limitation on the minimum operating voltage of the opamp based β-multiplier bandgap voltage reference circuit. However, it is our intention to leave the design of low voltage opamps to other texts, such that all the problems and concerns over the design and analysis of the voltage reference circuit with the assumption that low voltage opamp is available in the circuit implementation will be presented in the rest of this book.

3.3.1.1 Input Common Mode Voltage

The opamp in the voltage reference circuit should be able to operate with an input common mode voltage of V_{BE}, as V_+ and V_- are connected to Q_1 and Q_2 as shown in Figure 3.6. A voltage of magnitude equal to $V_{BE} \approx 0.73$ V at $T_{(nom)}$ is just enough to turn an NMOS transistor on. As a result, the opamp in Figure 3.10 uses a pair of PMOS as the differential input pair. For the output of the opamp, it needs to drive a PMOS transistor. Therefore, the output common mode voltage needs to be fairly high. This set of requirements complicates the opamp design, requires extra power and creates noise in the system. A detailed analysis of how the input common mode voltage of the opamp affects the design of voltage reference circuit with low supply voltage will be discussed in Chapter 6.

3.3.1.2 Loop Gain

By inserting the opamp in Figure 3.10 into the voltage reference circuit in Figure 3.6, we obtain a MOSFET level voltage reference circuit schematic as shown in Figure 3.11. The transistors $M_4 \sim M_8$ form the opamp. The current mirrors are formed by transistors M_1, M_2, and M_3 which have their W/L of the transistors equal $1 : 1 : N_1$, and the emitter area ratio of Q_1 and Q_2 equals $1 : N_2$ (where we left the non-unit current gain of the current mirror to be discussed in Section 4.1.1.2). As a result, the reference voltage is $V_{REF} = V_{BE_3} + N_1 \frac{R_2}{R_1} \ln(N_2) V_T$. A near-zero TC reference voltage equals to 1.23 V is obtained when $N_1 \ln(N_2) \frac{R_2}{R_1} = 19.22$. The feedback loop within the bandgap voltage reference circuit forms the following KVL loop

$$((X_2 - Y A_{M_2}) - (X_1 - Y A_{M_1}))A_v = Y, \tag{3.17}$$

where A_{M_1} and A_{M_2} are the gain of M_1 and M_2, respectively. A_v is the differential gain of the opamp. As a result the close loop gain is given by

$$A_{close-loop} = \frac{Y}{X_2 - X_1} = \frac{A_v}{1 + A_v(A_{M_2} - A_{M_1})}. \tag{3.18}$$

If A_v is large enough, the close loop gain can be approximated as

$$A_{close-loop} = \frac{1}{(A_{M_2} - A_{M_1})}. \tag{3.19}$$

It can be observed that $A_{M_1} = g_{m_1} R_{Q_1}$, $A_{M_2} = g_{m_2}(R_1 + R_{Q_2})$, and $R_1 >> R_{Q_2}$. Substituting the above into the approximated close loop gain yields,

$$A_{close-loop} = \frac{1}{g_{m_2} R_1 + (g_{m_1} + g_{m_2}) R_{Q_2}} \approx \frac{1}{g_{m_2} R_1}, \tag{3.20}$$

where the current mirror is assumed to be perfectly matched, and thus $g_{m_1} = g_{m_2}$. The total gain of the voltage reference circuit, also known as the system gain, is given by the output of the close loop and the gain of M_3,

$$A_{total} = A_{close-loop} g_{m_3}(R_2 + R_{Q_3}), \tag{3.21}$$

where $g_{m_3} = N_1 g_{m_1}$, and $R_{Q_3} = \frac{R_{Q_1}}{N_1}$. Substitute this into A_{total} with the assumption that the circuit is properly designed to achieve near-zero *TC*, then

$$\begin{aligned} A_{total} &= \frac{1}{g_{m_1} R_1} g_{m_3}(R_2 + R_{Q_3}) \\ &= N_1 \frac{R_2}{R_1} + \frac{R_{Q_1}}{R_1} \\ &= N_1 \frac{R_2}{R_1} + \frac{1}{\ln(N_2)}, \end{aligned} \tag{3.22}$$

where we have made use of the fact that $\Delta V_{BE_{1,2}} = I_C R_{Q_2} - I_C R_{Q_1} = V_T \ln(N_2)$ with the assumption that $R_{Q_1} \approx R_{Q_2}$. It can be observed that the total gain is linearly proportional to N_1 and inversely proportional to $\ln(N_2)$. Since g_{m_3} is linearly proportional to N_1, therefore, the larger the gain of the output stage, the larger the system gain. However, the increased system gain obtained in this way does not improve the loop gain, and thus does not improve the system stability. The overall system stability can be improved by using transistor Q_1 and Q_2 with area ratio close to 1. However, when the area ratio is close to 1, a large resistor ratio $\frac{R_2}{R_1}$ is required to achieve the necessary PTAT scaling for near-zero *TC* reference voltage. Thus high system stability is being traded with large resistor layout.

3.3.1.3 Layout Example

Figure 3.12 shows the layout of the opamp used in this book. The centroid symmetric and inter-digitized layout techniques, similar to those described in Section 1.4 for resistor matching, have been applied to the transistor pairs in the opamp in order to reduce the device mismatch problems. Readers should also consider the layout example in Section 3.3.2.1 for current mirrors to understand the layout technique presented in Figure 3.12 for both the input transistor pair and the current mirror transistor pair, where both inter-digitization and cross-coupling techniques are applied to reduce the input offset voltage (Hastings, 2001).

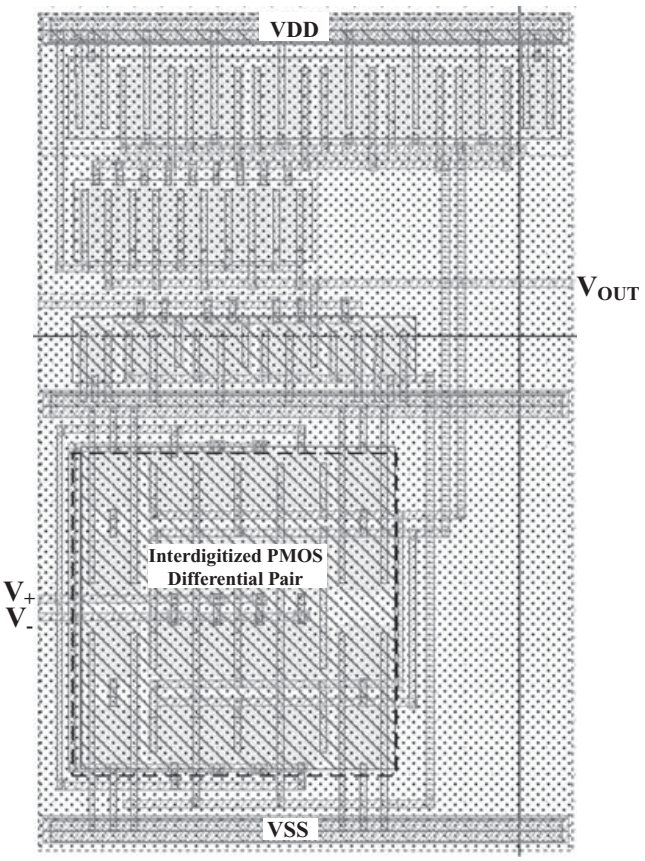


Figure 3.12 Layout of the opamp shown in Figure 3.10.

3.3.2 Current Mirror

The current mirror formed by M_1, M_2, and M_3 in the voltage reference circuit in Figure 3.6 has two functions, acting as the current source to the BJTs and acting as the current source to the β-multiplier. It further forms the output stage of the voltage reference circuit by copying the PTAT current generated by the β-multiplier to R_2, which will convert the PTAT current to a PTAT voltage and add to the CTAT voltage V_{BE_3} to generate a near-zero *TC* reference voltage. If I_3 is not identical to I_1 and I_2 due to a non-ideal current mirror, a temperature compensation error could result. Similarly, if there is a difference between I_1 and I_2, the PTAT current generated by the β-multiplier may not be the same as calculated, and thus causes temperature compensation error. The simple current mirror as shown in Figure 3.13(a) is able to accurately copy the current when all the transistors are operating in saturation mode, and their V_{GS} are the same, and the channel length modulation effect is being neglected. Note that sufficient supply voltage headroom is required to ensure the accuracy of the current mirror. The opamp based β-multiplier bandgap voltage reference circuit has a supply voltage headroom equal to $V_{DS,sat}$ for low supply voltage application. In this case, the simple current mirror circuit can only accurately copy the current within a limited current range and supply voltage range, disregarding all transistors being biased in saturation and their V_{GS} being the same. This is due to the adverse effects of the channel length modulation on the limited output impedance,

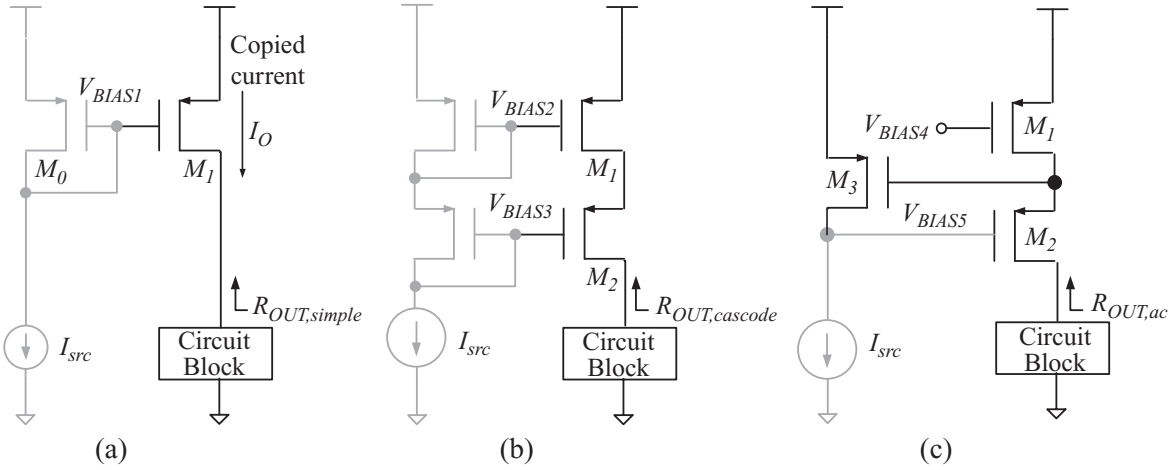


Figure 3.13 Output impedance by of (a) simple, (b) cascode, and (c) active biased current mirrors.

which will in turn limit the temperature compensation accuracy of the voltage reference circuit discussed in Section 3.2.1.

Figure 3.13(a) shows the output stage of the simple current mirror. The output transistor impedance of this simple current mirror is formed by the channel resistance R_{SD_1} of the output PMOS transistor M_1 in Figure 3.13(a). Thus we have the output resistance of the simple current mirror given by

$$R_{OUT,simple} = R_{SD_1}. \tag{3.23}$$

The classical solution to increase the output resistance is to use cascode current mirror architecture due to their simple design and impressive output impedance enhancement result. Two types of cascode architectures are shown in Figure 3.13(b) and (c).

Consider the simple cascode current mirror in Figure 3.13(b), where the cascode transistor M_2 acts as a source follower which regulates the drain voltage of M_1. The gain of M_2 determines how well the drain of M_1 is regulated. As the output voltage at $R_{OUT,cascode}$ changes, the voltage at the source of M_2 and drain of M_1 remains relatively unchanged. The drain current remains constant since there is no change in the gate, source, or drain voltages of M_1. The output impedance of this simple cascode current mirror is given by

$$R_{OUT,cascode} = (1 + g_{m_2} R_{SD_1}) R_{SD_2}. \tag{3.24}$$

This output impedance equals the intrinsic gain of the cascode transistor multiplied by the output impedance of the transistor that connects it to the supply. Assuming $R_{SD_1}, R_{SD_2} >> 1$, we can thus approximate

$$R_{OUT,cascode} \approx g_{m_2} R_{SD_1} R_{SD_2}. \tag{3.25}$$

Compare $R_{OUT,cascode}$ with the output impedance $R_{OUT,simple}$ obtained by the simple current mirror in Figure 3.13(a), the cascode current mirror in Figure 3.13(b) has increased the output impedance by a factor of $g_{m_2} R_{SD_2}$. Obviously, the output impedance of the current mirror can be improved by cascode structure, and an arbitrary high output impedance can

be obtained by increasing the number of cascode stages. However, this will increase the complexity and the operating voltage headroom. The supply voltage headroom in Figure 3.13(a) is $V_{BIAS1} + |V_{th,p}|$, while that of the cascode current mirror in Figure 3.13(b) has increased to $V_{BIAS3} + 2|V_{th,p}|$.

The output impedance enhancement by cascode architecture can be increased without increasing the operating voltage headroom by the application of an active bias current mirror output stage architecture as shown in Figure 3.13(c). The current mirror output stage in Figure 3.13(c) includes a negative feedback loop formed by transistors M_2 and M_3. The output impedance is given by

$$R_{OUT,active} = (g_{m_3} R_{SD_3}) g_{m_1} g_{m_2} R_{SD_1} R_{SD_2}, \tag{3.26}$$

where $g_{m_3} R_{SD_3}$ is the voltage gain, with g_{m_3} and R_{SD_3} being the transconductance and output impedance of the transistor M_3. As a result, the output impedance of the current mirror in Figure 3.13(c) is at least an order of magnitude higher than that of Figure 3.13(b). This active bias current mirror has the advantage of large output impedance and a low supply voltage headroom which equals to $V_{BIAS5} + 2|V_{th,p}|$. This is the same as that of a cascode current mirror with one cascode stage. It can also accurately copy the current with improved $PSRR$. The tradeoff in using this high output impedance current mirror in voltage reference circuit is the increased circuit complexity and increased quiescent current, because of the extra transistors and voltage source that are required to obtain V_{BIAS4}.

3.3.2.1 Layout Example

The layout of a simple current mirror formed by two PMOS transistors with the schematic shown in Figure 3.13(a) is depicted in Figure 3.14. Special layout considerations, such as that applied in the resistor network layout, have been applied to mitigate the effect of process variation and device mismatch problems. The layout of the two transistors in the simple current mirror shown in Figure 3.14 has been drawn in a fingering structure. The fingers of the two dummy transistors are inter-digitized and cross-coupled with identical seperation. This helps to alleviate the sheet resistance variation aroused by geometrical variation, and thus mitigates the current mismatch problem. Furthermore, two dummy transistors, with their drain, gate, and source terminals shorted to the supply rail, have been drawn at the two ends of the layout of the current mirror. These two dummy transistors help to resolve the edge effect problem. As discussed in Section 1.5, such layout techniques are also applicable to other devices, whenever the device ratio is critical.

3.3.3 Startup Circuit

The current mirror in the opamp based β-multiplier in Figure 3.6 has two functions; to act as the current source to both the β-multiplier and the BJTs and to maintain the currents flowing through two arms of the β-multiplier as equal (i.e., to keep $I_1 = I_2$). The difference voltages at the two terminals of resistor R_1 (denoted as ΔV_R) and that of the base-emitter voltages of Q_1 and Q_2 ($\Delta V_{BE_{1,2}}$) will vary upon the currents flowing through the devices, where their I-V characteristics are not exactly the same. Due to the unmatched I-V characteristics of the

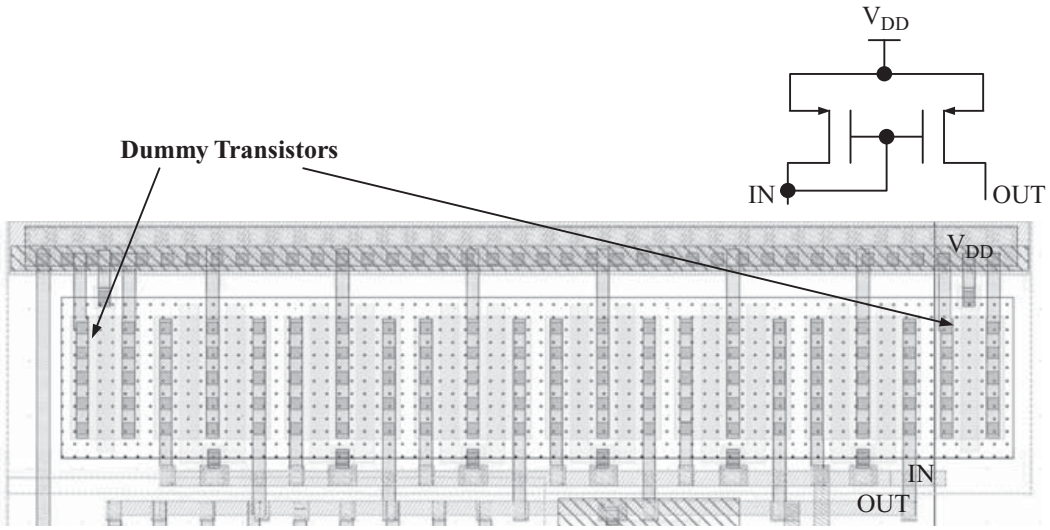


Figure 3.14 Layout example of the simple current mirror.

BJT and the resistor, the β-multiplier has two stable operation points, C and D, as indicated in Figure 3.15 assuming $S_1 = S_2$. The current I in the y-axis is the value of the current that flows through each arm of the β-multiplier and the difference voltage ΔV in the x-axis is the difference voltage under discussion, which can be ΔV_R or $\Delta V_{BE_{1,2}}$. The current mirror driven current source will be in stable operation when $V_A = V_B$ in Figure 3.6. In other words, the β-multiplier will be stable if $\Delta V_R = \Delta V_{BE_{1,2}}$.

Observe the changes in the current through the resistor I_R in Figure 3.15, which increases linearly with respect to ΔV_R starting from $\Delta V_R = 0$ at $I = 0$. On the other hand, the current

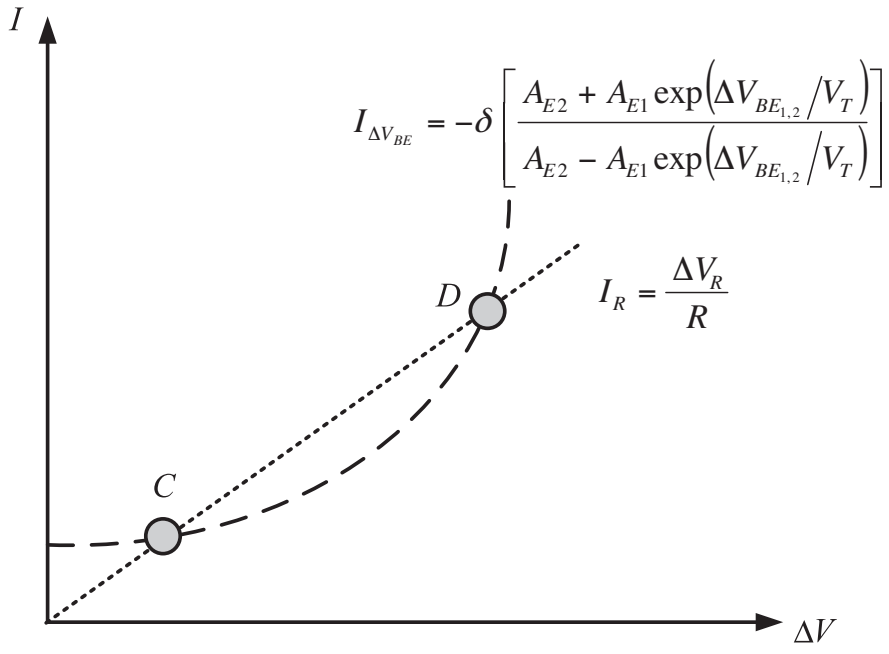


Figure 3.15 The operation points of the current mirror in the β-multiplier, where ΔV in the x-axis equals ΔV_R for the curve I_R, and equals $\Delta V_{BE_{1,2}}$ for the curve $I_{\Delta V_{BE}}$.

contributed by $\Delta V_{BE_{1,2}}$ increases exponentially with respect to the increasing $\Delta V_{BE_{1,2}}$. The exponential relationship is due to the mismatch between the currents flowing through each arm of the β-multiplier attributed to the mismatch in transistor sizes of the current mirrors (i.e., $S_1 \neq S_2$). Assume the current mismatch between the two arms of the current mirror is δ, such that the currents that flow into Q_1 and Q_2 are $I_{\Delta V_{BE_{1,2}}} + \delta$ and $I_{\Delta V_{BE_{1,2}}} - \delta$, respectively. As a result, the schematic in Figure 3.6 yields

$$\Delta V_{BE_{1,2}} = V_T \ln \frac{(I_{\Delta V_{BE_{1,2}}} + \delta)A_{E_2}}{(I_{\Delta V_{BE_{1,2}}} - \delta)A_{E_1}}, \tag{3.27}$$

where the current that flows into the two BJTs without mismatch equals $I_{\Delta V_{BE_{1,2}}}$. Re-arranging the terms in Equation 3.27 yields,

$$I_{\Delta V_{BE_{1,2}}} = -\delta \left[\frac{A_{E_2} + A_{E_1} \exp(\Delta V_{BE_{1,2}}/V_T)}{A_{E_2} - A_{E_1} \exp(\Delta V_{BE_{1,2}}/V_T)} \right]. \tag{3.28}$$

As a result, it is clear that the mismatch is between the two I-V curves, while the two I-V curves intersect at two points C and D. These two intersection points are the stable operation points of the β-multiplier. At position C, the currents flowing through the β-multiplier are too small to keep the BJTs on and the opamp of the β-multiplier will output a voltage close to V_{DD}, which will in turn bias M_1 and M_2 near the cutoff region and maintain a small I_1 and I_2 with $I_1 = I_2$. In this case, the bandgap voltage reference circuit core is not functioning. As a result, position C is regarded as a quasi-equilibrium state. This is the case when the opamp based β-multiplier powers up, where some of the MOSFETs in Figure 3.6 are biased at cutoff region and the β-multiplier and hence the whole voltage reference circuit does not yet function. At position D, identical currents $I_1 = I_2$ flow through Q_1, Q_2, and R_1. Thus, a proper reference voltage is generated. Therefore, the operation position D is regarded as an equilibrium position and the opamp based β-multiplier bandgap voltage reference circuit is said to be working normally. Clearly, to ensure normal operation of the voltage reference circuit, the operation at position D has to be guaranteed. This can be achieved by adding a startup circuit such as the one shown in Figure 3.16. The startup circuit will sense the reference voltage. If the reference voltage approaches 0 V, the startup circuit opens the loop of the self-bias β-multiplier circuit by either injecting current to or extracting current from the β-multiplier, which will upset the equilibrium of the circuit. As a result, the opamp will function to restore the equilibrium of the circuit. The operation of the opamp will generate the reference voltage. In return, the reference voltage will turn the startup circuit off and disable the interruption caused by the startup circuit through isolating the startup circuit from the bandgap core.

Two different methods are introduced in this section to accomplish the goal of injecting current into the self-bias β-multiplier circuit as shown in Figure 3.16. The first method makes use of a current source to inject a current I_{start1} to the β-multiplier, while the other method makes use of a current drain that extracts current I_{start2} from the bias of the current mirror. Even though the startup circuit can be designed to be completely electrically detached from the bandgap core during equilibrium, and hence will not affect both the static and dynamic performance of the voltage reference circuit after power up, the performance of the startup circuit does affect the settling time of the voltage reference circuit. Theoretically, a short startup time is desirable, which can save battery energy because of the extra current dissipated

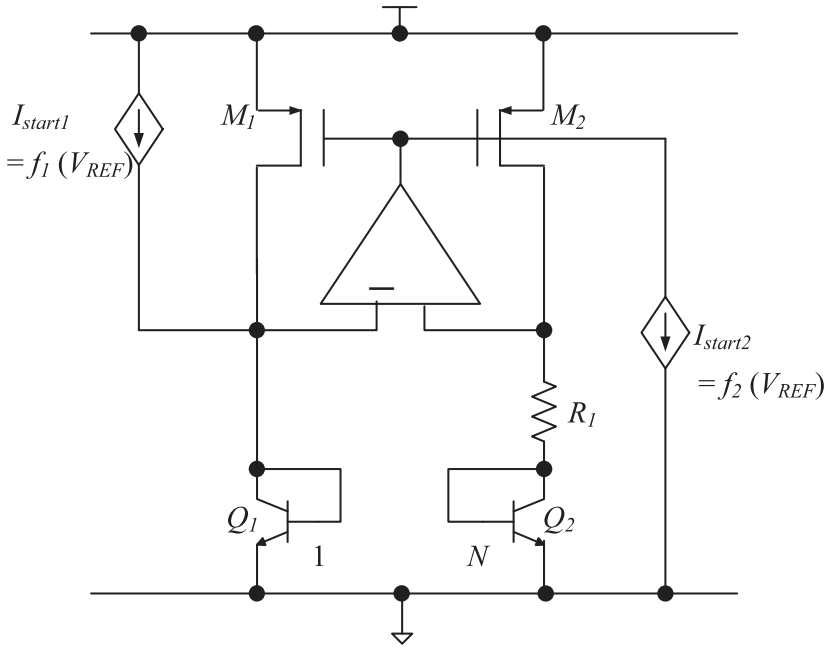


Figure 3.16 Two different startup methods for opamp based β-multiplier voltage reference circuit by current injection (I_{start1}) and current drain (I_{start2}).

during the startup period. This is especially true when I_{start1} and I_{start2} are large. Moreover, a shorter startup time can help to power up other circuits that depend on the reference voltage in the application more quickly.

When I_{start1} or I_{start2} is too small, a long startup time is required because one has to charge the parasitic capacitance for the current injection based startup circuit, or one has to discharge the gate capacitance of the MOSFET in the current mirror. On the other hand, when I_{start1} or I_{start2} is too large, an over discharged MOSFET in the current mirror, or an over charged BJT, may cause the voltage reference circuit to generate a transient high output voltage, which is not desirable in many applications, especially voltage regulator related applicatiosn, as it may cause electrical damage to the rest of the circuits in those applications. Therefore, the driving current of the startup circuit has to be carefully chosen to avoid a long startup time and high transient output voltage.

Figure 3.17 shows a typical startup circuit formed by $M_{S1} \sim M_{S3}$, R_{S_1}, R_{S_2}, and C_S for the voltage reference circuit in Figure 3.6 that uses the current draining method described by I_{start2} in Figure 3.16. When the voltage reference circuit first connects to V_{DD}, the capacitor C_S will be charged up by R_{S_1}. As a result, the input voltage to the NOT gate formed by M_{S1} and M_{S2} will be close to *GND* and forms a low input, hence outputs a high signal which turns on M_{S3}. The gate voltage of M_1, M_2, and M_3 will be brought to *GND* by the current drain M_{S3}, and thus the currents I_1, I_2, and I_3 will start to flow. The β-multiplier circuit is therefore started up. As time passes, the capacitor C_S will be charged to a voltage higher than the triggering voltage of the NOT gate formed by M_{S1} and M_{S2}. In this case, the NOT gate will output a low signal, which will bias M_{S3} to shut off. Therefore, the startup circuit will no longer affect the working of the bandgap voltage reference circuit after the startup period which is determined by the charging time of C_S through R_{S_1}. The startup delay is therefore controlled by the RC time delay of R_{S_1} and C_S. This startup delay should be adjusted to be longer than the V_{DD}

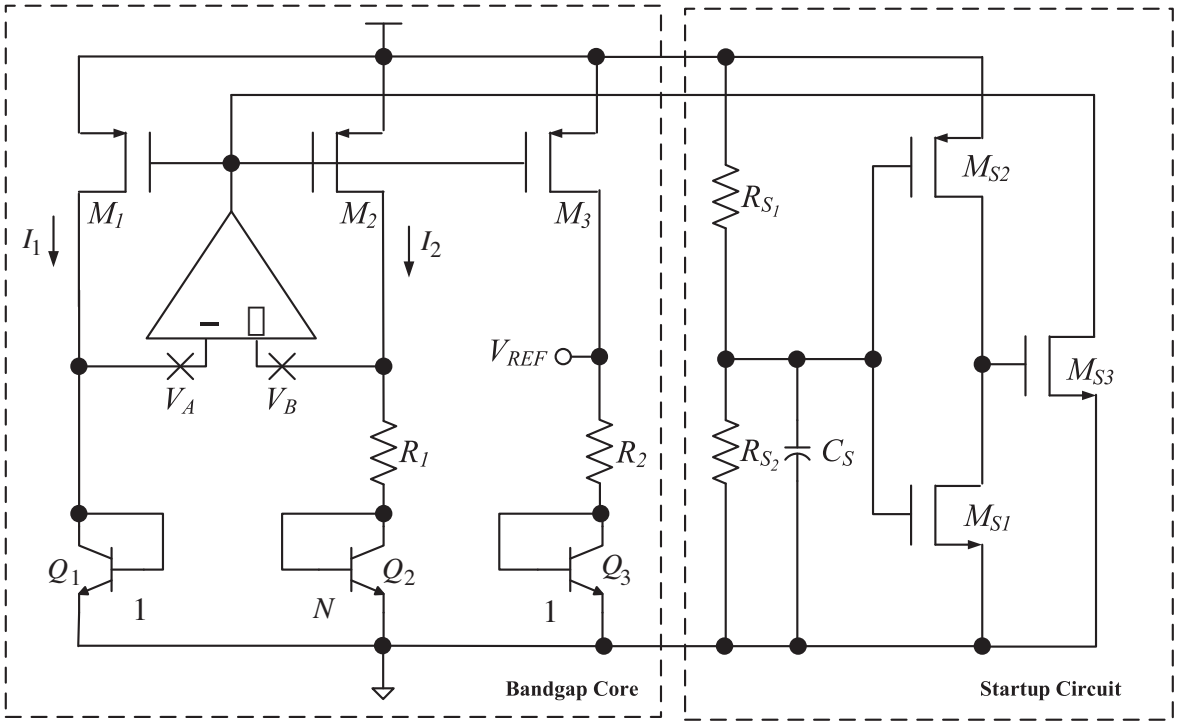


Figure 3.17 An opamp based β-multiplier bandgap voltage reference circuit with a conventional startup circuit formed by a *NOT* gate and *RC* delay network.

settling time, such as to avoid the propagation of the unstable V_{DD} to the V_{REF}. It should further be adjusted to be longer than the startup time required by the β-multiplier, such as to avoid a non-start situation.

This startup circuit will remain ineffective and does not affect the operation of the bandgap voltage reference circuit until C_S is discharged. This will be the case when the voltage reference circuit is detached from V_{DD}, such that C_S is discharged through R_{S_2}. As a result, in order to prevent excessive current being wasted by R_{S_2} when it is connected to V_{DD} through R_{S_1}, R_{S_2} will has a very large resistance. This will affect the drainage time of the startup capacitor C_S, and hence the shutdown to startup time delay. If the shutdown to startup time is shorter than the time required to drain the current from C_S, then the startup circuit won't function properly, and the voltage reference circuit may not function properly. On the other hand, if a small R_{S_2} is being used to shorten the shutdown to restart time, the quiescent current that flows through R_{S_2} will also increase and hence increase the power consumption of the voltage reference circuit.

A startup circuit with fast turn-on time and almost zero quiescent current can be achieved by detecting the change in V_{REF} instead of V_{DD}. One of such circuit is shown in Figure 3.18 which is first presented in (Luan 2001). Similar to the conventional startup circuit, there is a NOT gate formed by M_{S1} and M_{S2}. But this time, the input of the NOT gate is connected to V_{REF}. When the voltage reference circuit is in quasi-equilibrium state, $V_{REF} = 0$. As a result, the output of the NOT gate will be high, which will turn M_{S3} on. In return, M_{S3} will create a low potential to the gates of M_1, M_2, and M_3, which will startup the bandgap voltage reference circuit. In order to avoid a sudden increase of I_3, which will in turn create a larger than normal V_{REF}, M_{S3} should not change from cut-off to fully on in a short period. Therefore, a capacitor C_S has been added at the output of the NOT gate that connects to the gate of M_{S3}. The charging

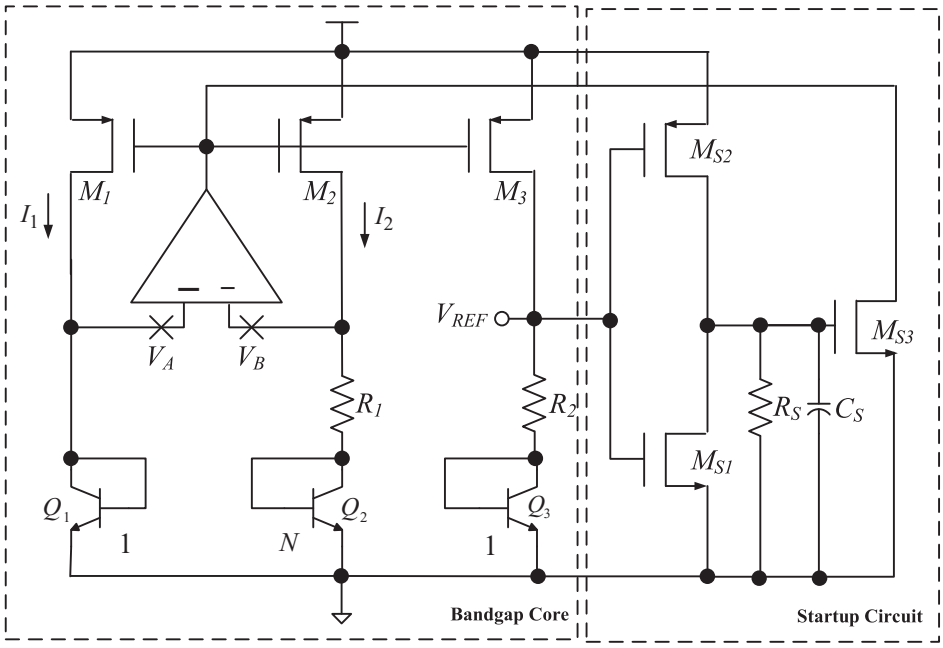


Figure 3.18 An opamp based β-multiplier bandgap voltage reference circuit with a soft startup circuit.

time of C_S (i.e. the RC delay caused by $R_S C_S$) will create a turn on delay for M_{S3}, which will turn M_{S3} on softly, that is moving slowly from cutoff to linear and then to saturation. This soft turn-on circuit will provide enough time for the bandgap voltage reference circuit to start and hence the NOT gate will go to a low output, which will turn M_{S3} off and detach the startup circuit from the voltage reference circuit. By choosing an appropriate C_S, the "softness" of the startup circuit can be altered as desired.

The drawback of the V_{REF} detection based soft startup circuit is the very low triggering voltage of the NOT gate. This is especially important for the case of sub-1V voltage reference circuit to be discussed in Chapter 6, where V_{REF} can be as low as a few hundred mV. In this case, a detector with very low triggering voltage will be required to be applied in place of the NOT gate. Such a low voltage detector is difficult to design, unstable in operation, and usually consumes a lot of power.

3.3.4 Resistor Network

The temperature compensation circuit topology of the voltage reference circuit in Figure 3.6 is based on scaling the PTAT voltage $\Delta V_{BE_{1,2}}$ by the V-I and I-V conversion ratio through resistors R_1 and R_2, respectively, and adding this PTAT voltage to the CTAT voltage V_{BE}. As discussed in Section 1.4, the implementation of resistors is process dependent and sensitive to temperature variation. Since the resistors are the largest components in the overall bandgap voltage reference circuit layout, any layout technique to improve the accuracy of the fabricated resistors will cause a significant impact on the silicon size and thus the implementation cost of the voltage reference circuit. Fortunately, it is the resistor ratio, R_2/R_1, in Equation 3.14 that is significant for the scaling of the PTAT voltage $\Delta V_{BE_{1,2}}$. As a result, it is the mismatch

problem of the resistor pair, but not the absolute resistances of the resistor pair, that is the major concern. We discussed in Section 1.4 that the inter-digitized and cross-coupled layout as shown in Figure 1.22 can be applied to reduce the matching error of the resistors and hence reduce the variation of the resistor ratio. The details of the opamp based β-multiplier bandgap voltage reference circuit output voltage variation caused by resistor ratio variation, the precautions needed to reduce such variation, and the post-processing techniques to remedy the accuracy problem caused by such variation, will be discussed in Section 4.4. Last but not least, even though it is the resistor ratio that is the major consideration, the temperature compensation topology, and the individual resistor values do affect the biasing currents to the BJTs. Therefore, their variations should be tightly controlled in order to lower the yield lost of the voltage reference circuit due to biasing the BJT in non-active regions.

3.3.5 Bipolar Transistor

The BJTs implemented in standard CMOS processes are usually provided with a standard unit cell from the foundry, and the SPICE model of the BJT implemented in the CMOS process is not scalable where the foundry can only provide SPICE characterization of the standard size BJT, which we shall call the unit size. As a result, both the circuit design and layout will use this standard unit size device and its associated layout. Otherwise, we would be designing with unknown device parameters, and it would be very difficult if not impossible to achieve a working circuit at the end of the design. Furthermore, with respect to the CMOS process under consideration in this book, we noted that the NPN and PNP transistors implemented by this CMOS process as discussed in Section 1.1 do not have the same design freedom. The PNP transistor has a design constraint that the collector node of the transistor is connected to the P-substrate, and thus it is connected to the most negative voltage in the CMOS circuit. In other words, the PNP transistors cannot be cascode, that is, they cannot be stacked. While it does not constitute a design problem in this Chapter, later Chapter will show that PNP transistors cannot be applied to some particular voltage reference circuit topologies. Of course, the NPN transistor also has its own problems, as will be discussed in Section 4.1.1.4. Nevertheless, we shall apply NPN transistors in almost all voltage reference circuits whenever applicable because of the larger β of this transistor when compared to the that of the PNP transistor.

3.3.5.1 Layout Example

The layout of a pair of the NPN transistors with area size ratio $N = 8$ is shown in Figure 3.19. Special layout considerations have been applied to mitigate the effect of process variation and device mismatch of the bipolar transistor pair. Note that unit size bipolar transistor with pre-defined layout from the foundry is usually applied in the voltage reference circuit. As a result, it will be difficult to apply inter-digitization and cross-couple layout techniques to alleviate the device mismatch problem. With pre-defined layout, and large area ratio between the device pair, centroid symmetric layout technique as shown in Figure 3.19 can be applied to lower the parameter variation problem due to geometric and doping variation, and thus enhance the parameter matching between the transistor pair fabricated in one silicon to that of another silicon.

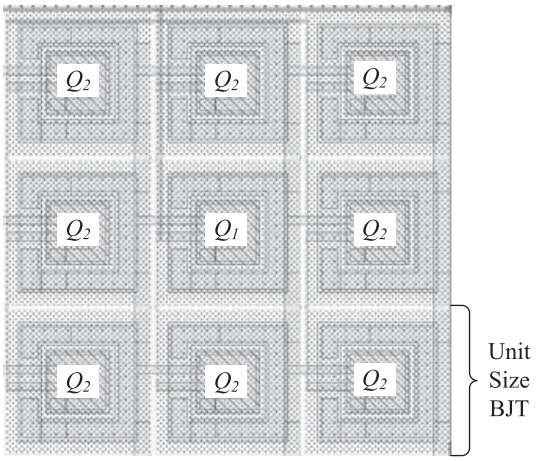


Figure 3.19 Centroid based layout of BJTs.

3.4 Complete Layout

The complete silicon layout of the opamp based β-multiplier bandgap voltage reference circuit in Figure 3.11 is shown in Figure 3.20. It can be observed that the layout is as simple as putting all layouts in Figures 3.12, 3.14, 3.19, and 1.22 together. Overall care has to be taken in the isolation of one circuit block by guard rings to the others to ensure successful implementation of the voltage reference circuit.

3.5 Summary

Although the energy gap of the silicon is a temperature dependent function, where the temperature dependency is a result of the lattice expansion and contraction in response to the temperature, the temperature coefficient of the energy gap of the silicon is so small in the temperature region of interest that the Widar bandgap voltage reference circuit is widely used to obtain a stable reference voltage for a large variety of CMOS circuits. The bandgap voltage reference circuit makes use of a simple temperature compensation technique to generate bandgap voltage with a low temperature coefficient, as has been presented in this chapter. A near-zero *TC* reference voltage is obtained from the weighted sum of two thermal voltages with complementary thermal properties. While the Wildar bandgap voltage reference circuit is

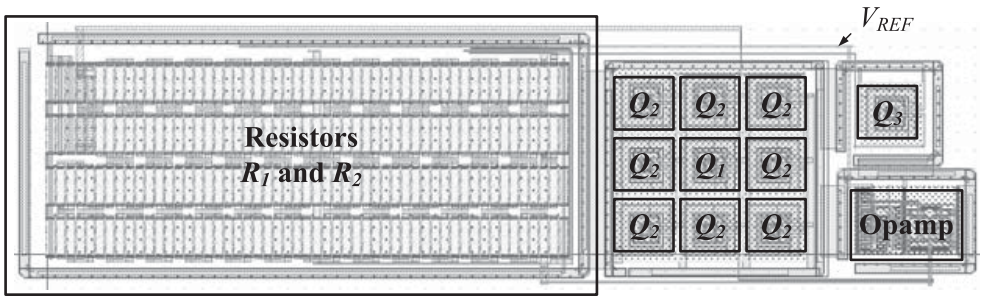


Figure 3.20 Silicon layout of the opamp based β-multiplier bandgap voltage reference circuit with schematic given in Figure 3.6.

simple, its performance is limited. The bandgap voltage reference circuits which make use of BJT as the temperature sensitive element always assume the base current is negligible because the BJT current gain β is very high. In reality, β is finite and the base current of the BJT will reduce the accuracy of the compensation, and it is not easy to include this effect in the analysis. When the reference circuit operates from current derived from a current source obtained from the power supply, this current changes along with the power supply variation. Therefore, the "conventional" opamp based β-multiplier bandgap voltage reference circuit that makes use of the β-multiplier circuit to mitigate the power supply variation problem is introduced. This self-biasing circuit mitigates the problem under consideration by generating the current source from the reference voltage, instead of generating the current from the power supply directly. The current is derived from the base-emitter difference voltage and a resistor. This current has very high immunity to supply voltage variation as long as the transistors remain forward-active. In addition, the bias current to the transistors in a conventional opamp based β-multiplier bandgap voltage reference circuit is proportional to the absolute temperature. The nonlinearity error in V_{BE} is independent to the temperature but is found to be smaller when the bias current of the transistor is PTAT. Therefore, the resulting reference voltage has a smaller nonlinear temperature error.

Almost all the necessary knowledge for the design and implementation of temperature independent reference voltage circuit can be acquired by studying the opamp based β-multiplier bandgap voltage reference circuit. The theory, design, and implementation of all the major circuit blocks of the opamp based β-multiplier bandgap voltage reference circuit are presented in detail in this chapter, together with a layout example of each circuit block, where the circuit blocks are divided into opamp, current mirror, bipolar transistors, resistor network, and startup circuit. The roles of these circuit blocks on the voltage reference circuit and their design concerns have been reviewed. In the next chapter, we shall discuss various error sources of the opamp based β-multiplier bandgap voltage reference circuit that limit the performance of the circuit, and the typical circuit techniques used to mitigate the effects of those error sources. The subsequent chapters will present voltage reference circuits with different temperature sensitive elements and circuit topologies. In particular, Chapter 6 will present a voltage reference circuit that can work with sub-1V V_{DD}, and generates sub-1V reference voltage. Chapter 7 will present voltage reference circuits that perform high order temperature compensation to achieve reference voltage with low TC. Finally, Chapter 8 will present a voltage reference circuit without resistors for reduced silicon size and sensitivity to process variation.

3.6 Exercises

Exercise 3.1 *Figure 3.21 is the schematic of a bandgap voltage reference circuit. Assume $R_1 = R_2$, the opamp is perfect, and the emitter area ratio of Q_1 to Q_2 is $1 : N$, show that V_{REF} can be expressed in the form of $V_{BE_2} + M\Delta V_{BE_{2,1}}$ and find M where M depends on R_1 and R_3 only.*

Exercise 3.2 *Figure 3.22 is the schematic of a bandgap voltage reference circuit. Assume $R_1 = R_2$, the opamp is perfect, and the emitter area ratio of Q_1 to Q_2 is $1 : N$, show that V_{REF} can be expressed in the form of $V_{BE_3} + M\Delta V_{BE_{1,2}}$ and find M where M depends on R_1 and R_3 only.*

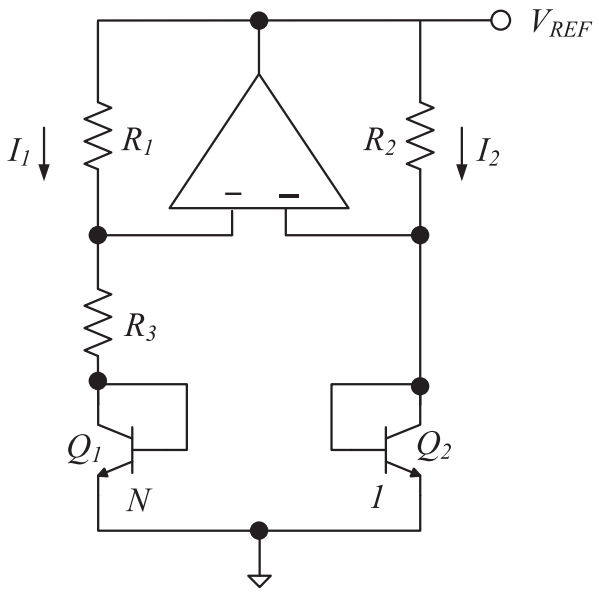


Figure 3.21 Schematic of a bandgap voltage reference circuit for Exercise 3.1.

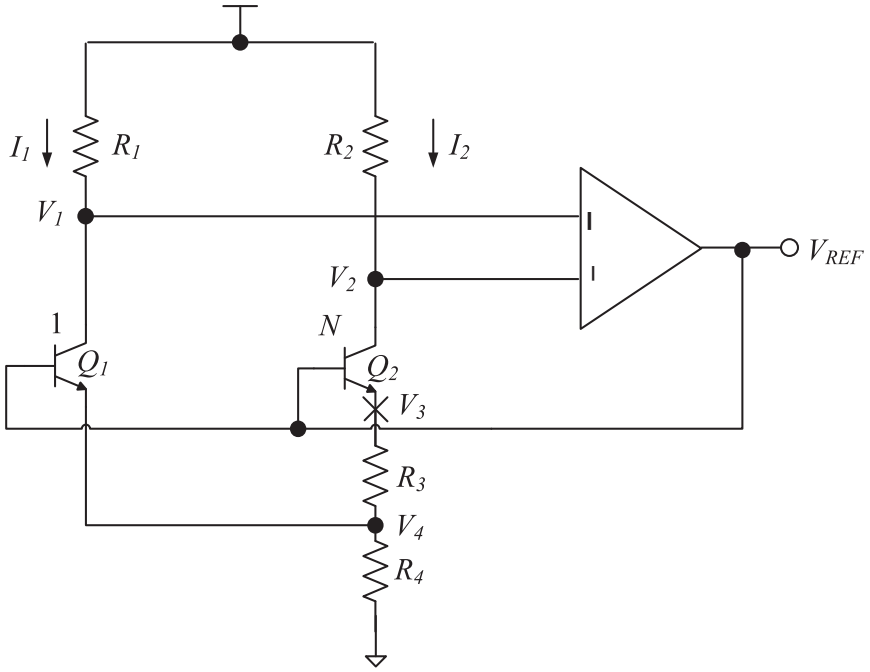


Figure 3.22 Schematic of a bandgap voltage reference circuit using active biased BJTs for Exercise 3.2.

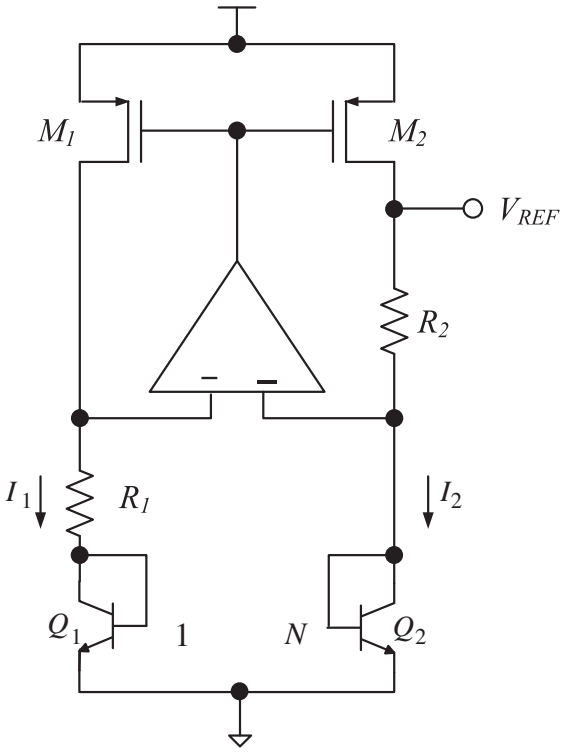


Figure 3.23 Schematic of a bandgap voltage reference circuit for Exercise 3.3.

Exercise 3.3 *Consider the bandgap voltage reference circuit in Figure 3.23. Given the emitter area ratio of bipolar transistors Q_1 to Q_2 is $1 : N$, and the $(\frac{W_2}{L_2})/(\frac{W_1}{L_1}) = m$; (a) Find the expression of V_{REF} in terms of V_T, V_{BE_2}, R_1, R_2, N, and m. (b) Find the resistor ratio R_2/R_1 to obtain a zero TC $V_{REF} = 300$ K with $m = 1$ and $N = 8$.*

Exercise 3.4 *Consider the bandgap voltage reference circuit in Figure 3.24. Given the emitter area ratio of bipolar transistors Q_1 to Q_2 is $1 : N$, and $(\frac{W_2}{L_2})/(\frac{W_1}{L_1}) = m$;*

1. *Find the expression of V_{REF} in terms of V_T, V_{BE_2}, R_1, R_2, R_3, N, and m.*
2. *Find the resistor ratio R_2/R_1 to obtain a zero TC V_{REF} at 300 K with $m = 1$ and $N = 8$.*
3. *Discuss the functionality of R_3, where $R_3 = mR_2$.*
4. *A resistor like R_3 in Figure 3.24 is missing in Figure 3.23, what kind of problem will the reference voltage in Figure 3.23 suffer, when compared to that of Figure 3.24?*

Exercise 3.5 *Derive with detailed steps the open loop gain of the opamp shown in Figure 3.10 to obtain*

$$A_v \approx g_{m_2} \cdot g_{m_7} \frac{r_{ds_2} r_{ds_4} r_{ds_6} r_{ds_7}}{(r_{ds_2} + r_{ds_4})(r_{ds_6} + r_{ds_7})} \tag{3.29}$$

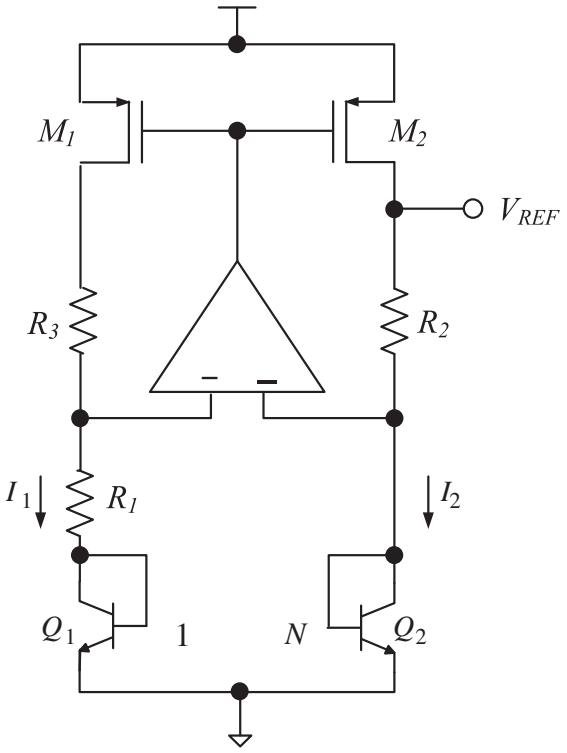


Figure 3.24 Schematic of a modified bandgap voltage reference circuit from Figure 3.23 for Exercise 3.4.

Exercise 3.6 *The maximum current that can pass through a conductor without blowing up is given by*

$$I_{max} = c \times d^{3/2},$$

where d is the diameter of the wire in inches, and c is a material dependent constant. In our case, $c = 7585$ *for a fuse implemented by the METAL 2 layer. Consider a fuse wire with length and width both equal to* $1.8\ \mu m$*, compute the current required to blow up this fuse.*

Exercise 3.7 *Figure 3.25 shows a simple startup circuit where the* V_{REF} *is the input to the startup circuit obtained through resistive divider obtaining* 95% *of the voltage, and a RC network obtains a delayed input signal.*

1. *Derive the equation that governs the startup time delay.*
2. *What is the implication/consideration for the startup circuit to achieve the same startup delay with the resistor R chosen to be* $10\ k\Omega$ *and* $100\ k\Omega$ *respectively?*

Exercise 3.8 *Over-temperature protection circuit: Consider a NPN transistor that is driven by a constant current source* I_1 *as shown in Figure 3.26, such that* V_{BE_1} *follows Equations 1.4 and 1.8. Note that* V_{BE_1} *is linearly related to temperature. This property can be used to construct an over-temperature protection circuit. The over-temperature protection circuit detects the operating temperature of a circuit. When the operating temperature of the silicon*

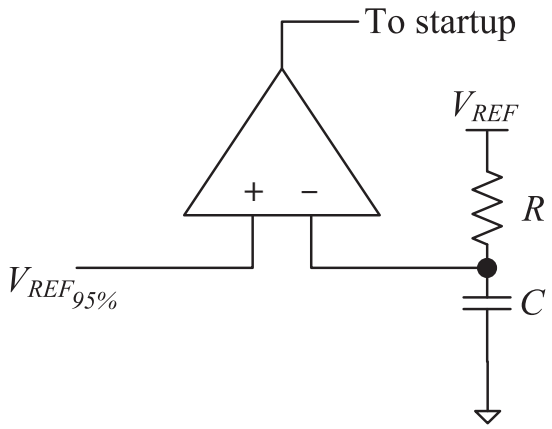


Figure 3.25 Analysis of the startup circuit of voltage reference circuit for Exercise 3.7.

becomes higher than a predefined temperature (T_{det}), an alarm signal will be generated at V_{OUT}. Consider the over-temperature protection circuit in Figure 3.26. Assume the over-temperature protection circuit closes the switch when the operating temperature is greater than $T_H = V_{det} + \Delta T$, and the switch will be open again when the operating temperature is smaller than $T_L = V_{det} - \Delta T$:

1. *Derive the voltage at the negative input terminal of the opamp in Figure 3.26 with and without the switch being closed.*
2. *Derive the hysteresis temperature $T_H - T_L$ with respect to I_1, R_1, and the temperature coefficient of V_{BE_1} (TC_{VBE}), and the temperature coefficient of V_1 (TC_{V1}).*
3. *The switch helps to create a detection/output signal hysteresis. Draw the output signal V_{OUT} versus temperature with the temperature swinging between $T_{det} - \Delta T - 10\ ^\circ\text{C}$ to $T_{det} + \Delta T + 10\ ^\circ\text{C}$ with $V_{DD} = 3$ V, and a perfect opamp.*

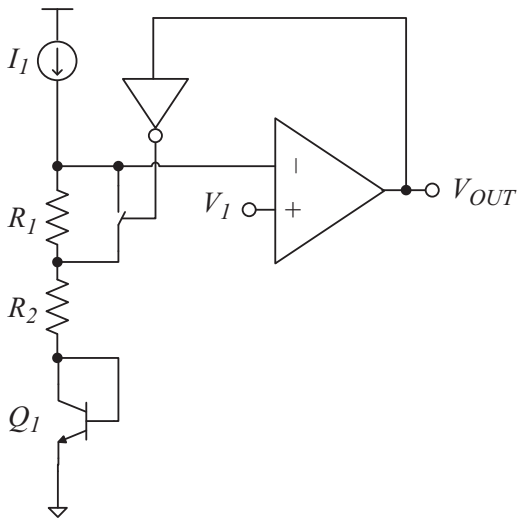


Figure 3.26 Over-heating protection circuit analysis for Exercise 3.8.

Exercise 3.9 *Based on V_{REF} derived in Section 3.2.2,*

1. *Derive the sensitivity $S_{I_{Q_1}}^{V_{REF}}$ of V_{REF} towards I_{Q_1} variation.*
2. *Derive the sensitivity $S_{M}^{V_{REF}}$ of V_{REF} towards varying M.*
3. *If the transistor Q_1 is to be trimmed after fabrication to obtain V_{REF} with high accuracy, determine and discuss which parameters (M, or I_{Q_1}) should be trimmed.*

References

Hastings, A. (2001) *The Art of Analog Layout*. Prentice Hall.

Luan, V. (2001) Low noise high PSRR bandgap with fast turn-on time, US Patent Number 6278320.

Widlar, R.J. (1971) New developments in IC voltage regulators. *IEEE Journal of Solid-State Circuits*, **6** (1), 2–7.

You, F., Embabi, S.H.K. and Sanchez-Sinencio, E. (1997) Multistage amplifier topologies with nested Gm-C compensation. *IEEE Journal of Solid-State Circuits*, **32** (12), 2000–11.

4

Error Sources in Bandgap Voltage Reference Circuit

The opamp based β-multiplier bandgap voltage reference circuit in Figure 3.4 discussed in Chapter 3 is derived with ideal components, such that the opamp can attain an infinite open loop gain, and zero input offset to maintain the voltages at the input terminals to be identical in the close loop circuit. Furthermore, the transistors M_1, M_2, and M_3 in Figure 3.4 are assumed to be perfectly matched, such that the currents at each branch of the current mirror are identical to $I_1 = I_2 = I_3$. Moreover, the output current I_{LOAD} from the bandgap voltage reference circuit is assumed to be zero and thus $I_3 = I_{BE_3}$. In addition, Q_1 and Q_2 are assumed to have the same I_S and β. Furthermore, the BJTs are assumed to have large β, such that I_B is small enough to be ignored in the circuit without affecting the analysis. Last but not least, the resistor ratio R_2/R_1 is assumed to be fabricated with high accuracy. With the above assumptions, the output voltage of the opamp based β-multiplier bandgap voltage reference circuit is given by Equation 3.12. Unfortunately, the above assumptions are void in reality and the consequences of components imperfection impose compensation errors and degrade the stability of the voltage reference circuit to different extents. Figure 4.1 shows the variation of the output voltages obtained from three different samples of the opamp based β-multiplier bandgap voltage reference circuit simulated with different process corners. It can be observed that even within the same wafer, each fabricated voltage reference circuit can have a different temperature coefficient, and different output voltage at $T_{(nom)}$. The application of such a voltage reference circuit will severely impact the performance of the overall system. Note that such output voltage variation problem is the sum of individual effects caused by each non-ideal circuit component and block, which will be discussed in the following sections. The worst case analysis of the adverse effect of these non-ideal circuit components and blocks on the reference voltage and other performance parameters of the voltage reference circuit will be analytically derived. We shall also review some of the possible solutions to mitigate these adverse effects caused by the non-ideal circuit components and blocks.

4.1 Non-Ideal Opamp

The performance of the opamp based β-multiplier bandgap voltage reference circuit depends on the performance of the opamp. However, the practical opamp deviates from the ideal opamp

CMOS Voltage References: An Analytical and Practical Perspective, First Edition. Chi-Wah Kok and Wing-Shan Tam.
 Published 2013 by John Wiley & Sons Singapore Pte. Ltd.

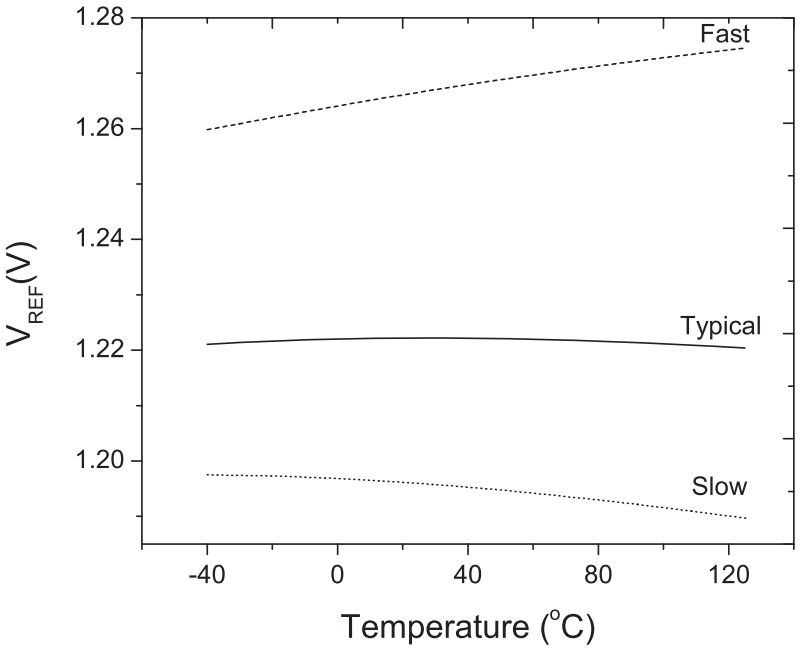


Figure 4.1 Variation of the output voltage of the bandgap voltage reference circuit simulated with different process corners.

in many ways. In the following, we shall consider the effect of opamp input offset voltage, limited open loop gain, limited $PSRR$, and limited line regulation on the performance of the bandgap voltage reference circuit. We shall also consider possible methods to alleviate their adverse effects on the voltage reference circuit.

4.1.1 Input Offset Voltage

Practical opamp suffers from the input offset voltage problem (Section 3.3.1). As a result, the bandgap voltage reference circuit in Figure 3.4 will operate with $V_A \neq V_B$. In this case, an error voltage will be induced to ΔV_{BE} and affect the performance of the temperature compensation. The non-ideal opamp suffering from input offset problems can be modeled as having an additional voltage source, denoted as the input offset voltage of the non-ideal opamp, V_{OS}, acting on the inverted input terminal of the ideal opamp as shown in Figure 4.2. The V_{OS} is super-imposed onto the voltage node V_A, and hence ΔV_{BE}. The output voltage of the bandgap voltage reference circuit in Figure 4.2 is now given by

$$\begin{aligned} V_{REF} &= \frac{R_2}{R_1} V_T \ln N + V_{BE_3} + \frac{R_2}{R_1} V_{OS} \\ &= V_{REF-CONV} + \Delta V_{REF,OS}, \end{aligned} \tag{4.1}$$

where $V_{REF-CONV}$ is defined in Equation 3.13 with $M = \frac{R_2}{R_1} \ln N$, and $\Delta V_{REF,OS} = \frac{R_2}{R_1} V_{OS}$. Assume the resistors R_1 and R_2 are temperature insensitive, Equation 4.1 implies that the

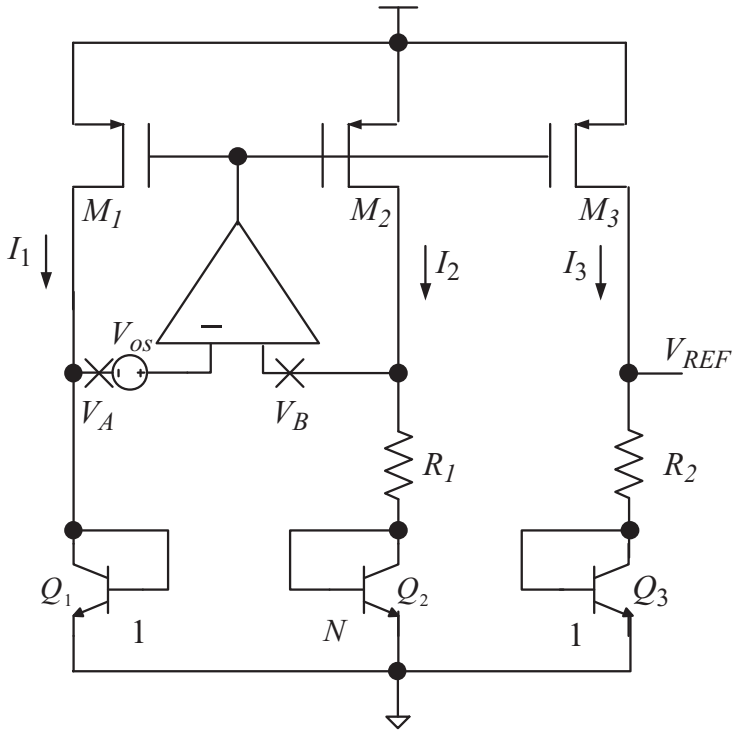


Figure 4.2 Bandgap voltage reference circuit with non-ideal opamp. An input offset voltage is observed at the negative input terminal of the opamp.

voltage reference circuit affected by the opamp input offset voltage problem will achieve a near-zero TC reference voltage under exactly the same condition as that of the voltage reference circuit in ideal condition. The opamp input offset voltage will only affect the static performance of the circuit, that is the nominal reference voltage. A typical opamp has an input offset voltage in the range of $5 \sim 20$ mV. With $R_2/R_1 = 9.24$ as derived in Equation 3.14, the variation in the output voltage given by Equation 4.1 will be in the range of $46.2 \sim 184.8$ mV, which yields an average $V_{REF} = 1.23 + (0.1848 - 0.0462)/2 = 1.2993$ V and the variation of V_{REF} equals $\pm 5.33\%$. In other words, $V_{REF} = 1.2993 \pm 0.0693$ V for voltage reference circuit suffers from opamp input offset voltage problem.

The output voltage variation of an opamp based β-multiplier bandgap voltage reference circuit can be reduced by using an opamp with small input offset voltage. A method to reduce the input offset voltage of an opamp is to use large and better layout-matched input differential transistor pair. Note that the large gate area and short gate length of the input differential transistor pair can help to reduce the input offset voltage (Allen and Holberg, 2003). Chopper stabilized circuit can also be applied to completely eliminate the input offset voltage of the opamp (Roh and Nair, 2002). However, such a circuit requires a clock signal and hence the bandgap voltage reference circuit will suffer from the switching noise coupled from the clock signal. The switching noise problem limits the application of the bandgap voltage reference circuit due to the higher overall noise level of the reference voltage. In the following, we shall review several practical circuit techniques to alleviate the reference voltage variation caused by the opamp input offset voltage problem.

4.1.1.1 Increasing the Transistor Emitter Area Ratio

A number of circuit techniques have been proposed to alleviate the nominal reference voltage variation caused by the opamp input offset voltage problem. As observed from Equation 4.1, reducing the resistor ratio R_2/R_1 will help suppress the error term $\frac{R_2}{R_1}V_{OS}$. Derived in Equation 3.12, $\frac{R_2}{R_1} = \frac{\partial V_{BE_3}}{\partial T}/(\ln(N)\frac{\partial V_T}{\partial T})$. Therefore, increasing the bipolar transistor emitter area (A_E) ratio from $1:N$ to $1:N_1$ will decrease the resistor ratio R_2/R_1. In this case, Equation 1.14 can be rewritten using N_1

$$\Delta V_{BE_{1,2}} = V_T \ln(N_1). \tag{4.2}$$

Assume $I_1 = I_2 = I_3$, the reference output voltage of this new bandgap voltage reference circuit is given by

$$\begin{aligned} V_{REF} &= \frac{R_2}{R_1} V_T \ln(N_1) + V_{BE_3} + \frac{R_2}{R_1} V_{OS} \\ &= V_{REF-CONV} + \Delta V_{REF,OS}, \end{aligned} \tag{4.3}$$

with $M = \frac{R_2}{R_1}\ln(N_1)$, and $\Delta V_{REF,OS} = \frac{R_2}{R_1}V_{OS}$. Note that a near-zero TC reference voltage is obtained with $M = 19.22$. Thus, by comparing with Equation 3.12, the resistor ratio $\frac{R_2}{R_1}$ term in Equation 4.3 is $\frac{\ln(N)}{\ln(N_1)}$ times smaller, and hence the ΔV_{REF} induced by V_{OS} is also reduced by a factor of $\frac{\ln(N)}{\ln(N_1)}$.

4.1.1.2 Increasing the Transistor Emitter Current Ratio

Instead of using a larger BJT emitter area ratio, such that the transistor emitter area ratio of $A_{E_1} : A_{E_2}$ is kept at $1:N$, the same reduction on $\Delta V_{REF,OS}$ induced by the opamp input offset voltage problem can be achieved by increasing the current mirror current ratio of $I_1 : I_2 : I_3$ from $1:1:1$ to $1:\frac{N}{N_1}:1$, such that

$$\begin{aligned} \Delta V_{BE_{1,2}} &= V_T \ln\left(\frac{I_1}{J_S A_{E_1}}\right) - V_T \ln\left(\frac{I_2}{J_S A_{E_2}}\right) \\ &= V_T \ln\left(\frac{I_1}{I_2}\frac{J_S A_{E_2}}{J_S A_{E_1}}\right) \\ &= V_T \ln(N_1). \end{aligned} \tag{4.4}$$

As observed in Equation 4.4 which has the same form as that of Equation 4.2, and hence V_{REF} will be obtained by Equation 4.3 in a similar manner. It is expected that the performance of the voltage reference circuit obtained from the increased current mirror ratio will have the same performance as that obtained from the voltage reference circuit with an increased BJT emitter area ratio, at least in theory. This, however, has both pros and cons. Since BJT is a large device in silicon layout, as a result increasing the emitter area ratio of the BJT pair will inevitability increase the size of the overall silicon area of the voltage reference circuit. Increasing the current ratio of the current mirror formed by PMOS transistors does not have such a large impact on the silicon area when compared to that of increasing the emitter area

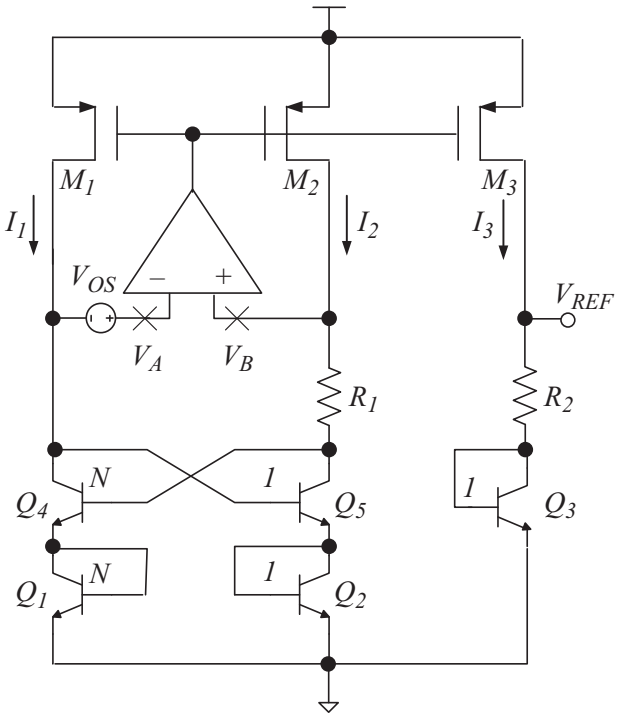


Figure 4.3 Application of cascode bipolar transistors to reduce the opamp offset voltage effect.

raio of the BJT pairs. However, increasing the current mirror current ratio does result in a higher channel length modulation effect hazard. In both cases, the collector current density ratio between the BJT pair is increased from N to N_1. As a result, the current consumption is increased. Furthermore, the $\Delta V_{BE_{1,2}}$ is subject to the finite β effect of the transistors and thus introduces another error source to the bandgap voltage reference circuit, which will be discussed in Section 4.3.3.

4.1.1.3 Cascode Cross-Coupled BJTs

One method to increase the effective bipolar transistor emitter area ratio is to use a cascode cross-coupled bipolar transistor current mirror as shown in Figure 4.3. Compared to the conventional opamp based β-multiplier bandgap voltage reference circuit as shown in Figure 3.4, a pair of cross-coupled bipolar transistors Q_4 and Q_5 are connected to the bipolar transistors Q_1 and Q_2, respectively in a cascode form. The opamp based β-multiplier regulates $I = I_1 = I_2 = I_3$. The cascode transistors Q_4 and Q_5 will not affect the magnitudes of the currents I_1 and I_2 as compared to that of the conventional opamp based β-multiplier voltage reference circuit in Figure 3.4. However, the extracted PTAT ΔV_{BE} voltage will depend on the emitter area ratio of Q_1, Q_2, Q_4 and Q_5. The detailed analysis is given by

$$\begin{aligned} V_A &= V_{CE_4} + V_{BE_1} \\ &= V_{B_5} - V_{E_4} + V_{BE_1}, \end{aligned}$$

and

$$\begin{aligned} V_B &= I_2R_1 + V_{CE_5} + V_{BE_2} \\ &= I_2R_1 + V_{B_4} - V_{E_5} + V_{BE_2}. \end{aligned}$$

The opamp clamps $V_A + V_{OS} = V_B$. Thus

$$\begin{aligned} V_A + V_{OS} &= V_B, \\ V_{B_5} + V_{OS} &= I_2R_1 + V_{B_4} \\ V_{BE_5} + V_{BE_2} + V_{OS} &= I_2R_1 + V_{BE_4} + V_{BE_1} \\ I_2R_1 &= V_{BE_5} - V_{BE_4} + V_{BE_2} - V_{BE_1} + V_{OS} \\ &= V_T \ln(N) + V_T \ln(N) + V_{OS} \\ &= V_T \ln(N^2) + V_{OS} \\ I_1 &= \frac{V_T \ln(N^2) + V_{OS}}{R_1}. \end{aligned} \tag{4.5}$$

Therefore,

$$\begin{aligned} V_{REF} &= I_3R_2 + V_{BE_3} \\ &= \frac{R_2}{R_1} \ln(N^2)V_T + V_{BE_3} + \frac{R_2}{R_1} V_{OS} \\ &= V_{REF-CONV} + \Delta V_{REF,OS}, \end{aligned} \tag{4.6}$$

where $M = \frac{R_2}{R_1} \ln(N^2)$ and $\Delta V_{REF,OS} = \frac{R_2}{R_1} V_{OS}$. Comparing Equations 3.12 and 4.5, we can observe that the addition of Q_4 and Q_5 will effectively increase the bipolar transistor emitter area ratio from N to N^2, which implies a 50% reduction in the resistor ratio (because of the $\ln(\cdot)$) when compared to that of the conventional opamp based β-multiplier voltage reference circuit with bipolar transistor emitter area ratio equals to $1 : N$. With $N = 8$, the resistor ratio $R_2/R_1 = 4.62$ is required to achieve near-zero TC at $T_{(nom)}$ for V_{REF} derived in Equation 4.6. As a result, the error term $\Delta V_{REF,OS}$ will also be reduced by 50%, while the actual increase in the silicon layout area for the bipolar transistor is just $2\times$ that of the conventional bandgap voltage reference circuit. As a result, the cascode cross-couple structure is an area-efficient solution to alleviate the opamp input offset voltage problem. On the other hand, the application of cascode structure will inevitability reduce the supply voltage headroom. The SPICE simulation result plotted in Figure 4.4 shows that the minimum supply voltage required to operate the circuit is 2.1 V, which is 0.7 V higher than the 1.4 V minimum V_{DD} required by the conventional opamp based β-multiplier bandgap voltage reference circuit.

4.1.1.4 Series Connected BJTs

Another method to reduce the opamp input offset voltage effect is to use a series BJT as illustrated by the circuit in Figure 4.5. The series connected BJT can increase ΔV_{BE}, which

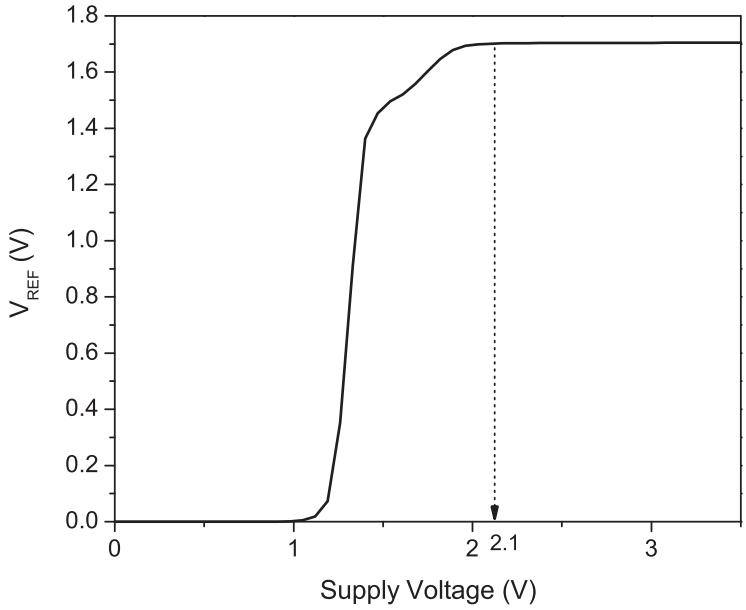


Figure 4.4 Output voltage of the bandgap voltage reference circuit in Figure 4.3 with varying supply voltage obtained by SPICE simulation.

helps to reduce the relative voltage error due to the input offset voltage of the opamp. Consider the schematic in Figure 4.5 with $I_1 = I_2 = I_4 = I_5 = 2I_3$, and $R_1 = R_3$. We can observe that

$$V_A = V_{EB_1} + V_{EB_4},$$
$$V_B = I_2 R_1 + V_{EB_2} + V_{EB_5}.$$

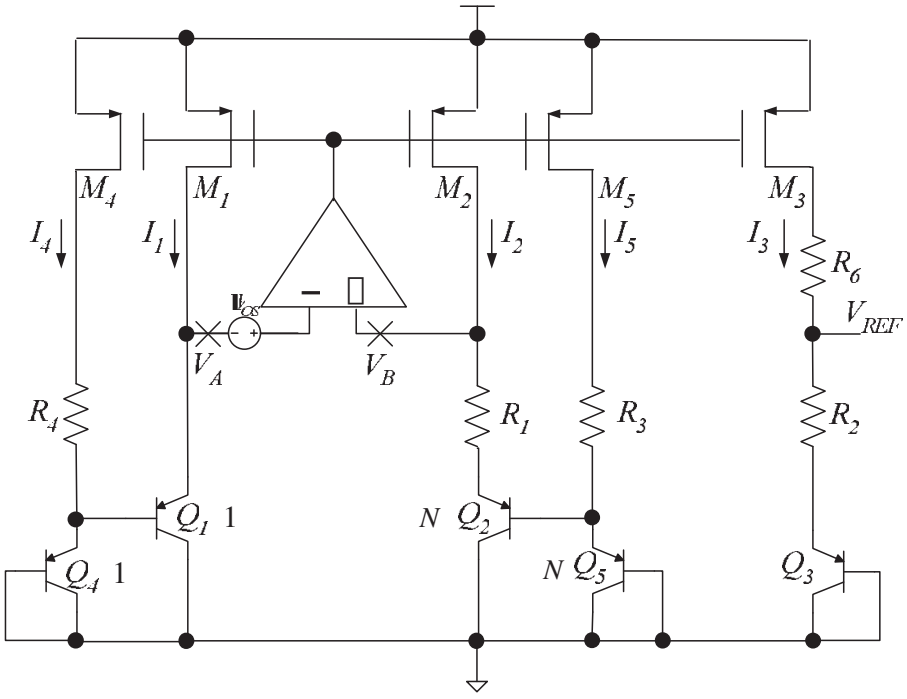


Figure 4.5 Application of series BJT to reduce the opamp offset voltage effect.

Assume the emitter area ratio of $Q_1 : Q_2 : Q_4 : Q_5$ equals $1 : N : 1 : N$. Since all BJTs are biased with the same current, we shall have $V_{BE_1} = V_{BE_4}$ and $V_{BE_2} = V_{BE_5}$. Assume the gain of the opamp is large enough such that the inputs of the ideal opamp can be considered virtually short-circuited in the close loop circuit in Figure 4.5. As a result,

$$\begin{aligned} V_A + V_{OS} &= V_B \\ V_{EB_1} + V_{EB_4} + V_{OS} &= I_2 R_1 + V_{EB_2} + V_{EB_5} \\ I_2 &= \frac{1}{R_1}(V_{EB_1} + V_{EB_4} + V_{OS} - V_{EB_2} - V_{EB_5}) \\ &= \frac{1}{R_1}(\Delta V_{EB_{1,2}} + \Delta V_{EB_{4,5}} + V_{OS}) \\ &= \frac{1}{R_1}(2V_T \ln(N) + V_{OS}). \end{aligned}$$

Note that

$$\begin{aligned} V_{REF} &= V_{EB_3} + I_3 R_2 \\ &= V_{EB_3} + \frac{I_2}{2} R_2 \\ &= V_{EB_3} + \frac{1}{2}\frac{R_2}{R_1}(2V_T \ln(N) + V_{OS}) \\ &= V_{EB_3} + \frac{R_2}{R_1} V_T \ln(N) + \frac{1}{2}\frac{R_2}{R_1} V_{OS} \\ &= V_{REF-CONV} + \Delta V_{REF,OS}, \end{aligned} \tag{4.7}$$

where $V_{REF-CONV}$ is the reference voltage of the conventional opamp based β-multiplier bandgap voltage reference circuit and $\Delta V_{REF,OS} = \frac{1}{2}\frac{R_2}{R_1} V_{OS}$ is the offset voltage of the present circuit. The $\Delta V_{REF,OS}$ in Equation 4.7 is half of that of the conventional opamp based β-multiplier bandgap voltage reference circuit depicted in Equation 4.3. Note that V_{REF} in Equation 4.7 is derived with the assumption that the base currents of Q_1 and Q_2 are negligible. If the base currents of the bipolar transistors are considered, the emitter of Q_4 will amplify the base current I_{b_1} of Q_1 as

$$I_{b_1} = \frac{I_1}{1+\beta},$$

where β is the gain of Q_1. As a result,

$$V_{BE_4} = V_T \ln\left(\frac{I_4 + \frac{I_1}{1+\beta}}{I_S}\right).$$

Similarly,

$$V_{BE_5} = V_T \ln\left(\frac{I_5 + \frac{I_2}{1+\beta}}{N I_S}\right).$$

Hence

$$\Delta V_{EB_{4,5}} = V_{EB_4} - V_{EB_5} = V_T \ln\left(\frac{I_4 + \frac{I_1}{1+\beta}}{I_S}\right) - V_T \ln\left(\frac{I_5 + \frac{I_2}{1+\beta}}{N I_S}\right)$$
$$= V_T \ln\left(\frac{I_4 + \frac{I_1}{1+\beta}}{I_5 + \frac{I_2}{1+\beta}} \times N\right).$$

If the current mirror is perfect, such that $I_1 = I_2 = 2I_3 = I_4 = I_5$, then

$$\Delta V_{EB_{4,5}} = V_T \ln N.$$

In other words, even if the base currents of the bipolar transistors are considered, the output voltage of the bandgap voltage reference circuit with series connected bipolar transistors will still be the same as that of the case of negligible base current. Nevertheless, such a circuit does have the disadvantage of a high working voltage similar to the case of cascode cross-coupled BJTs, in which both circuits require the $V_{DD(min)} = 2.1$ V, for reasons similar to the case of the cascode BJT presented in Section 4.1.1.3.

Comparing the performance of the series connected BJT bandgap voltage reference circuit (see Figure 4.5) with that of the cascode cross-coupled BJT bandgap voltage reference circuit (see Figure 4.3), it is easy to observe that both circuits consist of $2N$+2 unit size BJTs, while their output voltage variations and the $V_{DD(min)}$ are the same at $\frac{1}{2}\frac{R_2}{R_1}V_{OS} = \frac{9.24}{2}V_{OS}$ and 2.1 V, respectively. However, the cascode cross-coupled BJT circuit is considered to perform better than the series connected BJT circuit from the power consumption point of view. This is because the series connected BJT circuit has two more current paths (formed by M_4 and M_5), thus consuming higher quiescent current, at least 12 μA higher theoretically, when compared to that of the cross-coupled BJT circuit. Moreover, the additional current paths require more complicated current mirror matchings. As a result, the series connected BJT circuit is subject to a higher current mirror mismatch error which affects the accuracy of the reference voltage. Besides, the series connected BJT circuit has two more PMOS and two more resistors and thus requires a larger overall silicon layout area than that of the cross-coupled BJT circuit.

Finally, the series connected BJT bandgap voltage reference circuit requires the application of PNP transistors. The planar PNP transistor fabricated by the CMOS process under consideration in this book has the collector tied to ground. Such PNP transistors are not applicable to the cascode cross-coupled BJTs bandgap voltage reference circuit in Section 4.1.1.3. Fortunately, the collector of the PNP transistors in the series connected BJT bandgap voltage reference circuit are all connected to ground, and thus the planar PNP transistors are applicable in this case. On the other hand, the NPN transistors can be used to implement the cascode cross-coupled BJTs bandgap voltage reference circuit.

4.1.2 Limited Gain and Power Supply Rejection Ratio

Besides the input offset voltage problem, the performance of the opamp based β-multiplier bandgap voltage reference circuit is also affected by the limited open loop gain of the opamp, which may also result in $V_A \neq V_B$. Fortunately, the bandgap voltage reference circuit operates at low frequency, and it is easy to obtain an opamp with DC gain close to 100 dB. As a result, the limited open loop gain effect on the output voltage variation of the opamp based β-multiplier bandgap voltage reference circuit is comparatively much smaller than that caused by the opamp input offset problem.

The limited $PSRR$ of the opamp has the same awkward effect as that of the limited open loop gain of the opamp in β-multiplier bandgap voltage reference circuit. Fortunately, the $PSRR$ of the opamp can easily achieve 90 dB, which makes its effect on the β-multiplier bandgap voltage reference circuit incomparable to that of the opamp input offset voltage problem. Detailed analysis on the $PSRR$ of the opamp based β-multiplier bandgap voltage reference circuit including the effect of limited $PSRR$ and the limited gain of the opamp will be presented in Section 4.5.

4.1.2.1 Bootstrap Biasing

The performance of the opamp depends on the biasing circuit as shown in Figure 3.4. The biasing circuit is nothing more than a supply voltage independent constant current source. The variation of this biasing current will affect the gain, the offset voltage, and the stability of the opamp. However, all kinds of current sources will suffer from the same problems faced by the voltage reference circuits discussed in this book, and also problems that are not discussed in this book. One of the most severe problems faced by the current source used to bias the opamp is the power supply dependency. The power supply sensitivity of the opamp biasing circuit can be reduced by "*bootstrap*" biasing technique, which is also known as self-biasing. Note that the β-multiplier in the bandgap voltage reference circuit is itself a current source. As a result, a self-biasing circuit can be achieved by mirroring the current source in the β-multiplier to bias the opamp.

Showing in Figure 4.6 is the schematic of a self-biased opamp based β-multiplier bandgap voltage reference circuit, where the biasing current of the opamp is mirrored from the PTAT current source from the bandgap voltage reference circuit. The device sizes of the opamp based β-multiplier bandgap voltage reference circuit is shown in Table 4.1. Note that the voltage reference circuit in Figure 4.6 is the same as that in Figure 3.11, except that there is no external V_{BIAS} to generate I_4 for the differential input transistor pairs M_5 and M_6 of the opamp. The biasing current I_4 is derived from I_{PTAT} by connecting M_4 to form current mirrors with M_1, M_2, and M_3. The size of M_4 is therefore controlled by properly scaling $S_4 : S_1 : S_2 : S_3$. Such a self-biasing circuit does form a close loop, which is also known as bootstrap biasing circuit. The close loop implementation will improve the stability of the bandgap voltage reference circuit, including the line regulation. Note that this current source is PTAT in nature, and thus imposes a temperature dependent opamp performance variation. However, given the small PTAT current variation, the opamp performance variation will be at minimal. Of course, the best bootstrap biasing circuit is to use the reference voltage to feedback to bias the opamp through resistor networks, as shown in Figure 4.7. In this case, a second feedback loop is formed between the opamp and the output of the bandgap voltage reference circuit through

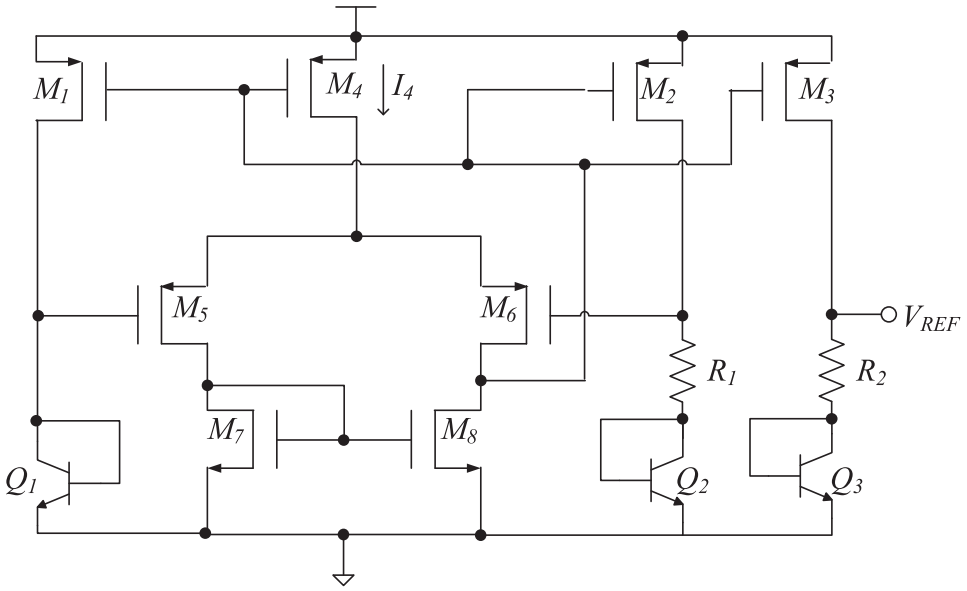


Figure 4.6 Opamp based β-multiplier bandgap voltage reference circuit using current source from the β-multiplier to bootstrap bias the opamp.

resistor dividers R_3 and R_4, and hence helps to improve the stability of the voltage reference circuit. Furthermore, the reference voltage has small TC. As a result, the opamp biasing circuit will also have small TC, and thus the opamp performance has small temperature dependency. The drawback of this circuit is the slow response of the bandgap voltage reference circuit towards external environmental variations. This is because, when there is an external variation that results in an increased reference voltage, the biasing current of the opamp will reduce and hence increase the loop delay of the bootstrap biased circuit. Furthermore, the resistors required by the bootstrap circuit will inevitability increase the overall silicon layout size.

4.1.3 Noise

Previous publications on standard CMOS amplifier circuits have reported mid-band equivalent input noise voltages (E_η) ranging from 9.8 nV/$\sqrt{\text{Hz}}$ to 70 nV/$\sqrt{\text{Hz}}$. In particular, E_η at 1 kHz

Table 4.1 Device sizes for the opamp based β-multiplier bandgap voltage reference circuit shown in Figure 4.6.

M_1, M_2, M_3	W/L=10 μm/1 μm
Q_1, Q_3	Emitter Area Ratio with respect to unit sized BJT, A_E=1
Q_2	Emitter Area Ratio with respect to unit sized BJT, A_E=8
R_1	9 kΩ
R_2	81.7 kΩ
M_4, M_5, M_7, M_8	W/L=8 μm/0.3 μm
M_6	W/L=32 μm/0.3 μm
M_9, M_{10}	W/L=2 μm/0.18 μm
M_{11}	W/L=16.7 μm/0.3 μm

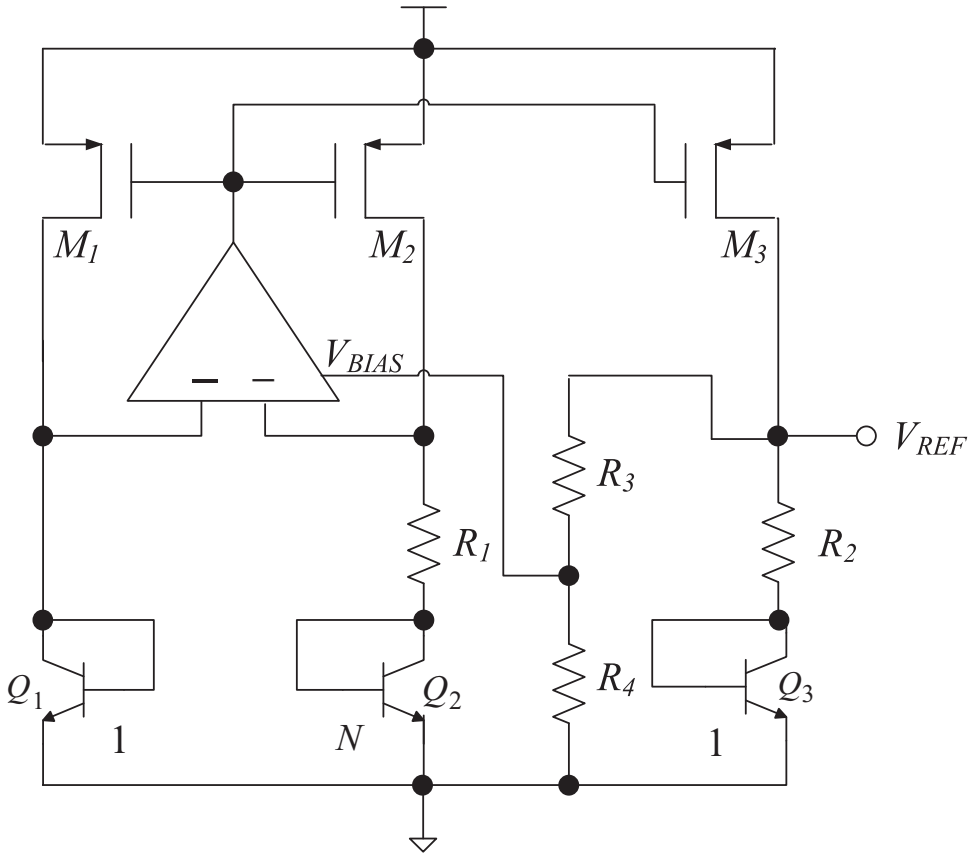


Figure 4.7 Opamp based β-multiplier bandgap voltage reference circuit using the output to bootstrap bias the opamp.

has been measured to equal 95 nV/$\sqrt{\text{Hz}}$ to 1.7 μV/$\sqrt{\text{Hz}}$. The $1/f$ noise corner frequency is observed to be located between 7 kHz and 159 kHz frequencies (Gray and Meyer, 1982). These high noise levels can seriously degrade the overall performance of the voltage reference circuit. Much efforts have been focused on reducing E_η, particularly the $1/f$ components, in recent years.

In a typical CMOS opamp, the equivalent input noise voltage is dominated by the E_η of the transistors in the differential input stage, especially by the input transistors where their transconductances are much greater than those of the current load transistors (Gray and Meyer, 1982). The detailed analysis of the noise effect of a simple one-stage opamp based β-multiplier bandgap voltage reference circuit will be presented in Section 4.7.

4.2 Current Mirror Mismatch

Figure 4.8 shows the schematic of an opamp based β-multiplier bandgap voltage reference circuit with current mirror mismatch error, where $e_{m,1}$ and $e_{m,2}$ denote the mismatch errors on I_1 and I_3, respectively when compared to I_2. This mismatch error is imposed by the mismatch in the current mirror formed by transistors M_1, M_2, and M_3. Such that the current ratio of the current mirror formed by M_1, M_2, and M_3 deviated from the ideal case of 1 : 1 : 1 to

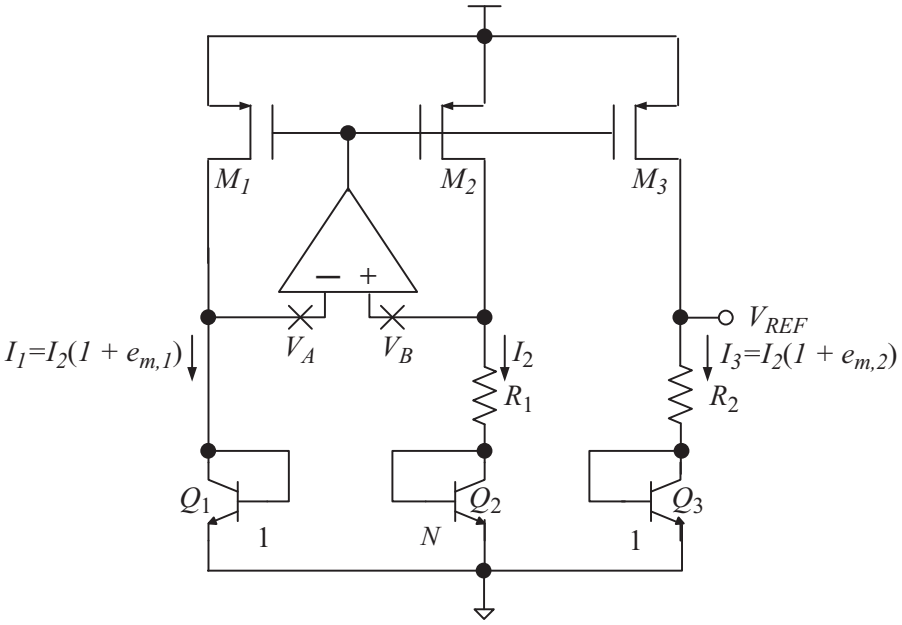


Figure 4.8 Bandgap voltage reference circuit with current mirror mismatch problem.

$1 + e_{m,1} : 1 : 1 + e_{m,2}$. The mismatch in the current mirror is commonly caused by process variation and channel length modulation problems. The output of the voltage reference circuit is given by

$$V_{REF} = (1 + e_{m,2})\frac{R_2}{R_1} V_T \ln(N(1 + e_{m,1})) + V_{BE_3}.$$

The reference voltage variation $\Delta V_{REF,CM}$ caused by the current mirror is thus given by

$$\begin{aligned}\Delta V_{REF,CM} &= e_{m,2}\frac{R_2}{R_1} V_T \ln(N(1 + e_{m,1})) + \frac{R_2}{R_1} V_T \ln(1 + e_{m,1}) \\ &\approx e_{m,2}\frac{R_2}{R_1} V_T \ln N + e_{m,1}\frac{R_2}{R_1} V_T,\end{aligned}$$

where we assume both $e_{m,1}$ and $e_{m,2} << 1$ for a small current mismatch error. Consider the case with $\frac{R_2}{R_1} = 9.24$, and $N = 8$ as in Equation 3.14, the mismatch errors are the same and equal to $e_{m,1} = e_{m,2} = 1\%$. The reference voltage variation is found to be $\Delta V_{REF,CM} = 7.36$ m V, which is 0.6% of the nominal reference voltage 1.23 V. When the current mismatch is reduced to $e_{m,1} = e_{m,2} = 0.1\%$, the output voltage variation is reduced to $\Delta V_{REF,CM} = 0.736$ m V or 0.06% of the V_{REF}.

As aforementioned, the current mirror mismatch problem is both a process variation and circuit design problem. It is a process variation problem because the currents passing through the transistors are proportional to $(V_{SG} - |V_{th,p}|)^2$. Due to the squares term, any small variation in $V_{th,p}$ will cause a large variation in the current passing through the transistor. As a result, a high V_{SG} is desirable to reduce the $V_{th,p}$ variation effect on the current that passes through the transistor, and thus reducing the current mismatch problem. A high V_{SG} can be achieved

using a transistor with small W/L such that the current passing though the transistor will be the same. Furthermore, the MOSFETs used in the current mirror should have large W and L, and be implemented with the matched layout technique to alleviate the geometric variation problem. As a result, there is a design paradox between the geometric variation and $V_{th,p}$ variation in the implementation of the current mirror.

The current mismatch problem is also a circuit problem because the unmatched currents can also be caused by the channel length modulation effect. This is because the drain of the two transistors M_1 and M_2 in the current mirror are connected to the inputs of the opamp and hence are maintained at the same voltage by the opamp. As a result, the channel length modulation problem is mainly observed at the output stage of the bandgap voltage reference circuit. Transistors with long channels can be used in the current mirror to reduce the channel length modulation effect, while the relative transistor size variation can be minimized by using large transistors and better layout matching techniques. The following section will present various circuit techniques that help to mitigate the current mirror mismatch problem caused by channel length modulation effect.

4.2.1 Channel Length Modulation Effect Compensation

Consider the opamp based β-multiplier bandgap voltage reference circuit in Figure 4.8, the intrinsic issue of the channel length modulation problem is caused by the direct connection of the transistors M_1 and M_2 of the current mirror to the opamp input nodes, in which the voltages at the opamp input terminals are different from the output reference voltage. In other words, the drain voltage of M_3 is different from those of M_1 and M_2. As a result, the channel length modulation problem is observed between the transistor M_3 of the current mirror at the output stage of the bandgap voltage reference circuit, and the transistors M_1 and M_2 in the current mirror. The problem will be clearer if it is considered analytically. Without the opamp input offset voltage problem and assuming the opamp has large enough gain, then $V_{SD_1} = V_{SD_2}$. Let's consider the transistor pair M_1, M_2, and M_3. The $V_{SD_1} = V_{DD} - V_{BE_1} \approx V_{DD} - 0.73$ V, while the $V_{SD_3} = V_{DD} - 1.23$ V. As a result, $V_{SD_3} \neq V_{SD_1}$, and thus the current mirror formed by M_1, M_2, and M_3 will suffer from the channel length modulation effect. To alleviate this problem, resistors R_3 and R_4 are inserted in-between M_1, M_2 and the opamp inputs as shown in Figure 4.9. In particular, we choose $I_3R_2 = I_1R_3 = I_2R_4$. In other words, the voltages across R_2, R_3, and R_4 are equal to 1.23 V $- V_{BE_3}$. As a result, $V_{SD_1} = V_{SD_2} = V_{SD_3}$. In this case, the channel length modulation effects of the current mirror formed by M_1, M_2, and M_3 due to the mismatch of V_{SD} can be alleviated. The simulation results in Figure 4.10 plotted the reference voltage variation under input voltage variation for both schematics in Figure 4.9 and the conventional opamp based β-multiplier bandgap voltage reference circuit in Figure 3.4. It can be observed from Figure 4.10(a) that the line regulation of both circuits are close with the minimum operating voltages both at 1.4 V. However, when we look into the output voltage in the supply voltage range of 1.8 V to 3 V (see Figure 4.10(b)), the channel length modulation effect compensated circuit achieves a lower output voltage variation of 1.69 mV while that of the conventional bandgap voltage reference circuit is 2.19 mV. As a result, it is clear that the voltage reference circuit with compensated channel length modulation effect can achieve better line regulation.

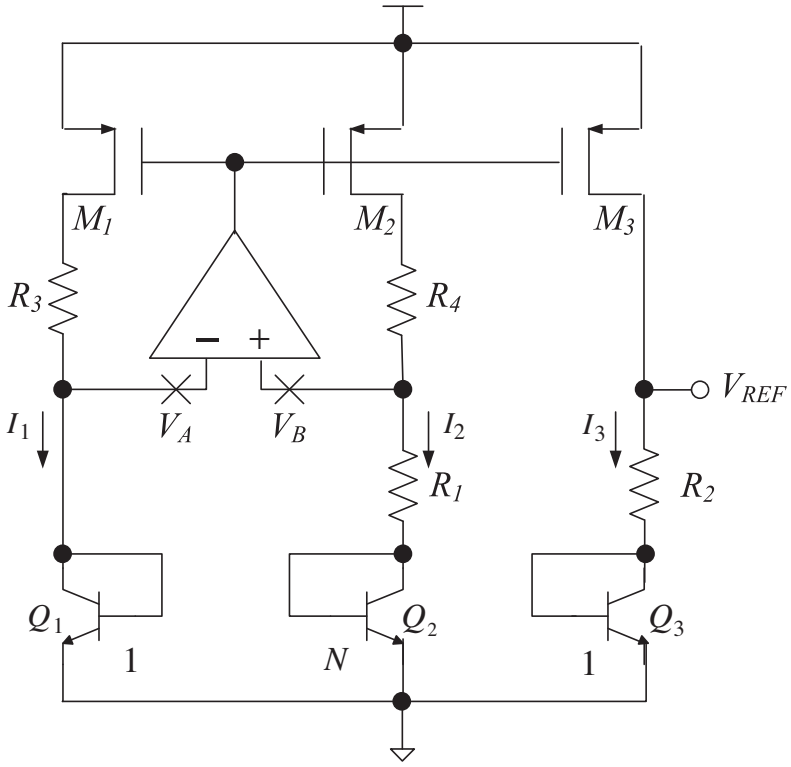
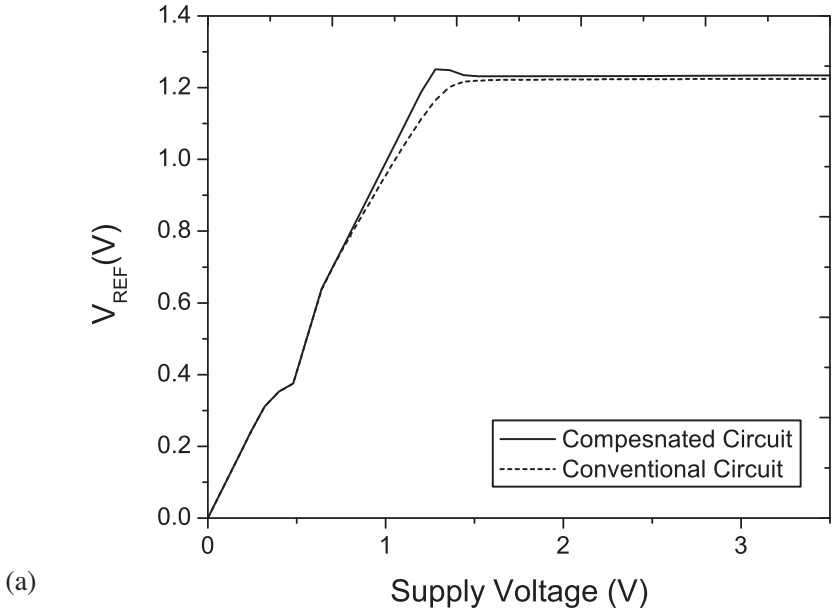


Figure 4.9 Schematic of bandgap voltage reference circuit with channel length modulation effect compensation.

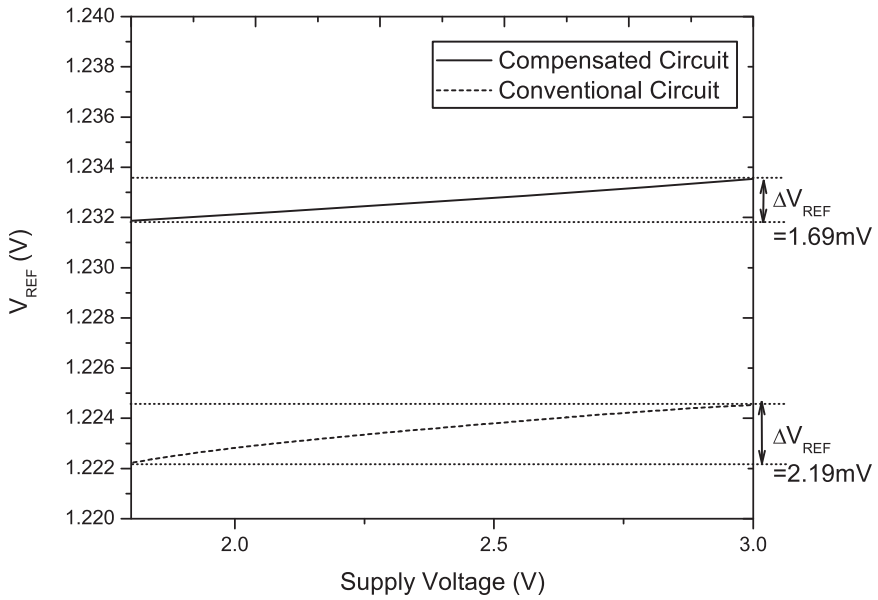
4.2.2 Cascode Current Mirror

Besides the process variation, and channel length modulation problems, the transistors in the current mirror will experience current mismatch problem when they are not operating in the saturation mode or when their V_{SG} are not the same. The mismatch problem can be relieved by increasing the output impedance using the high output impedance current mirror as discussed in Section 3.3.2. Figure 4.11 shows the schematic of the modified opamp based β-multiplier bandgap voltage reference circuit with the simple current mirror replaced by the cascode current mirror. Simulation results of the temperature dependency and the line regulation of the schematic in Figure 4.11 are shown in Figures 4.12 and 4.13, respectively.

As observed from Figure 4.12, the temperature dependency of the modified circuit is similar to that of the conventional circuit as shown in Figure 3.9. The TC of the modified circuit at $V_{DD} = 2$ V in the temperature range of -40 °C to 125 °C is 9.9 ppm/K, which is comparable to that of the conventional circuit. However, when comparing the line regulation of the modified circuit for the supply voltage range of 1.8 V to 3 V (see Figure 4.13) to that of the conventional circuit (see Figure 4.10(b)), the modified circuit achieves an output voltage variation of 1.68 mV which is lower than the 2.19 mV voltage variation of the conventional opamp based β-multiplier bandgap voltage reference circuit. The application of the cascode current mirror achieves a 23.3% improvement of the line regulation. However, this improvement comes with a tradeoff. The minimum operating voltage of the modified circuit is increased to 1.8 V, which is 0.4 V higher than that of the conventional opamp based β-multiplier bandgap voltage reference circuit. The increase in minimum operating voltage conforms to



(a)



(b)

Figure 4.10 SPICE simulation results of (a) the line regulation of the conventional opamp based β-multiplier bandgap voltage reference circuit in Figure 3.4 and the channel length modulation effect compensated opamp based β-multiplier bandgap voltage reference circuit in Figure 4.9; and (b) the line regulation in the supply voltage range from 1.8 V to 3 V.

that discussed in Section 3.3.2, which is caused by the additional transistor level (additional V_{SG} voltage) of the cascode current mirror, and hence reduces the voltage headroom of the opamp based β-multiplier bandgap voltage reference circuit with cascode current mirror.

The cascode current mirror also helps to improve the $PSRR$ of the voltage reference circuit. Consider a simplified small signal circuit representation of the opamp based β-multiplier bandgap voltage reference circuit shown in Figure 4.14, which was considered in (Rincon-Mora, 2002) with R_C and R_{OUT} being the small signal impedance measured at the

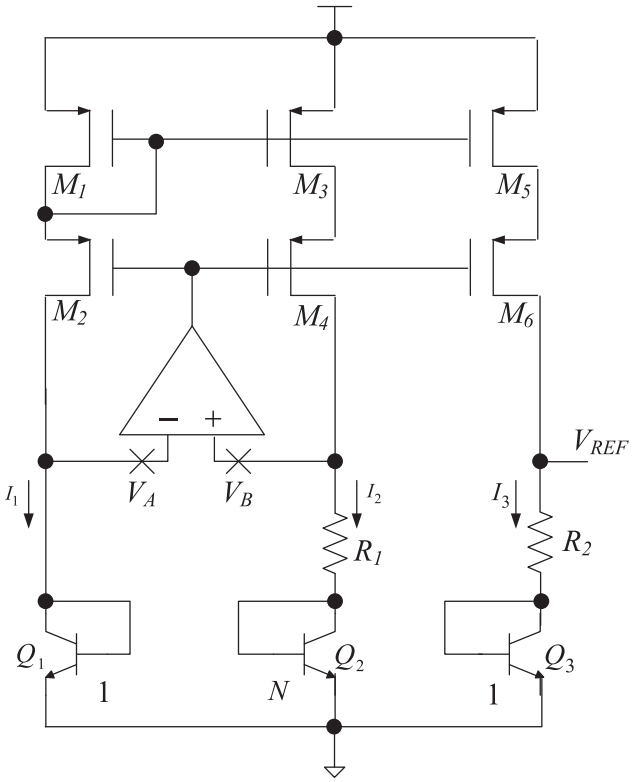


Figure 4.11 Schematic of modified opamp based β-multiplier bandgap voltage reference circuit with cascode current mirror.

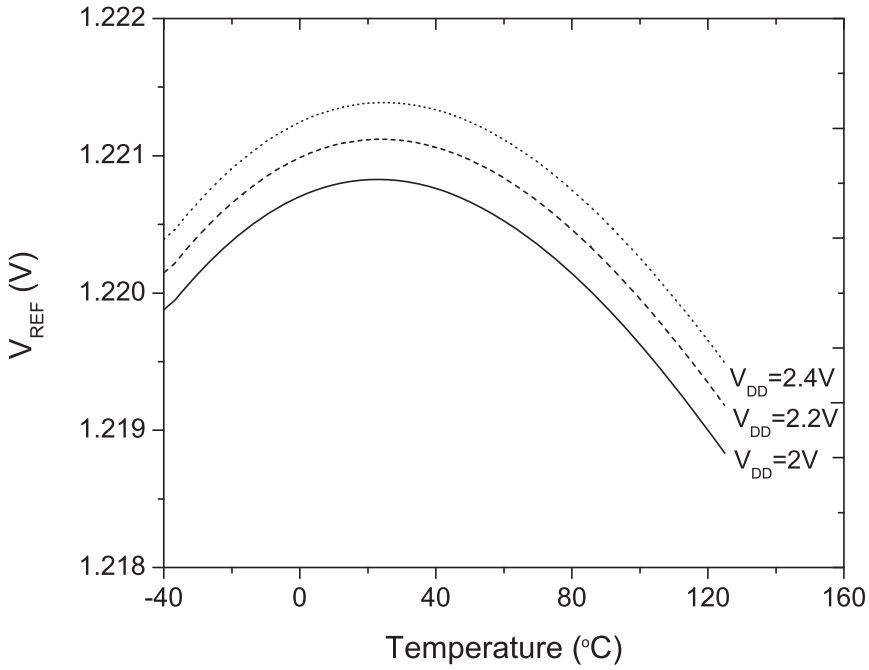


Figure 4.12 Simulated temperature dependency of modified β-multiplier bandgap voltage reference circuit shown in Figure 4.11.

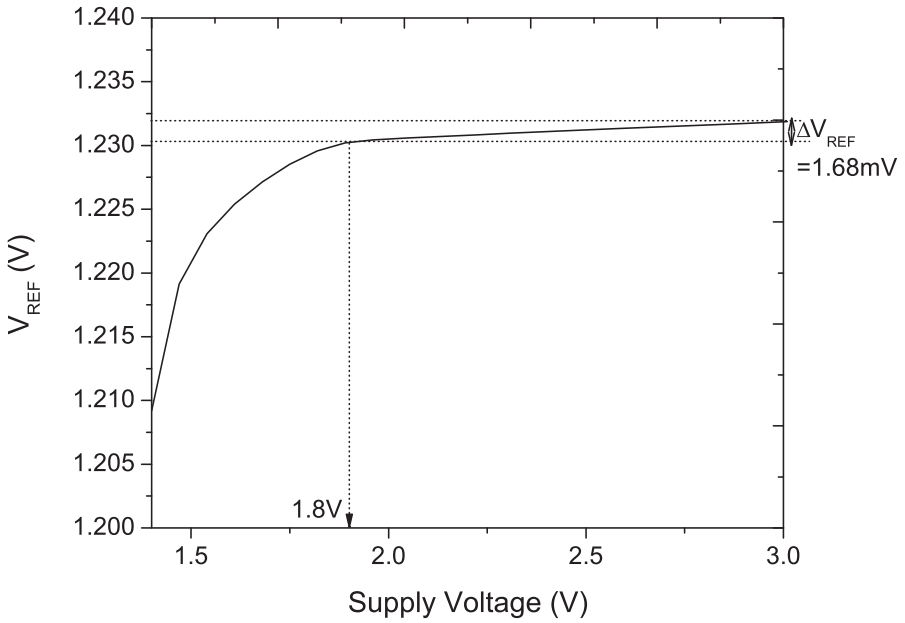


Figure 4.13 Simulated line regulation of modified β-multiplier bandgap voltage reference circuit shown in Figure 4.11.

V_{REF} node to the ground and V_{DD} nodes, respectively. The $PSRR$ of the voltage reference circuit is given by Equation 2.9 as

$$PSRR(f) = 20\log\frac{V_{REF,AC}(f)}{V_{DD,AC}(f)}.$$

As observed in Figure 4.14, we can derive

$$V_{REF,AC}(f) = V_{DD,AC}(f)\frac{R_C}{R_{OUT}+R_C},$$

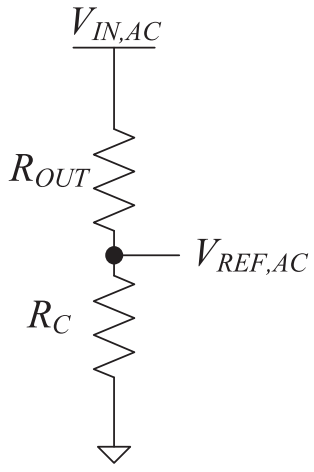


Figure 4.14 Small signal model of bandgap voltage reference circuit.

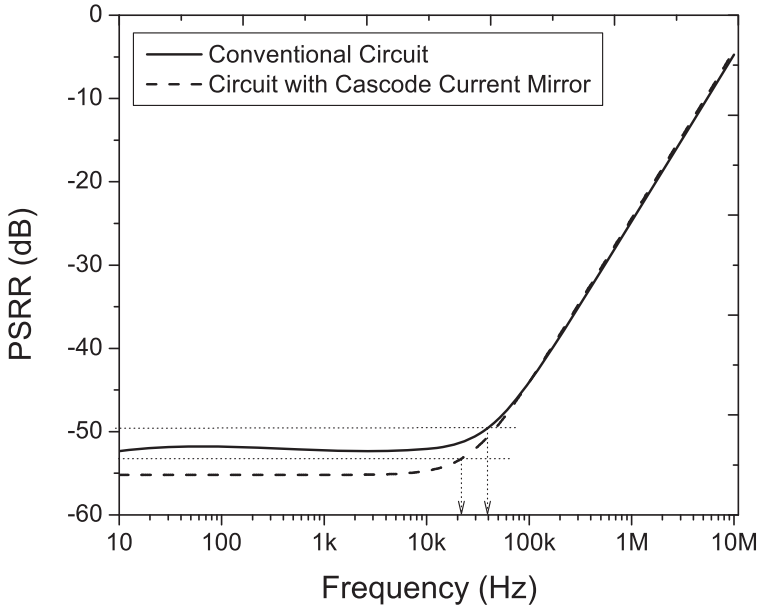


Figure 4.15 Simulated $PSRR$ of conventional opamp-based β-multiplier bandgap voltage reference circuit (using simple current mirror) and modified circuit (using cascode current mirror).

and thus can be incorporated to the small signal block diagram of Figure 4.14 and the $PSRR$ can be expressed as

$$PSRR(f) = 20\log\left(\frac{V_{DD,AC}(f)\frac{R_C}{R_{OUT}+R_C}}{V_{DD,AC}(f)}\right) = 20\log\left(\frac{R_C}{R_{OUT}+R_C}\right).$$

It is clear that the $PSRR$ can be improved (achieve a lower value) by increasing R_{OUT}, the output impedance of the current mirror in the opamp based β-multiplier bandgap voltage reference circuit. As discussed in Section 3.3.2, using an alternative current mirror circuit is both efficient and simple in order to achieve a higher output resistance R_{OUT}. Figure 4.15 shows the $PSRR$ simulation results of the circuit in Figures 3.4 and 4.11, respectively. It can be observed that the $PSRR$ of the opamp based β-multiplier bandgap voltage reference circuit with cascode current mirror is -55.2 dB in the frequency range of ($10 \sim 10$ kHz), which is 3 dB lower than that of the opamp based β-multiplier bandgap voltage reference circuit with a simple current mirror. It can also be observed that the modification of the current mirror circuits can achieve a $PSRR$ curve with a lower corner frequency around 20 kHz while that of the conventional opamp based β-multiplier bandgap voltage reference circuit is at 41.7 kHz. It is interesting to find that besides shifting the low frequency portion of the curve, the voltage reference circuit with modified current mirror will also achieve a low $PSRR$ corner frequency such that the $PSRR$ curve rolls together with that of the conventional opamp based β-multiplier bandgap voltage reference circuit at the high frequency portion.

4.3 Bipolar Transistor

The core of the bandgap voltage reference circuit is the base-emitter voltage of the bipolar transistors. However, the value of the base-emitter voltage varies due to process variation and it also deviates from Equation 1.7 as that equation can only model ideal BJT devices. In the following, the effects of the non-ideal bipolar transistors, including geometric variation, finite series connected base resistance, and finite β with variation will be investigated. Methods to alleviate their effects will also be presented.

4.3.1 Size Variation

The geometric variation of NPN transistors will affect the emitter area ratio N, which will induce a variation on the output voltage as

$$\Delta V_{REF,BJT,N} = \frac{R_2}{R_1} V_T \left\{ \ln\left[N(1+e_{BJT,N})\right] - \ln(N) \right\} \approx e_{BJT,N} \frac{R_2}{R_1} V_T,$$

where $e_{BJT,N}$ is the variation on the emitter area ratio N of the NPN transistor. As an example, consider the case of $e_{BJT,N} = 1\%$. If N is chosen to be 8, then $\frac{R_2}{R_1} = 9.24$. The output voltage variation will be $\Delta V_{REF,BJT,N} = 2.4$ mV. When the emitter area ratio variation is reduced to $e_{BJT,N} = 0.1\%$, then the output voltage variation will be $\Delta V_{REF,BJT,N} = 0.24$ mV. The transistor size variation effect can be alleviated by better layout with the application of a unit transistor pre-defined (characterized) for the process. Figure 3.19 shows a good example of a layout of well matched bipolar transistors Q_1 and Q_2 with size ratio 1 : 8 using the centroid symmetric layout technique as discussed in Section 1.5 and Section 3.3.5. Note that the layout of the BJT is usually large, and thus it is not usually possible to alleviate the transistor size variation effect by layout techniques other than the simple centroid symmetric layout technique shown in Figure 3.19.

4.3.2 Series Base Resistance

Another non-ideal property of the BJT, that is not considered in Equation 1.7, is the series resistance associated with the terminals of the BJT. Of the three series resistors, the series base resistor r_b has the greatest influence on the V_{BE} of a diode connected BJT. This is because the β of the NPN transistor fabricated by the CMOS technique is usually small. As a result, the current passing through r_b will be comparatively large, and hence induce a large voltage drop, which will be reflected in the V_{BE} of the diode connected BJT and result in non-ideal $I - V$ characteristics. We have already discussed the possible influence of the base current under the finite β in the bandgap voltage reference circuit in Section 4.1.1.4 for the series connected BJT applied in the bandgap voltage reference circuit. In this section, we shall provide a detail and formal analysis of the base current and the finite β problem with considering r_b of the BJT.

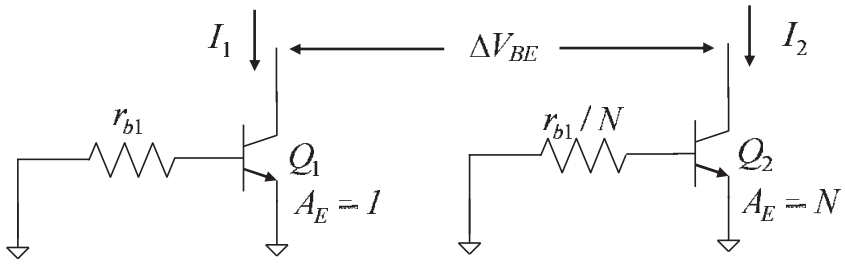


Figure 4.16 Illustration of the series resistances of the bipolar transistors.

Due to the finite β of the BJT implemented in the CMOS process, the V_{BE} observed from the BJT with series base resistor is given by

$$V_{BE} = I_b r_b + V_T \ln \frac{I_c}{I_S} = \frac{I_c}{\beta} r_b + V_T \ln \frac{I_c}{I_S}. \tag{4.8}$$

Consider the case where all the three transistors M_1, M_2, and M_3 in the current mirror of the opamp based β-multiplier bandgap voltage reference circuit are the same size and do not suffer from channel length modulation effect, and the three NPN transistors have the same β. As a result,

$$I_1 = I_2 = I_3 = I.$$
$$\beta_1 = \beta_2 = \beta_3 = \beta.$$

Figure 4.16 illustrates the series base resistances of Q_1 and Q_2 in the voltage reference circuit. We can obtain the $\Delta V_{BE_{1,2}}$ of these non-ideal BJTs as

$$\begin{aligned} \Delta V_{BE_{1,2}} &= \frac{I}{\beta} r_{b_1} + V_T \ln \frac{I}{I_{S_1}} - \frac{I}{\beta} r_{b_2} - V_T \ln \frac{I}{I_{S_2}} \\ &= \frac{I}{\beta} \Delta r_{b_{1,2}} + V_T \ln N, \end{aligned} \tag{4.9}$$

where $\Delta r_{b_{1,2}} = r_{b_1} - r_{b_2}$. Note that

$$\Delta V_{BE_{1,2}} = I \times R_1. \tag{4.10}$$

Substitute Equation 4.10 into 4.9 yields

$$I = \frac{\Delta V_{BE_{1,2}}}{R_1}$$
$$I = \frac{\frac{I}{\beta} \Delta r_{b_{1,2}} + V_T \ln N}{R_1}.$$

By rearranging the terms, it yields

$$I = \frac{V_T \ln N}{R_1 - \frac{\Delta r_{b_{1,2}}}{\beta}}. \tag{4.11}$$

As a result,

$$V_{REF} = I R_2 + V_{BE_3} = V_T \ln N \frac{R_2}{R_1 - \frac{\Delta r_{b_{1,2}}}{\beta}} + V_{BE_3}. \tag{4.12}$$

If we further consider the series base resistor r_{b_3} of Q_3, by substituting Equations 4.8 and 4.11 into Equation 4.12. We can rearrange the equation to obtain V_{BE_3} which will yield

$$\begin{aligned} V_{REF} &= \frac{V_T \ln N}{R_1 - \frac{\Delta r_{b_{1,2}}}{\beta}} \left(R_2 + \frac{r_{b_3}}{\beta} \right) + V_{BE_{30}} \\ &= \frac{V_T \ln N}{R_1} \frac{1}{1 - \frac{\Delta r_{b_{1,2}}}{\beta R_1}} \left(R_2 + \frac{r_{b_3}}{\beta} \right) + V_{BE_{30}}, \end{aligned} \tag{4.13}$$

where $V_{BE_{30}}$ is the V_{BE} of an ideal Q_3. Note that when $x << 1$, we can approximate $\frac{1}{1-x} \approx 1 + x$. As a result, when $\frac{\Delta r_{b_{1,2}}}{\beta R_1} \to 0$, for example when $\beta >> 1$, Equation 4.13 can be approximated as

$$V_{REF} = \frac{R_2}{R_1} V_T \ln N + V_{BE_{30}} + \Delta V_{REF,r_b},$$

where the error term associated with r_b is given by

$$\begin{aligned} \Delta V_{REF,r_b} &= \frac{R_2}{R_1} V_T \ln \left(N \frac{\Delta r_{b_{1,2}}}{\beta R_1} \right) + \frac{R_2}{R_1} V_T \ln \left(N \frac{r_{b_3}}{\beta R_2} \right) \\ &\quad + \frac{R_2}{R_1} V_T \ln \left(N \frac{\Delta r_{b_{1,2}} r_{b_3}}{\beta^2 R_1 R_2} \right) \\ &\approx \frac{R_2}{R_1} V_T \ln \left(N \frac{\Delta r_{b_{1,2}}}{\beta R_1} \right) + \frac{R_2}{R_1} V_T \ln \left(N \frac{r_{b_3}}{\beta R_2} \right). \end{aligned}$$

It can be observed that with a fixed $\frac{R_2}{R_1}$, the effect of the series resistor can be minimized by increasing the values of R_1 and R_2, increasing β, reducing the series base resistor r_b, or by better matching of the NPN transistors Q_1 and Q_2 such as to reduce $\Delta r_{b_{1,2}}$. On the other hand, it should be noted that β is associated with the fabrication process, and thus it is difficult to increase its value. However, the series base resistance r_{b_3} is the resistance between the transistor base connection via the metal wire (and metal vias). Therefore, the series resistance r_{b_3} can be reduced by using thick metal and increasing the number of connections to the active area and the metal wire. Therefore, the resistivity r_{b_3} is sensitive to the layout, number, and position of the connections, which range from 10 Ω to 500 Ω. It can also be observed that

$r_{b_2} \approx r_{b_1}/N$, when the transistor Q_1 and Q_2 are carefully matched. As a result if $N >> 1$, then $\Delta r_{b_{1,2}} \approx r_{b_1}$ and thus it is difficult to decrease its value. Therefore, it seems that the most viable solution is to use R_1 and R_2 with large resistance. The drawback of this approach is the increase in silicon layout, since resistors with large resistances will occupy a lot of silicon area.

Concerning other series resistors, the series emitter resistor r_e associated with the emitter of the NPN transistor has the same effect as the resistor value variation of R_1 and R_2, and thus can be lumped into the analysis of the effect of the resistor ratio variation between R_1 and R_2. The series collector resistor r_c associated with the collector of the NPN transistor will result in $V_{BC} \neq 0$ in the diode connected BJT (in a similar fashion, the existence of r_b will result in $V_{BC} \neq 0$). However, I_S is small (usually in the order of 10^{-14}). Therefore, its effect can usually be ignored.

4.3.3 β Variation

The BJT fabricated by the CMOS process will have a small β. Furthermore, the value of β is not exactly constant from one BJT to another on the same chip. The β of the BJT is affected by the process variation problem, and it is also affected by the operating currents of the bipolar transistor. Thus, the currents I_1, I_2, and I_3 should be controlled in a suitable region in order to maintain a large β and hence a small $\Delta V_{REF,r_b}$ (disregarding the β variations). To understand the effect of β variations, we shall consider Equation 4.8 with $I_1 : I_2$ equals $1 : \frac{N_1}{N}$, the BJT emitter area ratio $A_{E_1} : A_{E_2}$ equals $1 : N$, and the β of the transistors Q_1 and Q_2 being β_1 and β_2, respectively. As a result,

$$V_{BE_1} = I_{b_1} r_{b_1} + V_T \ln \frac{I_1}{I_{S_1}} = \frac{I_1}{\beta_1} r_{b_1} + V_T \ln \frac{I_1}{I_{S_1}}, \tag{4.14}$$

$$V_{BE_2} = I_{b_2} \frac{r_{b_1}}{N} + V_T \ln \frac{I_2}{I_{S_2}} = \frac{I_2 r_{b_1}}{\beta_2 N} + V_T \ln \frac{I_2}{I_{S_2}}. \tag{4.15}$$

where $r_{b_2} = \frac{r_{b_1}}{N}$. The $\Delta V_{BE_{1,2}}$ is thus given by

$$\Delta V_{BE_{1,2}} = r_{b_1} \left(\frac{I_1}{\beta_1} - \frac{I_2}{N\beta_2} \right) + 2V_T \ln N - V_T \ln N_1. \tag{4.16}$$

It can be observed from Equation 4.16 that the β variation of the BJTs will result in variations of the extracted $\Delta V_{BE_{1,2}}$. Furthermore, the variation is proportional to I_1 and I_2. As a result, we should control the two currents to mitigate the effect of β variation between transistors. To analytically derive the output voltage variation caused by $\Delta V_{BE_{1,2}}$ in Equation 4.16, we have to compare the difference between Equation 4.16 and 3.13. When we multiply the result by a factor of $\frac{R_2}{R_1}$ will yield

$$\Delta V_{REF,BJT,\beta} = \frac{R_2}{R_1} \epsilon_{BJT,\beta} = \frac{R_2}{R_1} \frac{N_1}{N} I_1 r_{b_1} \left(\frac{1}{\beta_1} - \frac{1}{N_{\beta_2}} \right). \tag{4.17}$$

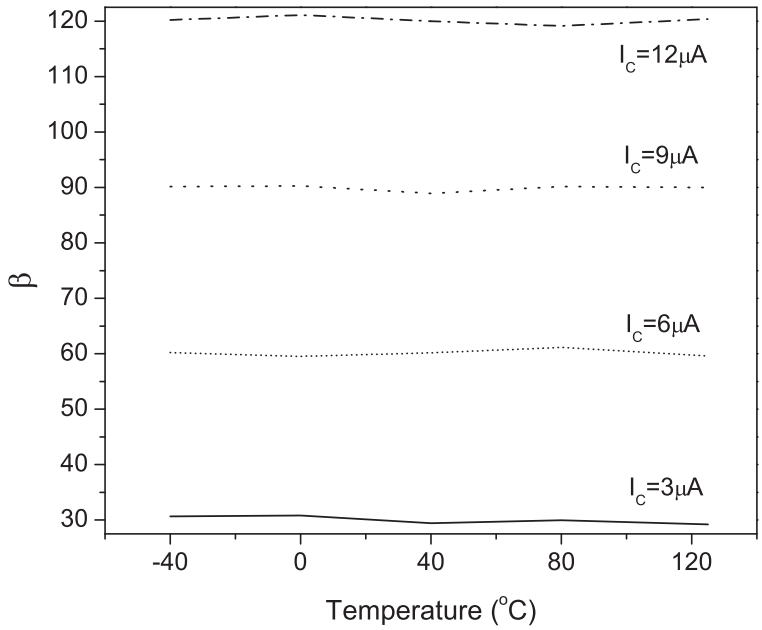


Figure 4.17 Temperature and biasing current dependency of β of a 4×4 μm^2 NPN BJT.

Figure 4.17 shows the β of a 4×4 μm^2 NPN BJT at different I_C and different temperatures. It is clear that the variation of β is small when I_C is smaller than 10 μA. With such a small I_C and small β variation, put into the context of Equation 4.16, the content inside the bracket will approximately equal 0, and thus Equation 4.16 will have the same form as the β variation free $\Delta V_{BE_{1,2}}$ as that in Equation 4.2. However, the I_C cannot be chosen to be too small, because as observed in Figure 4.17 the β will drop sharply when the current is too small. The emitter area size of the transistors Q_1 and Q_2 differ by a ratio of N, and the current passing through Q_1 and Q_2 will have current densities differ by a ratio of $\frac{N_1}{N}$. As a result, I_1 and I_2 have to be chosen carefully, such that both currents are within the range where the β variation is small. As a rule of thumb, with respect to the process under consideration in this book, I_1 is chosen to be 6 μA, while $I_2 = \frac{N_1}{N} I_1$, with $\frac{1}{8} \leq \frac{N_1}{N} \leq 1$, such that the two BJTs are properly biased.

4.4 Resistor Variation

Similar to the variation of the NPN transistors emitter area ratio, the resistance ratio $\frac{R_2}{R_1}$ variation can be modeled by $\frac{R_2}{R_1}(1 + e_R)$, where e_R denotes the associated variation. e_R will induce a variation on the output voltage given by

$$\Delta V_{REF,R} = \frac{R_2}{R_1} e_R V_T \ln N. \tag{4.18}$$

As an example, consider $N = 8$, and $\frac{R_2}{R_1} = 9.24$ as that in Section 3.2.2. The output voltage variation is thus obtained as $\Delta V_{REF,R} = 497.56\, e_R$ mV. Consider the case when the resistance of the resistors R_1 and R_2 are matched with an accuracy of 1%, that is, $e_R = 0.01$, then the induced voltage variation is 4.99 mV. Note that it is the resistor ratio that affects the

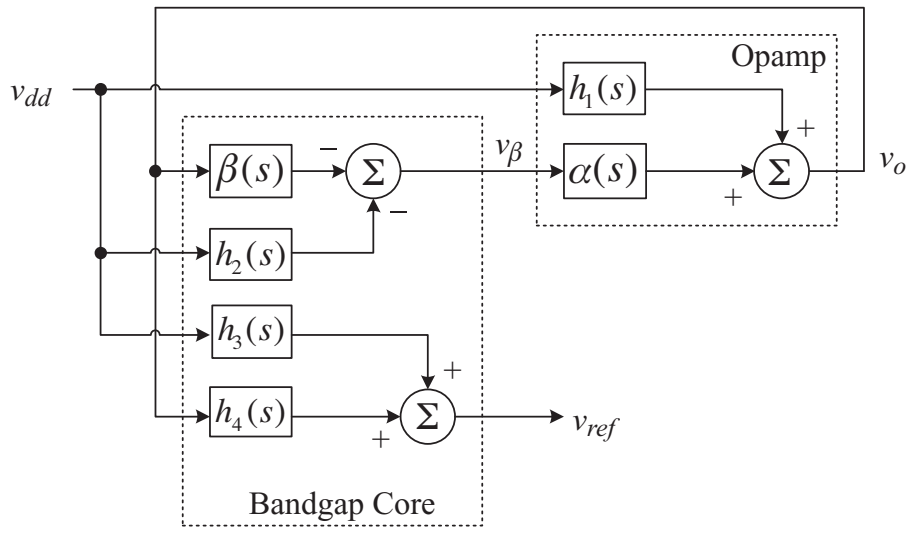


Figure 4.18 Small signal model of a bandgap reference in Figure 3.4.

reference voltages but not the resistance values. As a result, the output voltage variation can be reduced by proper layout matching as discussed in Section 1.5.

4.5 Power Supply Variation

Various circuit components that affect the power supply rejection ratio have been discussed in previous sections. This section is dedicated to a detailed analytical analysis of the $PSRR$ of the opamp based β-multiplier bandgap voltage reference circuit in Figure 3.4. Figure 4.18 shows the small signal analysis equivalent circuit diagram of the voltage reference circuit in Figure 3.4, which includes the bandgap core and the opamp. A similar small signal analysis was first proposed in (Giustolisi *et al.*, 2003) for a variety of voltage reference circuits, while we are adopting the same method for the opamp based β-multiplier bandgap voltage reference circuit.

The small signal differential input of the opamp is formed by the feedback signal $v_o \times \beta(s)$ and the supply noise voltage coupled to the differential input signal $v_{dd} \times h_2(s)$, where $\beta(s)$ is the feedback loop characteristics of the opamp based β-multiplier , and $h_2(s)$ is the transfer function of the power supply noise of the bandgap core coupled to the different voltage v_β.

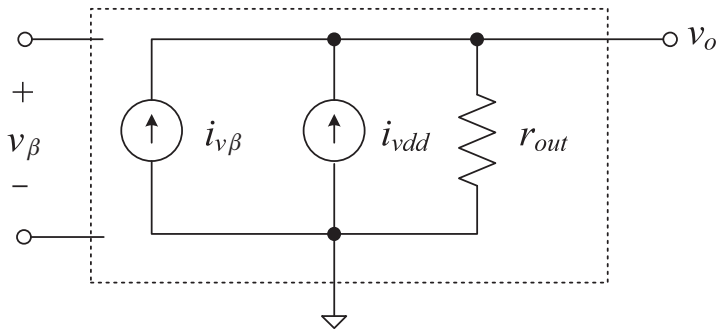


Figure 4.19 Small signal model of the opamp.

The output of the opamp is formed by $v_\beta \times \alpha(s)$, and power supply noise $v_{dd} \times h_1(s)$, where $\alpha(s)$ is the small signal gain of the opamp, and $h_1(s)$ is the transfer function of the power supply noise of the opamp. Therefore,

$$v_\beta = v_o\beta(s) + v_{dd}h_2(s), \tag{4.19}$$

$$v_o = v_\beta\alpha(s) + v_{dd}h_1(s). \tag{4.20}$$

The input to the bandgap core is v_{dd} and v_o. The output of the bandgap core circuit is v_β and v_{ref}, which are the differential input voltage to the opamp and the small signal reference voltages, respectively. In particular, the small signal reference signal is given by

$$v_{ref} = v_o h_4(s) + v_{dd}h_3(s), \tag{4.21}$$

where $h_3(s)$ is the transfer function of the power supply noise of the bandgap core coupled to the small signal output signal v_{ref}, and $h_4(s)$ is the transfer function for the small signal opamp output v_0 to the small signal output v_{ref}. Substituting Equations 4.19 and 4.20 into Equation 4.21, we shall obtain

$$\begin{aligned}
v_{ref} &= v_o\beta(s)\alpha(s)h_4(s) + v_{dd}(h_2(s)\alpha(s)h_4(s) + h_1(s)h_4(s) + h_3(s)) \\
&= \alpha(s)\beta(s)(v_{ref} - v_{dd}h_3(s)) \\
&\quad + v_{dd}(h_2(s)\alpha(s)h_4(s) + h_1(s)h_4(s) + h_3(s)) \\
(1 - \alpha(s)\beta(s))v_{ref} &= v_{dd}(h_2(s)\alpha(s)h_4(s) + h_1(s)h_4(s) + h_3(s)(1 - \alpha(s)\beta(s))) \\
v_{ref} &= v_{dd}\left(\frac{h_2(s)\alpha(s)h_4(s) + h_1(s)h_4(s)}{1 - \alpha(s)\beta(s)} + h_3(s)\right).
\end{aligned}$$

As a result, the power supply rejection ratio is given by

$$\begin{aligned}
PSRR(s) &= \frac{v_{ref}}{v_{dd}} \\
&= h_3(s) + \frac{h_4(s)(h_1(s) + h_2(s)\alpha(s))}{1 - \alpha(s)\beta(s)}.
\end{aligned} \tag{4.22}$$

To further analyze Equation 4.22 would require us to investigate the transfer functions $h_1(s) \sim h_4(s)$, $\alpha(s)$, and $\beta(s)$. Let's first investigate $h_1(s)$ and $\alpha(s)$ by considering the small signal model of the opamp in Figure 4.19, where the opamp has an equivalent output resistor r_{out}, and two voltage controlled current sources i_{v_β} and $i_{v_{dd}}$, which are controlled by the differential input voltage v_β and the small signal power source v_{dd}, respectively. The transfer functions of these two voltage controlled current sources are given by

$$\begin{aligned}
v_\beta\alpha(s) &= i_{v_\beta}r_{out}, \\
v_{dd}h_1(s) &= i_{v_{dd}}r_{out}.
\end{aligned} \tag{4.23}$$

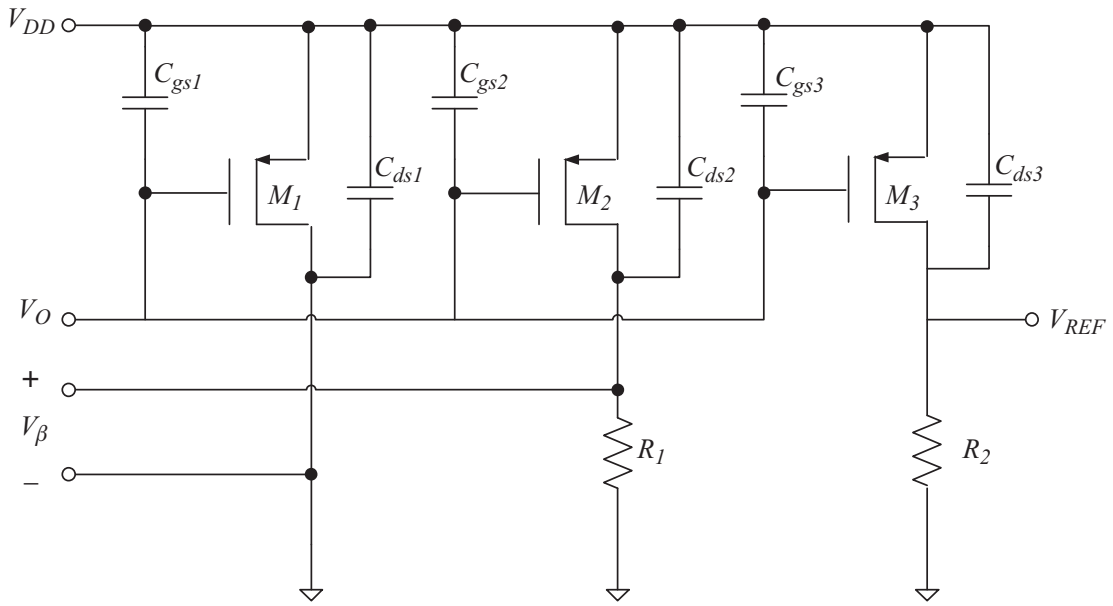


Figure 4.20 Small signal model of the bandgap core Figure 3.4.

Assume the differential voltage gain transfer function of the opamp contains only one pole, thus

$$\alpha(s) = A_{v_\beta} \frac{1}{1 + \frac{s}{p_a}}, \tag{4.24}$$

where A_{v_β} is the differential gain of the opamp to the differential input voltage v_β. Similarly, assume the transfer function $h_1(s)$ of the power supply noise of the opamp has one zero and one pole.

$$h_1(s) = A_{v_{dd}} \frac{1 + \frac{s}{z_1}}{1 + \frac{s}{p_1}},$$

where $A_{v_{dd}}$ is the gain of the opamp to the small signal power supply noise.

In a similar manner, the transfer functions $h_2(s)$, $h_3(s)$, $h_4(s)$, and $\beta(s)$ are investigated by considering the small signal model of the bandgap core in Figure 4.20. Comparing the equivalent block diagram in Figure 4.20 with that in Figure 3.4, the BJTs Q_1, Q_2, and Q_3 are assumed to have AC short-circuited in the small signal analysis. Those parasitic capacitors associated with the transistors M_1, M_2, and M_3 that have small values and are not in the major signal path are discarded, as they have almost no effect in the final analysis results. Furthermore, because of the Miller effect, the parasitic capacitor C_{gd} of transistors M_1, M_2, and M_3 can be neglected too. As a result,

$$\begin{aligned} \beta(s) &= \frac{g_{m_2}(R_1 // R_{M_2})}{1 + \frac{s}{p_\beta}} = A_\beta \frac{1}{1 + \frac{s}{p_\beta}}, \\ h_4(s) &= \frac{g_{m_3}(R_2 // R_{M_3})}{1 + \frac{s}{p_4}} = A_{h_4} \frac{1}{1 + \frac{s}{p_4}}, \end{aligned} \tag{4.25}$$

where R_{M_x} is the R_{DS} of transistor M_x, which equals $1/g_{m_x}$, and

$$p_\beta = \frac{1}{C_{ds_2}(R_1//R_{M_2})},$$
$$p_4 = \frac{1}{C_{ds_3}(R_2//R_{M_3})}.$$

Similarly

$$h_2(s) = \frac{g_{m_2}(R_1//R_{M_2})}{1+\frac{s}{p_2}} = A_{h_2}\frac{1}{1+\frac{s}{p_2}},$$
$$h_3(s) = \frac{g_{m_3}(R_2//R_{M_3})}{1+\frac{s}{p_3}} = A_{h_3}\frac{1}{1+\frac{s}{p_3}}, \tag{4.26}$$

where

$$p_2 = \frac{1}{C_{gs_2}(R_1//R_{M_2})},$$
$$p_3 = \frac{1}{C_{gs_3}(R_2//R_{M_3})}.$$

Since the transistor sizes of M_1, M_2, and M_3 are the same with only a small process variation, therefore, p_β, p_4, p_2, and p_3 can be approximated to be the same. Similarly, g_{m_2} and g_{m_3} should be almost equal and thus we can approximate A_{h_2}, A_{h_3}, A_{h_4}, and A_β to be the same. Hence, we can approximate $h_3(s)\beta(s) - h_4(s)h_2(s) \approx 0$, and thus Equation 4.22 will be approximately equal to

$$PSRR(s) = \frac{h_3(s) + h_4(s)h_1(s)}{1 - \alpha(s)\beta(s)}. \tag{4.27}$$

If we substitute Equations 4.24 $\sim$ 4.26 into Equation 4.27, and further approximate $p_1 \approx p_a$ and $p_3 \approx p_4 \approx p_\beta$, this yields

$$PSRR(s) = \frac{A_{h_3}\frac{1}{1+\frac{s}{p_3}} + A_{h_4}\frac{1}{1+\frac{s}{p_4}}A_{h_1}\frac{1+\frac{s}{z_1}}{1+\frac{s}{p_1}}}{1 - A_{v_\beta}A_\beta\frac{1}{1+\frac{s}{pa}}\frac{1}{1+\frac{s}{p\beta}}} \tag{4.28}$$

$$\approx \frac{A_{h_3} + A_{h_1}A_{h_4}}{1 - A_{v_\beta}A_\beta}\frac{1+\frac{s}{z_x}}{(1+\frac{s}{p_x})(1+\frac{s}{p_y})}$$
$$= PSRR(0)\frac{1+\frac{s}{z_x}}{(1+\frac{s}{p_x})(1+\frac{s}{p_y})}, \tag{4.29}$$

where

$$z_x = \frac{A_{h_3} + A_{h_1}A_{h_4}}{\frac{A_{h_3}}{p_a} + \frac{A_{h_1}A_{h_4}}{z_1}},$$
$$p_x = -(1 - A_{v_\beta}A_\beta)\frac{1}{\frac{1}{p_a} + \frac{1}{p_3}},$$
$$p_y = -(p_a + p_3).$$

It can be observed from Equation 4.29 that the frequency response of the $PSRR$ function of the opamp based β-multiplier bandgap voltage reference circuit has 1 zero and 2 poles, and the $PSRR$ at DC is given by

$$PSRR(0) = \frac{A_{h_3} + A_{h_1}A_{h_4}}{1 - A_{v_\beta}A_\beta} \approx \frac{-A_{h_3}}{A_{v_\beta}A_\beta} - \frac{A_{h_4}}{A_\beta}\frac{A_{h_1}}{A_{v_\beta}},$$

which is determined by the small signal gain A_{v_β}, the close loop gain A_β, and the $PSRR$ of the opamp given by $\frac{A_{v_\beta}}{A_{h_1}}$. As a result, increasing A_{v_β}, A_β, and the $PSRR$ of the opamp will effectively decrease $PSRR(0)$. The loop gain of the opamp based β-multiplier circuit has been derived in Section 3.3.1.2, and is shown to be able to obtain a large value. Similarly, it is relatively easy to design an opamp with an open loop gain that has large value and low $PSRR$. Therefore, $PSRR(0)$ are usually very small, and thus the opamp based β-multiplier bandgap voltage reference circuit has very good power supply noise suppression performance at low frequency. However, when the frequency under concerns increases to the power supply noise frequency and equals to, the first zero z_x in $PSRR(s)$, the power supply noise suppression capability will decay at a rate of 20 dB/decade. When the power supply noise frequency is between the frequencies of the two poles, p_x and p_y, the power supply noise suppression is the weakest. The power supply noise suppression capability of the opamp based β-multiplier bandgap voltage reference circuit will rise at a rate of -20 dB/decade after p_y. The $PSRR$ performance is graphically plotted in Figure 4.21 for the bandgap voltage reference circuit in Figure 3.11. Underneath the drawing, we have superimposed the $PSRR$ simulation result to make it easy to visualize the good match between the simulation result and the analytical result.

In particular, the worst case $PSRR$ is given by

$$\max_s(PSRR(s)) = PSRR(0) + \left(20\text{ dB}\frac{p_x}{z_x}\right).$$

Further analysis will show that p_x can be approximated by $A_{v_\beta}p_1\beta(s)$, where $A_{v_\beta}p_1$ is the bandwidth of the opamp. To increase the gain bandwidth of the opamp, we can increase the transconductance of the differential input transistor pairs of the opamp, or reduce the Miller frequency compensation capacitor (should the opamp contain a Miller capacitor for frequency compensation). However, if the Miller capacitor is too small, the opamp may not have enough

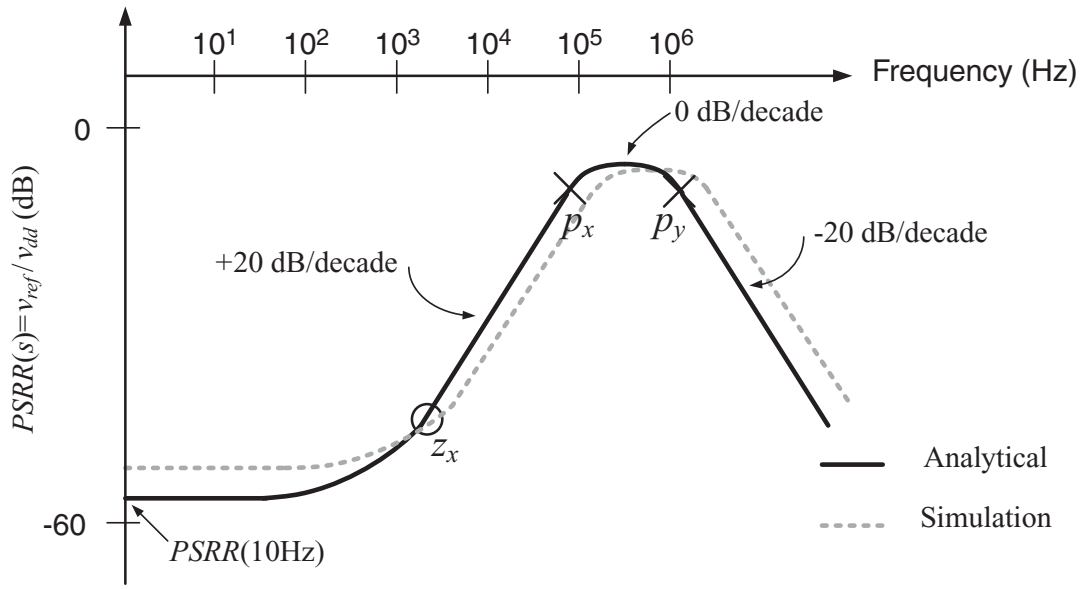


Figure 4.21 The $PSRR$ of the opamp based β-multiplier bandgpap voltage reference circuit obtained from a SPICE simulation being superimposed on the curve computed by Equation 4.29.

phase margin to maintain stable operation. On the other hand if we increase A_{v_β} to achieve a low $PSRR$ value, there may be a chance that the opamp will become unstable. At the same time, we notice that p_y is determined by the -3 dB frequency point of the current mirror formed by M_1, M_2, and M_3. To reduce this pole value, we can increase the length of the transistors, the working currents of the transistors, or the resistances of R_1 and R_2. Even though V_{REF} only depends on the resistance ratio of R_1 and R_2, increasing the resistance of either R_1 or R_2 will decrease the current to the BJTs (when V_{DD} is fixed), and thus may cause β variation problems as discussed in Section 4.3.3, and may even cause the the BJTs to have stability problem. This is because when the resistance is too large, the collector current may be too small, and thus cannot properly bias the BJTs to operate in the active region.

Note that most of the power supply noise is color in nature. As a result, the bandgap voltage reference circuit can be designed to have z_x, p_x, and p_y properly chosen, such that the power supply noise does not coincide with the $\max(PSRR(s))$. In this case the power supply noise can be suppressed appropriately, while there is not too much hammering of other performances of the bandgap voltage reference circuit.

4.5.1 Pre-Regulation

The simplest solution to improve the $PSRR$ of the voltage reference circuit is to place a RC filter in line with the V_{DD} as shown in Figure 4.22(a) to filter out fluctuations before they reach the voltage reference circuit. The RC filter will place a pole on the $PSRR$ curve as shown by Figure 4.23, where the pole $\frac{1}{2\pi R_F C_F}$ is added to the $PSRR$ curve by the RC filter. This pole will increase the supply noise suppression capability from -20 dB/decade to -40 dB/decade as shown by the dotted line in Figure 4.23. However the RC filter will reduce the voltage headroom of the voltage reference circuit due to the voltage drop across the resistor

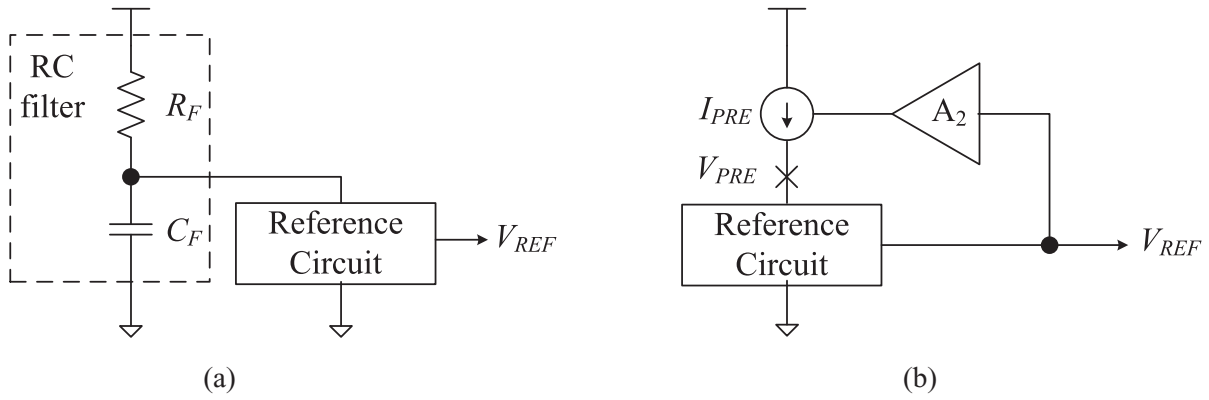


Figure 4.22 Methods to improve the $PSRR$ of voltage reference circuit by (a) in line RC filter, and (b) pre-regulation.

of the RC filter. Furthermore, the DC current flowing through this resistor equals the current consumed by the voltage reference circuit. As a result, a resistor with a large silicon layout has to be implemented such that the current density of the resistor is lower than its physical limit imposed by the fabrication process under concern. Furthermore, a RC filter pole at low frequency is desired for the best supply noise suppression result. Therefore, a capacitor with large capacitance, and hence large silicon layout, will be required. This will further increase the silicon size of the overall voltage reference circuit.

A better way to lower the loss in voltage headroom and reduce the implemented silicon size is to employ a "*pre-regulator*." A pre-regulator is formed by a negative feedback voltage regulation circuit (Books and Westwisk, 1994). This technique improves the voltage reference circuit $PSRR$ performance by increasing the resistance between V_{DD} and the supply of the voltage reference circuit. The core of the circuit is to use the reference voltage as the

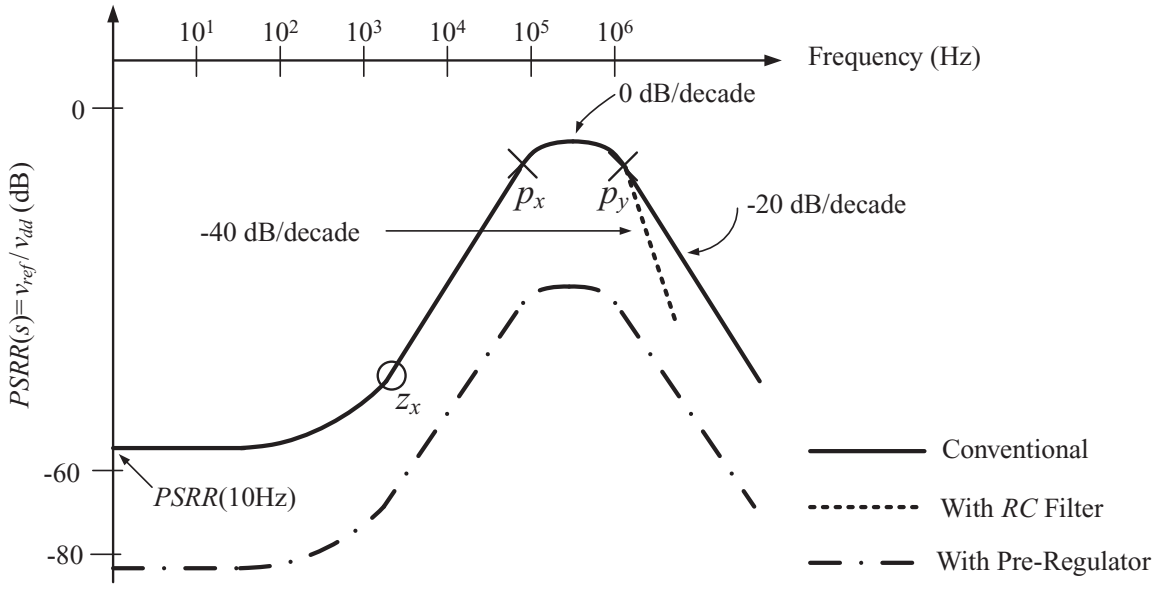


Figure 4.23 The solid line is the $PSRR$ of the conventional opamp based β-multiplier bandgap voltage reference circuit. The dotted line is the changes after adding an in line RC filter, and the dash-dotted line is the changes after adding a pre-regulator.

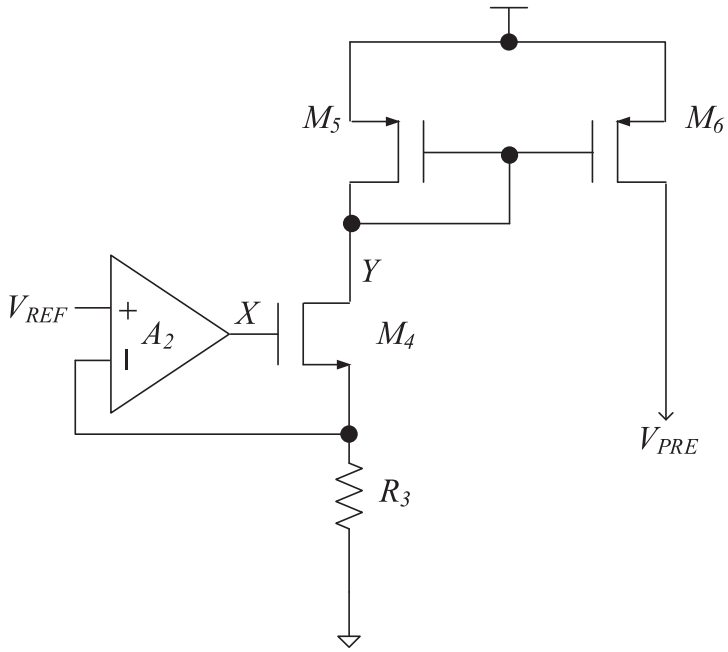


Figure 4.24 Schematic of voltage reference circuit with pre-regulator.

reference to a pre-regulator to generate a "*pre-regulated*" voltage V_{PRE}. This pre-regulated voltage is indeed the supply voltage to the bandgap voltage reference circuit. As a result, the power supply noise coupled to the bandgap core circuit is greatly reduced and this improves the $PSRR$ of the voltage reference circuit. The $PSRR$ of the pre-regulated voltage reference circuit ($PSRR_{REF}$) is determined by both the $PSRR$ of the pre-regulator ($PSRR_{PRE}$) and that of the bandgap voltage reference circuit core ($PSRR_{bandgap}$) as

$$PSRR_{REF} = PSRR_{PRE} \cdot PSRR_{bandgap}. \tag{4.30}$$

Obviously, the $PSRR_{REF}$ can be greatly enhanced by using a pre-regulator with a high $PSRR$. Figure 4.24 shows a detailed schematic of a pre-regulator applied to the bandgap voltage reference circuit. The pre-regulator is a linear regulator formed by opamp A_2 configurated as an error amplifier in a negative feedback loop with V_{REF} as a voltage reference and output driver M_4 and feedback resistor R_3.

Consider the power supply induced noise at node X in Figure 4.24, known as V_X, the ripple observed at node Y, V_{PRE} can be obtained as

$$\begin{aligned} PSRR_Y &= V_X \frac{g_{m_4}}{(1 + g_{m_4} R_3) g_{m_5}}, \\ PSRR_{PRE} &\approx PSRR_Y, \end{aligned} \tag{4.31}$$

where g_{m_4} and g_{m_5} are the transconductance of the transistors M_4 and M_5 respectively, and $S_5/S_6 = 1$. Note that

$$I_{R_3} = \frac{V_{REF}}{R_3},$$

which is copied by M_6 with respect to the ratio of the current mirror $S_5 : S_6$. As derived earlier in Section 4.5, the $PSRR$ of the opamp based β-multiplier bandgap voltage reference circuit is given by Equation 4.22. The size of the transistor M_6 is much larger than that of $M_1 \sim M_3$ in the opamp based β-multiplier bandgap voltage reference circuit. Therefore, it is safe not to consider the effect of C_{SD} in Equation 4.31 as the induced pole will be far away from the frequency of interest. Hence, the $PSRR_{REF}$ given by Equation 4.31 is almost flat across the frequency of interest. At the same time, it is easy to obtain $PSRR_{PRE}$ with a large magnitude, thus the $PSRR$ of the pre-regulated voltage reference circuit can be a lot lower than that of the opamp based β-multiplier bandgap voltage reference circuit as shown by the dash-dotted line in Figure 4.23, which is a vertical shift downwards when compared to the $PSRR$ curve obtained by conventional opamp based β-multiplier bandgap voltage reference circuit. While this is a compact and effective technique to achieve high $PSRR$ performance, the pre-regulator does consume a considerable amount of current, and hence lowers the power efficiency of the overall voltage reference circuit. Furthermore, the pre-regulated voltage in Figure 4.22(b) is greatly dependent on the $V_{th,p}$ of the transistor and the threshold voltage mismatch in the current mirror formed by M_5 and M_6 which generates the current source I_{PRE}. Note that $V_{th,p}$ can have $\pm 20\%$ variation which greatly sets back the line regulation and the temperature coefficient of the reference voltage.

4.6 Output Loading

Connecting an output load to the voltage reference circuit will affect the stability of V_{REF} in two ways: dynamic and static. The static effect of the output load is observed to be most severe when the output load impedance is small. Consider Figure 4.25 where a load resistor R_L is connected to V_{REF}. Inevitability, there will be $I_L > 0$ flowing out from I_3 into R_L. As a result, the output voltage V_{REF} will be changed to $\hat{V}_{REF}$ which is given by

$$\begin{aligned} \hat{V}_{REF} &= (I_3 - I_L)R_2 + V_{BE_3} \\ &= V_{REF} - I_L R_2 \\ &= V_{REF} - \hat{V}_{REF}\frac{R_2}{R_L}. \end{aligned} \tag{4.32}$$

It can be observed from Equation 4.32 that when R_L is small when compared to R_2, then will be large enough that it cannot be ignored. A large I_L will affect the PTAT voltage developed over R_2. Even if we assume the output loading is temperature insensitive, the inclusion of an output resistor will not only shift V_{REF} by an amount of $I_L R_2$, it will also affect the TC of V_{REF}. Such problems can be alleviated by the addition of an output buffer, such as a voltage follower formed by an invertly connected opamp as shown in Figure 4.26 at V_{REF} before connecting to R_L. Since the buffer has a high input impedance, the current required to drive the output buffer will be close to zero. As a result, the buffer will successfully isolate the interference from the load to the voltage reference circuit. On the other hand, the buffer will inevitability have an input offset error which will induce output voltage ambiguity, and degrade the reference voltage accuracy. Furthermore, the application of the output buffer will increase the power consumption of the overall voltage reference circuit. However, this design dilemma actually

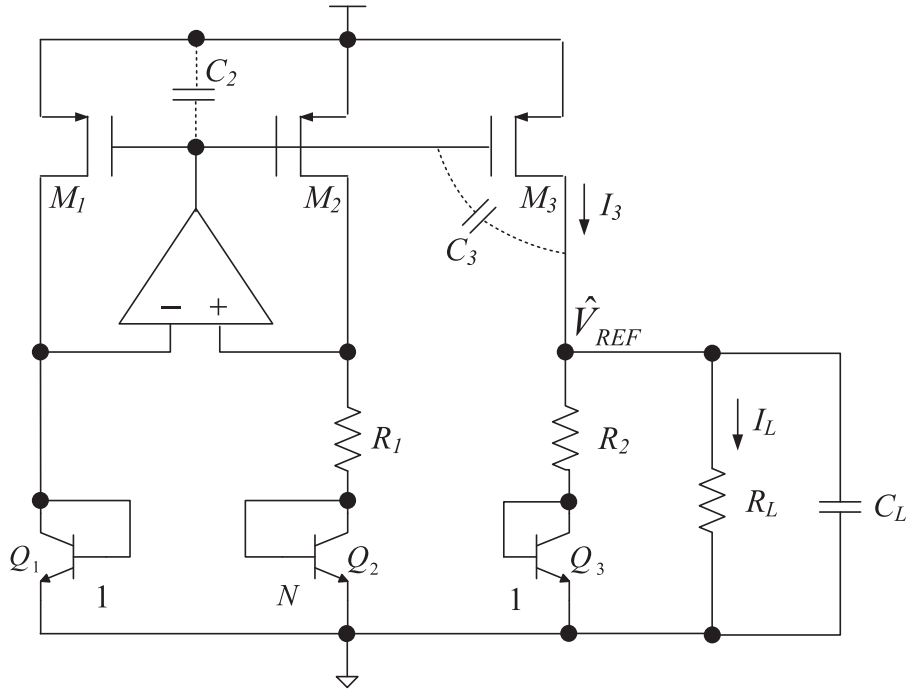


Figure 4.25 Opamp based β-multiplier bandgap voltage reference circuit with the consideration of output resistive and capacitive loading effect on the reference voltage.

originates from the high output current requirement and thus the addition of an output buffer may be essential due to the special request of the application under consideration.

Moreover, the output current problem may not be static in nature. When a time varying capacitive load is connected to V_{REF} of Figure 3.4, it will affect the output accuracy of the voltage reference circuit in a dynamic manner. Because of the charge sharing effect between the capacitive load C_L and the parasitic capacitance C_3 (the gate to drain capacitance $C_{gd,3}$ of M_3), and C_2 (which is largely contributed by the gate to source capacitance C_{gs} of $M_1 \sim M_3$) when the value of C_L changes, a voltage will be temporary induced on C_2 and C_3. Such a voltage will affect the gate voltage of the associated transistors, and thus affect the voltage of V_{REF}. The problem can be improved by connecting a large output capacitor in parallel

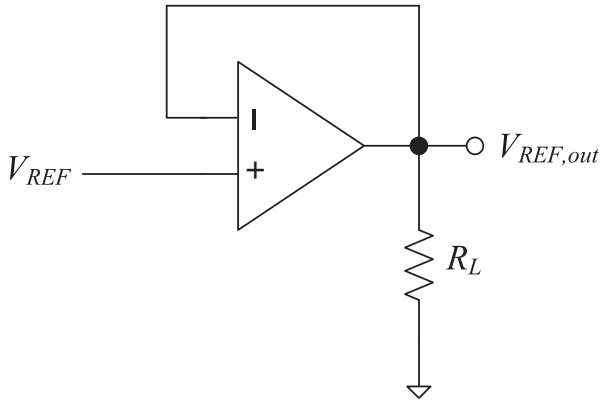


Figure 4.26 Reference voltage output buffer for large load R_L.

with C_L. The large output capacitor will suppress the load variations by lowering the output impedance. However, the use of a large output capacitance is prohibited in a voltage reference circuit embedded in the CMOS VLSI. If the capacitor is going to be off the chip, an extra output pin is required in the integrated circuit to accommodate the connection. On the other hand, the load variation can also be suppressed by increasing the output impedance of the transistors. However, the output impedance of the circuit is related to the output impedance of the current mirror which, as discussed in Section 3.3.2, does not have a simple way to increase the output impedance. Any attempts to modify the current mirror to achieve a higher output impedance will have two implications: A larger silicon area will be required for the overall voltage reference circuit, and larger output power will be required for the opamp to drive the transistors. This is not only because the increase in silicon size of current mirror will increase both the capacitive and resistive loads connected to the opamp. It is also because of the output impedance of the equivalent circuit of the opamp is connected in parallel to the input impedance of the current mirror, the increase of both the resistive and especially the capacitive loads will decrease the low frequency gain of the opamp, increase the frequency of the major pole, and hence increase the stability of the close loop β-multiplier circuit. An alternative method to alleviate the problem of time varying output loading is to use a high output impedance opamp, such that the β-multiplier has a fast enough response to maintain stability and output voltage. The output impedance of the opamp can be improved by connecting the opamp in the current mirror via a NMOS transistor M_5, such as to avoid the direct connection to the current mirror, and hence avoid the output impedance of the opamp being connected in parallel with the input impedance of the current mirror. Figure 4.27 shows one such circuit, where the output

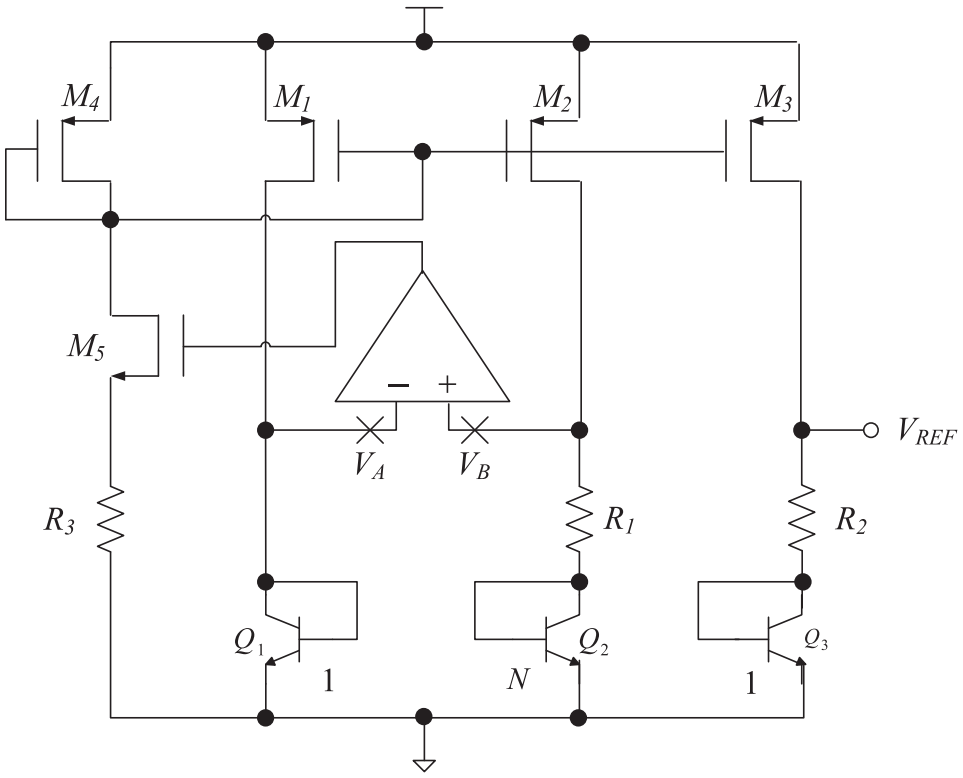


Figure 4.27 Improving the load regulation of the opamp based β-multiplier bandgap voltage reference circuit using a buffer amplifier formed by M_4 and M_5 (Hoon *et al.* 2002).

of the opamp will drive M_5, which is connected to the current mirror of the β-multiplier via the current mirror formed by M_4, M_1, M_2, and M_3. Such circuit is first proposed in (Hoon *et al.* 2002). Although the transconductance of M_4 and M_5 can help to increase the gain of the opamp in the β-multiplier loop, the transconductance product of M_4 and M_5 are usually designed to be at unity such as not to affect the loop stability of the β-multiplier circuit.

4.7 Output Noise

When the accuracy and temperature independence of the voltage reference circuit increases, the major error source of the generated voltage will then be in the order of a few ppm/K over a temperature range of 100 K. Consequently, the output noise of the reference voltage will become more and more important. For instance, consider a voltage reference circuit with the desired output voltage at 200 mV with a mean temperature variation of 2 ppm/K. In other words, the mean uncertainty due to temperature dependency of the desired voltage reference circuit should be at most 0.4 μV/K. When the equivalent noise voltage at the voltage reference circuit output is higher than this value, the noise of the bandgap reference will become the dominant source of the reference voltage uncertainty. To be able to analyze the noise level of the voltage reference circuit analytically, all the noise sources in the voltage reference circuit have to be transformed to the output.

Consider the transistor level opamp based β-multiplier bandgap voltage reference circuit in Figure 3.11. The transistors $M_4 \sim M_8$ formed the opamp. The current mirror formed by M_1, M_2, and M_3 has $S_1 : S_2 : S_3$ equal to $1 : 1 : N_1$. The two BJTs Q_1 and Q_2 have an emitter area ratio equal to $N_2 : 1$. As a result, the reference voltage is given by

$$V_{REF} = V_{BE_3} + N_1 \frac{R_2}{R_1} \ln(N_2) V_T .$$

A near-zero TC reference voltage equals to 1.23 V is obtained when $N_1 \ln(N_2) \frac{R_2}{R_1} = 19.22$.

The equivalent output noise of the opamp based β-multiplier bandgap voltage reference circuit can be computed by considering the noise contributed by each MOSFET to the differential input of the opamp and then multiplied by the total gain of the system computed in Section 3.3.1.2 and added to the noise model of M_3. Listed in the following is the thermal noise contributed by each transistor with the system gain considered.

$$\overline{V^2_{\eta_T, M_7}} = \overline{V^2_{\eta_T, M_8}} = \frac{4kT\gamma g_{m_7}}{g^2_{m_5}} (A_{total})^2 , \tag{4.33}$$

$$\overline{V^2_{\eta_T, M_5}} = \overline{V^2_{\eta_T, M_6}} = \frac{4kT\gamma}{g_{m_5}} (A_{total})^2 , \tag{4.34}$$

$$\overline{V^2_{\eta_T, M_2}} = 4kT\gamma g_{m_2} (R_1 + R_{Q_2})^2 (A_{total})^2 , \tag{4.35}$$

$$\overline{V^2_{\eta_T, M_1}} = 4kT\gamma g_{m_1} R^2_{Q_1} (A_{total})^2 , \tag{4.36}$$

$$\overline{V^2_{\eta_T, M_3}} = 4kT\gamma g_{m_3} \left(R_2 + R_{Q_3}\right)^2 , \tag{4.37}$$

The flicker noise contributed by each transistor with system gain considered are listed in the following

$$\overline{V^2_{\eta_{1/f},M_7}} = \overline{V^2_{\eta_{1/f},M_8}} = \frac{K_n g^2_{m_7}}{C_{ox,n} W_7 L_7 f g^2_{m_5}} (A_{total})^2 , \tag{4.38}$$

$$\overline{V^2_{\eta_{1/f},M_5}} = \overline{V^2_{\eta_{1/f},M_6}} = \frac{K_p}{C_{ox,p} W_5 L_5 f} (A_{total})^2 , \tag{4.39}$$

$$\overline{V^2_{\eta_{1/f},M_2}} = \frac{K_p g^2_{m_2} (R_1 + R_{Q_2})^2}{C_{ox,n} W_2 L_2 f} (A_{total})^2 , \tag{4.40}$$

$$\overline{V^2_{\eta_{1/f},M_1}} = \frac{K_p g^2_{m_1} R^2_{Q_1}}{C_{ox,p} W_1 L_1 f} (A_{total})^2 , \tag{4.41}$$

$$\overline{V^2_{\eta_{1/f},M_3}} = \frac{K_p g^2_{m_3}}{C_{ox,p} W_3 L_3 f} (R_2 + R_{Q_3})^2, \tag{4.42}$$

where K_n and K_p are process dependent parameters and are constants as defined in Section 1.7.1.3. By analyzing the noise contributed by each transistor, we can reduce the output noise. A typical output signal spectrum of the reference voltage obtained from the SPICE simulation of the opamp based β-multiplier bandgap voltage reference circuit is shown in Figure 4.28. It can be observed that the output noise is dominated by the low frequency noise. This is because the low frequency flicker noise has very large RMS value. The flicker noise can be reduced by increasing the size of the transistors as discussed in Section 1.7.1.3. Observed from Equation 4.33, 4.34, and 4.38, increasing the transconductance of M_5 and M_6 will reduce the thermal noise. Increasing the size of M_7 and M_8 will reduce the flickering noise. Reducing the transconductance of M_7 and M_8 will reduce the thermal and flickering noise.

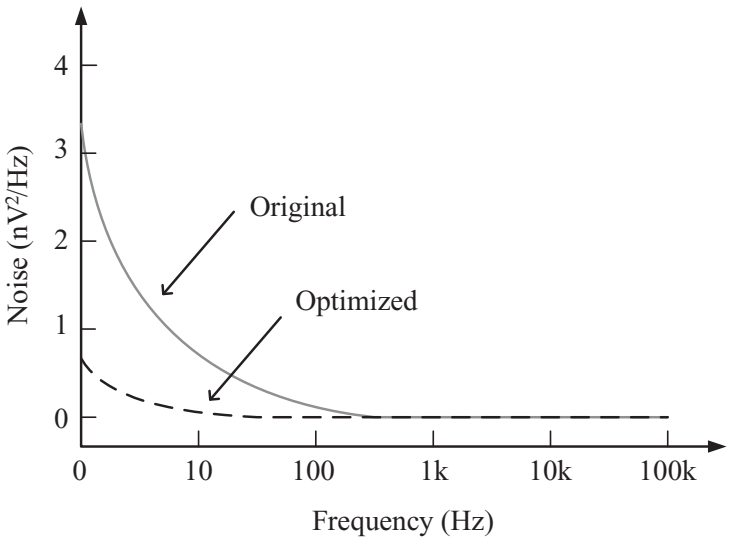


Figure 4.28 Reference voltage spectrum of opamp based β-multiplier bandgap voltage reference circuit in Figure 3.11 with transistor size given by SPICE netlist in Appendix B and that of the same circuit with the optimized transistor sizes.

As a result, we can conclude that increasing the W and L of $M_5 \sim M_8$ will increase the channel area of the transistors and thus reduce the flickering noise from the channel of the MOSFETs. However, care has to be taken when increasing W and L, because this will affect the transconductance of the transistors and affect the loop stability of the β-multiplier circuit. Reducing the W/L of $M_1 \sim M_3$ will reduce the transconductance, which helps to reduce the thermal noise. While increasing the W and L of $M_1 \sim M_3$ will help to reduce the flickering noise. In the case of M_5 and M_6, the W/L should be large, while that of M_7 and M_8 should be small.

The noise spectrum of the reference voltage obtained by the opamp based β-multiplier bandgap voltage reference circuit in Figure 3.11 with a transistor size given by the SPICE in the netlist in Appendix B, and that of the same circuit with optimized transistor sizes discussed in this section, are shown in Figure 4.28 (solid line for the original voltage reference circuit and dotted line for the circuit with optimized transistor sizes). Comparing the two curves reveals that the noise power of the voltage reference circuit with optimized transistor sizes can reduce the noise power at low frequency. The flickering noise spectral corner has reduced from 100 Hz to 10 Hz with the flicker noise in the low frequency has been reduced. At the frequency range from 10 Hz to 100 kHz, the output noise has been reduced from a maximum of over 300 μV to less than 90 μV. The drawback of the optimization is the increased operating current, which rises from 27 μA to 57 μA.

The output noise can also be reduced by connecting a large capacitor to V_{REF}, which acts as a lowpass filter with low corner frequency. However, given the constraints on silicon area imposed by modern CMOS integrated circuits, using large on-chip capacitors is often not viable. The situation is exacerbated in the sub-1V voltage reference circuit, where the noise to nominal reference voltage ratio is large because of the small magnitude of the nominal voltage. As a result, it is more important than just a list of analytical expressions, the analytically derived transistor sizings are the key to alleviating the noise problem in voltage reference circuit.

4.8 Voltage Reference Circuit Trimming

Any devices incorporated in an integrated circuit will generally deviate from the designed values due to variation in the manufacturing environment. Such manufacturing variation is also known as process variation, which will translate to reference voltage variation. To achieve the accuracy required by the voltage reference design specification beyond the limits of the manufacturing condition, it is common practice to calibrate the fabricated circuit by "*trimming*", which is a post-fabrication circuit adjustment technique. Note that the voltage reference circuit is required to meet the required accuracy specification, therefore the trimming circuit has to exploit available knowledge about the dependency of the error to the performance of the voltage reference circuit. Previous sections in this chapter have already demonstrated the many sources of errors affecting the reference voltage, which implies there are many ways to trim the reference voltage. However, trimming at more than one circuit element is very expensive, in both silicon area and post-processing time. Therefore, a typical trimming procedure only provides the calibration of one circuit element to adjust a particular parameter of the reference voltage circuit. Although this approach cannot give a voltage reference circuit with optimal performance, it can provide a voltage reference circuit with acceptable performance at an acceptable cost in most cases. The decision over which element to be

trimmed is mostly application specific, therefore we have no intention of discussing it here. On the other hand, we would like to point out that due to the nature of the bandgap voltage reference circuit topology, the correctional circuits are most commonly constructed in the form of resistor array for modulated domain trimming, BJT transistor array for voltage domain trimming, and current mirror transistor array for current domain trimming. These trimming techniques will be discussed in Section 4.8.3, Section 4.8.4, and Section 4.8.5, respectively. Note that even if a particular trimming element is selected, there are still a number of ways to calibrate that part of the circuit. Among the large number of trimming methods available nowadays, we shall discuss the two most commonly applied trimming methods in this section. In particular, we shall focus on the discussion of resistor value calibration, while the discussed method can be applied to the calibration of component values of other electron devices. The first method is laser trimming of a thin film metal resistor. The second method is selective open circuit of a metal fuse by a large current which results in a corrected circuit.

Consider the voltage domain trimming through calibration of a resistor value, which can be achieved by (i) using a digital string of 1s and 0s (a trim code) that control on-chip switches to open and/or short-circuit a number of binary weighted resistors connected in series, or (ii) reshaping and therefore resizing the resistor with a laser beam. The accuracy of the former is limited by the smallest value of the element in the binary weighted resistor chain. In other words, it is determined by the resistance that corresponds to the least significant bit (LSB) of the trim code. Reducing the LSB resistance to obtain high resolution while maintaining the trim-range of the overall resistance to be the same typically translates into the employment of a large number of trim bits which are always constrained by silicon area and test-time boundaries. Furthermore, connected to each end of a fuse are two probe pads, or known as trimming pads, roughly a square with 70 μm per each side. Through these probe pads, a current in the order of mA is applied to selected fuses and by so doing blows open the fuse. However, these probe pads are extremely large when compared to the size of the resistor. Furthermore, the number of probe pads increases linearly with the number of trimming elements. Therefore, with the trimming precision directly related to the number of trimming elements, it becomes clear that in order to achieve precise reference voltage, more silicon area is needed. This poses a design paradox on both precision and cost in the design of the high precision voltage reference circuit.

Laser trimming, on the other hand, is more accurate and area efficient and therefore is oftenly used in high performance voltage reference circuits. However, the laser energy sufficient to trim metal film can often cause substrate damage, and hence lower the yield of the functional device. Moreover, the inherent cost in test time and equipment often prohibits the application of laser trimming to the voltage reference circuit. In the following we shall discuss the metal fuse (also known as "*linked*" fuse) trimming technique, which is usually applied in voltage reference circuits due to cost considerations and which can also provide the adequate accuracy required by the final application of the trimmed voltage reference circuit.

4.8.1 Linked Fuse Resistor Trimming

Traditional metal fuse is typically fabricated from aluminum in a "*blow-tie*" configuration as shown in Figure 4.29. As can be seen from the figure, the linked fuse resistor contains a metal fuse with resistance R_{fuse}, and a resistor with resistance R_{trim} connected in parallel between

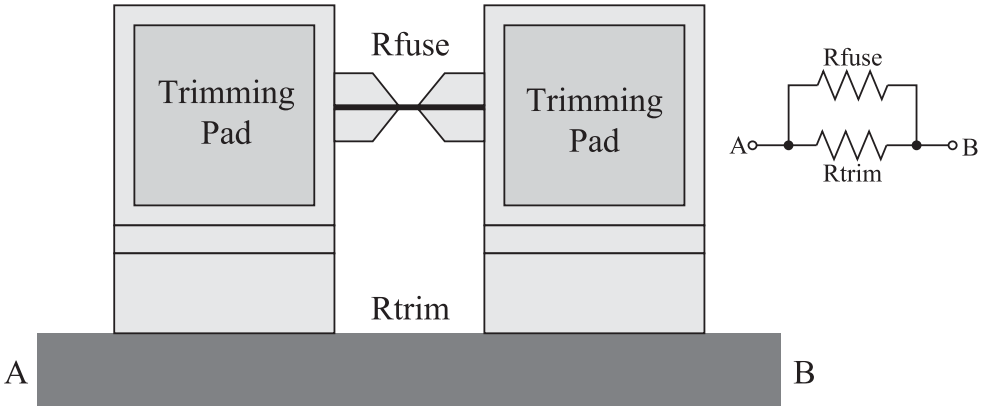


Figure 4.29 A typical linked fuse resistor.

the two trimming pads. When the fuse is intact, the resistance observed between nodes (A, B) is approximately equal to R_{fuse}, which is usually considered to be zero because of the low resistance of the metal fuse connection. The metal fuse can be blown open by applying a high current between the trimming pads. When the current flows through the fuse induces a current density higher than that which can be supported by the metal structure of the fuse and it heats up. When enough heat has built up on the fuse, it will melt the metal and blow open the fuse. After the fuse is blown open, the resistance observed between nodes A and B will equal R_{trim}. As a result, the linked fuse resistor trimming structure is a "*up-trimming*" structure, which means that the resistance increases with the fuse being broken. Anti-fuse resistor trimming structures and CMOS switch structures exist that can achieve "*down-trimming*" structures, where the trimmed resistance decreases with the fuse being broken. Of the two trimming structures, the up-trimming structure is most commonly used. There are also two basic ways of trimming. The first is known as "*static-trimming*" and is a means of adjusting the resistor value without power being applied. The second is known as "*dynamic-trimming*" or "*functional-trimming*," which consists of adjusting a resistor to obtain a specified reference voltage (in terms of the voltage reference circuit) while power is being applied to the circuit. Dynamic trimming will be of importance to voltage reference circuit implementations because that refers to the actual operating conditions.

Among various resistor trimming structures, linked fuse trimming is the process of selecting a desired resistance from a series of geometrically increasing resistors fused together by the metal fuse. For a trimming resistor network with M resistors, the resistance will increase from R_x to $2^k R_x$ that connects between the k and $(k+1)$-th trimming pads, all the way to $2^{M-1} R_x$ (similar to that shown in Figure 4.30). The precision is directly related to the number of resistors in the linked resistor array. Therefore it becomes clear that in order to achieve high precision resistor value, a large silicon area is required. As a result, this poses a design dilemma on the cost (both the cost of the silicon area and the cost of the machine hours to perform the trimming) and the output precision of the voltage reference circuit.

4.8.2 Resistor Trimming Circuit Analysis

Trimming is necessary to produce a predictable reference voltage. However, arbitrarily trimming a circuit to any target voltage can be detrimental. There are two problems associated

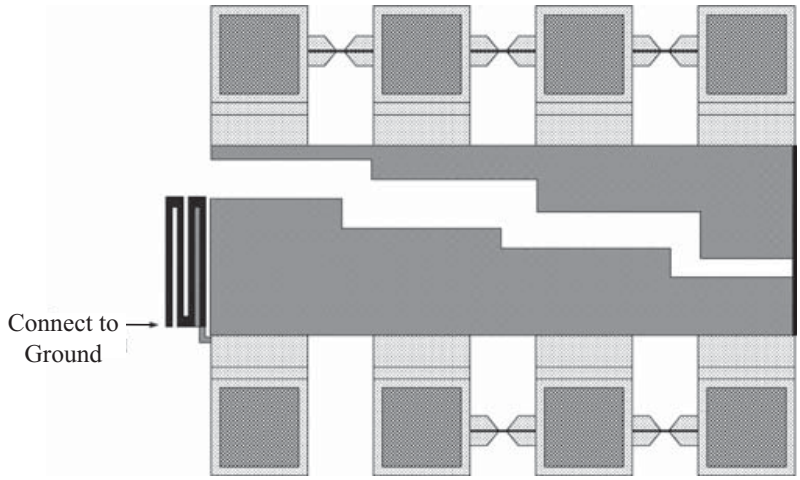


Figure 4.30 (a) Layout of linked fuse resistor array, and (b) the associated schematic.

with the trimming circuit and procedure. First, we analyzed in Chapter 3 that there is only one target voltage that achieves the lowest temperature coefficient. Hence the trimming circuit and procedure should be designed to cover and be able to achieve this target voltage. Second, the trimming circuit and procedure should be designed to achieve the target voltage with sufficient accuracy. The trimming circuit has to set up with enough fuses, m, to obtain a particular accuracy $\pm b\%$ for the target voltage when the input voltage has a variation of $\pm a\%$. Note that a trimming circuit designed with more than enough fuses will occupy a large silicon area and complicate the trimming procedure. Both of these will increase the cost of the voltage reference circuits.

To understand how to design a suitable trimming circuit for a voltage reference circuit, let's consider a voltage divider implemented with trimming resistor that allows alterations of the voltage ratio as shown in Figure 4.30(b). There are five fuses in the circuit, which will control the connections of five dyadic encoded resistors. As a result, by blowing up the appropriate fuses, the resistor that connects R_b and V_{OUT} can have the resistance values of mR_x where $m = 0, 1, \ldots, 31$. Let's denote the target voltage to be obtained from V_{OUT} through this resistive sub-divider as $\bar{y}$, with the desired input voltage as $\bar{x}$, where y and x are used to denote V_{OUT} and V_{IN} respectively for simplicity in the analysis. The trimming circuit in Figure 4.30(b) can obtain a different V_{OUT} from V_{IN} by blowing different fuse sets. With five fuses showing in the figure, we can obtain the following V_{OUT}

$$V_{OUT} = \frac{R_b + R_a + mR_x}{R_b} V_{IN}, \qquad m = 0, 1, \ldots, 31, \tag{4.43}$$

where the range of m of the resistance of the trimmed resistor is determined by $m = 5$, which is $0 \leq m \leq 2^5 = 32$. Such a voltage generation method can be analyzed by considering the model

$$k = \frac{y}{x} = \frac{V_{OUT}}{V_{IN}}. \tag{4.44}$$

In other words, the factor $(R_b + R_a + mR_x)/R_b$ in Equation 4.43 is equivalent to the factor k in Equation 4.44. Without loss of generality, the desired output voltage is assumed to be equal to $(R_b + R_a + 2^{n-1}R_x)V_{IN}/R_b$, such that half of the fuses are required to be blown to obtain the desired V_{OUT} when V_{IN} has no variation, that is $V_{IN} = \bar{x}$.

4.8.2.1 Model Analysis

For a given m, there exists $2^m = N$ different V_{OUT} values for a given V_{IN}. Without loss of generality, let's consider the set $k_1 < k_2 < \cdots < k_n$. When the input voltage variation $\hat{x} = \frac{x}{\bar{x}}$ from the desired voltage $\bar{x}$ is limited to the range $[1 - a, 1 + a]$, we can choose an appropriate k_ℓ, such that the output voltage variation $\hat{y} = \frac{y}{\bar{y}}$ from the desired output $\bar{y}$ with $y = k_\ell x$ is limited to the range $[1 - b, 1 + b]$. It can be observed from Equation 4.30 that when $\hat{x} > 1$, we should choose $k_\ell > 1$, while $\hat{x} < 1$, will require $k_\ell < 1$. The boundary conditions for both $\hat{x}$ and $\hat{y}$ to achieve their maximum variations are given by

$$k_1(1 + a) - 1 = b, \tag{4.45}$$

$$\text{and} \qquad 1 - k_N(1 - a) = b. \tag{4.46}$$

where k_ℓ are given by

$$k_\ell = k_1 + (\ell - 1)\Delta k, \qquad \ell = 1, 2, \ldots, N,$$
$$\text{with} \qquad \Delta k = (k_N - k_1)/(N - 1).$$

With respect to each k_ℓ, there is a corresponding quantized region $\hat{x}_\ell = [\hat{x}_{\ell,1}, \hat{x}_{\ell,2}]$ in the dynamic range of $\hat{x}$. As a result, $k_\ell \hat{x}_\ell \in [1 - b,\ 1 + b]$. In other words,

$$k_\ell \hat{x}_{\ell,1} - 1 = b,$$
$$1 - k_\ell \hat{x}_{\ell,2} = b.$$

Solving the above two equations yields

$$\hat{x}_{\ell,1} = (1 + b)/k_\ell, \tag{4.47}$$

$$\hat{x}_{\ell,2} = (1 - b)/k_\ell. \tag{4.48}$$

We can observe that Equations 4.47 and 4.48 establish N regions of k: $[\hat{x}_{1,1},\ \hat{x}_{1,2}]$ $[\hat{x}_{2,1},\ \hat{x}_{2,2}]$ $\cdots$ $[\hat{x}_{\ell,1},\ \hat{x}_{\ell,2}]$ $\cdots$ $[\hat{x}_{N,1},\ \hat{x}_{N,2}]$. At the same time, the boundary condition establishes $\hat{x}_{1,1} = 1 + a$, and $\hat{x}_{N,2} = 1 - a$. As a result, the above N quantized regions in $\hat{x}$ can be considered as $\hat{x}$ in one of the N sub-divided regions in the range of $[1 - a,\ 1 + a]$. In particular, if there are no gaps between these N regions, then

$$\hat{x}_{1,2} \le \hat{x}_{2,1},\ \hat{x}_{2,2} \le \hat{x}_{3,1}, \ldots,\ \hat{x}_{\ell,2} \le \hat{x}_{\ell+1,1}, \ldots, \hat{x}_{N-1,2} \le \hat{x}_{N,1}.$$

Together with the boundary condition that $\hat{x}_{\ell,2} \leq \hat{x}_{\ell+1,1}$, we shall obtain

$$\frac{(1-b)}{k_\ell} \leq \frac{(1+b)}{k_{\ell+1}}. \tag{4.49}$$

As a result, k_ℓ can be obtained by Equations 4.45, 4.46 and 4.49 as

$$k_\ell = \left\lceil \frac{1-b}{1+a} \right\rceil + (\ell-1)\frac{\left\lceil \frac{1-b}{1-a} \right\rceil - \left\lceil \frac{1+b}{1+a} \right\rceil}{N-1}, \qquad \ell = 1, 2, \ldots, N. \tag{4.50}$$

Substituting Equation 4.50 into Equation 4.49 yields

$$N \geq \frac{(k_N - k_1)(1+b)}{2k_1 b} + 1 + \frac{\ell(k_1 - k_N)}{k_1}. \tag{4.51}$$

Note that

$$\frac{k_1 - k_N}{k_1} = \frac{2(b-a)}{(1+b)(1-a)}.$$

Furthermore, the variation of V_{OUT} cannot be larger than that of V_{IN} in this voltage divider circuit, therefore, $0 < b < a < 1$. As a result,

$$\frac{k_1 - k_N}{k_1} < 0.$$

Therefore, the right hand side of the inequality in Equation 4.51 will achieve its maximum value when ℓ is the smallest, that is $\ell = 1$. In other words, the minimum value of m is given by

$$\min(N) = \left\lfloor \frac{(a-b)(1-b)}{b(1-a)(1+b)} + 1 \right\rfloor + 1, \tag{4.52}$$

where the floor operator, ($\lfloor \cdot \rfloor$) will retain the largest integer smaller than the content.

In conclusion, to achieve a scaled output voltage with accuracy $\pm b$ from an input voltage with accuracy $\pm a$ from a resistor network, we need to have at least m fuses for trimming, with $2^m \geq N$, where N is given by Equation 4.52. With a given m, we shall obtain $N = 2^m$ which will yield a trimming range given by Equation 4.50.

At the same time, this set of equations can also be used to explore the trimming accuracy with a given number of fuses, and each trimming range within the trimming network. In order to make use of this set of equations to find the input accuracy $\pm b$ required to achieve a given output voltage accuracy $\pm a$ and the number of trimming sections m, we shall consider the inequality $\hat{x}_{1,2} \leq \hat{x}_{2,1}$. The boundary condition is obtained when $\hat{x}_{1,2} = \hat{x}_{2,1}$, and together with Equation 4.47, we can rewrite Equation 4.50 as

$$c_2 x^2 + c_1 x + c_0 = 0, \tag{4.53}$$

where $c_2 = 2 - \frac{2}{(1-a)(N-1)}$, $c_1 = 2 + \frac{2(1+a)}{(1-a)(N-1)}$, $c_0 = \frac{-2a}{(1-a)(N-1)}$, $x = b$, and $N = 2^m$, with m being the number of fuses. One of the roots of Equation 4.53 is positive, while the other is negative. The positive root should be chosen as b, which is the required input voltage accuracy to achieve an output voltage with $\pm a$ accuracy using m bits dyadic resistive divider trimming structure. As an example, solving for x in Equation 4.53 with a 5-bit dyadic resistive divider trimming network (i.e., 5 fuses) to achieve an output voltage accuracy equal to $\pm 15\%$ will require $\hat{x} = 0.000543$, or $\hat{x} = -1.09024$. As a result, the required input voltage accuracy is $\pm 0.543\%$.

4.8.3 Modulated Trimming

Resistor trimming is trimming the physical property of the resistance of a resistor in the opamp based β-multiplier bandgap voltage reference circuit such that the output voltage of the voltage reference circuit is altered to achieve the target voltage. Besides resistor trimming, there are a number of components within the voltage reference circuit whose physical properties can be trimmed to alter the output voltage of the voltage reference circuit. The physical properties that can be trimmed include the voltage and current property of the devices. As a result, the trimming methods are also known as *"voltage trimming"* and *"current trimming"*. These two methods will be detailed in the following two sections.

Unlike voltage trimming and current trimming, resistor trimming has an indirect effect on the output voltage of the voltage reference circuit. Trimming the resistor will affect the induced voltage/current, and hence such trimming methods are known as *"modulated trimming"*. Among all the resistors in the opamp based β-multiplier bandgap voltage reference circuit, we shall consider the trimming of resistor R_2 that converts the PTAT current to PTAT voltage to achieve the target voltage. Figure 4.31 shows a modulated trimming structure of R_2 with 3 fuses. In the same figure you can also find voltage domain trimming of Q_2 with 3 fuses and current domain trimming of M_3 with 3 fuses, which will be discussed in Section 4.8.4, and 4.8.5, respectively.

4.8.3.1 Trimming Procedure

In order to trim a resistor to achieve the target reference voltage, a procedure has to be perfected in order to avoid over-trimming and ultimately scrapping the integrated circuit. This section will describe a particular trimming procedure which is useful for trimming R_2 in Figure 4.31 along with discussions on how it was developed.

It can be observed from Equation 3.12 that the output voltage V_{REF} is linearly proportional to R_2. By rewriting Equation 3.13 as the following

$$y = mx + b, \tag{4.54}$$

where a linear trimming model is adopted, such that $y = V_{REF}$, $x = R_2$, and $b = V_{BE_3}$. Note that $b = V_{BE_3}$ is the y-intercept of the linear equation in Equation 4.54, and the slope m of the

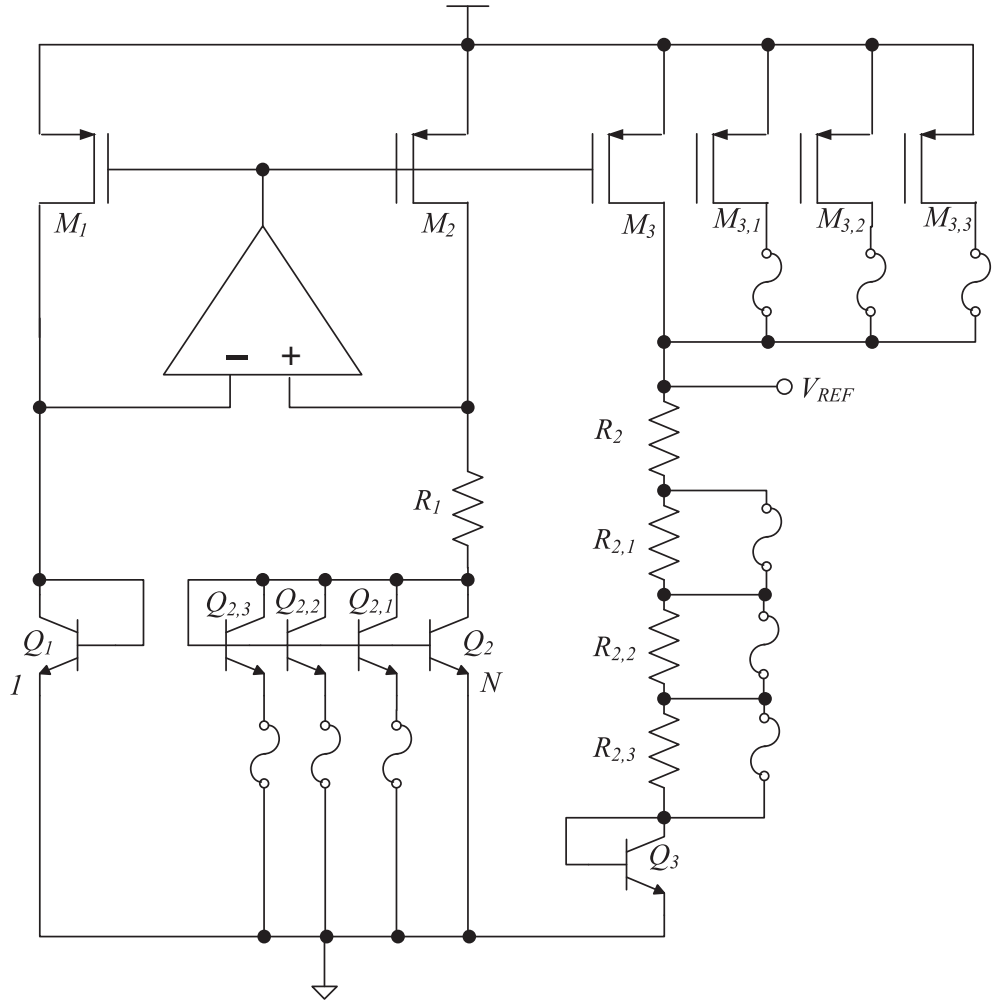


Figure 4.31 Opamp-based β-multiplier bandgap voltage reference circuit with resistor array modulated trimming structure, BJT array voltage domain trimming structure, and MOSFET array current domain trimming structure.

linear equation can be obtained from any two particular values of the (x, y) pair as

$$m = \frac{V_{REF,k+1} - V_{REF,k}}{R_{2,k+1} - R_{2,k}} = \frac{V_{REF,k+1} - V_{REF,k}}{\Delta R_{2,k+1}},$$

with $V_{REF,k}$ and $R_{2,k}$ being the measured reference voltage and resistance of R_2 at the k-th trimming procedure, with $k = 0$ being the untrimmed value. As a result, an initial trim is required in order to start making any calculation of the trim resistor value using the trimming model in Equation 4.54. The parameter $\Delta R_{2,k+1}$ denotes the difference of the resistance of R_2 after the $(k + 1)$-th and k-th trimming. The y-intercept of V_{REF} given by Equation 4.54 can be solved as

$$b = \frac{V_{REF,k+1}}{m R_{2,k+1}}.$$

The next trimming should then be made according to the calculated resistor value using the model in Equation 4.54. Note that the following trimming procedure assumes the resistor ratio does not change even thought the actual resistor values with the resistor array that makes up R_2 can have large variations. Such an assumption is considered to be valid because the resistor ratio can be fabricated with high accuracy, as discussed in Section 1.4.

Consider the case that the desired voltage is $V_{REF} = 1.23$ V. The trimming procedure would aim at a particular resistance of R_2 that satisfies the trimming model in Equation 4.54 with the desired V_{REF}. In other words, we are aimming at

$$x = \frac{1.23 - b}{m}.$$

The fuse needed to be blown in order to complete this trim is obtained by subtracting the calculated x with the current resistive value, which is also known as ΔR_2.

$$\Delta R_2 = x - R_{2,k},$$

where the previous trimming procedure is k, and thus the current trimming procedure is $k + 1$. As a result, the fuse associated with the resistor $R_{2,k}$ that is closest to ΔR_2 will be blown open in the $k + 1$ trimming step. The SPICE simulation excerise in Exercise 4.8 shows an actual trimming procedure to trim a bandgap voltage reference circuit to achieve a 1.23 V output, along with a filler page for calculations and measurements that will allow the reader to fill in the blanks when trimming the bandgap voltage reference circuit. In reality, the measurements, calculations and table lookup are all performed by the ATE machine during wafer probing in a similar manner as our hand calculations in the exercise.

4.8.4 Voltage Domain Trimming

Alternatively, the output voltage can be adjusted by changing the emitter area A_{E_2} of Q_2. The emitter area A_{E_2} can be made trimmable by constructing the transistor from a parallel corrections of sub-transistors with (dyadic)-scaled emitter areas, which can be disconnected from the voltage reference circuit through linked fuses as shown in Figure 4.31, where the case of three fuses is demonstrated.

By altering the number of parallel connected bipolar transistors to form Q_2, the transistor emitter area ratio N will be altered. It can be observed from Equation 3.12 that the output voltage V_{REF} is logarithmically proportional to N. The trimming model can thus be developed by rewriting Equation 3.13 as

$$y = m \ln(x) + b, \tag{4.55}$$

where a linear trimming model is adopted with $y = V_{REF}$, x being the transistor emitter area ratio N, and $b = V_{BE_3}$. A trimming procedure similar to that in Section 4.8.3.1 can be developed for voltage domain trimming.

A problem of this approach is that the voltage drop across the fuse may be comparable with the small $\Delta V_{BE_{1,2}}$. The worst case is that it is difficult if not impossible to reduce the

resistance of the linked fuse. One possible solution is to use the linked fuse to switch on and off a MOSFET switch, which will in turn connect/disconnect the bipolar transistors to the voltage reference circuit. By making the MOSFET switch large enough, the on-resistance can be made small enough such that the voltage drop across the switch can be neglected in the actual circuit operation.

4.8.5 Current Domain Trimming

To minimize the effect of linked fuse resistance, we can also consider trimming the output voltage by adjusting I_{PTAT} that flows through R_2, and hence altering the PTAT voltage built upon R_2, such that Equation 3.12 can be rewritten as

$$V_{REF} = \frac{R_2}{R_1} N_C V_T \ln(N) + V_{BE_3},$$

where N_c is the current ratio I_3/I_1. As a result, the output voltage is linearly proportional to the current ratio N_c. The PTAT current I_3 can be made programmable by switching a number of (binary)-weighted current sources. The detail trimming circuit that trims a MOSFET array that forms M_3 which in turn alters I_3 is shown in Figure 4.31. The linked fuses can be replaced by small MOSFET switch with low on-resistance due to the high impedance output of the current source. This will not lead to significant impact on the performance of the voltage reference circuit, nor the trimming structure. Trimming of the bias current may therefore be preferable over trimming of the emitter area.

4.9 Summary

More often than not, the accuracy of a voltage reference circuit imposes a fundamental limit on the accuracy of the system it is used in. This makes it imperative to analyze the various sources of error that degrade the performance of the voltage reference circuit with the ultimate aim of devising viable techniques to mitigate, if not eliminate, the detrimental impact of those sources of error. This chapter has presented analytical analysis on the most commonly observed error sources in the opamp based β-multiplier bandgap voltage reference circuit presented in Chapter 3. Each of the analyzed error sources affect the reference voltage uniquely and therefore pose a variegated set of challenges towards its compensation.

As an example, the opamp input offset voltage problem analyzed in Section 4.1.1 is imposed by process variations which have a strong random component. In other words, the magnitude of the error with respect to the nominal reference voltage induced by opamp input offset voltage varies from one sample to the next. As a result, we have discussed various methods to alleviate the opamp input offset voltage problem, these errors have been conventionally reduced by trimming, which involves measuring the reference voltage on each IC sample and tweaking circuit components using on-chip fuses till the reference voltage falls within its accuracy specification. While trimming enjoys wide popularity because of its effectiveness, the considerable increases in test time, silicon area, and ultimately manufacturing cost it incurs has prompted designers to look into more cost-effective strategies to achieve high accuracy

voltage reference circuits. After all, the trimming or other post-fabrication techniques do not actually eliminate the problem, but just provide an expensive alternative way to achieve a viable solution. Other error sources in the opamp based β-multiplier bandgap voltage reference circuit discussed in previous sections can be summarized to derive the erratic V_{REF} as

$$V_{REF} = \frac{R_2}{R_1} V_T \ln N + V_{BE_3} + \frac{R_2}{R_1} V_{OS} + e_1 \frac{R_2}{R_1} V_T + e_2 \frac{R_2}{R_1} V_T \ln N + \frac{R_2}{R_1} V_T \ln N \frac{\Delta r_{b_{1,2}}}{\beta R_1} + \frac{R_2}{R_1} V_T \ln N \frac{r_{b_3}}{\beta R_2}, \tag{4.56}$$

where the error parameter e_2 includes the mismatch error of the current mirror connected to the opamp. The error parameter e_1 includes the variation of the resistor value ratio $\frac{R_2}{R_1}$, the mismatch of the current mirror that causes mismatch of current flowing through R_1 and R_2, and the variation of the NPN transistors emitter area ratio. The error parameter $\Delta r_{b_{1,2}}$ is the series resistance of M_1 and M_2, while the error parameter r_{b_3} is the resistance of the NPN transistor measured from the emitter to the base. Besides the above static error sources, there are dynamic error sources, which include the power supply noise discussed in Section 4.5 and the device noise discussed in Section 4.7. It is clear from Equation 4.56 that a small R_2/R_1 can help to reduce the sensitivity of V_{REF} towards each of the considered error sources. As a result, various techniques in previous sections to obtain a reduced R_2/R_1, we have discussed and thus obtain a high accuracy V_{REF}. However, a small R_2/R_1 means the resistor size of R_1 is much larger than that of R_2. In the modern CMOS process, if R_2 is implemented with the smallest calibrated resistor, the size of R_1 may still be too big that it cannot be implemented economically.

Readers should also note that there are a large number of circuit analysis techniques that might treat the error sources and hence the variation of reference voltage in the voltage reference circuit differently. A number of voltage reference circuit error analysis are discussed in (Song and Gray, 1983), which uses similar circuit analysis tools as those discussed in this chapter with a different perspective on the design of high precision voltage reference circuit. However, no matter what the analysis tools are, we are aiming at estimating the effects of various component parameter variations, and hence deriving appropriate circuit topologies to alleviate such effects. Besides analytical calculation, the SPICE simulator is another great tool to estimate the performance of the voltage reference circuit under the influence of various error sources. In particular, the SPICE simulator provides corner analysis, which is discussed in Section 1.6, to estimate the impact of the process variations. Corner process parameters present extremes, and therefore give rather precise predictions when compared to the fabricated circuits. Various usages of the process corner simulation are applied extensively to obtain an estimation of the variation of some particular circuit parameters, which will enable the designers to design an appropriate trimming circuit for a given accuracy. The advantage of the process corner simulation is best experienced by the reader though design examples, instead of words alone. Therefore, we are not going to discuss it in this book. Instead, we shall move on to discuss and compare different voltage reference circuit topologies in the next chapters, where real examples with detailed analytical derivations will be presented. We will also discuss the advantages and disadvantages of different voltage reference circuit topologies.

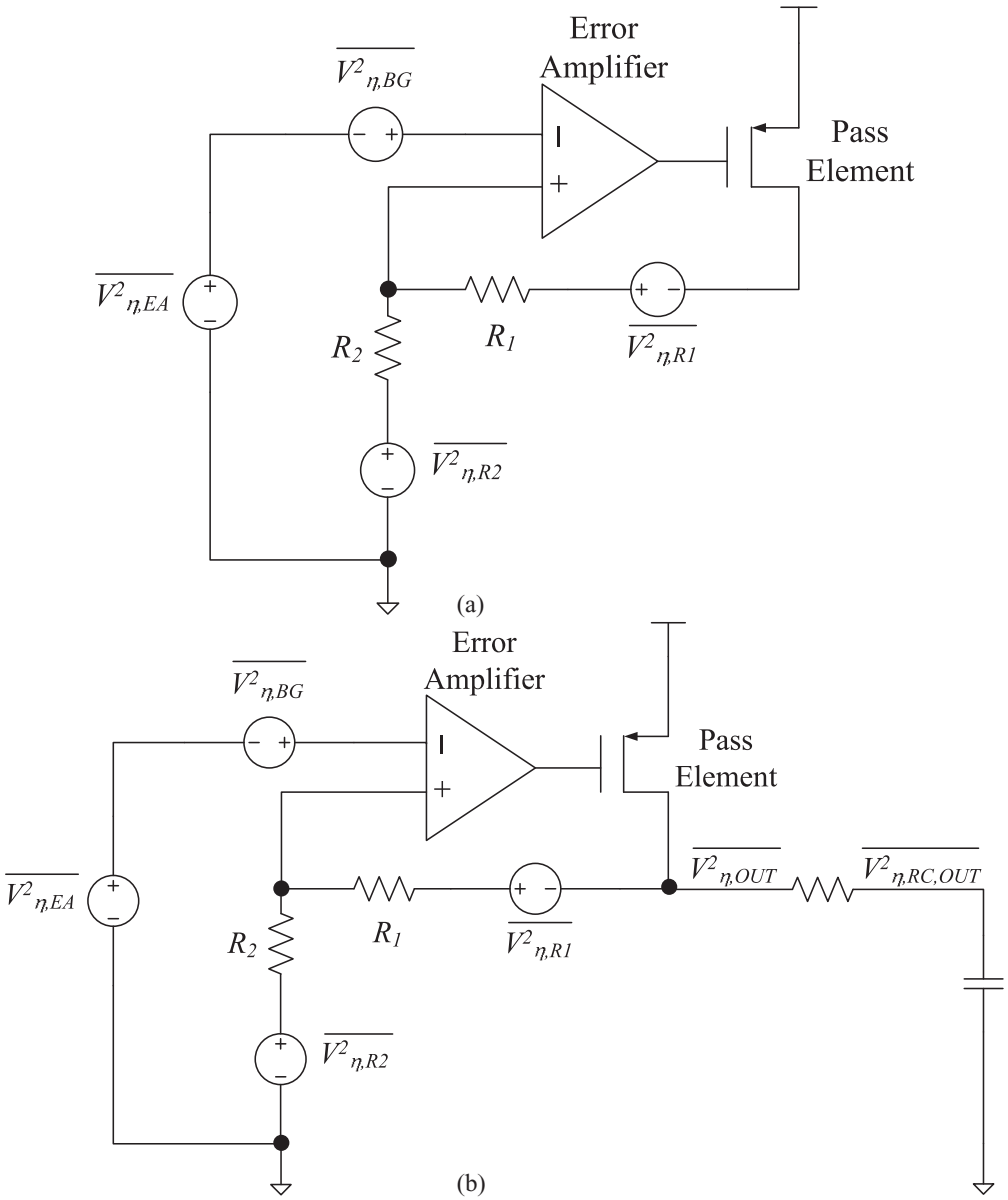


Figure 4.32 (a) LDO Noise Model. (b) LDO with RC output filter for Exercise 4.1.

4.10 Exercises

Exercise 4.1 *Figure 4.32(a) shows the equivalent noise model of a LDO, where* $\overline{V^2_{\eta,BG}}$ *is the equivalent noise power generated by the bandgap,* $\overline{V^2_{\eta,EA}}$ *is the equivalent noise power of the error amplifier, and* $\overline{V^2_{\eta,R1}}$ *and* $\overline{V^2_{n,R2}}$ *are the noise powers of the feedback resistor* R_1 *and* R_2 *respectively.*

1. *Derive the RMS output noise within the frequency range of* $10 \sim 100$ kHz *for the LDO in Figure 4.32(a).*
2. *A RC filter is added at the output of the LDO to reduce the noise power as shown in Figure 4.32(b). Derive the the RMS output noise after the RC filter.*

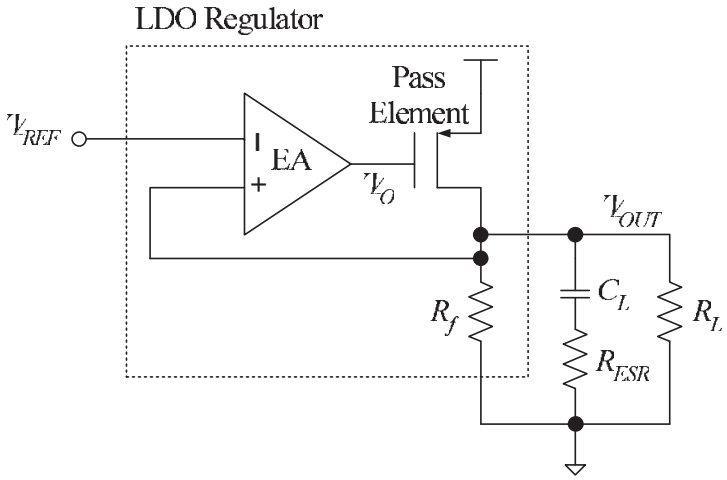


Figure 4.33 LDO $PSRR$ analysis model for Exercise 4.3.

3. *Discuss how to design such a RC filter to obtain an output voltage with low noise in the frequency under consideration.*

Exercise 4.2 *There are several free parameters in the design of the bandgap voltage reference circuit in Figure 3.4, which include I_3. Discuss a design strategy on I_3 that will lead to a low noise reference voltage, and the associated tradeoff.*

Exercise 4.3 *This exercise will show that the $PSRR$ of the LDO regulator circuit shown in Figure 4.33 can be approximated as a 1 zero 2 poles system. Consider the equivalent small signal model of the LDO regulator as shown in Figure 4.34, where the equivalent small signal model of the error amplifier is the same as that discussed in Figure 4.19, and the small signal model of the LDO core circuit is shown in Figure 4.35. The transfer functions $h_1(s)$ and $\alpha(s)$ are written with respect to v_{dd} and v_β of the error amplifier respectively. The $\beta(s)$ is the*

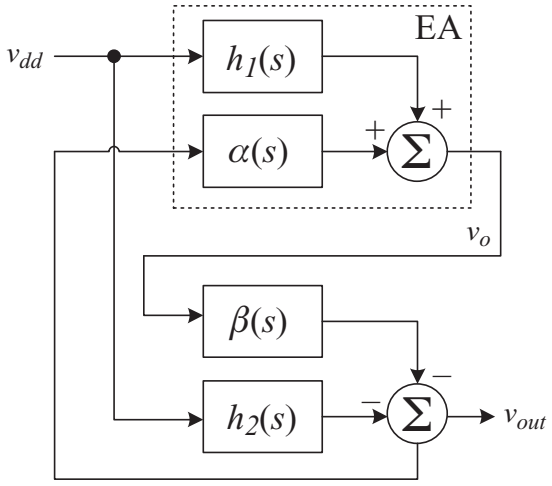


Figure 4.34 Small signal model of the LDO regulator circuit for Exercise 4.3.

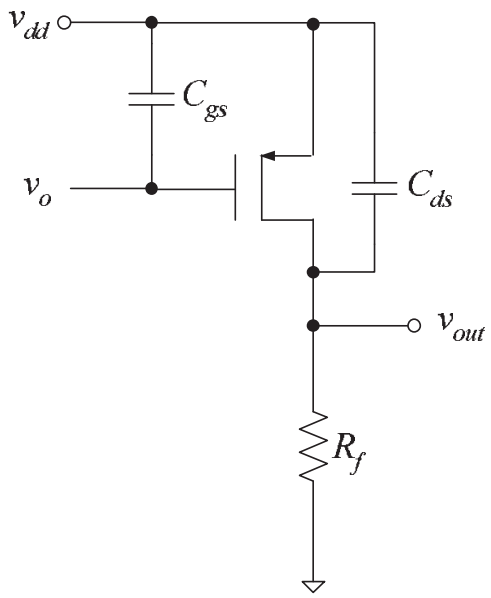


Figure 4.35 Small signal model of the LDO core circuit for Exercise 4.3.

input output transfer function of the LDO core circuit from the opamp output, and $h_2(s)$ is the transfer function of v_{dd} to the LDO core circuit observed at the LDO.

1. *Derive the $PSRR$ of the LDO, which equals $\frac{v_{out}}{v_{dd}}$.*
2. *If the close loop gain of the opamp is assumed to be a 1 pole system, derive i_β and $\alpha(s)$ with respect to the differential gain G_β of the input signal v_β to the opamp, and the equivalent output resistance r_{out} of the opamp (refer to Figure 4.19).*
3. *If the system $h_1(s)$ is assumed to be a 1 pole and 1 zero system, derive the system transfer function of $h_1(s)$ with respect to the gain $G_{v_{dd}}$ of the power supply noise at the opamp.*
4. *If the systems $\beta(s)$ and $h_2(s)$ are both assumed to be a 1 pole systems, derive the system transfer function of $\beta(s)$ and $h_2(s)$, with respect to the resistance $R_{DS,M}$ of the pass element of the LDO circuit.*
5. *If we approximate the equivalent poles $\alpha(s)$ with that of $h_1(s)$, and the equivalent poles of $\beta(s)$ with that of $h_2(s)$, show that the $PSRR(s)$ of the LDO circuit is a 1 zero 2 pole system, and derive $PSRR(0)$, the $PSRR$ Of the LDO circuit at DC point.*

Exercise 4.4 *The trimming resistor array should be designed with respect to process variation. Consider the design of a binary weighted resistor array as shown in Figure 4.36 that*

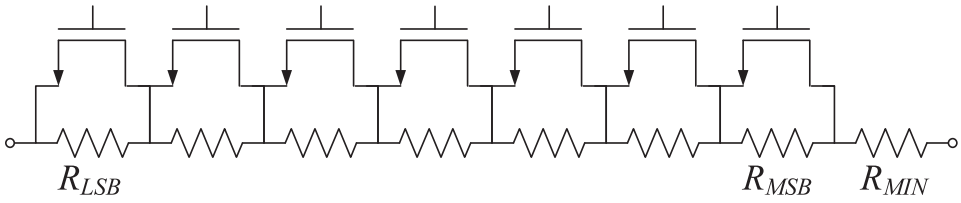


Figure 4.36 Binary weighted trimming resistor array with NMOS switch for Exercise 4.4.

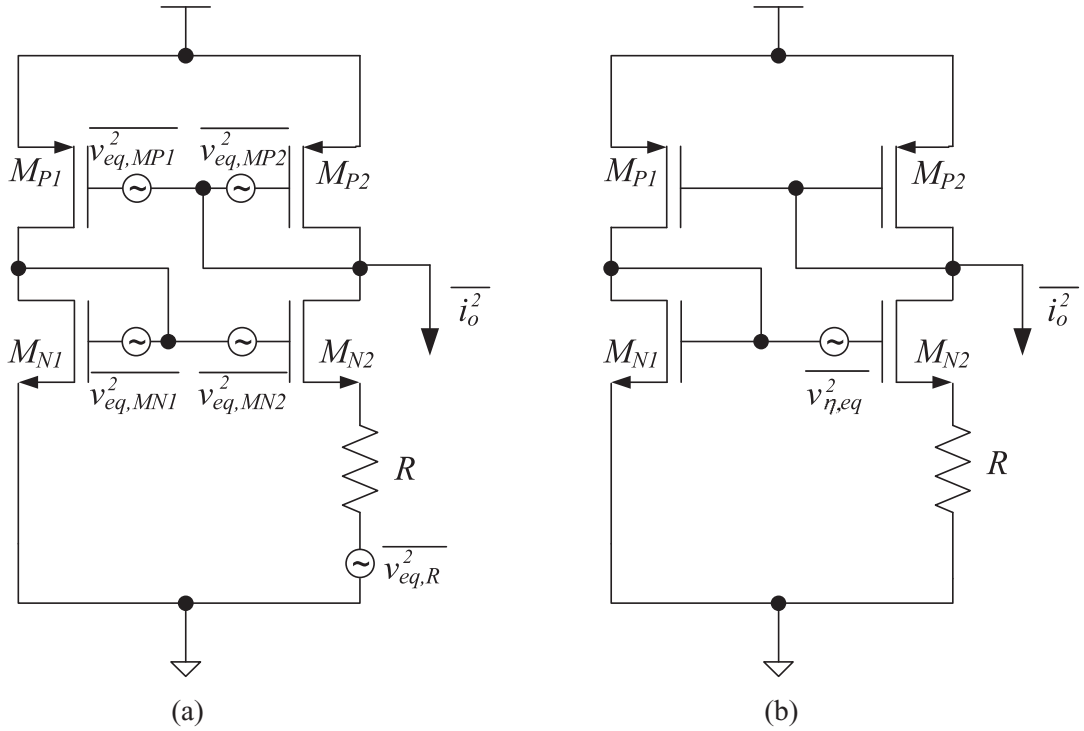


Figure 4.37 (a) Noise model of a Widlar current source, and (b) its equivalent noise model for Exercise 4.5.

is required to cover a $\pm 40\%$ *error variation, where the NMOS switches are used as the controlling bits.*

1. *Determine the maximum and minimum resistance that should be attained by the trimming resistor array when the desired resistance is 200* kΩ.
2. *Determine* R_{LSB} *and* R_{MSB} *of a 7-bit binary weighted resistor array.*
3. *Determine the trimming accurate that can be achieved by this resistor array in percentage of variation from the desired value of 200* kΩ.

Exercise 4.5 *Figure 4.37(a) shows the equivalent noise diagram of a Widlar current source. Similarly Figure 4.37(b) shows the equivalent noise diagram of Figure 4.37(a) where the equivalent output current noise is being modeled as an equivalent noise voltage acting on the gate of* M_{N2}.

1. *Derive the equivalent output current noise of the Widlar current source.*
2. *Derive the equivalent noise voltage* $\overline{V_{\eta,eq}^2}$.
3. *Assume* $S_{MN1} = S_{MN2}$ *and* $S_{MP1} = S_{MP2}$, *expand the derived* $\overline{V_{\eta,eq}^2}$ *using the noise model presented in Section 4.7, and show that*
   a. W/L *of PMOS transistors have to be bigger than that of NMOS transistors with* L *of PMOS being longer than that of NMOS to reduce the output current noise.*
   b. *A low resistance* R *helps to reduce the output current noise.*

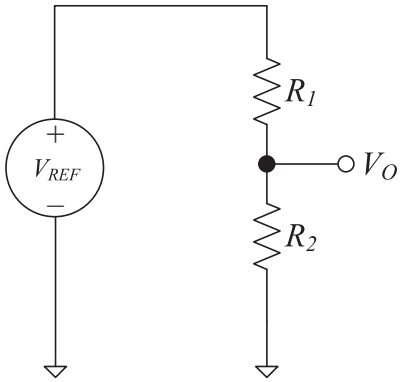


Figure 4.38 Obtaining a low reference voltage using applying a resistive divider on the output of conventional bandgap voltage reference circuit in Exercise 4.6.

Exercise 4.6 *This problem investigates the application of resistors divided to obtain a low reference voltage from the conventional bandgap voltage reference circuit. Refer to Figure 4.38, the output voltage is given by*

$$V_o = V_{REF}\frac{R_2}{R_1 + R_2}.$$

The output voltage V_o will have noise contributed by V_{REF}, R_1, and R_2. Show that $R = R_1 + R_2$ can be determined from $\overline{V^2_{\eta,REF}}$ when V_{REF} contributes 80% of the noise in V_o, and hence determine R_1 and R_2 with respect to $\overline{V^2_{\eta,REF}}$ when the output voltage is $1/3$ of V_{REF}.

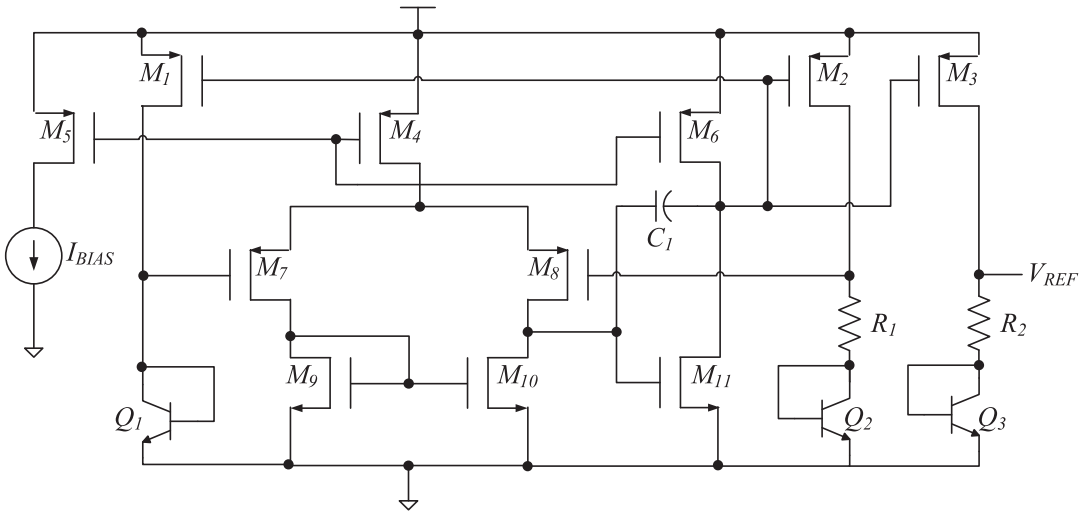


Figure 4.39 Schematic of bandgap voltage reference circuit for Exercise 4.8.

Table 4.2 Device sizes for the bandgap voltage reference circuit in Figure 4.40 for problem 4.8.

M_1, M_2, M_3	W/L=10 μm/1 μm
Q_1, Q_3	Emitter Area Ratio with respect to unit sized BJT, A_E=1
Q_2	Emitter Area Ratio with respect to unit sized BJT, A_E=8
R_1	9 kΩ
R_2	81.7 kΩ
M_4, M_5, M_7, M_8	W/L=8 μm/0.3 μm
M_6	W/L=32 μm/0.3 μm
M_9, M_{10}	W/L=2 μm/0.18 μm
M_{11}	W/L=16.7 μm/0.3 μm
C_1	150 fF
I_{BIAS}	20 μA

Exercise 4.7 *Compute the sensitivity parameters $\mathcal{S}_{I_{C_1}}^{V_{REF}}$ and $\mathcal{S}_{M_R}^{V_{REF}}$ of the bandgap voltage reference circuit in Figure 3.4, where $M_R = \frac{R_2}{R_1}$. Based on your derivation, determine an explanation of which circuit component parameter in this voltage reference circuit is more important to be trimmed in order to achieve high accuracy on the reference voltage.*

Exercise 4.8 *Trimming procedure Figure 4.39 shows a complete schematic of a bandgap voltage reference circuit which has the same structure as that shown in Figure 3.4, in which transistors M_4 to M_{11} form the opamp and current bias circuits. The purpose of this exercise is to trim R_2 of the circuit in Figure 4.39 to obtain a desired output voltage (*1.23 V*). Perform SPICE simulation of the bandgap voltage reference circuit in Figure 4.39 with the device parameter given in Table 4.2. Then follow the following trim procedure.*

1. *Take the output reading with no trimming, such that $R_2 = 60$ kΩ and record the data in Table 4.3. By opening up each fuse, a* 6.3 kΩ *resistor (where we assume the process variation will induce a maximum* 20% *resistance variation) will be added to R_2.*
2. *Measure V_{REF}, and fill in Table 4.3 together with the analytical calculation of the slop m, intercept b, and ΔR_2.*
3. *Choose the most appropriate number of fuses to cut.*
   a. *If there is no fuse that can be cut without over-trimming, the trimming is complete. Please go to procedure 4.*
   b. *Cut the chosen fuses and then go to procedure 2.*
4. *The trimming is complete. Record the final measured V_{REF} and compute the output voltage variation. Is it smaller than* 2%*?*

Table 4.3 Trimming table for problem 4.8.

V_{REF}(V)	m	b	ΔR_2	R_2

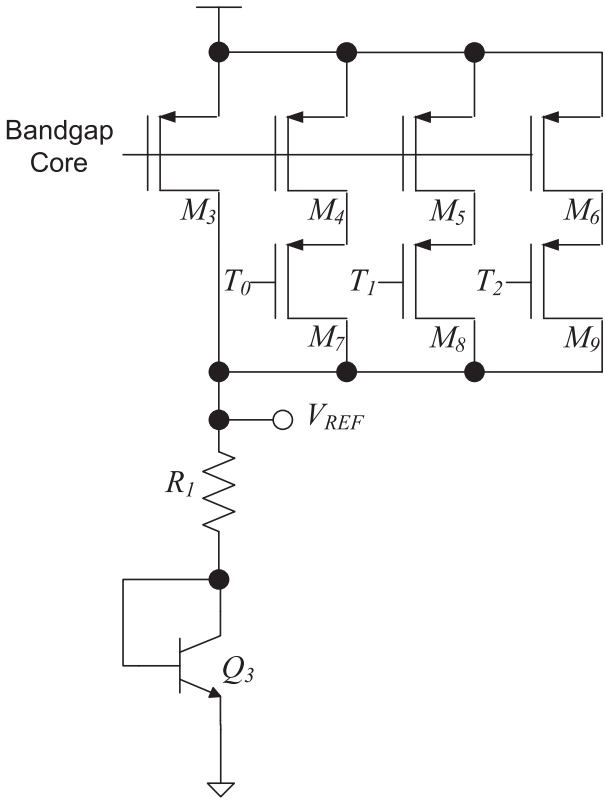


Figure 4.40 Current domain trimming with MOSFET switches that can be turned on and off by external input signal (T_0, T_1, T_2).

Exercise 4.9 *Consider the current domain trimming in Figure 4.31 with the fuses replaced by MOSFET switches as shown in Figure 4.40. Under nominal conditions, the different* V_{REF} *can be generated from the control logic as shown in Table 4.4.*

1. *Select the initial* (T_0, T_1, T_2) *to achieve the maximum trimmable region.*
2. *Given that the untrimmed reference voltage is* 1.21 V, *derive the trimming scheme to achieve the desired* 1.23 V *(also record the trimming step in your answer).*

Table 4.4 Trimming table for circuit in Figure 4.41.

T_2	T_1	T_0	V_{REF} (V)
0	0	0	1.30
0	0	1	1.29
0	1	0	1.28
0	1	1	1.27
1	0	0	1.26
1	0	1	1.25
1	1	0	1.24
1	1	1	1.23

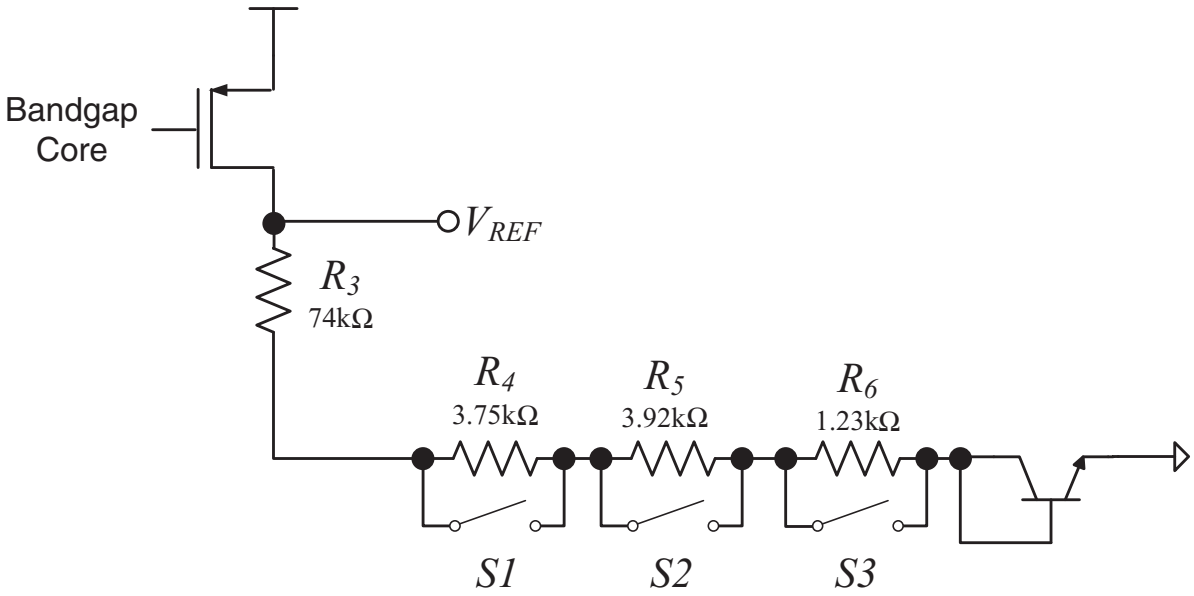


Figure 4.41 Modulated trimming with fuses connected parallel resistors for Exercise 4.10.

Exercise 4.10 *Consider the modulated trimming with fuses connecting parallel resistors in Figure 4.31 as shown in Figure 4.41. The modulated trimming structure is designed to accomodate a V_{REF} with $-0.4\% \sim 6\%$ variation from the nominal condition.*

The trimming procedure is detailed in the following:

(a) if V_{REF} is within $(Y, Z)V$, close $S1$, $S2$ and $S3$;
(b) if V_{REF} is within $(X, Y)V$, close $S2$ and $S3$;
(c) if V_{REF} is within $(W, X)V$, close $S3$.

1. *Derive W, X, Y, and Z if the nominate is $V_{REF} = 1.23$ V.*
2. *Show that the trimmed V_{REF} can achieve an accuracy of $\pm 1\%$ with respect to that of the nominal condition.*

Exercise 4.11 *Besides opening the fuses in a resistor network in Figure 4.41, another way to achieve modulated trimming is to use series connected resistors by opening up bypass fuses as shown in Figure 4.42. This modulated trimming structure operates by trimming the resistor through opening up fuses F_1, F_2, F_3 such that R_4, R_5, and R_6 are connected to the overall resistor string. As a result, the trimming V_{REF} never exceeds the nominal value, and therefore this trimming can only work with V_{REF} being lower than the nominal value.*

The trimming network can achieve a trimming accuracy of $\pm 1\%$ with nominal $V_{REF} = 1.23V$.

The trimming procedure is detailed in the following:

(a) if V_{REF} is within $(Y, Z)V$, cut fuse F_1;
(b) if V_{REF} is within $(X, Y)V$, cut fuses F_1 and F_2;
(c) if V_{REF} is within $(W, X)V$, cut fuses F_1, F_2 and F_3.

1. *Derive W, X, Y, and Z.*
2. *Determine the acceptable input voltage variation in % of this trimming network.*

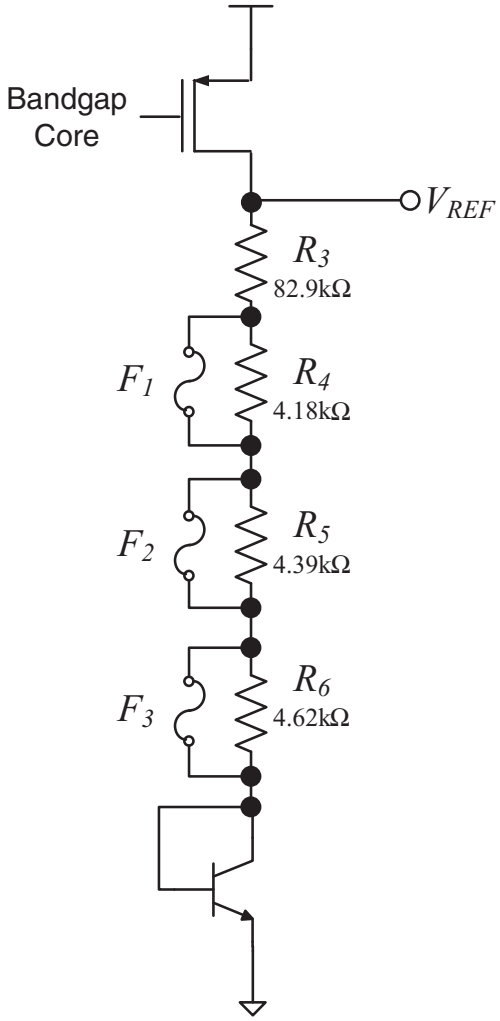


Figure 4.42 Modulated trimming using series connected resistors with fuse bypass for Exercise 4.11.

Exercise 4.12 *(Voltage divider) It is easiest to construct a high accuracy voltage divider with* 1 MΩ *input impedance from four resistors* 1 kΩ, 9 kΩ, 90 kΩ, *and* 900 kΩ *as shown in Figure 4.43(a). However, the CMOS process may not provide calibrated standard resistors with arbitrary resistances that fit the required resistance values in the schematic.*

1. *Consider the case where the CMOS process only provides calibrated resistors of values* 10 Ω, 1 kΩ, 10 kΩ 100 kΩ, 1 MΩ, *and* 10 MΩ. *Construct a voltage divider with similar voltage division ratio and similar input impedance as that in Figure 4.43(a) with the topology shown in Figure 4.43(b).*
2. *Compute the maximum voltage variation at each of the voltage divider output nodes in Figure 4.43(b) when compared to that in Figure 4.43(a), and show that it is smaller or equal to* 0.01%, *assuming that the resistors in both schematics are of* 1% *accuracy.*
3. *In order to minimize the silicon space, one of the resistors associated with each output node will be constructed with resistors with* 5% *variation, while others will be of* 1% *variation.*

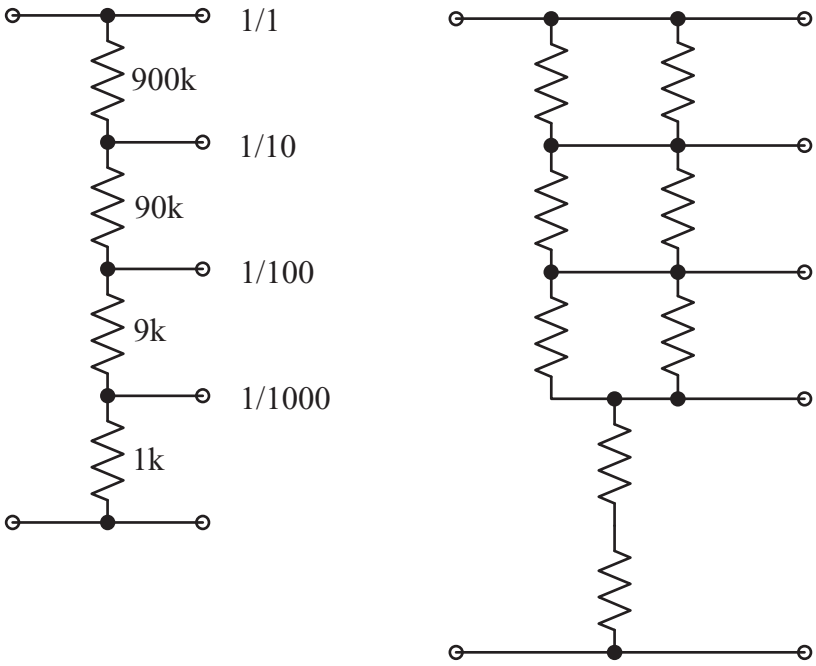


Figure 4.43 Voltage divider (a) with high accuracy resistors with arbitrary resistance, (b) with high accuracy resistors with limited resistance values.

Please label which resistors can be constructed with 5% *variation while the overall voltage divider can still achieve a high voltage division accuracy.*

Exercise 4.13 *(Opamp with finite gain) Consider the voltage reference circuit in Figure 4.44, where opamp has finite gain A, zero input offset* $V_{OS} = 0$ V*, and a stable voltage difference between the two input terminals measured as* ΔV *when the close loop circuit is at equilibrium.*

1. *Derive* V_{REF} *in terms of* V_{BE}, $\Delta V_{BE_{1,2}}$, ΔV, *and the resistor ratio* R_3/R_2 *only.*
2. *Note that* $V_{REF} = A\Delta V$, *derive* V_{REF} *in terms of A,* V_{BE}, V_T, *BJT area ratio N, and resistor ratio* R_3/R_2 *only.*
3. *Discuss the following cases:*
   a. *the effect of large gain A,*
   b. *the effect of an opamp with gain A dependent on temperature, and*
   c. *the effect of an opamp with gain A dependent on* V_{DD}.

Exercise 4.14 *(Opamp with both finite gain and offset voltage) Consider the voltage reference circuit in Figure 4.44, where the opamp has finite gain A and input offset voltage* V_{os}.

1. *Derive* V_{REF} *in terms of opamp gain A,* $\Delta V_{BE_{1,2}}$, *resistor ratio* R_3/R_2 *and opamp input offset* V_{os}.
2. *Discuss how does the sign of the opamp input offset voltage* V_{os} *affects the design of opamp gain A to achieve a precise reference voltage.*

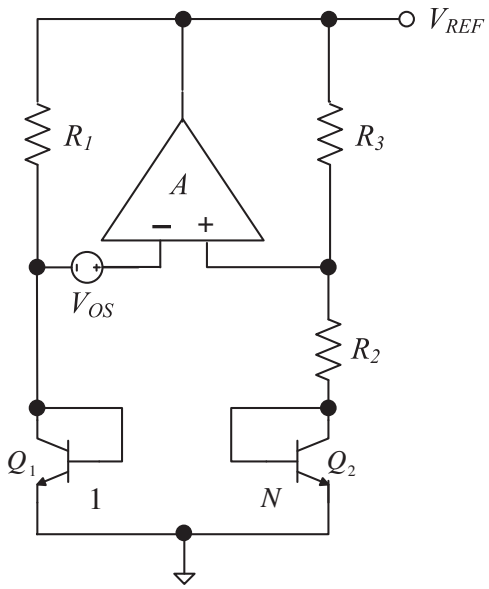


Figure 4.44 The schematic of a voltage reference circuit, where the opamp has finite gain and input offset.

References

Allen, P.E. and Holberg, D.R. (2003) *CMOS Analog Circuit Design*. Oxford Press, New York.

Books, T. and Westwisk, A.L. (1994) A low-power differential CMOS bandgap reference. *IEEE ISSCC Digest of Technical Papers*, pp. 248–49.

Giustolisi, G., Palumbo, G., Criscione, M. *et al.* (2003) A low-voltage low-power voltage reference based on subthreshold MOSFETs. *IEEE Journal of Solid-State Circuits*, **38** (1), 151–54.

Gray, P.R. and Meyer, R.G. (1982) MOS operational amplifier design - a tutorial overview. *IEEE Journal of Solid-State Circuits*, **SC-17**, 969–82.

Rincon-Mora, G.A. (2002) *Voltage reference-from diodes to precision high-order bandgap circuits*, Wiley.

Roh, J. and Nair, V.V. (2002) Chopper stablized bandgap reference circuit to cancel offset variation. US Patent Number 6462612.

Song, B.S. and Gray, P.R. (1983) A precision curvature-compensated CMOS bandgap voltage reference. *IEEE Journal of Solid-State Circuits*, **18** (6), 634–43.

Hoon, S.K., Chen, J. and Maloberti, F. (2002) An improved bandgap reference with high power supply rejection. *IEEE International Symposium on Circuits and Systems*, **2**, 400–403.

Advanced Voltage Reference Circuits

CMOS Voltage References: An Analytical and Practical Perspective, First Edition. Chi-Wah Kok and Wing-Shan Tam.
 Published 2013 by John Wiley & Sons Singapore Pte. Ltd.

5

Temperature Compensation Techniques

The fundamental circuit topology to remedy the temperature dependency of the voltage reference circuit is the mutual compensation between the PTAT and CTAT voltage/current sources. These temperature dependent factors can be constructed in either voltage or current forms. In either case, the temperature compensated voltage reference circuit can be considered to consist of three sub-circuits. The first sub-circuit generates the PTAT voltage/current, while the second sub-circuit generates the CTAT voltage/current. The two temperature dependent voltages/currents are summed by the third sub-circuit, which will also provide the I-V conversion. As an example, the third sub-circuit of the opamp based β-multiplier bandgap voltage reference circuit in Chapter 3 performs the summing operation by means of converting the PTAT current to voltage using a resistor, and then the PTAT voltage is super-positioned on top of a CTAT voltage to generate a temperature compensated reference voltage. There are a large number of circuit topologies to perform the summation operation and each has its own pros and cons. Similarly, there are a large number of circuit topologies to generate the PTAT and CTAT voltages/currents. Furthermore, depending on their availability in the fabrication process, different electron devices are employed in each topology to generate stable CTAT and PTAT voltages and currents. Previous chapters discussed the application of the base-emitter voltage (V_{BE}) of the bipolar transistor and the ΔV_{BE} between two bipolar transistors with different current density to generate the CTAT and PTAT voltages in the voltage reference circuit. This is because they are commonly available in most of the CMOS fabrication processes. Some of the foundries have multi-threshold voltages CMOS process, where MOSFET with different threshold voltages can be fabricated, and the threshold voltages are tightly controlled over process variation and thus the threshold voltage difference between two types of MOSFETs can be used to generate an accurate reference voltage with low temperature sensitivity. The temperature dependency of the gate-to-source voltage (V_{GS}) of the MOSFET can also be used as a temperature dependent component to generate an accurate reference voltage. The following sections will discuss some of the important voltage reference circuit topologies where different electron devices are employed to generate the PTAT and CTAT voltages.

Since no circuit is infallible, the importance of understanding the method cannot be overemphasized. It is in fact the rationale behind learning about analog circuits and hence temperature compensated reference voltage generation methods. Each temperature compensation technique presented in this chapter is explained in detail together with its strengths, weaknesses,

CMOS Voltage References: An Analytical and Practical Perspective, First Edition. Chi-Wah Kok and Wing-Shan Tam.
 Published 2013 by John Wiley & Sons Singapore Pte. Ltd.

and possible implementation difficulties. The hand computation that follows the individual temperature compensation technique illustrates the inner working of the method. The choice of methods is tilted toward relevance to practical implementation in modern CMOS foundries. Methods requiring overly complex fabrication and post-fabrication processes were rejected regardless of their efficiency and robustness. This decision, which was taken with great reluctance, is to keep with our intention to avoid emphasis on process and post-fabrication developments. Instead of concentrating on the theoretical development of voltage reference circuit, we shall discuss practical circuits that employ different temperature compensation techniques which we considered to be important. Note that the selection of temperature compensation methods presented in this book was also influenced by current practice. This disqualified several well-known historic methods that have been overtaken by more recent developments. Nevertheless, classical methods will be discussed in the first few sections to illustrate the development progress of voltage reference circuits over the last four decades.

5.1 $V_{BE} - \Delta V_{BE}$ Compensation

One of the earliest $V_{BE} - \Delta V_{BE}$ compensated bandgap voltage reference circuits is the Widlar bandgap voltage reference circuit introduced by Robert Widlar in 1971 (Widlar, 1971). The thermal voltage (V_T) extracted from the ΔV_{BE} of two BJTs with different emitter areas and hence different current densities will form the PTAT voltage, while the base-emitter voltage (V_{BE}) of the BJT will form the CTAT voltage. The circuit is simple but it is not easy to implement in modern CMOS process nor to control the output because the BJTs implemented in the CMOS process are sensitive to process variation. Nevertheless, we shall discuss this classical bandgap voltage reference circuit in detail, because of its simplicity, while still covering everything that we need to know about the $V_{BE} - \Delta V_{BE}$ compensation technique.

A simplified Widlar bandgap voltage reference circuit that is suitable for CMOS implementation is shown in Figure 5.1. Similar to the V_T extraction circuit discussed in Section 1.1, the emitter area of Q_2 is constructed to be N times larger than that of Q_1. The difference in current density will establish a voltage across R_3, which equals $\Delta V_{BE_{1,2}}$.

$$\begin{aligned} V_{BE_1} &= V_{BE_2} + I_2 R_3, \\ \Delta V_{BE_{1,2}} &= V_{BE_1} - V_{BE_2} = I_2 R_3 \end{aligned} \tag{5.1}$$

$$\begin{aligned} &= V_T \ln(\frac{I_1}{J_S A_{E_1}}) - V_T \ln\left(\frac{I_2}{J_S A_{E_2}}\right) \\ &= V_T \ln\left(\frac{I_1}{I_2} N\right). \end{aligned} \tag{5.2}$$

If we assume $I_1 = I_2$, then

$$\Delta V_{BE_{1,2}} = V_T \ln(N), \tag{5.3}$$

which is the same as that derived in Equation 1.13. The PTAT voltage is obtained from scaling V_T as that in Equation 5.3. The scaled V_T can be easily extracted in the current domain.

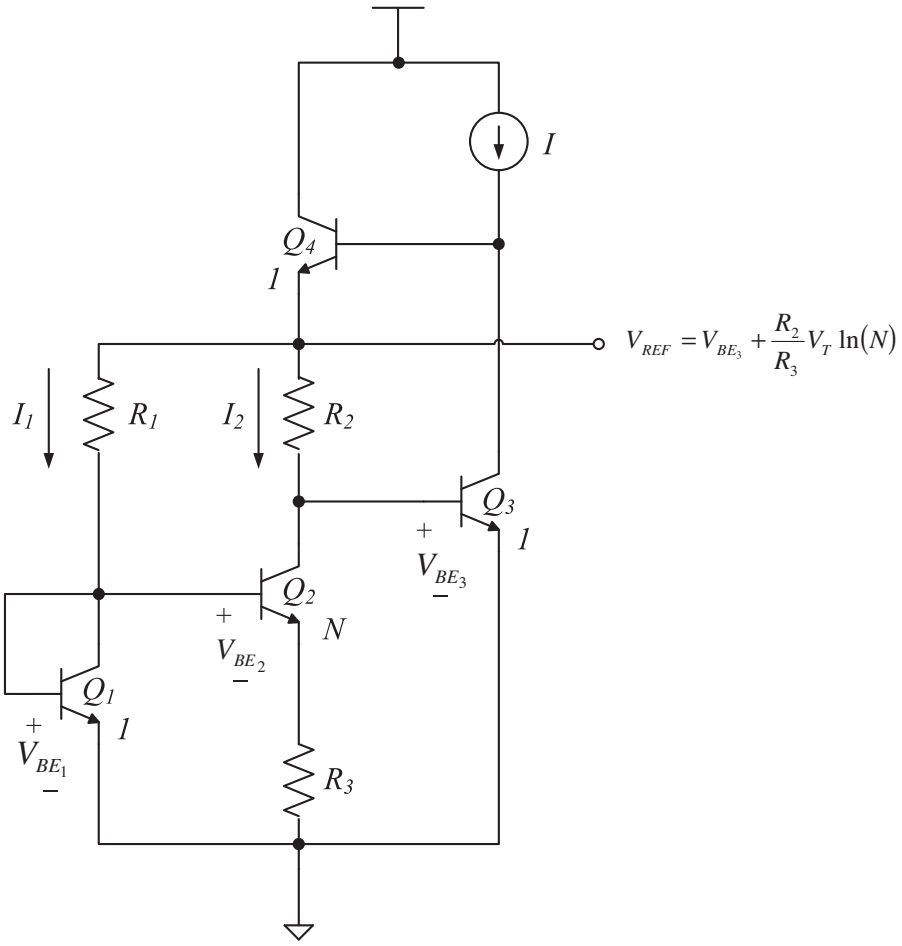


Figure 5.1 A simplified Widlar bandgap voltage reference circuit (Widlar, 1971).

Consider Equations 5.1 and 5.3, which can be rewritten as

$$I_2 = \frac{\Delta V_{BE_{1,2}}}{R_3} = \frac{V_T \ln(N)}{R_3}. \tag{5.4}$$

The current I_2 will form a PTAT current. This PTAT current is converted back to PTAT voltage over R_2 which is then summed with the CTAT voltage V_{BE_3} by super-position to generate V_{REF}.

$$\begin{aligned} V_{REF} &= V_{BE_3} + I_2 R_2 \\ &= V_{BE_3} + \frac{R_2}{R_3} V_T \ln(N). \end{aligned} \tag{5.5}$$

The V_{REF} obtained in Equation 5.5 has the same form as that obtained by Equation 3.12 for the opamp based β-multiplier bandgap voltage reference circuit. We can observe that the weighting factor M in Equation 3.12 is now given by $\frac{R_2}{R_3}\ln(N)$. Using the analogy in Section 3.2.1, a near-zero TC reference voltage can be obtained by properly tuning the parameters R_2, R_3, and N until $M = \frac{R_2}{R_3}\ln(N) = 19.22$. Consider the case of $N = 8$, which yields $\frac{R_2}{R_3} = 9.24$. To ensure the bipolar transistors are properly biased, the collector currents of Q_1 and Q_2

should be at least 6 μA. In other words, I_2 in Equation 5.4 should be 6 μA. As a result, Equation 5.4 yields $R_3 = 8.97\ \text{k}\Omega$, and $R_2 = \frac{R_3 M}{\ln N} = 82.9\ \text{k}\Omega$. Since $I_1 = I_2$, therefore, $R_1 = R_2 = 82.9\ \text{k}\Omega$. Finally, the V_{REF} obtained from Equation 5.5 equals 1.23 V, which is the bandgap voltage of silicon similar to that of the opamp based β-multiplier bandgap voltage reference circuit.

The above analysis of the output voltage is valid if and only if $I_1 = I_2$. In other words the currents flowing through the two bipolar transistors are the same. Otherwise, there will be an output voltage drift. In reality, severe voltage drift is observed in the Widlar bangap voltage reference circuit, due to the fact that the BJTs Q_1 and Q_3 are required to have much larger emitter sizes than that of Q_2, to have $I_{S_1} = I_{S_2} = I_{S_3}$. As a result, there will be an observable difference between I_1 and I_2. Furthermore, the current gain β of the BJT implemented by the CMOS process is small. Thus the situation of $I_1 \neq I_2$ is further worsened by the fact that the base currents of both BJTs with small β are not negligible. Since β varies with temperature, therefore, the base current will also vary with temperature. As a result, the output voltage drift caused by the base current will be temperature dependent, which will increase the temperature coefficient of the voltage reference circuit. These problems can be alleviated by tuning R_1 to equalize both the voltages and currents over Q_1 and Q_2. However, the tuning range of R_1 is very narrow and this makes it difficult if not impossible to achieve the "proper" value. Lastly, even with proper tuning of the resistor R_1, the currents flowing through the two BJTs are supply voltage dependent. As a result, when the supply voltage fluctuates, these two currents will fluctuate too, which reduces the output voltage stability and affects the line regulation, the $PSRR$, and the temperature coefficient of the voltage reference circuit. To improve the performance of the Widlar bandgap voltage reference circuit, a sub-circuit can be implemented to ensure the two currents $I_1 = I_2$. A.P. Brokaw presented one such circuit to equalize $I_1 = I_2$, which will be discussed in Section 5.1.1.

5.1.1 Brokaw Bandgap Voltage Reference

A.P. Brokaw in 1974 (Brokaw, 1974) applied an opamp to maintain the currents flowing through the bipolar transistors in the Widlar bandgap voltage reference circuit equal. A simplified schematic of the Brokaw bandgap voltage reference circuit is shown in Figure 5.2. Similar to that of the Widlar bandgap voltage reference circuit, the emitter area of the bipolar transistor Q_2 is made to be N times larger than that of Q_1, thereby resulting in different current density to produce ΔV_{BE}. The V_T extracted from the ΔV_{BE} forms a PTAT voltage. To create a stable and controllable ΔV_{BE}, the currents I_1 and I_2 are made equal by means of an opamp configured to form an inverted feedback loop. Assume the gain of the opamp is large, the two input nodes at A and B are virtually short-circuited because of the inverted feedback loop, and thus $V_A = V_B$. By selecting $R_A = R_B$, the currents flowing through Q_1 and Q_2 will be clamped to be the same by the opamp, and thus $I_1 = I_2 = I$. As a result, the currents flowing through R_2 and R_1 will be I and $2I$, respectively. The KVL loop formed by Q_1, Q_2, and R_2 yields

$$\begin{aligned} IR_2 &= V_{BE_1} - V_{BE_2} \\ &= \Delta V_{BE_{1,2}} = V_T \ln(N) \\ I &= \frac{\Delta V_{BE_{1,2}}}{R_2} = \frac{V_T \ln(N)}{R_2}. \end{aligned} \tag{5.6}$$

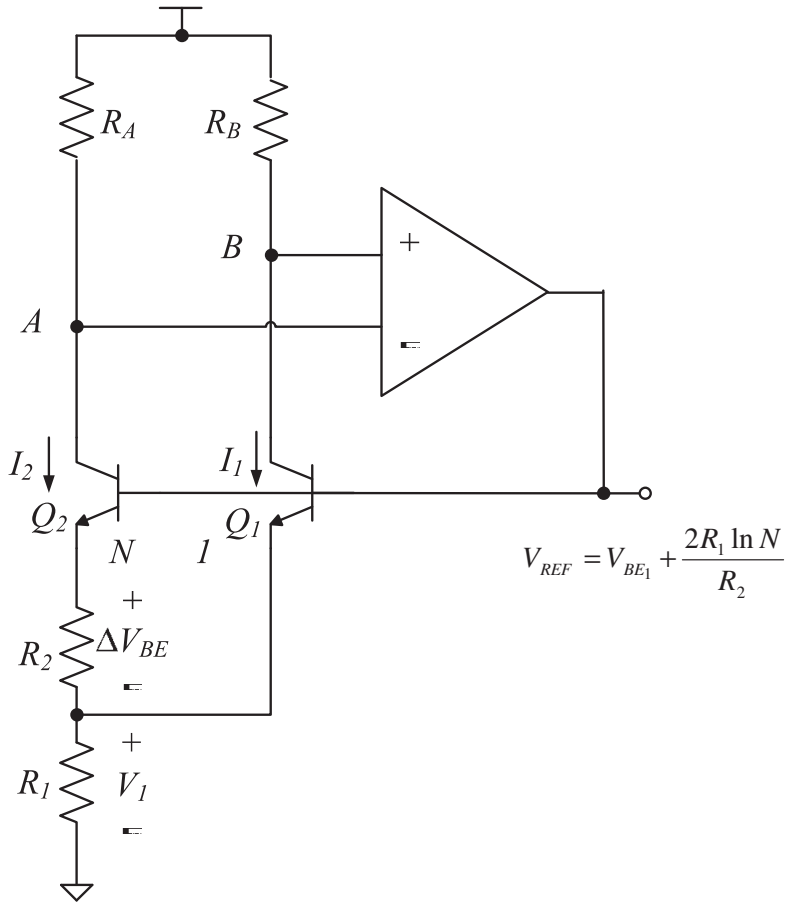


Figure 5.2 A simplified Brokaw bandgap voltage reference circuit (Brokaw, 1974).

Furthermore

$$\begin{aligned} V_1 &= 2IR_1 \\ &= 2R_1 \frac{\Delta V_{BE_{1,2}}}{R_2} \\ &= \frac{2R_1}{R_2} \ln(N) V_T . \end{aligned} \tag{5.7}$$

As a result, V_1 is a scaled version of the PTAT thermal voltage V_T. The reference voltage taken from the base of Q_1 is the sum of the CTAT base-emitter voltage V_{BE_1} and the scaled PTAT voltage V_1.

$$\begin{aligned} V_{REF} &= V_{BE_1} + V_1 \\ &= V_{BE_1} + \frac{2R_1 \ln N}{R_2} V_T . \end{aligned} \tag{5.8}$$

It can be observed that Equation 5.8 has the same form as Equation 3.12 with $M = 2\frac{R_1}{R_2} \ln(N)$, and hence a near-zero TC V_{REF} can be obtained by adjusting R_1, R_2, and N to achieve $M = 19.22$, which will yield $V_{REF} = 1.23$ V. Consider the case of $N = 8$, where $M = 19.22$,

which implies $\frac{R_1}{R_2} = 4.62$. To ensure the bipolar transistors are properly biased, I was chosen to be 6 μA, thus $V_1 = V_{REF} - V_{BE_1} = 1.23 - 0.73 = 0.5 = 2I \times R_1 = 2 \times 6\ \mu R_1$. As a result, $R_1 = 41.67\ \text{k}\Omega$, and $R_2 = R_1/4.62 = 9.02\ \text{k}\Omega$. Lastly, the two undetermined resistors R_A and R_B have to satisfy $R_A = R_B$. Furthermore, the KVL at node B yields $I \times R_B = V_{DD} - V_{REF} - V_{CB_1}$. With the opamp that dynamically biases the two BJTs, it will be difficult to determine V_{CB_1}. However, as a rule of thumb, the forward biased BJT usually has $V_{CE} \approx 0.9$ V, thus V_{CB} can be estimated to be approximately equal to 0.2 V (with $V_{BE} \approx 0.7$ V), which helps to determine R_A and R_B. In this case, if the dynamic range of V_{DD} is given *a priori*, R_B should be determined with the smallest ($V_{DD\,(min)}$), such as to ensure that there will be enough voltage headroom for the overall circuit to operate properly over the entire V_{DD} operating range. As an example,

$$V_{DD\,(min)} \geq IR_A + V_{CE_2} + IR_2 + 2IR_1 \tag{5.9}$$

$$\geq 6\mu\ R_A + 0.9 + 6\mu\ 9.02\text{k} + 2 \times 6\mu\ \times 41.67\text{k}, \tag{5.10}$$

$$3 \geq 6\mu\ R_A + 1.454, \tag{5.11}$$

$$R_A < 257.6\text{k}, \tag{5.12}$$

where by considering $V_{DD,min} = 3$ V, will yield the minimum $R_A = R_B = 257.6\ \text{k}\Omega$. The above will conclude our design of the Brokaw bandgap voltage reference circuit.

The Brokaw bandgap voltage reference circuit is simple and the compensation performance can be easily adjusted by post-processing, such as trimming the resistors R_1 and R_2, thus overcoming the process variation problem. On the other hand, trimming the resistors R_1 and R_2 in the Widlar bandgap voltage reference circuit alters the currents flowing through the BJTs and hence the performance of the voltage reference circuit. As a result, adjusting the performance of the Widlar bandgap voltage reference circuit by trimming is not as easy to implement as it seems. Nevertheless, a Brokaw bandgap voltage reference circuit that applies an opamp has the advantage of a large output driving power, which makes it suitable to be applied in circuits with heavy loads, while the Widlar bandgap voltage reference circuit requires an extra buffer stage to provide the driving power for large loads. However, this extra driving capability comes with the penalty of a large quiescent current and a high minimum operating voltage when compared to that of the Widlar bandgap voltage reference circuit presented in Section 5.1, which makes the Brokaw bandgap voltage reference circuit unfavorable in low power and low voltage applications.

5.1.2 β-Multiplier $V_{BE} - \Delta V_{BE}$ Compensation

One of the reasons that the Brokaw bandgap voltage reference circuit is able to achieve good performance is the inverted feedback loop formed by the opamp, which ensures the currents flowing through both BJTs are equal. There are other techniques that can maintain the currents flowing through the two BJTs to be equal. One of the effective techniques is the β-multiplier circuit, which is a self-biasing circuit, and thus has very good V_{DD} variation immunity. An example of the β-multiplier circuit implemented by opamp to extract the thermal voltage contained in ΔV_{BE} has been presented in Chapter 3, which is commonly adopted in a lot of

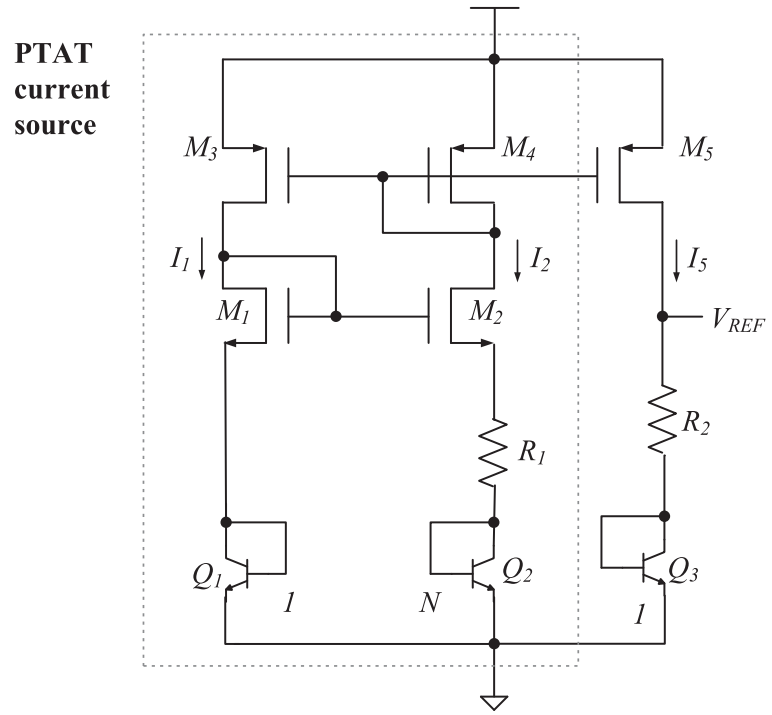


Figure 5.3 Schematic of β-multiplier based $V_{BE} - \Delta V_{BE}$ bandgap voltage reference circuit (Song and Gray, 1983).

CMOS application circuits. Without an opamp, a simple β-multiplier circuit as shown in Figure 5.3 can be used to extract the thermal voltage contained in $\Delta V_{BE_{1,2}}$ (Laber *et al.*, 1987; SanSen *et al.*, 1988). This simple β-multiplier circuit not only reduces the power consumption, it also lowers the voltage headroom required to operate the circuit, while still providing adequate capabilities to clamp the currents flowing through the two arms of the β-multiplier circuit to be the same.

Consider the β-multiplier circuit in Figure 5.3, which generates a PTAT current I_2. This PTAT current is mirrored to the voltage sum reference voltage output sub-circuit by M_5 and converted to a PTAT voltage through resistor R_2, which is summed with the CTAT voltage V_{BE_3} to obtain a near-zero TC reference voltage. The β-multiplier bandgap voltage reference circuit has the same output stage as that of the opamp based β-multiplier bandgap voltage reference circuit. The major difference is the generation of the PTAT current I_2. The transistor M_1, M_2, M_3, and M_4 form two current mirrors. Since M_3 and M_4 have the same V_{GS}, by selecting $S_3 = S_4$, we shall obtain $I_{D_3} = I_{D_4}$. As a result, the currents flowing through M_1 and M_2 should be the same. If we do not consider the short channel effect, the drain voltages of M_3 and M_4 will be the same. Since the gates of M_1 and M_2 are connected together, by selecting $S_1 = S_2$, we shall obtain $I_{D_1} = I_{D_2}$. As a result, $I_1 = I_2$. Again, if we do not consider the short channel effect, the drain voltage of M_1 and M_2 will be the same, which yields

$$\begin{aligned} V_{BE_1} &= V_{BE_2} + R_1 I_2, \\ I_2 &= \frac{(V_{EB_1} - V_{EB_2})}{R_1} = \frac{\Delta V_{BE_{1,2}}}{R_1}. \end{aligned} \tag{5.13}$$

Since $I_1 = I_{BE_1} = I_{BE_2} = I_2$, and the emitter area ratio of the two BJTs Q_1 and Q_2 equals N, it follows that

$$I_1 = I_2 = \frac{\Delta V_{BE_{1,2}}}{R_1} = \frac{V_T \ln N}{R_1}.$$

Thus I_2 is a PTAT current. This PTAT current is copied by the current mirror formed by M_3, M_4 and M_5. If $S_4 = S_5$, we shall obtain

$$I_5 = \frac{V_T \ln N}{R_1},$$

which is proportional to V_T and is independent with V_{DD}. The bandgap voltage reference circuit can be constructed with this PTAT current using the same CTAT voltage sum output stage as that in the conventional bandgap voltage reference circuit in Section 3.2.1. Such a bandgap voltage reference circuit was proposed by Song in (Song and Gray, 1983), where the schematic is shown in Figure 5.3. The reference voltage is given by

$$V_{REF} = I_5 R_2 + V_{BE_3} = \frac{R_2}{R_1} V_T \ln N + V_{BE_3}. \tag{5.14}$$

It can be observed that Equation 5.14 has the same form as Equation 3.12 with $M = \frac{R_2}{R_1} \ln N$, and hence the performance of the above bandgap voltage reference circuit should be comparable to that of the opamp based β-multiplier voltage reference circuit except that the $PSRR$ may be lower. This is because the β-multiplier in Figure 5.3 has a smaller loop gain than that of the opamp-based β-multiplier, which affects its ability to maintain the stability of the two currents flowing through Q_1 and Q_2 when V_{DD} varies.

Note that the implementation of the planar BJTs using the CMOS process always consumes a large silicon area. There are other PTAT current sources which do not require planar BJT. The most common PTAT current generators include Widlar current source, and peaking current source. We shall discuss the first and its variant in a sequel, together with their application in voltage reference circuits, while the latter will be discussed in Chapter 6 for the sub-1V bandgap voltage reference circuits.

Last but not least, the actual design of the β-multiplier PTAT current source starts from recognizing that Equation 5.14 implies R_1 and R_2 have the same values as that in Section 3.13. Furthermore, to ensure proper biasing of the BJTs, the I_{BE} of each bipolar transistor should be larger than or equal to 6 μA in the process under consideration. As a result, the transistor sizes for $M_1 \sim M_5$, and their W/L ratios should be chosen to be large enough to carry at least $|I_{DS}| = 6$ μA with the MOSFET biased at saturation such that there will be enough current to supply to the BJTs.

5.1.2.1 Cascode Current Mirror

The transistors M_3, M_4, and M_5 of the β-multiplier PTAT current source in Figure 5.3 will suffer from channel length modulation for a similar reason that discussed in Section 4.2 for the opamp based β-multiplier bandgap voltage reference circuit in Figure 3.4. This is because of the voltage differences between the V_{DS} of M_3 and that of M_4 and M_5. Similar to Section 4.2.2, the channel length modulation problem can be alleviated by using a cascode

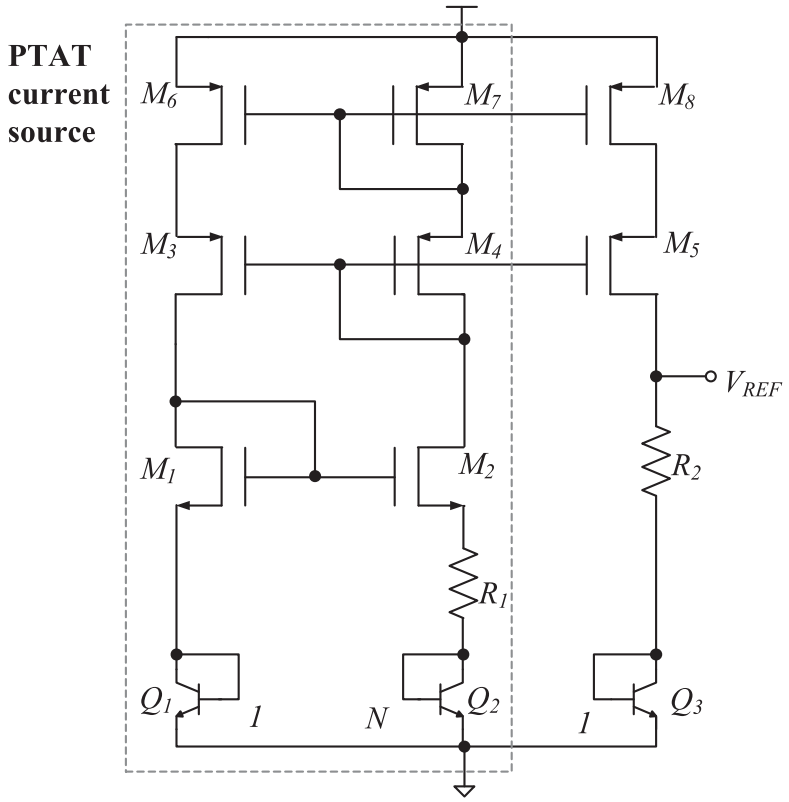


Figure 5.4 Schematic of a channel length modulation effect reduced voltage reference circuit using cascode current mirror. (Tzanateas *et al.*, 1979)

current mirror. Figure 5.4 shows the modified β-multiplier bandgap voltage reference circuit with cascode current mirror. This circuit was first presented in (Tzanateas *et al.*, 1979). The cascode current mirror can promote $PSRR$, and alleviate the problems caused by different V_{DS} of the transistors in the current mirror. However, the intrinsic difference between the V_{DS} voltages of the MOSFETs in the current mirror cannot be resolved by the cascode current mirror. The following section will present a modification of the circuit in Figure 3.4 to enhance the line regulation of the voltage reference circuit by eliminating the intrinsic V_{DS} voltage difference between the MOSFETs in the current mirror.

5.1.2.2 Channel Length Modulation Effect Alleviation

To alleviate the channel length modulation problem of the current mirror in the β-multiplier, we have to maintain the voltages at all the sources, drain, and gate nodes of M_3 and M_4 as equal. Figure 5.5 shows the schematic of a modified β-multiplier bandgap voltage reference circuit with a channel length modulation effect free current mirror M_3 and M_4. The channel length modulation problem of M_4 is alleviated by not connecting M_4 as a diode connected MOSFET. As a result, the node voltage of the drain of M_4 is now free from the V_{SG} constraint of the PMOS transistor. If we further adjust the W/L ratio of M_6 and M_7, such that $V_{GS_6} = V_{GS_2}$. Then the KVL of the transistors M_1, M_2, and M_6 yields

$$V_{D_1} = V_{G_6} = V_{S_2} + V_{GS_6} = V_{S_2} + V_{GS_2} = V_{D_2}.$$

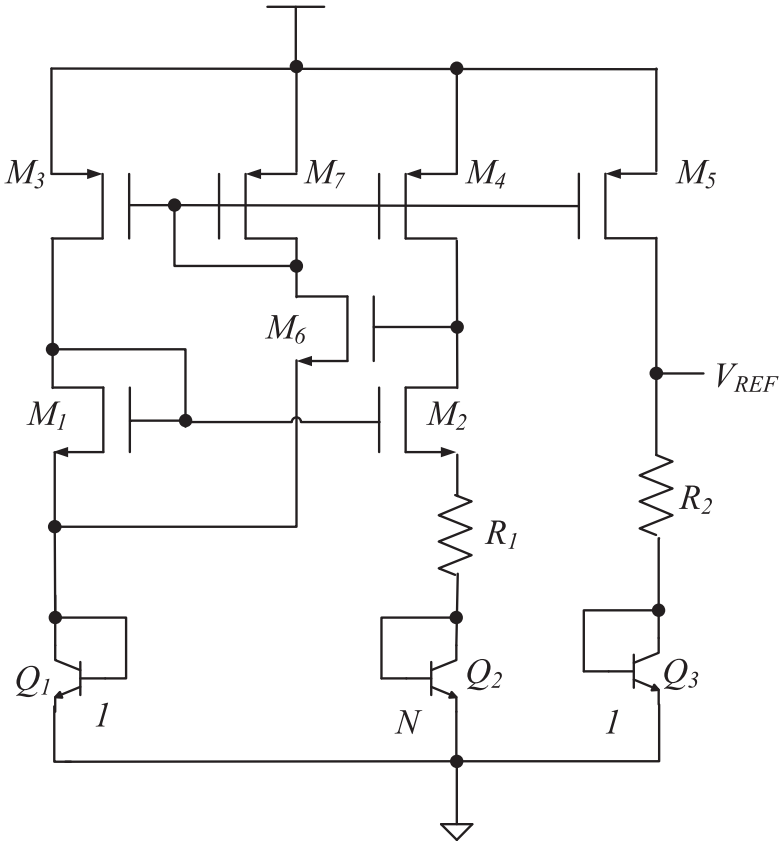


Figure 5.5 Schematic of a channel length modulation effect free β-multiplier, and the associated bandgap voltage reference circuit.

In other words, $V_{D_2} = V_{D_3} = V_{D_4} = V_{D_1}$. Furthermore, the source and gate of M_3 and M_4 are connected, and thus the two transistors are working in exactly the same condition. Therefore, the current mirror is free from the channel length modulation problem, and perfectly generates $I_{DS_1} = I_{DS_2}$.

The core of the bandgap voltage reference circuit in Figure 5.5 is the ΔV_{BE} voltage built up on R_1. There are two currents I_{DS_1} and I_{DS_6} flowing through Q_1. The current I_{DS_6} from M_6 depends on V_{S_6}, which is currently an unknown. Fortunately, the transistors M_4 and M_7 form a current mirror pair, and thus I_{SD_4} and I_{SD_7} are linearly related with respect to the width to length ratios of the two transistors. Furthermore, $I_{SD_7} = I_{DS_6}$. Therefore, the total current that flows through Q_1 can be obtained as

$$I_{DS_1} + I_{DS_6} = \frac{S_3}{S_4} I_{DS_2} + \frac{S_7}{S_4} I_{DS_2} = \left(\frac{S_3 + S_7}{S_4} \right) I_{DS_2}, \tag{5.15}$$

where we use the fact that M_1 and M_2 form a current mirror transistor pair, and thus I_{DS_1} is linearly related to I_{DS_2} with respect to the width and length ratio of the two transistors. If we select

$$S_3 + S_7 = S_4,$$

then we shall obtain $I_{Q_1} = I_{Q_2}$. If we further select $S_5 = S_4$, then V_{REF} is given by Equation 5.14 with output voltage $V_{REF} = 1.23$ V. As a result, at least in theory, the performance of the bandgap voltage reference circuit in Figure 5.5 has an output comparable to that of Figure 5.3. The devices in the circuit in Figure 5.5 can be designed in a similar manner as that in Figure 5.3.

The channel length modulation effect of the current mirror in the schematic of Figure 5.5 is almost perfectly eliminated, except that the width to length ratio of M_6 and M_7 can only be obtained by brute force and through extensive trial and error. Furthermore, a closer look at the schematic in Figure 5.5 will find that instead of having M_4 connected as a diode, its now M_7 being connected as a diode in the current mirror formed by M_7, M_3, M_4, and M_5. As a result, M_7 will be subject to the channel length modulation problem. On the other hand, by carefully selecting $S_7 << S_3$, S_4, S_5, the channel length modulation effect of M_7 on the output voltage variation caused by the variation of I_7 due to V_{DD} variation can be minimized and neglected in the analysis. As an example, the channel length modulation induced current variation is usually within 10% of the desired current value. Therefore, if the MOSFET W/L ratios S_3, S_4, and S_5 are chosen to be one hundred times larger than S_7, then the reference voltage variation induced by channel length modulation of M_7 due to input voltage variation will be small enough to be neglected. As a result, except for being difficult to obtain the optimal ratio between S_6 and S_7, this circuit can still be effectively applied to alleviate the channel length modulation problem of the current mirror in the β-multiplier circuit by selecting $S_7 << S_3$, S_4, S_5 as a design rule of thumb.

5.2 Widlar PTAT Current Source and V_{BE} Compensation

Besides ΔV_{BE}, there are a number of self-biased V_T extraction circuits that can be applied in the design of the voltage reference circuit. Among a large number of self-biased topologies presented in literature, we shall concentrate on the β-multiplier based self-biased current source. Furthermore, within various β-multiplier PTAT current sources, we shall limit ourselves to the self-biased Widlar PTAT current source (Widlar, 1971) (we shall call such a current source circuit a *Widlar PTAT current source* or simply Widlar current source in this book, as it is a generally accepted name for this circuit), and its variants in this section and the following subsections. We shall discuss their pros and cons, and possible remedies for each problem. We shall also discuss their applications in the Widlar-V_{BE} compensation based bandgap voltage reference circuit.

Figure 5.6 shows the schematic of a Widlar current source (a PTAT current generator), which looks like the β-multiplier ΔV_{BE} circuit in Figure 5.3 without the BJTs. Such a current source has been applied to implement voltage reference circuit (Tzanateas *et al.*, 1979), which resembles a similar schematic as the β-multiplier bandgap voltage reference circuit in Section 5.1. The transistors M_3, M_4 and M_1, M_2 form two pairs of current mirrors, such that the currents flowing into M_1 and M_2 are the same. The Widlar current source makes use of the ΔV_{GS} from a pair of MOSFETs working in subthreshold mode as the temperature dependent PTAT source. Similar to the ΔV_{GS} property studied in Section 1.2.2.1, the Widlar current source explores the difference in the current density I_{DS} between M_1 and M_2 with $S_1 \neq S_2$ to generate $\Delta V_{GS_{1,2}}$. The $\Delta V_{GS_{1,2}}$ will be converted to a current I_2 by resistor R_1. If I_1 is

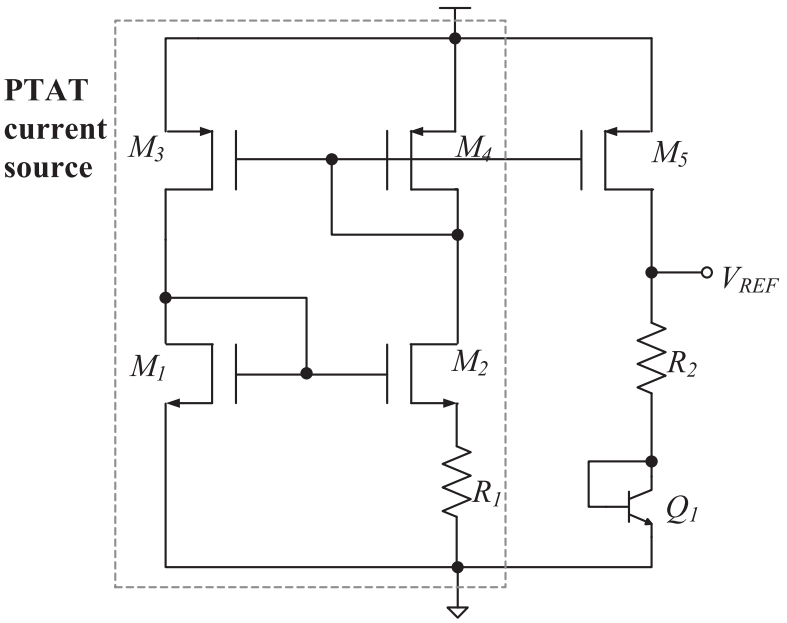


Figure 5.6 Schematics of Widlar current source (inside the dotted box) (Widlar, 1971), and the associated bandgap voltage reference circuit (Tzanateas *et al.*, 1979).

selected to bias M_1 to work in subthreshold mode, then the (I_1, V_{GS_1}) relationship is given by Equation 1.18 as

$$\begin{aligned} I_1 &= I_{D,leak} \exp \frac{V_{GS_1}}{\zeta V_T} \\ &= \hat{I}_{D,leak} S_1 \exp \frac{V_{GS_1}}{\zeta V_T}. \end{aligned}$$

We can obtain V_{GS_1} by rearranging the above equation as

$$V_{GS_1} = \zeta V_T \ln \left(\frac{I_1}{\hat{I}_{D,leak} S_1} \right). \tag{5.16}$$

Similarly, we shall obtain

$$V_{GS_2} = \zeta V_T \ln \left(\frac{I_2}{\hat{I}_{D,leak} S_2} \right). \tag{5.17}$$

Since the gates of M_1 and M_2 are connected, the difference between V_{GS_1} and V_{GS_2} will be observed as the voltage across R_1.

$$\begin{aligned} I_2 R_1 &= V_{GS_1} - V_{GS_2} = \Delta V_{GS_{1,2}} \\ &= \zeta V_T \ln \left(\frac{I_1 S_2}{I_2 S_1} \right) = \zeta V_T \ln \left(\frac{I_1}{I_2} N \right), \end{aligned} \tag{5.18}$$

where $N = \frac{S_2}{S_1}$ is the transistor size ratio between M_2 and M_1. If we choose $S_3 = S_4$, then the current mirror formed by M_3 and M_4 will have $I_1 = I_2$, and thus Equation 5.18 can be rewritten as

$$I_2 = \frac{\Delta V_{GS_{1,2}}}{R_1} = \frac{\zeta V_T}{R_1} \ln(\mathrm{N}). \tag{5.19}$$

This PTAT current can be copied by transistor M_5 which is configured to form a current mirror transistor pair with M_4. When this PTAT current is applied to the same output stage of the conventional opamp-based β-multiplier voltage reference circuit as shown in Figure 5.6, a Widlar-V_{BE} voltage reference circuit will be obtained, which is first presented in (Tzanateas *et al.*, 1979). The output voltage is given by

$$V_{REF} = \frac{R_2}{R_1} \zeta \ln(N) V_T + V_{BE_1}. \tag{5.20}$$

It can be observed that Equation 5.20 has the same form as Equation 3.12 with $M = \frac{R_2}{R_1} \zeta \ln(N)$. As a result, at least in theory, the performance of the bandgap voltage reference circuit in Figure 5.6 is comparable to that of the opamp based β-multiplier bandgap voltage reference circuit. To determine the component values in the schematic, we should note that Equation 3.12 implies near-zero TC reference voltage at $T = T_{(nom)}$ is obtained with $M = 19.22$, and the associated $V_{REF} = 1.23$ V. The BJT Q_1 will be properly biased with $I_5 = 6$ μA, and thus $R_2 = (V_{REF} - V_{BE_1})/I_5 = (1.23 - 0.73)/6\mu = 82.9$ kΩ. If we select $N = 8$, then $R_1 = R_2 \zeta \ln(N)/M = 82.9\ \mathrm{k}(1.5) \ln(8)/19.22 = 13.45$ kΩ. At the same time, the transistor sizes for $M_1 \sim M_4$ should be chosen such that their W/L ratios are large enough to carry at least 50 nA to correctly bias the MOSFET to work at the subthreshold region. As a result, the transistor size ratio is required to be approximately $S_5/S_3 = 6\ \mu/50$ n=120.

The Widlar current source based voltage reference circuit has the advantage of consuming very little power where the total current consumption of the circuit is $I_3 + I_4 + I_5 \geq 50\ \mathrm{n} + 50\ \mathrm{n} + 6\ \mu = 6.1$ μA. While that of the β-multiplier $V_{BE} - \Delta V_{BE}$ bandgap voltage reference circuit in Figure 5.3 has a total current consumption of $I_1 + I_2 + I_3 \geq 18$ μA. Furthermore, the Widlar current source based voltage reference circuit can operate at a lower V_{DD}, thus further reducing the power dissipation. However, M_3 in Figure 5.6 will suffer from the channel length modulation effect, and hence lower the $PSRR$. This problem is found to be severe in the Widlar current source when compared to that of the opamp-based β-multiplier ΔV_{BE} PTAT current source. This is because both M_3 and M_4 are biased to work in the subthreshold mode in the Widlar current source, and thus the two transistors M_3 and M_4 do not form a proper current mirror. Finally, the V_{DD} required to operate the Widlar-V_{BE} bandgap voltage reference circuit is constrained by the output voltage $V_{REF} = 1.23$ V, which is still larger than that required for the sub-1V reference voltage. In Chapter 6, the peaking current source will be introduced, which is shown to have the ability of achieving stable output voltage with sub-1V V_{DD}.

5.3 V_{GS} Based Temperature Compensation

The bandgap voltage reference circuits presented in previous sections utilize the compensation between PTAT voltage and CTAT V_{BE} voltage to generate a near-zero TC reference voltage.

Since the V_{BE} voltage of the BJT is highly process dependent, and the BJT usually occupies a comparatively large silicon area. Any extra costs and efforts attempting to alleviate the adverse effect of the process variation problem of the BJT will result in increased silicon area. A BJT free Widlar PTAT source (a ΔV_{GS} current source) presented in Section 5.2 can be used to partially alleviate the problem. In this section, we shall present a BJT free CTAT source that makes use of V_{GS} as the PTAT source. However, due to the finite output resistance of the MOSFETs, the V_{GS} based CTAT source has a low $PSRR$, and thus lowers the $PSRR$ of the bandgap voltage reference circuit constructed by the $\Delta V_{GS} - V_{GS}$ compensation technique. A channel length modulation effect alleviation technique will be presented at Section 5.3.1.1 to improve the $PSRR$ of the $\Delta V_{GS} - V_{GS}$ based voltage reference circuit.

5.3.1 V_{GS} Current Source

Figure 5.7 shows the schematic of a V_{GS} current source which exhibits a CTAT property (bounded within the CTAT dashed box). The circuit makes use of a resistor connected in parallel to the gate and source terminals of a MOSFET to generate a CTAT current. To understand how it works, let's start examining the circuit from the transistors M_5, M_7, and M_9 which are configured to form current mirror pairs. By selecting $S_5 = S_7 = S_9$, the currents passing through all transistors $M_5 \sim M_9$ will be the same. Consider the case of M_6 being biased at saturation, such that I_{DS_6} is given by Equation 1.26 as

$$I_{DS_6} = \frac{1}{2}\mu_n C_{ox,n} S_6 (V_{GS_6} - V_{th,n})^2.$$

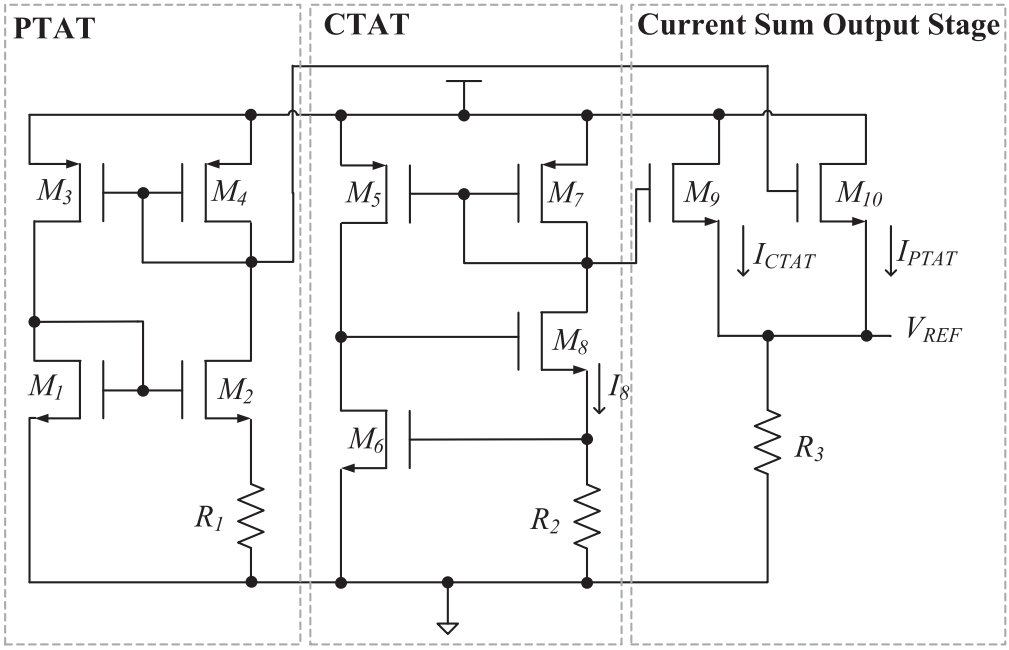


Figure 5.7 Schematic of a V_{GS} base CTAT current source, and the associated $V_{GS} - \Delta V_{GS}$ compensation bandgap voltage reference circuit.

Rearranging the terms in the equation yields

$$V_{GS_6} = V_{th,n} + \sqrt{\frac{2I_{DS_6}}{\mu_n C_{ox,n} S_6}}.$$

If M_6 is designed to have $I_{DS_6} << \mu_n C_{ox,n} S_6$, then

$$V_{GS_6} \approx V_{th,n}.$$

Without considering the short channel effect, the current mirror M_5 and M_7 ensures that $I_{SD_5} = I_{SD_7}$. Furthermore $I_{SD_5} = I_{DS_6}$, therefore,

$$I_{SD_7} = I_{DS_6} = \frac{V_{GS_6}}{R_2} \approx \frac{V_{th,n}}{R_2}. \tag{5.21}$$

Section 1.2.5.1 has shown that $V_{th,n}$ has CTAT property, and hence the current I_{SD_7} is also CTAT. This temperature dependent current source is also known as threshold voltage self-biasing current source. The current I_{SD_7} derived in Equation 5.21 is shown to be independent of the supply voltage. However, in practice this is seldom the case because of the finite output resistance of the MOSFETs. On the other hand, the self-biasing structure that implements a cascoding M_5 and M_7 helps to reduce the supply voltage sensitivity. As a result, this V_{GS} current source yields a low supply voltage sensitivity that is applicable for constructing a useful voltage reference circuit. This V_{GS} based CTAT current can be used in conjunction with the Widlar PTAT current source in Section 5.2 to generate a near-zero TC reference voltage. Figure 5.7 shows the complete $\Delta V_{GS} - V_{GS}$ voltage reference circuit. The CTAT current is copied by the current mirror formed by M_7 and M_9, while the PTAT current is copied by the current mirror formed by M_4 and M_{10}. These two currents are summed and converted to a voltage by resistor R_3. As a result, the output voltage is given by the sum of the two scaled currents in Equation 5.21 and 5.19 over resistor R_3 as

$$\begin{aligned} V_{REF} &= \frac{R_3}{R_1}\frac{S_{10}}{S_4}\zeta \ln(N) V_T + \frac{R_3}{R_2}\frac{S_9}{S_7} V_{th,n} \\ &= \frac{R_3}{R_2}\frac{S_9}{S_7}\left(\frac{R_2}{R_1}\frac{S_7}{S_9}\frac{S_{10}}{S_4}\zeta \ln(N) V_T + V_{th,n}\right). \end{aligned} \tag{5.22}$$

It can be observed that Equation 5.22 has a similar form as Equation 3.12 with V_{BE} being replaced by $V_{th,n}$ and $M = \frac{R_2}{R_1}\frac{S_7}{S_9}\frac{S_{10}}{S_4}\zeta \ln(N)$. As a result the stability of the temperature compensated reference voltage is determined by the matching between the resistors R_2 and R_1, the transistors M_4 and M_{10}, the transistors M_7 and M_9, and the stability of $V_{th,n}$. The first three requirements are similar to those required by the Widlar-V_{BE} bandgap voltage reference circuit in Section 5.2. The last requirement on the threshold voltage of the MOSFET in the CMOS process is usually tightly controlled, and thus $V_{th,n}$ will experience smaller process variation than that of V_{BE}. As a result, the voltage reference circuit in Figure 5.7 should have better stability than that in Section 5.2. However, the matching between resistors R_3 and R_2, and the transistors M_7 and M_9, will affect the absolute output voltage of the voltage reference circuit.

As a result, in view of the absolute output voltage variation, the circuit in Figure 5.7 is less favorable than that presented in Section 5.2 because of the possible extra matching problem between R_2 and R_3, and M_7 and M_9. Nevertheless, because of the area efficient layout due to the lack of BJT device, the voltage reference circuit in Figure 5.7 has been employed in a large number of practical circuits. A number of modifications have been presented in literature to further improve the performance of the circuit in Figure 5.7, including the improvement of the $PSRR$ of the voltage reference circuit by alleviating the channel length modulation effect suffered by the current mirror transistors in the CTAT source, which will be presented in the next section.

Last but not least, it is noted that a sub-1V V_{REF} may be obtained by properly scaling $\frac{R_3}{R_2}\frac{S_9}{S_7}$. However, the operating voltage of the V_{GS} CTAT current source is limited by $V_{GS_6} + V_{GS_8} + V_{GD_5} + V_{SG_5} \approx 0.7 \times 3 + 0.1 = 2.2$ V. Therefore, for the process under consideration in this book, V_{DD} is required to be higher then 2.2 V for the CTAT current source to obtain a stable output. As a result, the circuit in Figure 5.7 cannot be used as a sub-1V supply voltage reference circuit.

5.3.1.1 Channel Length Modulation Effect Alleviation

Using a similar technique as that presented in Section 5.1.2.2, the channel length modulation effect can be alleviated by releasing the node voltage of the drain of the PMOS M_4 from the V_{SG} voltage constraint. As a result, the current mirrors of both the PTAT and CTAT current sources can be designed to be free from the channel length modulation problem. While the derivation on the voltages and currents of such a channel length modulation alleviated Widlar current source is left as an exercise for the readers (Exercise 5.6), we shall present in this section a different method to alleviate the channel length modulation problem of the CTAT source. Figure 5.8 shows the modified $\Delta V_{GS} - V_{GS}$ compensated voltage reference circuit compared to the CTAT source in Figure 5.7. To alleviate the channel length modulation problem of the current mirror of the CTAT source, the CTAT source in Figure 5.8 has an extra current I_{11}

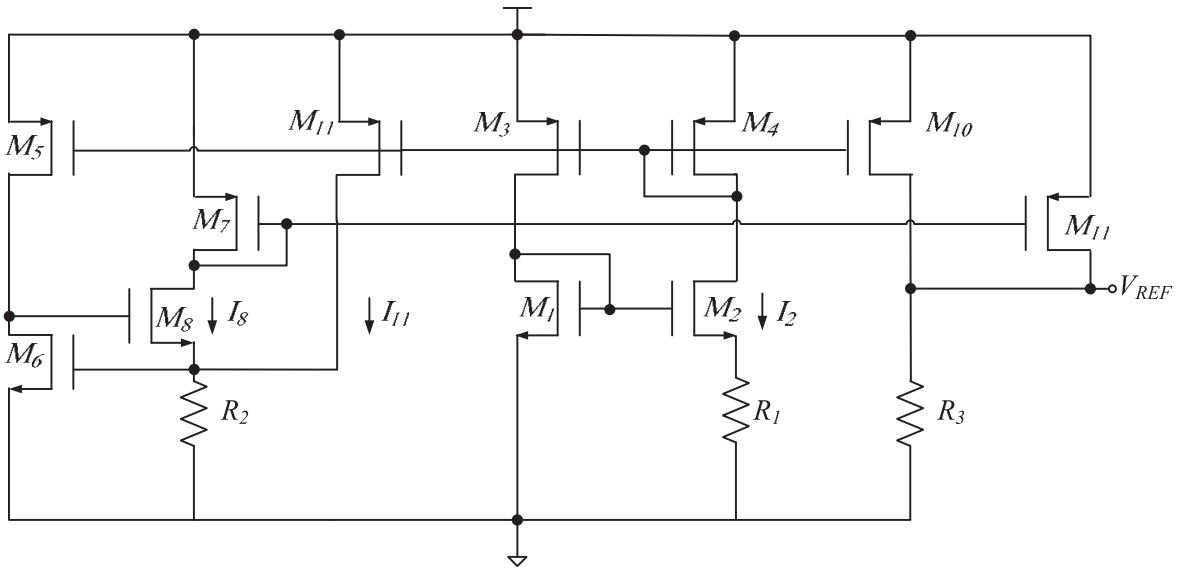


Figure 5.8 V_{GS} and Widlar current source compensation (Lin and Huang, 2006).

mirrored from I_4 of the ΔV_{GS} current source to inject into the V_{GS} current source. As a result, the CTAT current I_8 will be modified as

$$I_8 = \frac{V_{GS_6}}{R_2} - I_{11}.$$

Since $I_7 = I_8$, therefore, the reference voltage is modified as

$$\begin{aligned} V_{REF} &= \left(\frac{S_{10}}{S_4} I_4 + \frac{S_9}{S_7} I_7\right) R_3 \\ &= \left(\frac{S_{10}}{S_4} I_4 + \frac{S_9}{S_7}\left(\frac{V_{GS_6}}{R_2} - I_{11}\right)\right) R_3 \\ &= \left(\frac{S_{10}}{S_4} I_4 + \frac{S_9}{S_7}\left(\frac{V_{GS_6}}{R_2} - \frac{S_{11}}{S_4} I_4\right)\right) R_3 \\ &= \left(\left(\frac{S_{10}}{S_4} - \frac{S_9}{S_7}\frac{S_{11}}{S_4}\right) I_4 + \frac{S_9}{S_7}\frac{V_{GS_6}}{R_2}\right) R_3. \end{aligned} \tag{5.23}$$

If we substitute I_4 in Equation 5.4 and $\frac{V_{GS_6}}{R_2}$ in Equation 5.21 into Equation 5.23 will yield

$$\begin{aligned} V_{REF} &= \left(\frac{S_{10}}{S_4} - \frac{S_9}{S_7}\frac{S_{11}}{S_4}\right)\frac{R_3}{R_1}\zeta V_T \ln N + \frac{S_9}{S_7}\frac{R_3}{R_2} V_{th,n} \\ &= \frac{R_3}{R_2}\frac{S_9}{S_7}\left(\left(\frac{S_{10}}{S_4}\frac{S_7}{S_9} - \frac{S_{11}}{S_4}\right)\frac{R_2}{R_1}\zeta V_T \ln N + V_{th,n}\right). \end{aligned} \tag{5.24}$$

It can be observed that Equation 5.24 has a similar form Equation 3.12 with V_{BE} being replaced by $V_{th,n}$, and $M = \left(\frac{S_{10}}{S_4}\frac{S_7}{S_9} - \frac{S_{11}}{S_4}\right)\frac{R_2}{R_1}\zeta \ln N$. As a result, this modified circuit has the same performance as that in Section 3.1, at least in theory.

The only difference between the schematics in Figure 5.7 and Figure 5.8 is that the current I_{11} in the schematic of Figure 5.8 forms a negative term in V_{REF} in Equation 5.24. In this case, when M_4 suffers from a channel length modulation effect, the effective S_4 will alter, and the term $\frac{S_{10}}{S_4}\frac{S_7}{S_9}$ in M will increase or decrease depending on the effective value of S_4 after the channel length modulation effect. Assume the variation of the effective value of S_4 affected by channel length modulation is $S_4(1 - \epsilon_{S_4})$. If we expand this term by Taylor series, we shall obtain

$$\frac{S_{10}}{S_4(1-\epsilon_{S_4})}\frac{S_7}{S_9} \approx \frac{S_{10}}{S_4}\frac{S_7}{S_9}(1+\epsilon_{S_4}), \tag{5.25}$$

where we assume $0 < \epsilon_{S_4} << 1$, such that $\epsilon_{S_4}^n \approx 0$ with $n \geq 2$. On the other hand, when the second term $\frac{S_{11}}{S_4}$ is expanded by Taylor series with the value of S_4 being applied.

$$\frac{S_{11}}{S_4(1-\epsilon_{S_4})} \approx \frac{S_{11}}{S_4}(1+\epsilon_{S_4}). \tag{5.26}$$

As a result, the channel length modulation problem can be alleviated when the variation in Equation 5.25 is being compensated by Equation 5.26, which can be achieved by selecting a set of appropriate transistor sizes for M_7, M_9, M_{10}, and M_{11}, such that

$$\begin{aligned} \frac{S_{11}}{S_4}\epsilon_{S_4} &= \frac{S_{10}}{S_4}\frac{S_7}{S_9}\epsilon_{S_4} \\ S_{11} &= S_{10}\frac{S_7}{S_9}. \end{aligned} \tag{5.27}$$

In other words, when S_{11} is chosen to satisfy Equation 5.27, the voltage reference circuit in Figure 5.8 will be free from the channel length modulation problem of M_4. This technique is first presented in (Lin and Huang, 2006), and is shown to be almost perfect for alleviating the channel length modulation problem if the transistor sizes match well. Otherwise, the channel length modulation problem will be worsened by the added current I_{11}. In reality, the transistor size ratio will never match well, and thus the reference voltage will suffer from the incorrect compensation current I_{11}. As a result, a trimming network is required to implement M_{11} in order to generate the required I_{11}.

5.4 Summary

In this chapter, we have discussed various bandgap voltage reference circuit topologies with a focus on their working principle and temperature dependency. Different voltage reference circuit topologies employ different methods to extract the CTAT voltage (in the case of this chapter, it will be the base-emitter voltage V_{BE}, and the gate-to-source voltage V_{GS} of MOSFET biased at weak inversion), and the PTAT voltage. Furthermore, different circuit methodologies are employed to perform the PTAT and CTAT voltage/current sources addition/subtraction. The base-emitter voltage in the Widlar's design is obtained from Q_3, and a PTAT voltage is super-positioned (summed) with the CTAT base-emitter voltage obtained by biasing Q_3 and a resistor with a current I, which is PTAT. However, a portion of I is not PTAT in the Widlar's design, which affects the mutual compensation result, and thus cannot be used to obtain the reference voltage with a low temperature coefficient. The bandgap voltage reference circuit proposed by A.P. Brokaw (Brokaw, 1974) eliminates the BJT base current problem of being not completely PTAT by providing the current drive of the bases from the output of an opamp with inputs obtained from two BJTs with different emitter areas. This circuit also has all the advantages of the opamp based β-multiplier bandgap voltage reference circuit discussed in Chapter 3 with a PTAT current that biases all the transistors. Furthermore, these kind of opamp based voltage reference circuits have an additional merit in that they are able to drive large loading because of the high driving power of the opamp. The Widlar voltage reference circuit, however, cannot supply adequate power to subsequent circuits (output loading) without affecting the biasing current I. As a result, a buffer stage is still required to generate V_{REF} before supplying it to subsequent circuits with low input impedances. Other disadvantages of the opamp driven voltage reference circuits include large silicon area, high power consumption, and high voltage headroom, etc.

Besides using the V_{BE} to extract the temperature dependent voltage/current, in the late 1970s, when weak-inversion MOSFETs came into the picture of CMOS circuit design, bandgap voltage reference circuits implemented with MOSFETs biased in the subthreshold region were also proposed. In 1979, both Vittoz (Vittoz and Neyroud, 1979) and Tzanateas (Tzanateas

et al., 1979), published CMOS bandgap voltage reference circuits, where the PTAT voltage was realized by MOSFETs biased to work in the subthreshold region. As derived in Section 5.2, the temperature coefficients of the CMOS bandgap voltage reference circuits using MOSFETs in the subthreshold mode as temperature dependent devices can in theory achieve the same temperature coefficients as the opamp-based β-multiplier bandgap voltage reference circuits using V_{BE}. On the other hand, unlike the BJT based bandgap voltage reference circuits, The process corner variation of the MOSFET threshold voltages will cause the voltage reference circuit using MOSFETs biased in the subthreshold region a significant reference voltage variation of up to $\pm 15\%$ in the worst process corner. It should be noted that the effect of process variation is inevitable and requires different means to compensate for various effects on each component within the voltage reference circuit. This threshold voltage inaccuracy makes the voltage reference circuit using MOSFET in the subthreshold region difficult to apply in many applications. To overcome this problem, voltage reference circuits should use a reflective/ratio of threshold voltages as in Section 7.5.3 and Exercise 5.11, or apply special threshold voltage variation compensation techniques. The basic linear compensation of the PTAT and CTAT voltages discussed in this chapter will be extended to include advance curvature correction circuits in Chapter 7. Various curvature correction methodologies will be studied, and we shall also demonstrate that the increased design complexity of the curvature corrected bandgap voltage reference circuits can achieve better temperature compensation results than those achieved using linear compensation methods.

The reader should expect there to be a large number of voltage reference circuits in both the literature and practical implementations. Fortunately, most of the practical voltage reference circuits are variants of the presented voltage reference circuits. This is because almost all temperature depending devices can be applied to establish PTAT and CTAT sources, and any voltage/current sum/subtracting circuits can be applied to achieve mutual temperature compensation between the PTAT and CTAT sources, and hence generate near-zero TC reference voltages. In particular, most of the voltage reference circuits considered in this Chapter are bandgap voltage reference circuits that make use of the base-emitter voltage of the BJTs. The performance of the silicon voltage reference circuit relies on the behavior of the silicon bandgap voltage and the physical phenomena underlying the base-emitter voltage, as these physical properties are largely the same for all the bandgap voltage reference circuits. Therefore it has been shown that the temperature coefficient of the generated reference voltage is largely the same for various bandgap voltage reference circuit topologies using the V_{BE} of BJTs presented in this Chapter. However, some differences may exist because of the way of implementation. Furthermore, different voltage reference circuit topologies should be adopted based on the design requirements presented in Chapter 2 too.

5.5 Exercises

Exercise 5.1 *When the amplifier gain is limited, the inverted configured opamp of the Kuijk voltage reference circuit (Kuijk, 1973) shown in Figure 5.9 cannot achieve a virtual short circuit between V_+ and V_-, and there will be a ΔV difference between V_+ and V_-.*

1. *Derive the output voltage with the consideration of ΔV.*
2. *Given the gain of the amplifier is A, determine the reference output voltage with A and without ΔV.*

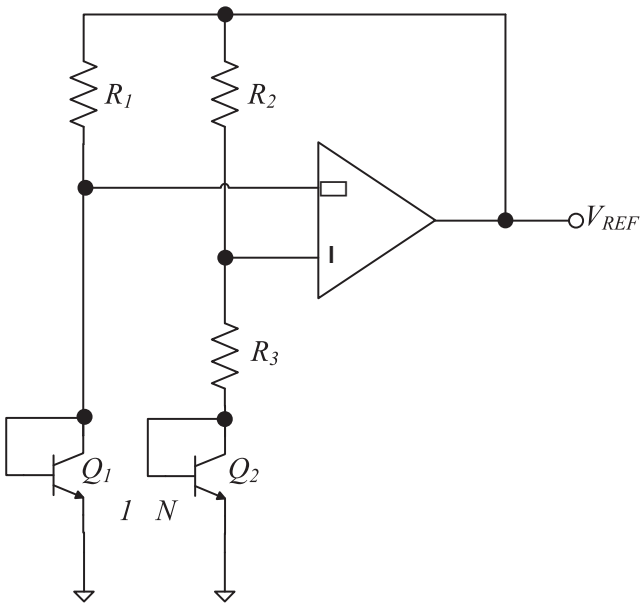


Figure 5.9 Kuijk voltage reference circuit (Kuijk, 1973) with limited gain opamp for Exercise 5.1.

Exercise 5.2 *Derive the resistor ratio each of the following voltage reference circuits to obtain a near-zero TC reference voltage of* $V_{REF} = 1.23\,\text{V}$ *at* $T = T_{nom}$ *with all current mirror ratio being 1:1,* $N = 8$ *and* $\zeta = 1.5$*.*

1. *Widlar voltage reference circuit given by Equation* 5.5*,*
2. *Brokaw voltage reference circuit given by Equation* 5.8*,*
3. *Widlar PTAT current source –* V_{BE} *temperature compensated voltage reference circuit like that described in Equation* 5.20*,*
4. V_{GS} *current source* V_T *compensation in Equation* 5.22*.*

Exercise 5.3 *The Kuijk bandgap voltage reference circuit is simple to construct and can achieve low TC, however, the output voltage is easily affected by the output load. To improve the output stability, an improved Kuijk bandgap voltage reference circuit is shown in Figure 5.10. The circuit in Figure 5.10 is a variation of (Werking, 2006), which modified the Kuijk bandgap voltage reference with an additional* Q_3 *between* R_3*,* R_4*, and* V_{DD}*. The base of* Q_3 *is biased from the output of the opamp which is aimed at obtaining a good* $PSRR$*. If we choose* $R_3 = R_4$*, it will ensure the feedback loop formed between* Q_3*,* R_3*, and* R_4 *is stable, and thus ensure that* V_+ *and* V_- *of the opamp input are virtually short-circuited, and hence have the same potential. Derive the output voltage* V_{REF} *of this circuit, and discuss what the potential problem of such a circuit is.*

Exercise 5.4 *This exercise will demonstrate the minimum operation voltage limitation of the Kuijk bandgap voltage reference circuit showing in circuit Figure 5.9.*

1. *Derive the minimum and maximum* V_{BE} *voltage in the temperature range of* $0\,^\circ\text{C}$ *and* $100\,^\circ\text{C}$*.*

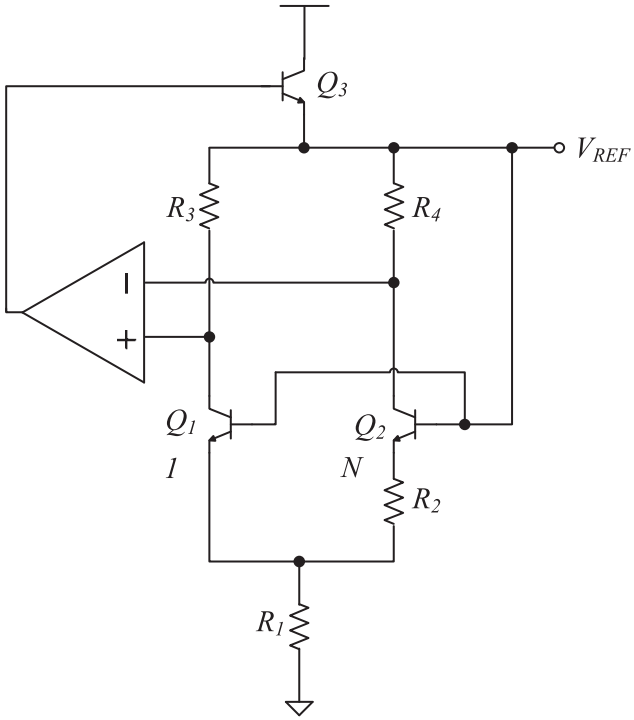


Figure 5.10 An improved Kuijk bandgap voltage reference circuit obtained from a variant of (Werking, 2006) for Exercise 5.2.

2. *Let $V_{gst,N}$ and $V_{gst,P}$ be at least* 0.2 V*, show that the Kuijk's bandgap voltage reference circuit cannot adopt an opamp with NMOS input stage if the operating temperature range of the circuit is required to be* [0 °C, 100 °C].
3. *Derive the minimum operating voltage of the Kuijk bandgap voltage reference circuit with respect to an opamp with PMOS input stage.*

Exercise 5.5 *Estimate the minimum operating supply voltage for the bandgap voltage reference circuit in Figure 5.3.*

Exercise 5.6 *Channel length modulation effect alleviation for Widlar PTAT current-V_{BE} compensation voltage reference circuit.*

To maintain $I_1 = I_2$ in the Widlar current source in Figure 5.6, we must alleviate the channel length modulation problem by maintaining the voltages at all the sources, drain, and gate nodes of M_3 and M_4 as equal. Figure 5.11(a) shows the schematic of a modified Widlar current source which is free from the channel length modulation effect using the same technique as described in Section 5.1.2.2. The following questions will guide you to derive the working principle of the channel length modulation effect free Widlar current source.

1. *Refer to Section 5.1.2.2, determine the design constraint on V_{GS_6}, and use the KVL of the transistors M_1, M_2, and M_6 to show that $V_{D_3} = V_{D_4}$.*
2. *Explain why the Widlar current source is free from the channel length modulation problem.*
3. *Derive $\Delta V_{GS_{1,2}}$ in terms of V_T.*

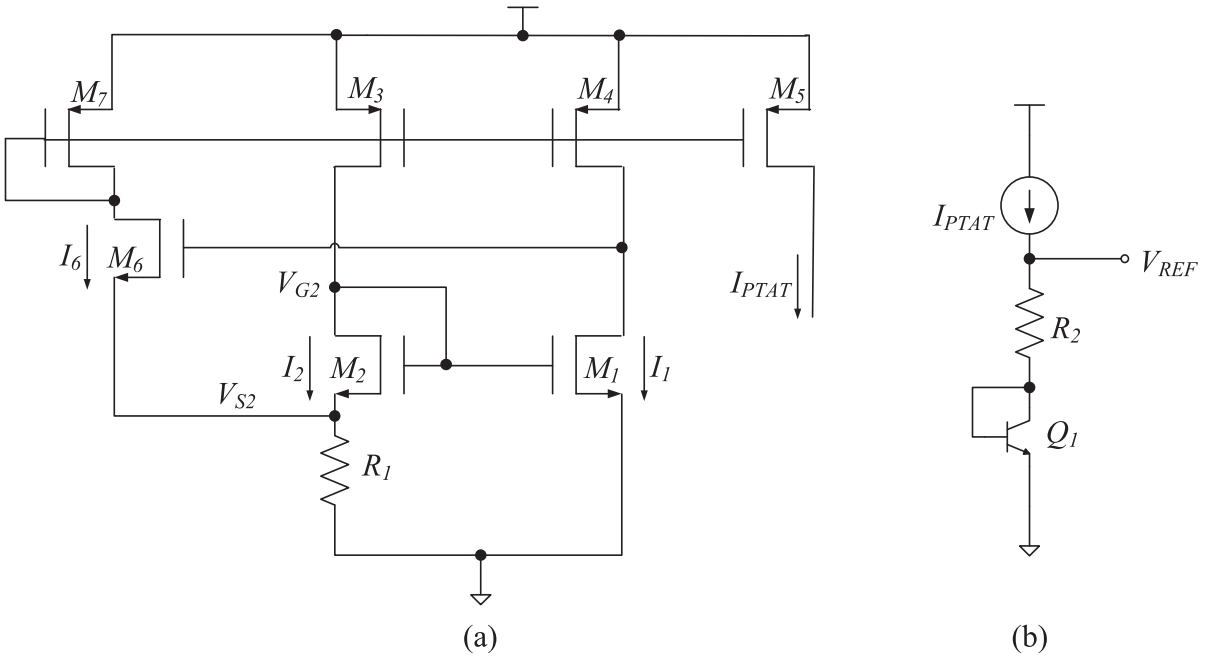


Figure 5.11 (a) Schematic of channel length modulation effect free current source, and (b) the associated bandgap voltage reference circuit for Exercises 5.6 and 5.7.

4. *Derive the PTAT current I_{DS_2} in term of V_T, the W/L ratio of transistors, ζ, and R_1 only.*
5. *A near-zero TC reference voltage can be obtained by feeding I_{PTAT} to a series connected R_2 and Q_1, output stage as shown in Figure 5.11(b). Derive V_{REF} in the form of a summation of weighted V_T and weighted V_{BE}, and show that it can achieve a similar performance to that of the conventional opamp based β-multiplier bandgap voltage reference circuit.*
6. *Determine the transistor size ratio to achieve $V_{REF} = \frac{R_2}{R_1}\zeta V_T + V_{BE_1}$.*
7. *List the implementation (fabrication) limitations of this voltage reference circuit.*

Exercise 5.7 *Derive the minimum V_{DD} required for the channel length modulation free Widlar current source in Figure 5.11 to operate properly. Also derive the maximum V_{DD} that can operate the circuit without damaging the device.*

Exercise 5.8 *As discussed in Chapter 3, any temperature sensitive devices can be used to construct a temperature insensitive voltage reference circuit. This exercise will study the application of a temperature sensitive resistor to construct a temperature insensitive voltage reference circuit. The circuit under consideration is shown in Figure 5.12, which is similar to that in Figure 5.11. The resistors R_1 and R_2 are both temperature sensitive resistors but they are allowed to have different temperature coefficients. Assume M_1, M_2, and M_6 are biased to work in subthreshold region, and M_3, M_4, M_5, and M_7 form perfect current mirrors.*

1. *Derive V_{REF} in terms of R_1 R_2, V_T, ζ, and the W/L ratios of the transistors only.*
2. *Discuss how M_3 and M_4 help to stabilize V_{REF} with respect to V_{DD} variations.*
3. *Determine if R_1 has to be CTAT or PTAT in order to achieve a near-zero TC V_{REF}.*
4. *Determine the temperature coefficient of $\frac{R_2}{R_1}$ required to achieve a near-zero TC V_{REF}.*

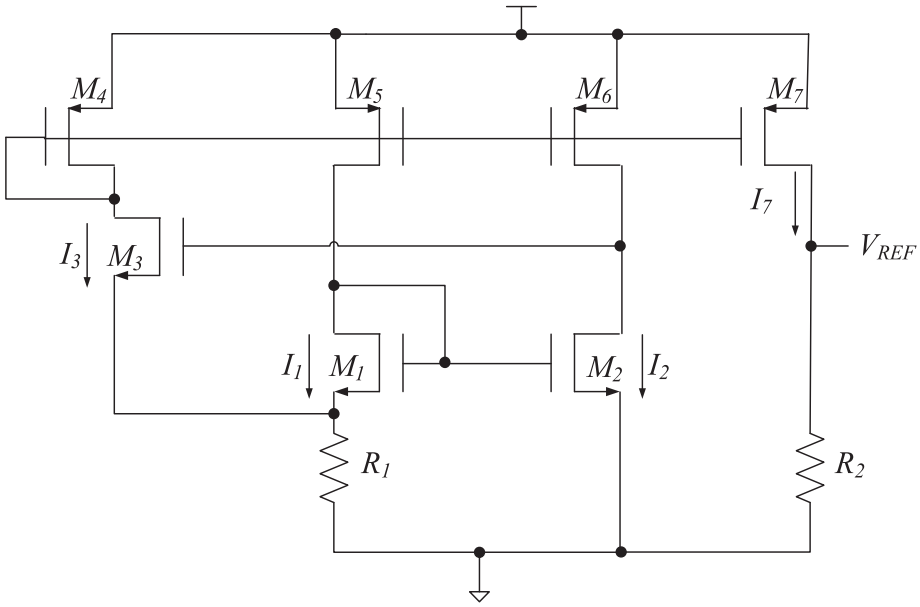


Figure 5.12 Temperature insensitive voltage reference circuit using temperature sensitive resistors R_2, with the PTAT source generated by the schematic in Figure 5.11 and a temperature sensitive resistor R_1 for Exercise 5.8.

Exercise 5.9 *Consider the Kujik voltage reference circuit (Kuijk, 1973) with* $R_1 = R_2$ *in Figure 5.9.*

1. *Derive* V_{REF} *in terms of* V_{BE_2}, V_T, *emitter area ratio N between* Q_2 *and* Q_1, R_2 *and* R_3.
2. *It has been showed in Exercise 5.1 that the opamp gain plays an important role in the stability of the reference voltage. The loop gain in particular is the major factor. Derive the loop gain* β_p *and* β_n *as noted in Figure 5.9 in terms of N, and resistors alone (the resistors are assumed to be selected to achieve near-zero TC at* 300 K*). Discuss the stability of this circuit.*
3. *Using the noise model in Figure 5.13, derive the output noise voltage of the voltage reference circuit.*
4. *Identify the noise amplification effect of the resistors for the computed output noise, and suggest solutions to reduce the noise amplification effect of each resistor.*

Exercise 5.10 *(*V_{th} *extraction circuit) Besides the* V_{GS} *current source,* V_{th} *can be extracted from the schematic shown in Figure 5.14 to form a CTAT current source.*

1. *Derive* V_1, V_2, *and* V_3 *in terms of the threshold voltages* V_{th_1}, V_{th_2}, *and* V_{th_3} *of the transistors* M_1, M_2, *and* M_3 *alone.*
2. *Assume all the threshold voltages are identical and equal* V_{th}, *derive the current* I_b.
3. *Assume the transistor sizes of* $M_1 \sim M_9$ *are the same, derive* V_O.
4. *Perform SPICE simulation of the circuit and find a linear expression of the temperature dependency of the threshold voltage* $V_{th}(T)$ *in the temperature range of* 200 K $\sim$ 400 K.

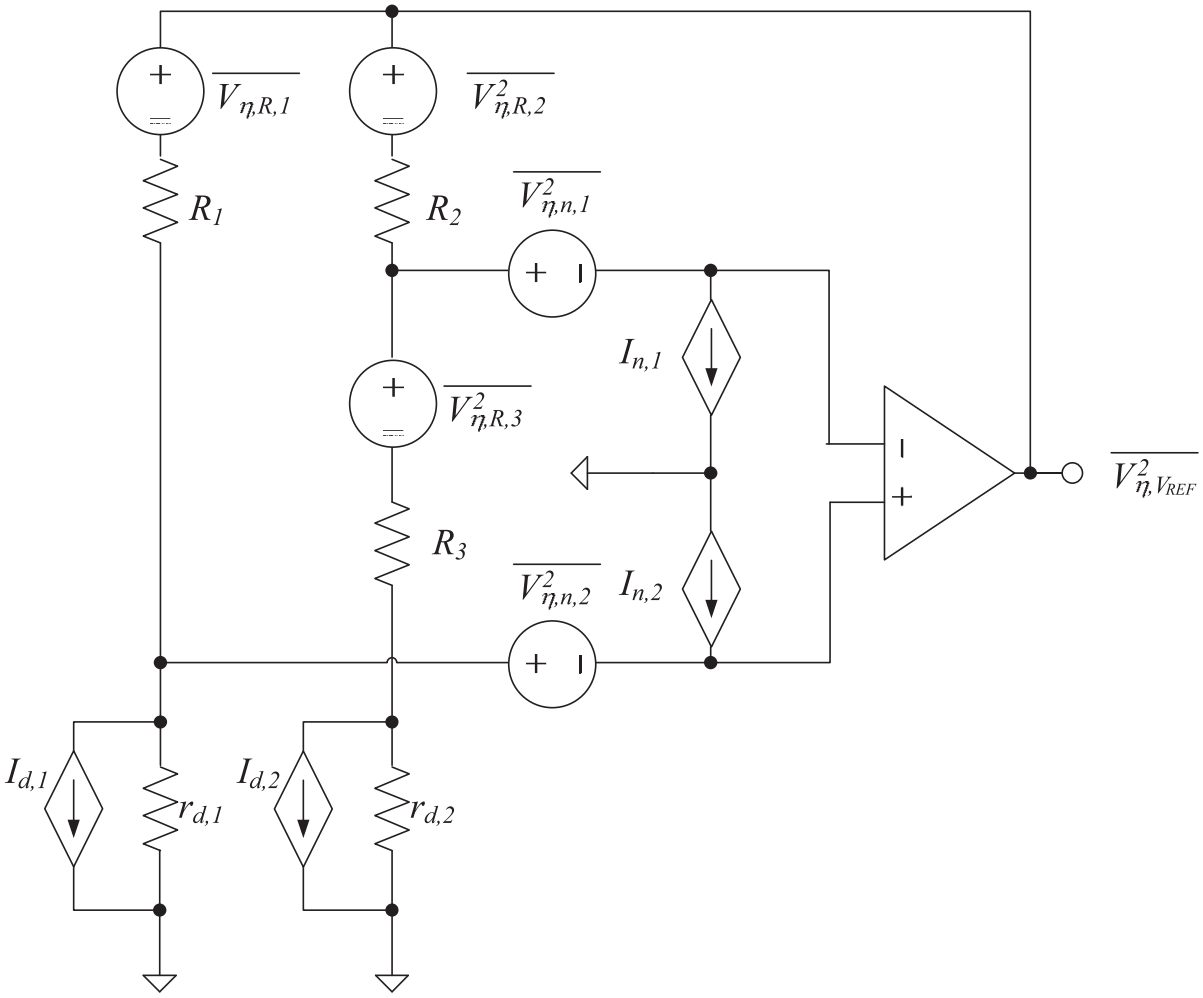


Figure 5.13 Noise model of Kujik voltage reference circuit.

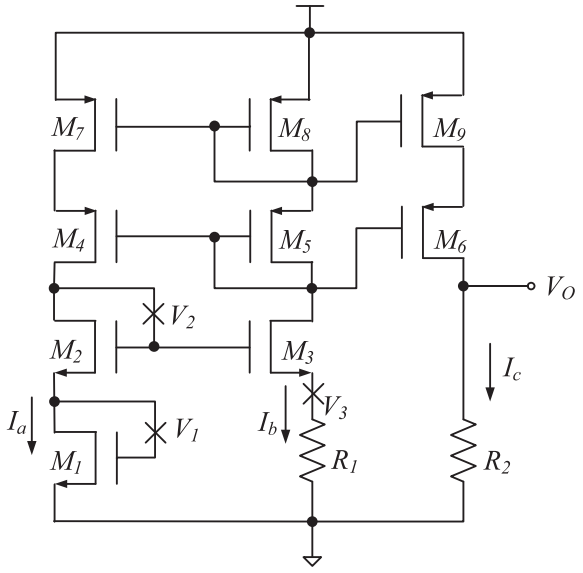


Figure 5.14 V_{th} extraction circuit for Exercise 5.10.

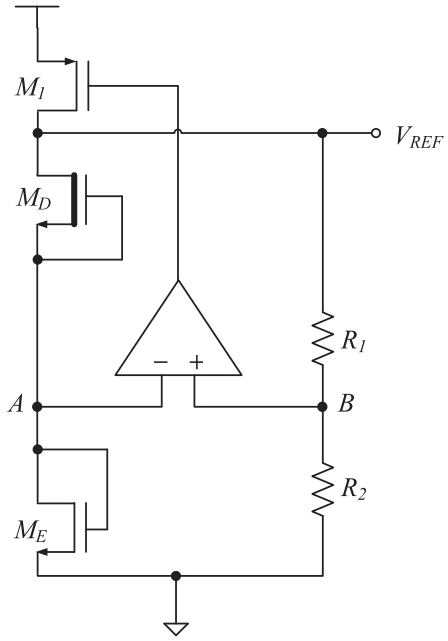


Figure 5.15 (Multi-threshold voltage reference circuit) A voltage reference circuit (modified from (Ugajin, 2002)) that makes use of transistors with different threshold voltages for the analysis in Exercise 5.11.

Exercise 5.11 *(Multi-threshold voltages reference circuit.) Consider the voltage reference circuit in Figure 5.15 (modified from (Ugajin, 2002)), where M_E is an enhancement mode NMOS with $V_{th} > 0$, and M_D is a depletion mode NMOS with $V_{th} < 0$.*

1. *Derive V_B with respect to V_{REF}, R_1 and R_2.*
2. *Derive V_A with respect to V_{REF}, and the characteristics of the transistors M_D and M_E.*
3. *Derive the V_{REF} with respect to R_1, R_2, and V_{th}. Also derive the condition to achieve V_{REF} with near-zero TC .*
4. *What is the major disadvantage of this circuit when generating a reference voltage? The details of such a voltage reference topology will be discussed in Section 7.5.*

References

Brokaw, A.P. (1974) A simple three-terminal IC bandgap reference. *IEEE Journal of Solid-State Circuits*, **9**, 388–93.

Kuijk, K.E. (1973) A precision reference voltage source. *IEEE Journal of Solid-State Circuits*, **SC-8**, 222–26.

Laber, C.A., Rahim, C.F., Dreyer, S.F. *et al.*, (1987) Design considerations for a high-performance 3-μm CMOS analog standard-cell library. *IEEE Journal of Solid-State Circuits*, **22** (2), 181–89.

Lin, H.C. and Huang, P.H. (2006) A simple subthreshold CMOS voltage reference circuit with channel-length modulation compensation. *IEEE Transactions on Circuits and Systems-II:Express Briefs*, **53** (9), 882–85.

SanSen, W.M., Eynda, F.O. and Steyaert, M. (1988) A CMOS temperature compensated current reference. *IEEE Journal of Solid-State Circuits*, **23**, 821–24.

Song, B.S. and Gray, P.R. (1983) A precision curvature-compensated CMOS bandgap voltage reference. *IEEE Journal of Solid-State Circuits*, **18** (6), 634–43.

Tzanateas, G., Salaman, C.A.T. and Tsividis, Y.P. (1979) A CMOS bandgap voltage reference. *IEEE Journal of Solid-State Circuits*, **14** (3), 655–57.

Ugajin, M., Suzuki, K. and Tsukaraha, T. (2002) A 0.6-V supply, voltage-reference circuit based on threshold-voltage-summation architecture in fully-depleted CMOS/SOI. *IEICE Transactions on Electronics*, **E85-C** (8), 1588–95.

Vittoz, E.A. and Neyroud, O. (1979) A low-voltage CMOS bandgap reference. *IEEE Journal of Solid-State Circuits*, **14** (3), 573–79.

Werking, P.M. (2006) Temperature compensated low voltage reference circuit. US Patent No. 7122997.

Widlar, R.J. (1971) New developments in IC voltage regulators. *IEEE Journal of Solid-State Circuits*, **6** (1), 2–7.

6

Sub-1V Voltage Reference Circuit

The trend in integrated circuit fabrication since its inception has been a move towards decreasing geometry size to increase circuit capacity, speed, and to reduce power consumption. As transistor size decreases, the circuit functionality of a given area of substrate increases. Smaller device size also yields lower parasitic capacitance which increases speed and decreases power consumption. At the same time, operating voltage must also be scaled down due to the increased electric field and reduced breakdown voltage caused by the higher doping profile required by small device. Decreased operating voltage facilitates low power consumption which is increasingly important as circuit complexity increases. However, the voltage reference circuit becomes more difficult to design with low supply voltage.

The low operating voltage imposes two design constraints onto the voltage reference circuit. The first constraint is the output of the voltage reference circuit. The output voltage of the voltage reference circuit has to be lower than the supply voltage. The output voltage of most of the conventional bandgap voltage reference circuits discussed in Chapters 3 and 5 is 1.23 V. When the supply voltage is lowered to below 1 V, one wonders how to achieve a reference voltage with magnitude below 1 V. The voltage reference circuit capable of generating a lower output voltage is referred as *sub*-1V *voltage reference circuit*, which literally means the output of the voltage reference circuit is lower than 1 V. Another design constraint is the operating supply voltage. The voltage reference circuit is required to be able to work with a low supply voltage. When the voltage reference circuit can operate at a supply voltage lower than 1 V, it is known as *sub*-1V *supply voltage reference circuit*. Obviously, a sub-1V supply voltage reference circuit can only generate reference voltage that is lower than the supply voltage. As a result, it is also a sub-1V voltage reference circuit. In the literature, there has been an abuse of notation in using "sub-1V voltage reference circuit" for "sub-1V supply voltage reference circuit." Without ambiguity, this book will also abuse the use of the notation "sub-1V." We shall, however, use the notations in their full forms whenever the authors feel it is necessary.

Conventional bandgap voltage reference circuits presented in Chapter 3 and most of the voltage reference circuits presented in Chapter 5 are neither suitable for low voltage applications, nor for generating low reference voltage. The constraint on achieving a sub-1V reference voltage is the bandgap voltage itself. As discussed in Section 3.1 a near-zero *TC* voltage can be generated by properly scaling the PTAT thermal voltage V_T with the weighting factor M, and summing it up with the CTAT base-emitter voltage V_{BE} of the bipolar transistor. The value of the weighting factor M is closely related to the thermal coefficient of V_T (i.e., $\frac{\partial V_T}{\partial T}$)

CMOS Voltage References: An Analytical and Practical Perspective, First Edition. Chi-Wah Kok and Wing-Shan Tam.
 Published 2013 by John Wiley & Sons Singapore Pte. Ltd.

and also the thermal coefficient of V_{BE} (i.e., $\frac{\partial V_{BE}}{\partial T}$). For the CMOS process used in this book, $|\frac{\partial V_T}{\partial T}| = 0.09$ mV/K and $|\frac{\partial V_{BE}}{\partial T}| = 1.39$ mV/K, hence the weighting factor M equals 19.22, which has to be greater than $\frac{1.39}{0.09}$. With $M = 19.22$, the bandgap voltage reference circuit generates a $V_{REF} = 1.23$ V. Intuitively, the reference voltage can be lowered to sub-1V by (i) lowering the weighting factor M through reducing the magnitude difference between the thermal coefficients of the CTAT term and the PTAT term; or (ii) using different thermal devices to lower the induced thermal voltages.

There are a number of methods in the literature that can reduce the magnitude of the PTAT and CTAT terms to obtain a low V_{REF}, such as resistive sub-division (Neuteboom, 1997). There are also a lot of methods presented in the literature to reduce the thermal coefficients of the PTAT and the CTAT terms, such as using depletion transistors (Annema, 1999) and threshold voltage based compensation (Miller and MacEachern, 2006). The resistive sub-division method has been employed in many voltage reference circuits to generate low V_{REF}. This is because such voltage reference circuits can be designed with the standard CMOS process in a similar manner as that of the opamp based β-multiplier bandgap voltage reference circuit. However, these circuits use multiple resistors which will inevitably increase the silicon area of the voltage reference circuit.

Another method to achieve low V_{REF} is the threshold voltage compensation scheme which makes use of the thermal properties of the threshold voltages $V_{th,n}$ and $V_{th,p}$ of MOSFETs with transistors biased in the saturation region. Compact voltage reference circuits can easily be obtained by this technique, which is also robust to process variation. However, due to the channel length modulation effect and supply voltage variation, without special considerations such circuits usually suffer from a degraded $PSRR$ performance. In addition to the reduction of the magnitude of M, we may simply sum up two currents with identical but complementary temperature characteristics to develop a near-zero TC current as will be discussed in Section 7.5. A reference voltage can be obtained by converting this near-zero TC current to voltage using an output resistor (Ripamonti *et al.*, 1999). By adjusting the output resistor value, an adjustable reference voltage can be obtained. In the following sections, we shall review some of the CMOS process compatible techniques in the literature to achieve sub-1V reference voltage, with detailed mathematical derivation and simulation results. We shall also explore some of the possible improvements on different voltage reference circuits to obtain low V_{REF}.

Besides the reference voltage has to be lower than 1 V, as discussed in the previous paragraph, the voltage reference circuits also face the problem of reduced voltage headroom. The minimum operating supply voltage of the conventional opamp based β-multiplier bandgap voltage reference circuit is required to be greater than 1 V (actually 1.7 V) due to two factors. (i) The reference voltage is 1.23 V, which exceeds the 1 V supply voltage (as we have already discussed in the previous paragraph). This can be alleviated by using the voltage sub-division method to scale down the 1.23 V reference voltage, as will be detailed in the first half of this chapter. (ii) The constraint in the design of low voltage PTAT current generation loop where the minimum operating supply voltage is limited by either/both the common collector structure of the BJT's V_{BE} voltage or the input common-mode voltage of the opamp. Note that these limitations are part technology and part circuit topology. They can always be alleviated using MOSFETs with low threshold voltages. However, such solutions are not elegant and are expensive, and they do not actually solve the problem. On the other hand, the solution using

advance circuit topology can enhance the performance of the voltage reference circuit. The drawback is a more complicated circuit, which will consume more power. Advanced CMOS process technology can also be applied in these circuit topologies, which will further push the performance towards a new frontier. As a result, the following sections will concentrate on the advanced circuit topologies that resolve various design problems of the sub-1V voltage reference circuit. We start our discussion by first investigating the possible remedies for the opamp based β-multiplier bandgap voltage reference circuit to generate a sub-1V reference voltage, as it is still the most commonly applied voltage reference circuit. Then we shall move on to discuss other circuit topologies.

6.1 Sub-1V Output Stage

It is simple to obtain a sub-1V output voltage reference circuit by resistive division with the opamp based β-multiplier bandgap voltage reference circuit. However, you should have learnt from Exercise 4.6 that there is a design tradeoff between sub-1V output and higher output noise and lower load regulation problems. Instead, we can modify the output stage as shown in Figure 6.1(a) to lower the reference voltage and avoid the above design tradeoff problems (Pletersek 2005). The transistors M_3 and M_4 in the output stage shown in Figure 6.1(a) are connected to M_2 in Figure 3.4 which will replace M_3, Q_2, and R_2 in Figure 3.4. By doing this, the output of the voltage reference circuit is obtained as a resistive sub-divided V_{BE_3} voltage, and thus the near-zero TC reference voltage of the circuit is lowered. Consider the case where the output stage in Figure 6.1(a) can obtain a reference voltage lower than V_{BE}, that is $V_{REF} < V_{BE}$. As a result, we can assume $V_2 > V_1$, we can observe from the schematic that

$$\begin{aligned} V_1 &= (I_3 + I_{4a})R_2 = V_{REF}, \\ V_2 &= V_{BE_3}, \\ V_2 - V_1 &= I_{4a}R_3 = V_{BE_3} - V_{REF}. \end{aligned}$$

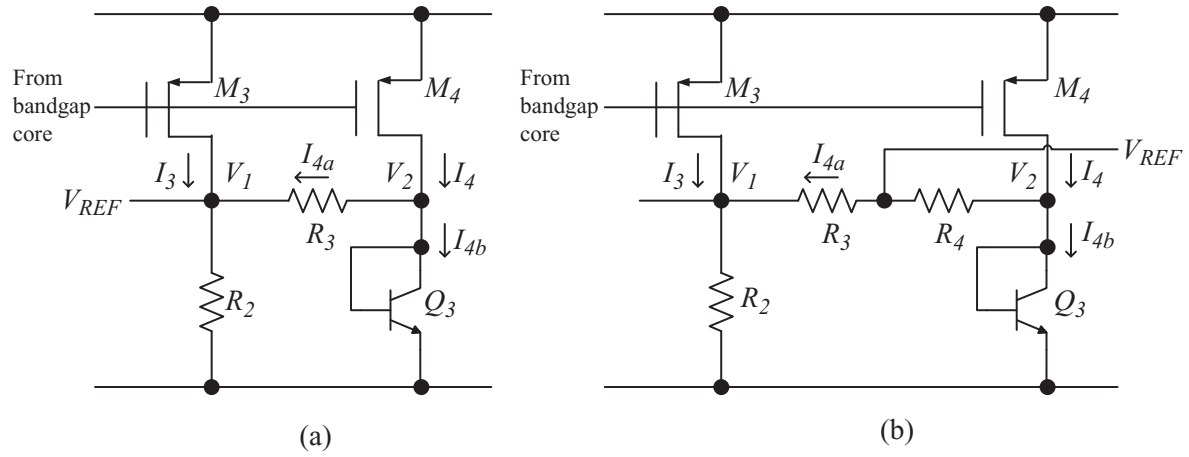


Figure 6.1 Output stages of the opamp based β-multiplier bandgap voltage reference circuit to obtain a sub-1V reference voltage by (a) resistive V_{BE} sub-division (Pletersek, 2005), and (b) modified resistive V_{BE} sub-division to maintain the current density on Q_3 (Doyle *et al.*, 2003).

As a result, we can rewrite I_{4a} in terms of V_{REF} and V_{BE_3} as

$$I_{4a} = \frac{V_{BE_3} - V_{REF}}{R_3}.$$

The output voltage is thus obtained as

$$\begin{aligned} V_{REF} = V_1 &= (I_3 + I_{4a})R_2 \\ &= (R_3 I_3 + V_{BE_3} - V_{REF})\frac{R_2}{R_3} \\ &= \frac{R_2}{R_2 + R_3}\left(\frac{R_3}{R_1}\ln N V_T + V_{BE_3}\right), \end{aligned} \tag{6.1}$$

where we assume $S_4 : S_3 : S_2 = 1 : 1 : 1$. It is clear that V_{REF} obtained from Equation 6.1 has the same form as that given by Equation 3.13 with $M = \frac{R_3}{R_1}\ln N$. As a result, the output stage in Figure 6.1(a) does not affect the performance of the opamp based β-multiplier bandgap voltage reference circuit. Except that the output voltage can be further scaled by the resistor ratio $\frac{R_2}{R_2+R_3}$, and thus can achieve an arbitrary output voltage which verifies our original assumption of $V_{REF} < V_{BE}$, while that of the conventional bandgap voltage reference circuit is 1.23 V. However, this arbitrary output voltage does have a constraint that needs to be satisfied. Consider the case $R_2 = R_3$, then

$$V_{REF} = \frac{1}{2}\left(\frac{R_2}{R_1}\ln N V_T + V_{BE_3}\right). \tag{6.2}$$

which is exactly half of the 1.23 V, that is 0.615 V in theory. In that case, the R_2 that can achieve near-zero TC in Equation 6.2 is given by 82.9 kΩ. Therefore, $I_{4a} = 1.29$ μA, and the current that passes through Q_3 equals $I_{4b} = 4.316$ μA, which is smaller than 5.6 μA in the case of the conventional bandgap voltage reference circuit. The difference in current density will induce a different V_{BE} voltage. Since V_{REF} depends on V_{BE_3}, as a result, it makes it complicated to analyse the output voltage V_{REF} analytically.

To avoid the change in current density on Q_3, and hence be able to properly bias Q_3, the output stage can be modified to the schematic shown in Figure 6.1(b) (Doyle *et al.*, 2003), where an extra resistor network formed by R_3 and R_4 is used to obtain V_{REF}. Again, assuming $V_2 > V_1$, we can observe from the schematic that

$$V_2 = V_{BE_3},$$

$$V_{REF} = I_{4a}(R_3 + R_2) + I_3 R_2, \tag{6.3}$$

$$V_2 - V_{REF} = I_{4a} R_4. \tag{6.4}$$

As a result, we can rewrite I_{4a} in terms of V_{BE_3} and V_{REF}.

$$I_{4a} = \frac{V_{BE_3} - V_{REF}}{R_4}. \tag{6.5}$$

Substitute Equation 6.5 into Equation 6.3 yields

$$\begin{aligned} V_{REF} &= (V_{BE_3} - V_{REF})\frac{R_3 + R_2}{R_4} + I_3 R_2 \\ &= \frac{R_2 + R_3}{R_2 + R_3 + R_4} V_{BE_3} + \frac{R_2 R_4}{R_2 + R_3 + R_4} I_3 \\ &= \left(\frac{R_2 + R_3}{R_2 + R_3 + R_4}\right)\left(V_{BE_3} + \frac{R_2 R_4}{R_1(R_2 + R_3)} \ln N V_T\right). \end{aligned} \tag{6.6}$$

As a result, the reference voltage obtained by the output stage in Figure 6.1(b) has the same form as that of the conventional opamp based β-multiplier bandgap voltage reference circuit in Equation 3.13 with $M = \frac{R_2 R_4}{R_1(R_2+R_3)} \ln N$, except that the output voltage is being scaled by the resistor ratio $\frac{R_2+R_3}{R_2+R_3+R_4}$. Consider the case $R_2 + R_3 = R_4$, then

$$V_{REF} = \frac{1}{2}\left(\frac{R_2}{R_1} \ln N V_T + V_{BE_3}\right),$$

which is exactly half of that derived in Equation 3.12, that is 0.615 V in theory. Note that the benefit of this circuit being I_{BE_3} can be maintained to be the same as long as $R_3 + R_4$ remains constant, while the output V_{REF} can be altered by varying the resistor ratio of R_3 and R_4. In that case, the current density of Q_3 will stay the same for different V_{REF}. The properly biased Q_3 will help to maintain V_{BE_3} and thus improve the stability of V_{REF}.

Last but not least, changing the output stage can obtain a sub-1V output reference voltage. However, there are other constraints on the minimum operating supply voltage of the opamp based β-multiplier bandgap voltage reference circuit. The following sections will discuss those constraints and the possible remedies that alleviate them to obtain a sub-1V supply voltage reference circuit.

6.2 Voltage Headroom in Opamp Based β-multiplier Voltage Reference Circuit

An obvious problem of the conventional opamp based β-multiplier bandgap voltage reference circuit operating at low supply voltage is the voltage headroom. We have defined V_{DROP} in Section 2.1.1, and discussed the possible relationship with the minimum operating supply voltage required to operate the voltage reference circuit. This supply voltage limitation is caused by the minimum operating supply voltage required to maintain the circuit in Figure 6.2 operating in the active region. This simple circuit consists of two NMOS transistors that operate in the active region if and only if the NMOS transistor that connects to V_{DD} can drive the gate of the NMOS transistor that connects to the ground, while remaining in the active region to propagate a bias current. This requires the drain to source voltage of the top NMOS to be greater than $V_{DS,\,sat}$. The gate to source voltage of the lower NMOS must be $V_{th,\,n} + V_{DS,\,sat}$ which pushes the minimum operating supply voltage to be greater than or equal to $V_{th,\,n} + 2V_{DS,\,sat}$.

The above analysis when applied to a conventional NMOS differential pair architecture as shown in Figure 6.3 will yield the worst case headroom of $V_{th} + 2V_{DS,\,sat}$. In other words,

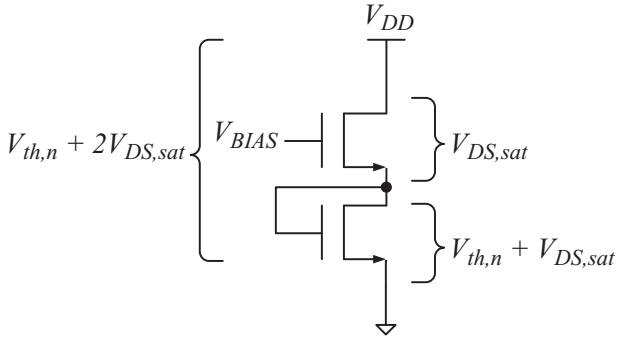


Figure 6.2 Operation of cascode NMOS transistors.

the differential pair requires input biasing at or above $V_{th} + 2V_{DS,\,sat}$, leaving no room for an input signal to achieve a sub-1V circuit design. Similarly, the PMOS differential pair in Figure 6.3 will perform the same. A quantitative analysis of the common mode input range (CMIR) problem of opamp in the conventional opamp based β-multiplier bandgap voltage reference circuit can be obtained by considering Figure 6.4 for opamp with NMOS and PMOS differential input architectures. It can be observed that the structure of the differential circuit poses certain limitations on the operating supply voltage. Figure 6.3 also shows a plot of V_{IN} and V_{DD} that marks the operating region of the operating amplifiers with both P and N channel input stages. This graph is obtained by observing that the minimum operating voltage, $V_{DD(min)}$, is constrained by the CMIR of the differential input stage. Consider applying the V_{IN} and V_{DD} relationship depicted in Figure 6.4 for the P-channel MOSFET differential input stage in Figure 6.3(b), the $V_{DD(min)}$ is given by

$$V_{DD(min)} = V_{BE_1} + |V_{th,p}| + 2V_{SD,sat}, \tag{6.7}$$

where the gate of the differential input transistor is connected to Q_1 with a voltage equal to V_{BE_1}. Referring to the MOSFET parameters listed in Chapter 1, $V_{DD(min)} = 0.73 + 0.47 + 2 \times$

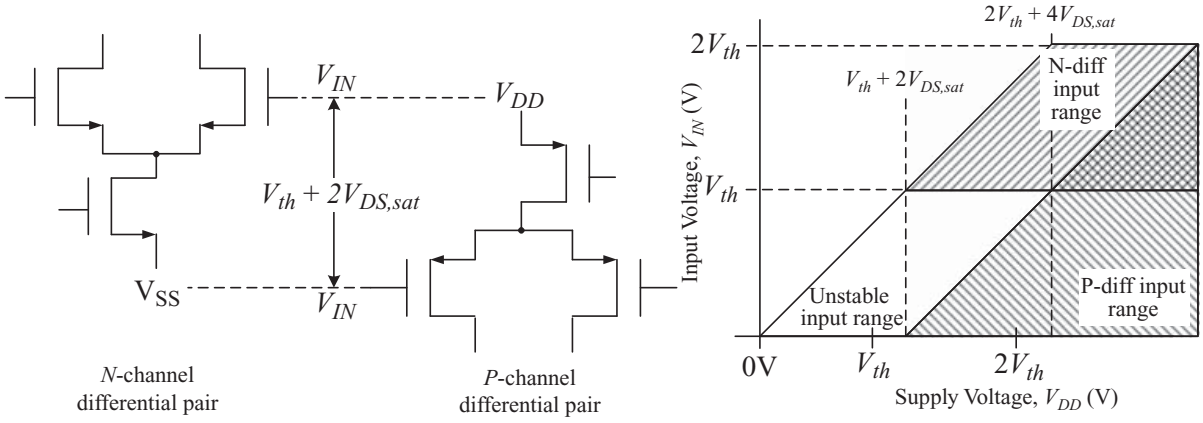


Figure 6.3 The common mode input range (CMIR) limitation of an opamp with N-channel and P-channel MOSFET differential input stage, and the associated operating regions with respect to input voltage and supply voltage.

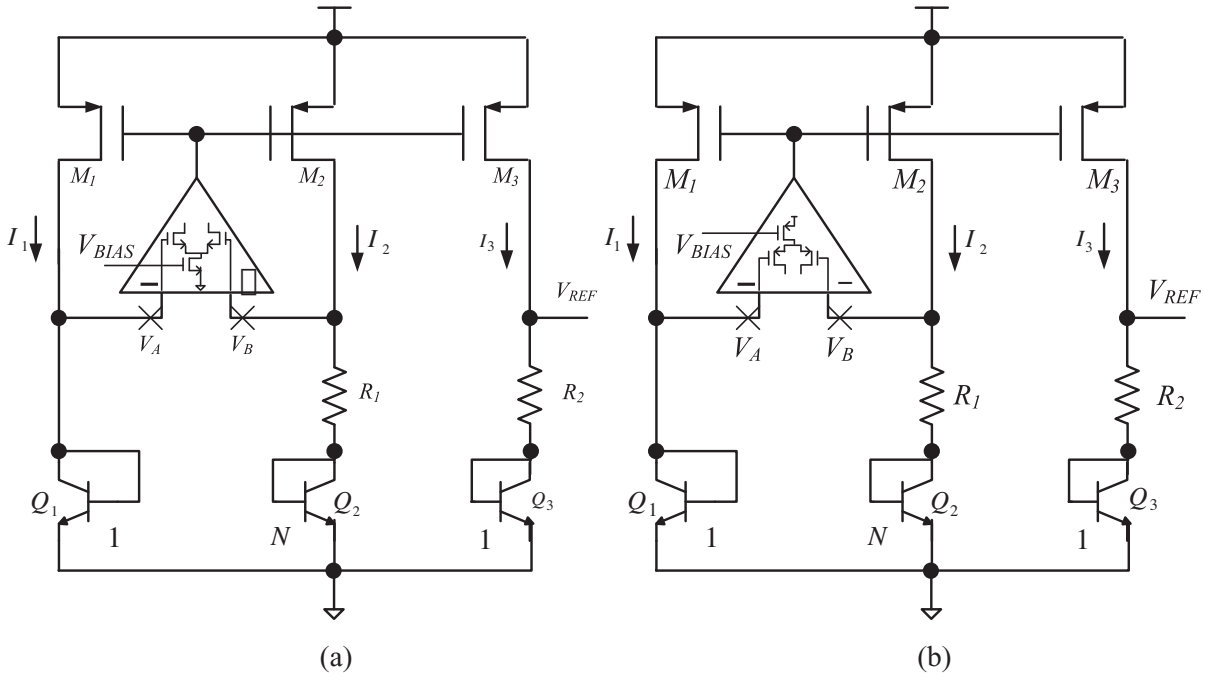


Figure 6.4 Opamp-based β-multiplier bandgap voltage reference circuits using an opamp with (a) N-channel MOSFET differential input stage, and (b) P-channel MOSFET differential input stage.

$(0.1) = 1.4$ V. This explains the minimum operation voltage observed from the simulation results shown in Figure 3.8.

6.2.1 Opamp with NMOS Input Stage

Alternatively, opamp with a N-channel MOSFET differential input stage can be considered to alleviate the constraint on CMIR. Note that the minimum input common-mode voltage $V_{CMIR(min)}$ of an amplifier with NMOS input stage when applied to the opamp based β-multiplier bandgap voltage reference circuit must be less than V_{BE}, that is,

$$V_{CMIR(min)} = V_{th,\,n} + 2V_{DS,\,sat} < V_{BE}. \tag{6.8}$$

To achieve a sub-1V supply voltage reference circuit, $V_{DD(min)} \geq V_{CMIR(min)}$. This implies $V_{th,\,n} < 0.63$ V is required for the voltage reference circuit to work with sub-1V supply voltage (assuming $V_{BE} = 0.73$ V, and $V_{DS,\,sat} = 50$ mV). This is acceptable as NMOS devices with $V_{th,\,n} < 0.63$ V can be easily found in many CMOS processes. However, since both V_{BE} and $V_{th,\,n}$ are CTAT voltages with TC approximately equal to -1.73 mV/K and -0.8 mV/K respectively, and since the magnitude of the TC of V_{BE} is larger than that of $V_{th,\,n}$, when the temperature increases, V_{BE} will decrease faster than $V_{th,\,n}$. As a result, even at low temperatures when $V_{th,\,n} + 2V_{DS,\,sat} < V_{BE}$, it is possible that when the temperature is high, $V_{th,\,n} + 2V_{DS,\,sat} > V_{BE}$. Thus the opamp may not be able to function properly, and may cause malfunctioning of the bandgap voltage reference circuit. In other words, a low minimum input common-mode voltage is being traded for a smaller operational temperature range.

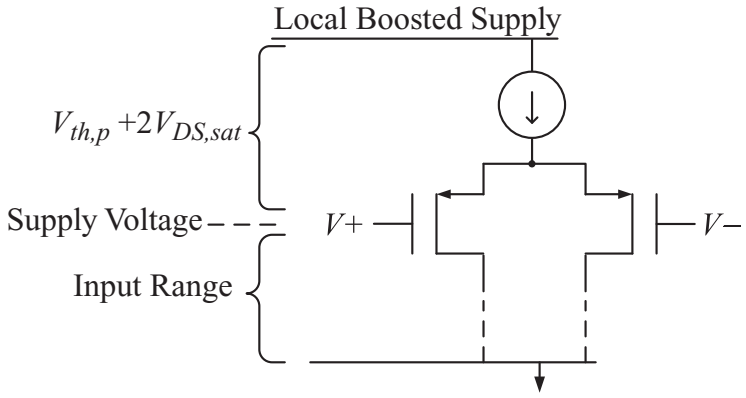


Figure 6.5 Voltage headroom and common mode input range of *P*-channel MOSFET differential input pair with a local boosted supply.

It is clear from the analysis of these two sections that the conventional opamp based β-multiplier bandgap voltage reference circuit cannot operate with low V_{DD} (no matter if the opamp uses PMOS or NMOS input transistor pairs). Even if it operates with low V_{DD} as in the case of the circuit in Figure 6.4(a), it will have poor *TC*. To achieve a bandgap voltage reference circuit that can operate in low supply voltage, the CMIR issue in the opamp has to be overcome. Techniques to achieve rail-to-rail input operation of a differential pair are required to overcome this worst-case condition at low supply voltages. Methods for maximizing the CMIR of the differential pairs include increasing the differential pair supply voltage, V_{th} shifting, input level shifting, and using bulk-driven MOSFET in the input stage etc. In the following, we shall first discuss the pros and cons of the above remedies to the CMIR constraints, and then we shall move forward to discuss a few popular low supply voltage bandgap voltage reference circuits.

6.2.2 *Local Voltage Boosting*

A simple way of overcoming low supply voltage problems is to create a boosted supply voltage for a small portion of the circuitry which is most affected by the reduced supply voltage. This is most appropriate for differential input stages. The input signal may use the entire supply range by increasing the local voltage of a PMOS transistor input pair to $V_{th,\,p} + 2V_{DS,\,sat}$ above the supply voltage as shown in Figure 6.5. While boosting supply voltage for small circuit can be effective, the voltage boost circuitry must be designed to avoid exceeding process breakdown voltage and to minimize added noise, which makes it more complex to design and less efficient. Even when this can be accomplished, lifetime reliability issues may arise due to hot carrier injection when boosting local supplies. The power efficiency is an additional limiting factor for supply boosted circuits.

6.2.3 *Low V_{th} Transistor*

If we bias Q_1 with a very small current, V_{BE_1} can be lowered to 0.6 V. Similarly, if we lower the biasing current of the differential input stage, $V_{SD,sat}$ can be lowered to 0.05 V. In this case,

if $V_{th,p}$ is smaller than 0.3 V, then $V_{DD(min)}$ in Equation 6.7 will be less than 1 V. However, such a low $V_{th,p}$ will cause potential latch up problems. As an alternative, input level shifting techniques, such as bulk-driven transistors, have been considered in the design of voltage reference circuits.

6.2.4 Bulk-Driven Transistors

The ideal solution to the input stage obstacle for the opamp to operate at low supply voltage is to use transistors with low V_{th}. Unfortunately, low V_{th} transistors are not available in most CMOS processes. The V_{th} is the gate to source voltage needed to accumulate enough charge to create the channel depletion region. If the bulk to source voltage is positive, then the depletion region charge will reduce, and thus lower the transistor V_{th}. This change in V_{th} is commonly known as the "body effect."

The bulk-driven threshold voltage reduction technique can produce MOSFET with a low equivalent V_{th} for low voltage circuits. In the case of low supply voltage opamp, an approach to obtain a low voltage differential input stage is to drive the bulk nodes of the input transistors rather than the gates. The bulk-driven input allows a very wide input range which can include the entire supply range at low voltages. Simple analytical analysis of an opamp with bulk-driven NMOS input stage indicates that it is operational with supply voltages as low as $V_{th,\,n} + 2V_{DS,\,sat}$ with the gates connected to ground.

However, the transconductance of a bulk driven transistor is about one tenth that of a gate driven transistor in 0.18 μm process. This is a serious drawback in low voltage design. The bulk driven transistor will also cause input referred noise and offset that are ten times higher than that of a similarly sized gate driven transistor. This will increase the input offset voltage problem of the voltage reference circuits discussed in Section 4.1.1. Furthermore, the total capacitance of the bulk driven node is much higher than the gate capacitance due to the depletion capacitance forms between the substrate, as well as the source, drain, and channel. All the above have made low voltage opamp with bulk-driven transistor input stage not the number one choice for low supply voltage voltage reference circuits.

6.3 Sub-1V Bandgap Voltage Reference by Resistive Division

These are many varieties of modification to the conventional opamp based β-multiplier bandgap voltage reference circuit that serve to lower the minimum operating supply voltage. Figure 6.6 shows a particular modification of the conventional opamp based β-multiplier bandgap voltage reference circuit using *resistive division*. Instead of stacking two thermal complementary voltages, this bandgap voltage reference circuit is a current sum circuit that generates a near-zero *TC* by converting a temperature independent current to the reference voltage through a resistor. Such circuit architecture is first proposed by (Neuteboom *et al.*, 1997), while the schematic shown in Figure 6.6 is a similar but simpler circuit proposed by (Banba *et al.*, 1999). This simple circuit is easy to construct and has almost all the benefits of the conventional opamp based β-multiplier bandgap voltage reference circuit.

The operation of the sub-1V opamp based β-multiplier bandgap voltage reference circuit with resistive division is similar to the conventional opamp based β-multiplier bandgap voltage reference circuit, where an opamp will form an inverted feedback loop to enforce the two input

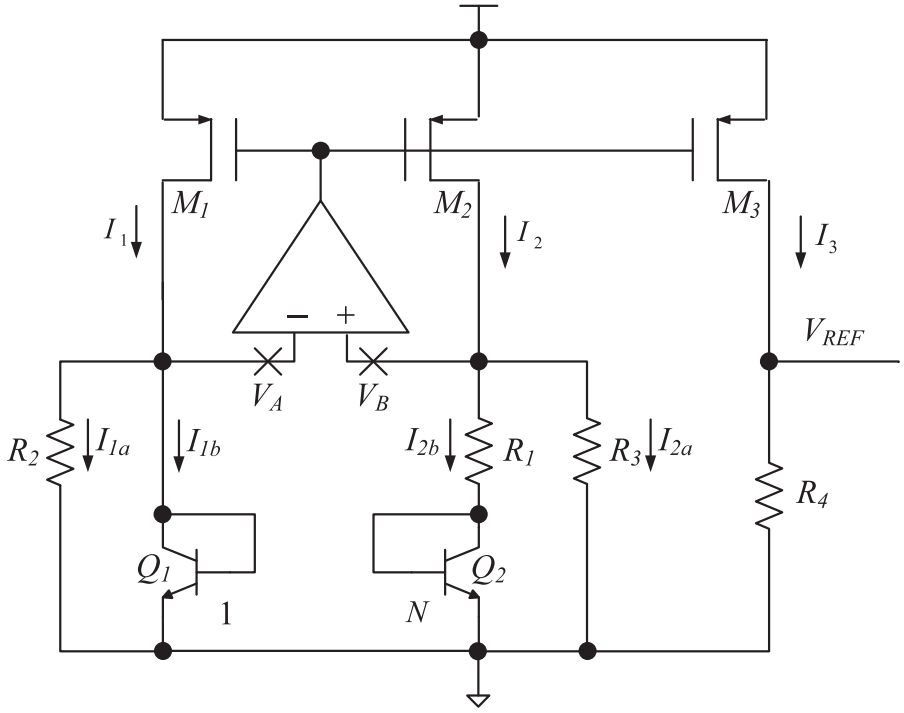


Figure 6.6 Sub-1V β-multiplier bandgap voltage reference circuit using resistive division (variation of (Bana *et al.*, 1999)).

nodes of the opamp having the same voltages. Consider the case of $R_2 = R_3$, such that $I_1 = I_2$, $I_{1a} = I_{2a}$ and $I_{1b} = I_{2b}$. The current $I_2 = I_{2a} + I_{2b}$, where I_{2a} and I_{2b} satisfy the following equations.

$$I_{2a} = \frac{V_B}{R_3} = \frac{V_A}{R_3} = \frac{V_{BE_1}}{R_3},$$
$$I_{2b} = \frac{V_B - V_{BE_2}}{R_1} = \frac{V_{BE_1} - V_{BE_2}}{R_1} = \frac{\Delta V_{BE_{1,2}}}{R_1},$$

with $\Delta V_{BE_{1,2}}$ being the difference in the base-emitter voltages of the two bipolar transistors Q_1 and Q_2, which has the following expression.

$$\Delta V_{BE_{1,2}} = V_{BE_1} - V_{BE_2} = V_T \ln(N),$$

where N is the emitter area ratio between Q_1 and Q_2. The current I_2 is mirrored to form I_3 and therefore the output voltage of the bandgap voltage reference circuit is given by

$$\begin{aligned} V_{REF} &= I_3 R_4 \\ &= (I_{2a} + I_{2b}) R_4 \\ &= \left(\frac{V_{BE_1}}{R_3} + \frac{\Delta V_{BE_{1,2}}}{R_1} \right) R_4 \\ &= \frac{R_4}{R_3} \left(V_{BE_1} + \frac{R_3}{R_1} V_T \ln N \right). \end{aligned} \tag{6.9}$$

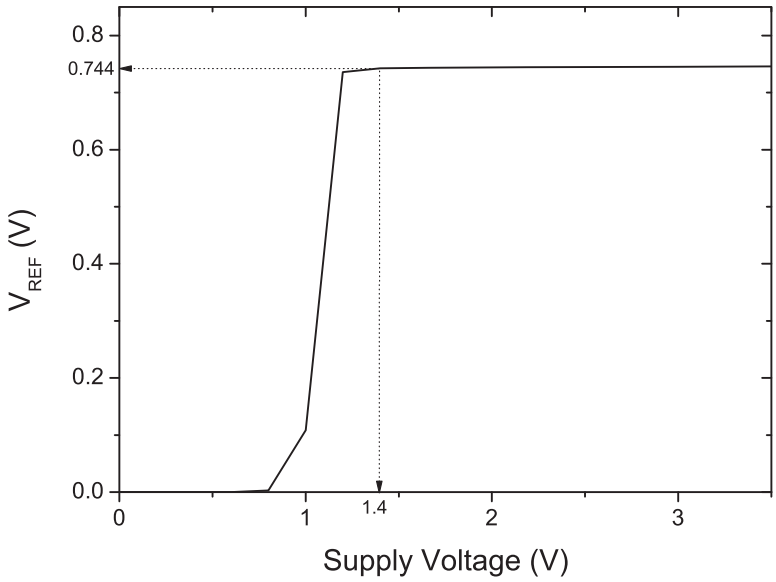


Figure 6.7 SPICE simulated line regulation of the Sub-1V bandgap voltage reference circuit using resistive division.

It can be observed that Equation 6.9 has the same form as Equation 3.12 with $M = \frac{R_3}{R_1}\ln(N)$. As a result, the performance of this voltage reference circuit should be comparable to that of the conventional opamp based β-multiplier bandgap voltage reference circuit, at least in theory. At the same time, we should also notice that the V_{REF} can be scaled by the resistor ratio $\frac{R_4}{R_3}$, and thus achieve an arbitrary V_{REF}. As an example, consider the case of $N = 8$. A near-zero TC reference voltage is obtained when $\frac{R_3}{R_1} = 9.24$. To properly bias the BJT, $I_{1b} = I_{2b}$ are set to be 6 μA. As a result, $R_1 = 8.97$ kΩ, which implies $R_3 = 82.9$ kΩ $= R_2$. The reference voltage of this bandgap voltage reference circuit is thus given by $\frac{R_4}{82.9\ \text{K}}1.23$ V. If we would like to achieve an output voltage exactly equal to 1 V, we must set $R_4 = 67.4$ kΩ. If we would like to further reduce V_{REF} to 744 mV, we must set $R_4 = 50.15$ kΩ. SPICE simulation results of this circuit with V_{REF} designed to be 744 mV at $T_{(nom)}$ is given in Figure 6.7, where the supply voltage varies between $0 \sim 3$ V at $T_{(nom)}$. Figure 6.8 shows the reference voltage variation with temperature variations between $-50 \sim 150$ °C and supply voltage equals to 1.8 V. Note that the output voltage depends on the resistor ratio, instead of a single resistor. Thus with a proper layout to obtain matched resistor pair, the process variation problem of the resistors will have a minimal effect on the reference voltage variation. As observed from Figure 6.7, the minimum operating supply voltage of such a circuit is found to be 1.4 V, which is almost the same as that of the conventional opamp based β-multiplier bandgap voltage reference circuit. This is due to the limitation of the input common mode of the opamp. This limitation makes the sub-1V opamp based β-multiplier bandgap voltage reference circuit with resistive division not applicable for low supply voltage applications. Furthermore, compared with the sub-1V output voltage reference circuit in Section 6.1, both circuits have almost the same power consumption. As a result, this new circuit does not offer better performance than the one in Section 6.1. Moreover, the susceptibility of the bandgap voltage reference circuit to noise increases because of the low output impedance of the bandgap voltage reference circuit, which is basically the output impedance of M_3. Lastly, the transistor M_3 has to be biased in

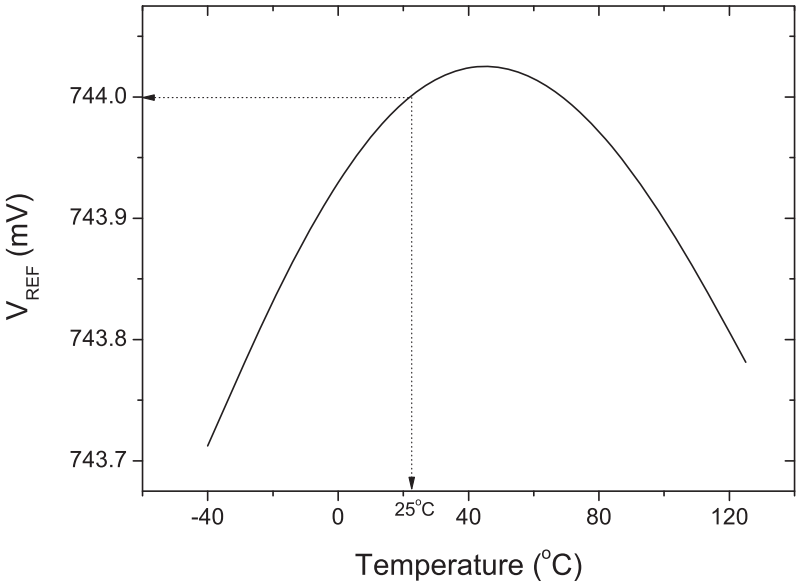


Figure 6.8 SPICE simulated temperature dependency of the Sub-1V bandgap voltage reference circuit using resistive division with $V_{DD} = 1.8$ V.

saturation mode to form a proper current mirror, thus, the resistor value of R_4 will be confined to a certain region of value. Last but not least is the fact that the load regulation of the circuit is very low (refer to Section 4.6) because of the low output impedance of the voltage reference circuit which equals the output impedance of the current mirror.

Nevertheless, the resistive division technique does demonstrate that there are circuit topologies that can alleviate the common mode input voltage constraint of the opamp in the opamp based β-multiplier circuit, and hence inspired a lot of sub-1V opamp based β-multiplier bandgap voltage reference circuit designs. The following sections present modifications to this sub-1V bandgap voltage reference circuit by resistive division, where the input voltage constraint to the opamp is lowered, and thus overcomes the input common mode voltage range problem to achieve sub-1V opamp based β-multiplier bandgap voltage reference circuits.

6.3.1 Resistive Divided V_{BE}

Although the resistor factor $\frac{R_4}{R_3}$ can help to overcome the sub-1V output voltage problem, such that the output voltage can be smaller than 1.23 V, the bandgap voltage reference circuit in Figure 6.6 still cannot work with a sub-1V supply voltage. If a P-channel differential input stage opamp is used, the supply voltage is limited by the input common mode voltage of the opamp. As a result, the input voltage to the opamp has to be low enough to make sure the P-channel input MOSFET pair are operating in the saturation region. Showing in Figure 6.9 is a modified bandgap voltage reference circuit in Figure 6.6 to lower the input voltages to the opamp with the application of resistive voltage divider (Leung and Mok, 2002). Assume $R_{1A} = R_{2A}$ and $R_{1B} = R_{2B}$. When the opamp has large gain, the inverted feedback loop of

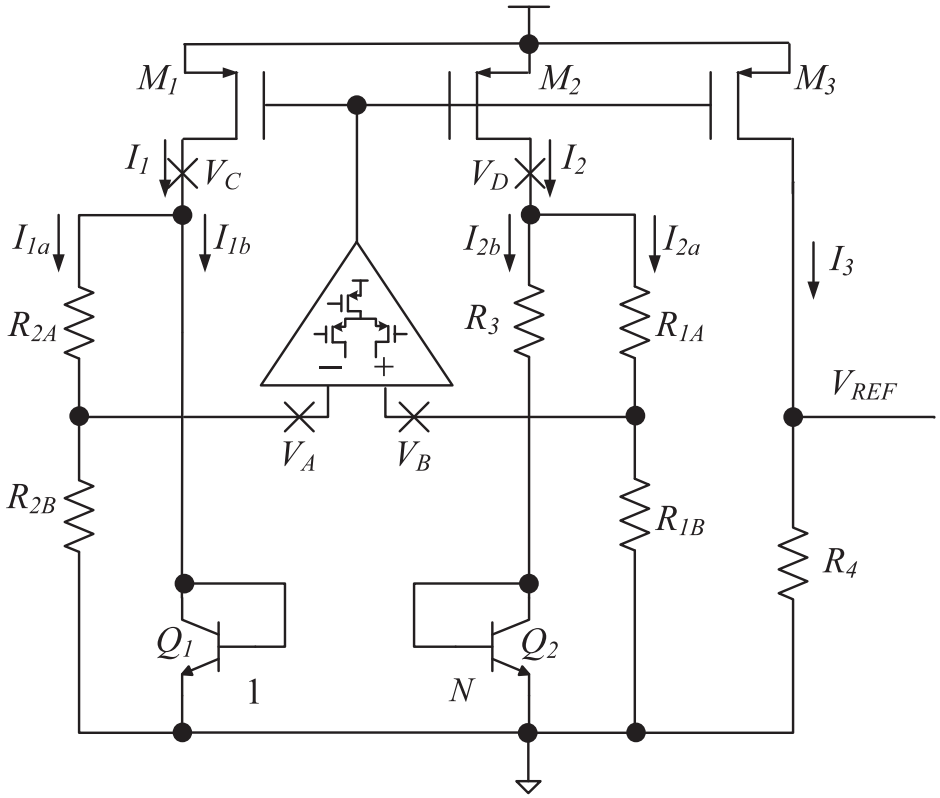


Figure 6.9 Sub-1V bandgap voltage reference circuit by resistive divided V_{BE} (Leung and Mok, 2002).

the amplifier will ensure $V_A = V_B$. As a result, $I_{1a} = I_{2a}$, and thus $V_C = V_D$. Furthermore, the current mirror formed by M_1 and M_2 will ensure $I_1 = I_2$. As a result, $I_{1b} = I_{2b}$. We can thus obtain

$$\begin{aligned} V_D = I_{2b}R_3 + V_{BE_2} &= V_{BE_1} = V_C \\ I_{2b}R_3 &= V_{BE_1} - V_{BE_2} = \Delta V_{BE_{1,2}} \\ I_{2b} &= \frac{1}{R_3}(V_T \ln N). \end{aligned}$$

Let $R_1 = R_{1A} + R_{1B} = R_2 = R_{2A} + R_{2B}$. The current mirror formed by M_1, M_2 and M_3 with $M_1 : M_2 : M_3 = 1 : 1 : 1$ will ensure $I_3 = I_2 = I_{2a} + I_{2b}$, which yields

$$\begin{aligned} V_{REF} &= I_3 R_4 \\ &= (I_{2a} + I_{2b})R_4. \end{aligned}$$

Note that

$$I_{2a} = \frac{V_D}{R_1} = \frac{V_C}{R_1} = \frac{V_{BE_1}}{R_1}.$$

As a result, the reference voltage is given by

$$V_{REF} = \left(\frac{V_{BE_1}}{R_1} + \frac{1}{R_3}(V_T \ln N)\right) R_4 = \frac{R_4}{R_1}\left(V_{BE_1} + \frac{R_1}{R_3} V_T \ln N\right). \tag{6.10}$$

It can be observed that Equation 6.10 has the same form as Equation 3.12 with $M = \frac{R_1}{R_3}\ln(N)$. Therefore, the voltage reference circuit in Figure 6.9 should be able to achieve a similar performance as that of the conventional opamp based β-multiplier bandgap voltage reference circuit. Similarly to Equation 6.9, the reference voltage can be adjusted by the resistor ratio R_4/R_1, while a near-zero TC reference voltage can be achieved by the fine adjustment of the resistor ratio R_1/R_3 such that $M = \frac{R_1}{R_3}\ln(N) = 19.22$. If the opamp input offset voltage is considered,

$$V_{REF} = \frac{R_4}{R_1}\left(V_{BE_1} + \frac{R_1}{R_3}\left(V_T \ln N + \frac{R_1}{R_{1B}} V_{OS}\right)\right). \tag{6.11}$$

It can be observed that the effect of the offset voltage V_{OS} has been amplified by a factor of $\frac{R_1^2}{R_3 R_{1B}}$. In order to minimize the offset voltage amplification effect, we can increase N which will in turn reduce R_1/R_3.

The opamp based β-multiplier structure of this bandgap voltage reference circuit has limited the minimum operating supply voltage to be the input common mode voltage of the opamp, which must be low enough to ensure the P-channel input MOSFET pair are opreating in the saturation region. The improvement of the circuit in Figure 6.9 means it will be able to operate with a low supply voltage, which is based on changing the position of the opamp input transistor pair, and hence the input voltage dynamic range. A feedback loop still exists, and produces a PTAT voltage through the resistor R_3. Meanwhile, the voltage between the supply voltage and the input common mode voltage of the opamp is enlarged by the resistor ratio of R_{1A} over R_{1B} (and R_{2A} over R_{2B}). This will ensure the P-channel MOSFET input pairs are operating in the saturation region even if the supply voltage is under 1 V. The minimum operating supply voltage of this voltage reference circuit is given by Equation 6.8 with the V_{BE} term being replaced by the resistive sub-divided V_{BE} term as

$$V_{DD(min)} = \left(\frac{R_{2B}}{R_2}\right) V_{BE_1} + |V_{th,p}| + 2|V_{DS,\,sat}|. \tag{6.12}$$

As a result, the minimum operating supply voltage of the voltage reference circuit is being lowered by a factor of R_{2B}/R_2 acting on V_{BE_1}.

As an example, consider the case of $N = 8$. A near-zero TC reference voltage is obtained with $\frac{R_1}{R_3} = 9.24$. To properly bias the BJT, $I_{1b} = I_{2b}$ are set to be 6 μA. As a result, $R_3 = 8.97$ kΩ, which implies $R_1 = 82.8$ kΩ $= R_2$. The reference voltage of this circuit is thus given by $\frac{R_4}{82.9\text{ K}}1.23$ V. If we would like to obtain a $V_{REF} = 744$ mV, we shall set $R_4 = 50.15$ kΩ. Furthermore, if we would like the voltage reference circuit to operate at 1V. According to Equation 6.12, we must set $\frac{R_{2B}}{R_2} = 1 - 0.47 - 2 \times 0.1 = 0.33$, which implies

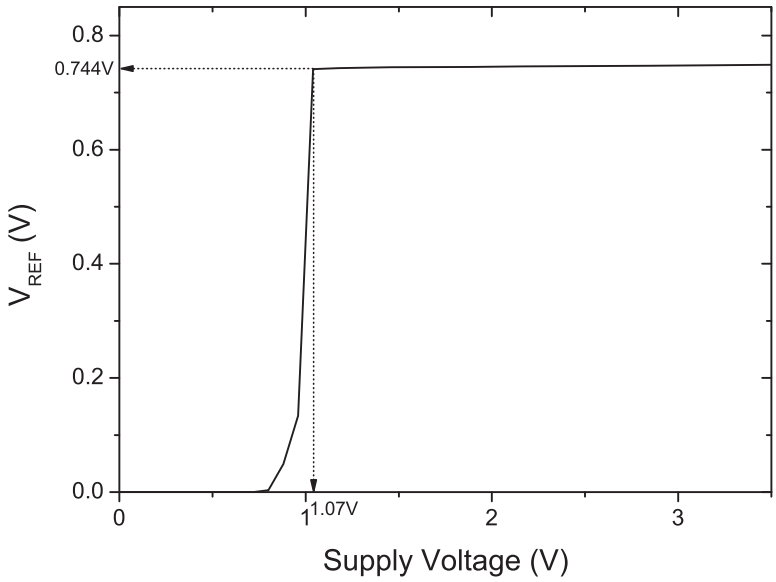


Figure 6.10 SPICE simulated line regulation of the sub-1V bandgap voltage reference circuit by resistive divided V_{BE}.

$R_{2B} = 27.357\ \text{k}\Omega$. The SPICE simulation result of this circuit designed with $V_{REF} = 744$ mV at $T_{(nom)}$ is shown in Figure 6.10, where the supply voltage varies between $0 \sim 3$ V at $T_{(nom)}$. As can be observed from the simulation result, the minimum operating supply voltage of this voltage reference circuit is found to be 1.07 V, which is almost the same as that of the analytical calculated value, and we can *almost conclude* that the circuit has alleviated all the sub-1V voltage reference circuit design problems.

On the other hand, this circuit has a similar β-multiplier circuit structure as the conventional opamp based β-multiplier bandgap voltage reference circuit, where the current mirror transistors are directly connected to the temperature sensitive BJTs. As a result, when the temperature varies from $-20\ ^\circ$C to $100\ ^\circ$C, the V_{BE} voltage of the BJT varies from 812.55 mV to 646 mV, while the bandgap voltage reference circuit output stays almost the same. As a result, the drain to source voltage between M_1, M_2, and M_3 will not be the same, and the transistors in the current mirror will suffer from the channel length modulation effect. Hence the above difference in source to drain voltage will cause the output current differences in the current mirror formed by M_1, M_2, and M_3. Although such current mirror output current mismatch problems exist in all source-to-drain voltage conditions, when V_{DD} is high, V_{SD_ℓ}, with $\ell = 1, 2, 3$, will be large, such that all three transistors are working far away from the linear region. On the other hand, when V_{DD} is low and close to 1 V, M_ℓ will be working close to the linear region. As a result, the I_{SD} current mismatch problem of the current mirror will be severe (Section 4.2). Although the current mirror current mismatch problem can be corrected by using a cascode current mirror, the extra layer of transistors in the cascode current mirror will increase the minimum operating supply voltage. Therefore, cascode current mirror is not applicable to correct the current mirror mismatch problem of the sub-1V voltage reference circuit. In the following section, another modification is presented to alleviate the current mirror mismatch problem by independently biasing the BJTs, instead of directly connecting the MOSFETs of the current mirror in the β-multiplier circuit to the BJTs.

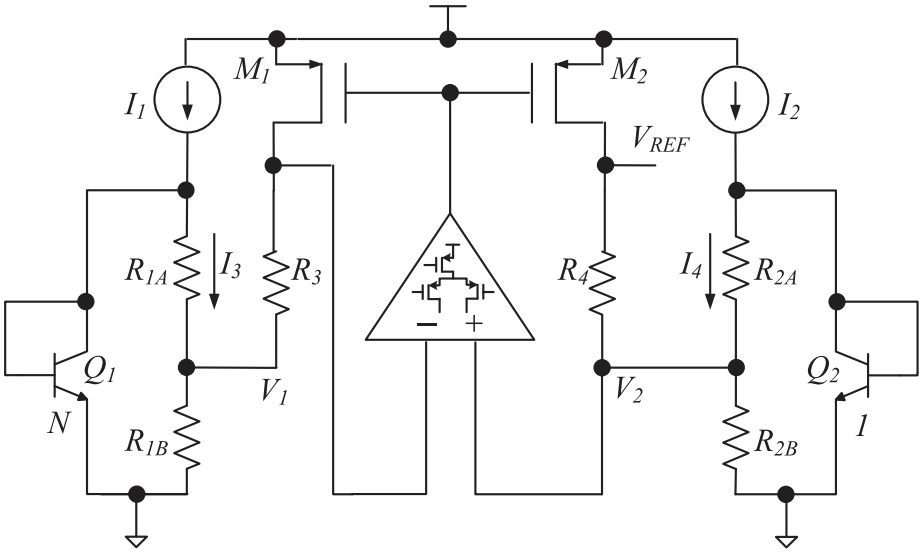


Figure 6.11 Sub-1V bandgap voltage reference circuit by resistive sub-division with independent biasing (Ker *et al.*, 2006).

6.3.2 Independent Biased Resistive Divided V_{BE}

To alleviate the channel length modulation effect that affects the performance of the current mirror, and hence the performance of the overall voltage reference circuit, Figure 6.11 shows a modified schematic of that in Figure 6.9, where the two BJTs are biased independently with two independent current sources instead of the opamp driven current sources. The independent biased resistive divided V_{BE} opamp based β-multiplier bandgap sub-1V voltage reference circuit was first proposed by Ker *et al.* (2006). Similarly to the voltage reference circuit in Section 6.3.1, resistive sub-division is applied to reduce the input voltage to the opamp. Knowing that $V_+ = V_- = V_2$, the KCL at nodes V_1 and V_2 yields the following two equations

$$\frac{V_{BE_1} - V_1}{R_{1A}} + \frac{V_2 - V_1}{R_3} = \frac{V_1}{R_{1B}}, \tag{6.13}$$

$$\frac{V_{BE_2} - V_2}{R_{2A}} + \frac{V_{REF} - V_2}{R_4} = \frac{V_2}{R_{2B}}. \tag{6.14}$$

Consider the case where the transistors M_1 and M_2 have the same size, such that $S_1 = S_2$. Furthermore, $R_{1A} = R_{2A}$ and $R_{1B} = R_{2B}$, then

$$\frac{\Delta V_{2,1}}{R_3} = \frac{V_{REF} - V_2}{R_4}, \tag{6.15}$$

where $\Delta V_{2,1} = V_2 - V_1$. If we subtract Equation 6.14 from 6.13 will obtain

$$\frac{\Delta V_{BE_{1,2}} - \Delta V_{1,2}}{R_{1A}} = \frac{\Delta V_{1,2}}{R_{1B}}$$

$$\Delta V_{1,2} = \frac{\Delta V_{BE_{1,2}} R_{1B}}{R_{1A} + R_{1B}},$$

where $\Delta V_{1,2} = V_1 - V_2$ and $\Delta V_{BE_{1,2}} = V_{BE_1} - V_{BE_2}$. The reference voltage can be rewritten from Equation 6.15 as

$$\begin{aligned} V_{REF} &= \frac{R_4}{R_3}\Delta V_{2,1} + V_2 \\ &= \frac{R_4}{R_3}\frac{R_{1B}}{R_{1A}+R_{1B}}\Delta V_{BE_{2,1}} + \frac{R_{1B}}{R_{1A}+R_{1B}}\left(V_{BE_2} + \frac{R_{1A}}{R_3}\frac{R_{1B}}{R_{1A}+R_{1B}}\Delta V_{BE_{2,1}}\right) \\ &= \frac{R_{1B}}{R_{1A}+R_{1B}}\left[\left(R_4 + \frac{R_{1A}R_{1B}}{R_{1A}+R_{1B}}\right)\frac{\Delta V_{BE_{2,1}}}{R_3} + V_{BE_2}\right]. \end{aligned} \tag{6.16}$$

If the emitter area ratio of the two transistors Q_1 and Q_2 satisfies $A_{E_1} : A_{E_2} = N : 1$, then

$$\Delta V_{BE_{2,1}} = V_{BE_2} - V_{BE_1} = V_T \ln(N).$$

As a result, it can be observed that Equation 6.16 has the same form as Equation 3.12 with

$$M = \left(\frac{R_4}{R_3} + \frac{R_{1A}R_{1B}}{R_3(R_{1A}+R_{1B})}\right)\ln(N),$$

and hence the performance of the above bandgap voltage reference circuit is compatible to that of the conventional opamp based β-multiplier bandgap voltage reference circuit. As an example, consider the case of $N = 8$. A near-zero TC reference voltage can be achieved by selecting $M = 19.22$, which yields $V_{REF} = \frac{R_{1B}}{R_1}1.23$ V. In this case,

$$\frac{R_{1A}}{R_3}\left(\frac{R_{1B}}{R_1}\right) = \frac{19.22}{\ln 8} - \frac{R_4}{R_3}. \tag{6.17}$$

To achieve $V_{REF} = \left(\frac{R_{1B}}{R_1}\right)1.23 \leq 1$, Equation 6.17 will lead to

$$\left(\frac{R_{1B}}{R_1}\right) \leq \frac{1}{1.23}. \tag{6.18}$$

As a result, Equations 6.17 and 6.18 show that by carefully selecting of the resistor values, such that

$$\left(\frac{19.22}{\ln 8} - \frac{R_4}{R_3}\right)\frac{R_3}{R_{1A}} \leq \frac{1}{1.23},$$

will yield a sub-1V opamp based β-multiplier bandgap voltage reference circuit. The minimum operating supply voltage of the above voltage reference circuit is reduced to

$$\begin{aligned} V_{DD(min)} &= V_2 + |V_{th,p}| + 2|V_{DS,\,sat}| \\ &= \frac{R_{1B}}{R_1}\left(V_{BE_2} + \frac{R_{1A}R_{1B}}{R_1}\frac{\Delta V_{BE_{2,1}}}{R_3}\right) + |V_{th,p}| + 2|V_{DS,\,sat}|. \\ &= V_{REF} - \frac{R_4}{R_3}\Delta V_{BE_{2,1}} + |V_{th,p}| + 2|V_{DS,\,sat}|. \end{aligned}$$

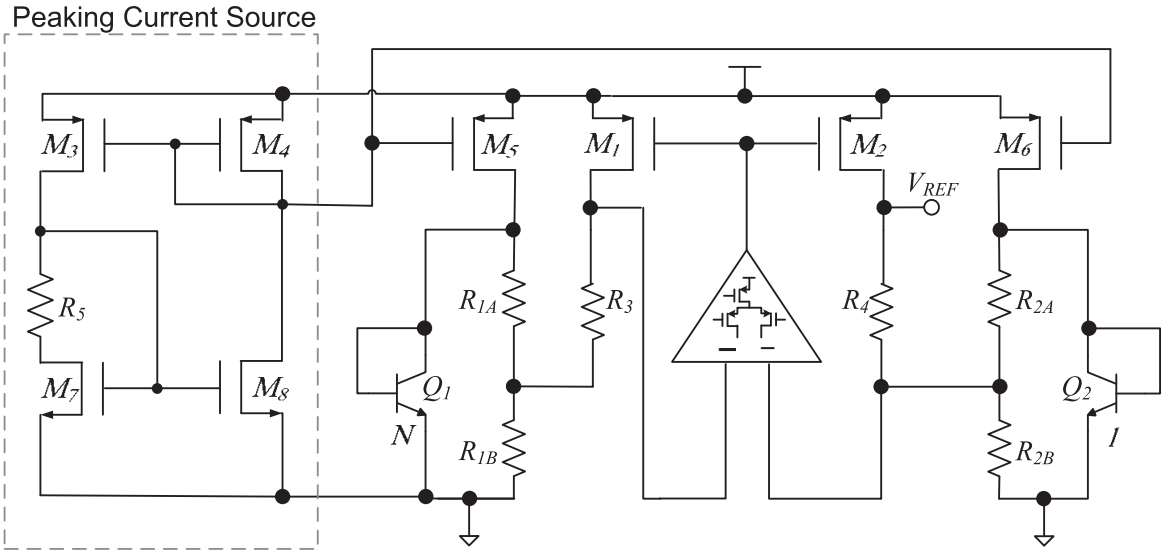


Figure 6.12 Sub-1V opamp based β-multiplier bandgap voltage reference circuit by resistive sub-division with independent biased V_{BE} (Ker *et al.*, 2006) using peaking current source.

Without going into the value of the resistor ratio, we can for sure be able to obtain a sub-1V voltage reference circuit when the reference voltage is less than $1 - |V_{th,p}| - 2|V_{DS,\,sat}|$.

When implementing the circuit, any current source that can operate with sub-1V V_{DD} can be applied. As an example, Figure 6.12 shows the complete schematic of that of Figure 6.11 down to the transistor level using a modified Widlar current source, known as the peaking current source, which will be discussed in a sequel. Note that although the current generated by the peaking current source is PTAT applying it to the sub-1V opamp based β-multiplier bandgap voltage reference circuit by resistive sub-division with independent biased V_{BE} will not affect the performance of the system as long as $I_1 = I_2$, and the two current sources have the same thermal property. This will require the two transistors M_5 and M_6 to satisfy $S_5 = S_6$. In this case, the thermal property of the current sources that biased the two BJTs will be eliminated by the subtraction action between the inversely connected opamp. Again, one of the major sources of reference voltage variation will be the opamp input offset voltage V_{OS}. With the consideration of opamp input offset voltage, the V_{REF} is given by

$$\begin{aligned} V_{REF} &= \frac{R_4}{R_3}(\Delta V_{2,1} - V_{OS}) + V_2 \\ &= \frac{R_{1B}}{R_{1A} + R_{1B}}\left[\left(R_4 + \frac{R_{1A}R_{1B}}{R_{1A} + R_{1B}}\right)\frac{\Delta V_{BE_{2,1}}}{R_3} + V_{BE_2}\right] - \frac{R_4}{R_3}V_{OS}. \end{aligned}$$

It is clear that the offset voltage effect on V_{REF} can be reduced by reducing the resistor ratio $\frac{R_4}{R_3}$. The reduced V_{REF} due to a reduced $\frac{R_4}{R_3}$ can be compensated by an increased $\Delta V_{BE_{2,1}}$, which can be achieved by enlarging the emitter area ratio N between Q_1 and Q_2. The cost is the large silicon size of the resulting bandgap voltage reference circuit.

Nevertheless, all resistive division voltage reference circuits require resistors with large resistance to scale down the reference voltage, and to suppress the noise induced by opamp. The use of resistors with large resistance causes the resistive division voltage reference circuit to suffer from the problems of large silicon area and high sensitivity to process variation. If

special layout techniques are applied to alleviate the process variation problem of the resistors, it will further increase the silicon area due to the large number of resistors in the circuit. Furthermore, almost all the resistors are inter-related, and thus matched layouts are required. The matched layout will further increase the required silicon area. The production cost of this kind of bandgap voltage reference circuit is high, which prohibits their implementation in many real world applications. Moreover, all the above topologies that use opamp and a current mirror will introduce various noise factors (as discussed in Chapter 4) to the voltage reference circuit. Nevertheless, the design of a power efficient opamp that operates with a sub-1V power supply is itself a difficult task. While the design of such a low supply operable opamp is outside the scope of this book, readers can expect that the low voltage opamps are both expensive to implement, and the implementation results are far from ideal. Readers are advised to refer to other opamp design textbooks on this topic.

6.4 Peaking Current Source and V_{BE} Compensation

Similar to the self-biasing voltage reference circuit discussed in Chapter 5, the Widlar current source and V_{BE} compensation topology discussed in Section 5.2 have been shown to be able to achieve low *TC* reference voltage. However, the PMOS M_3 in Figure 5.6 will suffer from the channel length modulation effect. The method presented in Section 5.1.2.2 can be used to alleviate the channel length modulation effect of the Widlar current source, and we have left that as an exercise (Exercise 5.5.6) for the reader to deduce the voltages and currents of the working circuit in Figure 5.11. In this section, we shall present another variant of the Widlar current source for low V_{DD} operation. The sub-1V supply voltage problem can be alleviated by using the peaking current source (Kerns, 1986) as shown in the dotted box of Figure 6.13. The peaking current source was first introduced by (Kwok, 1985) using bipolar technology. The CMOS version of the peaking current source is similar to Widlar current source. They both make use of the ΔV_{GS} of two NMOS transistors M_1 and M_2 with different width to length ratios working in the subthreshold region to generate a PTAT voltage. This PTAT voltage is converted to current by a resistor. By placing this resistor between M_1 and M_3, the channel length modulation effect of M_3 is alleviated.

The transistors M_1, M_2 and resistor R_1 form the peaking current source. The transistors M_3 and M_4 are connected to form a current mirror, and serve as β-multiplier to realize the function of self-biasing for the transistor M_1 and M_2. The transistors M_3 and M_4 are designed to make the drain currents of M_1 and M_2 functionally related by a peaked curve, then the voltage across R_1 will be a PTAT voltage. The gate-source voltage difference of the PTAT current source circuit in Figure 6.13 is given by

$$I_{DS_1} R_1 = V_{GS_1} - V_{GS_2}. \tag{6.19}$$

Making use of the relationship between the subthreshold I_{DS} and V_{DS} in Equation 1.18, we shall obtain

$$I_{DS_1} = S_1 \hat{I}_0 \exp\left(\frac{V_{GS_1}}{\zeta V_T}\right),$$
$$I_{DS_2} = S_2 \hat{I}_0 \exp\left(\frac{V_{GS_2}}{\zeta V_T}\right).$$

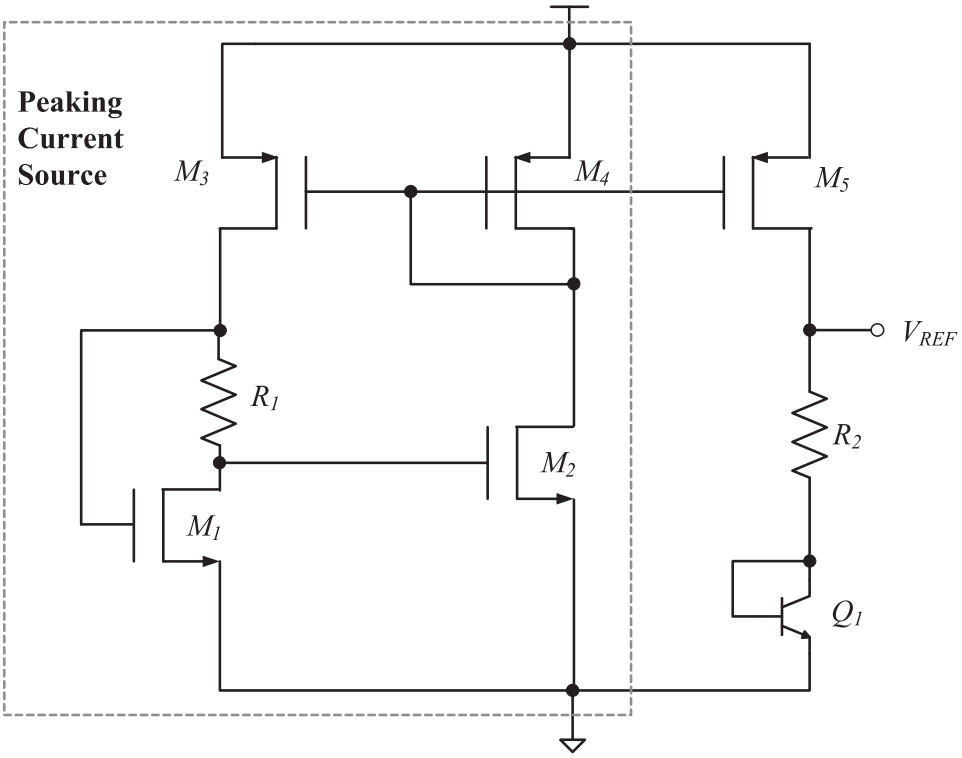


Figure 6.13 Schematic of peaking current source (inside the dotted box) (Kerns, 1986), and the associated bandgap voltage reference circuit.

Thus

$$I_{DS_1} = I_{DS_2} \frac{S_2}{S_1} \exp\left(\frac{V_{GS_2} - V_{GS_1}}{\zeta V_T}\right). \tag{6.20}$$

Substituting Equation 6.19 into Equation 6.20 yields

$$I_{DS_1} = I_{DS_2} \frac{S_2}{S_1} \exp\left(\frac{-I_{DS_1} R_1}{\zeta V_T}\right). \tag{6.21}$$

The peaking circuit is designed to obtain I_{DS_2} is at its peaking value. It can be achieved by zeroing $\frac{\partial I_{DS_2}}{\partial I_{DS_1}}$ using Equation 6.21, yielding the design condition to maintain the current peaking, which is given by

$$I_{DS_1} R_1 = \zeta V_T. \tag{6.22}$$

If Equation 6.22 is satisfied, then the drain currents of M_1 and M_2 given by Equation 6.21 are related by

$$I_{DS_1} = I_{DS_2} \frac{S_2}{S_1} e^{-1}. \tag{6.23}$$

On the other hand, the current mirror formed by M_3 and M_4 with $S_3 = S_4$ will ensure the two currents $I_{DS_1} = I_{DS_2}$, and thus Equation 6.23 will provide us the transistor size ratio of M_1 and M_2 to achieve peaking as $S_2/S_1 = e$. The current I_{DS_1} that passes through R_1 under the peaking condition is given by Equation 6.22, which is proportional to V_T, that is, PTAT. It can be observed that the peaking current source is easy to design, simple to realize, and can meet both the low power and low voltage requirements.

Figure 6.13 shows an example of the peaking current voltage reference circuit. The PTAT current generated by the peaking current source formed by $M_1 \sim M_4$ and R_1 is copied by the current mirror formed by M_2 and M_5. This PTAT current is converted to a PTAT voltage through R_2 and summed with a CTAT voltage V_{BE_1} to generate a near-zero TC reference voltage. The output voltage of the circuit in Figure 6.13 is given by

$$\begin{aligned} V_{REF} = I_{DS_5} R_2 + V_{BE_1} &= \frac{S_5}{S_3} I_{DS_1} R_2 + V_{BE_1} \\ &= \frac{S_5}{S_3} \frac{R_2}{R_1} \zeta V_T + V_{BE_1}. \end{aligned} \tag{6.24}$$

Compared to the conventional bandgap voltage reference circuit in Equation 3.12, it can be observed that Equation 6.24 resembles the same form with $M = \frac{S_5}{S_3} \frac{R_2}{R_1} \zeta$. Hence at least in theory, the reference voltage generated by the schematic in Figure 6.13 will have the same performance as that of the conventional opamp based β-multiplier bandgap voltage reference circuit. It is, however, a different CTAT source that is required to be applied together with the peaking current source to create a sub-1V voltage reference circuit.

6.5 Weighted ΔV_{GS} Compensation

Another device property that can be considered in the design of the voltage reference circuit is the threshold voltage of a MOSFET. Section 5.3 has shown that the thermal property of the MOSFET threshold voltage can be used to generate a near-zero TC reference voltage. As discussed in Section 1.2.5.1, the CTAT thermal property of the MOSFET threshold voltage can be extracted by a weighted V_{GS} circuit. The schematic in Figure 6.14 shows a particular implementation of the sub-1V voltage reference circuit using the weighted ΔV_{GS} circuit topology which was first presented in (Leung and Mok, 2003). The circuit consists of a low voltage peaking PTAT current source formed by $M_1 \sim M_4$ and R_1. This PTAT current is mirrored by M_5 to bias the core of the voltage reference circuit, where I_5 is derived in Equation 6.22 as

$$I_5 = \frac{S_5}{S_3} \frac{\zeta V_T}{R_1}. \tag{6.25}$$

This current will bias the core of the voltage reference circuit, which is formed by M_6, M_7, R_2, and R_3, with M_6 and M_7 being PMOS and NMOS transistors respectively. It is valid to assume the currents passing through R_2 and R_3 to be the same. As a result, the source voltage of M_6 will equal to a scaled voltage V_{GS_7} through the resistive voltage divider formed by

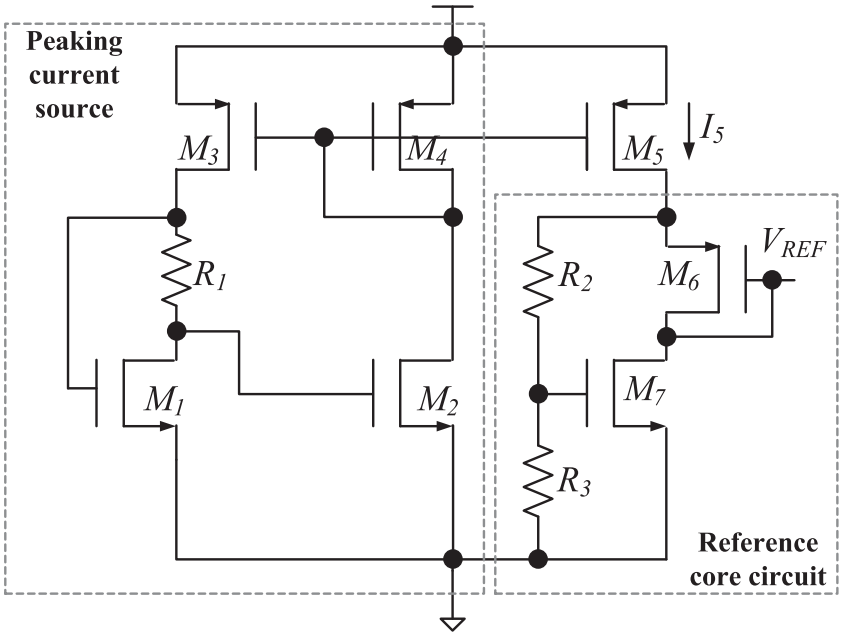


Figure 6.14 Peak current source biased V_{GS} voltage compensation voltage reference circuit (Leung and Mok, 2003).

R_2 and R_3. Finally, the reference voltage is obtained by subtracting V_{GS_6} from a weighted V_{GS_7} as

$$V_{REF} = \left(1 + \frac{R_2}{R_3}\right) V_{GS_7} - |V_{GS_6}|. \tag{6.26}$$

If M_6 and M_7 are operating in the saturation region, Section 5.3 suggests that Equation 6.26 will extract the ΔV_{th} of M_6 and M_7 and form V_{REF}. To investigate how to generate a near-zero TC reference voltage, we shall expand Equation 6.26 as

$$\begin{aligned} V_{REF} &= A_1 V_{GS_7} - |V_{GS_6}| \\ &= A_1 V_{th,n} - V_{th,p} + A_1 \sqrt{\frac{2I_5}{\mu_n C_{ox,n} S_7}} - \sqrt{\frac{2I_5}{\mu_p C_{ox,p} S_6}}, \\ &= V_{t1} + V_{t2}, \end{aligned}$$

where $A_1 = \left(1 + \frac{R_2}{R_3}\right)$, and V_{t1} is the part with the threshold voltages, while V_{t2} is the part with the mobilities. Let's first consider V_{t1},

$$\begin{aligned} V_{t1} &= A_1 V_{th,n} - V_{th,p} \\ &= A_1 V_{th,n}(T_r) - A_1 \beta_{th,n}(T - T_r) - |V_{th,p}(T_r)| + \beta_{th,p}(T - T_r). \end{aligned}$$

It is clear that V_{t1} is temperature independent if

$$A_1\beta_{th,n} - \beta_{th,p} = 0$$
$$A_1 = \frac{\beta_{th,p}}{\beta_{th,n}} \tag{6.27}$$

$$\frac{R_2}{R_3} = \frac{\beta_{th,p}}{\beta_{th,n}} - 1. \tag{6.28}$$

The above simple relationship established the condition on the resistor ratio R_2/R_3 to achieve a near-zero *TC* reference voltage. Now let's consider V_{t2}, the part with the mobilities.

$$V_{t2} = \sqrt{2I_3}\left(\frac{A_1}{\sqrt{\mu_n C_{ox,n} S_7}} - \frac{1}{\sqrt{\mu_p C_{ox,p} S_6}}\right)$$
$$= \sqrt{2I_3}\left(\frac{A_1}{\sqrt{\mu_n(T_r)\left(\frac{T}{T_r}\right)^{-\beta_{\mu_n}} C_{ox,n} S_7}} - \frac{1}{\sqrt{\mu_p(T_r)\left(\frac{T}{T_r}\right)^{-\beta_{\mu_p}}}} C_{ox,p} S_6\right).$$

It is clear that V_{t2} is temperature independent if

$$A_1^2 \mu_p(T_r)\left(\frac{T}{T_r}\right)^{-\beta_{th,p}} C_{ox,p} S_6 = \mu_n(T_r)\left(\frac{T}{T_r}\right)^{-\beta_{th,n}} C_{ox,n} S_7$$
$$\frac{S_7}{S_6} = A_1^2 \frac{\mu_p(T_{(nom)})}{\mu_n(T_{(nom)})}\left(\frac{T}{T_{(nom)}}\right)^{\beta_{mun} - \beta_{\mu_p}} \frac{C_{ox,p}}{C_{ox,n}},$$

where $T_r = T_{(nom)}$. Substituting A_1 from Equation 6.27 will yield the transistor size ratio for M_6 and M_7 to achieve a near-zero *TC* reference voltage. With appropriate selection of the component values, the reference voltage at $T_{(nom)}$ is given by

$$V_{REF}(T_{(nom)}) = \left(1 + \frac{R_2}{R_3}\right) V_{th,n}(T_{(nom)}) - |V_{th,p}(T_{(nom)})|, \tag{6.29}$$

and this near-zero *TC* temperature at $T_{(nom)}$ can be easily achieved by adjusting the resistor ratio $\frac{R_2}{R_3}$ to satisfy Equation 6.28. Note that the above derivation also reveals that theoretically this weighted V_{GS} voltage reference circuit is independent with the biasing current I_3 as V_{REF} in Equation 6.29 does not contain any terms that are related to I_3. The I_3 is therefore only required to be large enough to bias the MOSFETs M_6 and M_7 to work in the saturation region. To improve the power-supply rejection ratio, all the transistors should have long channel lengths to avoid channel length modulation. This circuit is simple and compatible with low supply voltage operation. Since the temperature dependency of the threshold voltage is not perfectly linear, and a complete cancellation of the temperature dependency of μ_p and μ_n is not possible in a wide temperature range, a nonlinear temperature-dependent error is

observed in the reference voltage. Last but not least, this voltage reference circuit requires both M_6 and M_7 to work in saturation mode. This implies a minimum operating supply voltage must be maintained in order to prevent the current source M_5 from being forced to operate in the triode region. Therefore V_{DD} must be larger than $\left(1+\frac{R_2}{R_3}\right)V_{GS,sat,n}+V_{SD,sat,p}$ or $V_{REF}+V_{th,p}+V_{SD,sat,p}$, which is about 650 mV in the process considered in this book.

There is another problem associated with the assumption that the current passing through R_2 and R_3 is the same. To reduce the power consumption of the voltage reference circuit, R_2 and R_3 are chosen to have magnitude of 1 MΩ which is comparable to the gate oxide resistivity. As a result, the finite gate to substrate resistance will result in almost 10% difference between the computed and the actual V_{REF} when I_{G_7} is not considered. On the other hand, when R_2 and R_3 have small resistances, a large portion of the current I_5 will pass through R_2 and R_3, leaving not enough current to bias the two transistors M_6 and M_7 to work in saturation mode or an increased power consumption of the voltage reference circuit. As a result, the transistor size of M_5, M_6, and M_7, and the resistance of R_2 and R_3 have to be designed with great care.

Finally, the authors would like to point out that this weighted ΔV_{GS} compensation voltage reference circuit topology is a particular implementation of the multi-threshold voltage curvature compensated voltage reference circuit, which will be discussed in detail in Section 7.5.3.

6.6 Summary

This chapter has discussed various sub-1V voltage reference circuits and topologies. Perhaps the most restrictive obstacle for the sub-1V voltage reference circuit design is the MOSFET threshold voltage. The V_{th} will affect the performance of the sub-1V voltage reference circuit. Section 6.2 has considered the P-channel MOSFET differential input stage of the opamp alone. The V_{th} represents a headroom requirement which is roughly 70% of the target $V_{th}+2V_{DS,\,sat}$ supply voltage. To bias any transistor in the active region, $V_{th}+V_{DS,\,sat}$ is required which approaches 85% of the target supply. If an N-channel MOSFET differential input stage is being considered, the headroom will increase to $V_{th}+2V_{DS,\,sat}$. Such a differential input stage will require an input biasing at or above $\max(V_{th}, 2V_{DS,\,sat})$ leaving no room for an input signal at the target supply voltage. Techniques for allowing rail-to-rail input operation of a differential pair have been considered to be the solution for the V_{th} limitation at low supply voltages. The ideal solution to the V_{th} obstacle is a depletion mode transistor, an N-channel transistor with a negative V_{th}, or P-channel transistor with a positive V_{th}. Unfortunately, depletion mode transistors are not available in most advanced CMOS processes. On the other hand, the threshold voltage of the enhancement mode transistor depends on process parameters such as oxide thickness, gate material, and doping levels, which cannot be altered easily. As a result, the effective V_{th} reduction in the standard process is limited to the use of floating-gate structures or bulk voltage induced threshold voltage lowering.

Both floating-gate and bulk-driven techniques can be used to mimic the operation of depletion mode transistors. At the same time, both techniques are standard MOSFET compatible. However, the floating-gate transistor is implemented with an unconnected or "floating" gate in parallel with a control gate, which will induce an extra masking step, and hence increase the fabrication cost. As a result, the application of bulk-driven input design technique seems very attractive. Consider the case of bulk-driven input architecture for the design of a low

voltage opamp. The advantage of such a design technique is that it can achieve near rail-to-rail operation, and hence has almost no head room problem. It is the case, however, that such an opamp suffers from low transconductance and increased input referred noise, offset, and large input capacitance (Blalock *et al.*, 1998). As a result, one is not encouraged to design voltage reference circuits using bulk-driven low voltage design techniques. Instead, traditional analog circuit design techniques are applied with the exception that most of the MOSFETs are biased to work in the subthreshold region.

On the other hand, unlike the requirement of process corners robustness for the design of accurate bandgap voltage reference circuits, the problem of designing voltage reference circuits with MOSFETs in the subthreshold is the process corner variation of the threshold voltages. The threshold voltage variation may result in a significant reference voltage variation of up to $\pm 15\%$ in the worst process corner. This inaccuracy may make it difficult to apply in many circuits. To overcome this problem, better compensation and post-processing trimming have to be applied, which can help to reduce the variation to $\pm 0.7\%$ or lower in the worst process corner in most of the practical sub-1V voltage reference circuit. Even though more components are required, the quality and post-processing cost of the final voltage reference circuit can approach that of the conventional opamp based β-multiplier bandgap voltage reference circuit. Most important, such a voltage reference circuit designed with traditional analog technique can still keep working even if the threshold voltage get lowered in the future, while process driven technique designed circuits will fail or will require a complete redesign whenever a more advanced process is applied.

Without a special CMOS process, the thermal voltages of the electron devices, such as V_{th} and V_{BE}, etc., will be large, which makes it difficult to implement a sub-1V voltage reference circuit. As a result, thermal voltage reduction techniques are required to make the implementation of sub-1V voltage reference circuits feasible. The reduction can be done at the sub-circuit that generates the thermal voltages, or at the summing circuit as presented in Section 6.1. Other voltage reference circuit topologies, such as sum/difference of thermal voltages with similar temperature characteristics, can also be used without the need to reduce the thermal voltages of the electron devices, such as the voltage reference circuit presented in Section 6.5 and Exercise 5.11. This kind of voltage reference circuit topology will be discussed in detail in Chapter 7.

6.7 Exercises

Exercise 6.1 *Why can the output voltage of the sub-*1V *opamp based β-multiplier bandgap voltage reference circuit discussed in Section 6.3 not be designed to be smaller than* 800 mV *if the circuit is to be operating in a temperature range of* $-30 \sim 70\ ^{\circ}$C*?*

Exercise 6.2 *Given* $V_{BE} = 0.6$ V, $V_{th,n} = 0.7$ V, *and* $V_{gst,n} = V_{gst,p} = 0.2$ V, *find the minimum stable* V_{DD} *to operate the opamp based β-multiplier bandgap voltage reference circuit in Figure 6.6.*

Exercise 6.3 *The Brokaw bandgap voltage reference circuit is simple to construct and can achieve low TC, however, the operating voltage is high. This is because the input to the opamp equals* V_{BE} *which is lower than the common mode input of the opamp when* V_{DD} *is small.*

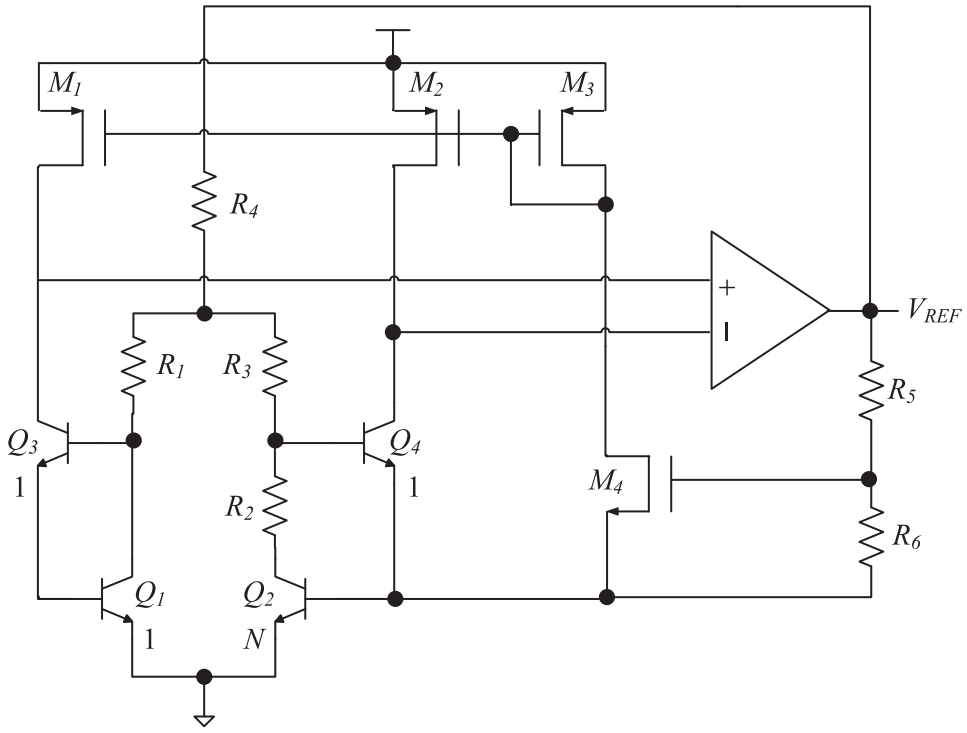


Figure 6.15 A modified Brokaw voltage reference circuit that can operate at low V_{DD} for Exercise 6.3.

Figure 6.15 shows a modified Brokaw bandgap voltage reference circuit which can operate at low V_{DD}. Two additional transistors are placed in series with the original transistors in the Brokaw circuit, such that the input voltages at V_+ and V_- of the opamp are both one V_{BE} higher, and thus satisfy the common mode input voltage range requirement. Assume the circuit has been properly started up, and has R_5, and R_6 properly chosen, such that $I_{DS_1} = I_{DS_2} = 6\ \mu A$ to bias the two BJTs Q_3 and Q_4 in the proper working region.

1. *Derive the output voltage V_{REF} in the form of $V_{REF-CONV}$, and obtain M.*
2. *Find the output voltage that achieves near-zero TC at $T = T_{(nom)}$, and the corresponding resistor ratios with $N = 8$.*

Exercise 6.4 *One of the major problems of the sub-1V opamp based β-multiplier bandgap voltage reference circuit in Figure 6.6 is the extra resistors R_2 and R_3, which inevitability increase the silicon area. Even worse is the resistivity for both resistors are usually large, and thus their layout will consume a large silicon area. One method to alleviate this problem is to share the resistor as shown in Figure 6.16.*

1. *Please derive the condition for the two circuits in Figure 6.6 and 6.16 to be compatible.*
2. *Please derive the best selection of R_5 in Figure 6.16, and share your selection criteria.*

Exercise 6.5 *Using the technique presented in Section 4.5:*

1. *Derive the expression of the $PSRR$ for the sub-1V opamp based β-multiplier bandgap voltage reference circuit with resistive division in Figure 6.6.*

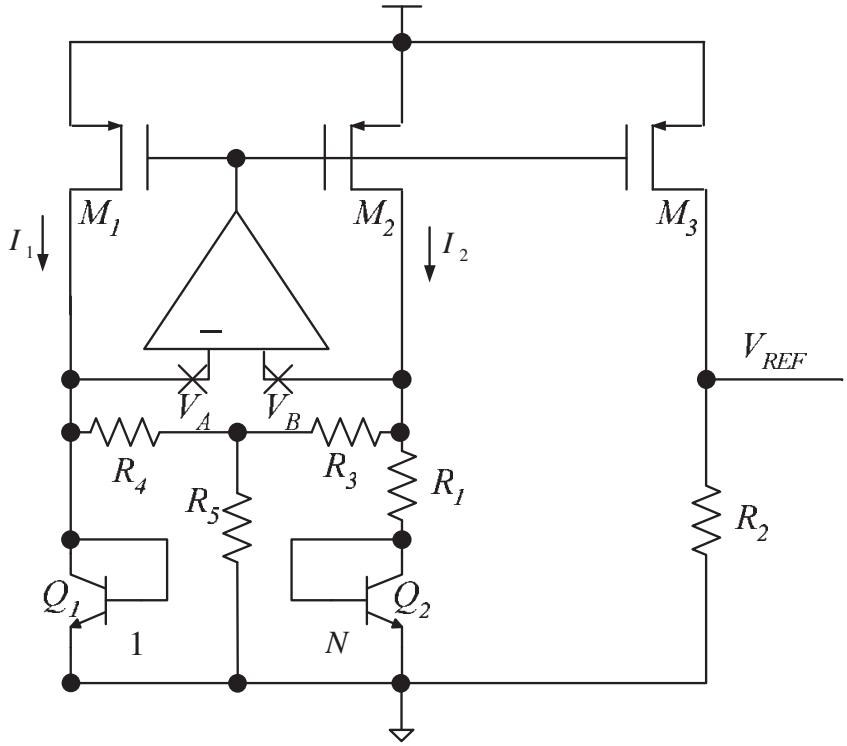


Figure 6.16 Sub-1V opamp based β-multiplier bandgap voltage reference circuit using resistive divided V_{BE} with shared resistors for Exercise 6.4.

2. *Discuss the difference between the PSRR expression of the conventional opamp based β-multiplier bandgap voltage reference circuit in Equation 4.29, and that derived in 1, which one is more robust to V_{DD} variations?*

Exercise 6.6 *Consider the schematic in Figure 6.17. The common gate node of M_1 and M_2 is sufficient to keep M_5 and M_6 operating in triode region. The width of the MOSFET M_7 and M_8 are made to be very large to ensure they are operating in the subthreshold region, and are configured as diode connected transistors. The V_{GS_8} forms the CTAT voltage; and the V_{DS_6} forms the PTAT voltage as M_6 is operating in the triode region. The reference voltage is obtained as*

$$V_{REF} = V_{GS_8} + V_{DS_6}.$$

1. *Expand V_{REF} using the basic equations in Chapter 1.*
2. *Assume*

$$\mu(T) = \mu T^{-1.5},$$
$$V_{th}(T) = -0.002T + V_{th,0} + b = -0.002T + c.$$

Derive the W/L ratio of M_8 with respect to that of M_6 to obtain $\frac{\partial V_{REF}}{\partial T} = 0$.

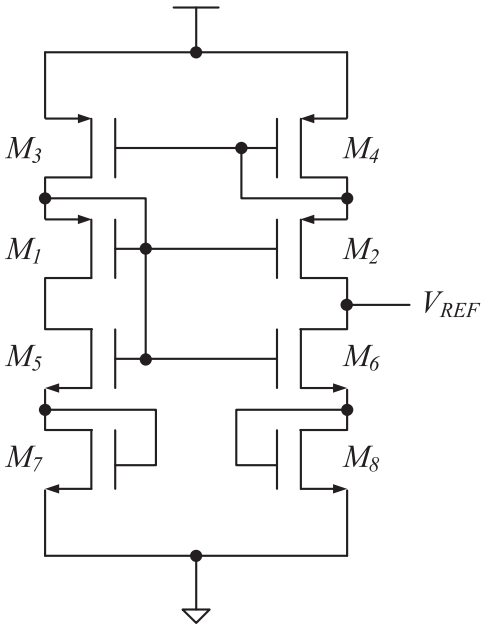


Figure 6.17 Sub-1V output voltage bandgap voltage reference circuit obtained from a modified Wildar voltage reference circuit for the analysis in Exercise 6.6.

Exercise 6.7 *Our discussion on the output stage showed that the loading impedance driven by the voltage reference circuit will alter the output voltage.*

1. *Derive the output voltage V_{REF} of an opamp-based β-multiplier bandgap voltage reference circuit with an output stage as shown in Figure 6.18(a).*
2. *There are a few designs that add additional transistors M_4 into the circuit as shown in Figure 6.18(b). Discuss and explain the use of M_4 in the circuit and choose the optimal I_4 for the circuit to maximize the performance of V_{REF}.*

Exercise 6.8 *(Sub-*1V *Kuijk's bandgap voltage reference circuit by V_{BE} sub-division.) The V_{BE} sub-division technique discussed in Section 6.3.1 that achieves sub-*1V *output voltage from the conventional opamp based β-multiplier bandgap voltage reference circuit can also be applied seamlessly to other β-multiplier bandgap voltage reference circuits. Figure 6.19 shows the schematic of a modified Kuijk's bandgap voltage reference circuit aimed at achieving sub-*1V *reference voltage which was proposed in (Hazucha et al., 2007). This exercise will guide you through the analytical analysis to understand how this circuit works.*

1. *Consider the two-port network Thevnin's equivalent circuit of a resistive voltage divider in Figure 6.20. Derive V_{IN} of the Thevenin's equivalent circuit with $R_{th} = R_X//R_Y$.*
2. *The voltage reference circuit in Figure 6.19 can be analyzed by the divide and conquer method, where the voltage reference circuit is divided into two core circuits as shown in Figure 6.21(a) and (b). Use the two-port Thevenin's equivalent circuit result in* 1 *to derive*

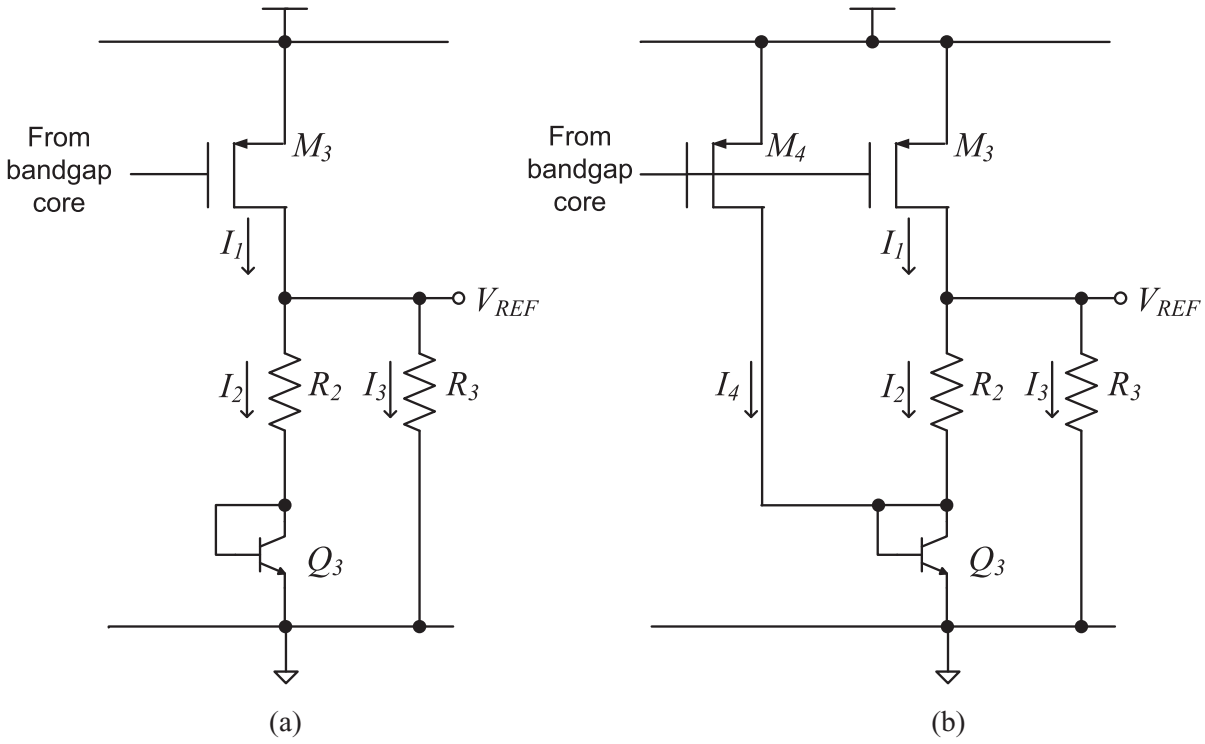


Figure 6.18 The influence of loading impedance driven by the opamp based β-multiplier bandgap voltage reference circuit using (a) conventional output stage, and (b) modified output stage with increased robustness for Exercise 6.7.

the Thevenin's equivalent circuit for Figure 6.21(a) and (b) in terms of the supply voltages K_1 and K_2, respectively.

3. *Derive the output currents I_1 and I_2 of the two Thevenin's circuit as denoted in Figure 6.21(a) and (b).*
4. *Assume an ideal opamp, derive the relationship of I_1/I_2 with $k_1k_2 = k_3k_4$.*

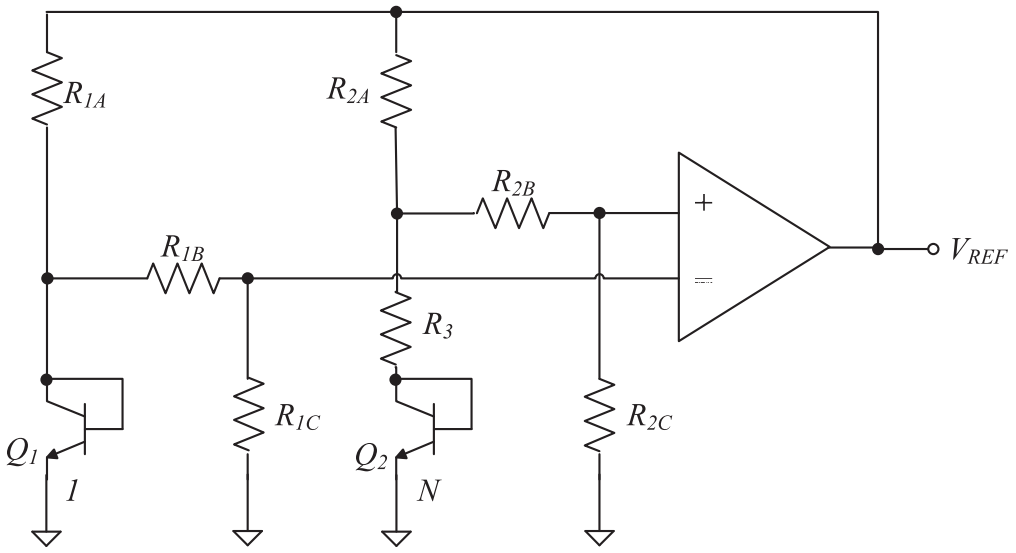


Figure 6.19 Schematic of a modified Kuijk bandgap voltage reference with V_{BE} sub-division (Hazucha *et al.*, 2007) to obtain sub-1V output voltage for Exercise 6.8.

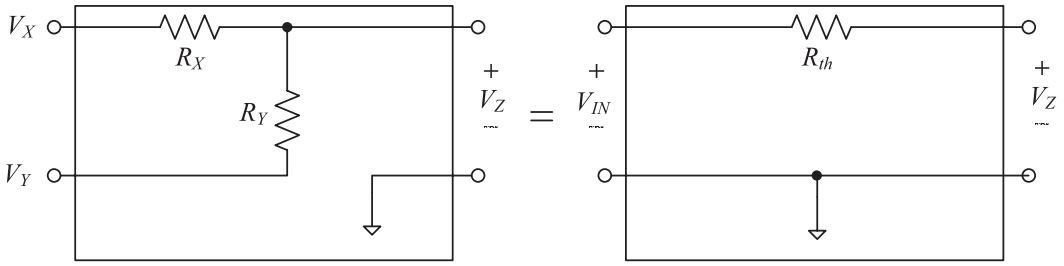


Figure 6.20 A two port Thevnin's equivalent circuit for conversion of the V_{BE} sub-division circuit block of the modified Kuijk bandgap voltage reference circuit in Figure 6.19.

5. *With the derived current ratio, compute* $\Delta V_{BE} = V_1 - V_2$.
6. *Assume* $k_1 = k_2 = k_3 = k_4 = 1$, *and* $R_1 = R_{1,A}$, *and* $R_2 = R_{2,A}$, *show that*

$$V_{REF} = V_{BE,Q_1} + V_T \frac{R_2}{R_3} \ln\left(N \frac{R_2}{R_1}\right),$$

where $N = \frac{A_{E,Q_2}}{A_{E,Q_1}}$ *is the emitter area ratio between* Q_1 *and* Q_2.

Exercise 6.9 *Through this exercise, readers should gain an understanding of the high degree of freedom found in combining various PTAT and CTAT sources together with an appropriate output stage to form a sub-*1V *reference voltage. Figure 6.22 shows a modified peak current voltage reference circuit in Figure 6.13 with a sub-*1V *output stage as shown in Figure 6.1(a). Derive the expression for* V_{REF} *and show that it can be less than* 1 V.

Exercise 6.10 *Considers the voltage reference circuit in Figure 6.23. Assume* $R_{2a} = R_{3a}$, $R_{2b} = R_{3b}$, $R_3 = R_{3a} + R_{3b}$, *and* $S_1 = S_2 = S_3$. *Derive* V_{REF} *in terms of* R_1, R_3, R_4, V_T, N, S_4, *and* S_5 *only.*

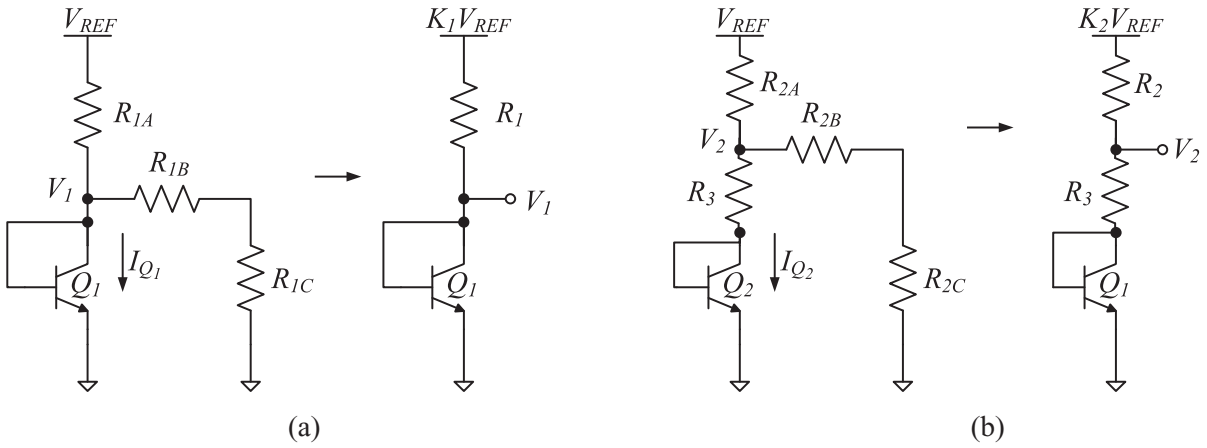


Figure 6.21 The equivalent circuit blocks of the modified Kuijk bandgap voltage reference with V_{BE} sub-division shown in Figure 6.19.

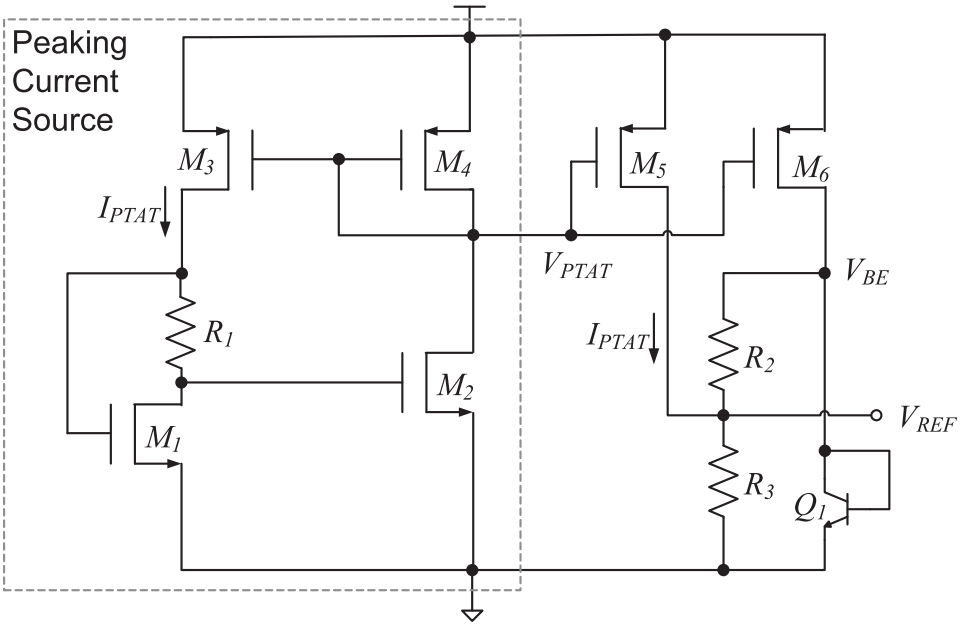


Figure 6.22 The schematic of a sub-1V peak current source based bandgap voltage reference circuit for Exercise 6.9.

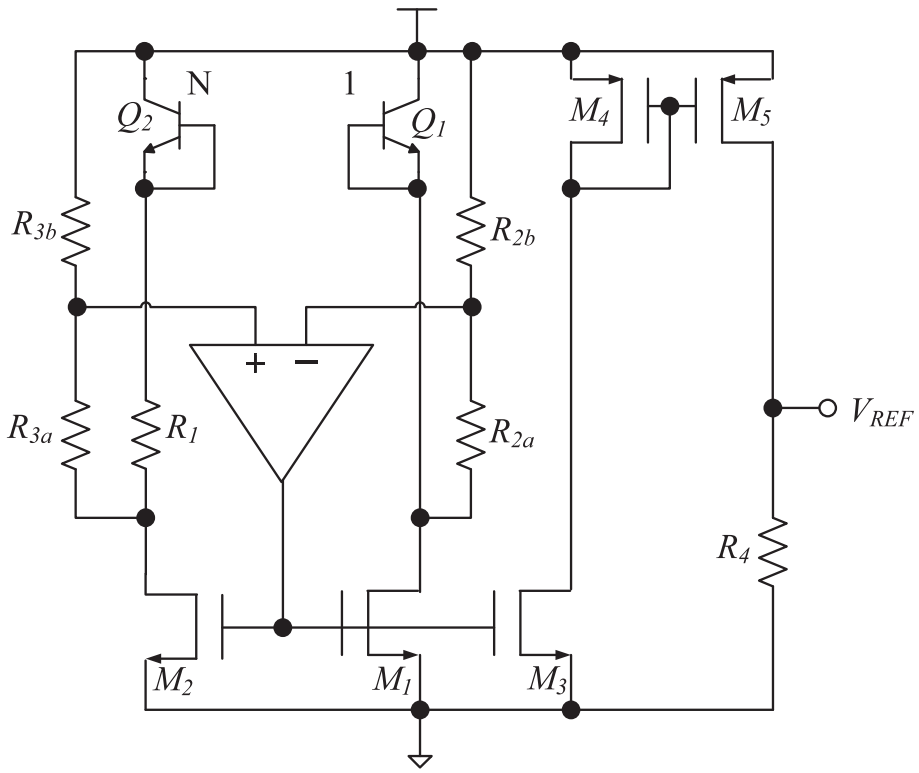


Figure 6.23 Sub-1V opamp based β-multiplier bandgap voltage reference circuit using resistor division (Leung and Mok, 2002) implemented with NPN transistors for Exercise 6.10.

References

Annema, A.J. (1999) Low-power bandgap references featuring DTMOSTs. *IEEE Journal of Solid-State Circuits*, **34** (7), 949–55.

Banba, H., Shiga, H., Umezawa, A. *et al.* (1999) A CMOS bandgap reference circuit with sub-1-V operation. *IEEE Journal of Solid-State Circuits*, **34** (5), 670 –74.

Blalock, B.J., Allen, P.E. and Rincon-Mora, G.A. (1998) Designing 1-V opamps using standard digital CMOS technology. *IEEE Transaction on Circuits and Systems II – Express Briefs*, **45** (7), 769–80.

Doyle, J.T., Lee, Y.J., Kim, Y.B. *et al.* (2003) Implementation of a 1 volt supply cmos subbandgap reference circuit. *Proceedings of IEEE International Systems – On-Chip Conference*, pp. 323–26.

Hazucha, P., Moon, S.T., Schrom, G. *et al.* (2007) Low-voltage, buffered bandgap reference with selectable output voltage US Patent Number 7274250.

Ker, M.D., Chen, J.S. and Chu, C.Y. (2006) New curvature-compensation technique for CMOS bandgap reference with sub-1-V operation. *IEEE Transaction on Circuits and Systems – II: Express Briefs*, **53** (8), 667–71.

Kerns, D.V. (1986) Optimization of the peaking current source. *IEEE Journal of Solid-State Circuits*, **21** (4), 587–90.

Kwok, C.Y. (1985) Low-voltage peaking complementary current generator. *IEEE Journal of Solid-State Circuits*, **20** (3), 816–18.

Leung, K.N. and Mok, K.T. (2002) Sub-1-v 15-ppm/°c CMOS bandgap voltage reference without requiring low threshold voltage device. *IEEE Journal of Solid-State Circuits*, **37** (4), 526–29.

Leung, K.N. and Mok, P.K.T. (2003) A CMOS voltage reference based on weighted ΔV_{GS} for CMOS low-dropout linear regulators. *IEEE Journal of Solid-State Circuits*, **38** (1), 146–50.

Miller, S. and MacEachern, L. (2006) A nanowatt bandgap voltage reference for ultra-low power applications. *Proceedings of IEEE International Symposium on Circuits and Systems*, pp. 625–48.

Neuteboom, H., Kup, B. and Janssens, M. (1997) A DSP-based hearing instrument IC. *IEEE Journal of Solid State Circuits*, **32**, 1790–1806.

Pletersek, A. (2005) A compensated bandgap voltage with sub-1-V supply voltage. *Analog Integrated Circuits and Signal Processing*, **44**, 5–15.

Ripamonti, G., Bertolaccini, M., Peritore, R. *et al.* (1999) Low power-low voltage band gap references for flash-EEPROM integrated circuits: design alternatives and experiments. *Proceedings of the 6th IEEE International Conference on Electronics, Circuits and Systems*, **2**, 635–38.

Sakurai, H. and Sugimoto, Y. (2007) The realization of an area-efficient CMOS bandgap reference circuit with less than 1.25 V of output voltage using a fractional v_{BE} amplification scheme. *IEICE Transactions on Electronic*, **E90-C** (2), 499–506.

7

High Order Curvature Correction

In theory, the voltage reference circuit can obtain a near-zero *TC* voltage by the mutual compensation of properly scaled CTAT and PTAT voltages. In practice, the CTAT and PTAT voltage sources are seldom precisely linearly proportional to temperature. To understand the temperature dependency of various voltage sources, let's consider the Taylor series expansion of the CTAT voltage $V_{BE}(T)$ in the opamp based β-multiplier bandgap voltage reference circuit at $T_{(nom)}$ as shown in Equation 7.1 in a sequel. We can observe that the $V_{BE}(T)$ voltage has high order temperature dependent terms. The opamp based β-multiplier bandgap voltage reference circuit considered in previous chapters generates the reference voltage by linear combination of the CTAT and PTAT voltages will be able to achieve mutual compensation of the first order temperature dependent terms of the CTAT and PTAT voltages. As a result, the opamp based β-multiplier bandgap voltage reference circuit is said to be a voltage reference circuit with *first order temperature compensation*. Using a similar argument, most of the temperature compensated voltage reference circuits presented in previous chapters are first order temperature compensated voltage reference circuits. Since the first order temperature compensated voltage reference circuit does not compensate the high order temperature dependent terms of the CTAT and PTAT sources, as a result, when the PTAT and CTAT terms are nonlinear functions (the reader will find that the terms "nonlinear" and a "high order" are used interchangeably in this book) of the temperature, such as in the case of $V_{BE}(T)$ and $\Delta V_{BE}(T)$. The first order temperature compensated voltage reference circuits will only be able to achieve a reference voltage within a given voltage variation in a limited temperature range. This limitation becomes obvious in the sub-1V supply/output voltage reference circuits (Banba *et al.*, 1999; Hirose *et al.*, 2005). High performance voltage reference circuits that suppress the high order temperature dependent terms between the mutual compensation of the CTAT and PTAT voltages can reduce the *TC* of the obtained reference voltage over a wide temperature range. The variation of the reference voltage due to temperature variation is also known as the "*curvature error*." The reduction of the high order temperature dependent terms of the reference voltage, or simply the nonlinear terms of the reference voltage is therefore referred to as "*curvature correction*" or "*curvature compensation*." In the following, we shall first formally define the compensation order of the high order temperature compensated voltage reference circuit. Various high order temperature compensation techniques will be discussed in subsequent sections, which include the piecewise temperature compensation, and mutual compensation of voltages with similar temperature dependency, etc.

CMOS Voltage References: An Analytical and Practical Perspective, First Edition. Chi-Wah Kok and Wing-Shan Tam.

7.1 Compensation Order

The classical voltage reference circuit generates a near-zero *TC* reference voltage through the weighted sum of the CTAT and the PTAT voltages. By expanding the CTAT and PTAT voltages into Taylor series at $T = T_{(nom)}$ yield

$$V_{CTAT}(T) = a_0 + a_1\left(T - T_{(nom)}\right) + a_2\left(T - T_{(nom)}\right)^2 + a_3\left(T - T_{(nom)}\right)^3 + \cdots, \tag{7.1}$$

$$V_{PTAT}(T) = b_0 + b_1\left(T - T_{(nom)}\right) + b_2\left(T - T_{(nom)}\right)^2 + b_3\left(T - T_{(nom)}\right)^3 + \cdots, \tag{7.2}$$

where a_k and b_k are constant coefficients of the k-th order temperature dependent terms with respect to $T_{(nom)}$. Even though the coefficients associated with the high order temperature dependent terms may be small, they will become dominant sources of the curvature error at temperature significantly higher or lower than $T_{(nom)}$. Consider the voltage reference circuit obtained by the temperature dependent weighted sum of CTAT and PTAT voltage sources where

$$V_{REF}(T) = m(T)V_{CTAT}(T) + n(T)V_{PTAT}(T). \tag{7.3}$$

To achieve near-zero *TC*, we shall design $m(T)$ or $n(T)$ such that

$$m(T)a_1 + n(T)b_1 \approx 0, \tag{7.4a}$$

$$m(T)a_2 + n(T)b_2 \approx 0, \tag{7.4b}$$

$$\vdots$$

$$m(T)a_k + n(T)b_k \approx 0, \tag{7.4k}$$

$$\vdots$$

In other words, the composite functions $m(T)V_{CTAT}(T) + n(T)V_{PTAT}(T)$ are voltage functions with high order temperature dependency. The order of the curvature compensation (temperature compensation) method is therefore formally defined as the highest order of the temperature dependent terms being nullified through the weighted sum in the system of equations in Equation 7.1.

Note that the system of equations in Equation 7.1 is not only difficult to solve, it is also difficult to implement. Various methods have been proposed to simplify the determination of the temperature dependent weighting function $m(T)$ and $n(T)$, and the implementation of the weighted sum system within an acceptable compensation error. These include:

1. First order temperature compensation: Where a_k and b_k are assumed to be equal to zero for $k \geq 2$. In this case, a zero *TC* reference voltage is obtained when $m(T) = 1$ and $n(T) = -\frac{a_1}{b_1}$. The β-multiplier bandgap voltage reference circuits, and most of the voltage reference circuits discussed in Chapters 3, 5, and 6 are first order temperature compensated voltage

reference circuits. Such systems are simple to design and implement. They also require a minimal set of device model parameters (a_1 and b_1 alone will be enough) to complete the design, and thus lower the requirement on device characterization. As a result, the simple SPICE model provided by most of the foundries in today's semiconductor industry can be applied to assist in the design of first order compensated voltage reference circuits. The drawback of the first order temperature compensation system is the poor curvature compensation result due to the fact that the high order temperature dependent terms are not compensated. As a result, the near-zero *TC* reference voltage can only be obtained in a very limited temperature range.

2. Second order temperature compensation: Where a_k and b_k are assumed to be equal to zero for $k \geq 3$. In this case, a zero *TC* reference voltage obtained by solving Equation 7.4 for $m(T)$ and $n(T)$ directly will yield a second order temperature function $m(T)$ and $n(T)$. This scaling factor is difficult to design, and difficult to apply to scale $V_{CTAT}(T)$ and $V_{PTAT}(T)$ in Equation 7.3. As a result, instead of solving $m(T)$ and $n(T)$ from the system of equations in Equation 7.4, temperature independent constant values are adopted, such that $m(T) = m$ and $n(T) = n$. An additional second order temperature dependent voltage $s(T - T_{(nom)})^2$ (s is a constant, and we shall assume that a voltage sum voltage reference circuit is under consideration for the ease of explanation while the same technique can also be applied to current sum voltage reference circuits) is applied to compensate the curvature error obtained from Equation 7.3, such that

$$V_{REF}(T) = mV_{CTAT}(T) + nV_{PTAT}(T) + s\left(T - T_{(nom)}\right)^2,$$

is a zero *TC* reference voltage. One of the possible designs to obtain a zero *TC* reference voltage is to use

$$m(T) = 1, \tag{7.5}$$

$$n(T) = \frac{-a_1}{b_1}. \tag{7.6}$$

Thus

$$\begin{aligned} V_{REF}(T) &= \left(a_0 + a_1(T - T_{(nom)}) + a_2(T - T_{(nom)})^2\right) \\ &\quad - \frac{a_1}{b_1}\left(b_0 + b_1(T - T_{(nom)}) + b_2(T - T_{(nom)})^2\right) \\ &\quad + s(T - T_{(nom)})^2 \\ &= \frac{a_0 b_1 - a_1 b_0}{b_1} + \frac{a_2 b_1 - a_1 b_2 + s b_1}{b_1}(T - T_{(nom)})^2. \end{aligned} \tag{7.7}$$

As a result, a zero TC $V_{REF}(T)$ will be obtained when $a_2 b_1 - a_1 b_2 + s b_1 = 0$, which will in turn require $s = \frac{a_1 b_2 - a_2 b_1}{b_1}$. Theoretically, high order temperature dependent terms can be designed and induced into the voltage reference circuit to obtain high order curvature compensated reference voltage with low *TC* over a wide temperature range. As a result, it is tempting to induce high order temperature dependent terms with order higher than 2 to compensate the curvature error with orders higher than 2. However, the third order

and higher order curvature correction are not practical because of the high sensitivity of the compensation error with respect to device mismatch, and process variation, etc. Due to the nature of the high order temperature dependency, a small error in the high order temperature compensation will easily dominate the overall compensation error in the temperature range under consideration, and thus cannot achieve a low *TC* reference voltage over a wide temperature range. Furthermore, the high device mismatch and process variation sensitivity will lower the yield, or require a complicated post-fabrication trimming procedure. Therefore, it is rare to find high order temperature compensated voltage reference circuit with an order higher than 2 in practice.

3. Piecewise linear compensation: The temperature range of interest is divided into multiple consecutive non-overlapping sections, and different temperature compensation circuits are applied to different temperature sections. There are several advantages to performing temperature compensation in separate temperature sections. First, because the size (the temperature range covered by each section) of each section is small, the curvature of $V_{CTAT}(T)$ and $V_{PTAT}(T)$ can be approximated to be linear in each section. As a result, a simple temperature compensation technique can be applied. Even if zero *TC* cannot be obtained in each section, the variation of the reference voltage with respect to each temperature section will be small because of the small size of each section which limits the temperature compensation error within each section. Furthermore, if we can alter the directions (signs of the slope) of the temperature dependency of the reference voltages in adjacent sections as shown in Figure 7.1, the variation of the reference voltage in adjacent sections will not accumulate, and thus we can obtain a low *TC* reference voltage over a wide temperature range where the reference voltage variation in the whole temperature range of interest will be close to that of the temperature section with the largest voltage variation. This property is clearly observed in Figure 7.1. The idea is similar to the Alternation Theorem in approximation theory (Cheney, 1982). In practice, multi-section curvature compensation can also be applied with high order temperature compensation within each temperature section. In this case, the high order temperature compensation can also benefit from the multi-section curvature compensation. This is because, in reality, it will be

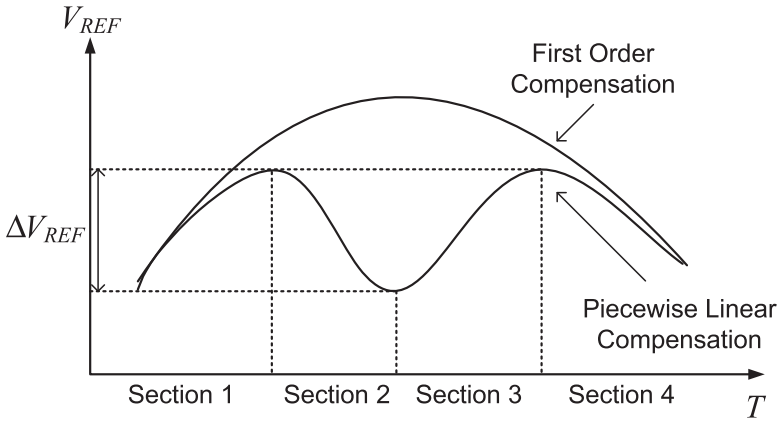


Figure 7.1 Adjacent sections of multi-section curvature compensation having alternate signs of the temperature coefficient help to lower the temperature coefficient of the voltage reference circuit over the entire temperature range of interest.

difficult to obtain current/voltage sources with temperature dependent orders higher than 2 for a wide temperature range. Instead, it is more practical to obtain a current/voltage source that can approximate the desired order of temperature dependency within a limited temperature range.

This "multi-section curvature compensation" technique is also known as the "*multi-point curvature compensation*" and "*piecewise linear compensation*" technique. The last name is the most popular, although in most cases there are high order temperature dependent current/voltage terms being applied in the temperature compensation, instead of linear temperature dependent current/voltage terms. Indeed, due to the naming convention of Rincon-Mora (Rincon-Mora and Allen, 1998), since then the term piecewise linear compensation has been commonly adopted in the literature.

Since the voltage variation can be reduced with a narrower temperature range, it is tempting to sub-divide the temperature range of interest into many sections to obtain a small *TC* over a wide temperature range. However, all the circuits used to generate the curvature compensation current/voltage are sensitive to temperature and process variations. Therefore, the temperature sub-division boundaries between each section are also sensitive to temperature and process variations, and thus increasing the number of sections may degrade the overall *TC* of the reference voltage due to the increasing inaccuracy in compensation and variation of the temperature boundaries of each temperature section. A balance between the number of sub-divided temperature sections and the desired *TC* of the reference voltage is the key to the successful application of the piecewise linear compensation technique.

4. Weighted sum of voltage/current with similar temperature dependency: Without loss of generality, this text will only discuss temperature dependent voltage sources, while the discussions are useful to both temperature dependent voltage and current sources. Two temperature dependent voltage sources, $V_1(T)$ and $V_2(T)$ that have temperature characteristics

$$V_1(T) = a_0 + a_1\left(T - T_{(nom)}\right) + a_2\left(T - T_{(nom)}\right)^2 + a_3\left(T - T_{(nom)}\right)^3 + \cdots \tag{7.8}$$

$$V_2(T) = b_0 + b_1\left(T - T_{(nom)}\right) + b_2\left(T - T_{(nom)}\right)^2 + b_3\left(T - T_{(nom)}\right)^3 + \cdots \tag{7.9}$$

are said to be similar in temperature dependency if $a_\ell = c\ b_\ell$ for all $\ell \geq 1$, where c is a constant. In other words, the graph of $V_1(T)$ and $V_2(T)$ against temperature are a vertical shift (and possible flip) of each other. These voltage sources can be used to construct a zero *TC* reference voltage V_{REF} by weighted sum of $V_1(T)$ and $V_2(T)$ as

$$V_{REF}(T) = m(T)V_1(T) + n(T)V_2(T),$$

with $n(T) = -cm(T)$. When $m(T) = 1$, $V_{REF} = a_0 - cb_0 \neq 0$ which is temperature independent (where we assume that $a_0 \neq cb_0$, hence the vertical shift characteristics). These two voltages $V_1(T)$ and $V_2(T)$ are allowed to have high order temperature dependence, in contrast to the monotonically increasing/decreasing voltage sources against temperature required in the first order temperature compensation topology for the generation of V_{REF} with zero *TC*. The mutual compensation of voltage sources with similar temperature dependence is therefore a generalization of the mutual compensation of the CTAT and PTAT

voltages. Note that the mutual compensation of voltage sources with similar temperature dependency should be able to provide more design freedom, while this method is also more sensitive to device mismatch and process variation.

One of the major sources of compensation errors occurs when the two temperature dependent voltage sources are not that "similar" to each other. This will occur when there is device mismatch and process variation. Besides the potential temperature compensation problem, the obtained reference voltage is also subject to higher nominal voltage variation. This is because the reference voltage nominal value variation is the sum of nominal voltages variation of individual voltage sources. Note that the voltage sources under consideration are high order temperature dependent, and hence the temperature dependence is highly unpredictable when compared to that of the first and second order temperature compensated voltage reference circuits.

There are a large number of voltage reference circuits in the literature that do not fall into any of the above discussed categories. Each of the voltage reference circuits has its own pros and cons, and are designed to tackle different design and real world application problems. However, for most of the practical design requirements, simple voltage reference circuits from one of the above four categories should be sufficient. Furthermore, although almost all CTAT and PTAT voltages that can be obtained in CMOS circuits contain high order temperature dependent terms. The magnitude of the coefficients associated with the high order temperature dependent terms are very small and could be ignored with respect to the temperature range of interest. Therefore, for most practical applications, second order temperature compensation will be sufficient to achieve the desired reference voltage performance. As a result, Section 7.2 will first discuss two different techniques to achieve second order temperature compensation using the conventional opamp-based β-multiplier bandgap voltage reference circuit. Another popular second order temperature compensation voltage reference circuit topology known as BJT current subtraction will be discussed in Section 7.3. Section 7.4 will discuss the design of voltage reference circuit with linear compensation using both addition and subtraction of second order current sources at selected temperature locations from the PTAT current of the conventional opamp based β-multiplier bandgap voltage reference circuit discussed in Section 3.2.1 to achieve a reference voltage with low *TC* over a wide temperature range. The temperature compensated reference voltage obtained from the mutual compensation of devices and circuits with similar temperature dependent voltage characteristics will be discussed in Section 7.5. This chapter will conclude in Section 7.6 with a brief discussion on various high order temperature compensation techniques in the literature.

7.2 Second Order Temperature Compensation

The limitation of the first order temperature compensation arises from the high order temperature dependent terms of the CTAT and PTAT voltages as shown in Equations 7.1 and 7.2. The consequence is the near-zero *TC* reference voltage can only be achieved in a limited temperature range, as shown in Figure 3.1. A low *TC* voltage reference circuit over a wide operable temperature range can be obtained by second order temperature compensation. This can be achieved in many ways. In this section, we shall discuss two effective methods by the addition and subtraction of second order temperature dependent currents from the current sources of

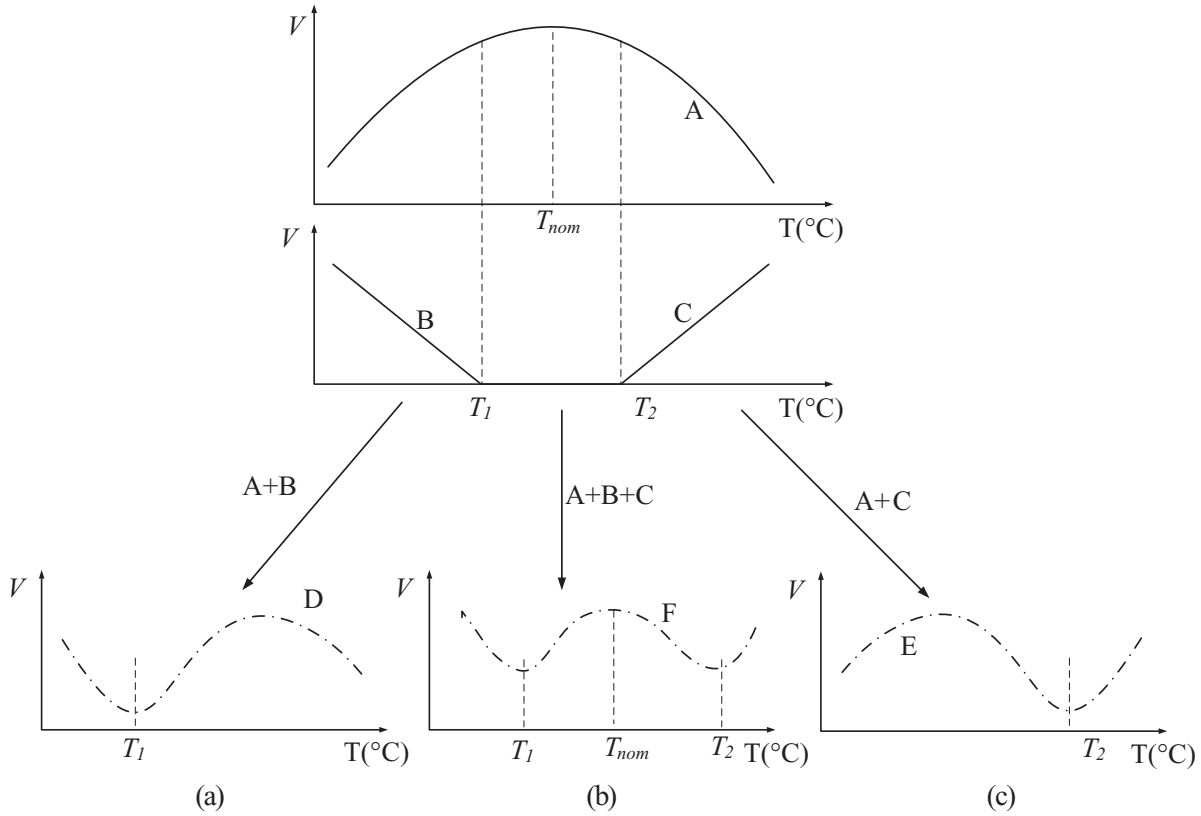


Figure 7.2 Illustration of second order temperature dependent voltage source $n_1(T)$ (curve C) or $n_2(T)$(curve B) to the bandgap voltage reference circuit output voltage $V_{BE} + MV_T$ to obtain the 2^{nd} order curvature compensated reference voltage in sub-figure (c) and (a), respectively.

the β-multiplier to achieve second order temperature compensation. Figure 7.2 shows the topological diagram to obtain a second order temperature compensated reference voltage by the addition of second order temperature dependent voltages $n_1(T)$ or $n_2(T)$ to the first order temperature compensated bandgap voltage reference output voltage $V_{BE} + MV_T$. As you can observe from the figure, the addition of a voltage with second order *TC* at the appropriate temperature region will be able to increase the reference voltage at the selected temperature region, and thus achieve a low *TC* reference voltage over a wide temperature range.

Before the discussions of the second order temperature compensation methods, we shall first discuss the construction of current source and current sink with second order *TC*. A current source with high order *TC* can be conveniently obtained by BJTs. Subsequent sections will present methods to insert this second order current source/sink into the opamp based β-multiplier bandgap voltage reference circuits to obtain reference voltages with low *TC* over wide temperature ranges.

7.2.1 Second Order Current Source

In this section, we shall discuss the design of current sources with second order temperature dependence that activate at a chosen temperature. Such current sources can exist in two forms: a current sink as shown in Figure 7.3(a), and a current source as shown in Figure 7.3(b). (The

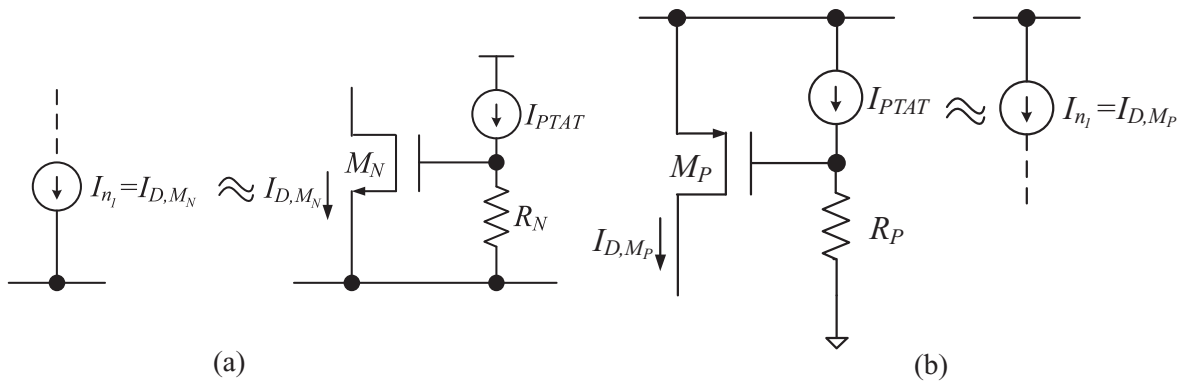


Figure 7.3 The schematic of second order temperature dependent current sources in (a) current sink form and (b) current source form.

current sink and source under concern are I_{D,M_N} and I_{D,M_P}, respectively.) Let's first consider the current sink in Figure 7.3(a) which consists of a resistor R_N driven by a PTAT current source thus producing a PTAT voltage. This PTAT voltage will form the V_{GS,M_N} of the NMOS transistor M_N. If we use the same PTAT current obtained from the opamp based β-multiplier, we shall obtain

$$V_{GS,M_N} = R_N \frac{V_T \ln N}{R_1}. \tag{7.10}$$

When $V_{GS,M_N} \geq V_{th,n}$, the current I_{D,M_N} sunk by transistor M_N will be large enough to influence the rest of the circuit that it is plugged into. Consider the case where the rest of the circuit is designed to obtain $V_{DS} \geq V_{GS} - V_{th,n}$ and $V_{GS,M_N} \geq V_{th,n}$. As a result, M_N will be working in saturation, which yields

$$I_{D,M_N} = \frac{1}{2}\mu_n C_{ox,n} S_{M_N} (V_{GS,M_N} - V_{th,n})^2. \tag{7.11}$$

The temperature dependence of I_{D,M_N} can be investigated by the temperature dependence of its components. If we take time to review Section 1.2.4, we shall find that the temperature dependence of the electron mobility is approximately a second order inverse temperature dependent function, and that of the threshold voltage is a first order temperature function, and finally V_{GS,M_N} is obtained by the I-V conversion of I_{PTAT} through R_N, which is assumed to have near-zero TC . Since I_{PTAT} is a second order temperature dependent function (otherwise second order temperature compensation will not be required), therefore V_{GS,M_N} will also be a second order temperature dependent function. As a result, Equation 7.11 can be approximated as

$$\begin{aligned} I_{D,M_N} &= c_0 T^{-2}(c_1 + c_2(T - T_2) + c_3(T - T_2)^2)^2 \\ &= a_{-2}(T - T_2)^{-2} + a_{-1}(T - T_2)^{-1} + a_0 + a_1(T - T_2) + a_2(T - T_2)^2, \end{aligned} \tag{7.12}$$

where the temperature coefficient for electron mobility is lumped together with $C_{ox,n}$ and S_{M_N} to form c_0, the temperature coefficients of the second order PTAT voltage V_{GS,M_N} and the first

order PTAT voltage $V_{th,n}$ are lumped to the second order polynomial with coefficients c_1, c_2 and c_3. Finally, T_2 is the activation temperature as detailed in Figure 7.2. After expanding and rearranging the equation, the coefficients are grouped to and from (a_{-2} and a_2). If we refer to Figure 7.2, it is clear that we require $I_{D,M_N} = 0$ for $T < T_2$. Let's assume our design can achieve this requirement, then we shall be able to observe that in the temperature range of ($T > T_2$), the negative order temperature coefficients will not have any significant contribution to I_{D,M_N}. As a result, we finally obtain

$$I_{D,M_N} \approx a_0 + a_1(T - T_2) + a_2(T - T_2)^2, \qquad \text{for } T > T_2.$$

For most of the CMOS process, the coefficients a_0, a_1, and a_2 are small, and thus the term with the highest temperature coefficient will dominate I_{D,M_N}. This is especially true when the temperature region of interest is at the high temperature region. As a result,

$$I_{D,M_N} \begin{cases} = 0, & T \leq T_2, \\ \propto (T - T_2)^2, & T > T_2. \end{cases}$$

Now, it leaves to us to determine the circuit condition that will fulfill $I_{D,M_N} = 0$ at $T \leq T_2$. Note that V_{GS,M_N} is given by Equation 7.10, therefore the inequality of the temperature requirement are equivalent to

$$I_{D,M_N} \begin{cases} = 0, & V_{GS,M_N} \leq V_{th,n}, \\ \propto (T - T_2)^2, & V_{GS,M_N} > V_{th,n}. \end{cases}$$

This is because there will be $I_{D,M_N} > 0$ flowing through the transistor if V_{GS,M_N} satisfies Table 1.1 for saturation operation. This will in turn require

$$V_{GS,M_N} = R_N \frac{V_T \ln N}{R_1} > V_{th,n}$$

$$T > \frac{R_1}{R_N} \frac{q}{k} \frac{V_{th,n}}{\ln N} = T_2. \tag{7.13}$$

As a result, by adjusting either the resistor R_1, R_N or the BJT transistor emitter area ratio N of the opamp based β-multiplier PTAT current source, we shall be able to adjust the temperature position that will activate this second order temperature dependent current.

Similarly, the current source shown in Figure 7.3(b) that consists of a resistor R_P driven by a PTAT current source to form V_{GS,M_P} will generate a current source I_{D,M_P} with a second order temperature dependence, such that

$$I_{D,M_P} \approx b_0 + b_1(T_1 - T) + b_2(T_1 - T)^2, \qquad \text{for } T < T_1. \tag{7.14}$$

As observed from Figure 3.1(b), this second order temperature dependent current source should be activated at temperature range $T \leq T_1$. In other words

$$I_{D,M_P} \begin{cases} \propto (T_1 - T)^2, & T < T_1, \\ = 0, & T \geq T_1. \end{cases}$$

Similarly, we can determine the circuit condition that fulfills $I_{D,M_P} = 0$ at $T \geq T_1$ by examining the equivalent condition

$$I_{D,M_P} \begin{cases} \propto (T_1 - T)^2, & V_{SG,M_P} > -V_{th,p}, \\ = 0, & V_{SG,M_P} \leq -V_{th,p}. \end{cases}$$

Note that V_{SG,M_P} is given by

$$V_{SG,M_P} = R_P \frac{V_T \ln N}{R_1}.$$

As a result, we shall obtain the activation temperature

$$T_1 = \frac{R_1}{R_P} \frac{q}{k} \frac{V_{th,p}}{\ln N}. \tag{7.15}$$

These two current sinks/sources with second order temperature dependence can be applied to compensate the high order temperature dependent terms of the reference voltage by appropriate selection of R_1, R_P, R_N, and N. The following two sections will discuss two techniques that apply these two current sinks and sources to the conventional opamp based β-multiplier bandgap voltage reference circuit to achieve reference voltages with a low temperature coefficient over a wide temperature range.

Besides the MOSFET transistors, the BJT can also be used to generate current with second order temperature dependence, and be applied to compensate the high order temperature dependent terms of the reference voltage. Section 7.3 will discuss the application of BJT generated current sink with second order temperature dependence to compensate the high order temperature dependent terms of the opamp based β-multiplier bandgap voltage reference circuit.

7.2.2 Current Subtraction

The current sink in Figure 7.3(a) can be used to construct a second order temperature dependent current subtraction circuit at a selected temperature range. Note that there are only two important current paths in the opamp based β-multiplier bandgap voltage reference circuit, which are the two current paths that pass through Q_1 and Q_2. Figure 7.4 shows currents can be injected into or extracted from the BJTs at nodes A and B respectively, to affect the output voltage of the voltage reference circuit. The following sections will discuss the effects of connecting the current source/sink with second order temperature dependency to node A/B. Consider the schematic in Figure 7.5, which connects a current sink to node B. If R_N is selected according to Equation 7.13 for a pre-selected temperature T_2 as shown in Figure 7.2(c), then the second order temperature dependent current I_{D,M_N} will be small when $T < T_2$, and can be ignored. Therefore, in the temperature range $(-\infty, T_2]$, the voltage reference circuit in Figure 7.5 will behave as a normal opamp based β-multiplier bandgap voltage reference circuit discussed in Chapter 3. When the temperature reaches T_2, I_{D,M_N} will be large enough to affect the opamp based β-multiplier circuit by draining current from I_2. In other words, the

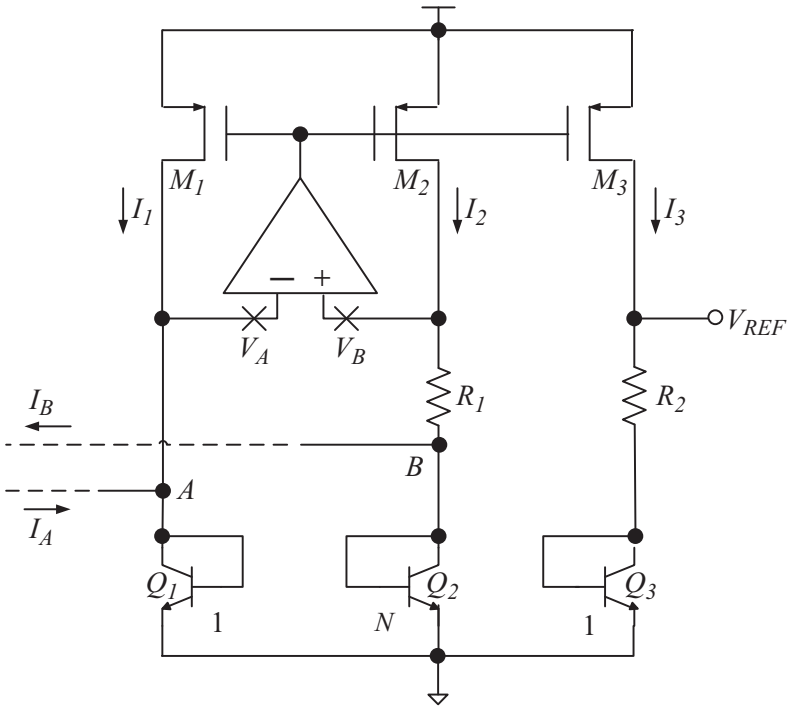


Figure 7.4 Second order temperature compensation by addition and subtraction through nodes A and B, respectively.

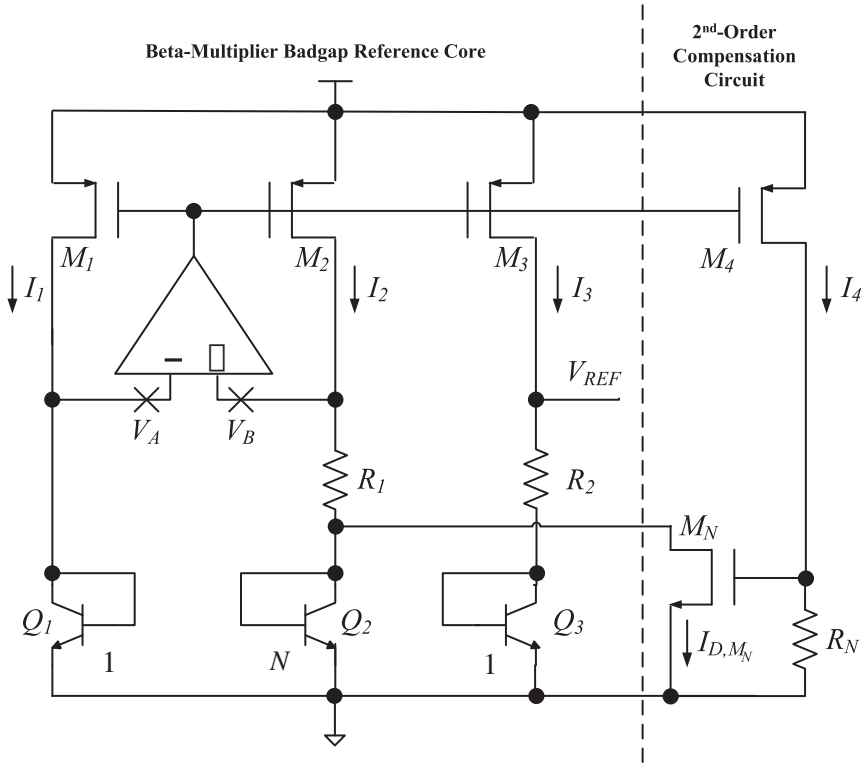


Figure 7.5 The schematic of second order temperature compensated voltage reference circuit by current subtraction with second order temperature characteristics.

current density of Q_2 will be reduced and hence V_B will be reduced too. Since $V_A \neq V_B$ will upset the negative feedback loop of the opamp based β-multiplier, as a result, the opamp will drive M_2 to increase I_2, until the voltage drop across R_1 and Q_2 is the same as that of Q_1. In other words, I_2 will be increased to restore V_B to having the same potential as V_A. Because of the current mirror between M_2 and M_3, the PTAT voltage across R_2 will increase, and thus increase the output voltage V_{REF}. The higher the temperature, the larger the PTAT current I_4, and thus the higher the PTAT voltage across R_N, which will in turn increase the amount of current I_3, and hence increase the voltage drop across R_2. Finally, it will increase V_{REF} and achieve high order temperature compensation.

We can determine T_2 by examining the temperature dependent voltage in Figure 3.9. The only question that remains is how to choose an appropriate resistance for R_N and W/L for M_N. We can determine this analytically. Following the derivation in Chapters 1 and 3

$$\begin{aligned} V_{REF}(T) &= V_{BE_3}(T) + M\Delta V_{BE_{1,2}}(T) \\ &= V_{G0}\left(1 - \frac{T}{T_{(nom)}}\right) + V_{BE_3}\left(T_{(nom)}\right)\frac{T}{T_{(nom)}} - \rho V_T \ln\left(\frac{T}{T_{(nom)}}\right) \\ &\quad + V_T \ln\left(\frac{I_{Q_3}(T)}{I_{Q_3}(T_{(nom)})}\right) + MV_T \ln\left(\frac{I_{Q_1}(T)}{I_{Q_2}(T)}N\right), \end{aligned} \tag{7.16}$$

where Equation 1.4 is substituted into $V_{BE}(T)$ instead of Equation 1.7 because the collector current is assumed to be high order temperature dependent. Similarly, Equation 1.14 is applied in the case of $\Delta V_{BE_{1,2}}$. The temperature dependence of V_{REF} can be computed by differentiating with respect to T, which yields

$$\begin{aligned} \frac{\partial V_{REF}}{\partial T} &= \frac{-V_{G0}}{T_{(nom)}} + \frac{V_{BE_3}(T_{(nom)})}{T_{(nom)}} - \rho\frac{k}{q}\left(\ln\left(\frac{T}{T_{(nom)}}\right) + 1\right) + \frac{k}{q}\ln\left(\frac{I_{Q_3}(T)}{I_{Q_3}(T_{(nom)})}\right) \\ &\quad + \frac{V_T}{I_{Q_3}(T)}\frac{\partial I_{Q_3}(T)}{\partial T} + M\frac{k}{q}\ln\left(\frac{I_{Q_1}(T)}{I_{Q_2}(T)}N\right) \\ &\quad + MV_T\left(\frac{1}{I_{Q_1}(T)}\frac{\partial I_{Q_1}(T)}{\partial T} - \frac{1}{I_{Q_2}(T)}\frac{I_{Q_2}(T)}{\partial T}\right). \end{aligned} \tag{7.17}$$

Note that

$$I_{Q_1}(T) = I_{Q_3}(T) = I_{Q_2}(T) + I_{D,M_N}(T) = I(T). \tag{7.18}$$

If we further assume $I_{Q_2} >> I_5$, then we can simplify Equation 7.17 as

$$\begin{aligned} \frac{\partial V_{REF}}{\partial T} &= \frac{V_{BE_3}(T_{(nom)}) - V_{G0}}{T_{(nom)}} + (1-\rho)\frac{k}{q}\left(1 + \ln\left(\frac{T}{T_{(nom)}}\right)\right) + \frac{k}{q}M\ln N \\ &\quad + MV_T\left(\frac{1}{I_{Q_1}(T)}\frac{\partial I_{Q_1}(T)}{\partial T} - \frac{1}{I_{Q_2}(T)}\frac{\partial I_{Q_2}(T)}{\partial T}\right), \end{aligned} \tag{7.19}$$

where we assume the PTAT current $I_{Q_3}(T) = g_0 + g_1 T \approx g_1 T$ for $T >> 1$. If we substitute Equation 7.18 into Equation 7.19, we shall get

$$\begin{aligned}\frac{\partial V_{REF}}{\partial T} &= \frac{V_{BE_3}(T_{(nom)}) - V_{G0}}{T_{(nom)}} + (1-\rho)\frac{k}{q}\left(1 + \ln\left(\frac{T}{T_{(nom)}}\right)\right) + \frac{k}{q}M \ln N \\ &\quad + MV_T\left(\frac{1}{I(T)}\frac{\partial I(T)}{\partial T} - \frac{1}{I(T) - I_{D,M_N}(T)}\frac{\partial I(T) - I_{D,M_N}(T)}{\partial T}\right) \\ &\approx \frac{V_{BE_3}(T_{(nom)}) - V_{G0}}{T_{(nom)}} + (1-\rho)\frac{k}{q}\left(1 + \ln\left(\frac{T}{T_{(nom)}}\right)\right) + \frac{k}{q}M \ln N \\ &\quad + M\frac{V_T}{I(T)}\frac{\partial I_{D,M_N}(T)}{\partial T}. \end{aligned} \tag{7.20}$$

Note that Equation 7.12 yields

$$\frac{\partial I_{D,M_N}(T)}{\partial T} = a_1 + 2a_2(T - T_2),$$

which when substituted into Equation 7.20 yields

$$\begin{aligned}\frac{\partial V_{REF}}{\partial T} &\approx \frac{V_{BE_3}\left(T_{(nom)}\right) - V_{G0}}{T_{(nom)}} + (1-\rho)\frac{k}{q}\left(1 + \ln\left(\frac{T}{T_{(nom)}}\right)\right) + \frac{k}{q}M \ln N \\ &\quad + M\frac{V_T}{I(T)}(a_1 + 2a_2(T - T_2)).\end{aligned}$$

Our target is to set up the proper a_1 and a_2, such that there are two temperatures T_2 and $T_{(nom)}$ in the temperature range of interest $[T_{min}, T_{max}]$ with $T_{(nom)} < T_2$, and $\frac{\partial V_{REF}}{\partial T}|_{T=T_{(nom)}} = \frac{\partial V_{REF}}{\partial T}|_{T=T_2} = 0$. Comparing the coefficients implies the following two functions

$$\begin{aligned}F_1(T) &= \frac{V_{BE_3}\left(T_{(nom)}\right) - V_{G0}}{T_{(nom)}} + (1-\rho)\frac{k}{q}\left(1 + \ln\left(\frac{T}{T_{(nom)}}\right)\right) + \frac{k}{q}M \ln N, \\ F_2(T) &= M\frac{V_T}{I(T)}(a_1 + 2a_2(T - T_2)),\end{aligned}$$

have to satisfy

$$F_1(T_{(nom)}) = F_2(T_{(nom)}) = 0, \tag{7.21}$$

$$F_1(T_2) + F_2(T_2) = 0. \tag{7.22}$$

The constraint in the Equation 7.21 is the same as that of the conventional opamp based β-multiplier bandgap voltage reference circuit to achieve near-zero TC at $T_{(nom)}$. If this constraint is satisfied, the V_{REF} will exhibit a local maximum at $T = T_{(nom)}$. The additional constraint in Equation 7.22 will achieve a local minimum at $T = T_2$, through second order temperature compensation, since the coefficients a_1 and a_2 are functions of the size of the transistor M_5 and the resistance of R_3. For a given temperature dependent V_{REF} variation, Equations 7.21

and 7.22 can be applied to determine T_2, a_1, and a_2 which in turn will determine R_3 and S_{M_N} of M_N. When Equation 7.22 is satisfied, V_{REF} will exhibit a local minimum at $T = T_2$.

With a large number of design parameters in Equations 7.21 and 7.22, the best way to fit V_{REF} to a predetermined temperature response is to perform a least squares fitting which minimizes the sum of squares difference between the temperature characteristic of V_{REF} and the expected temperature characteristic curve. The typical targeted temperature characteristic curve is a constant over the temperature range of interest. Such a technique was first proposed in (Cave, 2005) for piecewise linear temperature compensation voltage reference circuit topology, and is general enough to take care of any practical situations. However, the above system of equations are high order functions of temperature, and therefore cannot be solved analytically. Instead, SPICE simulation has to be applied to perform the least squares fitting. In the worst case, trial and error calculations with SPICE simulations are performed manually to achieve a low temperature coefficient voltage reference circuit over a wide temperature range. However, the analytical analysis should always be performed to ensure that it is possible for the circuit topology under consideration to achieve the desired performance before going into the tedious trial and error design loop.

7.2.3 Current Addition

The current source in Figure 7.3(b) can be used in opamp based β-multiplier second order temperature compensated bandgap voltage reference circuit through current addition at node A (negative input node of the opamp), which has the same effect as current subtraction at node B (positive input node of the opamp) discussed in Section 7.2.2. Figure 7.6 shows a second order curvature compensated bandgap voltage reference schematic that makes use of the addition of second order temperature dependent current source. The $V_{REF}(T)$ obtained by this circuit has exactly the same form as that given by Equation 7.16, while $I_{Q_1}(T)$ is being modified in this circuit and is comparable to $I_{Q_2}(T)$ of Figure 7.5. The temperature sensitivity of the circuit can be analyzed in a similar manner as that in Section 7.2.2 with the assumption that $I_{Q_1} = I_1 + I_{D,M_P} >> I_{D,M_P}$, and $I_{Q_2} = I_{Q_3} = I_1 = I$. As a result,

$$\frac{\partial V_{REF}}{\partial T} \approx \frac{V_{BE_3}(T_{(nom)}) - V_{G0}}{T_{(nom)}} + (1-\rho)\frac{k}{q}\left(1 + \ln\left(\frac{T}{T_{(nom)}}\right)\right) + \frac{k}{q}M \ln N - M\frac{V_T}{I(T)}\left(d_1 + 2d_2(T_1 - T)\right),$$

where $I_{D,M_P}(T) = d_0 + d_1(T_1 - T)$ for $T < T_1$. Our target is to properly set up d_1 and d_2, such that there are two points T_1 and $T_{(nom)}$ in the temperature range of interest $[T_{min}, T_{max}]$ such that $T_{min} < T_1 < T_{(nom)}$, and $\frac{\partial V_{REF}}{\partial T}|_{T=T_{(nom)}} = \frac{\partial V_{REF}}{\partial T}|_{T=T_1} = 0$. By comparing the coefficients of the two differential equations, we shall obtain the following two functions

$$F_1(T) = \frac{V_{BE_3}\left(T_{(nom)}\right) - V_{G0}}{T_{(nom)}} + (1-\rho)\frac{k}{q}\left(1 + \ln\left(\frac{T}{T_{(nom)}}\right)\right) + \frac{k}{q}M \ln N,$$

$$F_3(T) = M\frac{V_T}{I(T)}(d_1 + 2d_2(T_1 - T)),$$

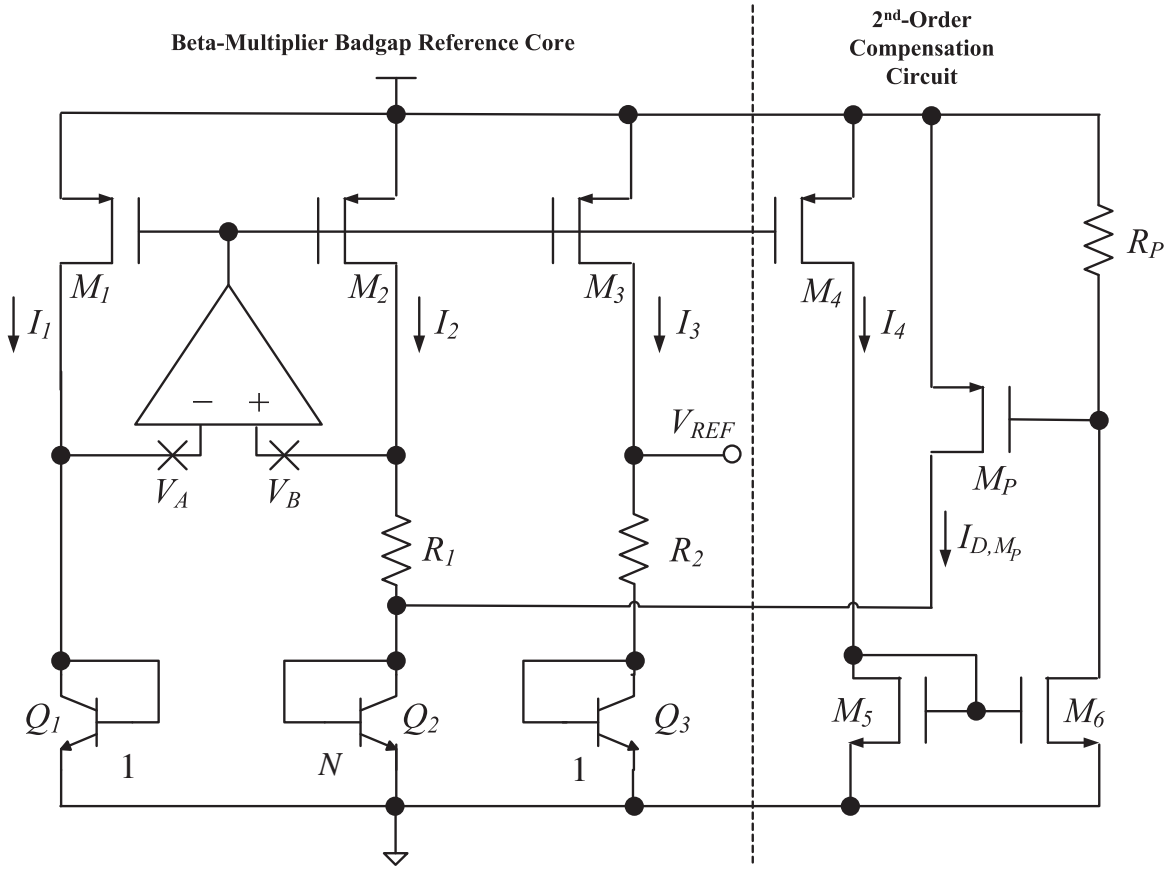


Figure 7.6 The schematic of second order temperature compensated voltage reference circuit by current addition with second order temperature characteristics.

which have to satisfy

$$F_1\left(T_{(nom)}\right) = F_3\left(T_{(nom)}\right) = 0, \tag{7.23}$$

$$F_1(T_1) - F_3(T_1) = 0. \tag{7.24}$$

$F_1(T)$ is exactly the same as that in Section 7.2.2. As a result, satisfying Equation 7.23 will produce a V_{REF} with a local maximum at $T = T_{(nom)}$. The function $F_3(T)$ has the same form as that of $F_2(T)$ in Section 7.2.2 with a_k changed to d_k, and T_2 changed to T_1. When Equation 7.24 is satisfied, V_{REF} will exhibit a local minimum at $T = T_1$, since the coefficients d_1 and d_2 are functions of the size of the transistor M_P and the resistance of R_P. Thus, for a given temperature dependent V_{REF} variation, Equations 7.23 and 7.24 can be applied to determine T_1, d_1, and d_2 which in turn will determine R_P and S_{M_P} of M_P. Similar to the discussions in Section 7.2.2, the least squares fitting method can be applied to determine the best R_P and S_{P_1}, although the trial and error method using SPICE simulation will be more convenient in practice.

7.3 BJT Current Subtraction

As discussed in the introduction of Section 7.2, a current source with second order temperature dependency can be conveniently obtained by the BJT in the same way as that in the output stage of the opamp based β-multiplier bandgap voltage reference circuit. (The second-order temperature dependent nature of the BJT V_{BE} voltage is one of the major reasons why there is a need to implement second order temperature compensation to obtain a low TC reference voltage over a wide temperature range.) When this BJT current source is appropriately connected to the voltage reference circuit, it forms a current sink and hence functions as second order current subtraction circuit to achieve second order curvature correction similar to that in Section 7.2.2. Consider the schematic of the opamp-based β-multiplier bandgap voltage reference circuit in Figure 7.7 with the BJT current subtraction, which is first discussed in (Gunawan *et al.*, 1993). The resistors in the circuit satisfy $R_3 = R_8$, $R_4 = R_7$, and $R_5 = R_6$. The emitter areas of Q_1, Q_2, Q_3, and Q_4 are in the ratio of $1 : N : 1 : 1$. Note that the negative feedback configured opamp will bias the input voltages to be the same, thus

$$V_A = V_B.$$

Therefore, with $R_5 = R_6$, the currents that flow through R_5 and R_6 will be the same and equal to I_2. Assume the opamp is ideal, no current will be flowing in/out of V_+ and V_-. As a result,

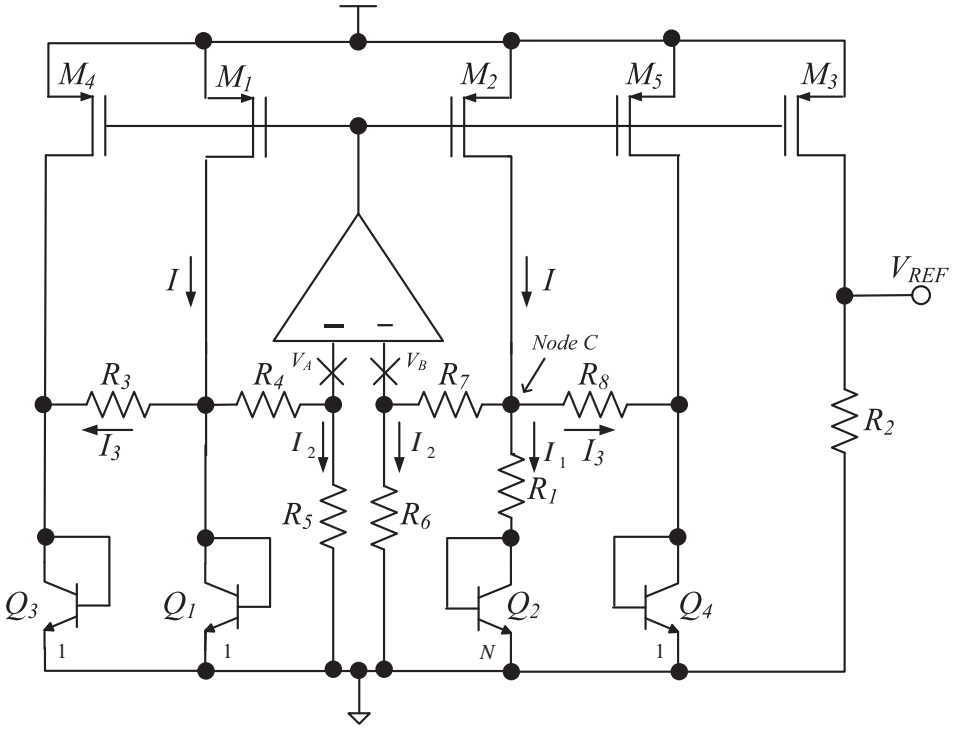


Figure 7.7 The schematic of opamp based β-multiplier bandgap voltage reference circuit with BJT current subtraction to achieve second order curvature correction (Gunawan *et al.*, 1993).

the currents that flow through R_4 and R_7 will be the same, hence

$$\begin{aligned} V_A = V_{BE_1} + I_2 R_4 &= I_2 R_7 + I_1 R_1 + V_{BE_2} = V_B \\ V_{BE_1} &= +I_1 R_1 + V_{BE_2} \\ I_1 &= \frac{V_{BE_1} - V_{BE_2}}{R_1} \\ I_1 &= \frac{\Delta V_{BE_{1,2}}}{R_1} \\ I_1 &= \frac{\ln(N)}{R_1} V_T. \end{aligned}$$

Assume the opamp has infinite input impedance, where the input currents are close to zero. Therefore the current flowing through R_4 equals that of R_5. Similarly, the current flowing through R_7 equals that of R_1. As a result,

$$I_2 = \frac{1}{R_4 + R_5} V_{BE_1}.$$

Furthermore, if $S_4 = S_1 = S_2 = S_5$, then the current mirror formed by M_4, M_1, M_2, and M_5 will have the same current flowing through each MOSFET. Since $A_{E_3} = A_{E_4}$, and $I_{Q_3} = I_{Q_4}$, therefore,

$$V_{BE_3} = V_{BE_4}.$$

As a result, the currents that flow through R_3 and R_8 will be the same, and equal I_3. If we consider the KVL of Q_1, R_3 and Q_3, which yields

$$\begin{aligned} I_3 R_3 + V_{BE_3} &= V_{BE_1} \\ I_3 &= \frac{V_{BE_1} - V_{BE_3}}{R_3} \\ I_3 &= \frac{\Delta V_{BE_{1,3}}}{R_3} \\ I_3 &= \frac{\ln\left(T/T_{(nom)}\right)}{R_3} V_T. \end{aligned}$$

The KCL at node C implies $I = I_1 + I_2 + I_3$, and the current mirror pair formed by M_2 and M_3 copies the current to the output branch. By selecting $S_2 = S_3$, we shall obtain

$$\begin{aligned} V_{REF} &= I R_2 \\ &= \left(\frac{\ln(N)}{R_1} V_T + \frac{1}{R_4 + R_5} V_{BE_1} + \frac{\ln(T/T_{(nom)})}{R_3} V_T \right) R_2 \\ &= \frac{R_2}{R_4 + R_5} \left(\left(\frac{R_4 + R_5}{R_1} \ln(N) \right) V_T + V_{BE_1} \right. \\ &\quad \left. + \left(\frac{R_4 + R_5}{R_3} \ln\left(\frac{T}{T_{(nom)}} \right) \right) V_T \right). \end{aligned} \tag{7.25}$$

We may express Equation 7.25 as

$$\begin{aligned} V_{REF} &= K_1 \left(K_2 V_T + V_{BE_1} + K_3 \ln(T/T_{(nom)}) V_T \right) \\ &= K_1 \left(V_{REF\text{-}CONV} + K_3 \ln(T/T_{(nom)}) V_T \right), \end{aligned} \tag{7.26}$$

where $K_1 = \frac{R_2}{R_4+R_5}$, $K_2 = \frac{R_4+R_5}{R_1} \ln(N)$ and $K_3 = \frac{R_4+R_5}{R_3}$. We can observe that K_2 is equivalent to the factor M in the conventional $V_{REF-CONV}$ given by Equation 3.5. Furthermore, it is clear that when $T = T_{nom}$ the voltage reference obtained by Equation 7.26 will have the same form as that of the conventional bandgap voltage reference circuit at $T_{(nom)}$. As a result, at least in theory the voltage reference circuit in Figure 7.7 has compatible performance at $T = T_{(nom)}$ with that of the conventional opamp-based β-multiplier bandgap voltage reference circuit in Figure 3.8 discussed in Chapter 3. At other temperatures, the high order temperature dependent term $K_3 \ln(T/T_{(nom)})V_T$ will compensate the second order temperature dependent term of V_{BE_1}. This is achieved by an appropriate selection of the resistor R_3 to drive Q_3. Consider the case of $\theta = 1$ (the reader should refer to Section 1.1). As a result,

$$\begin{aligned} \frac{R_4 + R_5}{R_3} &= \rho - 1 \\ R_3 &= \frac{R_4 + R_5}{\rho - 1}, \end{aligned}$$

can be chosen to achieve high order curvature compensation.

Note that the high order temperature dependent term $K_3 \ln(T/T_{(nom)})V_T$ has the same form as curve C in Figure 7.2, thus the high order curvature corrected V_{REF} in Equation 7.26 will behave similarly to Figure 7.2(c).

7.4 Piecewise Linear Compensation

The second order temperature compensation of the opamp based β-multiplier bandgap voltage reference circuit by both the addition/subtraction of a current sink/source with high order temperature coefficients has been shown to be able to achieve a reference voltage with low *TC* in Section 7.2. As a result, it is tempting to consider the application of both addition and subtraction of currents with high order temperature dependency to achieve a reference voltage with low *TC* over an even wider temperature range than those in Section 7.2.

Such temperature compensation technique is known as the piecewise linear compensation method. To understand how to achieve piecewise linear compensation, let's consider the temperature compensation topology of various curvature compensation techniques of the opamp based β-multiplier bandgap voltage reference circuit that we've studied so far, and which is summarized in Figure 7.8. With reference to Figure 7.8, the conventional opamp based β-multiplier voltage reference circuit has $k_1 = 1$, $k_2 = M$, $k_3 = k_4 = 0$. The second order compensated voltage reference circuit in Section 7.2.3 has $k_1 = 1$, $k_2 = M$, $k_3 = \phi_1$, and $k_4 = 0$, where ϕ_1 is the scaling constant of the second order temperature dependent source $n_1(T)$. The second order compensated voltage reference circuit in Section 7.2.2 has $k_1 = 1$, $k_2 = M$, $k_3 = 0$, and $k_4 = \phi_2$. These two high order temperature compensated voltage

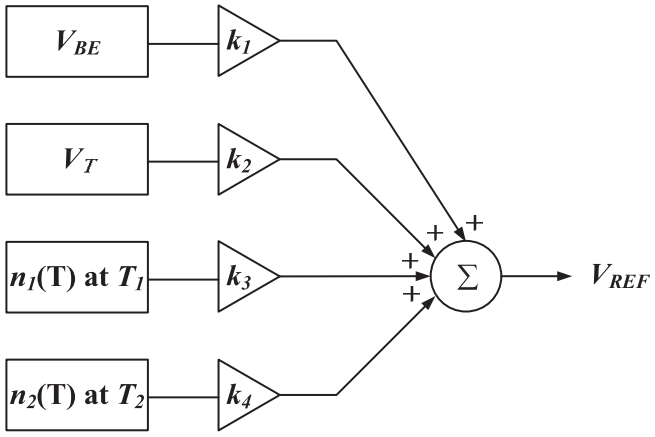


Figure 7.8 A topological overview of a three-section curvature corrected opamp based β-multiplier bandgap voltage reference by the addition of two second order temperature dependent voltage sources.

reference circuits have illustrated the piecewise compensation technique with two distinguished temperature regions, which are $[T_{min}, T_1]$ and $[T_1, T_{max}]$ for the circuit in Section 7.2.2, and the temperature compensation result will behave like Figure 7.2(a). In the case of the voltage reference circuit in Section 7.2.3, the temperature regions are $[T_{min}, T_2]$ and $[T_2, T_{max}]$, and the temperature compensation result will behave like Figure 7.2(c). The piecewise linear compensation method will allow an arbitrary k_1, k_2, k_3, k_4, $n_1(T)$, $n_2(T)$, T_1, and T_2. As a result, a three-section temperature compensation voltage reference circuit can be achieved by selecting $k_1 = 1$, $k_2 = M$, $k_3 = \phi_1$, and $k_4 = \phi_2$ in Figure 7.8. The temperature region of interest is divided into three distinguished regions $[T_{min}, T_1]$, $[T_1, T_2]$, and $[T_2, T_{max}]$ as shown in Figure 7.8. The temperature compensation result will behave like Figure 7.2(b).

The piecewise compensation will allow an arbitrary k_1, k_2, k_3, and k_4, $n_1(T)$, $n_2(T)$ and T_1, T_2. As discussed at the end of Section 7.2.2, with such a large number of parameters, the best way to fit such a large number of parameters to achieve a reference voltage with a pre-determined temperature response is to perform a least squares fitting that minimizes the sum of squares difference between the temperature varying V_{REF} and the desired V_{REF}.

However, being too general also means that a lot of design freedom is required to implement the obtained voltage reference. In reality, not only do such design freedoms not exist, there are usually added design constraints due to the nature of the second order curvature correction sources n_1 and n_2. Fortunately, the divide and conquer method can be applied to simplify the design. Knowing that the two second order current sources $n_1(T)$ and $n_2(T)$ will act at different temperature regions, we can therefore make use of the results in previous sections (Section 7.2.2 and 7.2.3) to help to design k_1, k_2, k_3, k_4, T_1, and T_2. However, in order to achieve the lowest TC, the reference voltage against temperature should exhibit equal ripple property to that shown in Figure 7.9. As a result, in addition to the alternative slope, and the maximum and minimum saddle points requirements in Equations 7.21, 7.22, 7.23, and 7.24, we shall also have the V_{REF} obtained in Section 7.2.2 at T_2 has the same voltage as the V_{REF} obtained in Section 7.2.3 at T_1. Such that the equal ripple property will be fulfilled.

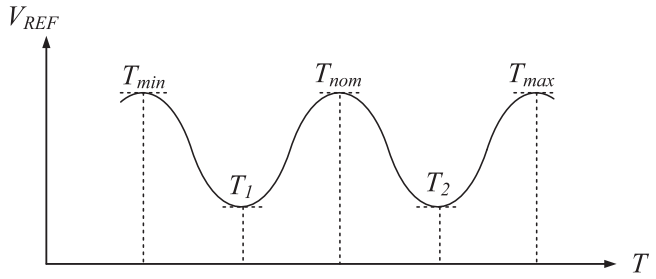


Figure 7.9 Illustration of the piecewise temperature compensated reference voltage with three sections, where the obtained reference voltage exhibits equal ripple property.

Let $V_{REF1}(T)$ be the V_{REF} obtained by the circuit in Figure 7.5 in Section 7.2.2, and $V_{REF2}(T)$ be the V_{REF} obtained by the circuit in Figure 7.6 in Section 7.2.3. In that case, the equal ripple constraint can be stated as

$$V_{REF1}(T_2) = V_{REF2}(T_1). \tag{7.27}$$

Furthermore, at the two ends of the of the temperature range of interest $[T_{max}, T_{min}]$, we shall have

$$V_{REF_1}(T_{max}) = V_{REF_2}(T_{min}). \tag{7.28}$$

The obtained $V_{REF}(T)$ will exhibit equal ripple property as shown in Figure 7.9. Collaboratively, Equations 7.21, 7.22, 7.23, 7.24, 7.27, and 7.28 will be the complete design constraint for the temperature compensation topology in Figure 7.8 to achieve the lowest temperature coefficient. The overall schematic that implements the temperature compensation topology in Figure 7.8 is shown in Figure 7.10, which is clearly a marriage of the two schematics in Figures 7.5 and 7.6.

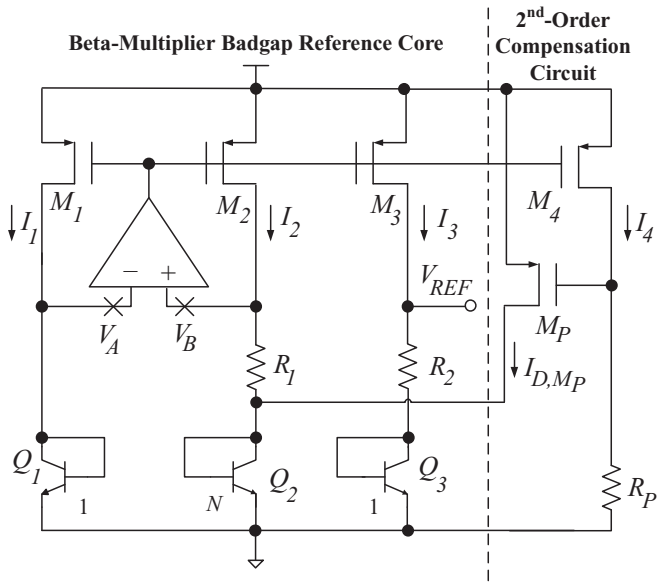


Figure 7.10 Illustration of I_{NL} of the piecewise compensated bandgap voltage reference circuit.

7.5 Sum and Difference of Sources with Similar Temperature Dependence

The first order temperature compensated voltage reference circuit that sums the PTAT and CTAT sources has been shown to be able to obtain a reference voltage with a concave temperature dependency. It is this concave shaped temperature characteristic that helps to provide the low temperature coefficient within a limited temperature region (with reference to the approximation theory, three extremes are required to provide the best 2^{nd} order polynomial approximation). Previous sections have discussed adding various high order temperature dependent voltage/current sources to the core of the opamp based β-multiplier bandgap voltage reference circuit to achieve a reference voltage with low temperature coefficient over a wide temperature range. On the other hand, it seems to be more intuitive to add a properly scaled downward curvature first order temperature compensated voltage to a upward curvature first order temperature compensated voltage as shown in Figure 7.11(a) to obtain a high order curvature corrected reference voltage. In a similar analogy, a properly scaled downward curvature first order temperature compensated voltage can be subtracted from a first order temperature compensated voltage as shown in Figure 7.11(b) to obtain a high order curvature corrected reference voltage. Actually, a general temperature compensation voltage reference circuit involves the mutual compensation of voltage sources of similar temperature dependent. The voltage reference circuit that makes use of NPN BJT and PNP BJT will provide two voltage sources with a concave temperature dependence characteristic that are a shift from each other, and hence similar. When these two voltage sources are subtracted from each other, a low *TC* reference voltage over a wide temperature range can be obtained. Such implementation is very straightforward, and can be applied to any voltage reference circuit. As a result, if sub-1V voltage reference circuits are applied to generate the voltage sources with similar temperature dependence, we shall easily obtain a low *TC* sub-1V reference voltage. In the following, we shall discuss the detailed design of such a voltage reference circuit, where the opamp based β-multiplier sub-1V voltage reference circuit discussed in Section 6.3.1 will

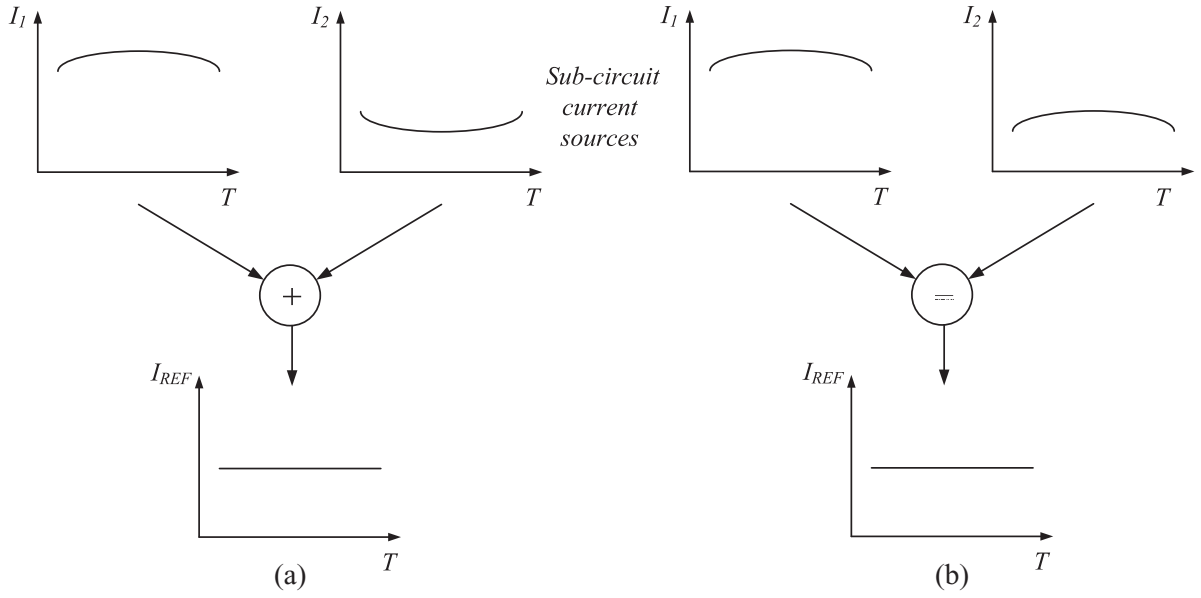


Figure 7.11 Mutual compensation of voltages with similar temperature dependence: (a) voltage addition, (b) voltage subtraction.

be applied to generate the voltage sources with similar temperature dependency. The pros and cons of this voltage reference circuit will be discussed in detail. The design flexibility of this voltage reference circuit is traded for power efficiency in Section 7.5.3, where voltage sources with similar temperature dependency are obtained from thermal devices with similar but inversely dependent temperature characteristics.

7.5.1 Difference of Voltages with Similar Temperature Dependence

To understand and analyze the design and implementation of mutual compensation of voltage sources with similar temperature dependency using conventional opamp based β-multiplier bandgap voltage reference circuit, we shall consider a particular implementation by (Ker *et al.*, 2006). The sub-1V opamp based β-multiplier bandgap voltage reference by resistive sub-division presented in Section 6.3.1 can be applied to design sub-circuit 1 shown in Figure 7.12. The current $I_{DS_{3,PNP}}$ will have the characteristic concave shape with respect to the temperature as investigated in Section 6.3.1. If a temperature compensation scheme by current subtraction is applied, the similar temperature dependent source should be a current source of concave shape with respect to temperature which is a shift of that of sub-circuit 1. The method presented in Ker *et al.* (2006) to obtain such a shifted current source is by the use of opamp based β-multiplier bandgap voltage reference circuit constructed with NPN transistors as shown in sub-circuit 2 in Figure 7.12. While the derivation of the operation of the sub-1V current source in sub-circuit 2 is left as exercise for the reader in Chapter 5, it should not be difficult for the reader to understand that $I_{M_{3,NPN}}$ is given by

$$I_{M_{3,NPN}} = \frac{1}{R_{1,NPN}} \left(V_{BE_{1,NPN}} + \frac{R_{1,NPN}}{R_{3,NPN}} V_T \ln N_{NPN} \right). \tag{7.29}$$

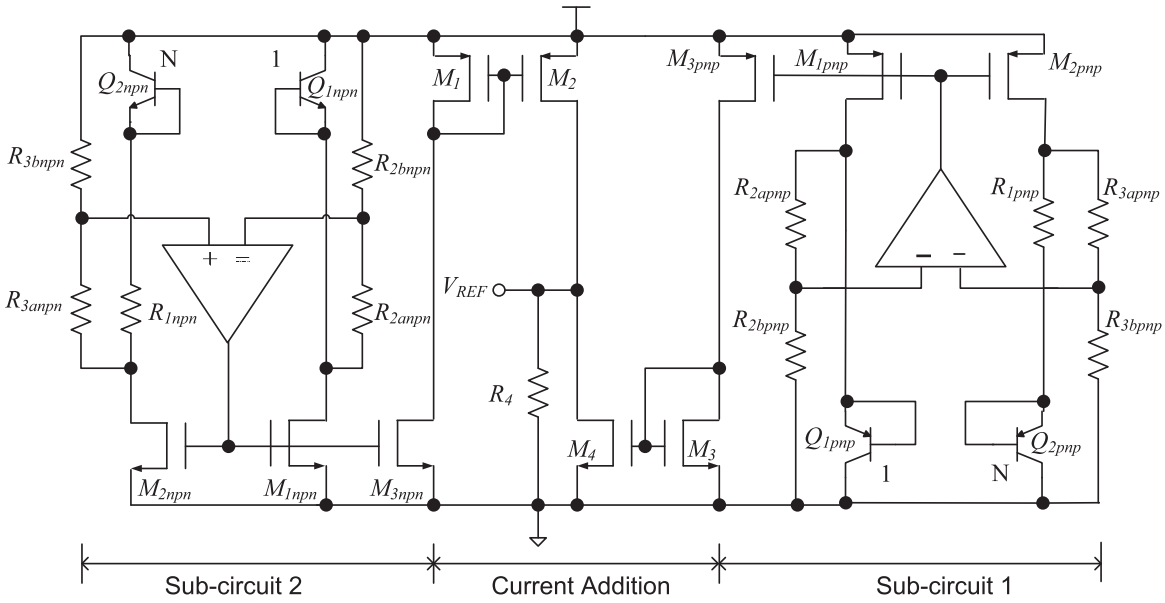


Figure 7.12 Sub-1V bandgap voltage reference by resistive sub-division with NMOS transistors current mirror based β-multiplier, and the complete schematic (Ker *et al.*, 2006).

Similarly, we have derived in Section 6.3.1 that $I_{M_{3,PNP}}$ is given by

$$I_{M_{3,PNP}} = \frac{1}{R_{1,PNP}} \left(V_{BE_{1,PNP}} + \frac{R_{1,PNP}}{R_{3,PNP}} V_T \ln N_{PNP} \right). \tag{7.30}$$

It is clear from the equation that $I_{M_{3,NPN}}$ has a similar temperature dependence as that of $I_{M_{3,PNP}}$ scaled by a factor K and a temperature shift. If both currents are designed to achieve zero temperature coefficients at $T_{(nom)}$, then the difference between $K I_{M_{3,NPN}}$ and $I_{M_{3,PNP}}$ will has a very low temperature sensitivity. The scaling factor K can be achieved by simple current mirror as shown in the current addition sub-circuit in Figure 7.12. By selecting $S_1 : S_2 = 1 : K$, and $S_3 = S_4$, the output V_{REF} in Figure 7.12 is given by

$$\begin{aligned} V_{REF} &= R_4(K I_{REF,NPN} - I_{REF,PNP}) \\ &= R_4 \left(\left(\frac{K}{R_{1,NPN}} - \frac{1}{R_{1,PNP}} \right) \left(V_{BE_1,NPN} - V_{BE_1,PNP} \right) \right. \\ &\quad \left. + V_T \left(\frac{K \ln N_{NPN}}{R_{3,NPN}} - \frac{\ln N_{PNP}}{R_{3,NPN}} \right) \right). \end{aligned} \tag{7.31}$$

Knowing that the temperature dependence of $V_{BE_{1,NPN}}$ is similar to that of $V_{BE_{1,PNP}}$, therefore $V_{BE_{1,NPN}} - V_{BE_{1,PNP}}$ will be a temperature independent term, and hence is V_{REF} obtained in Equation 7.31. To investigate the minimum operating voltage of this voltage reference circuit, we observed that the minimum supply voltage of the circuit in Figure 7.12 is the maximum of that of the sub-circuits 1 and 2 in Figure 7.12. Both sub-circuits have a minimum operating voltage lower than 1 V. As a result, the voltage reference circuit in Figure 7.12 is also a sub-1V voltage reference circuit.

This topologically simple voltage reference circuit does pose several design difficulties. The design problems include the search of the scaling factor K, and the mismatch of the temperatures that achieve zero *TC* between the two bandgap voltage reference sub-circuits. While trimming the current mirror formed by M_1 and M_2 can be applied to adjust K, post-fabrication adjustment of the zero *TC* temperature of the bandgap voltage reference sub-circuit may jeopardize the concave shape of the temperature characteristics of $I_{REF,NPN}$ and/or $I_{REF,PNP}$, and hence created another curvature error source that affects the minimization of the temperature coefficient of the overall obtained reference voltage over a wide temperature range. To avoid this problem, it may be wise for us to use sub-circuits that have the same circuit topology. The following section will discuss the generation of current sources with concave and convex temperature characteristics using the same bandgap voltage circuit topology.

7.5.2 Sum of Voltages with Inverted Temperature Dependence

The conventional opamp based β-multiplier bandgap voltage reference circuit will produce a reference voltage with a concave shape with respect to the temperature. The sum of voltages with similar temperature dependence to obtain a near-zero *TC* reference voltage would require another opamp based β-multiplier bandgap voltage reference circuit that generates a reference voltage with a convex (or downward concave) shape with respect to the temperature. This can

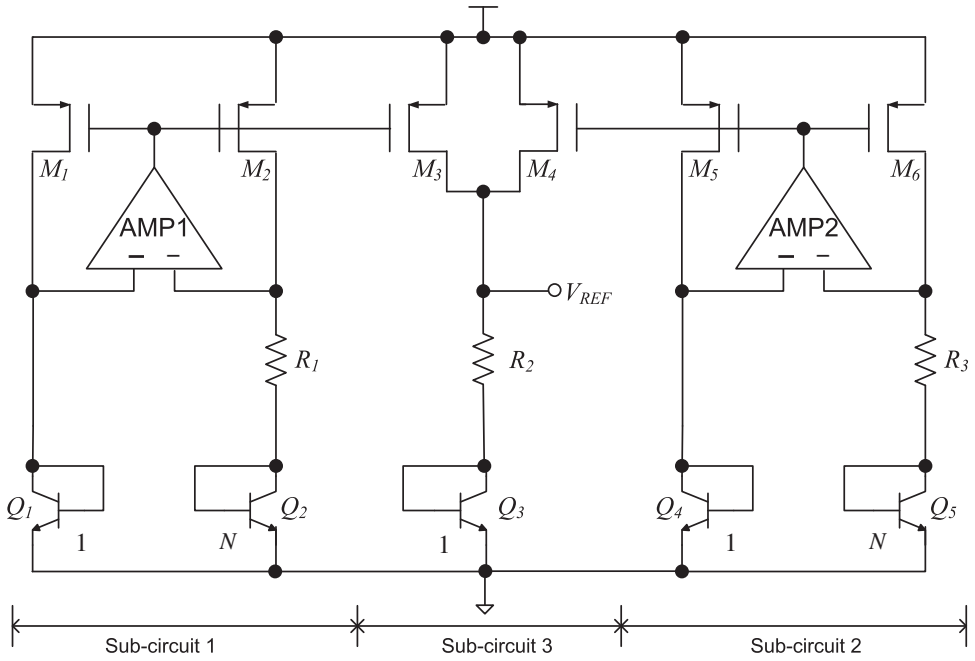


Figure 7.13 Schematic of a high order temperature compensated voltage reference circuit by sum of current sources with inverted temperature property (Zhou *et al.*, 2006).

be achieved by making use of resistors with different temperature property in the conventional opamp based β-multiplier bandgap voltage reference circuit.

To invert the concave shaped temperature dependence of the reference voltage obtained by the bandgap voltage reference circuit from downward to upward, we shall make use of resistors with different temperature properties. Consider the voltage reference circuit in Figure 7.13, which is formed by three sub-circuits. Sub-circuits 1 and 2 are conventional opamp based β-multiplier current sources with R_1 and R_3 implemented by non-silicide $N+$ poly resistor and non-silicide $P+$ diffused resistor, which have T_{CR} equal -1350 ppm/°C and 1410 ppm/°C, respectively. These two resistors not only have inverted temperature coefficients, they also have close absolute values z of the T_{CR}. Consider the resistor value of R_1 and R_3 expanded at $T = T_0$.

$$R_1(T) = R_1(T_0)(1 - \lambda_1(T - T_0)), \tag{7.32}$$

$$R_3(T) = R_3(T_0)(1 + \lambda_0(T - T_0)), \tag{7.33}$$

where λ_1 and λ_0 are the absolute value of the temperature coefficients of R_1 and R_3, respectively. With sub-circuits 1 and 2 are conventional opamp based β-multiplier bandgap voltage reference circuits and sub-circuit 3 is a current adder, the voltage reference circuit in Figure 7.13 yields

$$V_{REF} = \left(\frac{1}{R_1} + \frac{1}{R_3}\right) R_2 \ln(N) V_T + V_{BE_3}.$$

We notice that by equating the differentiation of V_{REF} with respect to T to zero at $T = T_{(nom)}$

$$\left.\frac{\partial V_{REF}}{\partial T}\right|_{T=T_{(nom)}} = \left(\frac{1}{R_1} + \frac{1}{R_3}\right) R_2 \ln(N) \left.\frac{\partial V_T}{\partial T}\right|_{T=T_{(nom)}} + \left.\frac{\partial V_{BE_3}}{\partial T}\right|_{T=T_{(nom)}} = 0,$$

will give us the resistor ratio to obtain a near-zero TC reference voltage at $T = T_{(nom)}$. In particular

$$\left.\frac{\partial^2 V_{REF}}{\partial T^2}\right|_{T=T_{(nom)}} = \left(\frac{1}{R_1} + \frac{1}{R_3}\right) R_2 \ln(N) \left.\frac{\partial^2 V_T}{\partial T^2}\right|_{T=T_{(nom)}} + \left.\frac{\partial^2 V_{BE_3}}{\partial T^2}\right|_{T=T_{(nom)}} \leq 0. \quad (7.34)$$

Since $\left.\frac{\partial^2 V_T}{\partial T^2}\right|_{T=T_{(nom)}} > 0$, therefore, it is clear that there exists factor A such that

$$A R_2 \ln(N) \left.\frac{\partial^2 V_T}{\partial T^2}\right|_{T=T_{(nom)}} + \left.\frac{\partial^2 V_{BE_3}}{\partial T^2}\right|_{T=T_{(nom)}} \geq 0. \quad (7.35)$$

As a result, we can design V_{REF1} obtained by sub-circuits 1 and 3 to follow Equation 3.12. Similarly, V_{REF2} can be obtained by sub-circuits 2 and 3 that have the near-zero TC reference voltage at $T_{(nom)}$ while the second order derivative of V_{REF2} has the opposite sign. Obviously this can be achieved with A given by $\frac{1}{R_1}$ that satisfies Equation 7.35, R_1 given Equation 7.32, and R_3 given by Equation 7.33. With sub-circuit 3 acts as a current sum circuit, as a result, the circuit will generate V_{REF} being a linear compensation of V_{REF1} and V_{REF2}. The similarity between the temperature dependence of sub-circuits 1 and 2 can be adjusted by M_3 and M_4, which will in turn adjust the current mirrors containing M_3 and M_4 to alter the current values of the current sources from sub-circuits 1 and 2, respectively. Such voltage reference circuit is first proposed in (Zhou *et al.,* 2006; Figure 7.13). Theoretically, this voltage reference circuit has a similar curvature correction property as that in Section 7.5.1. However, since the same circuit topology is applied to generate the voltage sources of similar temperature dependence in this circuit, while different circuit topologies are applied to generate the voltage sources of similar temperature dependence in the voltage reference circuit in Section 7.5.1, as a result, this voltage reference circuit will suffer less from the device mismatch compensation error problem and hence can achieve higher performance.

7.5.3 Multi-threshold Voltages Curvature Compensated Voltage Reference

The mutual compensation of voltage/current sources with similar temperature dependence can produce reference voltages with very low temperatures. The drawback is the increase in quiescent current of the voltage reference circuit. Note that each temperature dependent voltage/current source is generated by one sub-circuit. In the case of Sections 7.5.1 and 7.5.2, each sub-circuit is itself a conventional opamp based β-multiplier bandgap voltage reference circuit. Therefore, the mutual compensation of voltage/current sources with similar temperature dependency voltage reference circuits in Sections 7.5.1 and 7.5.2 will be more than twice that of the conventional opamp based β-multiplier bandgap voltage reference circuit. The high power consumption will not only prohibit the implementation of the mutual compensation of voltage/current sources with similar temperature dependence in power source limited applications, such as battery operated devices, etc., it will also cause self-heating and thus lower the temperature coefficient of the voltage reference circuit in actual implementation when compared to that obtained from analytic analysis.

A typical method to lower the power consumption of the mutual compensation of voltage sources with similar temperature dependence is to make use of device characteristics obtained

from different devices that have similar temperature dependence instead of complicated circuits that generate voltage sources with similar temperature dependence. One of such device characteristic is the threshold voltage of MOSFETs. The application of the threshold voltage of MOSFET to design voltage reference circuits has been discussed in Section 5.3. Similar to Section 5.3, the V_{th} of the MOSFETs can be applied to construct CTAT current source for the design of a BJT free voltage reference circuit. However, the threshold voltage is highly process dependent and temperature sensitive. Thus a relative value rather than an absolute one should be used, such that mutual compensation between the V_{th} of two devices will alleviate the process variation problem. As discussed in Section 1.2.4.1, the threshold voltage can be obtained from the differential gate-source voltage of MOSFETs biased at the saturation region. If there exists MOSFETs that have different threshold voltages with similar temperature dependence, and the threshold voltages are tightly controlled in the fabrication process, then, subtracting the threshold voltage of one MOSFET from the other will yield a constant voltage difference which can be used as a reference voltage. Since the threshold voltages of the MOSFETs fabricated by a similar process with different doping will have similar temperature dependence, therefore subtracting the threshold voltages will help to nullify the high order temperature coefficients by mutually compensating the high order temperature coefficients of the threshold voltages as discussed in Section 7.5.1. Another benefit of subtracting the threshold voltage is that it will hopefully nullify the process variation problem of the threshold voltage at the same time, as we have already discussed earlier in this paragraph.

In the age of multi-threshold voltages CMOS process being expensive, the threshold voltage difference obtained from the MOSFET in enhancement mode and in depletion mode can be used to generate near-zero *TC* voltage reference (Song and Kim, 1993). Nowadays, MOSFETs with different threshold voltages can be easily obtained via a multi-threshold voltages process, in which an additional implantation is involved to tailor the threshold voltage of the selected transistors. As a result, voltage reference circuits can be constructed from the threshold voltage difference extracted from the gate-to-source voltage (V_{GS}) of the transistors fabricated with different threshold voltages. Although the absolute value of the extracted threshold voltage is not easy to get accurate, the relative accuracy of the threshold voltage difference is shown to be fairly high in (Maloberti, 2001), hence it can be used to generate an accurate reference voltage.

Figure 7.14 shows the circuit generating the threshold voltage difference from transistors M_1 and M_2 (where a similar circuit has been presented in (Ugajin *et al.*, 2002), and is a modification from the voltage reference circuit proposed in (Blauschild *et al.*, 1978) to work with enhanced MOSFET devices alone). The transistors M_1 and M_2 have different threshold voltages, V_{th_1} and V_{th_2}, respectively. These transistors are biased at saturation. As a result, the gate-to-source voltage drop of the two transistors is equal to V_{th_1} and V_{th_2} on M_1 and M_2, respectively. Hence, the positive input of the opamp is $-V_{th_1}$. Assume the opamp is ideal, the feedback loop formed by the opamp and M_2 will guarantee the voltages at the positive input terminal and the negative terminal to be identical, and thus

$$\begin{aligned} V_{REF} - V_{th_2} &= -V_{th_1} \\ V_{REF} &= -V_{th_1} + V_{th_2}, \end{aligned} \tag{7.36}$$

where the gate-to-source voltage drop of M_2 is $-V_{th_2}$.

This circuit works with any current source. Assume a low voltage opamp is being applied in the schematic in Figure 7.14, a sub-1V voltage reference circuit can be easily obtained by

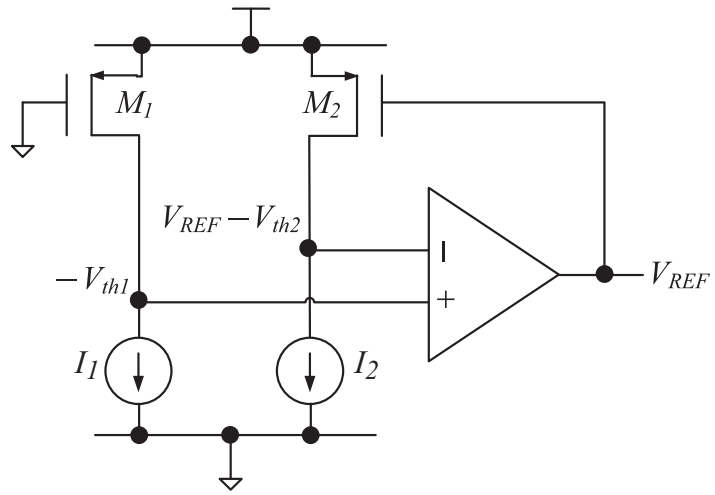


Figure 7.14 Threshold difference reference circuit (a modified voltage reference circuit from (Ugajin, 2002)).

making use of peak current sources to generate I_1 and I_2. Figure 7.15 shows the schematic of the complete voltage reference circuit with the core as that in Figure 7.14. The two current sources I_1 and I_2 can be made the same by choosing $S_3 = S_4$. Furthermore, the two transistors M_1 and M_2 have to be biased to work at saturation. As a result, we can choose S_3 and S_4 appropriately, such that $I_1 = I_2 = 6\,\mu$A in the process under concern. Such a multi-threshold voltages temperature compensated voltage reference circuit is simple and can provide reference voltages with low *TC*. It has been demonstrated as able to achieve 33.8 ppm/°C over a wide temperature range of −50 °C to 75 °C by (Song and Kim, 1993). However, this method still has

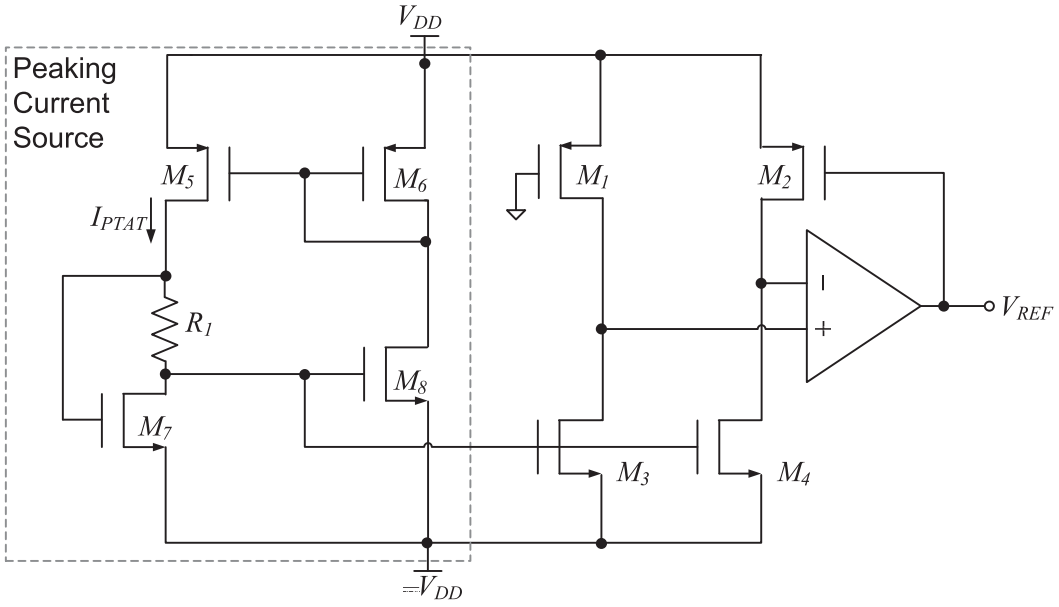


Figure 7.15 Schematic of the mutual compensation of voltage sources with similar temperature dependency voltage reference circuit based on the multi-threshold voltages MOSFETs (a modified voltage reference circuit from (Ugajin, 2002)).

several drawbacks. First, although the multiple threshold voltages process is not as expensive as before, it does require some special process steps which are not often available in standard CMOS processes. Second, the absolute output voltage is not easy to control because of the variation in the extra implantation steps required to obtain multiple threshold voltages. Post-fabrication processing is often required to adjust the final value of the reference voltage. Last, a dual supply is required for this circuit (note that the supply voltage in Figure 7.15 is $\pm V_{DD}$), which is not easily available in a lot of applications, such as battery operated systems. Nevertheless, the dual supply will also mean small supply voltage headroom.

In the next section, we shall show you how to obtain a mutual compensation of voltage sources with similar temperature dependence voltage reference constructed with a differential threshold voltage similar to that of Equation 7.36 obtained from the intrinsic threshold voltage difference between $V_{th,n}$ and $V_{th,p}$ of NMOS and PMOS, respectively. Similar to the multi-threshold voltages process, the threshold voltage of P-channel and N-channel MOSFETs in the standard CMOS process tends to vary in the same direction and thus can form a pair of voltage sources with similar temperature dependence.

7.5.3.1 Threshold Voltage Difference between PMOS and NMOS

The PMOS and NMOS transistors are the intrinsic multi-threshold voltages MOSFETs in all commercial CMOS processes. This section will present a multi-threshold voltages based voltage reference circuit using the difference between the threshold voltages of PMOS and NMOS, which has a simple circuit, low power consumption, and a small silicon layout area. To achieve the above design criteria, opamp cannot be applied in the voltage reference circuit. The core of PMOS and NMOS threshold voltages extraction circuit is shown in Figure 7.16, where M_6 and M_7 are PMOS and NMOS transistors respectively. Assume the current flowing through

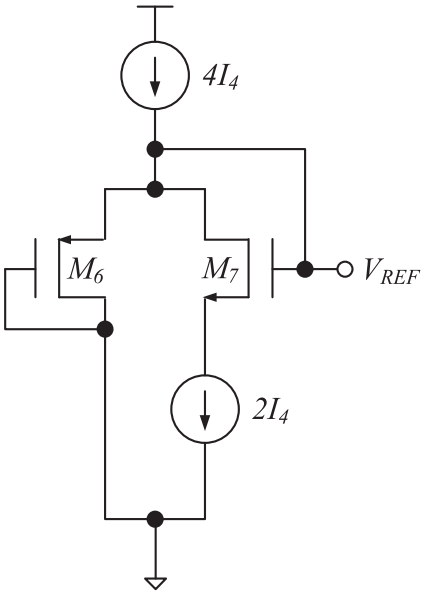


Figure 7.16 Schematic of the voltage reference core circuit based on the PMOS and NMOS threshold voltage differences (Kong, 2007).

the two transistors is the same, and both transistors are biased at saturation. As a result V_{REF} is given by

$$\begin{aligned} V_{REF} &= V_{GS_6} - V_{GS_7} \\ &= V_{th,p} + \sqrt{\frac{2I_4}{\mu_p C_{ox,p} S_6}} - V_{th,n} - \sqrt{\frac{2I_4}{\mu_n C_{ox,n} S_7}} \\ &= V_{th,p} - V_{th,n} + \sqrt{2I_4}\left(\frac{1}{\sqrt{\mu_p C_{ox,p} S_6}} - \frac{1}{\sqrt{\mu_n C_{ox,n} S_7}}\right) \qquad (7.37) \\ &= V_{th,p} - V_{th,n}, \qquad (7.38) \end{aligned}$$

where I_4 is assumed to be small, and thus the square root of I_4 is even smaller. Furthermore, S_6 and S_7 are designed to be large such that the terms inside the brackets in Equation 7.38 is practically zero.

To construct a sub-1V voltage reference circuit, the two current sources in Figure 7.16 can be implemented by peak current source, and the overall schematic is shown in Figure 7.17. The current ratio can be easily obtained by choosing $S_8 = 2S_5$ and $S_9 = S_{10}$. The simulation result of this circuit can achieve 60 ppm/°C over a wide temperature range of −50°C to 75°C. This result is not as good as that obtained in Section 7.5.3. This is because even though the term associated with $\sqrt{I_4}$ in Equation 7.37 is small (but not zero, due to geometric and process variation problems), it is still compatible with 60 ppm/°C, and thus the temperature coefficients of I_4, which is a PTAT current, will limit the temperature performance of the voltage reference circuit. Nevertheless, the lack of opamp in Figure 7.17 makes this circuit as attractive as that in Figure 7.14.

Such voltage reference circuit is first proposed in (Kong, 2007) and there are other voltage reference circuit constructions that are variations of the above presented voltage reference

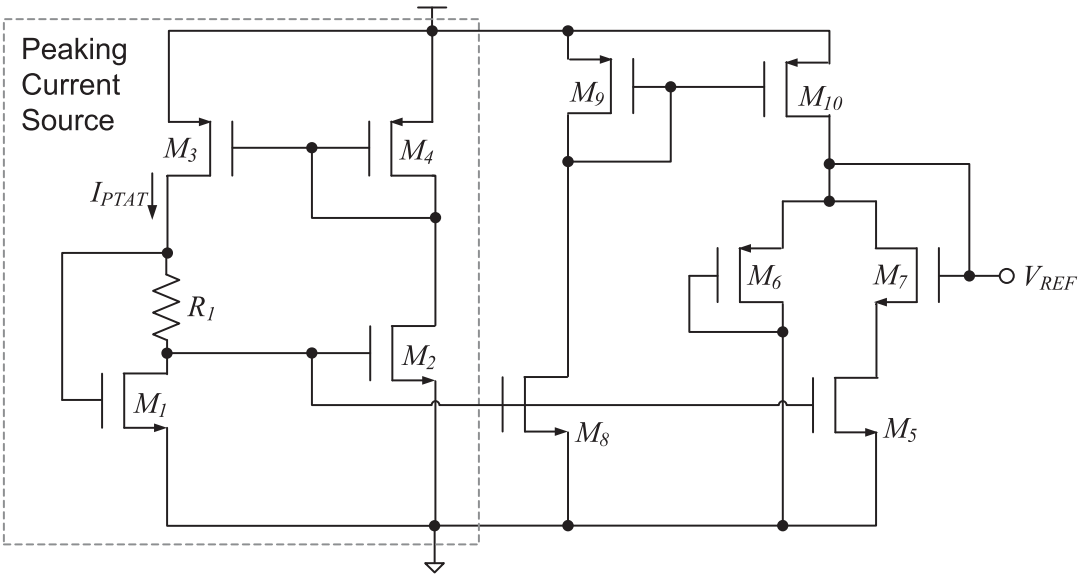


Figure 7.17 Voltage reference circuit based on the PMOS and NMOS threshold voltage differences (Kong, 2007).

circuit, such as that discussed in Section 6.5 which is first presented in (Leung and Mok, 2003). The circuit in Section 6.5 replaces the direct subtraction with a weighted difference circuit. This improves the temperature compensation precision in exchange for the reference voltage precision. A costly trimming circuit can be applied to adjust the resistivity ratio to obtain the necessary variation requirement of the nominal value of the reference voltage.

7.6 Summary

The methods presented in this chapter have been implemented with various variations and presented in the literature, which include the mutual compensation of voltage sources of similar temperature dependency such as that presented in (Ker *et al.*, 2006) which compensates a concave first-order curvature compensated term with a convex first-order curvature compensated term, where both terms have the same center temperature. Perfect compensation could only be achieved if the curvature of these two terms are the exact opposite of each other and the alignment of the center temperature is accurate. Moreover, such methods require the use of resistors and opamps, which are not favorable. The thermal sensitive resistor compensation techniques presented in (Zhou *et al.*, 2006) achieves mutual compensation of voltage sources with similar temperature dependency by using resistors with different *TCs*. This method relieves the mis-alignment problem of the zero *TC* temperatures of the two voltage sources by using voltage sources with the same circuit topology. The drawback is the increase in silicon area because of the increased layout size of the resistors. Other higher order compensation technique introduces high order temperature dependent source to the bandgap voltage reference circuits to lower the temperature coefficients of the obtained reference voltage. In (Song *et al.*, 2004), a second order temperature dependent source obtained from the output is fedback to bias the PNP transistor, thus creating a high-order temperature dependent PTAT source that compensates the high order temperature dependent terms in the CTAT source. The performance of such a compensation method greatly depends on the accuracy of the NPN transistor model. In (Rincon-Mora and Allen, 1998), the nonlinear factor is implemented in current-mode and it is added to the bandgap voltage reference circuit when the operating temperature is higher than a pre-determined temperature, namely piecewise compensation. The added current will cancel the second order temperature dependent term of the high order temperature dependent thermal current of the MOSFETs. Theoretically, the higher the order of the temperature compensation, the better the compensation. Based on this belief, a "third order curvature correction" method is presented in (Leung and Mok, 2003). However, the proposed third order compensation was in fact a second order compensation, because the highest order of the PTAT voltage is only 2. However, no matter whether it is a "third-order" or even a higher order temperature compensation method, the effectiveness of such compensation will be leveraged by the process variation problem (Falconi *et al.*, 2005). Therefore, high order temperature compensation methods with order higher than 2 are seldom found in real world applications.

In 1978, Widlar proposed a configuration which exhibits an intended compensation of the second-order temperature behavior. The principal difference from techniques presented in previous references is that the transistors generating the base-emitter voltages are biased at collector currents having different temperature dependencies. This results in different second-order temperature behaviors obtained by the two base-emitter voltages and (partial) curvature

correction by mutaul compensation becomes possible. In 1981, (Palmer and Dobkin, 1981) presented a curvature corrected bandgap voltage reference circuit. The circuit adopted the Widlar voltage reference circuit to form a linear temperature compensated voltage source as the core. To achieve high order curvature correction, the current ratio of the current mirror in the Widlar voltage reference is driven by temperature sensitive current sources, where one branch of the current mirror is driven by a PTAT current source while the other branch is driven by a CTAT current source. In a similar manner, (Gunawan *et al.*, 1993) presented a high order curvature compensated voltage reference circuit based on the voltage reference circuit presented in (Hilbiber, 1964). The curvature correction was realized by biasing one of the two BJT current paths with a PTAT current and a constant current derived from the reference voltage to obtain a reference voltage with low *TC*.

A principally different way of curvature correction was discussed in Section 7.5. This temperature compensation method makes use of the mutual compensation of voltage sources with similar temperature dependence is considered to be the generalization of the mutual compensation between PTAT and CTAT sources in the first order temperature compensation voltage reference circuit. The voltage sources with similar temperature dependency can be constructed by using devices with similar temperature dependency or through circuit topologies. The pros and cons of these two methods are the post-fabrication trimming flexibility and the power consumption of the overall voltage reference circuit while the voltage sources with similar temperature dependency constructed by devices with similar temperature dependency have the simplest circuitry and lowest power consumption, it is also difficult if not impossible to perform post-fabrication procedures to adjust the similarity between the two voltage sources, and hence this will result in large compensation error.

In comparison, it is the easiest to incorporate post-fabrication trimming circuitry into voltage sources with similar temperature dependency constructed with smart circuit topology. Such design and post-fabrication freedom is traded for high power consumption.

Among various voltage reference circuit topologies, the one that is considered to provide the highest design and post-fabrication freedom, and achieves reference voltage with the lowest *TC*, is the piecewise linear temperature compensation voltage reference circuit. However, the voltage reference circuit also comes with the highest power consumption. In particular, when the power consumption of the voltage reference is a major concern, the voltage summing circuit topology can always achieve a lower power consumption than that of the current summing circuit topology to design reference voltages with the same *TC*. On the other hand, even if the same temperature sensitive devices are being applied, the current summing circuit topology has been shown to be easier to manipulate than the voltage summing topology for voltage reference circuit that generates reference voltage with similar temperature coefficients.

In the literature, there are many high order curvature compensated voltage reference circuits, and some of them that are not discussed in this chapter are developed as exercises which will guide the reader through the design procedure.

7.7 Exercises

Exercise 7.1 *Figure 7.18 shows a modified opamp based β-multiplier bandgap voltage reference with high order curvature compensation presented in (Malcovati et al., 2001). Discussed in Chapter 3, there is a PTAT current passing through Q_2, and the voltage across the*

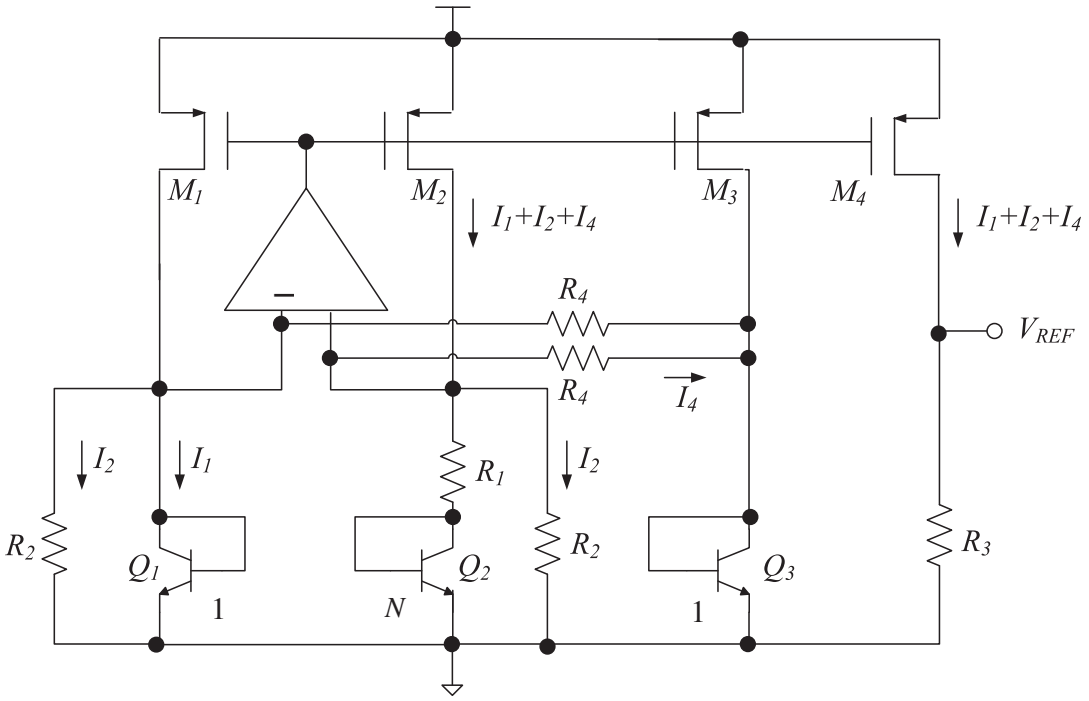


Figure 7.18 Low *TC* bandgap voltage reference by compensating the high order temperature dependent term of the V_{BE} for Exercise 7.1.

BE nodes of Q_2 is given by Equation 1.7. Assume the current I_{Q_3} is temperature independent, then

$$V_{BE_3}(T) = V_{G0}\left(1 - \frac{T}{T_r}\right) + V_{BE}(T_r)\frac{T}{T_r} - (\rho - \theta)\frac{kT}{q}\ln\left(\frac{T}{T_r}\right).$$

1. *Derive the current I_4 that flows through R_4.*
2. *Note that since the same values of current are extracted from I_{D,M_1} and I_{D,M_2}, therefore the β-multiplier is not upset, but just required to provide the extra current to compensate the extracted current. Consider the case where $S_1 = S_2 = S_3 = S_4$. As a result, the current passing through R_3 equals $I_1 + I_2 + I_4$. Derive the output voltage V_{REF}.*
3. *Select the resistor ratio R_2/R_4, such that the high order temperature dependent term in V_{REF} can be alleviated.*

Exercise 7.2 *(Curvature correction by additional temperature dependent current.)*
(a) Derive V_{REF} in Figure 7.19 in the same form as that of the conventional β-multiplier bandgap voltage reference circuit.
(b) A low TC voltage reference circuit in the low temperature range can be obtained by adding a current to R_3. What is the nature of this current?
(c) Show that I_{10} in Figure 7.20 satisfies the requirement in (b).
(d) Design and simulate the complete high order compensated voltage reference circuit.

Exercise 7.3 *The sub-*1V *β-multiplier bandgap voltage reference circuit using resistive division that was discussed in Section 6.3 can be modified as shown in Figure 7.21 to achieve a low temperature coefficient through the addition of a temperature dependent current with*

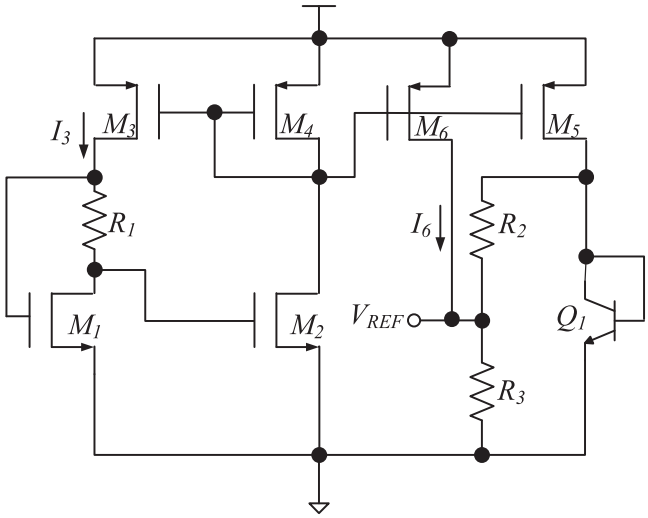


Figure 7.19 Bandgap voltage reference circuit for Exercise 7.2

high order temperature coefficient. Note that when the temperature increases, V_{BE_2} decreases, and so does the gate voltage of M_4 which is obtained from the resistive voltage divider formed by $R_{3,a}$ and $R_{3,b}$. With proper transistor size scaling, the added current I_4 will be large enough to affect the output voltage of the voltage reference circuit only when M_4 is biased at saturation.

1. *Let $K = R_{3,b}/(R_{3,a} + R_{3,b})$, derive the expression that shows the turn on temperature of M_4.*
2. *Derive the expression of I_4 in terms of K, and show that it has a second order temperature characteristics.*

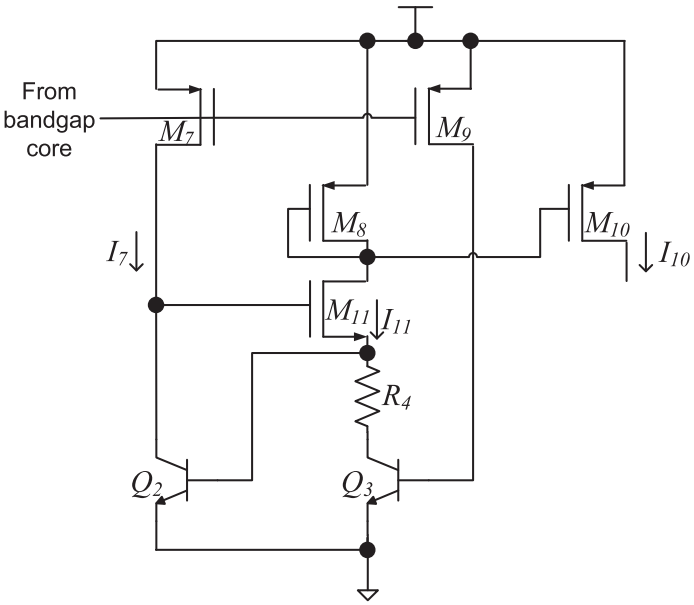


Figure 7.20 High order temperature dependent current for high order curvature compensation of the bandgap voltage reference circuit in Figure 7.19 for the analysis in Exercise 7.2.

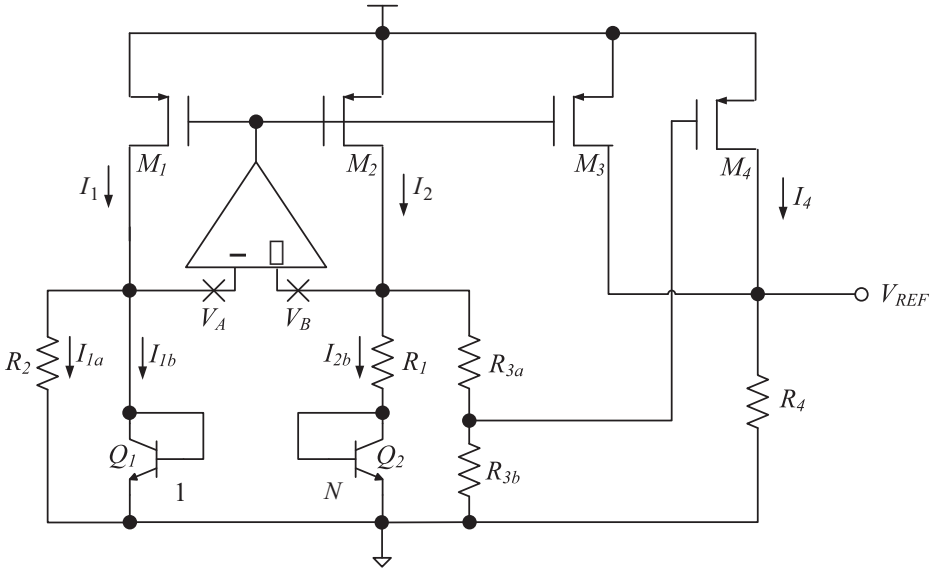


Figure 7.21 Higher order temperature compensated sub-1V opamp based bandgap voltage reference circuit by resistive division through the addition of a second order current for Exercise 7.3.

Exercise 7.4 *Figure 7.22 shows a traditional voltage reference circuit that achieves high order temperature compensation by adding high order temperature dependent currents at selected temperature regions.*

1. *Derive* I_2 *in terms of* V_{REF}, R_X, R_Y, R_Z, V_{BE_4}, *and* R_P.
2. *Design and simulate the voltage reference circuit in Figure 7.9 with* V_{REF} *achieving zero TC at* 25 °C.

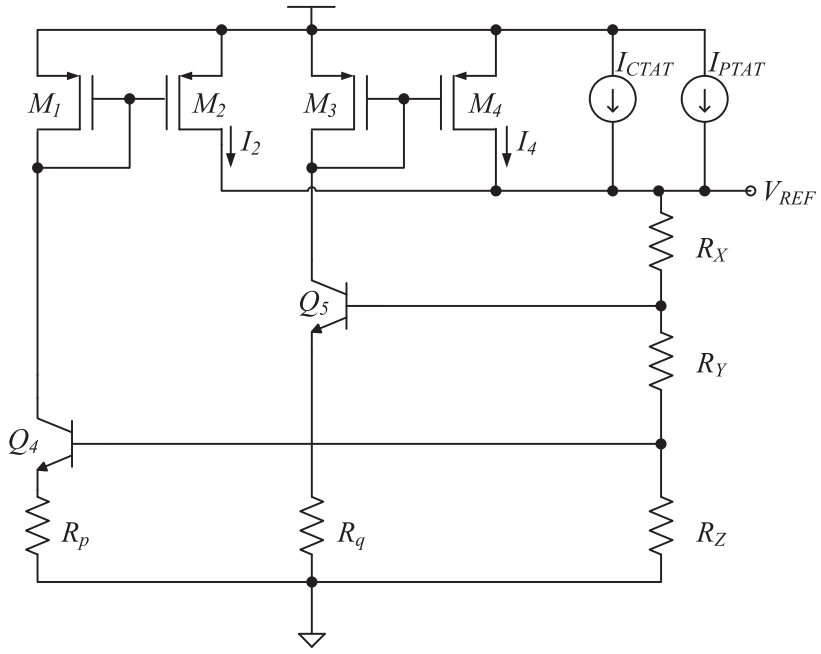


Figure 7.22 Higher order temperature compensated voltage reference circuit by injecting a nonlinear current into the traditional voltage reference circuit for Exercise 7.4.

3. *The voltage reference circuit in Figure 7.9 is applied to the schematic in Figure 7.20 without Q_5, R_q, M, and M from the schematic, that is, with only I_2 added to V_{REF}, adjust R_P, R_X, R_Y, and R_Z, such that V_{REF} achieves zero TC at both* 25 °C *and* 50 °C.
4. *Using the result in Exercise 7.4.3, consider both I_2 and I_4 are added to V_{REF} as shown in Figure 7.20, adjust R_q and R_Y, such that V_{REF} achieves zero TC point at* 25 °C, 50 °C, *and* 75 °C.

References

Banba, H., Shiga, H., Umezawa, A. *et al.* (1999) A CMOS bandgap reference circuit with sub-1-V operation. *IEEE Journal of Solid-State Circuits*, **34** (5), 670–74.

Blauschild, R.A., Tucci, P.A., Muller, R.S. *et al.* (1978) A new NMOS temperature-stable voltage reference. *IEEE Journal of Solid-State Circuits*, **13** (6), 767–74.

Cave, M.D. (2005) Scalable voltage reference for ultra deep submicron technologies. PhD dissertation, University of Texas Austin.

Cheney, E.W. (1982) *The Approximation of Functions*, McGraw-Hill.

Falconi, C., D'Amicoa, A., Natale, C.D. *et al.* (2005) Low cost curvature correction of bandgap references. *Sensors and Actuators A: Physical*, **117** (1), 127–36.

Gunawan, M., Meijer, G.C.M., Fonderie, J. *et al.* (1993) A curvature-corrected low-voltage bandgap reference. *IEEE Journal of Solid-State Circuits*, **28** (6), 667–70.

Hilbiber, D.F. (1964) A new semiconductor voltage standard. *IEEE International Solid-State Circuits Conferece Digest of Technical Papers (ISSCC)*, pp. 32–33.

Hirose, T., Matsuoka, T., Taniguchi, K. *et al.* (2005) Ultralow-power current reference circuit with low temperature dependence. *IEICE Transactions on Electronics*, **E88-C** (6), 1142–47.

Ker, M.D., Chen, J.S. and Chu, C.Y. (2006) New curvature-compensation technique for CMOS bandgap reference with sub-1-V operation. *IEEE Transaction on Circuits and Systems II: Express Briefs*, **53** (8), 667–71.

Kong, M., Guo, J., Zhang, K. *et al.* (2007) A novel CMOS voltage reference based on threshold voltage difference between p-type and n-type MOSFETs. *Chinese Journal of Semiconductor*, **28** (10), 1546–50.

Leung, K.N. and Mok, P.K.T. (2003) A CMOS voltage reference based on weighted ΔV_{GS} for CMOS low-dropout linear regulators. *IEEE Journal of Solid-State Circuits*, **38** (1), 146–50.

Malcovati, P., Maloberti, F., Fiocchi, C. *et al.* (2001) Curvature-compensated bicmos bandgap with 1-V supply voltage. *IEEE Journal of solid-State Circuits*, **36** (7), 1076–81.

Maloberti, F. (2001) *Analog Design for CMOS VLSI Systems*, Kluwer Academic Publishers.

Nicollini, G. and Senderwoicz, D. (1991) A CMOS bandgap reference for differential signal processing. *IEEE Journal of Solid-State Circuits*, **26**, 41.

Palmer, C. and Dobkin, R. (1981) A curvature corrected micropower voltage reference. *IEEE International Solid-State Circuits Conferece*, pp. 58–9.

Rincon-Mora, G. and Allen, P. (1998) A 1.1-V current-mode and piecewise-linear curvature-corrected bandgap reference. *IEEE Journal of Solid-State Circuits*, **33** (10), 1551–54.

Song, H. and Kim, C. (1993) A temperature-stabilized SOI voltage reference based on threshold voltage difference between enhancement and depletion NMOSFET's. *IEEE Journal of Solid-State Circuits*, **28**(December), 671–77.

Song, Y., Jia, S. and Zhao, B.Y. (2006) A precise curvature compensated cmos bandgap voltage reference with sub-1v supply. *Proceeding of the 8th IEEE International Conference on Solid-State and Integrated Circuit Technology*, pp. 1754–56.

Song, Y., Lu, W.G., Chen, Z.J. *et al.* (2004) A precise compensated bandgap reference without resistors. *Proceeding of the 7th IEEE International Conference on Solid-Sate and Integrated Circuit Technology*, **2**, 1583–86.

Ugajin, M., Suzuki, K. and Tsukaraha, T. (2002) A 0.6-V supply, voltage-reference circuit based on threshold-voltage-summation architecture in fully-depleted CMOS/SOI. *IEICE Transactions on Electronics*, **E85-C** (8), 1588–95.

Zhou, H., Zhang, B., Li, Z.J. and Luo, P. (2006) A new CMOS current reference with high order temepratre compesnation. *Journal of Electronic Science and Technology of China*, **4** (1), 8–11.

8

CMOS Voltage Reference without Resistors

In Chapter 5, we reviewed different temperature compensation techniques to design voltage reference circuits. The general technique is of the mutual compensation between weighted PTAT and CTAT sources. The PTAT source and the CTAT source can be in the form of currents or voltages extracted from different thermal characteristics of semiconductor devices. Let's consider the opamp based β-multiplier bandgap voltage reference circuit which has been thoughtfully analyzed in Chapter 3. The opamp based β-multiplier bandgap voltage reference circuit adopts the basic $V_{BE} - \Delta V_{BE}$ compensation topology to produce a temperature compensated reference voltage by summing up the V_{BE} and a weighted ΔV_{BE} with the factor M as depicted in Equation 3.3. The schematic of the opamp based β-multiplier bandgap voltage reference circuit is shown in Figure 3.4, where ΔV_{BE} builds on R_1 will be converted to a PTAT current I_2 by performing voltage-to-current conversion with $I_2 = \Delta V_{BE}/R_1$. The PTAT current I_2 is copied from the core circuit to the output circuit by the current mirror formed by M_2 and M_3. The PTAT I_2 is converted back to a PTAT voltage and summed with the CTAT voltage V_{BE_3} via resistor R_2. This will complete the generation of temperature compensated reference voltage $V_{REF} = V_{BE_3} + (\frac{R_2}{R_1}\ln(N))\Delta V_{BE}$, where $M = \frac{R_2}{R_1}\ln(N)$ with N being the ratio of current densities between Q_1 and Q_2. It can be noted that the weighting factor M in the voltage reference circuit is generated along with the extraction of the ΔV_{BE} from the V_{BE} of two bipolar transistors biased to have different current densities. The extraction of the ΔV_{BE} involves a voltage-to-current conversion followed by a current-to-voltage conversion. The conversion sequence also scales the PTAT ΔV_{BE} to match the required mutual compensation with the CTAT V_{BE} and to generate a temperature compensated reference voltage. The use of a resistor to perform the current-to-voltage and voltage-to-current conversion is simple and almost perfectly linear. However, the use of resistors inevitably increases the chip size and it also results in increased noise coupling from substrate. In this chapter, we shall review several conversion methods based on the inverse function approach (Torrance *et al.*, 1985), which is found to be a common approach for voltage-to-current or current-to-voltage conversion without using resistors, and how to apply such conversion methods to the design of resistor free voltage reference circuits (Buck *et al.*, 2002; Hirose *et al.*, 2005, 2008; Oguey and Aebischer, 1997; Tam *et al.*, 2010; Ming *et al.*, 2010).

CMOS Voltage References: An Analytical and Practical Perspective, First Edition. Chi-Wah Kok and Wing-Shan Tam.
 Published 2013 by John Wiley & Sons Singapore Pte. Ltd.

8.1 Generation of Weighted PTAT Source By Inverse Functions

The use of resistors is a simple and direct method to accomplish the voltage-to-current and current-to-voltage conversion to generate a weighted PTAT source for the mutual compensation with a CTAT source. Besides the resistors, the MOSFETs can also achieve voltage-to-current or current-to-voltage conversion. However, due to the squares-law characteristics of the MOSFETs, the conversions are nonlinear functions. Fortunately, the nonlinearity of the conversions can be canceled by the inverse function approach. Therefore, MOSFET is a promising device to take the role of resistors in linear voltage-to-current or current-to-voltage conversions, at the same time suppressing the reliability problems and adverse effects caused by the resistor. The inverse function approach refers to the use of an inverse function pair to achieve a voltage-to-current and a current-to-voltage conversion (Torrance *et al.*, 1985). The function pair can be a transconductance function (voltage-to-current conversion) and a transimpedance function (current-to-voltage conversion), in which these two functions are not necessarily linear in nature, but they have to be inverse functions of the other, such that their nonlinearity can be canceled out when the two functions are applied consecutively. Let's denote the inverse function pair as $f_1(\cdot)$ and $f_2(\cdot)$, where $f_1(\cdot)$ and $f_2(\cdot)$ can be nonlinear functions and $f_2^{-1}(\cdot) = Mf_1(\cdot)$, with M being a scalar constant.

8.1.1 Weighted Differential Circuit

The inverse function pair can be implemented by transconductance and transimpedance functions realized by groups of matched differential pairs that utilize the squares-law characteristic of NMOS transistors. Figure 8.1 shows the schematic of a weighted differential voltage circuit that performs the inverse function pair. This circuit consists of two differential pairs formed by (M_1, M_2) and (M_3, M_4) connecting by a pair of current mirrors formed by (M_5, M_6). The differential pair (M_1, M_2) performs the voltage-to-current ($V - I$) conversion that converts the difference of V_1 and V_2 into a current. It should be noted that the converted current is a function of (V_2-V_1). Then, the converted current is copied to the second differential pair (M_3, M_4) by the current mirror (M_5, M_6). Finally, the second differential pair (M_3, M_4) performs the current-to-voltage ($I - V$) conversion to generate an output voltage V_O, which is therefore a function of (V_2-V_1). Assume all threshold voltages of the transistors are identical, the output voltage V_O can be derived by first considering the differential pair (M_1, M_2), which obtains

$$V_1 - V_Y = \sqrt{\frac{I_1}{A\kappa}} + V_{th_1}, \tag{8.1}$$

$$V_2 - V_Y = \sqrt{\frac{I_2}{AB\kappa}} + V_{th_2}, \tag{8.2}$$

where $\kappa = \frac{1}{2} S_u \mu_n C_{ox}$ with S_u is the W/L of a unit size transistor adopted in the circuit. Then,

$$V_2 - V_1 = \sqrt{\frac{I_2}{AB\kappa}} - \sqrt{\frac{I_1}{A\kappa}}. \tag{8.3}$$

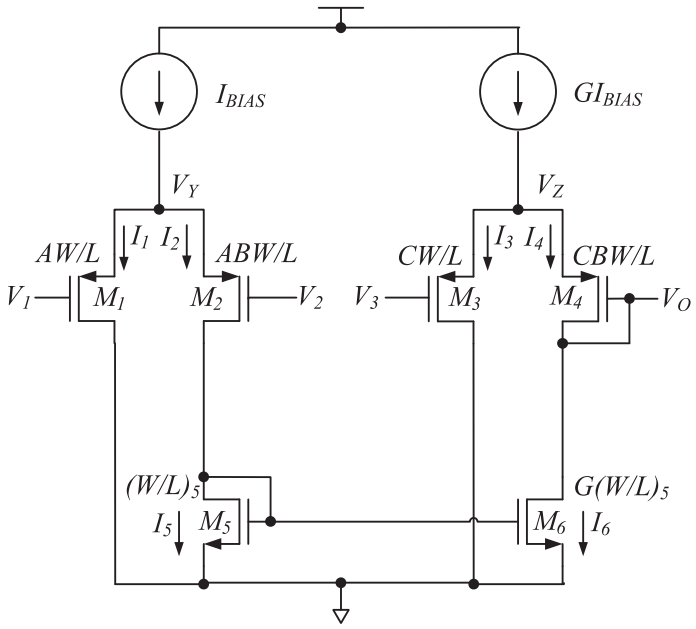


Figure 8.1 A weighted differential circuit: generation of $V_O = \sqrt{\frac{AG}{C}}(V_2 - V_1)$ based on the inverse function approach via the voltage-to-current followed by current-to-voltage conversion, where A, C, and G are the transistor ratios.

As a result, we have $(V_2 - V_1)$ as a function of I_1 and I_2. With the current mirror (M_5, M_6) and the second differential pair (M_3, M_4), the following relations are obtained

$$I_1 + I_2 = I_{BIAS}, \tag{8.4}$$

$$I_3 + I_4 = GI_{BIAS}, \tag{8.5}$$

$$I_4 = I_6 = GI_5 = GI_2. \tag{8.6}$$

The second differential pair (M_3, M_4) obtains

$$V_3 - V_Z = \sqrt{\frac{I_3}{C\kappa}} + V_{th_3}, \tag{8.7}$$

$$V_O - V_Z = \sqrt{\frac{I_4}{BC\kappa}} + V_{th_4}. \tag{8.8}$$

Then,

$$V_O - V_Z = \sqrt{\frac{I_4}{BC\kappa}} - \sqrt{\frac{I_3}{C\kappa}}. \tag{8.9}$$

Substitute Equations 8.4, 8.5, 8.6 into Equation 8.9 will yield

$$V_O - V_3 = \sqrt{\frac{GI_2}{BC\kappa}} - \sqrt{\frac{G(I_{BIAS} - I_2)}{C\kappa}} \tag{8.10}$$

$$= \sqrt{\frac{AGI_2}{ABC\kappa}} - \sqrt{\frac{AG(I_{BIAS} - I_2)}{AC\kappa}} \tag{8.11}$$

$$= \sqrt{\frac{AG}{C}} \left(\sqrt{\frac{I_2}{AB\kappa}} - \sqrt{\frac{I_1}{A\kappa}} \right) \tag{8.12}$$

$$= \sqrt{\frac{AG}{C}} (V_2 - V_1). \tag{8.13}$$

Consider $V_3 = 0$, the output voltage $V_O = \sqrt{\frac{AG}{C}} (V_2 - V_1)$, in which a weighted difference voltage $(V_1 - V_2)$ is perfectly extracted. It should be noted that the extraction involves a voltage-to-current conversion followed by a current-to-voltage conversion via two differential pairs and a current mirror. It can also be noted that all the process, supply voltage, and temperature dependent terms, for examples the threshold voltage V_{th} and the mobility μ, are canceled through this sequential conversion. Therefore, a perfect linear scaling of $(V_2 - V_1)$ can be obtained by the use of this weighted differential circuit and the scaling factor can be easily adjusted by tuning the parameters A, C, and G. The linear extraction offered by the weighted differential circuit makes it a suitable replacement of resistor for the extraction and scaling of the difference voltage of thermal devices, which is important in the generation of temperature compensated reference voltage.

8.1.2 Negative Impedance Converter

The negative impedance converter (NIC) is another circuit that can achieve voltage-to-current and current-to-voltage conversions without the use of resistor. The NIC is a circuit block that forms a negative relationship between the input impedance (Z_{in}) and the output impedance (Z_{out}) of a system, that is $Z_{in} = -K(\cdot)Z_{out}$, or $Z_{out} = -K(\cdot)Z_{in}$, where $K(\cdot)$ is not necessarily linear with respect to its function parameters. Generally, the function parameters can either be currents or voltages in the application of voltage-to-current or current-to-voltage conversions. Thanks to the inverse-function approach, a linear function $K(\cdot)$ with respect to voltage or current can be obtained from the NIC implemented in the CMOS process (Brennan *et al.*, 1988), in which the linearity is achieved by the mutual compensation of the nonlinear inverse function pairs of the transconductance and transimpedance of MOSFETs (Torrance *et al.*, 1985).

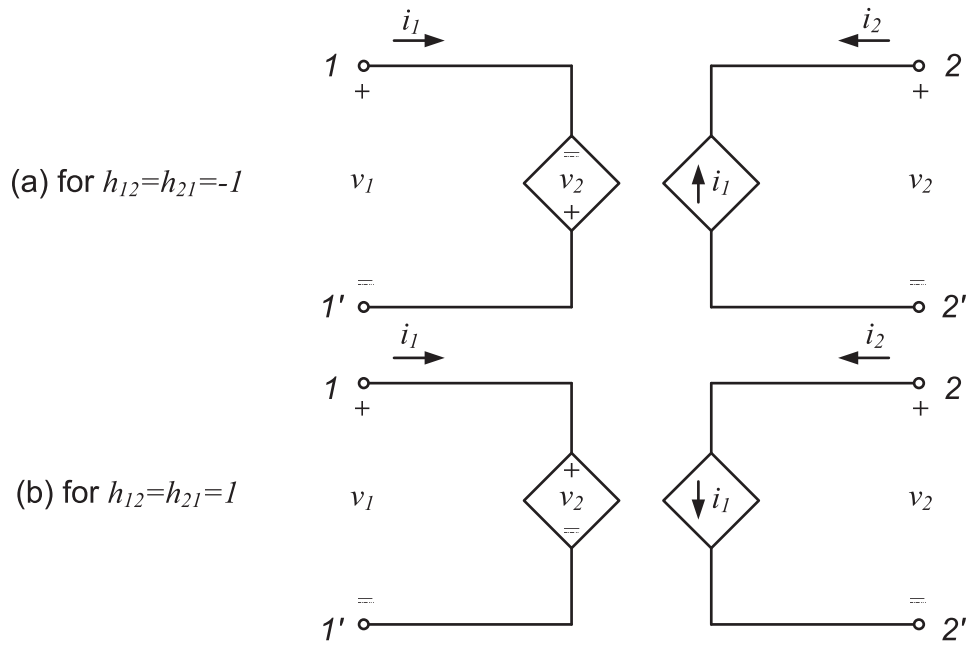


Figure 8.2 A two-port system illustrating (a) a current-controlled and (b) a voltage-controlled negative impedance converter (NIC) for $K = 1$.

Before we go into the CMOS implementation of the NIC, let's review the voltage-to-current or current-to-voltage conversions in the NIC analytically by considering its representation using a two-port system as shown Figure 8.2. The system has two ports, port 1 ($1 - 1'$) and port 2 ($2 - 2'$), where these ports can be considered as the input port or output port, depending on the external impedance, voltage polarity, and current direction applied to the ports. Therefore, the two-port system can be classified as a current-controlled system (see Figure 8.2(a)) or a voltage-controlled system (see Figure 8.2(b)), depending on the relationship between the two ports, which will be detailed later. The two-port system can be formulated as a h-parameter transfer function given by

$$\begin{bmatrix} v_1 \\ i_2 \end{bmatrix} = \begin{bmatrix} h_{11} & h_{12} \\ h_{21} & h_{22} \end{bmatrix} \begin{bmatrix} i_1 \\ v_2 \end{bmatrix}, \tag{8.14}$$

where v_ℓ and i_ℓ are the voltage and current applied to port ℓ. The transfer function parameters h_{11}, h_{12}, h_{21}, and h_{22} are free functions. To confine our discussions to linear voltage-to-current conversion or current-to-voltage conversion, and without losing generality, let's consider the special case where $h_{11} = h_{22} = 0$ and $h_{12}h_{21} = K = 1$, such as to yield a negative relationship between Z_{in} and Z_{out}. In this case, it is perfectly possible for $h_{12} = h_{21} = -1$ or $h_{12} = h_{21} = 1$ or some other values too.

In particular, Figure 8.2(a) shows the case of $h_{12} = h_{21} = -1$, which yields the relationship of $i_1 = -i_2$ (note that the direction of the port currents is inverted) and $v_1 = -v_2$ (note that the polarity of the port voltages is inverted). It should be noted that the current source at port 2 is defined as having the same direction as that of port current i_1 at port 1, whereas the voltage source at port 1 has the inverted polarity as that of port voltage v_2 at port 2. Therefore, it forms

the so-called current-controlled voltage inversion, which is also known as current-controlled negative impedance (CCNIC). Figure 8.2(b) shows the case of $h_{12} = h_{21} = 1$, which yields the relationship of $i_1 = i_2$ (note that the direction of the port currents is the same) and $v_1 = v_2$ (note that the polarity of the port voltages is the same). It should be noted that the current source at port 2 has current flowing in inverted direction when compared to the port current i_1 at port 1, whereas the voltage source at port 1 has the same polarity as that of port voltage v_2 at port 2. Therefore, it forms the so-called voltage-controlled current inversion, which is also known as voltage-controlled negative impedance (VCNIC).

It should be noted that the two-port NIC can be configured to invert the polarity of the induced voltage source or the direction of the induced current source by coupling different impedance at both ports. Since the inversion in voltage polarity is current-controlled, and the inversion in current direction is voltage-controlled, it can be observed that such a system can be applied to perform voltage-to-current and current-to-voltage conversions. In real practice, h_{11} and h_{22} are not precisely equal to zero and the h parameters are usually in complex form. However, the negative resistance property of the NIC will form a stable system even when port 1 is in open circuit (or high impedance) and port 2 is in short circuit (or low impedance).

Figure 8.3 shows the basic CMOS implementation of a NIC circuit block. It is clear that this circuit block is similar to the β-multiplier circuit. The four transistors, M_1 to M_4, form a close loop system that will either keep the currents at the two legs the same or the voltages at the two ports the same, depending on the impedance at the two ports. MOSFET or bipolar transistors can be used to provide the impedance to the NIC for the generation of a constant voltage or current, instead of using resistors. Such voltage source and current source without using resistors makes the design of resistorless voltage reference circuits possible.

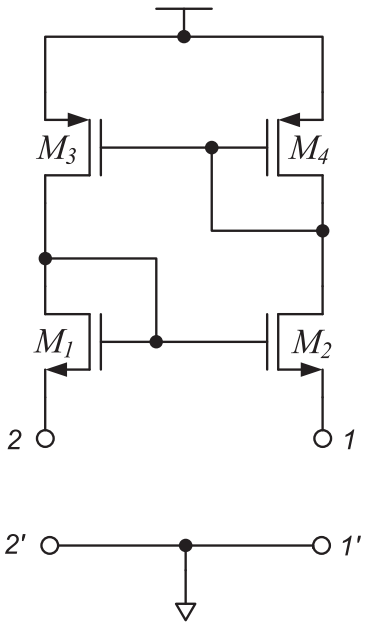


Figure 8.3 CMOS implementation of a negative impedance converter.

8.2 Resistorless Voltage and Current Sources

In Chapter 5, we reviewed the generation of a temperature compensated reference voltage through the combination of different voltage sources and current sources. It should be noted that voltage-to-current conversion, or vice versa, is inevitable in temperature compensation. The use of a resistor is the simplest and easiest approach for linear conversion, because the resistor is intrinsically linear. However, the use of a resistor will have inherent thermal noise, dissipate more power, and occupy a large silicon area. To achieve a resistor free voltage reference circuit design, resistorless voltage sources and current sources are needed. In the following sections, we will present several resistorless voltage or current sources based on the weighted differential circuit and the negative impedance converter. The output voltage or current of the resistorless sources will have inherently different temperature dependency which can be applied to design resistorless voltage reference circuits, where the associated voltage reference circuits will be discussed in later sections.

8.2.1 Resistorless Voltage Source

Figure 8.4 shows a weighted differential circuit that generates a PTAT voltage V_{OUT}, by setting $V_1 = V_{BE_1}$, $V_2 = V_{BE_2}$, and $V_3 = 0$ in Figure 8.1, where V_{BE_1} and V_{BE_2} are obtained from the base-emitter voltages of the NPN transistors Q_1 and Q_2, respectively. Note that Q_1 and Q_2

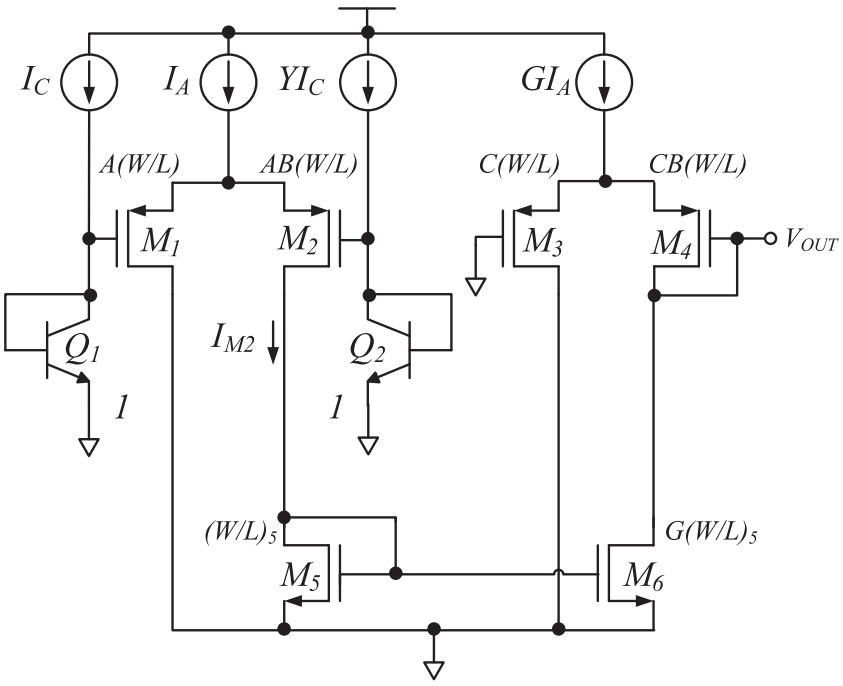


Figure 8.4 Simplified schematic diagram of a first order bandgap voltage reference circuit without resistor constructed with the weighted differential voltage circuit.

have identical emitter areas but are biased with different biasing currents. As a result, it is clear from Equation 8.13 that

$$\begin{aligned} V_{OUT} &= \sqrt{\frac{AG}{C}}(V_{BE_2} - V_{BE_1}) \\ &= \sqrt{\frac{AG}{C}}\Delta V_{BE_{1,2}} \\ &= \sqrt{\frac{AG}{C}}\ln\left(\frac{I_{BE_2}}{I_{BE_1}}\right)V_T \\ &= \sqrt{\frac{AG}{C}}\ln(Y)\,V_T \\ &= MV_T. \end{aligned} \tag{8.15}$$

As a result, V_{OUT} is linearly dependent on V_T and is therefore a PTAT voltage. This PTAT voltage generation technique is widely used in resistorless voltage reference circuit in the literature. We shall discuss a landmark voltage reference circuit based on this circuit technique in a later section.

8.2.2 Resistorless Current Source

Before discussing the resistorless current source, let's review a conventional PTAT current source built by a NIC and a resistor as shown in Figure 8.5. Compare Figure 8.5 with the schematic shown in Figure 8.3, the port 1 is terminated with a resistor R and port 2 is shorted to the ground. The NIC hence forms a stable system with the current flowing into the two legs

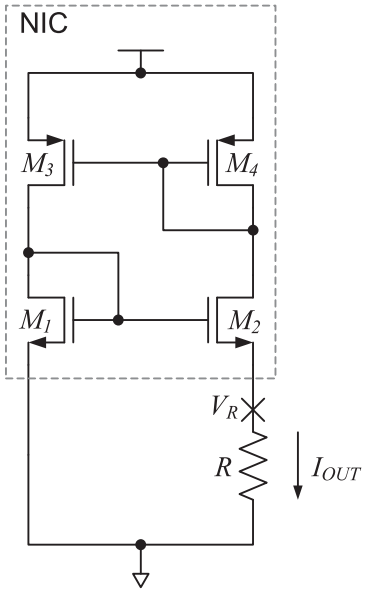


Figure 8.5 PTAT current sources built with resistor by connecting a resistor to NIC.

being identical. The transistor sizes of M_1 and M_2 are required to be identical so as to force the currents in the two branches to be the same, while M_3 and M_4 are designed to have different sizes. It should be noted that M_3 and M_4, in the current source in Figure 8.5, are biased current mirrors in saturation, while M_1 and M_2 are biased in weak inversion, which is different from that in the β-multiplier circuit. The voltage V_R is given by (Vittoz and Fellrath, 1977)

$$V_R = V_T \ln\left(\frac{S_3 S_1}{S_4 S_2}\right), \tag{8.16}$$

where V_T is the thermal voltage and S_x is the W/L ratio of transistors M_x. By Ohm's law, the output current of this current source is given by

$$I_{OUT} = \frac{V_R}{R} = \frac{V_T}{R} \ln\left(\frac{S_3 S_1}{S_4 S_2}\right). \tag{8.17}$$

From Equation 8.17, I_{OUT} is a function of V_T which is a PTAT voltage. It should be noted that the voltage V_R is insensitive to the supply voltage variation and the current level as long as M_1 and M_2 are in weak inversion. Typically, this can be achieved when V_R is in the range of V_T to $4V_T$.

This PTAT current source forms the basic structure for other resistorless current sources in literature. Oguey and Aebischer (Oguey and Aebischer, 1997) proposed a PTAT current source with MOSFET only by introducing a simple modification on the current source shown in Figure 8.5 which replaces the resistor by a MOSFET. The modified schematic is shown in Figure 8.6, where M_5 is the transistor that replaces the resistor R in Figure 8.5. The NMOS M_5 is biased in strong inversion just below saturation. The additional MOSFETs M_6 and M_7

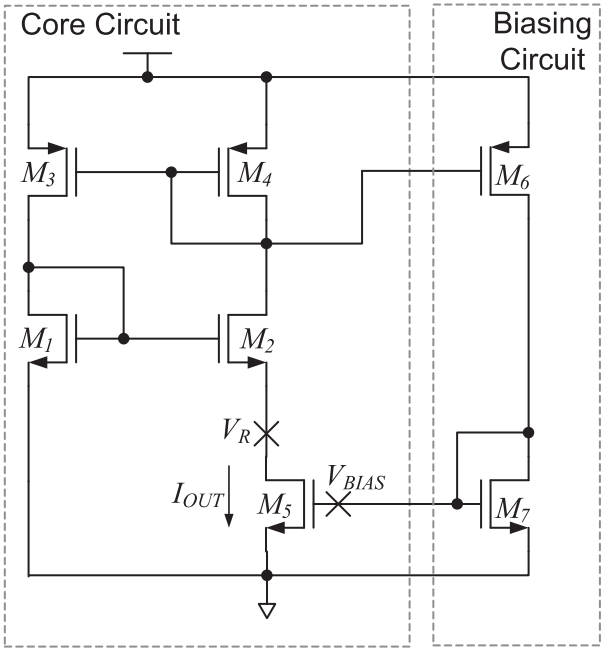


Figure 8.6 The resistor free constant current source discussed in (Oguey and Aebischer, 1997), which connects a self-biased MOSFET M_5 to an NIC to replace the resistor in Figure 8.5.

in Figure 8.6 form a biasing circuit, in which M_6 forms part of the PMOS current mirror with M_1 and M_2. The current I_{DS_6} is copied by M_7 to bias M_5. Thus both M_6 and M_7 are biased in saturation mode and in strong inversion. Hence, the drain voltage of M_5 is low and the output current is given by (Oguey and Aebischer 1997)

$$I_{OUT} = \frac{\beta_7}{2}\frac{S_1}{S_6}\left(V_{BIAS} - V_{th_5}\right)^2, \tag{8.18}$$

where β_7 is the process transconductance of M_7. Hence, the TC of I_{OUT} can be expressed as

$$\frac{1}{I_{OUT}}\frac{\partial I_{OUT}}{\partial T} = -\frac{2\partial V_{th_5}/\partial T}{(V_{BIAS} - V_{th_5})^2}. \tag{8.19}$$

As $\frac{\partial V_{th_5}}{\partial T} < 0$, therefore, the TC of I_{OUT} is always greater than 0, such that I_{OUT} in Oguey's current source is a PTAT current.

In 2005 (Hirose *et al.* 2005) proposed biasing M_5 to operate in the linear mode with other transistors in subthreshold mode; hence a near-zero TC reference current can be obtained and the current is given by

$$\begin{aligned} I_{OUT} &= \frac{V_{DS_5}}{R_{ON_5}} \\ &= \left(V_{OS,1} - V_{OS,2} + \eta V_T \ln\left(\frac{S_2}{S_1}\right)\right) \\ &\quad \times \mu C_{OX}\left(\frac{W}{L}\right)\left(V_{BIAS} - V_{th_5}\right), \end{aligned} \tag{8.20}$$

where R_{ON_X}, S_X, η, and $V_{OS,X}$ are the on-resistance, the aspect ratio, the subthreshold swing parameter, and the offset voltage difference between the threshold voltage in strong inversion and that in the subthreshold region, respectively. A particular V_{BIAS} is required to pursue a near-zero TC biasing current with respect to the technology used in this book. The near-zero TC biasing current can be obtained at $(V_{BIAS} - V_{th_5})$ to be less than 1 V and the V_{BIAS} has to be a PTAT voltage (Hirose *et al.*, 2005), thereby compensating for the CTAT effect caused by the threshold voltage and mobility. The generation of PTAT and CTAT currents using the modified current source circuit proposed by Hirose *et al.* will be discussed in a later section.

8.3 First Order Compensated Resistorless Bandgap Voltage Reference Circuit

The first order temperature compensated opamp based β-multiplier bandgap voltage reference circuit presented in Chapter 3 performs voltage summing of a CTAT voltage with a weighted PTAT voltage to obtain a near-zero TC reference voltage. In general, the CTAT source and the PTAT source can be either in the form of voltage or current as demonstrated in Chapter 5. The same temperature compensation voltage reference circuit topology can also be applied in the design of resistorless bandgap voltage reference circuits.

8.3.1 Voltage Summation Based Resistorless Reference Circuit

The summation of a CTAT voltage and a weighted PTAT voltage is one of the simplest temperature compensation methods. A CTAT voltage can be easily obtained from any *PN* junction without the need of explicit extraction. However, a complicated extraction circuit is always required for the generation of a PTAT voltage. The weighted differential circuit is a suitable candidate for the extraction of a properly scaled PTAT voltage without the use of resistor. In order to obtain a consistency presentation, like other $V_{BE} - \Delta V_{BE}$ voltage reference circuits presented in this book, the temperature dependent device will be constructed by diode connected NPN transistors.

Figure 8.7 shows the schematic for a landmark first order temperature compensated voltage reference circuit presented by Buck *et al.* (2002). Buck's voltage reference circuit was in fact built from the weighted differential circuit but with the summation of an additional CTAT voltage. The same as that in Figure 8.4, the bipolar transistors Q_1 and Q_2 are with the same emitter area but biased with different currents in Figure 8.7. Furthermore, the gate of transistor M_3 is coupled to the diode connected Q_2, hence the CTAT V_{BE_2} is added to the PTAT voltage given by Equation 8.15. As a result, the V_{REF} is given by

$$V_{REF} = V_{BE_2} + \sqrt{\frac{AG}{C}}(\Delta V_{BE_{2,1}}) = V_{BE_2} + MV_T = V_{REF-CONV}. \tag{8.21}$$

Note that when $M = \sqrt{\frac{AG}{C}}\ln(\frac{I_{BE_2}}{I_{BE_1}}) = 19.22$, as described in Section 3.2.1, this temperature compensated voltage reference circuit will achieve a near-zero *TC* reference voltage

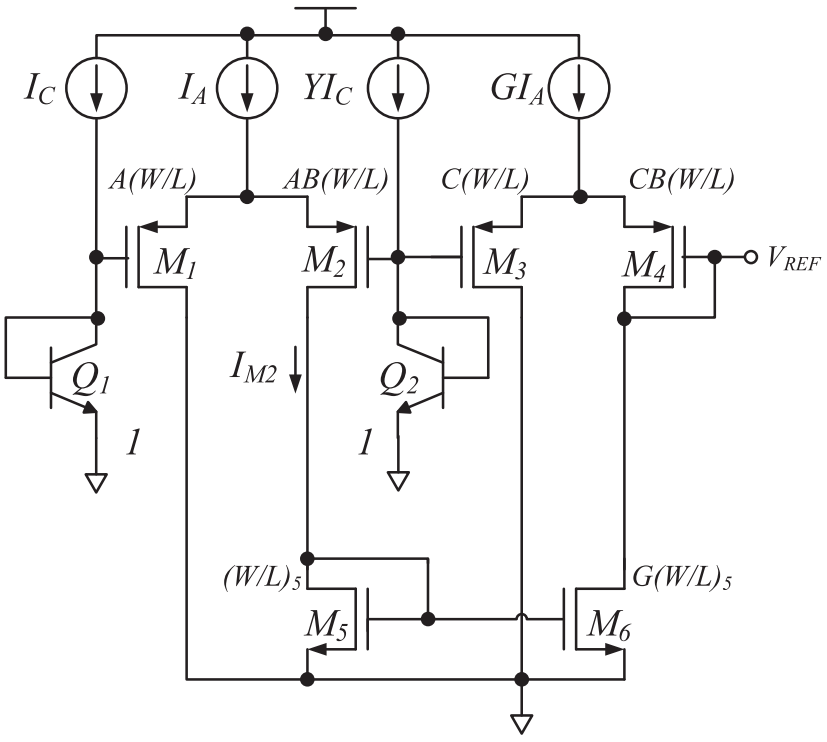


Figure 8.7 Schematic of the bandgap voltage reference circuit without resistor proposed by Buck *et al.* (2002).

$V_{REF} = 1.23\,V$. Further analysis on the performance of the resistorless bandgap voltage reference circuit in Figure 8.7 will show that it is compatible with the opamp based β-multiplier bandgap voltage reference circuit presented in Section 3.2.1, at least in theory.

8.3.2 Current Summation Based Resistorless Reference Circuit

Similarly to the voltage summation based reference circuit, a near-zero *TC* current source can also be obtained by summing up a PTAT current with a CTAT current. By combining current sources acquiring different thermal properties, we can design a first order compensated current reference circuit. Figure 8.8 shows an example of a first order temperature compensated current reference circuit which consists of a PTAT current source, a CTAT current source, and a current addition circuit. The PTAT current source formed by $M_1 \sim M_7$ implements an Ogeuy's current source (Ogeuy *et al.*, 1997). The CTAT current source formed by $M_8 \sim M_{15}$ is a modified Ogeuy's current source which is biased with a different biasing voltage $V_{BIAS,2}$, such that a CTAT current I_{CTAT} is generated (Hirose *et al.*, 2008). The current mirrors formed by $(M_6 - M_{17})$ and $(M_{13} - M_{16})$ copy the I_{PTAT} and I_{CTAT}, respectively, to the current scaler and adder circuit formed by M_{16} and M_{17}. The current adder circuit sums the I_{PTAT} and the I_{CTAT} up to give a reference current I_{REF} with near-zero *TC* (i.e., $I_{OUT} = I_{PTAT} + I_{CTAT}$). It should be noted that the CTAT current source has a similar structure as that of PTAT current source but with a different biasing circuit that generates $V_{BIAS,2}$.

8.4 Resistorless Sub-Bandgap Reference Circuit

We have reviewed the voltage summation based and current summation based resistorless voltage reference circuits. It should be noted that the temperature compensation is not limited

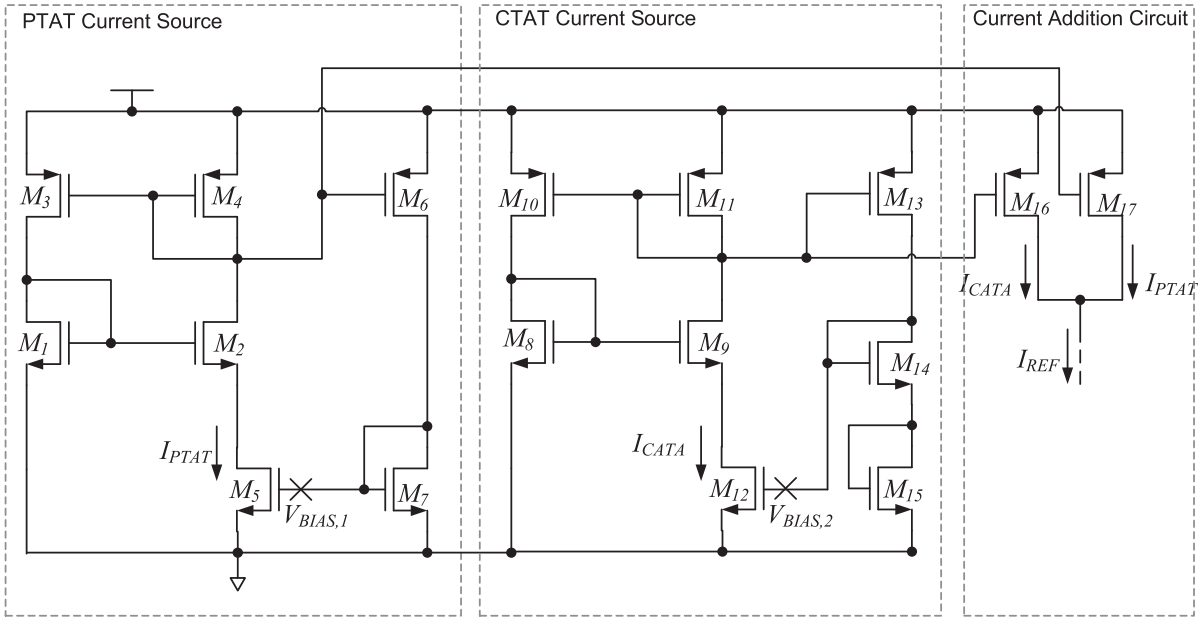


Figure 8.8 Schematic of the current source based reference circuit.

by voltage summation or by current summation. The temperature compensation can also be achieved by combining two complementary thermal properties extracted either from the voltage sources or from the current sources. It can be observed that there is a minimum operating supply voltage requirement for the normal operation of those voltage reference circuits or current reference circuits. For example, the minimum operating supply voltage required for the voltage summation based resistorless reference circuit, the Buck's voltage reference circuit, has to be greater than its output voltage. A below 1 V biasing voltage is needed to bias the Ogeuy's current reference circuit to produce a near-zero *TC* reference current (Hirose *et al.*, 2005). Therefore, the design of resistorless sub-bandgap reference circuit is yet to develop. Lowering the output voltage of the reference circuit not only releases the minimum operating supply voltage requirement, it also promotes the ease of integration of such reference circuits to the design of low power systems.

In this section, we will focus on the techniques that lower the reference voltage to be less than the bandgap voltage. Recall the general form of the first order compensation where

$$V_{REF} = V_{BE_2} + MV_T. \tag{8.22}$$

To achieve $TC = \frac{\partial V_{REF}}{\partial T} = 0$, $M = \frac{\partial V_{BE}}{\partial T} / \frac{\partial V_T}{\partial T}$. Since $\frac{\partial V_{BE}}{\partial T} = -1.73\,\text{mV/K}$ and $\frac{\partial V_T}{\partial T} = 0.09\,\text{mV/K}$, M is required to be 19.22. Moreover, the CTAT voltage $V_{BE_2} = 0.73\,\text{V}$ and the PTAT voltage $V_T = 26\,\text{mV}$ at room temperature. Therefore, the final reference voltage is always close to the bandgap voltage at around 1.2 V. Clearly, the simple method to reduce V_{REF} can be achieved if the CTAT voltage at room temperature can be lowered. Moreover, we can achieve a sub-bandgap voltage reference if either the magnitude of the PTAT *TC* ($\frac{\partial V_T}{\partial T}$) increases or the magnitude of the CTAT *TC* ($\frac{\partial V_{BE_2}}{\partial T}$) decreases, thus lowering the magnitude of M that achieves a near-zero *TC* reference voltage (Sakurai and Sugimoto, 2007).

In addition to the V_{BE} voltage of a bipolar transistor, the threshold voltage, V_{th}, of a MOSFET is a possible CTAT voltage source that can be extracted. When compared to the V_{BE}, V_{th} has lower voltage magnitude at room temperature in a standard CMOS process as discussed in Chapter 1. Moreover, it also has a lower CTAT *TC* than that of V_{BE}. Hence, the use of V_{th} as the CTAT voltage source is one of the common approaches to lower the final reference voltage. The CTAT voltage can be further reduced by biasing the MOSFET into subthreshold mode. However, the V_{th} varies upon its biasing current. Moreover, the noise immunity of the CTAT voltage will be degraded if the MOSFET is biased in subthreshold mode. Hence, special biasing techniques have to be considered to suppress the variation subject to supply voltage change and noise, when the V_{th} of the MOSFET biased in subthreshold mode is adopted as the CTAT device.

8.4.1 The Voltage Summation Approach

One of the easiest ways to achieve a sub-1V voltage reference circuit is to use a diode connected MOSFET biased in the subthreshold mode to replace the diode connected BJT. However, the noise level of the diode connected MOSFET biased in the subthreshold mode is so high that it will tremendously affect the performance of the voltage reference circuit. To lower the noise generated by the voltage reference circuit, Hirose *et al.* (2005) proposed performing voltage

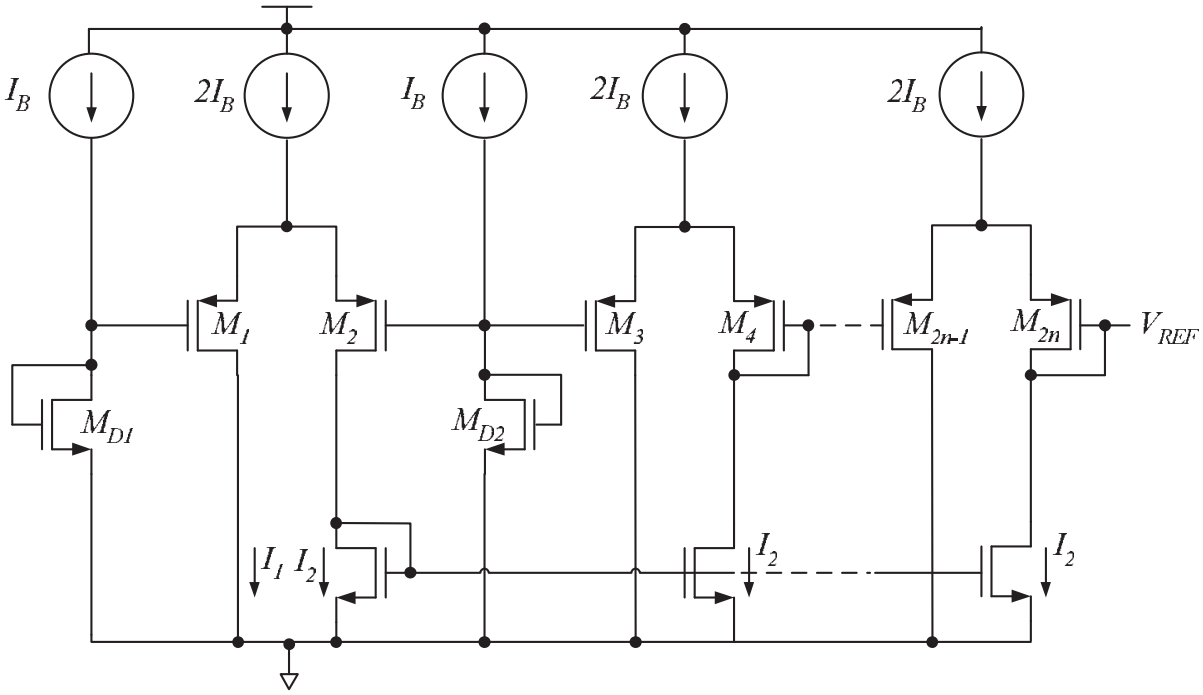


Figure 8.9 A simplified schematic of Hirose's reference circuit (Hirose *et al.*, 2005).

summation by stacking up n differential circuits as shown in Figure 8.9, where $G = 1$, and $A = C$ for each of the differential sub-circuits. As a result, the obtained V_{REF} equals the sum of the gate-to-source voltage of M_{D2} (denoted as $V_{GS_{D2}}$) and the gate-to-gate voltages of the differential pairs (denoted as ΔV_{GS}), and given by

$$V_{REF} = V_{GS_{D2}} + (n-1)\Delta V_{GS_{D1,D2}}, \tag{8.23}$$

where the first $(n-1)$ stage of the differential circuit generates the $(n-1)\Delta V_{GS_{D1,D2}}$ term in Equation 8.23, while the last stage performs the summation with $V_{GS_{D2}}$ to generate V_{REF}. It is clear that Hirose's voltage reference circuit is a modified Buck's voltage reference circuit (Buck *et al.*, 2002) discussed in Section 8.3.1. Instead of performing a series of voltage sums through stacking differential circuits, Buck's voltage reference circuit performs the scaling directly through voltage multiplications. As we have learned from Section 1.7.2, the voltage summation approach can achieve $(n-1)$-time lower noise when compared to the voltage multiplication appraoch of Buck's voltage reference circuit.

The drawback of such a circuit is the high demand in the device matching requirement across all n differential circuits. Second, although the use of the subthreshold mode transistor helps to reduce the power consumption of the voltage reference circuit, the power supply rejection ratio, and all sorts of noise immunity of the circuit will be inevitably degraded. Last but not least, the generated reference voltage is obtained by first order compensation, hence, the *TC* will be small only within a limited temperature range. This is especially true because of the highly nonlinear temperature dependency of $V_{GS_{D1,D2}}$ obtained from MOSFETs biased at the subthreshold region (Rincon-Mora, 2002). The situation is further worsened by the fact that the voltage reference circuit is a sub-1V voltage reference circuit.

The following section will discuss a CTAT voltage reduction scheme that makes use of BJT as the thermal device to obtain sub-1V voltage reference such as to avoid all awkward circuit problems with MOSFETs working in the subthreshold.

8.4.2 CTAT Voltage Reduction

To enhance the robustness of the voltage reference circuit and to pursue a better noise immunity, an improved CTAT voltage reduction circuit was proposed by Tam *et al.* in 2010 (Tam *et al.*, 2010). Similarly, Tam's voltage reference circuit modifies Buck's voltage reference circuit (Buck *et al.*, 2002) presented in Section 8.3.1 by replacing the CTAT V_{BE} of the bipolar transistors with the V_{th} of a MOSFET. However, Tam's voltage reference circuit does not bias the transistors in the subthreshold mode, such that the noise immunity and stability of the reference voltage is compatible with that of the Buck's voltage reference circuit with BJT as CTAT voltage source. Moreover, Tam's voltage reference circuit makes use of a self-biased system to provide the required biasing current, such that no restriction of a dedicated current source is needed. Figure 8.10 shows the schematic of the core circuitry of Tam's voltage reference circuit, which includes the sub-1V generation circuit, the CTAT voltage reduction circuit, and a self-biased current source. Compared to the Buck's voltage reference circuit, the CTAT voltage V_{BE_2} of the bipolar transistor Q_2, is not directly adopted as the CTAT voltage. A CTAT voltage reduction circuit as shown in Figure 8.10 (the circuit inside the dotted box) is implemented to manipulate the V_{BE_2} and to generate a reduced CTAT voltage.

The CTAT voltage reduction circuit is formed by a differential pair with active current loads and identical input voltages at both terminals. As a result, $V_{SUB} = V_{GS_9} = V_{th,n}$. The NMOS

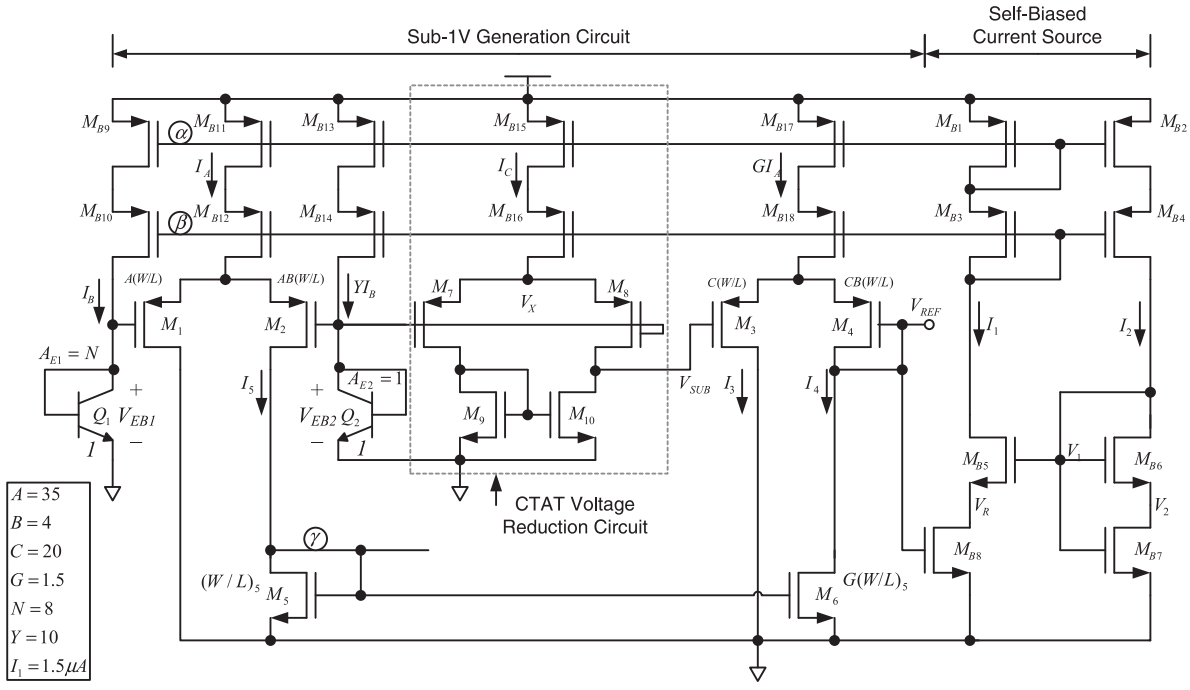


Figure 8.10 Schematic of the sub-1V resistorless CTAT voltage reduction based bandgap voltage reference circuit (Tam *et al.*, 2010).

transistor threshold voltage, $V_{th,n}$, equals 0.48 V at room temperature and has $|\frac{\partial V_{th,n}}{\partial T}| \approx 0.779$ mV/°C, which is smaller than 1.73 mV/°C of $|\frac{\partial V_{BE}}{\partial T}|$ and is closer to 0.09 mV/°C of $|\frac{\partial V_T}{\partial T}|$. Biasing the differential pair M_7 and M_8 at saturation mode will improve the gain, and thus improve the line regulation of V_{SUB}. The CTAT voltage reduction circuit will satisfy

$$|V_{GS7}| - |V_{th_7}| \leq |V_{DS_7}| \tag{8.24}$$

$$V_X - V_{G7} - |V_{th,p}| \leq V_X - V_{th,n} \tag{8.25}$$

$$V_{G7} + |V_{th,p}| \leq V_{th,n} \tag{8.26}$$

$$V_{G7} \leq V_{th,n} - |V_{th,p}| \tag{8.27}$$

$$V_{G7} \leq 0.01V, \tag{8.28}$$

where the threshold voltages of the NMOS and the PMOS are 0.48 V and −0.47 V, respectively, the minimum voltage required to be presented at the gate terminal of M_7 is found to be 0.01 V as depicted in Equation 8.28. Therefore, a base-emitter connected NPN transistor which provides $V_{BE} = 0.73$ V can be used to obtain the required voltage as shown in Figure 8.10. With reference to Equation 8.21, the output voltage V_{REF} of the proposed sub-1V voltage reference circuit in Figure 8.10 is given by

$$V_{REF} = V_{SUB} + \sqrt{AG/C}\ln(NY)\Delta V_{BE_{1,2}}, \tag{8.29}$$

where $N = A_{E1}/A_{E2}$ is the ratio of the emitter areas of Q_1 to that of Q_2, and $Y = I_{BE_2}/I_{BE_1}$ is the ratio of the base-to-emitter currents of Q_2 to that of Q_1. Note that the CTAT and PTAT voltages of this voltage reference circuit are given by V_{SUB} and $\Delta V_{BE_{2,1}}$, respectively. The same as for the other first order compensated circuit, a near-zero TC reference voltage can be obtained by a weighted sum of the CTAT and the PTAT terms, where the weighting factor herein is given by $M = \sqrt{AG/C}\ln(NY)$. When the core circuit is properly biased by a current source and with $Y = 10$ and $N = 8$, the required M is found to be 5.06, and the generated $V_{REF} = 635$ mV. Note that the factor B is set to be greater than 1, thus biasing all the transistors in the core circuit to operate in saturation mode.

8.4.2.1 Self-Biased Current Source

Compared to the Hirose's voltage reference circuit, Tam's voltage reference circuit can operate with different current sources. However, to achieve better line regulation, a self-biased β-multiplier current source as shown in Figure 8.10 can be used. The MOSFET M_{B8} is biased in linear mode by V_{REF}, which forms a close loop circuit. The current source of the $\beta-$multiplier circuit is proportional to the voltage-controlled on-resistance $R_{DS_{B8},ON}$ of M_{B8}, which is given by

$$R_{DS_{B8},ON} = 1/[\mu_n C_{ox} S_{B8}(V_{OUT} - V_{th,n} - V_R)], \tag{8.30}$$

where $\mu_n C_{ox}$ and S_{B8} are the process transconductance of the NMOS and the aspect ratio of M_{B8}, respectively. A cascode current mirror formed by PMOS transistors (M_{B1}, M_{B2}, M_{B3}, M_{B4}), and a current mirror formed by NMOS transistors (M_{B5}, M_{B6}, M_{B7}) are adopted to enhance the line regulation of the voltage reference circuit further. Noted that implementing the cascode current mirror will reduce the line regulation by half, but it will also increase the minimum operating supply voltage of the voltage reference circuit.

Recall the subthreshold current equation, Equation 1.18, in Chapter 1. The subthreshold current of MOSFET M_x can be approximated as $I_x = S_x I_{Dx} \exp(\frac{V_{GSx}}{\zeta V_T})$, where S_x is the aspect ratio, I_{Dx} is the drain-to-substrate current, V_{GSx} is the gate-to-source voltage. As a result, the current that flows through both transistors M_{B6} and M_{B7}, which are biased in subthreshold mode, is given by

$$I_2 = S_{B7} I_{D_7} \exp(V_1/\zeta V_T), \tag{8.31}$$

$$= S_{B6} I_{D_6} \exp(V_1 - V_2)/\zeta V_T. \tag{8.32}$$

This implies $V_2 = \zeta V_T \ln(S_{B6}/S_{B7})$. Current I_1 is determined by the transistor ratio of the current mirror formed with M_{B3} and M_{B4} and constrained by the current flowing through M_{B5}, such that

$$I_1 = \frac{S_{B3}}{S_{B4}} I_2 = S_{B5} I_{D_5} \exp\left(\frac{V_1 - V_R}{\zeta V_T}\right). \tag{8.33}$$

Substituting Equation 8.31 into Equation 8.33 will yield $V_R = \zeta V_T \ln(\frac{S_{B4} S_{B5}}{S_{B3} S_{B7}})$. If we further substitute $I_1 = V_R/R_{DS,ON}$, $V_R = V_{OUT} - V_{th,n}$ and solve for $TC = \frac{1}{I_1}\frac{\partial I_1}{\partial T} = 0$ we will obtain

$$V_{REF} - V_{th,n} = \frac{\frac{\partial V_{th,n}}{\partial T}}{\frac{1}{\mu}\frac{\partial \mu}{\partial T} - \frac{1}{V_T}\frac{\partial V_T}{\partial T}} + V_{th,n} \approx 130\ \text{mV}, \tag{8.34}$$

where the term $\frac{1}{\mu}\frac{\partial \mu}{\partial T}$ is being ignored because it is comparatively small. As a result, $V_{REF} \approx 634$ mV at $T = T_{(nom)}$, which is close to the voltage provided by the core circuit. To obtain a near-zero TC reference voltage, the output of the voltage reference core circuit has to be PTAT which will compensate the CTAT property of the β-multiplier current source. In this case both the reference voltage, and the output of the β-multiplier current source will have a near-zero TC.

8.4.2.2 Piecewise Curvature Compensation

Similarly to all first order temperature compensated voltage reference circuits, a small TC can only be obtained in a limited temperature range due to the high order temperature dependency of the CTAT current source. To achieve a reference voltage with small TC over a wide temperature range, piecewise curvature compensation technique can be applied. Considering the circuit in Figure 8.11, it generates a first order PTAT current, I_{COMP}. When the operating temperature T equals or is greater than a pre-determined temperature T_{COMP}, which is the

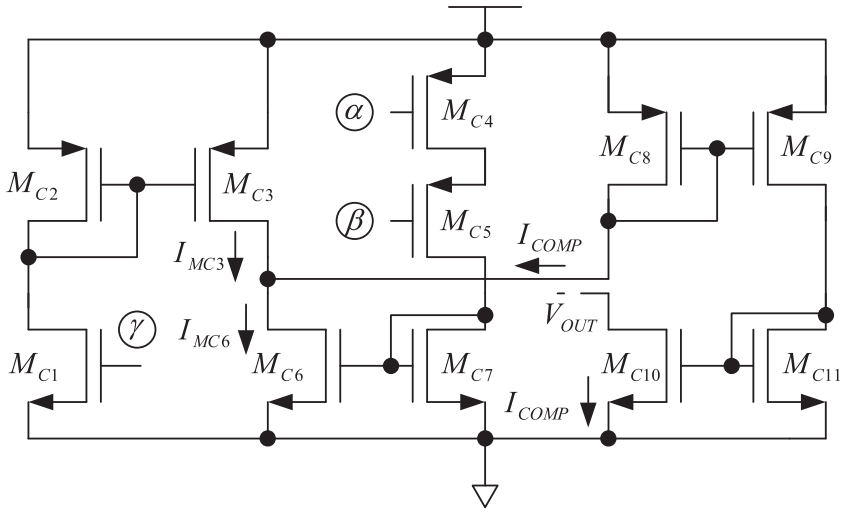


Figure 8.11 Schematic of the piecewise curvature compensation circuit of Tam's reference (Tam *et al.*, 2010).

temperature where the high order temperature dependent terms of the CTAT V_{SUB} begins to dominate, the current at the output branch of the voltage reference circuit is subtracted by I_{COMP}, thus superimposing a first order PTAT voltage onto the output of the reference circuit and compensating the high order temperature dependent terms of the CTAT term.

The I_{COMP} is generated by subtracting a PTAT current (I_5 in Figure 8.10) with a near-zero TC current (I_1 in Figure 8.10). I_5 and I_1 are copied from the core circuit to the piecewise curvature compensation circuit by the current mirrors formed by (M_{C2}, M_{C3}) and (M_{C6}, M_{C7}), respectively. The current levels can be adjusted by the transistor size ratio of the current mirror, such that $I_{COMP} = I_{M6} - I_{M3} \geq 0$ for $T \geq T_{COMP}$. The PTAT current I_{COMP} is copied to the voltage reference core circuit by current mirror formed by $M_{C8} \sim M_{C11}$, such that $\widehat{I_3} = I_3 + I_{COMP}$ and $\widehat{I_4} = I_4 - I_{COMP}$, where $\widehat{I_3}$ and $\widehat{I_4}$ are the compensated currents flowing through M_3 and M_4 in Figure 8.10. As a result, the reference voltage becomes

$$V_{REF} = V_{SUB} + \sqrt{\frac{AG}{C}}\Delta V_{BE} + \sqrt{\frac{2I_{COMP}(1 - B^{-1})}{\mu_p C_{ox} C(W/L)}}. \tag{8.35}$$

The compensation level can be adjusted by I_{COMP} where

$$I_{COMP} = \begin{cases} P_1 \cdot (I_{M6} - I_{M3}) & T \geq T_{COMP}, \\ 0 & T < T_{COMP}, \end{cases} \tag{8.36}$$

with

$$I_{M3} = P_2 \cdot \zeta \mu_n C_{ox} S_{B8} V_T (V_{OUT} - V_{th,n}) \ln\left(\frac{S_{B4} S_{B5}}{S_{B3} S_{B7}}\right), \tag{8.37}$$

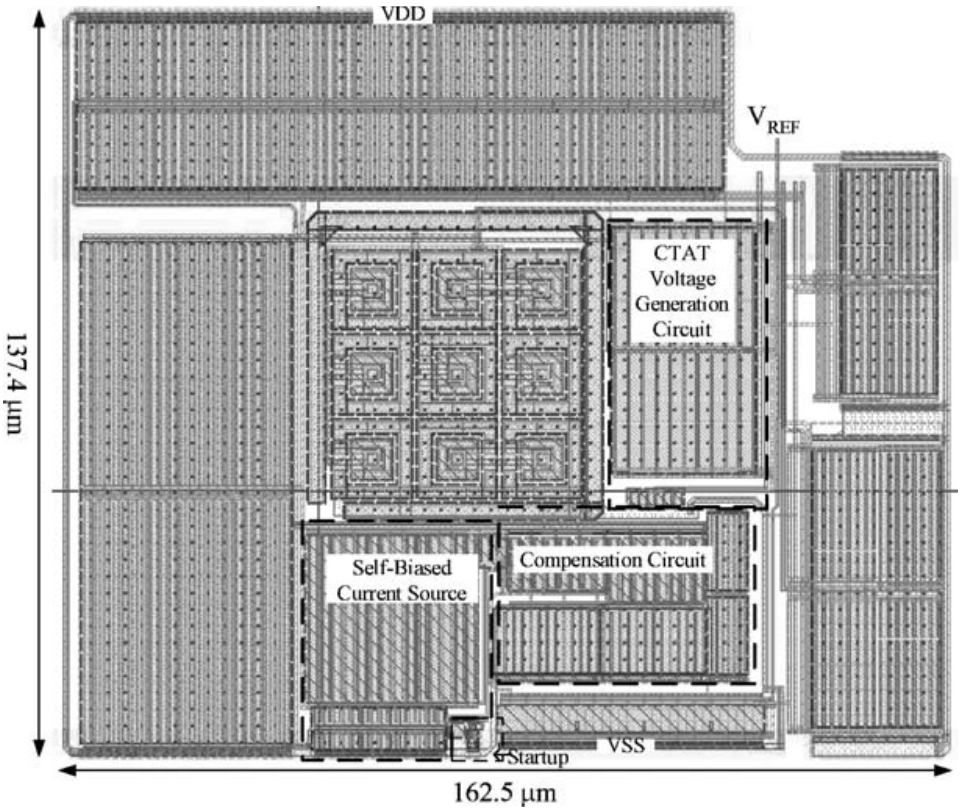


Figure 8.12 Layout of the sub-1V resistorless CTAT voltage reduction based bandgap voltage reference circuit (Tam *et al.*, 2010). The cell size 137.4 μm × 162.5 μm.

and

$$I_{M6} = P_3 \cdot \frac{1}{2}\mu_p C_{ox} AB \cdot S_2(V_{BE2} - V_x - |V_{th,p}|), \tag{8.38}$$

where $P_1 = \frac{S_{MC10}S_{MC8}}{S_{MC11}S_{MC9}}$, $P_2 = \frac{S_{MC3}S_{M5}}{S_{MC2}S_{MC1}}$ and $P_3 = \frac{S_{MC6}S_{MB4}}{S_{MC7}S_{MC4}}$ are the current mirror transistor size ratios, which are also equal to the current ratios.

Figure 8.12 shows the silicon layout of the resistorless voltage reference circuit in Figure 8.10 using the 0.18 μm technology considered in this book. The silicon area of the circuit is 0.022 mm^2. The layout of the circuit follows the matching and placement rules presented in Chapter 4. The BJTs, as the major thermal devices in this circuit, are placed at the center of the entire layout such as to avoid the situation being unable to sense any localized self heating in the rest of the silicon when this voltage reference is applied as part of the circuit in any SoC. With the introduction of piecewise curvature compensation circuit, a small *TC* of 9.617 ppm/°C (or ±0.0673%) in the temperature range of $-10\,^{\circ}\text{C} \sim 130\,^{\circ}\text{C}$ was achieved.

Figure 8.13 shows the temperature dependency obtained from V_{REF} of the circuit at different supply voltages from 1.5 V to 2.4 V. It is observed that the circuit shows a high order temperature dependency. Consider the curve at $V_{DD} = 1.8$ V, the V_{REF} is observed to achieve a local maximum at 60 °C, which is precisely where T_{COMP} is chosen. The value of T_{COMP} adjusted by the appropriate setting of P_1, P_2, and P_3, which in our case were chosen to be 0.625, 1.667, and 0.6, respectively. The value of T_{COMP} varies with V_{DD} which is caused

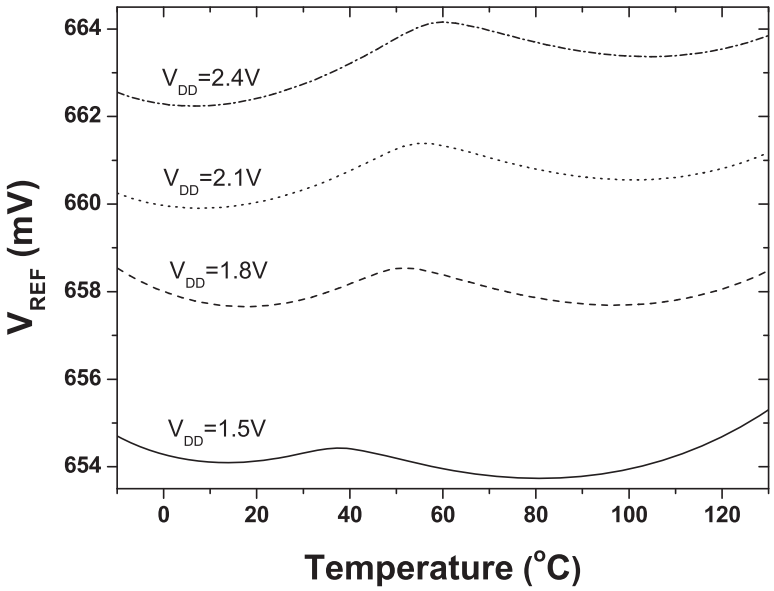


Figure 8.13 Temperature dependency of V_{REF} obtained from the sub-1V resistorless CTAT voltage reduction based bandgap voltage reference circuit (Tam *et al.*, 2010) at different supply voltages.

by the variation of the biasing current I_1. This variation will also limit the line regulation of the circuit which is measured to be 1.78% when the circuit is implemented without the cascode current mirrors. With the introduction of cascode current mirrors, the line regulation was reduced to 0.89%, much lower than that of the voltage reference circuits used in a commercial integrated circuit which is around 2%. However, the minimum supply voltage of the voltage reference circuit with cascode current mirror will be increased to $V_{DD(min)} = V_{OUT} + |V_{th,p}| + V_{DSB_{18},SAT} + V_{DSB_{17},SAT} \approx 1.408$ V, where $V_{DSB_{17},SAT}$ and $V_{DSB_{18},SAT}$ are the V_{DS} of $M_{B_{17}}$ and $M_{B_{18}}$ in saturation mode. This analytical $V_{DD(min)}$ value is shown to be very close to the 1.5 V measured from the SPICE simulation.

Figure 8.14 shows the *TC* and *PSRR* of the reference voltages obtained by the voltage reference circuit in Figure 8.10 under different supply voltages. It is found that the reference voltage with the smallest *TC* is obtained at $V_{DD} = 1.8$ V and is equal to 9.617 ppm/°C and the maximum *TC* is found to be 20.4 ppm/°C which is obtained when $V_{DD} = 2.4$ V. This validates the efficiency of the piecewise temperature compensation circuit. In the same figure, the *PSRR* of the reference voltage is observed to be lower than −34 dB under various V_{DD}, and has an optimal value of −42.1 dB at $V_{DD} = 1.8$ V. Such a good performance in *PSRR* is achieved by biasing most of the transistors in saturation mode with the application of cascode current mirrors. The drawback is the increased minimum operating supply voltage. The *PSRR* of the reference voltage degrades comparatively severely when the supply voltage is lower than 1.6 V. The degradation is caused by insufficient supply voltage headroom which hurts the linearity of the current mirrors. Large supply voltage headroom is required because the cascode current mirrors have been adopted to promote the line regulation of the voltage reference circuit. Though the *PSRR* is lower than −40 dB with supply voltage below 1.7 V, this voltage reference circuit is able to achieve a *PSRR* lower than −34 dB with supply voltage down to 1.5 V, which should be applicable to most of the applications implemented in the

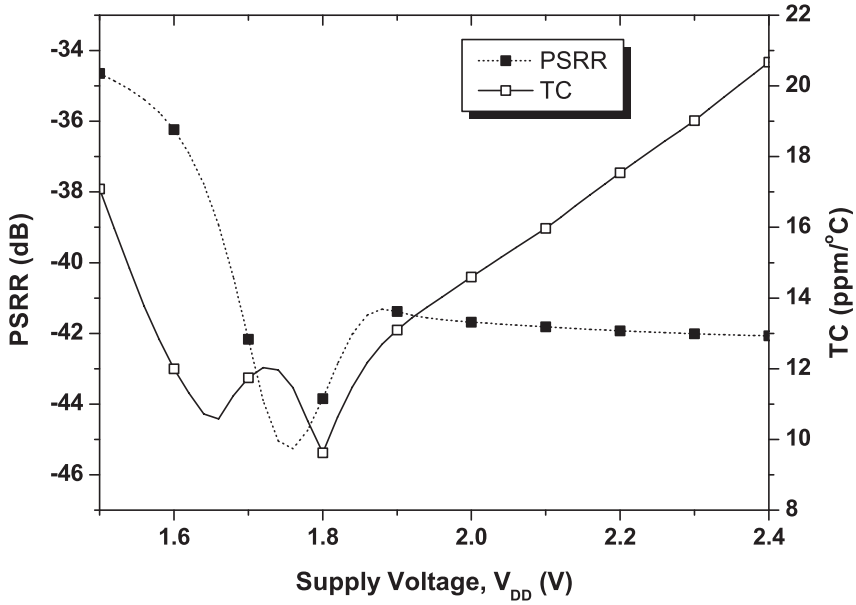


Figure 8.14 Plots of temperature coefficient (*TC*) and power supply rejection ratio (*PSRR*) as functions of supply voltage (V_{DD}) for the sub-1V resistorless CTAT voltage reduction based bandgap voltage reference circuit (Tam *et al.*, 2010).

0.18 μm process where the nominal supply voltage usually starts from 1.5 V. The simulated root-mean-squares (RMS) noise measured at V_{REF} at room temperature with 1.8 V supply voltage over 1 Hz to 100 kHz was found to be 76.18 $\mu V/\sqrt{Hz}$, which is comparable to most commercially available voltage reference circuits.

8.5 Summary

In this chapter, we have reviewed the pros and cons of constructing resistor free voltage reference circuits. We have analyzed the operations of several exemplary resistor free voltage reference circuits. Although the temperature compensation topologies of the presented circuits are variants of the traditional $V_{BE} - \Delta V_{BE}$ technique, when implemented with the inverse function technique and negative impedance converter technique, the use of a resistor can be avoided. Both of these techniques make use of the forward and inverse conversions between current and voltage, or vice versa, to achieve the necessary scaling of the temperature sensitive current or voltage required in the $V_{BE} - \Delta V_{BE}$ compensation topology. In particular Buck's voltage reference circuit (Buck *et al.*, 2002) makes use of the weighted differential circuit to produce the inverse function pairs. However, the generated reference voltage is the same as the bandgap voltage, and thus cannot be applied in sub-1V voltage reference circuit design. To achieve sub-1V reference voltage, the $V_{BE} - \Delta V_{BE}$ temperature compensation topology is replaced with $V_{th} - \Delta V_{GS}$ compensation with MOSFET biased in the subthreshold mode. Such a voltage reference circuit has been discussed by Hirose *et al.* in (Hirose *et al.*, 2005), where a self-biasing circuit is applied to stabilize the subthreshold biased MOSFETs. The drawbacks are the tight transistor matching requirement and the high susceptibility of the reference voltage to thermal noise as the MOSFETs are biased at subthreshold (refer to Section 1.7.1,

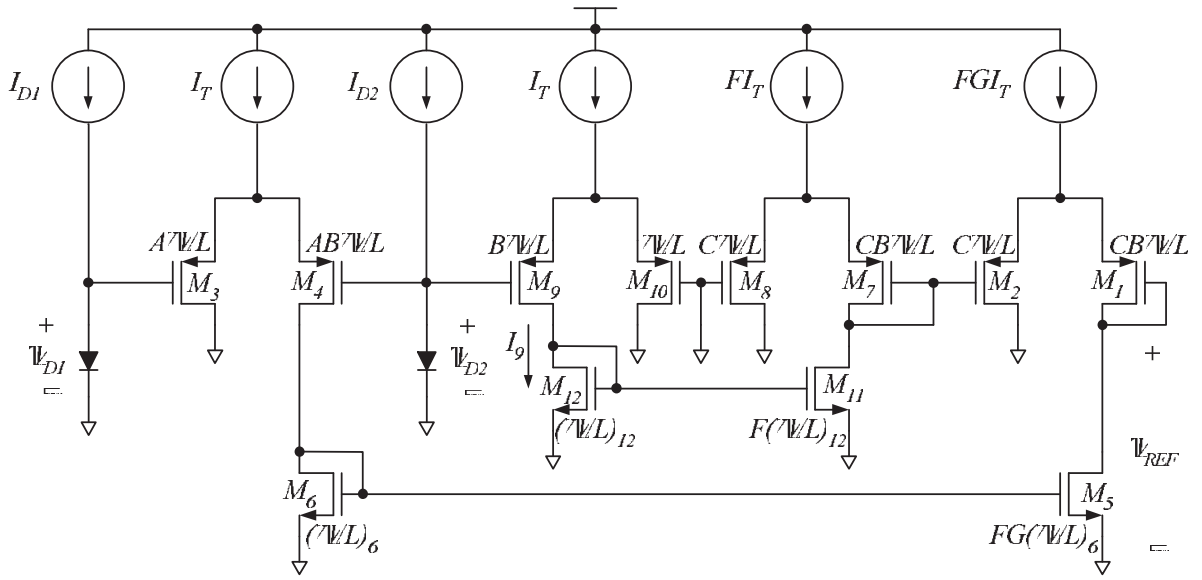


Figure 8.15 Sub-1V output voltage resistorless bandgap voltage reference for Exercise 8.1.

MOSFETs biased to work in the subthreshold mode will have high channel resistance, thus generates high thermal noise). To tackle the high noise susceptibility problem, Hirose *et al.* proposed to cascade n differential circuits to achieve the required weighting factor $(n-1)$ through a series of voltage sums instead of directly applying a $(n-1)$-weighted differential circuit. The idea is similar to that presented in Section 1.7.1.1, where the sum of $(n-1)$ identical independent sources can achieve a scaling factor of $(n-1)$ which has less thermal noise than that obtained by scaling the source with an amplifier of gain $(n-1)$. To further reduce the noise level in the generated reference voltage, the MOSFETs cannot be biased to work in subthreshold mode. Tam *et al.* (Tam *et al.*, 2007, 2010) presented a voltage reference circuit that modifies Hirose's voltage reference circuit to have all the transistors biased in linear or saturation mode, while still able to generate sub-1V reference voltage.

8.6 Exercises

Exercise 8.1 *(Sub-*1V *voltage reference) The voltage scaling method using the transimpedence circuit can be used to scale the CTAT voltage in the resistorless voltage reference circuit in Figure 8.4 to generate a reference voltage that is lower than bandgap voltage. Figure 8.15 shows such a circuit.*

1. *Compute* $V_{GS10} - V_{GS9}$*, and* $V_{GS8} - V_{GS7}$*, and write* V_{D2} *as a linear function of* $(V_{GS8} - V_{GS7})$.
2. *Compute an expression for* $\Delta V_{D_{2,1}} = V_{D2} - V_{D1}$ *as a linear function of* $V_{GS2} - V_{GS1}$.
3. *Compute an expression for* V_{REF} *as a linear function of* V_{D2} *and* $\Delta V_{D_{2,1}}$.
4. *Describe how can we achieve a sub-*1V *reference voltage.*
5. *Choose an appropriate set of MOSFET sizes and current sources to generate SPICE simulation results on* V_{DD} *versus* V_{REF}.

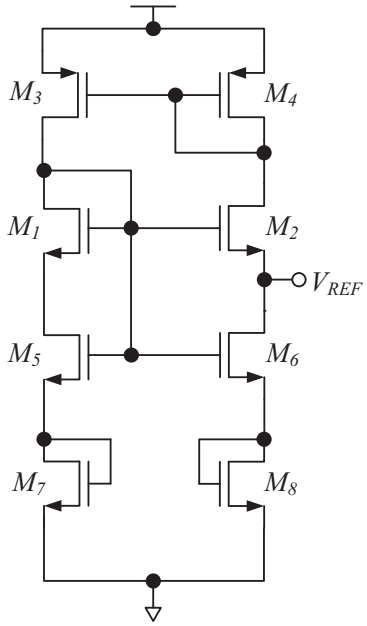


Figure 8.16 Resistor free voltage reference circuit for Exercise 8.2.

6. *Think of one reason why the constructed bandgap voltage reference circuit may not work in real world implementation (hint: consider the operating current of each transistors).*

Exercise 8.2 *Figure 8.16 shows a resistor free voltage reference circuit consisting of 8 transistors M_1 to M_8. Transistors M_1 to M_4 are biased to be operated in the saturation mode. Transistors M_5 and M_6 are biased in the triode mode, both behave as voltage controlled resistors and further maintain the symmetry in the circuit. Transistors M_7 and M_8 are biased to work in the subthreshold region and are connected to form a diode. Assume the gate bias obtained from the common gate node of M_1 and M_2 is sufficient to keep M_5 and M_6 to operate in triode region, derive the output V_{REF}.*

References

Brennan, R.L., Viswanathan, T.R. and Hanson, J.V. (1988) The CMOS negative impedance converter. *IEEE Journal of Soil-State Circuits*, **23** (5), 1272–75.

Buck, A.E., McDonald, C.L., Lewis, S.H. *et al.* (2002) A CMOS bandgap reference without resistors. *IEEE Journal of Solid-State Circuits*, **37** (1), 81–3.

Hirose, T., Asai, T. and Amemiya, Y. (2008) Temperature-compensated CMOS current reference circuit for ultralow-power subthreshold LSIs. *IEICE Electronics Express*, **5** (6), 204–210.

Hirose, T., Matsuoka, T., Taniguchi, K. *et al.* (2005) Ultralow-power current reference circuit with low temperature dependence. *IEICE Transactions on Electronics*, **E88-C** (6), 1142–47.

Ming, X., Ma, Y.Q., Zhou, Z.K. *et al.* (2010) A high-precision compensated CMOS bandgap voltage reference without resistors. *IEEE Transactions on Circuits and Systems II: Express Briefs*, **57** (10), 767–71.

Oguey, H.J. and Aebischer, D. (1997) CMOS current reference without resistance. *IEEE Journal of Solid-State Circuits*, **32** (7), 1132–35.

Rincon-Mora, G.A. (2002) *Voltage Reference-from Diodes to Precision High-order Bandgap Circuits*, Wiley.

Sakurai, H. and Sugimoto, Y. (2007) The realization of an area-efficient CMOS bandgap reference circuit with less than 1.25 V of output voltage using a fractional v_{BE} amplification scheme. *IEICE Transactions on Electronic*, **E90-C** (2), 499–506.

Tam, W.S., Mok, K.Y., Wong, O.Y. *et al.* (2007) High-performance resistorless sub-1V bandgap reference circuit based on piecewise compensation technique *Proceedings of IEEE Conference on Electron Devices and Solid-State Circuits*, pp. 373–76.

Tam, W.S., Wong, O.Y., Kok, C.W. *et al.* (2010) Generating sub-1V reference voltages from a resistorless CMOS bandgap reference circuit by using a piecewise curvature temperature compensation technique. *Microelectronics Reliability*, **50** (8), 1054–61.

Torrance, R., Viswanathan, T. and Hanson, J. (1985) CMOS voltage to current transducers. *IEEE Transaction on Circuits and Systems*, **32** (11), 1097–104.

Vittoz, E. and Fellrath, J. (1977) CMOS analog circuits based on weak inversion operation. *IEEE Journal of Solid State Circuits*, **12** (3), 224–31.

A

SPICE Model File

```
.PARAM
*1.8V core NMOS
+DTOX_NM      = 0   DXL_NM       = 0   DXW_NM       = 0
+DVTH_NM      = 0   DCJ_NM       = 0   DCJSW_NM     = 0
+DCJSWG_NM    = 0   DCGDO_NM     = 0   DCGSO_NM     = 0
*
*1.8V core PMOS
+DTOX_PM      = 0  DXL_PM        = 0   DXW_PM       = 0
+DVTH_PM      = 0  DCJ_PM        = 0   DCJSW_PM     = 0
+DCJSWG_PM    = 0  DCGDO_PM      = 0   DCGSO_PM     = 0
*
*1.8V CORE NPN
+DBF_NPN      = 0.00      DIS_NPN   = 0.00     DNF_NPN    = 0.00
+DCJE_NPN     = 0.00      DCJC_NPN  = 0.00
*
.model nm nmos
+LEVEL    = 49
*
* GENERAL PARAMETERS
*
+LMIN     = 1.5E-7              LMAX     = 1.0E-5          WMIN     = 1.9E-7
+WMAX     = 1.0E-4              TNOM     = 25.0            VERSION  = 3.2
+TOX      = '3.87E-09+DTOX_NM'  TOXM     = 3.87E-09        XJ       = 1.60E-07
+NCH      = 3.869E+17           LLN      = 1.121           LWN      = 0.920
+WLN      = 1.060               WWN      = 0.877           LINT     = 1.576E-08
+LL       = 2.635E-16           LW       = -2.263E-16      LWL      = -2.058E-22
+WINT     = -1.445E-09          WL       = -2.367E-16      WW       = -3.641E-14
+WWL      = -4.00E-21           MOBMOD   = 1               BINUNIT  = 2
+XL       = '1.0E-8+DXL_NM'     XW       = '0.00+DXW_NM'   DWG      = -5.96E-09
+DWB      = 4.50E-09
* DIODE PARAMETERS
+ACM      = 12                  LDIF     = 7.00E-08        HDIF     = 2.00E-07
+RSH      = 7.08                RD       = 0.00            RS       = 0.00
+RSC      = 1.7                 RDC      = 1.7
*
* THRESHOLD VOLTAGE PARAMETERS
*
+VTH0     = '0.4018+DVTH_NM'    WVTH0    = -2.971E-08          PVTH0    = 5.00E-16
+K1       = 0.6801              WK1      = -2.4897E-08         PK1      = 1.30E-15
+K2       = -4.998E-02          K3       = 10.0                DVT0     = 1.30
+DVT1     = 0.577               DVT2     = -0.172              DVT0W    = 0.00
```

CMOS Voltage References: An Analytical and Practical Perspective, First Edition. Chi-Wah Kok and Wing-Shan Tam.
 Published 2013 by John Wiley & Sons Singapore Pte. Ltd.

```
+DVT1W    = 0.00               DVT2W    = 0.00               NLX      = 7.545E-08
+W0       = 5.582E-07          K3B      = -3.00
*
* MOBILITY PARAMETERS
*
+VSAT     = 8.250E+04       PVSAT    = -8.30E-10      UA       = -1.03E-09
+LUA      = 7.735E-19       PUA      = -1.00E-24      UB       = 2.3667E-18
+UC       = 1.20E-10        PUC      = 1.50E-24       RDSW     = 55.55
+PRWB     = -0.240          PRWG     = 0.40           WR       = 1.00
+U0       = 3.40E-02        LU0      = 2.306E-11      WU0      = -3.101E-09
+A0       = 0.830           KETA     = -3.000E-03     LKETA    = -1.700E-09
+A1       = 0.00            A2       = 0.99           AGS      = 0.32
+B0       = 6.00E-08        B1       = 0.00
*
* SUBTHRESHOLD CURRENT PARAMETERS
*
+VOFF     = -0.103         LVOFF    = -3.30E-09      NFACTOR  = 1.25
+LNFACTOR = 4.50E-08       CIT      = 0.00           CDSC     = 0.00
+CDSCB    = 0.00           CDSCD    = 1.00E-04       ETA0     = 2.800E-02
+ETAB     = -2.700E-02     DSUB     = 0.4000000
*
* ROUT PARAMETERS
*
+PCLM     = 1.20           PPCLM    = 3.00E-15       PDIBLC1  = 2.50E-02
+PDIBLC2  = 3.80E-03       PPDIBLC2 = 2.70E-16       PDIBLCB  = 0.00
+DROUT    = 0.56           PSCBE1   = 3.45E+08       PSCBE2   = 1.00E-06
+PVAG     = 0.00           DELTA    = 1.00E-02       ALPHA0   = 1.775E-08
+ALPHA1   = 0.176          LALPHA1  = 7.625E-09      BETA0    = 11.168
*
* TEMPERATURE EFFECTS PARAMETERS
*
+KT1      = -0.2573        KT2      = -4.00E-02      AT       = 3.70E+04
+PAT      = -7.50E-10      UTE      = -1.55          UA1      = 1.76E-09
+LUA1     = 6.00E-18       WUA1     = -1.10E-16      PUA1     = -5.00E-25
+UB1      = -2.40E-18      UC1      = -1.00E-10      LUC1     = 1.7E-17
+PUC1     = -3.00E-24      KT1L     = -1.00E-09      PRT      = -55.00
*
* CAPACITANCE PARAMETERS
*
+CJ       = '9.68E-04+DCJ_NM'     MJ       = 0.346               PB       = 0.7
+CJSW     = '7.95E-11+DCJSW_NM'   MJSW     = 0.538               PBSW     = 1
+CJSWG    = '4.18E-10+DCJSWG_NM'  MJSWG    = 0.538               PBSWG    = 1
+TCJ      = 8.42E-04              TCJSW    = 6.69E-04            TCJSWG   = 6.69E-04
+TPB      = 1.47E-03              TPBSW    = 8.68E-04            TPBSWG   = 8.68E-04
+JS       = 3.52E-07              JSW      = 3.0E-13             NJ       = 1.04
+XTI      = 3.25                  NQSMOD   = 0                   ELM      = 5
+CGDO     = '3.70E-10+DCGDO_NM'   CGSO     = '3.70E-10+DCGSO_NM' TLEVC    = 1
+CAPMOD   = 3                     XPART    = 1                   CF       = 0.00
+ACDE     = 0.64                  MOIN     = 24                  NOFF     = 1.203
+DLC      = 8.5E-09               DWC      = 4.5E-08
+NLEV     = 3                     AF       = 0.85                KF       = 1.5E-24
*
.model pm pmos
+LEVEL    = 49
*
* GENERAL PARAMETERS
*
+LMIN     = 1.5E-7             LMAX     = 1.0E-5         WMIN     = 1.9E-7
+WMAX     = 1.0E-4             TNOM     = 25.0           VERSION  = 3.2
+TOX      = '3.74E-09+DTOX_PM' TOXM     = 3.74E-09       XJ       = 1.70E-07
+NCH      = 5.50E+17           LLN      = 1.00           LWN      = 1.00
```

```
+WLN      = 1.045               WWN      = 1.00           LINT     = 1.00E-08
+LL       = 3.40E-15            LW       = -3.36E-16      LWL      = 0.00
+WINT     = 8.00E-09            WL       = 3.59E-15       WW       = -1.90E-15
+WWL      = -1.12E-21           MOBMOD   = 1              BINUNIT  = 2
+XL       = '-4.0E-09+DXL_PM'   XW       = '0.00+DXW_PM'  DWG      = -1.74E-08
+DWB      = 2.00E-08
* DIODE PARAMETERS
+ACM      = 12                  LDIF     = 7.00E-08       HDIF     = 2.00E-07
+RSH      = 7.83                RD       = 0.00           RS       = 0.00
+RSC      = 1.5                 RDC      = 1.5
*
* THRESHOLD VOLTAGE PARAMETERS
*
+VTH0     = '-0.395+DVTH_PM'    WVTH0    = 1.2675E-08     PVTH0    = -1.25E-15
+K1       = 0.587               LK1      = 3.553E-09      K2       = 7.0907E-03
+K3       = 2.60                DVT0     = 0.719          DVT1     = 0.247
+DVT2     = 7.89E-02            DVT0W    = 0.00           DVT1W    = 8.00E+05
+DVT2W    = 0.00                NLX      = 9.00E-08       W0       = 0.00
+K3B      = 2.486               NGATE    = 3.168E+20
*
* MOBILITY PARAMETERS
*
+VSAT     = 1.00E+05       UA       = 2.85E-10       LUA      = 5.50E-18
+PUA      = -2.00E-24      UB       = 1.00E-18       UC       = -4.77E-11
+WUC      = 3.167E-17      PUC      = -2.50E-24      RDSW     = 4.55E+02
+PRWB     = -0.40          PRWG     = 0.00           WR       = 1.00
+U0       = 8.661E-03      LU0      = -2.00E-11      WU0      = 1.382E-10
+A0       = 1.00           KETA     = 2.00E-02       LKETA    = -8.50E-09
+PKETA    = 5.00E-16       A1       = 0.00           A2       = 0.99
+AGS      = 0.20           B0       = 6.30E-08       B1       = 0.00
*
* SUBTHRESHOLD CURRENT PARAMETERS
*
+VOFF     = -9.50E-02      LVOFF    = -1.70E-09      WVOFF    = -1.99E-09
+PVOFF    = -1.00E-16      NFACTOR  = 0.90           LNFACTOR = 1.00E-07
+PNFACTOR = -5.00E-15      CIT      = 0.00           CDSC     = 0.00
+CDSCB    = 0.00           CDSCD    = 0.00           ETA0     = 4.00E-02
+ETAB     = -2.50E-02      DSUB     = 0.56
*
* ROUT PARAMETERS
*
+PCLM     = 0.70           PDIBLC1  = 0.00           PDIBLC2  = 7.00E-03
+PDIBLCB  = 0.00           DROUT    = 0.56           PSCBE1   = 4.00E+08
+PSCBE2   = 1.00E-07       PVAG     = 0.00           DELTA    = 1.00E-02
+ALPHA0   = 7.00E-08       ALPHA1   = 7.049          BETA0    = 22.84
+LBETA0   = -7.50E-08
*
* TEMPERATURE EFFECTS PARAMETERS
*
+KT1      = -0.258          KT2      = -3.098E-02     LKT2     = -3.00E-09
+PKT2     = -6.53E-16       AT       = 1.00E+04       PAT      = -1.00E-09
+UTE      = -1.270          UA1      = 5.3867E-10     WUA1     = 1.10E-16
+PUA1     = -2.37E-24       UB1      = -2.071E-18     UC1      = 2.061E-11
+KT1L     = -8.00E-09       PRT      = 90.0
*
* CAPACITANCE PARAMETERS
*
+CJ       = '0.001+DCJ_PM'          MJ       = 0.415          PB       = 0.817
+CJSW     = '9.89E-11+DCJSW_PM'     MJSW     = 0.489          PBSW     = 1.00
+CJSWG    = '5.07E-10+DCJSWG_PM'    MJSWG    = 0.489          PBSWG    = 1.00
+TPB      = 0.00153                 TPBSW    = 0.00117        TPBSWG   = 0.00117
```

```
+TCJ      = 0.000876              TCJSW    = 0.000745            TCJSWG   = 0.000745
+JS       = 1.66E-07              JSW      = 1.2E-13             NJ       = 1.0384
+XTI      = 4.5                   NQSMOD   = 0                   ELM      = 5
+CGDO     = '4.20E-10+DCGDO_PM'   CGSO     = '4.20E-10+DCGSO_PM' TLEVC    = 1
+CAPMOD   = 3                     XPART    = 1                   CF       = 0.00
+ACDE     = 0.851                 MOIN     = 14.95               NOFF     = 1.43
+DLC      = -1.5E-09
+NLEV     = 3                     AF       = 1.15                KF       = 3E-23
*
.model NPN4 npn
+LEVEL    = 1
+VAF      = 38.0                IKF      = 1.50E-03
+ISE      = 1.15E-16            NE       = 1.48                BR       = 0.271
+NR       = 1.007               VAR      = 21.782              IKR      = 1.30E-03
+ISC      = 5.80E-16            NC       = 1.43                RB       = 200.0
+IRB      = 1.00E-04            RBM      = 0.1                 RE       = 18.0
+RC       = 25.0                XTI      = 3.0                 EG       = 1.16
+TREF     = 25.0                NKF      = 0.5                 TLEV
+TLEVC    = 1                   SUBS     = 1                   TBF1     = 6.1E-03
+TBR1     = 8.50E-04            TIKF1    = -3.0E-03            TNE1     = 2.5E-04
+CTC      = 1.2E-3              CTE      = 8.42E-4             TVJC     = 1.9E-3
+VJE      = 0.7                 MJE      = 0.346
+VJC      = 0.693               MJC      = 0.343
+TVJE     = 0.00147
+IS       = '2.80E-18+DIS_NPN'
+BF       = '28.2+DBF_NPN'
+NF       = '1.01+DNF_NPN'
+CJC      = '3.43E-14+DCJC_NPN'
+CJE      = '3.87E-15+DCJE_NPN'
*
```

B

SPICE Netlist of Voltage Reference Circuit

```
.SUBCKT opamp v_neg v_pos vbias vdd vout vss
*.PININFO v_neg:I v_pos:I vbias:I vout:O vdd:B vss:B
C1 net9 vout 150f
M11 vout net9 vss vss NM W=16.7u L=580.00n
M9 net15 net15 vss vss NM W=2u L=580.00n
M10 net9 net15 vss vss NM W=2u L=580.00n
M6 vout vbias vdd vdd PM W=32u L=300.00n
M4 net26 vbias vdd vdd PM W=8u L=300.00n
M8 net9 v_pos net26 vdd PM W=8u L=300.00n
M7 net15 v_neg net26 vdd PM W=8u L=300.00n
.ENDS
```

```
.SUBCKT refcir IBIAS VDD VREF VSS
*.PININFO VREF:O IBIAS:B VDD:B VSS:B
XI0 net8 net35 IBIAS VDD net24 VSS opamp
Q1 net8 net8 VSS NPN4
Q3 net13 net13 VSS NPN4
Q2 net7 net7 VSS NPN4 M=8
R2 VREF net13 81.7K
R1 net35 net7 9K
M5 IBIAS IBIAS VDD VDD PM W=8u L=300n
M1 net8 net24 VDD VDD PM W=10u L=1u
M3 VREF net24 VDD VDD PM W=10u L=1u
M2 net35 net24 VDD VDD PM W=10u L=1u
.ENDS
```

CMOS Voltage References: An Analytical and Practical Perspective, First Edition. Chi-Wah Kok and Wing-Shan Tam.
 Published 2013 by John Wiley & Sons Singapore Pte. Ltd.

INDEX

Bandgap voltage reference, 71
  Widlar, 71
β-multiplier, 77, 170–73
  Cascode current mirror, 172
  Channel length modulation, 172
    Alleviation, 173
  Loop gain, 172
  Self-bias, 170
  Voltage headroom, 171
  Voltage reference, 170
BJT (Bipolar Junction Transistor), 1–5, 39, 94, 122, 125
  A_E (base-emitter voltage), 3
  Base-emitter voltage, 3
  Base resistance, 122
  β (current gain), 2, 122, 125
  Collector current, 3
  ΔV_{BE} (differential V_{BE}), 5
  Gummel and Poon model, 1
  Layout, 2, 94
  Parameter, 39
  $\partial V_{BE}/\partial T$ (V_{BE} temperature dependency), 4
  Series resistance, 122
  Size, 122
BJT free CTAT, 178
Brokaw bandgap voltage reference, 168, 170
  Output driving, 170
  Supply voltage headroom, 170
  Trimming, 170

Channel length modulation, 23, 75, 86, 107, 115, 116, 172, 177, 179–81, 205, 209, 213
  β-multiplier, 172
    Alleviation, 180
  $V_{GS} - \Delta V_{GS}$, 180
    Alleviation, 180
  Widlar current source, 177
Common mode input range, *see* Operational Amplifier
CTAT (Complementary to absolute temperature), 4, 178, 224
  BJT free, 178
  Taylor expansion, 224
Current mirror, 86–8, 114–15, 117, 121, 137, 275, 277
  Active bias, 88
  Cascode, 87, 117, 275, 277
  Channel length modulation, 86, 107, 115–16
    Alleviation, 116
    Drain voltage equalization, 116
      Resistor, 116
  Mismatch, 111, 114
  Output impedance, 87, 117, 121, 137
  Simple, 87
  Supply voltage headroom, 86
Curvature Compensation, 223
Curvature correction, 223
Curvature error, 74, 79

Device matching, *see* Layout
Differential pair, *see* Weighted differential circuit
Differential V_{GS}, 13, 16
  Saturation, 16
  Subthreshold, 13
Diode, 23–4
  Diode connected BJT, 24
  Diode connected MOSFET, 24
Drain voltage equalization, 74, 116
Dropout voltage, 52
Dummy element, *see* Layout
Dynamic performance, *see* Voltage reference

Equal ripple, 241
Error amplifier, 75

Guard ring, *see* Layout

CMOS Voltage References: An Analytical and Practical Perspective, First Edition. Chi-Wah Kok and Wing-Shan Tam.

Input offset, 82
Intrinsic gain, 20
Inversion function, 259–60
  Current-to-voltage conversion, 260
  Function pair, 260
  Transconductance, 260
  Transimpedance, 260
  Voltage-to-current conversion, 260

Layout, 2, 8, 26–8, 30, 85, 88, 94–5, 122
  BJT, 2, 94, 122
  Centro-symmetric, 30, 94, 122
  Cross-couple, 26, 85, 88
  Device matching, 28
    Variation
      Random, 28
      Systematic, 30
  Dummy element, 27
  Guard ring, 27, 95
  Inter-digitization, 26, 30, 85, 88
  MOSFET, 8
  Opamp based β-multiplier bandgap voltage reference circuit, 95
  R_{sheet} (sheet resistance), 27
Line regulation, 51, 79
Load regulation, 202
  Opamp based β-multiplier bandgap voltage reference
    Resistive division, 202
Loop gain, 77, 84, 172
  β-multiplier, 172

Minimum operating voltage, 52, 79, 83, 86, 108, 171, 180, 195, 201, 207, 214, 245
  β-multiplier, 171
  ΔV_{GS}
    Supply voltage headroom, 214
  Opamp based β-multiplier bandgap voltage reference, 79, 195
    Resistive division, 201
    Independent biased resistive divided V_{BE}, 207
  Similar temperature dependency, 245
  $V_{GS} - \Delta V_{GS}$, 180
Modified sensitivity parameter, *see* Sensitivity parameter
MOSFET (Metal-Oxide Semiconductor Field-Effect Transistor), 6–23, 39, 198–9, 214
  Body effect, 199
  Bulk driven, 199, 214
  Channel length modulation effect, 23
  Cutoff, 11
  Differential V_{GS}, 13
    Subthreshold, 13
    Saturation, 16
  Effective voltage, 14
  g_m (transconductance), 20
    Thermal property, 21
  Linear, 14
  Low V_{th}, 198
  μ (carrier mobility), 19
    Thermal property, 19
      β_{mu}, 19
  Parameter, 39
  Pinched-off, 16
  Saturation, 16
  S (channel width to length ratio), 12
  Strong inversion, 14
  Subthreshold, 11
    ζ (subthreshold slope), 12
  Thermal property, 19
  Triode, 14
  V_{GS} (gate source voltage), 21
    Subthreshold, 22
    Thermal property, 21
      $\beta_{gs,sub}$, 22
  V_{th} (threshold voltage), 8, 214
    $V_{th,n}$ (NMOSFET threshold voltage), 8
    $V_{th,p}$ (PMOSFET threshold voltage), 8
    Extraction, 18
    Thermal property, 19
      β_{th}, 19
  Weak inversion, 11

Near zero temperature coefficient, 71
NIC (Negative impedance converter), 262–6
  CMOS implementation, 264
  Current control, 263–4
    Negative impedance, 264
    Voltage inversion, 264
  h-parameter transfer function, 263
  Resistorless, 264
  Voltage control, 263–4
    Negative impedance, 264
    Current inversion, 264
Noise, 36–8, 60, 113, 128, 132, 140, 201, 208
  Color, 132
  Density, 60
  $1/f$ (flicker), 38
  Multiplication, 38
  Opamp based β-multiplier bandgap voltage reference, 138, 208
    Opamp, 113
    Resistive division, 201
  Power supply, 128
  RC filter, 140
  Reference voltage, 60
  Shot, 37
  Sum, 38
  Thermal, 36
  White, 60

Nominal reference voltage, 50
Nominal supply voltage, 50

Opamp based β-multiplier bandgap voltage reference circuit, 77, 79, 81–2, 95, 103, 106–108, 110–17, 120, 122, 125–6, 132, 135, 138, 195, 199, 201, 207
  Bipolar transistor, 110, 122
    Base current, 110
    Base resistance, 122
    β (current gain), 110, 122, 125
    Series resistance, 122
    Size, 122
  Cascode cross-couple, 107, 111
  Current mirror, 114
    Cascode, 117
    Channel length modulation, 115–16
    Mismatch, 114
  Curvature error, 79
  Error source, 103
  Independent biased resistive divided V_{BE}, 206
    Supply voltage headroom, 207
  Input offset, 82
  Layout, 95
  Line regulation, 79, 112, 117
  Load regulation, 202
  Loop gain, 84
  Minimum operating voltage, 79, 108, 111, 117, 132, 195, 201, 207
  Noise, 113, 138, 208
  Opamp, 103
    Bootstrap bias, 112
    Input offset, 104
      Cascode cross-couple, 107
      Series connection, 108
      Transistor emitter area ratio, 106
      Transistor emitter current ratio, 106
    Limited gain, 112
    Noise, 113
    $PSRR$ (Power supply rejection ratio), 112
    Self bias, 112
  Output loading, 135
  Pre-regulation, 132
  Quiescent current, 107, 111
  $PSRR$ (Power supply rejection ratio), 120, 126
    RC filter, 132
  Resistive divided V_{BE}, 202
  Resistive division, 199
    Load regulation, 202
    Noise, 201
    Supply voltage headroom, 201
  Resistor, 126
  Small signal, 126
  Transistor level schematic, 81
  Trimming, 140
    Current, 141, 149
    Modulation, 146
    Voltage, 141, 148
Operational Amplifier (Opamp), 81–4, 104, 112, 131, 135, 196–7, 201–202, 204, 208, 215
  Bootstrap bias, 112
  Bulk driven, 215
  Common mode input range, 196–7, 201–202, 204
  DC gain, 83
  Gain bandwidth, 131
  Input common mode voltage, 84
  Input offset, 82, 104, 135, 202, 208
  Input stage, 197
  Limited gain, 112
  Minimum operating voltage, 83
  Open loop gain, 83
  $PSRR$ (Power supply rejection ratio), 112
  Self bias, 112

Peaking current source, 209, 249, 251
Piecewise linear compensation, *see* Temperature compensation, and Voltage reference
Pre-regulation, 132
Probe pad, 141
Process control, 32–3
  Fast, 33
  Slow, 33
Process corner, 34
  Statistical, 34
  Worst case, 34
$PSRR$ (power supply rejection ratio), 56, 120, 213
PTAT (proportional to absolute temperature), 6, 224
  Taylor expansion, 224

Quasi-equilibrium state, 77
Quiescent current, 59, 107, 245

Resistive division, 193, 199
  Opamp based β-multiplier bandgap voltage reference, 199
Resistor, 25–7, 93
  End effect, 26
  Network, 93
  Resistor type, 27
  R_{sheet} (sheet resistance), 25
  T_{CR} (temperature coefficient), 26–7
  V_{CR} (voltage coefficient), 26
Resistorless, 265–7, 269–73
  Current source, 265–7
  Current sum, 270
  Sub-bandgap, 270–73
    Voltage reduction, 273
    Voltage sum, 271
  Voltage source, 265
  Voltage sum, 269

Second order current source, 229–31
  Sink, 231
Self-bias, 112, 170, 175, 179, 209, 273–4
  β-multiplier, 170
  Current source, 274
  Resistorless, 273–4
Sensitivity parameter, 50
  Modified, 50
Silicon bandgap voltage, *see* V_{G0}
Similar temperature dependency, 227
  See also Temperature compensation, and Voltage reference
Startup, 77, 90–91
  Current drain, 91
  Current injection, 90
  Time, 90
Static performance, *see* Voltage reference
Sub-1V voltage reference, 191, 193, 202, 206, 209, 211
  Independent biased resistive divided V_{BE}, 206
  Peaking current source, 211
  Peaking current source and V_{BE}, 209
  Resistive division, 193
  Resistive divided V_{BE}, 202
  Sub-1V supply voltage, 191
  Weighted ΔV_{GS}, 211
    Power supply rejection ratio, 213
    Supply voltage headroom, 214
Supply voltage boosting, 198

Temperature coefficient, 54, 71
  Near zero, 71
Temperature compensation, 223–7, 275, 277
  First order, 224
  Multipoint, 227
  Multisection, 226
  Order, 224
  Piecewise linear, 226, 275, 277
  Second order, 225, 228
  Similar temperature dependency, 227
  Third and higher order, 225
Thermal voltage, 3, 6
  $\partial V_T/\partial T$ (V_T temperature dependency), 6
Trimming, 33, 140–43, 146, 148–9, 170
  Accuracy, 143
  Anti-fuse, 142
  Brokaw bandgap voltage reference, 170
  Current, 149
  Down-trimming, 142
  Dynamic, 142
  Functional, 142
  Linked fuse, 141
    Blow-tie, 141
  Modulation, 146
    Procedure, 146
  Probe pad, 141
  Static, 142
  Up-trimming, 142
  Voltage, 148
Typical design, 32
Variation, 28, 30
  Random, 28
  Systematic, 30
V_{GS} current source, 178
V_{G0} (silicon bandgap voltage at 0 K), 3
Voltage reference, 49, 52, 54, 56, 59–60, 78, 166, 168, 170, 175, 177, 180, 228, 232, 236, 238, 240, 243–50
  Brokaw, 168
  Dropout voltage, 52
  Linear regulation, 51
  Minimum operating voltage, 52
  Multi-threshold voltage, 247
    Difference, 250
  Noise, 60
  Performance measure, 49
    Dynamic, 50
    Static, 49
  Piecewise linear, 240
  $PSRR$ (power supply rejection ratio), 56
  Quiescent current, 59
  Second order, 228
    BJT current subtraction, 238
    Current addition, 236
    Current subtraction, 232
  Similar temperature dependency, 243
    Difference, 244
    Quiescent current, 245
    Sum, 245
    Supply voltage headroom, 245
  Temperature coefficient, 54
  $V_{BE} - \Delta V_{BE}$, 166
    β-multiplier, 170
  $V_{GS} - \Delta V_{GS}$, 177
    Supply voltage headroom, 180
  $V_{REF\text{-}CONV}$, 78
  Widlar, 166
  Widlar-V_{BE}, 175

$V_{REF\text{-}CONV}$, 78

Weighted differential circuit, 260, 262, 265, 269
  Differential pair, 260
  Weighted difference voltage, 262
Widlar bandgap voltage reference, 71, 166
Widlar current source, 175
  Channel length modulation, 177
  Current consumption, 177