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REGULAR PAPER

Compact 0.3-to-1.125 GHz self-biased phase-locked loop for system-on-chip clock generation in 0.18 μm CMOS

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In this paper, we propose a compact ring-oscillator-based self-biased phase-locked loop (SBPLL) for system-on-chip (SoC) clock generation. It adopts the proposed triple-well NMOS source degeneration voltage-to-current (*V–I*) converter instead of the operational amplifier (OPAMP) based *V–I* converter and a proposed simple start-up circuit with a negligible area to save power and area. The SBPLL is implemented in the 0.18 μm CMOS process, and it occupies 0.048 mm^2 active core. The measurement results show the SBPLL can generate output frequency in a wide range from 300 MHz to 1.125 GHz with a constant loop bandwidth that is around 5 MHz and a relatively low jitter performance that is less than 4.9 mUI over the entire covered frequency range. From −20 to 70 °C the rms jitter variation and loop bandwidth variation at 1.125 GHz are 0.2 ps and 350 kHz, respectively. The rms jitter performance variation of all covered frequency points is less than 10% in the supply range from 1.5 to 1.7 V. Such SBPLL shows robustness over environmental variation. The maximum power consumption is 5.6 mW with 1.6 V supply at an output frequency of 1.125 GHz.

1. Introduction

The phase-locked loop (PLL) is the critical building block that is widely used in many system-on-chip (SoC) systems. There are several design challenges in the design of such PLLs. First, the PLL should cover a wide frequency range to meet different frequency requirements of building blocks such as a universe serial bus (USB) interface, low-voltage differential signal (LVDS), and dynamic random-access memory (DRAM). Secondly, the jitter should be relatively low to meet tightly timing constraint in some high speed building blocks. Thirdly, because of the need for the implementation of multiple PLLs in some SoC systems, low power and area efficiency are necessary. Last but not least, insensitivity to environmental variation is also required.

There are mainly two kinds of PLLs: the LC-oscillator-based PLL (LC-PLL)[1–6] and the ring-oscillator-based PLL (RPLL).[7–13] The LC-PLLs show superior phase-noise performance at the cost of large area. LC oscillators need a multiple-switched-capacitors array[14–16] and auto-frequency calibration (AFC)[17–19] techniques to expand the tuning range, which raise the design complexity of the PLL. The RPLL is more attractive than the LC-PLL for SoC applications because it has the advantages of small area and large tuning range, but the phase noise is much worse than that of the LC-PLL, and may greatly degrade the jitter performance. To improve the jitter performance, several techniques were presented in prior works. The sub-sampling PLL (SSPLL)[20] can increase the phase detector gain and thus suppress the in-band phase noise and jitter. However, it has a relatively narrow capture range and high spur level. The sub-harmonically injection-locked PLL (SILPLL)[21] was proposed to suppress the either the in-band or the out-band phase noise, but complicated calibration is need to adjust the injection timing and to avoid the issue of losing locking. In addition, the spur level is also relatively high.

An alternative way of designing PLLs that meet the SoC requirement is to adopt the self-biased PLL (SBPLL).[22–25] The loop bandwidth to reference frequency ratio can be kept relatively constant with the help of matched passive components regardless of the output frequency, and process, voltage, and temperature (PVT) variations. Having such advantages, a wide loop bandwidth can be set to suppress the phase noise of the ring oscillator and thus achieve low jitter performance without the issue of stability due to the PVT variation. However, the SBPLL has a complex structure[22,23] that leads to large area or high power consumption. Although the SBPLL was much simplified,[24,25] but more than one operational amplifier (OPAMP) is needed, leading to high power consumptions and the occupation of a large area.

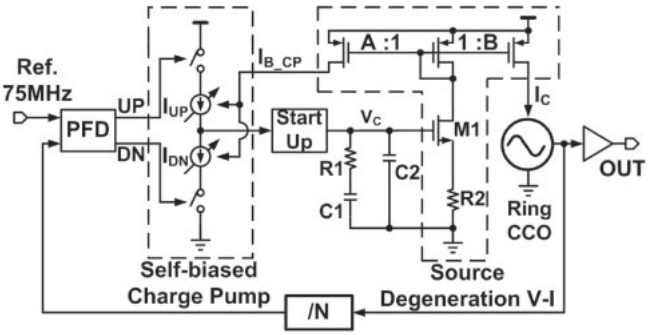


Fig. 1. Block diagram of proposed SBPLL.

We propose a compact ring oscillator based SBPLL. It adopts a triple-well NMOS source degeneration voltage-to-current (*V–I*) converter instead of the operational amplifier (OPAMP)-based *V–I* converter and a simple start-up circuit with a negligible area to save power and area. The SBPLL can operate with a constant loop bandwidth in a wide range of output frequency and shows relatively low jitter. It occupies an active area of only 0.048 mm^2 in an inexpensive 0.18 μm CMOS process, which is a good choice for the clock generation of a low-cost SoC application.

2. Architecture of proposed SBPLL

2.1 Overall architecture

Figure 1 shows the block diagram of the proposed SBPLL. It consists of a phase/frequency detector (PFD), self-biased charge pump, start-up circuit, loop filter (LPF), source degeneration *V–I* converter, ring current-controlled oscillator

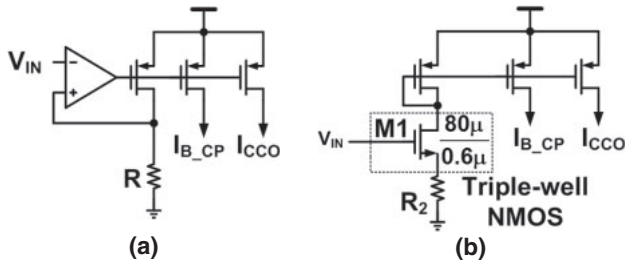


Fig. 2. Schematic of (a) OPAMP based *V–I* converter and (b) proposed triple-well NMOS source degeneration *V–I* converter.

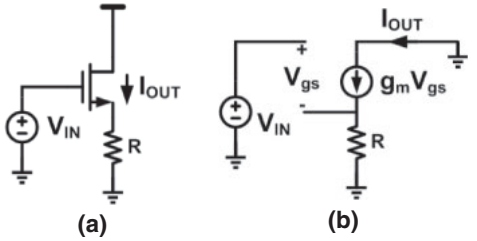


Fig. 3. (a) Simplified schematic of source degeneration *V–I* converter and (b) its small signal model.

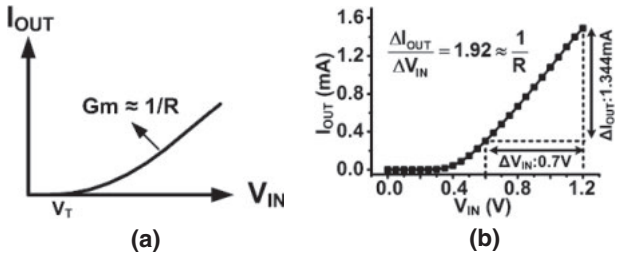


Fig. 4. (a) Theoretical transfer curve and (b) simulated transfer curve of the source degeneration *V–I* converter.

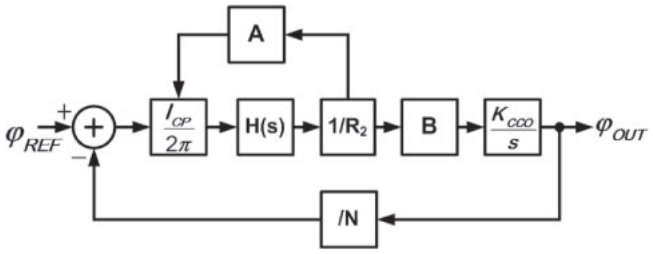


Fig. 5. Linear model of proposed SBPLL.

(RCCO), frequency divider and output buffer. The proposed triple-well NMOS source degeneration *V–I* converter replaces the OPAMP based *V–I* converter to save power and area. The detailed performance comparison in detail between the two kinds of *V–I* converter is presented in Sect. 3. The proposed simple start-up circuit with a negligible area ensures a robust start-up operation of the SBPLL. Thus the SBPLL can robustly generate a wide range of output frequency with relatively low jitter. As shown in Fig. 1, the CP current is set proportional to the control current of the RCCO to keep the loop bandwidth to reference frequency ratio relatively constant. In order to suppress the phase noise contributed from RCCO, the reference clock is set to be a relatively high frequency of 75 MHz so that the loop bandwidth can be set to be as large as 5 MHz. The frequency divider and PFD are implemented with truly single-phase clock logic (TSPC) to lower the power consumption while maintaining high operation speed.

The proposed SBPLL adopts the proposed triple-well NMOS source degenerated *V–I* converter instead of the OPAMP-based *V–I* converter,[24] as shown in Fig. 2. The source degenerated *V–I* converter consists of only four MOS transistors and one degeneration resistor R_2, which is much simpler than the OPAMP-based *V–I* converter. Therefore, the power consumption and area of the proposed SBPLL can be reduced. Figure 3 shows a simplified schematic of the source degenerated *V–I* converter and its small signal model. The transfer function of such a *V–I* converter can be written as

$$G_{\mathrm{m}} = \frac{I_{\mathrm{out}}}{V_{\mathrm{in}}} = \frac{g_{\mathrm{m}}}{1 + g_{\mathrm{m}}R}, \tag{1}$$

where g_{m} is the transconductance of the NMOS transistor. As V_{in} increases, g_{m} also rises, and G_{m} tends to be $1/R$, as shown in Fig. 4(a). In order to increase the linearity of G_{m}, a large width/length ratio and low threshold voltage V_{T} are needed for NMOS to achieve larger g_{m} under the same input voltage V_{in}. In our design, the source and body terminals of the triple-well NMOS transistor M1 shown in Fig. 2(b) are connected together to avoid the body effect. In addition, the triple-well NMOS has better noise isolation performance, compared with the normal NMOS. The channel width and length of M1 are chosen to be 80 and 0.6 μm. The long channel can reduce the V_{T} by means of the reverse short-channel effect.[26] The simulation result shows that M1 has V_{T} of about 300 mV, which is a relatively low value in the 0.18 μm process. The simulated transfer curve of the proposed source degeneration *V–I* converter in this SBPLL is shown in Fig. 4(b). The source degeneration resistor used in the *V–I* converter is 450 Ω. As shown in Fig. 4(b), the simulation result can matches well with the theoretical analysis result shown in Fig. 4(a).

Figure 5 shows the linear model of proposed SBPLL, where K_{CCO} is the gain of the RCCO and I_{CP} is the current of the CP. As shown in Figs. 1 and 5, the ratio of I_{CP} to the control current of RCCO is A. By analyzing the linear model shown in Fig. 2, the loop bandwidth of the SBPLL can be expressed as

$$\omega_{\mathrm{BW}} \approx \frac{A}{2\pi} \times \frac{R_1}{R_2} \times \omega_{\mathrm{REF}}, \tag{2}$$

where R_1 and R_2 are shown in Fig. 1, and ω_{REF} is the angular frequency of the reference clock. Equation (2) indicates that the loop bandwidth to reference clock frequency ratio can not only be kept constant regardless of the divider ratio N but also is not sensitively to the PVT variation because such a ratio is proportional to the ratio between two matched resistors, R_1 and R_2.

In SBPLL, it is necessary to implement the start-up circuit. Figure 6(a) shows the proposed simple start-up circuit, it consists of only two PMOS transistors, two switches, and one inverter, which occupy an area of only $15 \times 14\,\mu\mathrm{m}^2$, a negligible area. The operation process of SBPLL with the proposed start-up circuit is presented in Fig. 6(b). The operation process mainly includes two phase: the reset phase

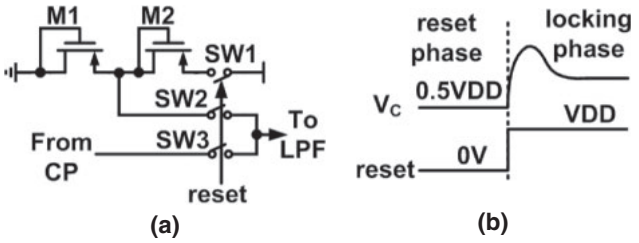


Fig. 6. (a) Schematic of proposed start-up circuit. (b) Operation process of SBPLL.

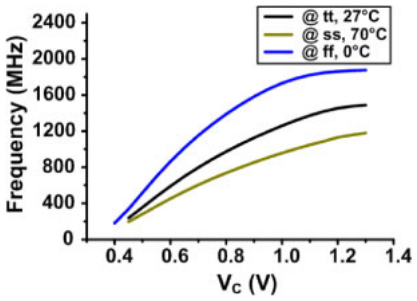


Fig. 8. (Color online) Simulated CCO frequency tuning curve.

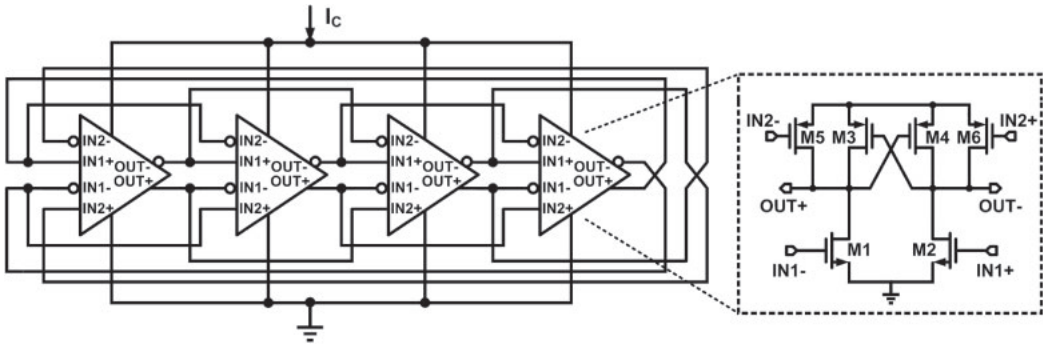


Fig. 7. Schematic of Ring CCO and its delay cell.

and the tracking/locking phase. In the reset phase, the SW1 and SW2 are open and SW3 is closed, the SBPLL loop is open and the control voltage V_C of the LPF is set to be half the supply voltage $V_{DD}/2$ to make the oscillator and the charge pump start to work. In the tracking and locking phase, the reset signal goes high first, then SW2 turns off and SW3 turns on to close the loop and the PLL starts to lock to the desired frequency. By turning SW1 off, the start-up circuit is turned off not only to save power but also to avoid any effect on the PLL frequency tracking and locking. In summary, the SBPLL can start up and lock to the desired frequency correctly and robustly by following above the process.

The reset signal in the start-up circuit can be connected to the global reset signal in the SoC systems, which shows good compatibility to the SoC application.

2.2 Ring CCO

Figure 7 shows the schematic of the RCCO and its delay cell. This CCO is implemented with a four-stage dual-delay path loop[27,28] to achieve higher operation frequency and wide tuning range. The dual-delay path includes both the normal paths and the negative skew paths. The negative skew paths are achieved by adding the secondary differential input signals IN2+ and IN2− to every delay cell. The PMOS M3 and M4 are adopted as the regenerative cross-coupled transistors to achieve fast switching and rail-to-rail output and thus reduce the phase noise of RCCO.

Figure 8 shows the post-layout simulated frequency tuning range of the RCCO at different PVT corner. The RCCO and source degeneration *V–I* converter are connected together to simulate the frequency tuning range by sweeping the control voltage V_C shown in Fig. 1. Figure 8 indicates that the design target frequency range from 0.3 to 1.125 GHz can be achieved at different PVT corners.

2.3 Multi-modules frequency divider, PFD and CP

Figures 9(a) and 9(b) show the frequency divider and its cell, respectively. It is implemented with the three-stage multi-modules frequency divider (MMD) with extended logic to extend the division ratio from 4 to 15. The differential to single-end converter (DTS) is adopted to convert the CCO differential output to the CMOS rail-to-rail single-ended signal. Although the MMD with a current-mode logic (CML) structure[29] can achieve a very high operation speed, it has the drawbacks of high power consumption and large area occupation. Thus in this design, we adopt the TSPC MMD[6] to meet the high-operation-speed requirement with low power and small area. The area is only 0.0013 mm^2 and its simulated power at 1.5 GHz operation frequency is only 0.45 mW.

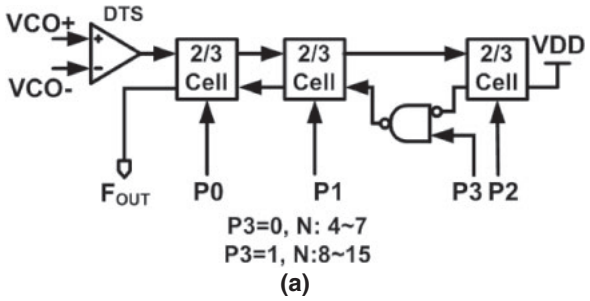
Figure 10 shows the schematic of PFD. Because of the relatively high reference frequency in this SBPLL, the TSPC structure is also adopted in the PFD.[30] Moreover, compared with the classic static PFD, the delay of the reset path can be shorter than that in the TSPC PFD because it has fewer logic gates, which means the phase noise contributed by the PFD and CP can be reduced. In this design, the reset delay is set at about 300 ps. The CP[8] is adopted to achieve fast switching speed and good current matching performance.

3. Performance comparison between the source degeneration *V–I* converter and the OPAMP based *V–I* converter in the SBPLL

In this section, the performance comparison between source degeneration *V–I* converter and the OPAMP based converter in the SBPLL is presented below.

3.1 Noise and power comparison

First we compare the theoretical noise and power performance between the two *V–I* converter. Because the SBPLL phase



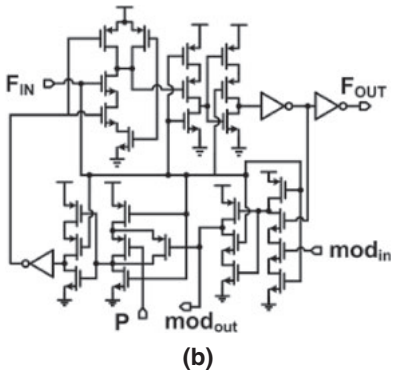


Fig. 9. Schematic of TSPC MMD and its cell.

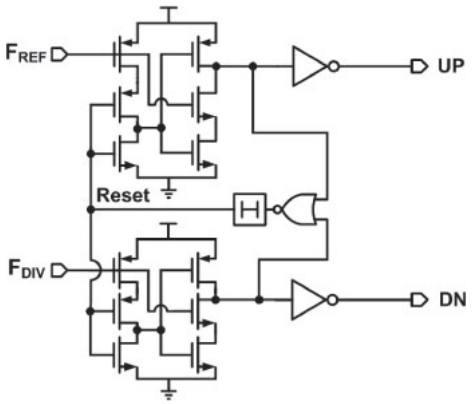


Fig. 10. Schematic of TSPC PFD.

noise contributed from the *V–I* converter shows bandpass character and the SBPLL loop bandwidth is designed to be relatively high, we only consider the impact of the thermal noise and ignore the influence of the low frequency flicker noise. The output current noise of the source degeneration *V–I* converter shown in Fig. 11(a) can be expressed as

$$\overline{I_{\mathrm{n,out2}}^2} = \frac{4KT\gamma_{\mathrm{N}} g_{\mathrm{mA}}}{(1+g_{\mathrm{mA}}R)^2} + 4KT\gamma g_{\mathrm{mB}}, \tag{3}$$

where g_{mA} and g_{mB} are the transconductances of MA and MB shown in Fig. 11(a) and γ_{N} is the thermal noise parameter of NMOS.

Figure 11(b) shows the small signal noise model of the OPAMP-based *V–I* converter. The current noise power of the output current I_{out1} can be expressed as

$$\overline{I_{\mathrm{n,out1}}^2} = \frac{\overline{V_{\mathrm{n,amp}}^2}}{R^2} + \frac{4KT\gamma_{\mathrm{P}} g_{\mathrm{m1}}}{(1+Ag_{\mathrm{m1}}R)^2}, \tag{4}$$

where $V_{\mathrm{n,amp}}$ is the equivalent input noise of the OPAMP, g_{m1} is the transconductance of the M1, A is the gain of the OPAMP and γ_{P} is the thermal noise parameter of PMOS. The

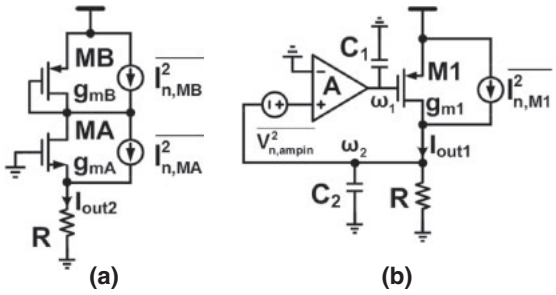


Fig. 11. Schematic of the (a) OPAMP-based *V–I* and (b) source degeneration *V–I* for noise calculation.

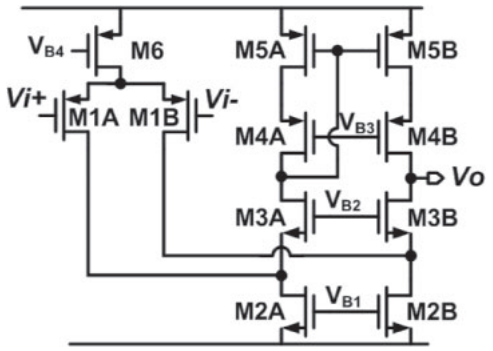


Fig. 12. Schematic of the folded-cascode OPAMP.

second item of Eq. (4) can be ignored owing to the high gain of the OPAMP. The typical folded-cascode OPAMP shown in Fig. 12 is adopted in such a *V–I* converter. The equivalent input noise power can be written as

$$\overline{V_{\mathrm{n,amp}}^2} = 2\left(\frac{4KT\gamma}{g_{\mathrm{m1}}} + \frac{4KT\gamma g_{\mathrm{m2}}}{g_{\mathrm{m1}}^2} + \frac{4KT\gamma_{\mathrm{P}} g_{\mathrm{m5}}}{g_{\mathrm{m1}}^2}\right). \tag{5}$$

And Eq. (4) can be rewritten as

$$\overline{I_{\mathrm{n,out1}}^2} = \frac{2}{R^2}\left(\frac{4KT\gamma_{\mathrm{N}}}{g_{\mathrm{m1}}} + \frac{4KT\gamma_{\mathrm{N}} g_{\mathrm{m3}}}{g_{\mathrm{m1}}^2} + \frac{4KT\gamma_{\mathrm{P}} g_{\mathrm{m5}}}{g_{\mathrm{m1}}^2}\right), \tag{6}$$

where g_{m1}, g_{m3}, and g_{m5} are the transconductances of M1A(B), M3A(B), and M5A(B) shown in Fig. 12, respectively. Equations (3) and (6) indicate that the OPAMP based *V–I* converter has more noise source than the source degeneration one. To achieve the same amount of noise, g_{m1} must be higher than g_{mA}, and thus more power consumption of the OPAMP is needed.

Figures 13(a) and 13(b) show the schematic for simulating the tuning curve and the phase noise of the CCO with the two kinds of *V–I* converter, respectively. The CCOs in Figs. 13(a) and 13(b) are same and the details are shown in Fig. 7. Figure 13(c) shows that the CCO with both two *V–I* converters can achieve a similar linear tuning range. Figure 13(d) shows that the CCO with the source degenerated *V–I* converter has phase noise at least 3 dB lower than that of the CCO with the OPAMP converter. The OPAMP in this simulation consumes 0.36 mW with a 1.6 V supply, which is not a negligible value especially when the SBPLL generates low-frequency clock.

Thus both the theoretical and the simulation results show that the source degeneration *V–I* converter can achieve better noise performance than the OPAMP-based converter with less power consumption and smaller area.

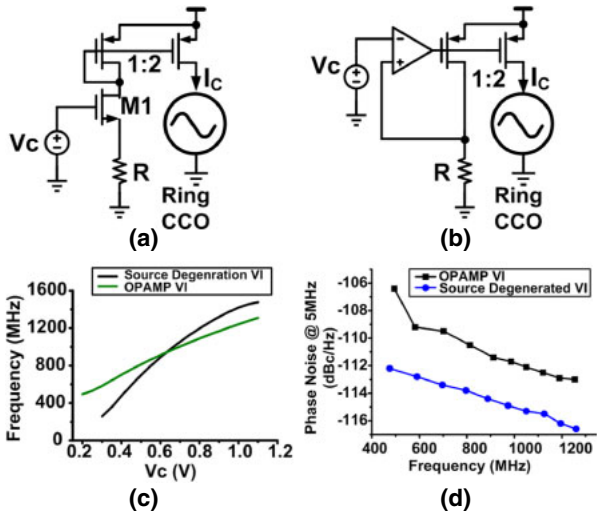


Fig. 13. (Color online) Schematics for simulation comparison of the (a) source degeneration *V–I* converter and (b) the OPAMP-based *V–I* converter, and the simulation result of (c) the tuning curve and (d) phase noise performance.

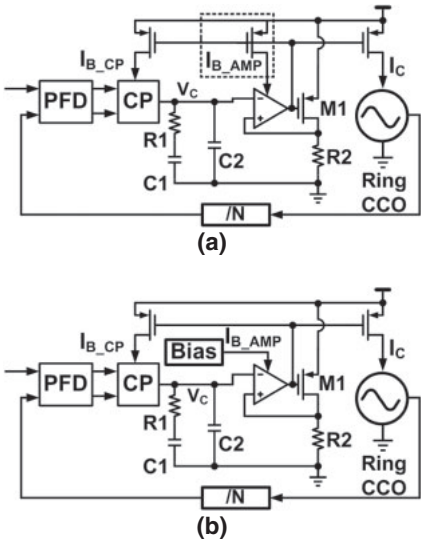


Fig. 14. Solutions to generate the bias current for OPAMP (a) with the *V–I* converter itself and (b) with an additional bias generation circuit.

3.2 Stability comparison

We analyze the stability of SBPLLs based on the OPAMP based *V–I* converter and source degeneration *V–I* converter, respectively. The OPAMP-based *V–I* converter has two poles, ω_1 and ω_2, as shown in Fig. 11(b). If the SBPLL adopts the *V–I* converter, the two poles must be much higher than the loop bandwidth to maintain the stability of the PLL. Therefore, more power consumption is needed.

The OPAMP in the *V–I* converter requires a bias circuit. There are two possible solutions to generate the bias circuit. The first solution is to bias the OPAMP by the *V–I* converter itself,[24] as shown in Fig. 14(a) and the second solution is to use a bias current generation circuit, as shown in Fig. 14(b). In the first solution, if the SBPLL generates a low-frequency clock, the bias current of the OPAMP in the *V–I* converter becomes lower and may cause a stability problem owing to the decrease of the two poles in the *V–I* converter. The second solution can avoid the problem in the first one, but the additional bias generation circuit occupies more area and the bias current for the OPAMP should also be set high enough to make the PLL stable regardless of the PVT variation. Thus such a solution is also not efficient in terms of power and area.

In the source degeneration *V–I* converter, there is no high impendence node and thus there is no pole that can degrade the stability of the SBPLL. In addition, no bias circuit is needed for such a *V–I* converter. Therefore, the SBPLL implemented with such a *V–I* converter is easier to stabilize and more PVT variation tolerable with lower power consumption, compared with the SBPLL that adopts the OPAMP based one.

In summary, as the noise, power and stability comparisons show, it is an effective way to replace the OPAMP based *V–I* converter with the proposed source degeneration *V–I* converter to make the SBPLL more power and area efficient without the penalty of noise, stability and PVT tolerance.

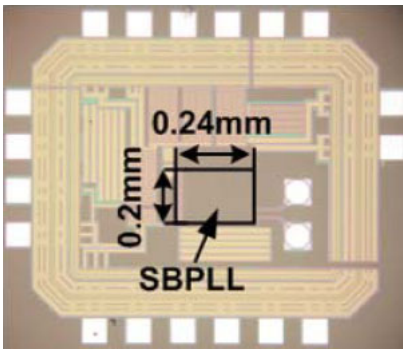


Fig. 15. (Color online) Chip micrograph.

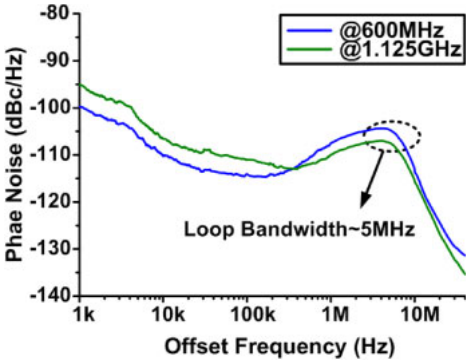


Fig. 16. (Color online) Phase noise at 1.125 GHz and 600 MHz, respectively.

4. Implementation and measurement results

The chip micrograph is shown in Fig. 15. It is implemented with the 0.18 µm process and occupies active area of only 0.048 mm^2 with 1.6 V supply voltage. Measurement shows that the SBPLL can generate a clock with the frequency range from 300 MHz to 1.125 GHz. Figure 16 shows the measured phase noise of 10 MHz offset frequency is −113 and −115 dBc/Hz at clock frequency of 600 MHz and 1.125 GHz, respectively. The loop bandwidth is around 5 MHz at the two frequency points. Figure 17 shows the reference spur level is −60 dB at 1.125 GHz clock frequency. The rms jitter integrated from 1 kHz to 40 MHz over all

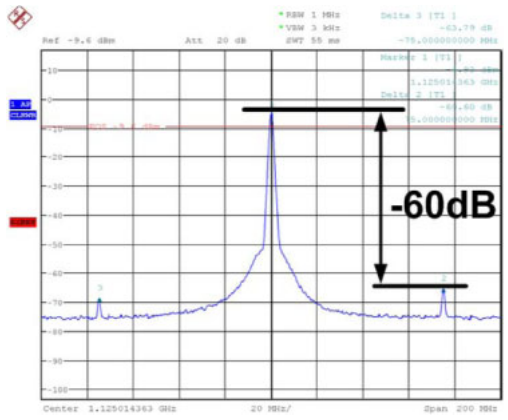


Fig. 17. (Color online) Frequency spectrum at 1.125 GHz.

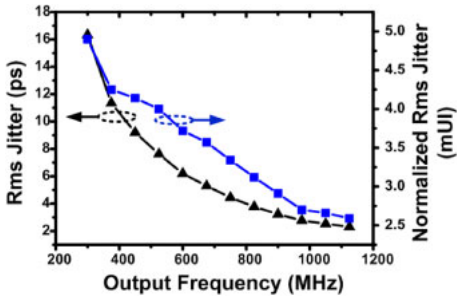


Fig. 18. (Color online) Integrated rms jitter over the entire covered frequency range.

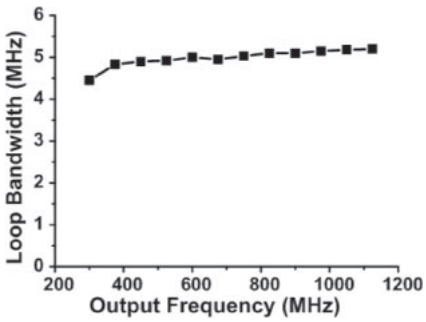


Fig. 19. Loop bandwidth over the entire frequency range.

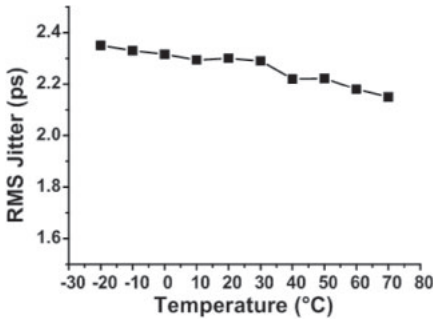


Fig. 20. Rms jitter performance at carrier frequency 1.125 GHz over temperature range from −20 to 70 °C.

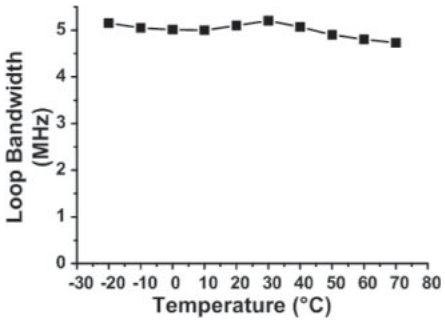


Fig. 21. Loop bandwidth at carrier frequency of 1.125 GHz over temperature range from −20 to 70 °C.

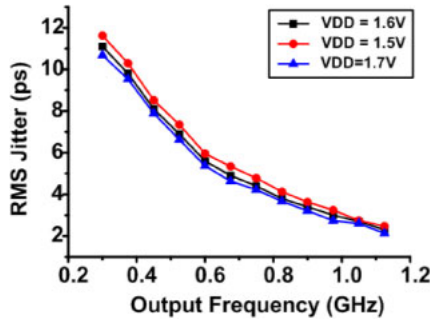


Fig. 22. (Color online) RMS jitter performance at different supply voltages.

covered frequency range is presented in Fig. 18. The worst rms jitter is 4.9 mUI at 300 MHz, which indicates a relatively low jitter performance. The worse jitter performance at a lower clock frequency is mainly due to the smaller swing of CCO output at lower output frequency.

Figure 19 presents the loop bandwidth versus output frequency. It indicates that the loop bandwidth f_{BW} is around 5 MHz regardless of the output frequency. The maximum variation of the f_{BW} is only about 750 kHz or 15% over all covered frequency range. The variation of f_{BW} is mainly caused by the nonlinearity of the *V–I* converter, the gain of CCO and the channel length modulation effect of MOS in the current mirrors of the CP.

Figures 20 and 21 show the rms jitter and loop bandwidth over a temperature range from −20 to 70 °C at 1.125 GHz output. It indicates the rms jitter variation is 0.2 ps and the f_{BW} variation is 350 kHz over a wide temperature range. Figure 22 shows the rms jitter performance at supply voltage of 1.5, 1.6, and 1.7 V, respectively. The rms jitter variation is less than 10% with a supply range from 1.5 to 1.7 V. In summary the SBPLL shows good tolerance of environment variation.

The performance summary of the SBPLL is listed in Table I, in which the figure of merit (FOM) is calculated by Eq. (3).[31]

$$\mathrm{FOM} = 10\log\left[\left(\frac{\sigma}{1\,\mathrm{s}}\right)^2 \times \left(\frac{\mathrm{Power}}{1\,\mathrm{mW}}\right)\right] \tag{7}$$

where the σ is the rms jitter of the PLL. Compared with the SBPLL,[24] the measurement results show that the proposed SBPLL has lower jitter and better FOM, which shows better noise performance and lower power of the proposed source degeneration *V–I* converter than the OPAMP-based one.[24] Although the SBPLL[24] shows the smallest area and lowest power to date, it is mainly due to the advanced process. If the proposed SBPLL is implemented in an advanced nanometer CMOS process, power and area can be further reduced.

Table I. Performance summary and comparison.

	This work	Ref. 24	Ref. 23	Ref. 9	Ref. 32	Ref. 10
Output frequency	0.3–1.125 GHz	1.5 GHz	240 MHz	3.1 GHz	2 GHz	1.21 GHz
Phase noise	−115 dBc/Hz@10 MHz	NA	−102 dBc/Hz@1 MHz	NA	−105 dBc/Hz@1 MHz	−119.6 dBc@1 MHz
RMS jitter	2.3 ps	5.8 ps	NA	1.01 ps	2.77 ps	0.57 ps
Reference spur	−60 dB	NA	−60 dB	NA	−50 dB	−55 dB
Power	5.6 mW	1.2 mW	8.46 mW	27.5 mW	32 mW	51.6 mW
Supply voltage	1.6 V	1 V	1.8 V	1.2 V	1.2 V	1.2 V
FOM	−225.3 dB	−223.9 dB	NA	−225.5 dB	−216 dB	−227.7 dB
Area	0.048 mm^2	0.02 mm^2	0.078 mm^2	0.32 mm^2	0.13 mm^2	0.12 mm^2
Temperature	−20 to 70 °C	NA	NA	NA	NA	NA
Technology	0.18 μm	90 nm	0.18 μm	65 nm	65 nm	65 nm

Compared with the other prior works shown in Table I, the proposed SBPLL shows lower power and small area with comparable FOM.

5. Conclusions

A compact 0.3-to-1.125 GHz SBPLL is proposed and implemented in inexpensive 0.18 μm CMOS process. The proposed triple-well NMOS source degeneration *V–I* converter is adopted in the SBPLL to save power and area. A simple start-up circuit is proposed to achieve robust start-up operation while occupies negligible area. The measured loop bandwidth can be kept at around 5 MHz with the variation of only 15%. The rms jitter integrated from 1 kHz to 40 MHz at a carrier frequency of 1.125 GHz is 2.3 ps and normalized rms jitter over the entire frequency range is less than 4.9 mUI. The variation in the rms jitter and loop bandwidth at 1.125 GHz is 0.2 ps and 350 kHz in the temperature range from −20 to 70 °C, respectively. The rms jitter performance variation of all the covered frequency points is less than 10% in the supply range from 1.5 to 1.7 V. The SBPLL shows good robustness to environmental variation. The maximum power is 5.6 mW at 1.125 GHz with 1.6 V supply and the FOM of −225.3 dB. Measurement shows that the proposed SBPLL has smaller area and lower power with comparable FOM than those of the prior works.

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