The Flipped Voltage Follower: A Useful Cell for Low-Voltage Low-Power Circuit Design

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***Abstract*—In this paper, a basic cell for low-power and/or low-voltage operation is identified. It is evidenced how different versions of this cell, coined as "flipped voltage follower (FVF)" have been used in the past for many applications. A detailed classification of basic topologies derived from the FVF is given. In addition, a comprehensive list of recently proposed low-voltage/low-power CMOS circuits based on the FVF is given. Although the paper has a tutorial taste, some new applications of the FVF are also presented and supported by a set of simulated and experimental results. Finally, a design example showing the application of the FVF to build systems based on translinear loops is described which shows the potential of this cell for the design of high-performance low-power/low-voltage analog and mixed-signal circuits.**

***Index Terms*—Analog circuits, analog integrated circuits, continuous time filters, differential amplifiers, low-power design, low-voltage design.**

I. Introduction

DOWNSCALING of CMOS processes has forced analog circuits to operate with continuously decreasing supply voltages. This trend has been mainly driven by the need to reduce power consumption of the digital circuitry in mixed-mode very large-scale integration (VLSI) systems and to prevent oxide breakdown with decreasing gate-oxide thickness. In addition, low power consumption and low supply voltages are requirements of the portable electronic equipment market. Several techniques have been proposed to reduce supply voltage requirements in analog and mixed-signals circuits, among them: folding, triode-mode and subthreshold operation of MOS transistors, floating-gate techniques, and current-mode processing [1]–[5].

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In this paper, a cell called "flipped voltage follower" (FVF) is proposed. It is shown that different versions of this cell have been used in the past for low-voltage and low-power operation, and proper references will be given in this paper when convenient (the authors have made their best to compile a good list of references, although they cannot claim it to be exhaustive). The FVF cell and its properties are presented in Section II. Section III deals with basic circuits derived from the FVF. In Section IV, these basic circuits are used to build low-voltage, low-power analog cells like current mirrors, operational transconductance amplifiers (OTAs), operational amplifiers, and buffers. Although this section mainly has a tutorial orientation, some new results of FVF applications are also reported, such as new current conveyors (Section IV-A-I), and a new four-quadrant transconductance multiplier with a high current efficiency (Section IV-D-II). In Section V, a complete example of how to apply the FVF cell to implement low-voltage, low-power translinear loops is proposed and experimentally verified. These new circuits are described in more detail providing simulation and/or experimental results. Finally, in Section VI some conclusions are drawn.

II. Flipped Voltage Follower

Let us consider the common drain amplifier in Fig. 1(a), frequently used as a voltage buffer. If body effect is neglected the circuit follows the input voltage with a dc level shift, i.e., $V_o = V_i + V_{\mathrm{SGM1}}$, where V_{SGM1} is the source-to-gate voltage of transistor M_1. Concerning large-signal behavior, this circuit is able to sink a large current from the load, but its sourcing capability is limited by the biasing current source I_b. A drawback of this circuit is that current through transistor M_1 depends on the output current, so that V_{SGM1} is not constant and, hence, for resistive loads, the voltage gain is less than unity. A similar problem occurs with capacitive loads at high frequencies.

The circuit in Fig. 1(b) also operates as a source follower where the current through transistor M_1 is held constant, independent on the output current. It could be described as a voltage follower with shunt feedback. Neglecting body effect and the short-channel effect, V_{SGM1} is held constant, and voltage gain is unity. Unlike the conventional voltage follower, the circuit in Fig. 1(b) is able to source a large amount of current, but its sinking capability is limited by the biasing current source I_b. The large sourcing capability is due to the low impedance at the output node, which is (see derivation below) approximately

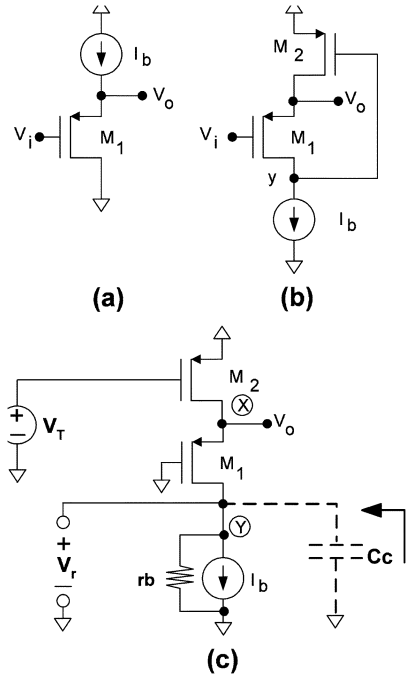

Fig. 1. (a) Common-drain amplifier (voltage follower). (b) FVF. (c) Open-loop gain analysis of circuit of (b).

$r_o = 1/(g_{m1}g_{m2}r_{o1})$, where g_{mi} and r_{oi} are the transconductance and output resistance of transistor M_i, respectively. This value is in the order of 20–100 Ω.

Note that M_2 provides shunt feedback and that M_1 and M_2 form a two pole negative feedback loop. Fig. 1(c) shows the same circuit with the feedback loop open at the gate of M_2 and including a test voltage source V_T. This circuit has an open-loop gain $A_{\rm OL} = V_r/V_T = -g_{m2}R_{\rm OLY}$ (where the open-loop resistance at node Y is given by $R_{\rm OLY} \approx r_b||g_{m1}r_{o1}r_{o2}$), a dominant pole at node Y, $\omega_{pY} = 1/C_YR_{\rm OLY}$, and a high-frequency pole at node X, $\omega_{pX} = 1/R_{\rm OLX}C_X$ (where the open-loop resistance at node X is given by $R_{\rm OLX} \approx (1+r_b/r_{o1})/g_{m1}||r_{o2}$). C_X and C_Y are the parasitic capacitances at nodes X and Y respectively (C_X also includes the load capacitor, if any). The gain bandwidth product is given by ${\rm GB} = g_{m2}/C_Y$. The closed-loop resistance at node X is given by

$$R_{\rm CLX} = \frac{R_{\rm OLX}}{1+|A_{\rm OL}|} \approx \frac{\frac{1}{g_{m_1}}\left(1+\frac{r_b}{r_{o1}}\right)||r_{o2}}{g_{m_2}(r_b||g_{m_1}r_{o1}r_{o2})}. \quad (1)$$

If the source I_b is a simple current mirror ($r_b \approx r_{o1}$) $R_{\rm CLX}$ tends to $2/(g_{m1}g_{m2}r_{o1})$. In the case that I_b is a cascode current mirror ($r_b \approx g_{m1}r_{o1}r_{o2}$), or for very large r_b, $R_{\rm CLX}$ is approximately given by $1/(g_{m1}g_{m2}r_{o1})$. In any case, $R_{\rm CLX}$ is a very low resistance.

In order to ensure stability the condition $\omega_{pX} > 2\,{\rm GB}$ must be satisfied. For $r_b \approx r_{o1}$, this condition leads to $C_X/C_Y < g_{m1}/(4g_{m2})$, which is easily achieved by proper sizing of the relative W/L ratio of transistors M_1 and M_2, except for large capacitor loads. For large capacitor loads and for large values of r_b where the stability condition reduces to $C_X/C_Y < 1/(g_{m2}r_{o2})$, the addition of a compensation capacitor [C_c in Fig. 1(c)] could be necessary. In the following, the circuit in Fig. 1(b) will be coined as FVF.

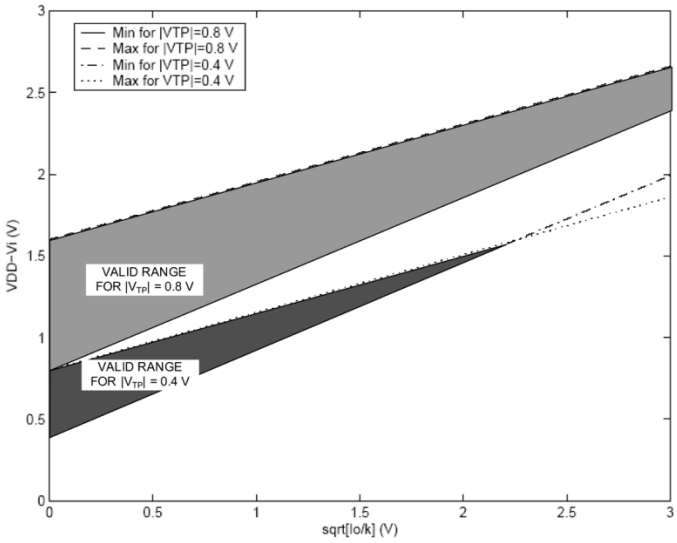

Fig. 2. Allowable input range for two different transistor threshold voltages.

Note that the FVF can be operated at a very low voltage supply, and that it is the operating condition we are interested in. The FVF can also be used with a large supply voltage, but in this case, biasing transistor M_1 in saturation can become difficult if the input voltage V_i is low. If we take a look to the circuit in Fig. 1(b), the following relation can be written: $V_{\rm SGM2} = V_{\rm SDM2} + V_{\rm SDM1}$. Let us assume quiescent conditions with no output current. Assuming that transistor M_1 is in saturation, and neglecting second-order effects, the condition of saturation for transistor M_2 is given by

$$V_{\rm SDM2} = V_{\rm DD} - \left(V_i + |V_{TP}|_{M1} + \sqrt{\frac{2I_o}{k_P\left(\frac{W}{L}\right)_{M1}}}\right) > \sqrt{\frac{2I_o}{k_P\left(\frac{W}{L}\right)_{M2}}} \quad (2)$$

where I_o is the drain current (I_b in this case), $k_P = \mu_P C_{\rm ox}$, and V_{TP} is the transistor threshold voltage. In the same way, assuming that transistor M_2 is biased in saturation, the condition of saturation for transistor M_1 is given by the following relation:

$$V_{\rm SGM1} - V_{\rm SDM1} = V_{\rm DD} - \left(|V_{TP}|_{M2} + \sqrt{\frac{2I_o}{k_P\left(\frac{W}{L}\right)_{M2}}}\right) - V_i < |V_{TP}|_{M1}. \quad (3)$$

Although the linear region of operation is still valid for transistors M_1 and/or M_2 in certain applications, we will limit ourselves to the saturation region in this analysis. Therefore, the valid region of operation for the input signal is limited by

$$|V_{TP}|_{M1} + \sqrt{\frac{2I_o}{k_P}}\left(\sqrt{\frac{1}{\left(\frac{W}{L}\right)_{M1}}} + \sqrt{\frac{1}{\left(\frac{W}{L}\right)_{M2}}}\right) < V_{\rm DD} - V_i < |V_{TP}|_{M1} + |V_{TP}|_{M2} + \sqrt{\frac{2I_o}{k_P}}\sqrt{\frac{1}{\left(\frac{W}{L}\right)_{M2}}}. \quad (4)$$

Fig. 2 depicts the valid range of values for $V_{\rm DD} - V_i$ versus the square root of (I_o/k_P) for $(W/L)_{M1} = 64$, $(W/L)_{M2} = 16$, and two values of $|V_{TP}|$: 0.8 V and 0.4 V. It can be observed that the valid input signal range decreases with the transistor

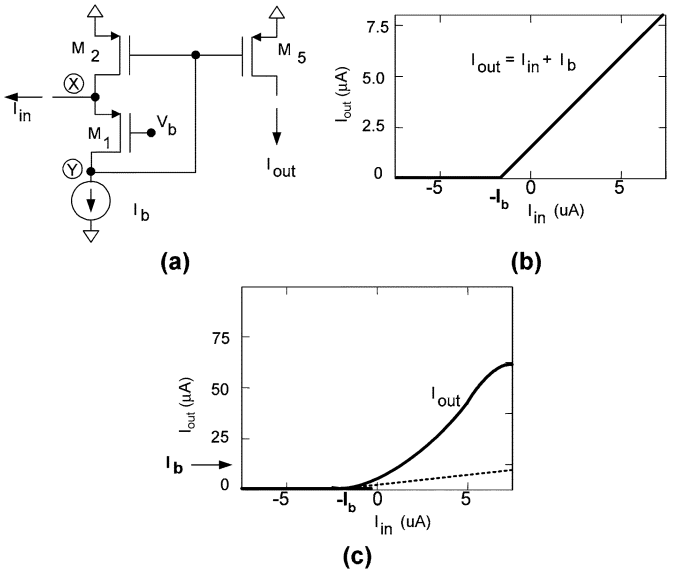

Fig. 3. FVFCS. (a) Basic implementation. (b) DC response. (c) DC response with M_2 biased near the linear region.

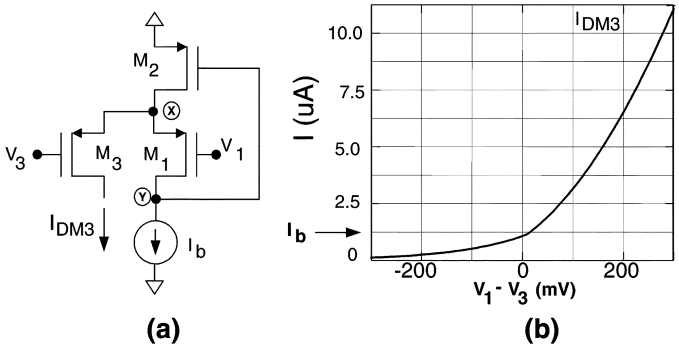

Fig. 4. (a) DFVF amplifier . (b) DC transfer characteristic.

threshold voltage, which limits the applications of the FVF in deep submicron technologies.

A possible solution to overcome these problems is to include a dc level shifter between node Y and the gate of transistor M_2, like in [6], at the cost of increased power consumption, and reduced bandwidth. This solution can be applied to most of the circuits presented in this paper and we will not insist on it.

III. Basic FVF Structures

A. FVF Current Sensor (FVFCS)

The FVF can be also considered to be a current sensing cell, and when used in this way it will be called a "FVF current sensor (FVFCS)." Let us consider node X in Fig. 3(a) as the input current sensing node and that all transistors are properly biased to work in the saturation region. Due to the shunt feedback provided by transistor M_2, the impedance at node X is very low and, this way, the amount of current that flows through this node does not modify the value of its voltage. Note that node X can source large current variations at the input and the FVF translates them into compressed voltage variations at output node Y. This voltage can be used to generate replicas of the input current as shown in Fig. 3(a) by means of transistor M_5. Fig. 3(b) shows the dc response of the circuit in Fig. 3(a). The output and the input currents are related through the expression $I_{\rm out} = I_{\rm in} + I_b$. The current I_b can be easily removed from the output node using current mirroring techniques if this is needed for a specific application.

A special condition of the FVFCS occurs when transistor M_2 is biased near the linear region and M_5 is maintained in the saturation region. In this case, the output current can increase several times compared to the input current [Fig. 3(c)]. This mode of operation can be used to achieve Class-AB behavior as was demonstrated in [7], but it is not suitable for very low-voltage operation as the voltage of node Y can experience large variations from its quiescent value, thus affecting the current source I_b.

Apart from this particular operating condition, the FVFCS can be operated with very low supply voltage. The minimum supply voltage is $V_{\rm DD}^{\rm MIN} = |V_{TP}| + 2V_{\rm DSsat}$, where V_{TP} is the transistor threshold voltage and $V_{\rm DSsat}$ is the minimum drain-to-source voltage required to maintain a transistor in saturation. $V_{\rm DD}^{\rm MIN}$ can be as low as 950 mV for a 0.35-μm CMOS technology with $|V_{TP}| = 650$ mV. Obviously, with $V_{\rm DD} = V_{\rm DD}^{\rm MIN}$ there is no room for input current variation; for a given input current $I_{\rm in}$, ranging from 0 to $I_{\rm in}^{\rm MAX}$, the minimum supply current is $|V_{TP}| + 2V_{\rm DSsat} + \sqrt{2\left(I_{\rm in}^{\rm MAX} + I_b\right)/k_P(W/L)_{M2}}$, where, once again, $k_P = \mu_P C_{\rm ox}$.

B. FVF Differential Structure (DFVF)

Several differential Class-AB circuits can be derived using the current sensing property of the previous scheme. The first differential structure based on the FVF cell can be built by adding an extra transistor M_3 connected to node X, as it is shown in Fig. 4(a) [1]. It will be called the "FVF differential structure (DFVF)." As indicated in the previous section, the impedance at node X is very low and its voltage remains approximately constant for large currents through transistor M_3. If we consider quiescent conditions when $V_1 = V_3$, and assuming the same transistor sizes for M_1 and M_3, the condition $I_{DM1} = I_{DM3} = I_b$ is satisfied. A differential voltage $V_1 - V_3$ generates current variations in M_3 that follow the MOS square law. This is a very interesting property of the DFVF as the maximum output current can be much larger than the quiescent current I_b. Fig. 4(b) shows the dc transfer characteristic for I_{DM3} versus $V_1 - V_3$. The typical Class-AB behavior can be observed.

Another characteristic of the DFVF is that the output is available as both a current (I_{DM3}, or the current through transistor M_2 replicated by means of a current mirror), and a voltage (node Y). This feature can be advantageously employed to simplify the circuit implementations reducing both noise and number of poles and zeros. Finally, the DFVF can also be operated with very low supply voltage. The minimum supply voltage is, as in the case of the FVFCS, $V_{\rm DD}^{\rm MIN} = |V_{TP}| + 2V_{\rm DSsat}$. Once again, with a supply of $V_{\rm DD}^{\rm MIN}$ there would be no room for variation of the input signals V_1 and V_3. It is easy to obtain an expression relating the expected variation of V_1 and V_3 with the minimum supply voltage which maintains the DFVF cell properly biased.

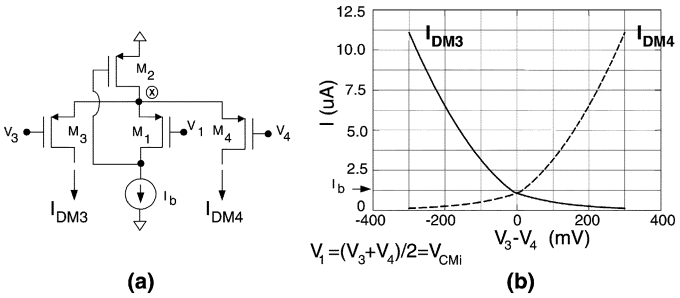

Fig. 5. (a) FVFDP. (b) DC transfer characteristic.

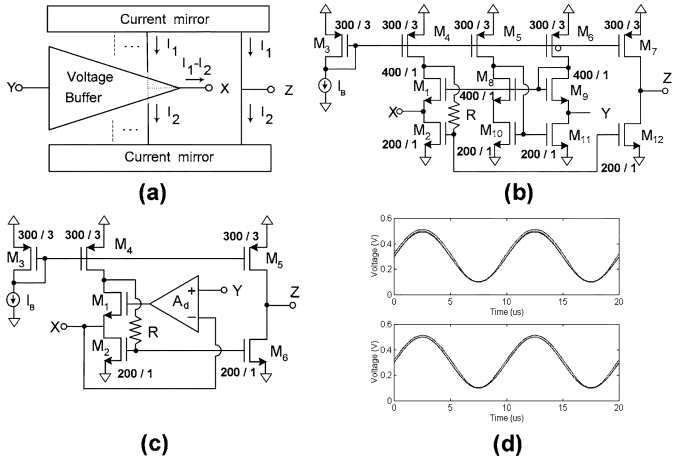

Fig. 6. (a) Simplified diagram of a CCII. (b) Implementation of a CCII using the FVF. (c) Improved CCII. (d) Transient response: Upper figure for the circuit in (b), and lower figure for the circuit in (c).

C. FVF Pseudo-Differential Pair (FVFDP)

A pseudo-differential pair can be easily constructed from the DFVF by adding an extra transistor (M_4) connected to node X, as shown in Fig. 5(a). This structure will be called the "FVF pseudo-differential pair (FVFDP)." Fig. 5(b) shows the dc output currents I_{DM3} and I_{DM4} versus the differential input voltage $V_3 - V_4$, in a typical case. The pseudo-differential pair also exemplifies the characteristic behavior of a Class-AB circuit, where the quiescent output current I_b can be much lower than the peak value. In this case, we have considered that, under quiescent conditions, $V_1 = V_3 = V_4$. That is, assuming perfect matching between transistors M_1, M_3 and M_4, the voltage at the gate of M_1 corresponds to the common mode of M_3 and M_4: $V_1 = (V_3 + V_4)/2 = V_{CMi}$. If the common-mode value V_{CMi} of input voltages V_3 and V_4 is not equal to V_1 the dc output characteristic has the same shape, but a dc level shift is applied to the curves of transistor currents in opposite directions of the horizontal axis.

The main difference between the DFVF and the FVFDP is that the latter has a true differential output. The output current I_{DM3} of the DFVF can be large if $V_1 - V_3$ is positive and zero if $V_1 - V_3$ is negative, while in the FVFDP we can have positive or negative large differential output currents $(I_{\text{out}} = I_{DM3} - I_{DM4})$ depending on the value of the input differential voltage $(V_{\text{in}} = V_3 - V_4)$. This pseudo-differential pair can be also operated with a minimum supply voltage of $V_{\text{DD}}^{\text{MIN}} = |V_{TP}| + 2|V_{\text{DSsat}}|$, as in the cases of the FVFCS and DFVF.

IV. Low-Power and/or Low-Voltage Analog Cells

Using the basic FVF structures presented in Sections II and III (FVF, FVFCS, DFVF, and FVFDP), several analog building blocks can be derived. Although most of them have been proposed in the past, new ones are presented in this paper. All of them have a common property: they are suitable for operation under low-power and/or low voltage supply restrictions and take advantage of the FVF to achieve the imposed specifications.

A. Applications of the FVF

The basic application of the FVF is as an analog buffer with dc level shifting. Level shifting is a well-known technique to reduce the voltage specifications of circuits [4], [5], [10], [11].

1) Current Conveyors: Current Conveyors are basic building blocks in many current-mode circuits. Since their introduction in 1968 [12], the interest generated by them has steadily increased, being nowadays recognized as extremely versatile analog building blocks, and being also commercially available. They are three-port structures (being their ports traditionally named X, Y and Z) described by the following matrix equation:

$$\begin{bmatrix} I_Y \\ V_X \\ I_Z \end{bmatrix} = \begin{bmatrix} 0 & M & 0 \\ 1 & 0 & 0 \\ 0 & N & 0 \end{bmatrix} \begin{bmatrix} V_Y \\ I_X \\ V_Z \end{bmatrix} \tag{5}$$

I_X, I_Y, I_Z, and V_X, V_Y, V_Z being currents and voltages at nodes X, Y and Z, respectively. Depending on the value of constant M, several types of current conveyors are obtained. We will focus our attention in this paper on second-generation current conveyor (CCII) structures where $M = 0$, being the most widely employed.

Fig. 6(a) shows the basic structure of most CCII circuits. It is based on a voltage buffer having input node Y and output node X, and a current mirror that copies the buffer output current and delivers it at the high impedance node Z. Performance of the CCII is strongly affected by the characteristics of this buffer. In particular, it should have:

- very high input impedance at node Y, very low output impedance at node X, and high output impedance at node Z;
- accurate voltage copy from node Y to node X and accurate copy of the output current at node X to the Z terminal;
- highest speed for a given bias current;
- low supply voltage requirement.

The last two requirements are often related to the simplicity of the buffer in terms of transistor stacking and number of internal nodes. Two new CCII cells which fulfil the above requirements are proposed with the structure of Fig. 6(a), using a FVF as the voltage buffer.

Fig. 6(b) shows the first possible implementation. A simple dc level shifter formed by the diode-connected transistor M_9 biased by two identical current sources is employed. The circuit becomes very simple, having only two internal nodes (excluding biasing current mirrors). However, the input impedance of terminal Y is finite and in the order of $r_{o11} \| r_{o6}$. The output

TABLE I
MAIN PARAMETERS OF THE PROPOSED CCII CIRCUITS

CCII	Fig. 6b	Fig. 6c
Input impedance, node Y	$r_{o6} \parallel r_{o11}$	∞
Output impedance, node X	$\frac{1}{g_{m1}g_{m2}(r_{o4} \parallel r_{o1})}$	$\frac{1}{A_d g_{m1}g_{m2}(r_{o4} \parallel r_{o1})}$
Output impedance, node Z	$r_{o7} \parallel r_{o12}$	$r_{o5} \parallel r_{o6}$
Voltage gain V_X / V_Y	1	1
Current gain I_Z / I_Y	1	1

impedance at terminal X is very low thanks to the FVF structure. The small-signal voltage gain from terminal Y to terminal X is

$$A_v \approx \frac{1}{1+r_s\left(\frac{1}{r_{o6}}+\frac{1}{r_{o11}}-\frac{g_{m_{11}}}{g_{m_{10}}r_{o10}}\right)} \times \frac{1}{1+\frac{1}{g_{m_1}r_{o1}}\left[1+\frac{1}{g_{m_2}(r_{o2}||R_L)}\left(1+\frac{r_{o1}}{r_{o4}}\right)\right]} \approx 1 \quad (6)$$

where R_L represents the load resistance at node X, and r_s the impedance of the input voltage source located at node Y. In (6), $r_s > 1/g_m$ has been assumed. It can be noted that, even for very small loads the superior driving features of the FVF lead to a voltage gain of approximately 1. Note that resistor R in the FVF cell has been introduced to improve the signal bandwidth [13].

A modified structure is shown in Fig. 6(c). The difference between input and output FVF dc levels is now solved by driving the FVF with an amplifier whose inputs are terminals X and Y. This way, the diode-connected dc level shifter is avoided, leading to a very high input impedance at node Y. At the same time, the amplifier feedback further reduces the output impedance of terminal X and also makes the voltage gain come closer to the ideal (unity) value. Biasing of the cell also becomes simpler thanks to the avoidance of the dc level shifter. Nevertheless, additional internal nodes are introduced by the amplifier. The amplifier A_d can be implemented with a simple differential pair. Table I summarizes the main characteristics of both current conveyors.

The circuits of Fig. 6(b) and (c) were simulated in a Cadence environment using BSIMSv3 models for a 0.5-pm CMOS technology with nMOS and pMOS threshold voltages of approximately 0.8 V. Bias voltage was 1.5 V, and the bias current I_B was 100 μA. First, its time response was evaluated by configuring the CCII cells as unity-gain voltage amplifiers. In order to do so, ports X and Z were loaded with 25 kΩ resistances. The input voltage, a 100-kHz, 400-mV, sinusoidal signal was applied to the Y port, and Fig. 6(d) shows the results obtained. The upper graph corresponds to the CCII of Fig. 6(b), whereas the lower one was obtained with the CCII of Fig. 6(c). In these figures the voltages at ports X and Y are almost identical. Only the output at port Z is slightly different in both cases due to the channel-length modulation effect in the MOS transistors of the biasing current mirrors. The ac small-signal frequency response for both circuits was subsequently obtained, using the same load resistors. No compensation was required in internal nodes. The simple structure of Fig. 6(b) has a -3 dB bandwidth of 100 MHz, larger that that of Fig. 6(c), as expected. Table II compares some simulation results for these cells and another low-voltage current conveyor recently reported in the literature [14]. The advantages in terms of supply voltage, bandwidth and power consumption are clearly evidenced.

TABLE II
PERFORMANCES OF THE PROPOSED CCII CIRCUITS

CCII	Fig. 6b	Fig. 6c	Rajput-Jamuar [14]
Supply Voltage (V)	1.5	1.5	$\pm$ 1
Bandwidth (MHz)	100	65	60
Power consumption (mW)	0.75	0.6	3
THD (%)	1.3	1.1	Not available
Number of transistors	12	14	57

2) Multipliers and Mixers: The FVF has been used in the past for the implementation of mixers and multipliers. In [15], the FVF cell was used to build a 1-GHz CMOS up-conversion mixer that takes advantage of the low output impedance of the FVF to create a high-frequency buffer. There are also several OTA and transconductance multiplier structures reported in the past which can be modified to reduce the voltage specifications and, sometimes, to improve the power consumption and performances, by using the FVF. See, for instance, [16], where the low impedance nodes required by the classical four-quadrant four-transistor multiplier were implemented in a simple way by using FVF cells.

B. Applications of the FVFCS

The FVFCS has been used in the past for different applications [8], [17]–[21]. For example, in [17] the FVFCS was used as a part of a power amplifier.

1) Current Mirrors: The first and simplest use of the FVFCS is as the input stage of a low-voltage current mirror [8], [18]–[22]. High-performance current-mirrors with very low input and output voltage requirements are needed as building blocks of mixed-mode VLSI systems that operate from a single supply of 1.5 V or below. High accuracy requires very high output resistance and low input resistance. Low voltage operation requires low input and output voltages as well as low supply requirements for the control circuitry used to improve the mirror's input and output resistance.

Taking all these considerations into account the circuit in Fig. 7(a), which is a basic implementation of the FVFCS, has the lowest input resistance as well as the lowest input voltage requirements reported to date. The input voltage required for such current mirror is in the order of V_{DSsat}, which can be as small as 0.1 V, which is much smaller than the V_{GS} drop required for the conventional low-voltage current mirror. Also, as it was specified in Section II, the input impedance is very low, $r_o = 1/(g_{m1}g_{m2}r_{o1})$, which is in the order of 20–100 Ω. Moreover, in Section III the minimum voltage supply for the FVFCS

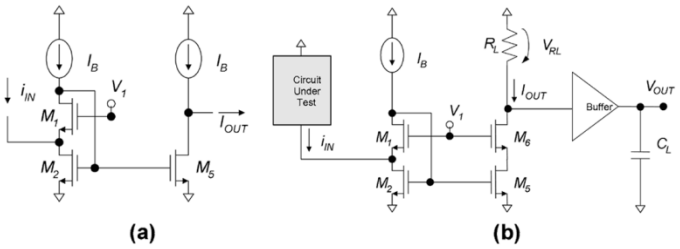

Fig. 7. (a) Low-voltage current mirrors using the FVFCS. (b) Low-voltage $I_{\rm DD}$ current sensor based on the FVFCS.

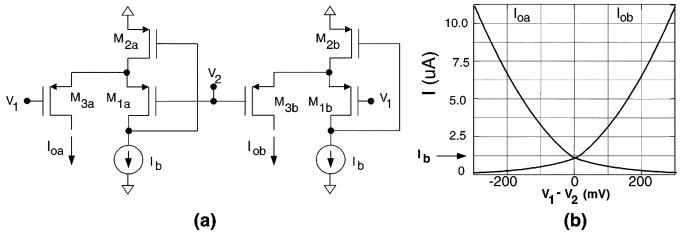

Fig. 8. (a) Core cell for the OTA in [33]. (b) DC transfer characteristic.

was expressed as $V_{\rm DD}^{\rm MIN} = |V_{TP}| + 2V_{\rm DSsat}$ and for this reason the mirror in Fig. 7(a) has low voltage supply requirements.

As mentioned before, a high-performance current mirror also requires very high output resistance and low-voltage requirements at the output stage. One simple approach to build the output stage is by means of a simple or cascode current source. If a large output resistance is required, two low-voltage high-performance current mirrors based on the FVFCS have been recently reported by the authors which are able to operate with low input and output voltage requirements [21], [22].

2) Other Applications of the FVFCS: In [23] a current sensor for $I_{\rm DD}$ test was proposed. A current sensor based on the FVFCS is appropriate for this purpose, since it has low supply voltage and low input voltage requirements, very low input impedance and the capability to sink large currents with an approximately constant input voltage close to one of the supply rails. The current sensor basic scheme is shown in Fig. 7(b). It consists of a FVFCS plus a cascode output stage M_6 and a resistor R_L that transforms a replica of the transient $i_{\rm IN}$ supply current into an observable voltage V_{RL}. A high-frequency buffer is also included to drive the voltage signal across R_L out of chip and to isolate it from the large output load capacitance C_L. The FVFCS is biased with the current source I_B which determines the effective bandwidth of the current sensor. An earlier implementation of this current sensor cell can be found in [24] where a level shifter was also included to enlarge the signal swing.

The FVFCS has been recently used as the input stage of a very low-voltage voltage-to-current conversion cell [25], where a resistor connected between the input signal $V_{\rm in}$ and the node X in Fig. 3(a) is used to generate a current $I_{\rm in} = (V_x - V_{\rm in})/R$. In this way, a current proportional to the input voltage plus a constant term is obtained. This idea can be extended ([26], [27]) to perform transconductance and transimpedance operations in the same way as proposed in [10]. The FVFCS has also been recently used to build a low-voltage switched-current (SC) cell [28].

Finally, different log-domain circuits have been proposed which take profit of the compression of the input current which takes place at the gate voltage of transistor M_2 in Fig. 3(a) [29], [30] (see also [31], [32] which use the same basic structure with bipolar transistors).

C. Applications of the DFVF

DFVFs are mainly employed to build low-power low-voltage Class-AB stages in a variety of applications. Some of them will be now reviewed.

1) Transconductance Operational Amplifiers: In [33], a low-power low-voltage fully differential OTA for SC applications was proposed. The core cell for this OTA is shown in Fig. 8(a). This cell uses two DFVFs in order to obtain a fully differential behavior. In Fig. 8(b) the dc transfer characteristic of the circuit proposed in [33] is shown. It can be seen that the quiescent current ($I_{oa} = I_{ob} = I_b$ when $V_1 = V_2$) is much smaller than the maximum achievable value providing a low-power Class-AB operation. Although for small signals, it has a linear differential output $I_{oa} - I_{ob}$, the large signal behavior is mainly nonlinear. This is not of concern if the circuit is used in SC applications where the slew performance benefits from the Class-AB behavior of the cell. Note that the circuit has a large common-mode rejection ratio (CMRR) as each DFVF, neglecting second-order effects, is only sensitive to the difference between the input signals. Based on this circuit, an OTA was designed to build a 12 bit, low-voltage, low-power, Sigma-Delta modulator that proved experimentally the good properties of the DFVF and the FVFCS to provide Class-AB behavior under the aforementioned restrictions [8], [34].

2) Output Stage: Several low-voltage ($V_{\rm DD} < 1.5$ V) Class-AB op-amp schemes have been recently reported [7], [11], [35], [36]. The DFVF structure can be used to build output stages for operational amplifiers as was shown by the authors in [37]. In Fig. 9(a), the bias current I_o in the DFVF structures formed by transistors $M_{1p} - M_{3p}$ and $M_{1n} - M_{3n}$ accurately determines the quiescent output current $I_{\rm out}^Q = I_{\rm moutn}^Q = I_{\rm moutp}^Q = 2\alpha I_o$ (superindex ^{Q} stands for quiescent value). Furthermore, the minimum current in the output transistors is given by $I_{\rm out}^{\rm MIN} = I_{\rm moutn}^{\rm MIN} = I_{\rm moutp}^{\rm MIN} = \alpha I_o$. Note that $I_{\rm out}^Q$ and $I_{\rm out}^{\rm MIN}$ do not depend on the value of the floating voltage sources $V_{\rm AB}$, which is selected to allow an accurate copy of currents I_{M3p} and I_{M3n} to transistors $M_{\rm outp}$ and $M_{\rm outn}$, respectively. An appropriate value for $V_{\rm AB}$ is $V_X^Q - V_Y^Q = V_{\rm DD} - V_{\rm GSM1n}^Q - V_{\rm SGM1p}^Q - 2V_{\rm DSsat} - \Delta V_X^{\rm MAX}$, where $\Delta V_X^{\rm MAX}$ is the maximum expected variation for the input node voltage V_X. If the input node V_X in Fig. 9(a) is the output of the first stage of an op-amp, negative feedback reduces $\Delta V_X^{\rm MAX}$ to only a few millivolts so that, for a 0.8-μm CMOS technology with 0.8-V of transistor threshold voltages, $V_{\rm DD} - V_{\rm AB}$ is in the order of 1.8 to 3 V depending on transistor sizes and biasing currents. According to this reasoning, this stage can be operated with less than 1 V supply voltage if $V_{\rm AB} = -0.8$ V. Note that this stage can also be operated with a high supply voltage if $V_{\rm AB}$ is positive. The dynamic biasing scheme in [38] [Fig. 9(b)] can be used to generate the floating voltage sources $V_{\rm AB}$ between nodes X–Y and W–Z. Diode connected transistors M_1 and M_2 determine the voltage

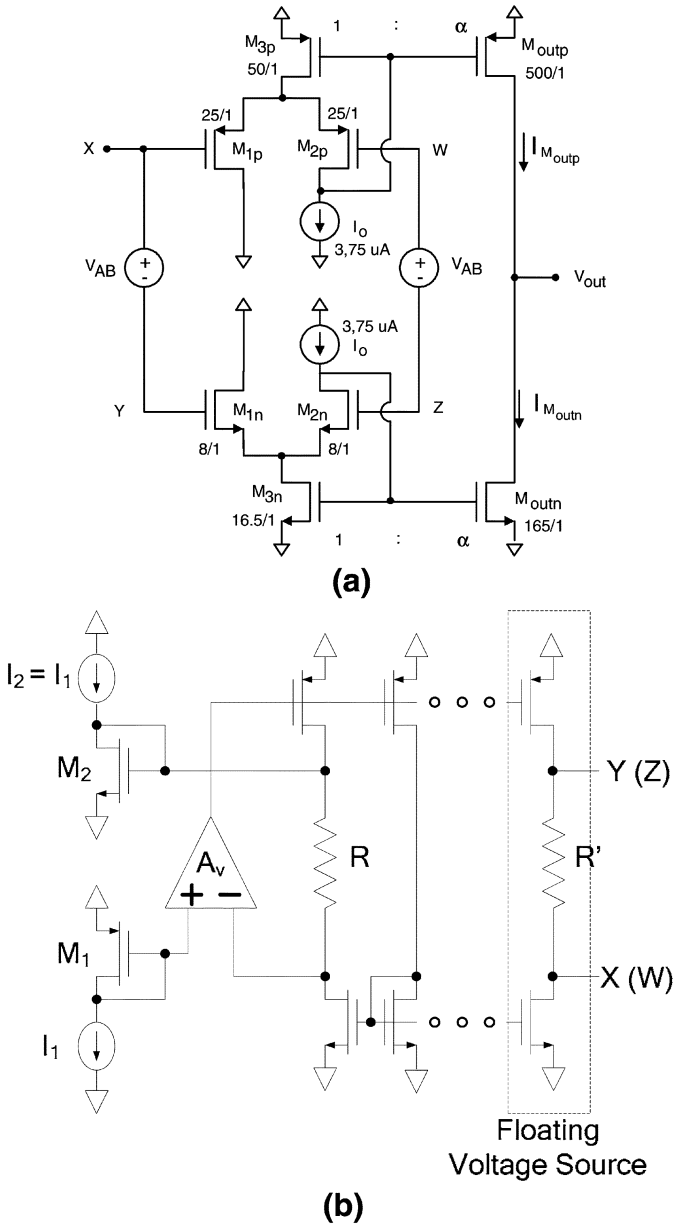

Fig. 9. (a) Class-AB output stage with DFVFs. (b) Biasing circuitry.

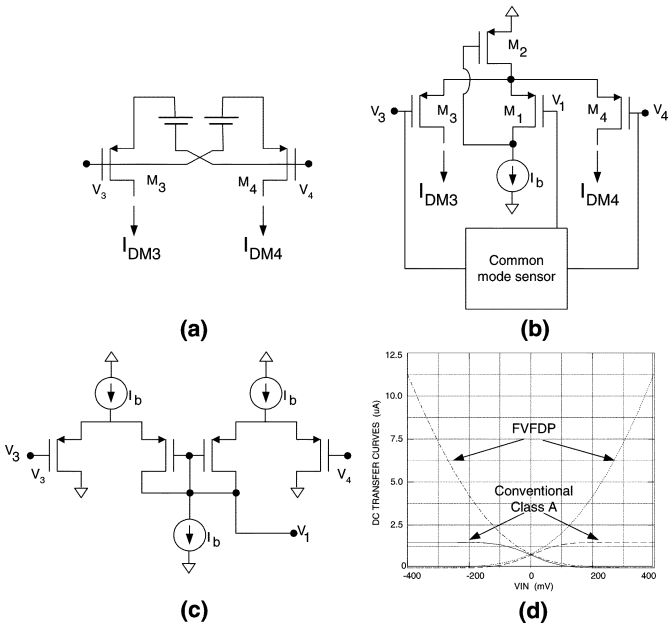

Fig. 10. Class-AB input differential stages. (a) Concept. (b) Low-voltage implementation using FVFDP. (c) Common mode sensing network. (d) Comparison of dc transconductance characteristics of FVFDP and conventional Class-A stage.

drop required to provide the required quiescent current to the transistors M_{outp} and M_{outn}, respectively. Floating voltage sources V_{AB} are built with matched floating resistors and current mirrors. Note that this biasing circuit provides the stage with a large power-supply rejection ratio.

As the currents through the output transistors never vanish, this stage can be shown to provide a high linearity with reduced quiescent power consumption. To this end, it was used as the output stage of a two-stage opamp [39]. A version of this stage was also used in [40] to build a low-power Class-AB analog buffer with low input capacitance.

D. Applications of the FVFDP

Owing to its differential characteristic, the main application of the FVFDP is as the input stage of operational amplifiers and operational transconductance amplifiers. The authors have found application for this cell in many circuits and some of them are reported here.

1) Class-AB Input Stages for OP-AMPs and OTAs for SC Applications: Some Class-AB input stages have been reported in literature [33], [41], [42]. Class-AB input stages are able to provide a large peak current with a low quiescent consumption, which is of interest in SC circuits. Commonly used implementations of Class-AB MOS differential amplifiers correspond to implementations of the same basic scheme shown in Fig. 10(a) [43]. One example is the OTA based on DFVF and reported in [33] which has already been mentioned in Section IV-C-I.

Another low-voltage low-power Class-AB input stage was proposed by the authors in [9] using a FVFDP. The implementation of the new scheme is shown in Fig. 10(b). It is basically a FVFDP with a common-mode input signal detector (shown as a black box in Fig. 10(b). Assuming perfect matching between transistors M_1, M_3 and M_4, the common-mode detector provides a signal $V_1 = (V_3 + V_4)/2$ at the gate of M_1. In the case that linearity is of concern (for example for implementation of linear transconductors) cutoff of M_3 and M_4 must be avoided. The implementation of the common-mode signal detector of Fig. 10(b) is shown in Fig. 10(c) and has been reported elsewhere [43]. An even simpler implementation of the input common-mode sensor uses two equal valued resistors R_{CM} connected between both FVFDP input terminals and the gate of M_1. Fig. 10(d) shows a comparison of the simulated dc transconductance characteristics of a conventional Class-A differential amplifier and that of the FVFDP in Fig. 10(b). For the comparison, the same bias current $(I_b = 0.75\ \mu\text{A})$ was used. It can be seen that, as expected, the Class-AB input stage has an essentially larger maximum output current.

This FVFDP input stage was used to build low-voltage, low-power OTAs for SC applications [44]. Fig. 11(a) shows the first

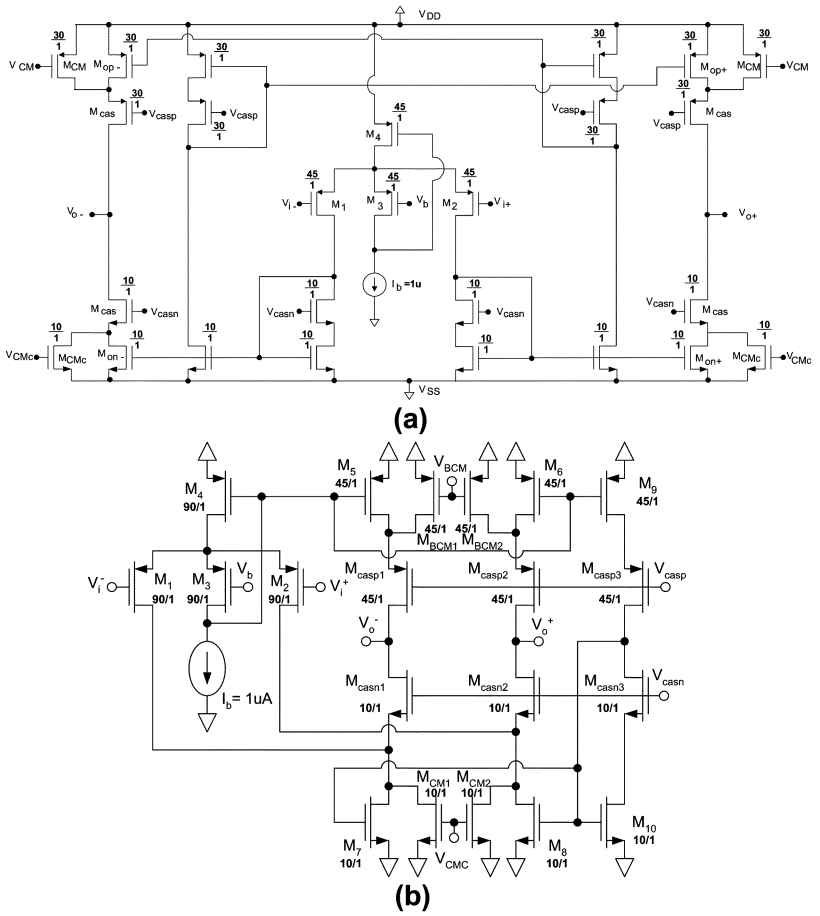

Fig. 11. (a) First proposed Class-AB OTA. (b) Second proposed Class-AB OTA.

Class-AB OTA. The output currents of the FVFDP are copied to the transconductor outputs using low-voltage current mirroring techniques. Note that the drain current of transistor M_1 is copied to the lower branch of the negative output V_o^- and to the upper branch of the positive output V_o^+. A similar rule applies to the drain current of transistor M_2. In this way, balance is maintained for the differential output current. Cascode transistors $M_{\rm cas}$ are optional, as they are used to increase the amplifier dc gain. The output common-mode voltage can be controlled using conventional SC common-mode sensing techniques, by means of the control voltage $V_{\rm CMc}$ and additional transistors $M_{\rm CMc}$.

Fig. 11(b) shows another Class-AB OTA with the same input stage. Even though it is similar in appearance to a conventional folded-cascode OTA, there are two main differences.

1) The input stage uses the FVFDP, providing Class-AB behavior.
2) The current of transistors M_5 and M_6 also has Class-AB behavior, as it is a copy of half the current flowing through transistor M_4.

Therefore, this circuit can be considered to be a fully differential Class-AB folded cascode amplifier.

Both OTAs have been designed using a 0.35-μm CMOS technology, achieving a 15-MHz gain-bandwidth product, and more than 70° phase margin with 1-pF load capacitor and 1.1-V supply voltage. Total power consumption was 12 μW for the circuit in Fig. 11(a) and 8 μW for the circuit in Fig. 11(b). Transistor sizes and biasing currents are shown in Fig. 11(a) and (b).

Although these OTAs have not a large CMRR, they are suitable for SC applications, where they are operated in an inverting, negative feedback configuration with a constant voltage at the input terminals, which allows the operation of the FVFDP without an input common-mode sensing network. The OTA in Fig. 11(a) was used in [45] to build a second-order sigma-delta modulator capable for operation at 1.1-V supply voltage, providing 86 dB of dynamic range in a 16-kHz bandwidth with only 35-μW of quiescent power consumption, which is in the state of the art of sigma–delta conversion.

2) Transconductance Multipliers: Analog CMOS multipliers find wide utilization in analog signal processing systems such as wide range adjustable linear transconductors, modulators, detectors, etc. The FVFDP can be used to build four quadrant transconductance multipliers.

The circuit shown in Fig. 12(a) is an OTA based on the basic transconductance multiplier (enclosed in a box in the Figure), which is a version of the classical multiplier [4], [46] based on two cross-coupled differential pairs. The novelty in the circuit of Fig. 12(a) is in the efficient implementation of the low-impedance voltage sources $V_{a'}$ and $V_{b'}$ by means of FVF circuits. This circuit has also Class-AB behavior as the quiescent output currents can be programmed by means of current sources I_b to be much lower than their maximum value. This fact makes

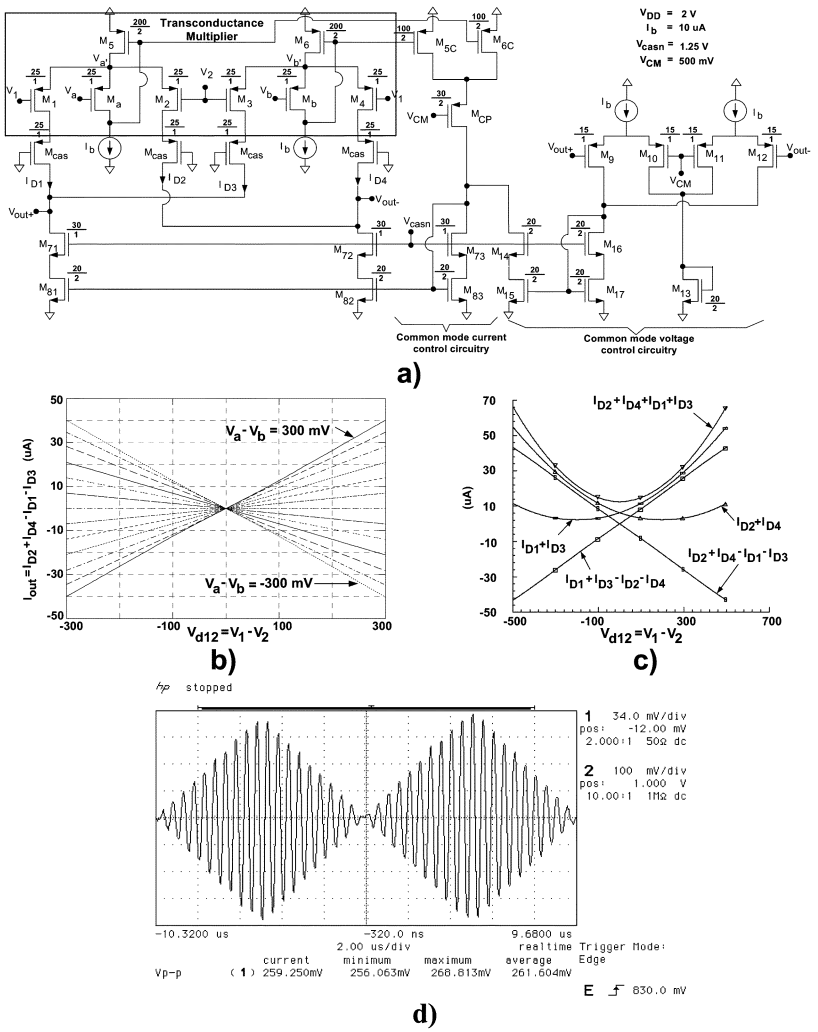

Fig. 12. (a) Proposed transconductor composed of a transconductance multiplier (circuit inside the box) and common-mode control circuits for output voltages and currents. (b) Differential output current for different values of $V_a - V_b$. (c) Circuit currents ($V_a - V_b = 200$ mV). (d)Experimental transient response.

this circuit very attractive for low-power applications. Assuming perfect matching between transistors M_1 to M_4, and using the square-law function of the MOS transistor in the saturation region, it can be shown that $I_{\rm out} = -k_P(W/L)_{M1-M4}(V_1 - V_2)(V_{a'} - V_{b'})$, where $k_P = (\mu_P C_{\rm ox})$.

A figure of merit for current-mode multipliers is the current efficiency (CE), defined by the ratio between the useful output current and the total current drained from the supply voltage. For the circuit inside the box in Fig. 12(a), $\mathrm{CE} = I_{\rm out}/(I_{D1}+I_{D2}+I_{D3}+I_{D4}) = (I_{D1}-I_{D2}+I_{D3}-I_{D4})/(I_{D1}+I_{D2}+I_{D3}+I_{D4})$. Since CE is a measure of power efficiency, Class-AB multipliers are expected to have a higher CE than Class-A multipliers.

In order to demonstrate the high current efficiency of this transconductance multiplier, some simulations are shown. Fig. 12(b) shows the simulated dc transfer curve for the transconductance multiplier of Fig. 12(a) in a typical case. It presents the typical behavior of a multiplier with a highly linear output current over a wide input range. Fig. 12(c) shows the output current $(I_{D1} + I_{D3} - I_{D2} - I_{D4})$ as well as the total current $(I_{D1} + I_{D3} + I_{D2} + I_{D4})$. It can be seen that the current efficiency becomes higher than 50%.

The transconductance multiplier inside the box of Fig. 12(a) was fabricated using 0.5 μm AMI CMOS technology. The multiplier was measured with $I_b = 10$ μA, a single supply $V_{\rm DD} = 1.4$ V and resistors $R_L = 1$ kΩ connected between the multipliers outputs and ground. Fig. 12(d) shows the experimental transient response of the transconductance multiplier using a triangular wave of 250 $\mathrm{mV}_{peak\text{-}to\text{-}peak}$ and 50 kHz for $V_a - V_b$ and a sinusoidal waveform of 450 $\mathrm{mV}_{peak\text{-}to\text{-}peak}$ and 2 MHz frequency for $V_1 - V_2$. The absence of an on-chip high-frequency buffer precluded the high-frequency measurement of this multiplier.

This transconductance multiplier can be also used as a programmable Class-AB transconductor. To this end, an output stage is necessary to provide high output impedance. In addition extra circuitry to control the common-mode value of the output voltages is required. However, unlike conventional Class-A transconductors, in the one proposed here, the common-mode value of the current is not constant $I_{oCM} = 0.5((I_{D1} + I_{D3}) + (I_{D2} + I_{D4}))$. Due to its Class-AB behavior, it depends on the differential value of the input voltages, as shown in Fig. 12(c). Therefore, additional circuitry to control the common-mode value of the currents is also required.

These three tasks can be performed in a compact and simple way if we take advantage of the special properties for sensing currents of the FVF structure. It is easy to demonstrate that the

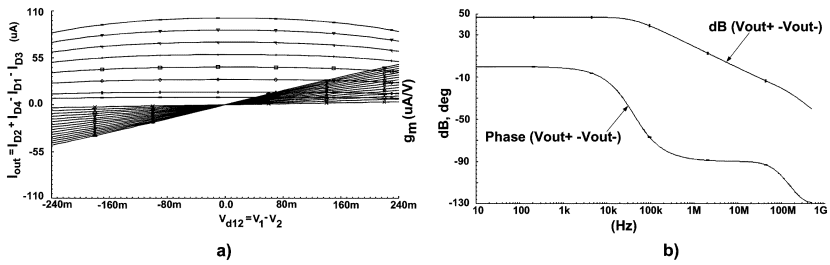

Fig. 13. Simulated performances for the circuit in Fig. 12(a). (a) DC transfer curve and transconductance. (b) AC response.

current through transistors M_5 and M_6 in Fig. 12(a) is $(I_{D5}+I_{D6})=(I_{D1}+I_{D3})+(I_{D2}+I_{D4})+2I_B=2(I_{oCM}+I_B)$ and therefore, they drive twice the common-mode output current I_{oCM} plus the bias current I_b. The solution proposed here is to sense these currents by means of current mirroring techniques, and to subtract a scaled copy of them from the output current, so as to keep the common-mode value of the output currents constant. Transistors M_{5C}, M_{6C}, $M_{\rm CP}$, M_{81}, M_{82}, M_{83}, M_{71}, M_{72} and M_{73} form the common-mode current control circuitry. The current flowing through transistor $M_{\rm CP}$ is the common-mode current plus I_b. Current I_b may be removed but it is used to bias the common-mode output voltage control circuit. A conventional common-mode feedback network has been used to control the common-mode value of the output voltages (left part of the circuit in Fig. 12(a). Finally, transistors $M_{\rm cas}$ have been included between the input transistors M_1, M_2, M_3, M_4 and the outputs of the transconductor to increase the output impedance and the dc gain of the transconductor.

The proposed transconductor has been designed using a standard 0.8-μm CMOS technology with threshold voltages of 700 and –800 mV, for nMOS and pMOS transistors, respectively. The circuit has a quiescent power consumption of only 260 μW with a 2-V supply voltage for the nominal transconductance value $(V_a-V_b=200\ \text{mV})$. Fig. 13(a) shows the simulated dc output currents and transconductance. A wide transconductance adjustment range (g_m) is achieved (from 0.6 to 207 μA/V) with a small variation in power consumption (from 240 to 380 μW). Fig. 13(b) shows the ac response of the voltage gain with a load capacitor of 2 pF connected between the outputs of the transconductor. A dc gain of 47 dB and a unity-gain bandwidth of 90 MHz can be observed. Transient simulations with a 10.7-MHz sinusoidal input signal show less than 1% of total harmonic distortion (THD) for a differential input voltage of 600 mV (with $V_a-V_b=200$ mV). The complete circuit remains operational down to 1.4 V of supply voltage.

V. Translinear Circuits Using the FVF Cell

This section shows, as an example, the abilities of the FVF to solve the problems which appear when operating analog and mixed-signal systems with a low voltage supply. To this end, a set of new translinear circuits that overcome the voltage limitations of previous implementations are proposed and experimentally verified.

Various low-voltage translinear (TL) techniques in MOS technologies have been proposed recently. In [47], very low voltages are achievable, yet operating the loop transistors in weak inversion mode and thus leading to poor matching characteristics and restricting their operation to several tens of kilohertz. An alternative approach that does not have the aforementioned limitations is to exploit the approximately square law of MOS transistors in strong inversion and saturation,

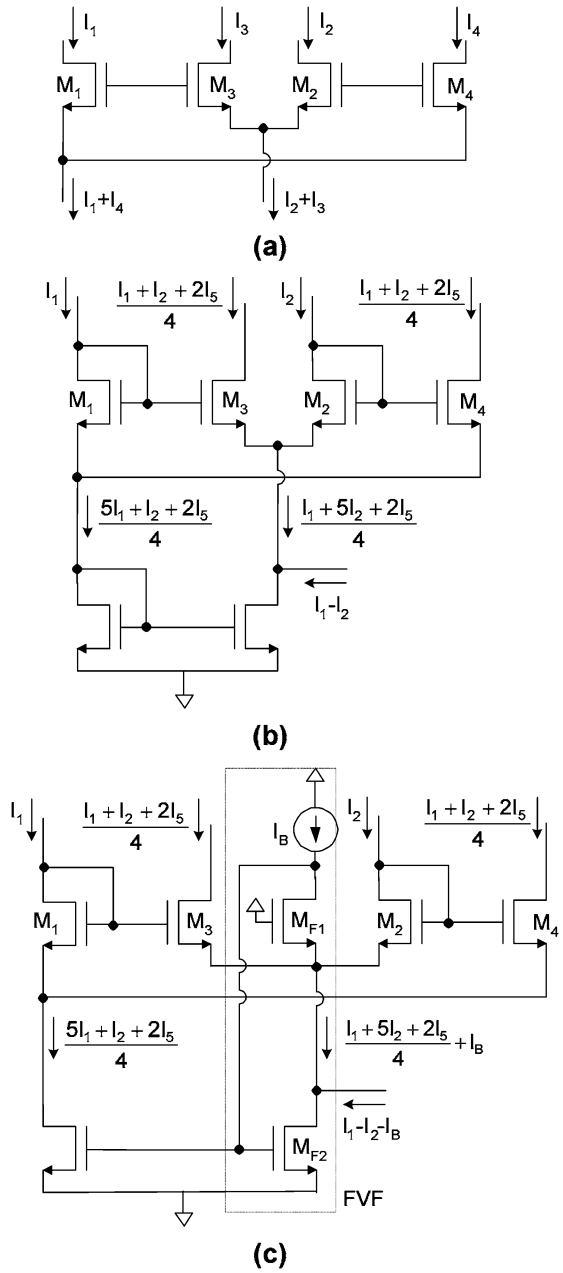

Fig. 14. (a) Second-order folded voltage-translinear loop. (b) Conventional biasing. (c) Biasing using FVF.

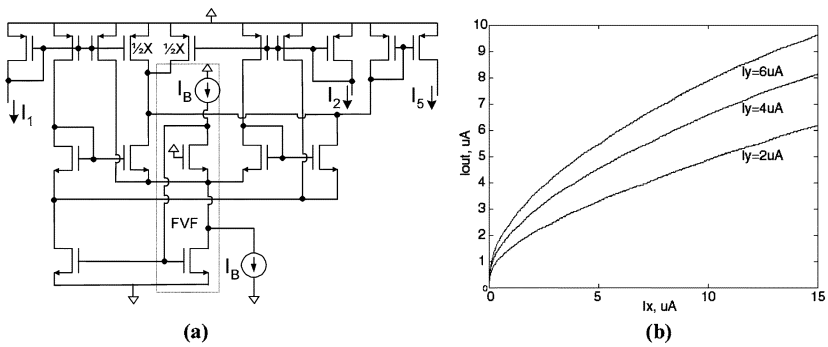

Fig. 15. (a) Proposed geometric-mean circuit. (b) Measured geometric-mean output for different input currents.

leading to the so-called voltage-TL loops [48]. Unfortunately, the resulting loops are not well suited for very low voltage applications if conventional biasing strategies are employed for the loop transistors [49]–[51]. In this section, we propose an alternative biasing of voltage-TL loops based on the application of the FVF [52] that allows significantly to reduce the supply voltage requirements. The resulting loop topologies can advantageously replace conventional ones employed for building either static nonlinear computational circuits (e.g., geometric-mean, square-root, squarer/divider, vector normalization) or dynamic linear and nonlinear circuits (e.g., companding filters and RMS-dc converters) leading to a new family of very low voltage analog signal processing circuits based on the voltage-TL paradigm.

A. FVF Voltage Translinear Loops

Fig. 14(a) shows a folded second-order voltage-TL loop. Using the MOS square law and assuming that all transistors are equal, loop currents are related by the equation

$$\sqrt{I_1} + \sqrt{I_2} = \sqrt{I_3} + \sqrt{I_4}. \tag{7}$$

Hence, several nonlinear current-mode functions can be implemented by properly injecting such currents. For instance, if we force

$$I_3 = I_4 = \frac{I_1 + I_2 + 2I_5}{4} \tag{8}$$

being I_5 a certain current, after squaring both sides in (7) and rearranging, currents I_1, I_2 and I_5 become related by

$$I_5 = \sqrt{I_1 I_2}. \tag{9}$$

Therefore, a geometric-mean circuit is obtained if I_1 and I_2 are the input currents and the output current is a copy of I_5. Alternatively, a squarer/divider is obtained if the output is a copy of I_2 and the inputs are I_5 and I_1.

The simplest way to force (8) is to use the well-known structure of Fig. 14(b), commonly employed in practice [49]–[51]. However, the diode-connected MOSFET of the current mirror precludes very low voltage operation due to the stacking of two diode-connected transistors. Equation (8) can be alternatively implemented using the novel topology of Fig. 14(c). Now a FVF, formed by transistors M_{F1} and M_{F2}, sets the proper reference dc voltage at the loop nodes. An adequate choice of current I_B allows setting the desired voltage at the source of transistor M_{F1}, ensuring the correct operation of the lower current mirror. If the aspect ratio of M_{F1} is properly chosen, I_B can be made small, so that the increase in current consumption is very modest. An additional advantage is that the source of M_{F1} is a very low impedance node, so that voltage at this node is kept essentially constant regardless of the input and output current levels.

B. Static Nonlinear Circuits

The FVF voltage-TL loop can be employed for implementing several static nonlinear processing circuits, where the FVF cell not only decreases the supply voltage requirements but also improves performance. Its application to a geometric-mean circuit, a squarer/divider circuit and a multiplier/divider circuit will be presented in this section.

1) Geometric-Mean Circuit: A low-voltage geometric-mean circuit implementing (9) can be readily obtained according to the guidelines in Section V-A, based on the topology of Fig. 14(c). The complete schematic is shown in Fig. 15(a). Note that the current $I_1 - I_2$ injected in the drain of M_{F2} in Fig. 14(c) has been replaced in Fig. 15(a) by a direct injection of I_2 in the common source of $M_1 - M_4$, and by a direct injection of I_1 in the common source of $M_2 - M_3$. The circuit was fabricated in a 2.4 μm DPDM n-well CMOS process, with threshold voltages of, approximately, 0.80 V for nMOS transistors and 0.88 V for pMOS transistors. The aspect ratio of the loop transistors was 80 μm/4.8 μm, whereas bias current was $I_b = 2$ μA. Supply voltage was 1.5 V. Fig. 15(b) shows the measured output current of the geometric-mean cell for input current $I_X = I_1$ varying from 0 to 10 μA and input current $I_Y = I_2$ stepped from 2 μA to 6 μA in 2 μA steps. Note how the circuit can operate as a variable-gain square-rooting cell.

2) Squarer/Divider Circuit: As described in Section V-A, a squarer/divider can be readily obtained based on the topology shown in Fig. 14(c), being the only difference with the geometric-mean cell that the output current was a copy of I_2 instead of I_5, as mentioned previously. The complete schematic is shown in Fig. 16(a), being very similar to the geometric-mean circuit. The same transistor sizes, supply voltage and bias current are used, and just an input terminal is transformed into an output one (and vice versa) with regard to the circuit in Fig. 15(a). It was also fabricated in the same process. Fig. 16(b) shows the output of the squarer/divider cell for input currents $I_Y = I_5 = 10$ μA and $I_X = I_1$ varying from 0 μA to 10 μA. The theoretical response is shown in the dotted curve, whereas the measured one corresponds to the solid one. The relative

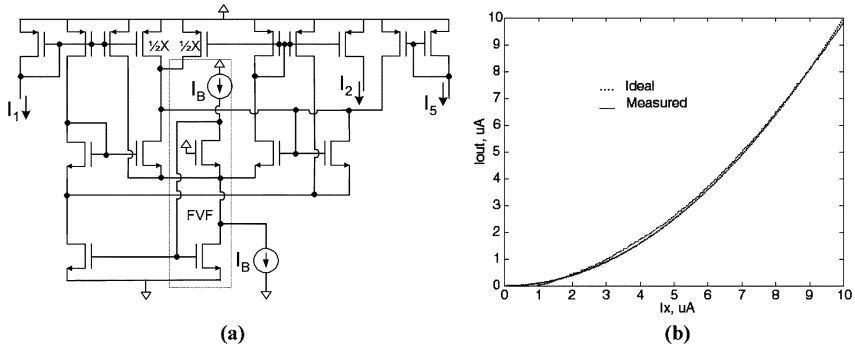

Fig. 16. (a) Proposed squarer/divider circuit. (b) Measured and ideal output of the squarer/divider circuit.

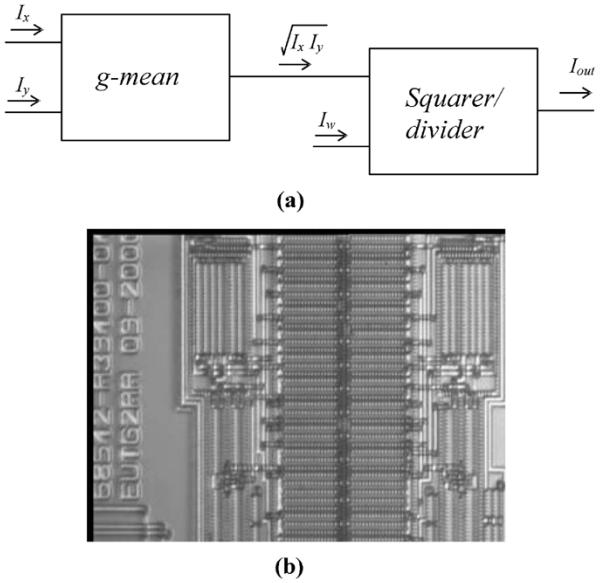

Fig. 17. (a) Multiplier/divider circuit. (b) Microphotograph of the multiplier/divider.

error of the output is less than 2%, a similar accuracy than that measured for the geometric-mean cell. The total silicon area employed for either the geometric-mean circuit or the squarer/divider circuit was 0.09 mm^2.

3) Multiplier/Divider Circuit: The cascade connection of the former circuits can be employed for building a low-voltage multiplier/divider circuit [50], as shown in Fig. 17(a). The geometric-mean circuit generates a current related to its input currents I_x and I_y given by

$$I_{gm} = \sqrt{I_x I_y} \tag{10}$$

which is injected (once reversed by a current mirror if necessary) into the squarer/divider circuit, so that its output is given by

$$I_{\text{out}} = \frac{(\sqrt{I_x I_y})^2}{I_w} = \frac{I_x I_y}{I_w} \tag{11}$$

leading to the multiplier/divider operation. Fig. 17(b) shows a microphotograph of the circuit, fabricated in the aforementioned process. The total area is 0.19 mm^2. When used as a gain cell, measured THD is less than 3% for a supply voltage of 1.5 V and peak input currents up to 20 μA. A similar circuit was fabricated in the same technology having conventional voltage-TL loops instead of the FVF biased loops and reported in [50]. It achieves a 3% THD for a 3.3-V supply and 20-μA peak input currents. This fact evidences the superior performance of FVF voltage-TL loops at low supply voltages.

4) Dynamic Linear Circuits: The FVF voltage-TL loop can also be employed as the basic building block for implementing dynamic linear (ie. filters) and nonlinear transfer functions in a very low-voltage environment. A method for synthesizing these circuits from geometric-mean and squarer/divider blocks was described in [51]. The use of the former FVF-based voltage TL loops for implementing such basic building blocks lead to topologies equating or even improving the performance of former proposals [51], [53], [54] at a much lower supply voltage. If the internal nonlinearities are chosen in such a way that they cancel out externally, an overall linear dynamic transfer function is obtained. This last method is employed for building a type of current-mode companding filters known as square-root domain (SRD) filters [51]. Voltage at the capacitor nodes in these filters are compressed according to a square-root law.

Fig. 18(a) shows a first-order current-mode SRD filter, based on two geometric-mean cells and a squarer/divider cell. The filter cutoff frequency and dc gain are given by

$$\omega_{-3\text{dB}} = \frac{\sqrt{2\beta I_{B1}}}{C} \tag{12}$$

$$k = \sqrt{\frac{I_{B2}}{I_{B1}}} \tag{13}$$

being β the transconductance factor of the input and output MOS transistors. Such a filter, using conventional voltage-TL loops, is presented in [51], requiring a single 3.3 V supply. When using the FVF voltage-TL loops proposed here for implementing the geometric-mean and squarer/divider circuits, comparable tuning range and distortion levels are obtained for a single 1.5 V supply and for the same process. The novel FVF-based filter was fabricated in this 2.4 μm CMOS process, based on the blocks of Figs. 15(a) and 16(a). Its total area was 0.3 mm^2. The capacitor was not integrated, so that an external 1 nF capacitance was employed. Fig. 18(b) shows the frequency response of the filter for different bias currents, ranging from $I_{B1} = I_{B2} = 2.5$ to 7.5 μA in 2.5-μA steps. Note how an independent frequency tuning can be achieved, thus agreeing with the expected behavior given by (12) and (13).

The measured time response of the circuit was subsequently evaluated, using 10-μA bias currents. The dotted waveform in the upper half of Fig. 18(c) shows the input current, a 1-kHz sinusoid with 20-μA peak-to-peak amplitude and 10-μA dc

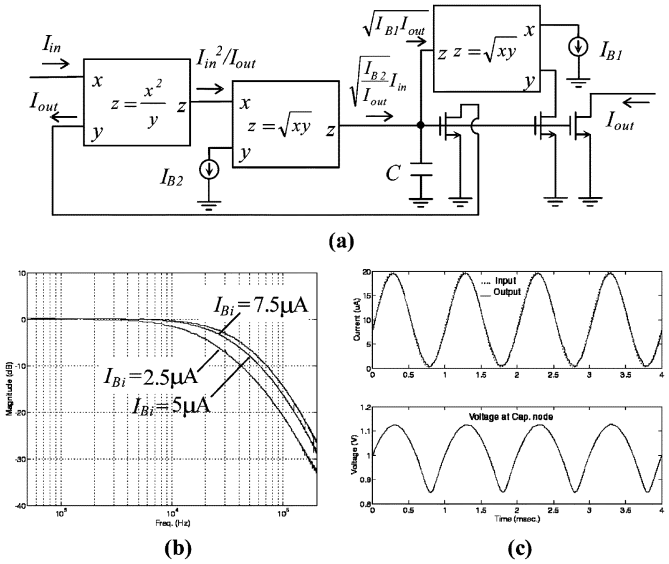

Fig. 18. (a) SRD first-order filter. (b) Measured frequency response for bias currents stepped from 2.5 to 7.5 μA in 2.5-μA steps. (c) Measured time response. Upper half: input current (dotted sinusoid) and output current (solid sinusoid). Lower half: capacitance voltage.

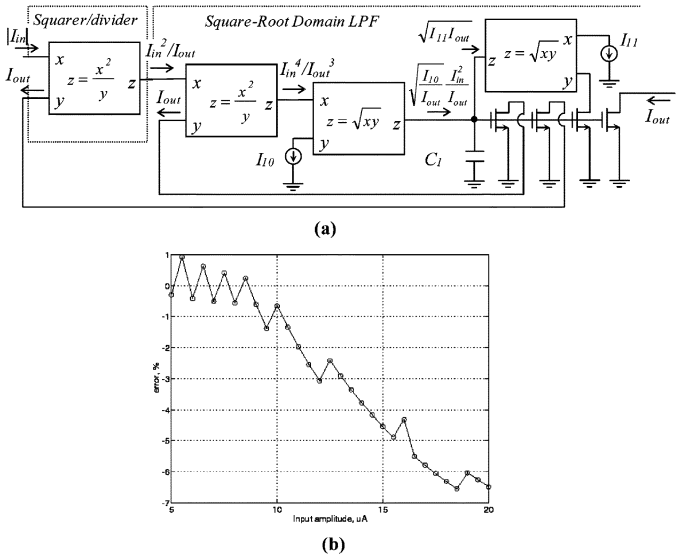

Fig. 19. (a) RMS-DC converter. (b) Measured error versus input current amplitude.

offset, whereas the solid sinusoid close to it corresponds to the output current. Note that distortion in the output waveform is negligible, and only a small phase shifting due to the filtering action allows to distinguish the input and output waveforms. In fact, a 1.2% THD was measured for this output. This modest distortion is obtained even though the capacitance voltage is strongly distorted, as can be noticed from the lower half of Fig. 18(c), thus highlighting the voltage companding nature of the circuit, which is externally linear but not internally. The FVF cell combined with the synthesis method in [51] allows us to extend these ideas to the implementation of higher order very low voltage filters.

5) Dynamic Nonlinear Circuits: Apart from the particular input-output nonlinearity cancellation in SRD filter design, the former circuits allow in general the implementation of nonlinear time-dependent transfer functions that can also benefit from the FVF voltage-TL cell for achieving very low- voltage operation. This idea will be illustrated with the implementation of a current-mode rms-dc converter operating at a 1.5-V single supply.

RMS-DC conversion constitutes one of the most notable instances of nonlinear dynamic operation from a practical viewpoint. It its basic form, and assuming input and output currents, such operation can be described by

$$I_{\rm out} = \sqrt{\langle I_{\rm in}^2 \rangle} \tag{14}$$

where $I_{\rm in}$ and $I_{\rm out}$ are the input and output currents of the RMS-DC converter, respectively, and the operator $\langle \cdots \rangle$ represents a time averaging. A (mathematically equivalent) approach, with better results in terms of offset [55], is given by

$$I_{\rm out} = \left\langle \frac{I_{\rm in}^2}{I_{\rm out}} \right\rangle. \tag{15}$$

Hence, two operations have to be performed: squaring/division and subsequently, averaging. Thus, a very low voltage rms–dc converter can be implemented using the SRD filter of Fig. 18(a) and the squarer/divider of Fig. 16(a), combined as shown in Fig. 19(a). Both circuits, fabricated on the same integrated circuit, were connected according to this figure to build the rms–dc converter. The area occupied was, therefore, 0.4-mm^2. A 150-nF external capacitor was employed in the filter. Bias currents were set to 10 μA, and $V_{\rm DD}$ was 1.5 V. A full-wave rectified signal was provided by an Arbitrary Waveform Generator, whose output voltage was transformed into the input current by a current conveyor using a 10-kΩ resistor. The output current of the rms–dc converter was measured across a 10-kΩ resistor. The measured relative error of the output for a rectified 10 kHz input current, as a function of the input amplitude, is shown in Fig. 19(b). It is noticeable that errors are below $\pm 2\%$ for input amplitudes beyond 10 μA. The accuracy obtained is similar to other proposals for rms–dc converters (e.g., [54], [55]). In particular, that reported in [54] uses the same topology and fabrication process but with conventional voltage-TL loops, operating at 3.3 V. Therefore, the use of the FVF cell allows the rms–dc supply voltage to decrease from 3.3 to 1.5 V without a penalty in circuit performance.

Concerning the measurement results presented in this section, it should be noticed that the fabrication process employed (2.4 μm CMOS) featuring low transistor transconductance and large threshold voltages does not allow to fully exploit the advantages in terms of supply voltage reduction achievable in these circuits thanks to the FVF cell. Simulation results using BSIM3v3 models for a 0.8-μm CMOS process were conducted, allowing the FVF voltage TL loops to operate at supply voltages below 1.2 V with similar performance. Operation at 1 V is also possible using modern deep submicron processes.

VI. Conclusion

In this paper, a cell coined as FVF has been revisited. Its usefulness in different applications in low-power/low-voltage analog design has been evidenced. A detailed analysis of the

cell, together with a classification of its applications based on the way the cell is employed has been provided. Several new circuits that exploit their Class-AB behavior in low-power, low-voltage environments have been also presented. These circuits have found a large variety of applications, such as current conveyors, current mirrors, current sensors, voltage buffers, multipliers, OTAs, and input and output stages for operational amplifiers. Some of these circuits have been recently published and new ones have been presented here. A complete design example of how to apply the cell in order to improve the performance of a circuit in low-voltage/low-power environments has been offered and verified on silicon. Simulations and experimental result support the utility of this cell for low-power, low-voltage analog circuit design.

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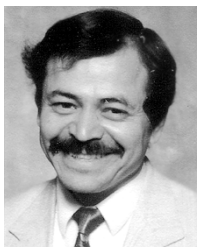

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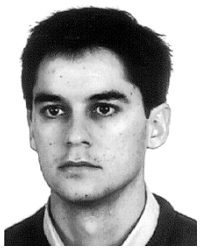

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