Comparison of CMOS VCO Topologies

Michael Haase, Viswanathan Subramanian, Tao Zhang, Amin Hamidian
Microwave Engineering Lab, Berlin Institute of Technology
10587 Berlin, Germany
haase@mwt.ee.tu-berlin.de

***Abstract*—In this work the phase noise behavior of integrated LC VCOs in 130 nm SiGe BiCMOS technology is investigated. Three different VCO topologies i) Full NMOS ii) Full PMOS and iii) Complementary NMOS PMOS structures have been considered for investigation. Through circuit level simulations, the dependency of the phase noise on various parameters like frequency of operation, transistor type, transistor width and transit frequency has been studied and various tradeoffs will be discussed and validated. Using foundry based RF transistor models the comparison of the VCOs has been made at three different operating frequencies: 5 GHz, 15 GHz, and 25 GHz. It will be shown that with ideal passive elements, the PMOS VCO structure achieves the best phase noise performance at 15 GHz and higher operating frequencies.**

Keywords-component - LC-tank, VCO, phase noise, thermal noise, flicker noise, phase locked loop.

I. INTRODUCTION

The demand for a higher data rate and further miniaturization in wireless applications like communications, sensor networks and geo-positioning drives the development of large scale system-on-chip in CMOS technology. Following the trend using smaller CMOS geometries the VCO design becomes more and more critical. In this work, various VCO topologies are investigated and compared in conjunction with a transceiver for low power sensor networks. The goal of such a system is a distance measurement using 250 MHz bandwidth allocated in the 24 GHz ISM band. A FMCW modulation scheme well known from RADAR applications is employed. High precision distance measurements imposes stringent accuracy requirements to the LO (Local Oscillator) signal. Therefore VCOs with low phase noise and a high operating frequency are required.

LC tank oscillators [1] are widely used because they exhibit low phase noise operation up to the millimeter wave band. In addition, planar inductors as part of resonator are employed instead of transmission lines. These properties make them attractive for large scale integration in CMOS technology.

The ongoing progress in the understanding and modeling of phase noise [2,3,4] enabled the circuit designers to improve the phase noise performance in a large number of realizations [5,9-12]. Despite those efforts in the LC VCO design at frequencies around 25 GHz, challenging problems arise in the inductor modeling and particularly device sizing.

The impact of the device type and sizing on the VCO performance has been investigated in [6]. It has been concluded that the switching noise of cross coupled transistors is superior to current bias noise. In the same work, the AM/PM conversion coefficient has been considered as a measure for the noise. Finally it has been stated that the phase noise can be improved effectively by finding the optimum width of the switching transistors or setting the optimum overdrive voltage for the switching transistors.

In this work three different LC VCO architectures have been investigated. Performance parameters such as the frequency, device type, device size, transit frequency and phase noise have been considered. Various tradeoffs have been discussed and validated through circuit level simulations.

This paper is organized as follows: In section II the NMOS LC VCO, the PMOS LC VCO and the complementary NMOS PMOS LC VCO are introduced and discussed. In section III all LC VCO architectures are compared and assessed against the background of phase noise in 5 GHz, 15 GHz and 25 GHz operating frequencies.

II. VCO TOPOLOGIES

A 130 nm SiGe BiCMOS technology is employed for VCO design. This technology allows low supply voltage operation at 1.2 V. Figure 1 shows the analyzed VCO topologies which will be explained and investigated.

A. NMOS LC VCO

In Figure 1 (a) a LC VCO based on NMOS transistors is depicted. It consists of a NMOS current source, cross coupled NMOS switches, two inductors and a varactor.

The inductor with the varactor form a LC tank. The negative resistance of the oscillator is given by the transconductance of the cross coupled NMOS devices. It injects energy to compensate the losses of the tank and maintain the oscillation (Barkhausen criterion).

The varactor is separated from the supply by the inductor and from the ground by the cross coupled NMOS pair and the current source. The inductors are directly connected to the supply. Unfortunately this makes the oscillator more sensitive to disturbances from the supply. However the current source provides a good rejection to the LC tank against the ground. The implementation of the switching transistors and the current source forms a symmetrical differential pair which causes a lower harmonic distortion.

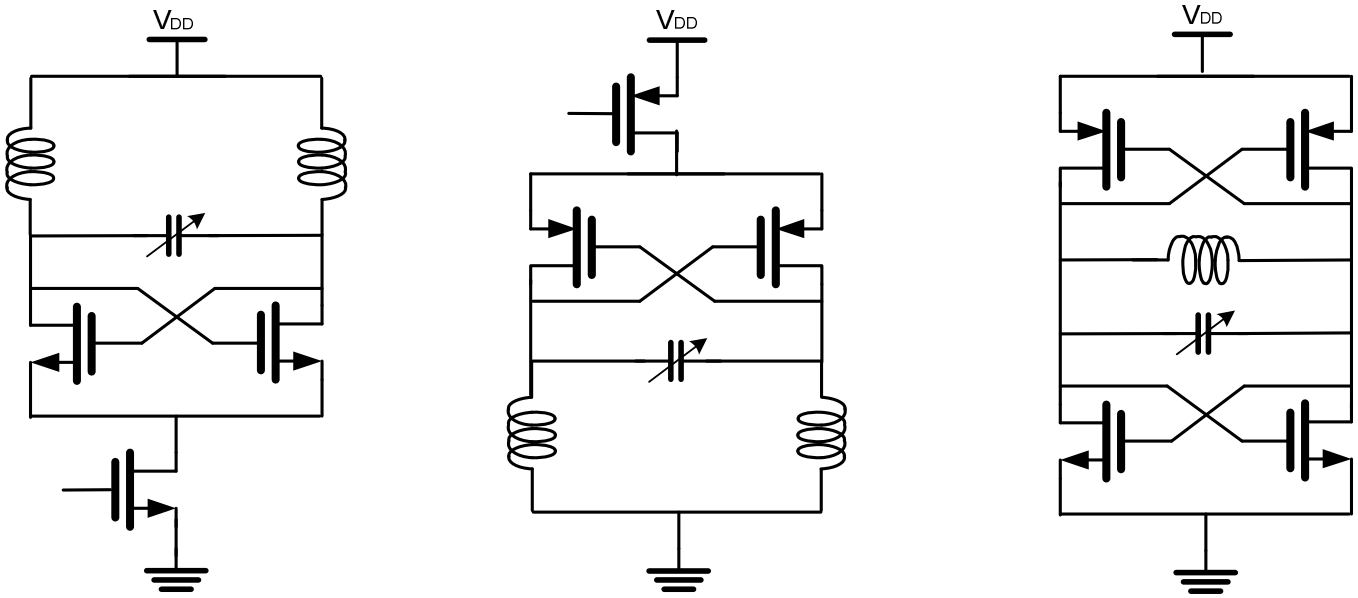


Figure 1. . (a) NMOS LC VCO (b) PMOS LC VCO (c) NMOS PMOS LC VCO

Although the oscillator operates under low voltage conditions, the available headroom enables a maximum tuning range. The capacitance of the varactor is controlled by the tuning voltage. If the bulk voltage is tied to the supply voltage, the varactor works from the depletion – to the weak inversion region, where the capacitance tuning voltage characteristic achieves its best linearity. The varactor also upconvertes noise depending on nonlinear behavior of the tuning capacitance. The phase noise performance is determined by the quality factor of the inductor and varactor according to the Leeson [2] formula (1).

Apart from the quality factor, the phase noise performance is additionally affected by the current source and voltage across the LC tank.

B. PMOS LC VCO

Figure 1 (b) shows a LC VCO based on PMOS transistors. The structure is fully complimentary to NMOS LC VCO (Figure 1 (a)).

However for comparison reasons, the PMOS transistor is sized three times larger compared to the NMOS counter part in order to achieve the same transconductance and to provide the same negative resistance. The reason is the reduced mobility of holes in the PMOS transistor. Further the current density in the PMOS transistor is lower compared to the NMOS transistor, which leads to inherent less thermal and flicker noise contribution. Therefore the noise factor is lower for PMOS based VCO structures. This results in a better phase noise performance as will be shown in the comparison section.

C. Complementary NMOS PMOS LC VCO

The complementary NMOS PMOS LC VCO, shown Figure 1 (c), exhibits two structural differences: The negative resistance is provided by the NMOS and PMOS cross coupled pair and the inductive loads in Figure 1 (a) or Figure 1 (b) are replaced with a differential inductor.

The NMOS and PMOS transistors are operating in a mutual switching scheme during one half period. Thus the amplitude of the voltage across the LC tank is increased. The drawback of such a structure is the sensitivity to supply noise. Due to the higher harmonic distortion the thermal – and flicker - noise will be upconverted.

Finally complementary structure exhibits immunity against process variations due to the presence of both PMOS and NMOS cross-coupled pairs. This makes it more attractive for deep submicron CMOS technologies

III. COMPARISON

A. Methodology

Phase noise is the key property to evaluate the oscillator performance. According to the Leeson formula [2] the phase noise behavior can be modeled using an empirical approach as given by:

$$L(f_m) = \frac{2kT\,\mathrm{Re}_q F}{V_0^2}\left(\frac{f_0}{2Qf_m}\right)^2\left(1+\frac{\Delta f_{1/f^3}}{f_m}\right) \qquad (1)$$

Where:

- V_0 is the amplitude across the LC tank

- R_{eq} is the equivalent tank resistance
- f_0 is the carrier frequency
- f_m is the offset frequency
- Q is the quality factor of the LC tank
- $\Delta f_{1/f}^3$ is the flicker noise corner frequency
- F is the noise factor

In simulations f_0, and Q are set to be constant. Further, a constant power consumption of 4.8 mW has been chosen for all the VCOs. The LC tanks are implemented with ideal inductance and capacitance. The phase noise performance of all the three topologies are investigated for three different operating frequencies 5 GHz, 15 GHz and 25 GHz at various frequency offsets. The simulation results and the analyses are presented in the following section.

B. Simulation Results and Discussion

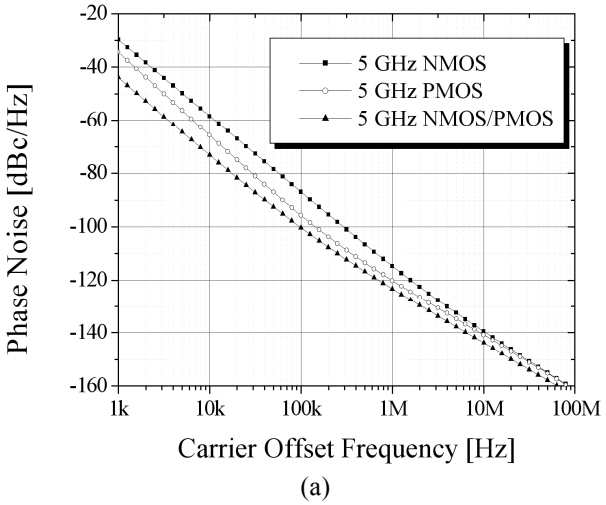
In Figure 2 (a) the phase noise of the NMOS LC VCO (Fig. 1 (a)) and the PMOS LC VCO (Fig. 1 (b)) at a frequency of 5 GHz is plotted. NMOS, PMOS switches each with 20 µm and 60 µm width and a complementary NMOS/PMOS have been simulated at 5 GHz. An LC tank with ideal components has been implemented. Table I summarizes the performance of the VCOs at 5 GHz at three different offsets.

It can be seen that the phase noise of PMOS VCO structure achieves a better performance than the full NMOS VCO. The reason for this is the inherent better flicker noise of the PMOS device. The best phase noise performance is shown by the complementary NMOS/PMOS VCO. This structure omits the current source. Therefore the headroom is increased and thus the voltage across the tank which leads to better phase noise values.

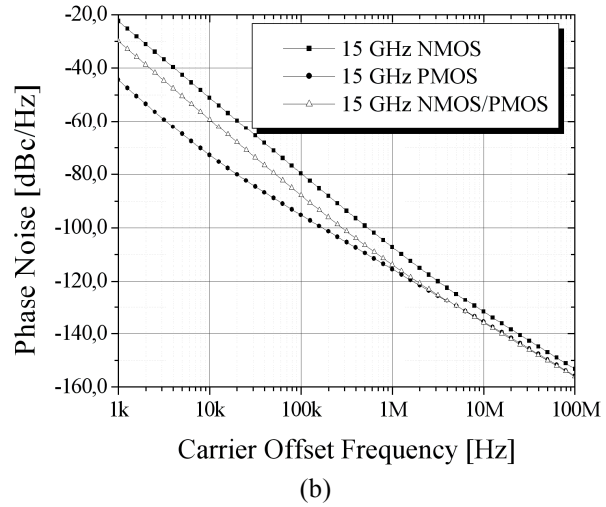
TABLE I. PHASE NOISE AT 5 GHZ

Δf [Hz]	NMOS PN [dBc/Hz]	PMOS PN [dBc/Hz]	NMOS/PMOS PN [dBc/Hz]
10 k	-58	-65	-73
100 k	-86	-95	-100
1 M	-114	-120	-123

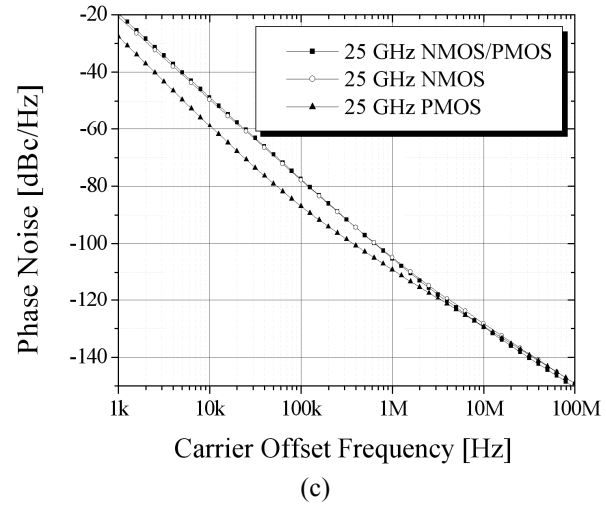
In Figure 2 (b) the phase noise results of the NMOS, PMOS and complementary NMOS/PMOS VCOs at 15 GHz are presented. With respect to the 5 GHz experiment it can be seen that the NMOS/PMOS VCO performance is degraded. The increased noise in the $1/f^3$ region is due to AM/PM conversion of switching noise of the cross coupled NMOS/PMOS transistor pair.



(a)



(b)



(c)

Figure 2. Phase noise plot (a) 5 GHz, (b) 15 GHz, (c) 25 GHz

TABLE II. PHASE NOISE AT 15 GHZ

Δf [Hz]	NMOS PN [dBc/Hz]	PMOS PN [dBc/Hz]	NMOS/PMOS PN [dBc/Hz]
10 k	-51	-72	-59
100 k	-79	-95	-87
1 M	-107	-115	-113

Figure 2 (c) plots the phase noise results at 25 GHz. It can be seen that the PMOS VCO achieves again the best phase noise performance compared to the rest. The phase noise performance of the complementary NMOS/PMOS VCO is degraded with respect to the NMOS and PMOS due the above mentioned reasons together with larger parasitic effects leading to amplitude degradation. Finally the NMOS VCO has over all the three simulated frequencies the poor phase noise results compared to the other topologies. At 15 GHz and higher operating frequencies up to 25 GHz, the full PMOS architecture has the best phase noise performance because of a lower flicker noise and low noise upconversion.

TABLE III. PHASE NOISE AT 25 GHZ

Δf [Hz]	NMOS PN [dBc/Hz]	PMOS PN [dBc/Hz]	NMOS/PMOS PN [dBc/Hz]
10 k	-49	-58	-48
100 k	-77	-86	-77
1 M	-104	-109	-105

IV. CONCLUSION

In this work three VCO topologies operating at 5 GHz, 15 GHz, 25 GHz have been analyzed, compared and investigated. At various frequency offsets, the phase noise performance under constant power consumption has been compared at three different operating frequencies. Two fundamental observations have been made: At first the PMOS VCO achieves a better phase noise over all three simulated frequencies. Secondly the phase noise results of the PMOS VCO are better than the NMOS counter part and the complementary NMOS/PMOS at 15 GHz and 25 GHz. Hence for the chosen scenario, it can be concluded that by proper optimization PMOS VCOs can achieve an overall better phase noise performance compared to NMOS.

V. REFERENCES

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