A 16-bit 250-MS/s IF Sampling Pipelined ADC With Background Calibration

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***Abstract*—This paper describes a 16-bit 250 MS/s ADC fabricated on a 0.18 μm BiCMOS process. The ADC has an integrated input buffer with a new linearization technique that improves its distortion by 5–10 dB and lowers its power consumption by 70% relative to the state of the art. It demonstrates a new background calibration technique to correct the residue amplifier (RA) gain errors and lower its power consumption. This summing node sampling (SNS) calibration technique is based on sampling the summing-node voltage of the residue amplifier and using it with the corresponding residue to estimate the amplifier open loop gain. The ADC achieves an SNDR of 76.5 dB and consumes 850 mW from a 1.8 V supply, while the input buffer consumes 150 mW from a 3 V supply. Up to 125 MS/s, the SFDR is greater than 100 dB for input frequencies up to 100 MHz and 90 dB up to 300 MHz input frequency. At 250 MS/s, the SFDR is greater than 95 dB up to 100 MHz and 85 dB up to 300 MHz.**

***Index Terms*—A/D converter (ADC), background calibration, buffer, IF sampling, pipeline, sample-and-hold amplifier (SHA)-less.**

I. Introduction

WIRELESS communication applications have driven the development of high-resolution A/D converters (ADCs) with high sample rates, good AC performance and IF sampling capability to enable wider cellular coverage, more carriers, and to simplify the system design. Some systems, like multi-carrier GSM and long term evolution (LTE) over GSM, require a signal-to-noise ratio (SNR) higher than 75 dB and a spurious-free dynamic range (SFDR) better than 95 dB for high input frequencies. In addition, bandwidths up to 75–100 MHz are needed in some systems, which dictate a sample rate of about 250 MS/s. These specifications are also needed in some other applications, such as instrumentation and imaging, which benefit from the high-speed IF sampling with such a high performance.

One major challenge in achieving this combination of high SNR and high SFDR is that it requires a large sampling capacitor to reduce the integrated thermal noise (kT/C noise). This large capacitance is difficult to drive while keeping the distortion low. An input buffer using bipolar transistors (BJTs) is needed in order to reduce the charge injection (kick-back) on the ADC driver and help achieve the desired linearity. The state of the art of this buffer consumes a large amount of power (500 mW to 1 W) and achieves an SFDR of about 95 dB at 100 MHz input frequency and 125 MS/s sample rate [1]. In this work, we employ a new linearization technique in the input buffer that helps improve the performance while lowering the power consumption substantially.

In addition, the large sampling capacitance leads to high power consumption in the MDAC's (multiplying DACs) residue amplifier (RA) that drives it. The targeted high performance and sample rate, which is twice as fast as the prior art [1], [2], require the RA to have a high gain and a very large bandwidth. This is aggravated even further in the first stage by using a SHA-less architecture [3], where the sample-and-hold amplifier (SHA) is removed to reduce power consumption and improve linearity. To reduce the power consumption, we employ background calibration to relax the gain requirement of the first stage RA. This new calibration technique relies on sampling and digitizing the summing node voltage and statistically estimating the amplifier gain digitally using the summing node and the residue voltages.

In this paper, we describe a 16-bit ADC with a sample rate up to 250 MS/s [4]. The ADC is implemented on a 0.18 μm BiCMOS process with an integrated highly linear input buffer and background calibration of the first stage RA gain errors. Section II describes the ADC architecture and some implementation issues. Section III covers the input buffer and the sampling network. Section IV discusses the background calibration algorithm and the RA analog design. Section V presents the whole ADC measurement results and finally Section VI concludes the paper.

II. ADC Architecture

The architecture of this paper's ADC is shown in Fig. 1. The pipelined ADC is SHA-less, where the sample-and-hold circuit is integrated with the first stage MDAC. An input buffer is used to improve distortion, reduce the kick-back from the ADC sampling capacitor and make it easier to drive. Although it increases the power and noise of the ADC, a highly linear input buffer is essential to provide the low impedance required to achieve the targeted high linearity. It is composed of three parallel buffers as shown in Fig. 2. Two buffers (B2) drive the bootstrap circuit and back-gate switching circuit of the input switch. The third (B1) drives the input switch and sampling capacitance. This separation is done to isolate the charge injection and non-linear load of the secondary paths (B2) from the main input path (B1). In addition, since the low distortion is needed only in the main

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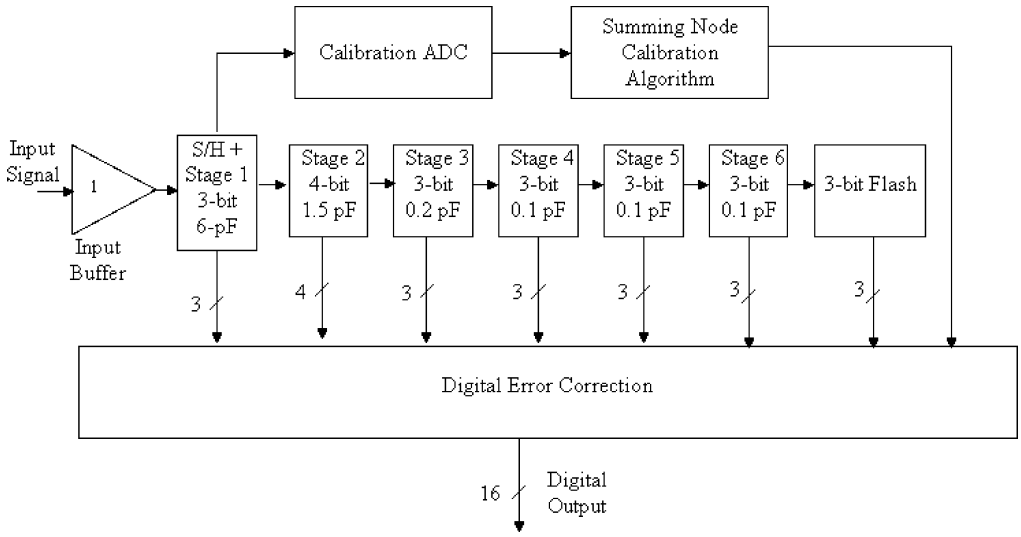


Fig. 1. Block diagram of the ADC.

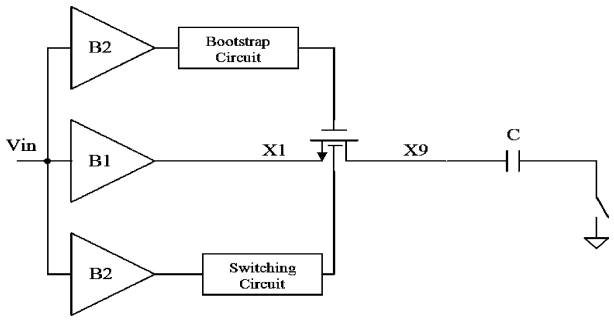


Fig. 2. A simplified schematic of the input sampling network showing the three buffers driving the main path (B1), the bootstrap path and the back-gate path (B2).

path, this arrangement allows us to optimize the buffers independently and reduce the power consumption by reducing the load on the main buffer.

The first stage sub-ADC (flash ADC) has sampling networks for its comparators that closely match that of the MDAC. This is needed because any mismatch in the sampling time or bandwidth between the MDAC and the comparators causes the input value sampled by the MDAC to be different from that sampled by the comparators. This leads to flash offset and gain errors that get worse with increasing the input frequency [1]. This error consumes a portion of the correction range of the first stage residue and can be corrected by the digital error correction only as long as the residue does not exceed the correction range [1]. The pipeline consists of 3 bits in the first stage, 4 bits in the second stage, followed by four stages with 3-bits/stage and a 3-bit back-end flash ADC. The input sampling capacitor is 6 pF in the first stage to achieve the noise target with a 2.5 Vp-p input span. The input buffer uses a 3 V supply, while the ADC core uses a 1.8 V supply.

To achieve the desired linearity, the capacitor mismatches of the first and second stages need to be calibrated. Since those are supply, temperature and sample rate independent, they can be factory calibrated. This is done by using digital coefficients in the digital correction logic that scale the different sub-ranges

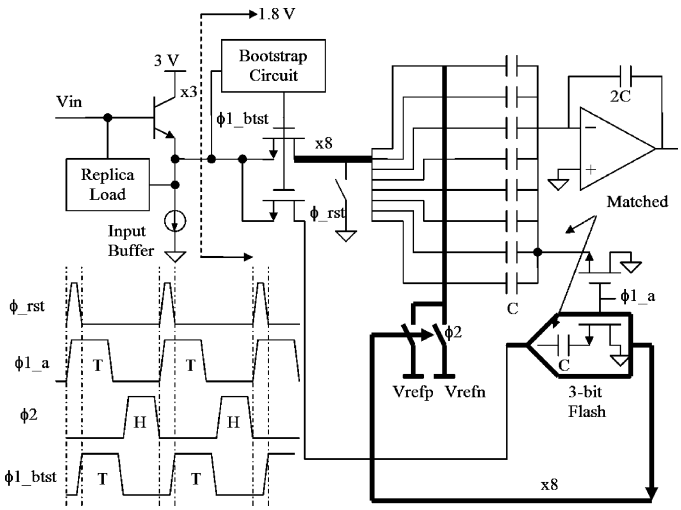


Fig. 3. The front-end of the ADC showing the input buffer, the first MDAC and the first flash. The timing diagram is also shown.

appropriately to correct for both the DAC and gain errors that are due to the capacitor mismatches.

A simplified schematic of the front-end and first stage is shown in Fig. 3. During the tracking/sampling phase, the input is sampled on the MDAC and the flash sampling capacitances. The sampling switches ($\phi 1\_a$) and the bootstrapped switch ($\phi 1\_btst$) are turned on. During the hold/gain phase, the flash comparators make their decisions and propagate them to the DAC switches, which connect the DAC capacitances to either Vrefp or Vrefn depending on the flash bits. In this design, the flash takes about 1 ns to make its decision. At 250 MS/s, this leaves about 1 ns for the RA output to settle to the needed accuracy. This large percentage of the hold/gain time taken up by the flash relative to the prior art [1], [2] stresses the first RA, whose output needs to settle in less than half the time compared to the following stages. The bandwidth required for this amplifier to achieve 16-bit performance is about 2 GHz. In addition, its open loop gain needs to be larger than 100 dB [1], [2].

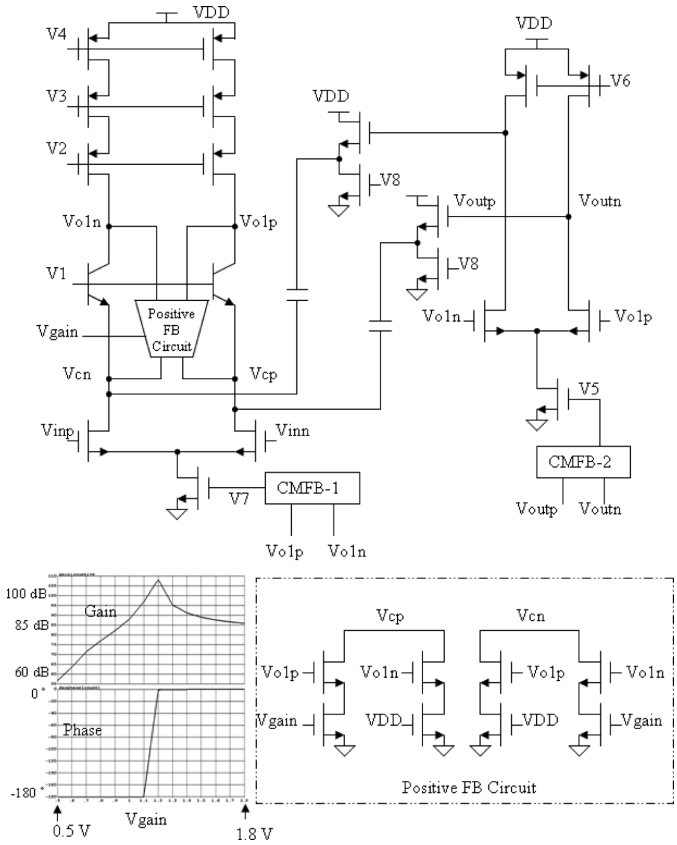


Fig. 4. The first stage residue amplifier. Also shown is the positive feedback circuit and a plot of the open loop gain and phase of the amplifier as a function of the voltage "Vgain."

This required high gain-bandwidth product leads to high power consumption. Relaxing some of these requirements would help reduce the power but causes inter-stage gain errors that tend to be temperature, supply and even sample-rate dependent.

The residue amplifier (RA) is shown in Fig. 4 and consists of two stages. The first stage is a cascode amplifier with double-cascoded PMOS and BJT-cascoded NMOS. The second stage is a simple differential pair. The compensation capacitances are connected through source followers between the outputs of the second stage and the emitters of the first stage cascode BJT [8]. This arrangement helps push the non-dominant pole frequency up to higher frequencies, while substantially increasing the frequency of the right-hand side zero that is normally introduced by the compensation capacitances.

A positive feedback circuit is connected between the outputs of the first stage and the cascode nodes. This circuit uses positive feedback, through cross-coupling, to create a negative trans-conductance (g_m) circuit in parallel with the main devices. This negative g_m substantially reduces the output conductance of the first stage and hence increases the output impedance and the gain. Such an effect is achieved by "tuning" the output impedance of the positive feedback circuit to closely match that of the first stage with an opposite sign. This is done by controlling the bias voltage "Vgain." Although the resulting gain can be as high as 110 dB as shown in Fig. 4, it depends strongly on the process, supply, temperature and operating point. The variation in those parameters can cause the gain to drop to as low as 85 dB in some conditions. Therefore, background calibration is employed to correct the resulting gain error. The correction is done either in the digital domain by adaptively multiplying the residue by a correction factor, or in the analog domain by adaptively controlling the voltage "Vgain." In the former case, where the correction is done in the digital domain, the positive feedback circuit would not be needed. This approach of relaxing the open loop gain allows us to lower the power consumption of the amplifier by about 40%.

During the gain phase, the sampling capacitors store a total charge that is proportional to the coarsely quantized value of the input sample (3-bits). This quantized signal is a highly non-linear version of the input signal. During the next tracking phase, this charge causes a non-linear "kick-back" on the input driver. In spite of the presence of the buffer, some of this kick-back propagates to the ADC driver and may degrade the linearity if it does not dissipate within the sampling time. To reduce this effect, a reset switch (ϕ_rst) is employed to briefly reset the capacitance after the gain phase and before the capacitance is connected to the input in the next sample phase.

III. The Input Buffer

Traditional buffers are usually implemented as emitter followers or source followers as shown in Fig. 5(a). These circuits have high input impedances and low output impedances, which enable them to isolate the ADC driver from the charge injection (kick-back) of the sampling capacitances and the input switch. In addition, the low output impedance reduces the distortion caused by the non-linearity in the load impedance and enables a large acquisition bandwidth that helps improve the sampling accuracy and linearity at high sample rates. An emitter-follower is substantially superior to a source follower due to the higher trans-conductance (g_m), higher output impedance and smaller parasitics of the BJT compared to an NMOS device.

One major source of non-linearity in an emitter- (or source-) follower is the current variation through the follower device Q1. This current variation is due to the signal current flowing through the sampling capacitance, which normally needs to be supplied by the device Q1. This variation causes the device parameters (such as its g_m) to be dependent on the input signal, which leads to distortion. This is shown in the buffer transfer function as follows:

$$\frac{V_o}{V_{in}} \cong \frac{1}{1+\dfrac{1}{g_m Z_L\left(1+\dfrac{1}{g_m Z_\pi}\right)}} \cong 1-\frac{1}{g_m Z_L} \tag{1}$$

where V_o is the buffer output voltage, V_{in} is the input voltage, g_m is the transconductance of the device Q1, Z_L is the load impedance and Z_π is the internal input impedance of the BJT device according to the π-model.

The non-linearity in the output voltage can be approximated as

$$\frac{\Delta V_o}{V_o} \cong \frac{\dfrac{\Delta g_m}{g_m}}{1+g_m Z_L}. \tag{2}$$

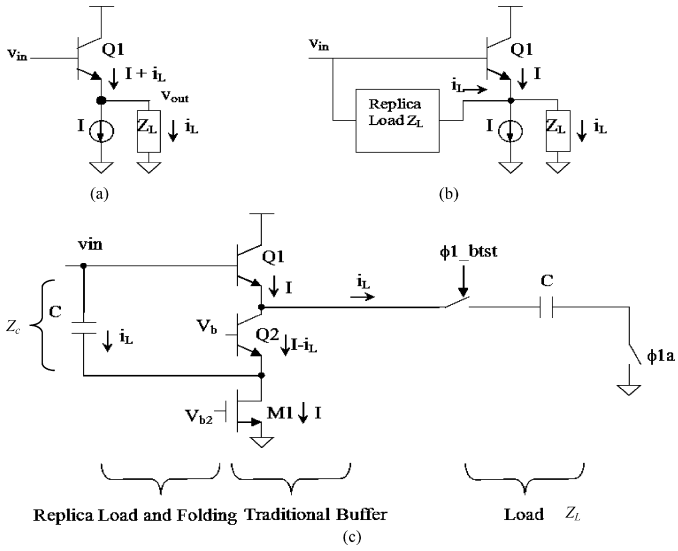


Fig. 5. (a) Traditional emitter-follower. (b) Simplified conceptual schematic of the linearization technique. (c) Simplified schematic of the emitter-follower used in this work.

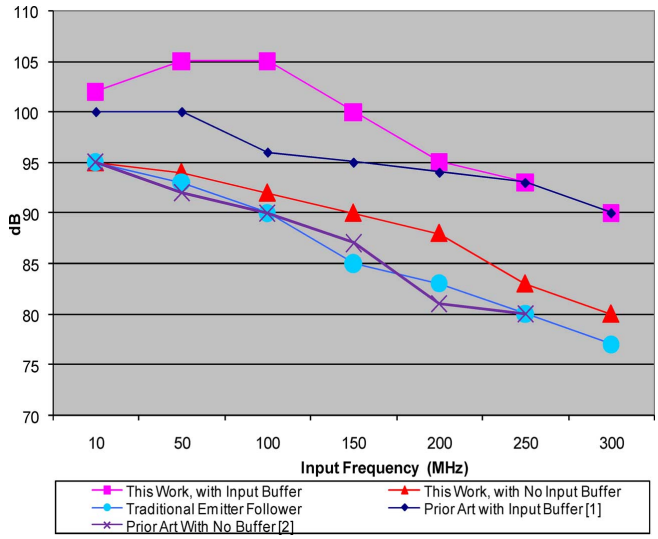


Fig. 6. The SFDR measured performance of this work compared to the state of the art under the same conditions at 125 MS/s.

It is clear from (2) that the non-linear term (g_m) causes a distortion in the transfer function because of its input dependence. The distortion is directly proportional to $\Delta gm/gm$, and inversely proportional to the load impedance Z_L and the trans-conductance g_m. That is, as the load impedance or the trans-conductance increases, the distortion improves.

Some linearization techniques have been implemented in the literature for various kinds of samplers [5]–[7]. However, the linearity previously achieved was in the order of 60–80 dB which is not adequate for this design. In addition, most of those techniques were for architectures that are not compatible with this design, such as bipolar samplers with common-emitter input buffers.

On the other hand, the traditional approach to improve the distortion in an emitter- (or source-) follower buffer has been to increase the dc (bias) current of Q1, so that the relative change in current, and hence $\Delta gm/gm$, is small enough to achieve the desired linearity. Unfortunately, this current increase dictates an increase in the size of the devices and possibly the supply voltage to accommodate the signal dynamic range. This in turn increases the device parasitics, which eventually limit the achievable linearity because some of those parasitics tend to be input dependent. In addition, this approach leads to high power consumption due to the large bias current and supply voltage [1].

To overcome these performance limitations and reduce the power consumption, we employ a buffer linearization technique that reduces the current variation in the follower device Q1 of the main input buffer (B1). This is shown conceptually in Fig. 5(b), where a replica load is used to inject a current into the output node of the follower that is almost equal to the current needed by the load. This reduces the current variation in the emitter-follower device Q1 and hence improves its linearity. It also alleviates the need for a high bias current and a large supply. The injection mechanism, shown in Fig. 5(c), utilizes the high trans-conductance of the cascode device Q2, which creates a virtual ground on the other terminal of the replica capacitor, to drive a current in it that is almost equal to the sampling current (i_L). The large output resistance of the MOS current source M1 will force most of this current to flow up into the output node, and hence keep the current in the device Q1 almost constant. This linearity improvement is shown analytically as follows:

$$\text{If} \quad \varepsilon = \frac{1}{g_m Z_\pi} \text{ and } \lambda = \frac{1}{g_{m2} Z_{\pi 2}} + \frac{1}{g_{m2} Z_c} \tag{3}$$

where Z_c is the impedance of the replica load (capacitance) connected between the input and the emitter node of device Q2. Then, the transfer function of the linearized buffer is given by

$$\frac{V_o}{V_{in}} = \frac{1 + \dfrac{1}{g_m Z_c} \dfrac{1}{(1+\varepsilon)} \dfrac{1}{(1+\lambda)}}{1 + \dfrac{1}{g_m Z_L (1+\varepsilon)}} \tag{4}$$

$$\text{If} \quad Z_L = Z_c(1+\lambda) \cong Z_c \tag{5}$$

$$\text{Then} : \frac{V_o}{V_{in}} \cong 1. \tag{6}$$

Therefore, the linearization technique practically eliminates the non-linearity of the buffer due to the current variation.

It is interesting to note that in addition to improving the distortion at the output of the buffer, this technique also improves the distortion at the input of the buffer. This is because the reduction in the current variation will reduce the variation of the buffer input impedance and hence improve the input linearity.

In addition, it is also important to note that this technique still requires the ADC driver to supply the current i_L originally needed by the sampling capacitor to the newly added compensation capacitance. Therefore, this buffer is different from a traditional buffer in that it does not increase the overall input impedance of the ADC. It, however, makes the input impedance much more linear and static (i.e., not switched). The main problem from the distortion standpoint is not the linear current required by the sampling network, but rather the non-linear current drawn by the non-linear impedance in that

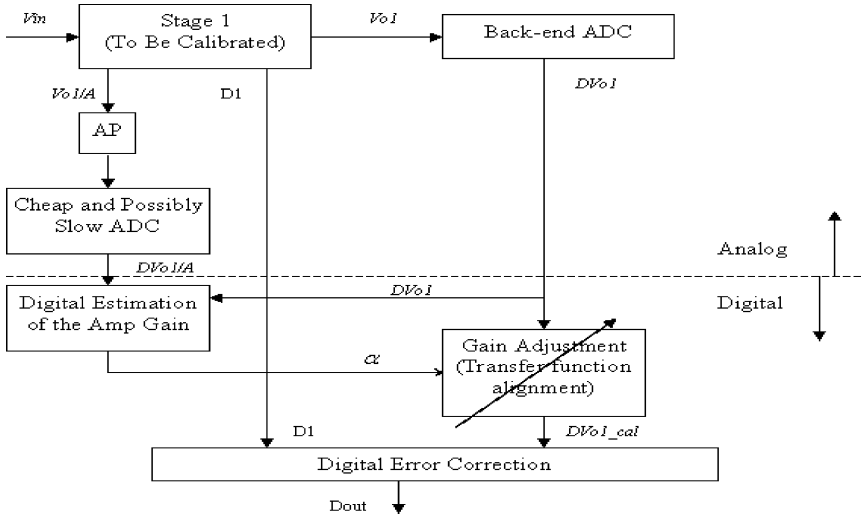


Fig. 7. A block diagram illustrating the summing node sampling (SNS) background calibration algorithm with digital estimation and digital correction of the inter-stage gain error of stage-1 amplifier. The summing node voltage is sampled, amplified and digitized using a slow analog processor. The algorithm estimates the open loop gain of the amplifier and its inverse α. This is used to correct the residue voltage (DV_{o1_cal}).

network. This non-linear impedance is due to the non-linear parasitic capacitances and resistances in the input switch and other devices connected to the input path. The new buffer effectively isolates the input from this non-linear impedance and provides a low output impedance to drive it with reduced distortion. On the other hand, the newly added compensation capacitance at the input of the buffer is not switched and is quite linear. Hence, it is a relatively benign load and requires a much more linear current from the driver. So the buffer effectively replaces a non-linear and switched load on the ADC driver with a linear and un-switched one. However, if driving this compensation capacitance is undesirable, an auxiliary buffer can be added in the compensation path to drive this capacitance and remove the need for the driver to supply the current i_L. This, however, was not needed in our design.

Silicon results show the superior performance of this buffer compared to the prior art, while reducing the power consumption by 50–70% relative to the state of the art [1]. This is shown in Fig. 6, where the SFDR is plotted versus input frequency for the new linearized buffer, a traditional buffer and the double buffer used in [1]. We can clearly see the advantage of the linearized buffer compared to traditional buffers. The performance of the un-buffered ADC is also shown for this work and for the prior art [2]. It is interesting to see that although the SFDR of the current work without the buffer is better than the prior art, it is still substantially worse than the SFDR with the buffer. This illustrates the need for the input buffer to achieve this level of linearity.

IV. Background Calibration

To correct the inter-stage gain error caused by the relaxed design of the first stage residue amplifier, we employed a new background calibration algorithm that focuses on the amplifier gain error and helps reduce the power consumption in the first stage by about 50%. This Summing Node Sampling (SNS) algorithm utilizes the fact that the amplifier open loop gain can be estimated using its output (i.e., the residue voltage) and the summing node voltage. The summing node voltage is sampled and processed at a sample rate that can be substantially lower than the ADC sample rate, together with the corresponding stage-1 residue sample, to statistically estimate the RA's open loop gain.

In this work, the summing node voltage is amplified by a gain of 64 and digitized using an on-chip low-resolution (13-bit), low-power (10 mW) and low-speed (1/20th the speed of the main ADC) auxiliary ADC. The first stage residue voltage is digitized using the following stages of the main pipeline. The digital values of both voltages are high-pass filtered to remove the offset and processed using the Least-Mean-Square (LMS) algorithm to filter the noise and statistically estimate the RA open loop gain, or more accurately its inverse $\alpha = 1/A$. After estimating the gain digitally, the correction is applied in one of two ways:

A. Digital Correction

This is shown in Fig. 7, where the gain estimate is used to correct the gain error in the digital domain in a feed-forward fashion by multiplying the residue by a correction factor. The LMS algorithm is used to iteratively estimate the value of α that minimizes the squared error

$$\begin{aligned}\varepsilon &= \left[D\left(\frac{V_{o1}}{A}\right)_{\text{\_estimated}} - D\left(\frac{V_{o1}}{A}\right)_{\text{\_measured}}\right]^2 \\ &= \left[\alpha D(V_{o1}) - D\left(\frac{V_{o1}}{A}\right)\right]^2 \end{aligned} \tag{7}$$

as follows:

$$\begin{aligned}\alpha_{i+1} &= \alpha_i - \mu D(V_{o1i})\left[\alpha_i D(V_{o1i}) - D\left(\frac{V_{o1i}}{A}\right)\right] \text{ and} \\ \alpha_{i+1} &= \alpha_i - \mu D(V_{o1i})[\alpha_i D(V_{o1i}) - D(V_{e1i})] \end{aligned} \tag{8}$$

where α_i is the i^{th} iteration of α, $D(x)$ is the digital value of x, μ is the algorithm step size, V_{o1} is the first stage residue and $V_{e1} = V_{o1}/A$ is the first stage summing node voltage.

The correction is then applied in the digital domain using the formula

$$V_{o1\_cal} = V_{o1}(1 + K\alpha). \tag{9}$$

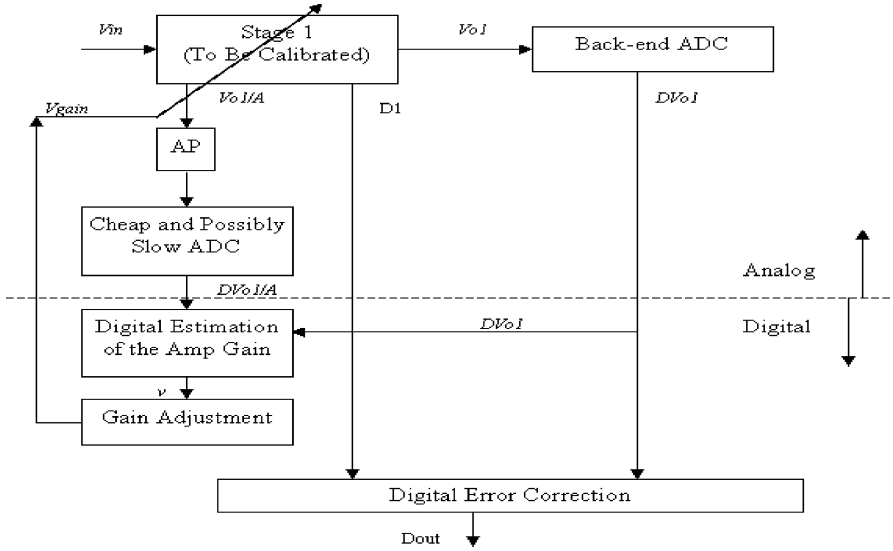


Fig. 8. A block diagram illustrating the SNS background calibration algorithm with digital estimation and analog correction of the inter-stage gain error of stage-1 amplifier. algorithm maximizes the open loop gain of the amplifier and minimizes its inverse α by generating a control parameter ν, which is fed-back to control the voltage "$\mathrm{V}\mathrm{gain}$" of the positive feedback circuit in the residue amplifier of Fig. 4.

B. Analog Correction

This is shown in Fig. 8, where the gain estimate is used to maximize the open loop gain of the amplifier in the analog domain using the control voltage $\mathrm{V}\mathrm{gain}$ in the positive feedback circuit described in Section II. The background calibration forms a feedback loop that controls that voltage in order to keep the amplifier working in the maximum gain spot regardless of changes in supply, temperature, and process. This is a statistical "minimization" problem (as opposed to an "estimation" one), where the LMS algorithm works on minimizing the estimate of α. This substantially simplifies the problem and makes it immune to gain errors in the slow path. This LMS algorithm is shown as follows:

$$\begin{aligned}\nu_{i+1} &= \nu_i - \mu D(V_{o1i}) D\left(\frac{V_{o1i}}{A}\right) \quad \text{and} \\ \nu_{i+1} &= \nu_i - \mu D(V_{o1i}) D(V_{e1i}).\end{aligned} \tag{10}$$

The number of samples needed for the algorithm to converge depends on the required accuracy, the noise in the calibration (slow) path, and the amplitude of the residue voltage. It can be shown that the number of samples needed for convergence is given by

$$N \approx \left(\frac{V_{Noise\_calpath}}{\frac{V_{o1RMS}}{A_{needed}}}\right)^2 = 10^{[(A_{needed\_\mathrm{dB}} - SNR_{calpath} - V_{o\_\mathrm{dB}})/10]} \tag{11}$$

where A_{needed} is the needed gain in the RA to achieve the desired performance. To converge to 16-bit accuracy (i.e., $A_{needed} = 110$ dB) with a full-scale input signal and an SNR in the calibration path of 67 dB, the algorithm needs about 40,000 samples. Since the slow path is designed to be 1/20th the speed of the main pipeline, at 250 MS/s the slow path works at 12.5 MS/s. Therefore, 40,000 samples translate into less than 10 ms of convergence time, which is about 100 times faster than the state-of-art correlation-based approaches [9], [10].

Moreover, unlike correlation-based algorithms, the SNS algorithm does not use any portion of the MDAC correction range, which eliminates the large analog power overhead of the correlation-based approaches, which can be as high as 50% of the first stage power. Its digital power is also substantially lower than correlation-based techniques, by a factor of 20, because of the lower clock rate used in this algorithm's digital block. The transistor count of the digital implementation however is comparable because the core processing is similar.

In addition, since we measure the summing node voltage and use it to estimate the open loop gain directly instead of the closed loop gain error, it can be shown analytically that the needed accuracy of the gain estimate is relaxed by the actual open loop gain of the amplifier. This is shown as follows:

Since from (9)

$$V_{o\_cal} = V_o\left(1 + \frac{K}{A_{est}}\right).$$

Then

$$\partial V_o = V_o\frac{K}{A_{est}} - V_o\frac{K}{A_{act}}$$

and

$$\left|\frac{\partial V_o}{V_o}\right| = \frac{K}{A_{act}}\left|\frac{\partial A_{est}}{A_{est}}\right| \tag{12}$$

where V_o is the residue voltage, A_{est} is the estimated open loop gain, A_{act} is the actual open loop gain and K is the inverse of the feedback factor. For example, to achieve 16-bit accuracy using an RA with an open loop gain of 80 dB, the gain estimate needs to be only 5-bit accurate, while correcting a 60 dB RA requires a 9-bit accurate estimate. This relaxed accuracy requirement allows the use of low accuracy circuits to process the summing node voltage.

It is important to note that this algorithm does not depend on the input signal's exact shape or statistics. However, for the

TABLE I
A COMPARISONOF THE MEASURED ADC PERFORMANCE WITH FIXED FACTORY CALIBRATION ONLY (i.e., WITHOUT BACKGROUND CALIBRATION) COMPARED TO USING BACKGROUND CALIBRATION. SINCE FACTORY CALIBRATION IS PERFORMED AT ROOM TEMPERATURE TO REMOVE ALL SOURCES OF INTER-STAGE GAIN ERROR IN THIS TEST, THE PERFORMANCE IS SIMILAR TO USING BACKGROUND CALIBRATION IN THAT CONDITION. HOWEVER, THAT FIXED CALIBRATION DOES NOT HOLD AS CONDITIONS (SUCH AS TEMPERATURE) CHANGE, AS CAN BE SEEN IN THE TABLE

Temperature	Parameter	Without Background Calibration	With Background Calibration
27°C	SNR	76.5 dB	76.5 dB
	SFDR	100+ dB	100+ dB
85°C	SNR	75.5 dB	76.7 dB
	SFDR	90 dB	99 dB
-40°C	SNR	74.3 dB	76.2 dB
	SFDR	86 dB	98 dB

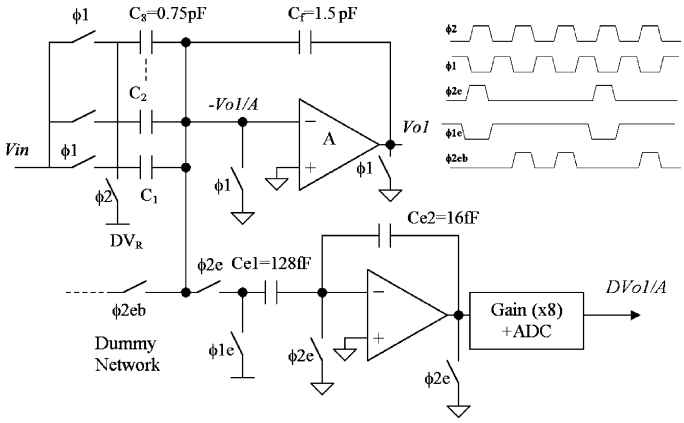


Fig. 9. A schematic of the implementation of the summing node voltage sampling for the SNS algorithm. Also shown is the dummy network used to minimize the effect of the slow clock on the main path.

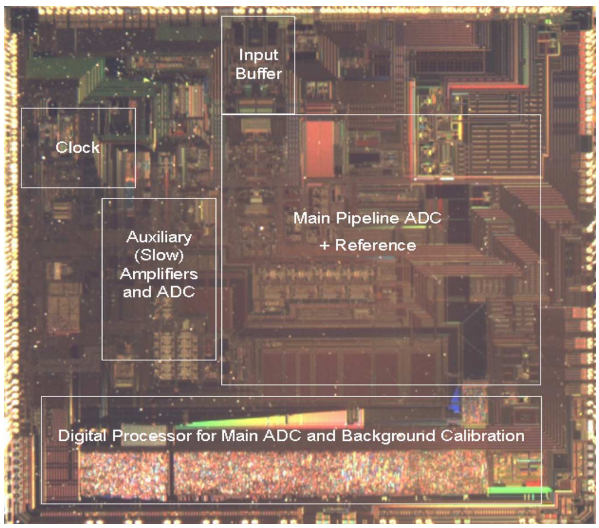


Fig. 10. Die micrograph.

samples to be useful to the algorithm, the input signal needs to be variable (not DC), because the DC component is filtered out by the algorithm, and its amplitude needs to be above a certain threshold that is determined by the chosen value of the step size μ and the desired convergence time. If this condition is not satisfied, the corresponding samples are thrown out and the algorithm is frozen for that sample. In addition, although this algorithm is used in this work to correct for linear gain errors, it can be extended to correct for gain non-linearity as well. This discussion however is beyond the scope of this paper.

The circuit implementation of the calibration technique is shown in Fig. 9. The summing node voltage ($V_{e1} = V_{o1}/A$) is sampled on the capacitance C_{e1} whose value is chosen to be small enough to have negligible impact on the MDAC feedback factor, but large enough to have a reasonable SNR in the slow path to achieve the desired convergence time. The sampled voltage V_{e1} is then amplified by a factor of 64, and digitized using the slow ADC. Given the gain of 64, the resolution of the slow ADC needs to be 12 bits in order to achieve an input-referred 18-bit resolution. We chose to implement the slow ADC as a pipeline with 13-bit resolution.

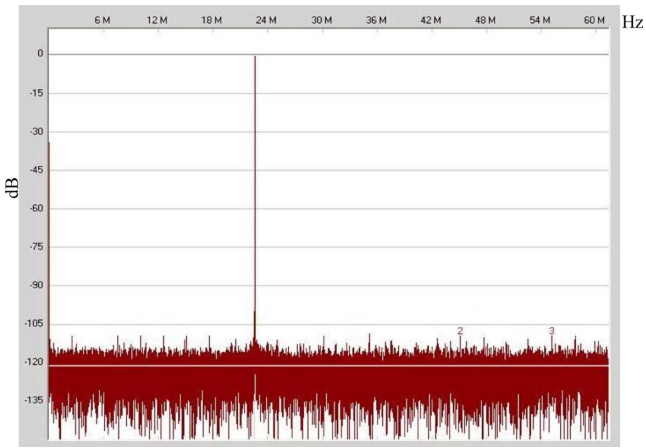


Fig. 11. An FFT of the ADC output at 125 MS/s for an input frequency of 100 MHz at −1 dBFS. The SNDR is 76.5 dB and the SFDR is 110 dB.

In order to reduce the impact of the slow clock on the summing node of the main ADC, a dummy network is connected

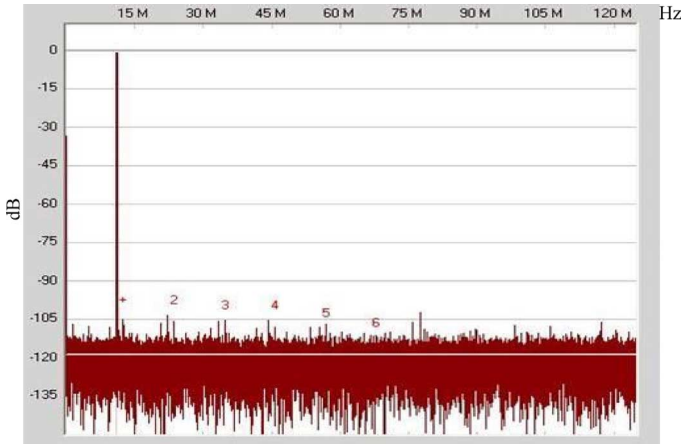


Fig. 12. An FFT of the ADC output at 250 MS/s for an input frequency of 10 MHz at -1 dBFS. The SNDR is 76.5 dB and the SFDR is 98 dB.

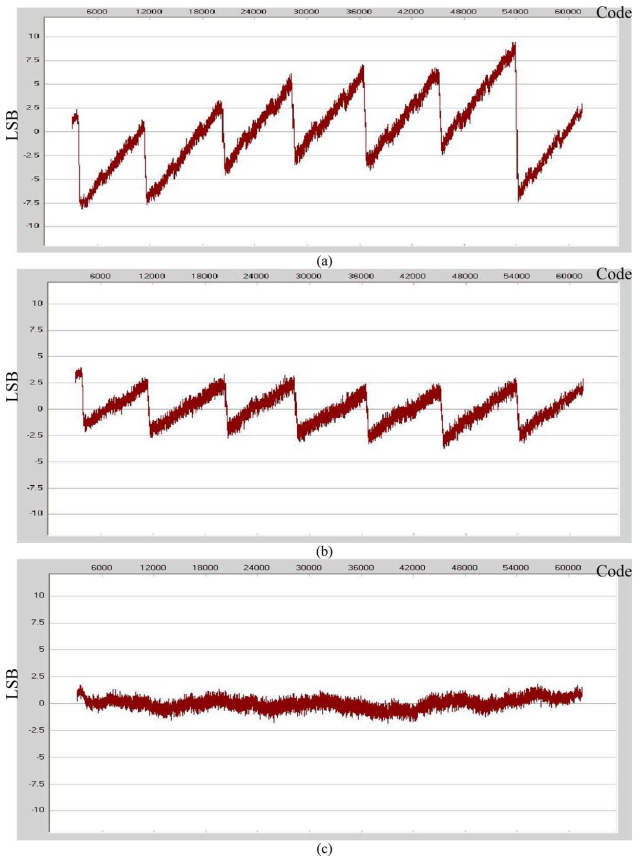


Fig. 13. Integral non-linearity (INL) plots for: (a) no calibration; (b) with capacitance calibration but no background calibration; (c) with capacitance and background calibration.

in parallel using the clock $\phi 2\mathrm{eb}$. This network, shown in Fig. 9, samples the summing node voltage every cycle of the main clock except the one where the slow network samples the summing node. This way the two networks complement each other and provide a constant load on the summing node at every clock. This reduces the spurs that could result from the slow clock. In addition, a clock spreading technique is used to randomize the slow clock edge in order to distribute the energy of any remaining spurs in the noise floor. Silicon results indicate a spur level of better than 105 dB without spreading and better than 120 dB with spreading.

The calibration algorithm is implemented with all the digital processing needed for the calibration on chip. Both the digital and analog correction techniques mentioned above are implemented and verified on silicon with comparable effectiveness. Although only one of the two techniques is usually needed, there was no harm in running them simultaneously. The calibration improved the SNDR by 5 dB and the SFDR by 10 dB. The calibration also preserved the performance with temperature variation, regardless of the initial gain value on the curve of Fig. 4. The measured results are summarized in Table I.

V. ADC Performance Summary

The ADC is fabricated on a 0.18 μm BiCMOS process with five metal layers. The die size is 50 mm^2 and a die micrograph is shown in Fig. 10. When the input buffer is bypassed, the SNR is 77.8 dB and the SFDR is 90 dB at 10 MHz input frequency. With the input buffer, the SNR is 76.5 dB and the SFDR is greater than 95 dB. The SNR numbers capture all of the noise sources in the signal and clock paths including the off-chip termination resistors. The ADC consumes 850 mW from a 1.8 V supply, and the input buffer consumes 150 mW from a 3 V supply. The input span is 2.5 Vp-p and the jitter is 60 fs.

Example FFT plots are shown in Figs. 11 and 12 and the INL plots are shown in Fig. 13. A plot of the SFDR and SNR versus input frequency is shown in Fig. 14 at 250 MS/s, together with a summary of the various performance parameters. On the other hand, in Fig. 6, the SFDR is shown versus input frequency at 125 MS/s.

To evaluate the power efficiency of this ADC, we use the figure-of-merit given in [14] by

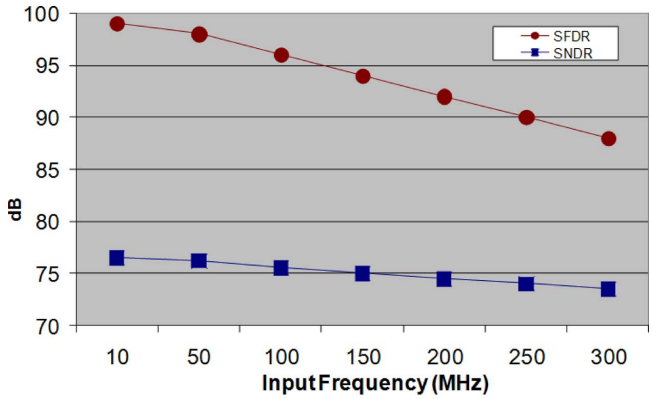
$$\mathrm{FOM} = \mathrm{SNDR} + 10\log\left(\frac{\mathrm{BW}}{\mathrm{Power}}\right). \tag{13}$$

Although it has serious limitations and does not capture all the design parameters of the ADC (such as the SFDR and IF sampling), this FOM captures accurately the trade-offs involving power, noise and sample rate. Applying this formula to the current work, with the BW equal to the Nyquist frequency, yields an FOM of 158.7 dB without the buffer and 157 dB with the buffer. This compares favorably with the state of the art [15]–[20] as shown in Fig. 15.

It is interesting to note the impact of the input buffer on the power efficiency of the ADC from the SNDR and bandwidth perspective as expressed by the FOM. The buffer degrades the FOM by about 1.7 dB. This translates into about 48% more power for a buffered ADC to achieve the same SNDR and sample rate as an un-buffered ADC. This, however, is the price of the superior linearity that is achieved by the buffer, which is usually not captured in the FOM calculations.

VI. Conclusion

In this paper, we present a 16-bit 250 MS/s pipelined ADC. It employs an input buffer linearization technique that enables an SFDR performance that is 5–10 dB better than the state of the art, while reducing the power consumption by 50%-70%. It also employs the summing node sampling (SNS) background



	With No Input Buffer	With Input Buffer
Power	850 mW	1 W
SNDR (10 MHz)	77.8 dB	76.5 dB
SFDR (10 MHz)	90 dB	98 dB
INL	3 LSB	3 LSB
DNL	0.5 LSB	0.5 LSB
Supply	1.8V	1.8V/3.0V

Fig. 14. Summary of the measured ADC performance at 250 MS/s.

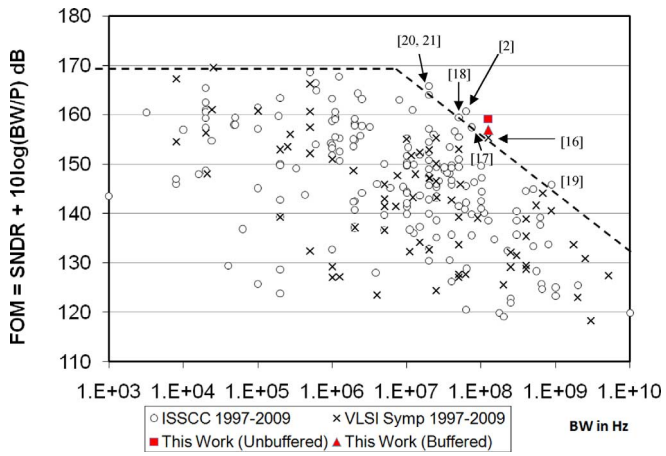


Fig. 15. Figure-of-merit of this work compared to the state of the art. The plots show the FOM versus input bandwidth from [10].

calibration algorithm that helps improve the performance and reduce the power consumption of the first stage residue amplifier. We demonstrated the viability of the background calibration algorithm, and presented the silicon performance of the whole ADC with and without the input buffer.

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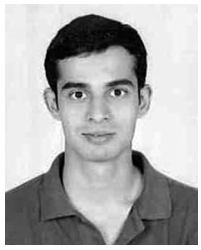

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