# Improved Reversed Nested Miller Frequency Compensation Technique With Voltage Buffer and Resistor

Alfio Dario Grasso, *Member, IEEE*, Davide Marano, Gaetano Palumbo, *Fellow, IEEE*, and Salvatore Pennisi, *Senior Member, IEEE*

***Abstract*—This brief introduces and develops a novel frequency compensation technique for three-stage operational transconductance amplifiers. The new compensation topology exploits a voltage buffer and a nulling resistor to achieve a double pole–zero cancellation, occurring beyond the gain-bandwidth product. To verify the effectiveness of the compensation scheme, an amplifier has been fabricated in a standard 0.5-$\mu$m CMOS process. Experimental measurements are found to be in good agreement with the theoretical analysis and show an improvement in small-signal and large-signal performances.**

***Index Terms*—Frequency compensation, operational transconductance amplifier (OTA), reversed nested Miller (RNM).**

## I. Introduction

THE operational transconductance amplifier (OTA) is a basic building block in most analog and mixed-signal electronic systems. An increasing number of applications requires high-gain high-bandwidth amplifiers which are able to drive large capacitive loads under low-voltage supply conditions. As the supply voltage continues to scale down, traditional cascode topologies are no longer suitable for achieving high dc gains, since they cause a significant reduction of the signal voltage swing. In order to avoid cascoding stages, dc gains in excess of 100 dB are achieved by cascading three or more simple transconductance gain stages. However, this approach causes a bandwidth reduction, since each stage inevitably introduces low-frequency poles which require additional compensation capacitors to provide adequate closed-loop stability.

At this purpose, compensation of three stage amplifiers, where the second stage is the only noninverting one, is traditionally obtained through the nested Miller compensation (NMC) technique [1]–[5]. This approach employs two compensation capacitors which exploit the Miller effect to split the low-frequency poles and achieve the desired phase margin and transient response. However, this solution results in a bandwidth and slew rate reduction (the gain-bandwidth product is proved to be one-quarter compared to that achievable by a single stage amplifier, [6]) and in a high power consumption as well. Recently, different compensation topologies have been proposed in order to overcome the inherent limits of NMC [6]–[13],

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The authors are with the Dipartimento di Ingegneria Elettrica, Elettronica e dei Sistemi Elettrotecnica (DIEES), Università di Catania, Catania, Italy (e-mail: gpalumbo@diees.unict.it).

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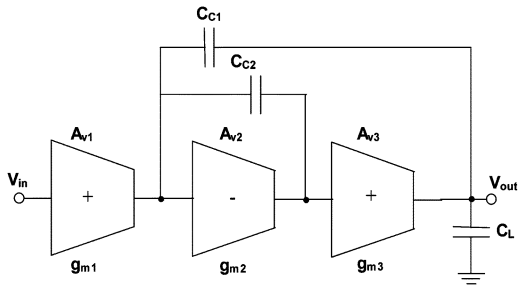


Fig. 1. Block diagram of the basic RNMC.

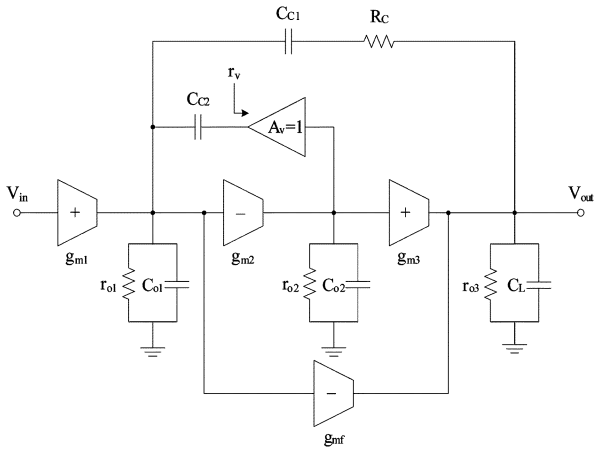


Fig. 2. Block diagram of the proposed compensation technique.

especially for heavy capacitive loads [14]–[17]. Indeed, many applications require high-gain OTAs driving on-chip loads in the order of hundreds of picofarads in battery-powered equipments, such as high accuracy $\Sigma\Delta$ modulators, flash and pipeline analog-to-digital converters, linear regulators, thin-film transistor (TFT) display drivers.

When the inner OTA stage is the only inverting one, another kind of compensation scheme, termed the reversed NMC (RNMC), is the most suitable option [4], [5], [18]–[22]. This technique exploits the same operating principle of the NMC but provides an inherent bandwidth improvement since, as shown in Fig. 1, the inner compensation capacitor does not load the output node [4], [20].

In this brief, we shall discuss a simple and high-performance compensation strategy, namely the RNMC with voltage buffer and outer resistor (RNMC-VB-OR). This new compensation

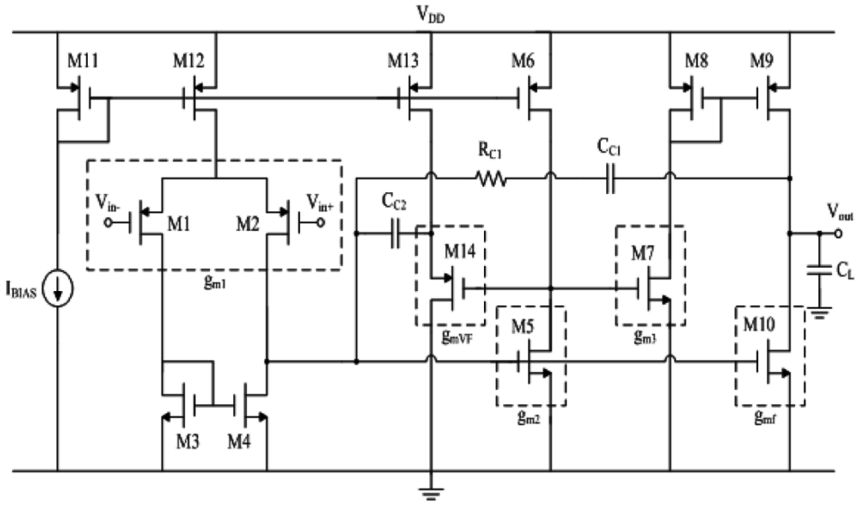


Fig. 3. Schematic of the implemented three-stage amplifier.

scheme improves the basic topology proposed in [18] by introducing an additional resistor in the compensation network. Unlike the technique proposed in [19], the resistor is connected in the outer compensation branch, and an additional feedforward stage enhancing large-signal performance is also used.

This brief is organized as follows. Analysis and design equations of the proposed technique are presented in Section II. The circuit implementation and some experimental results along with a performance comparison with other previously reported compensation schemes are exposed in Section III. Finally, the authors' conclusions and some remarks are given in Section IV.

## II. Compensation Technique

The block diagram of a three-stage amplifier exploiting the proposed technique is illustrated in Fig. 2, where parameters $g_{mi}$, $r_{oi}$, and $C_{oi}$ represent the $i$th stage transconductance, resistance and equivalent output capacitance, respectively, whereas $C_L$ is the load capacitance. The compensation network includes the two Miller capacitors $C_{C1}$ and $C_{C2}$, the feedforward stage $g_{mf}$, resistor $R_C$, and the voltage buffer $A_V$, whose output resistance is $r_V$. It is worth noting that the proposed approach employs the voltage buffer in the inner compensation loop, thus preserving the output swing [5].

It should be also noted that the additional feedforward stage $g_{mf}$ has been introduced to realize a push-pull pseudo class AB output stage, as will be clarified in the transistor level scheme of Fig. 3. However, it only affects large-signal performance and does not alter the small-signal open-loop transfer function.

The analysis starts from the evaluation of the open loop transfer function of the amplifier. In order to simplify its expression while maintaining accuracy, in the following the transfer function will be carried out assuming that the dc gain of each stage $A_{Vi} = g_{mi}\, r_{oi}$ is much greater than unity, and that $C_L, C_{C1}, C_{C2} \gg C_{oi}$. Therefore, small-signal symbolic analysis yields (1), shown at the bottom of the page, where $w_{p1} \approx 1/(r_{o1}g_{m2}r_{o2}g_{m3}r_{o3}C_{C1})$ represents the dominant pole and $A_0 = g_{m1}r_{o1}g_{m2}r_{o2}g_{m3}r_{o3}$ the dc voltage gain. Consequently, the gain-bandwidth product is, as usual, $\omega_{\mathrm{GBW}} = g_{m1}/C_{C1}$. The transfer function (1) also exhibits two high-frequency intermediate poles, a very high-frequency pole due to parasitics at the output of the second stage and two zeros that can be both allocated in the left-half plane (LHP) by means of a suitable choice of the compensation network components. In particular, the values of both LHP-zeros can be adjusted to exactly match the two intermediate poles. Equating the coefficients of the second-order polynomials, $r_V$ and $R_C$ can be derived as

$$\begin{cases} r_v = \frac{1}{g_{m3}} \frac{C_L}{C_{C1}} \\ R_C = \frac{1}{g_{m3}} \frac{C_{C2}}{C_{C1}} \left(1 + \frac{C_L}{C_{C1}}\right). \end{cases} \tag{2}$$

After the double pole–zero cancellation, (1) reduces to a single pole transfer function and the phase margin, neglecting the effect of the parasitic pole, is almost equal to 90°. Note that (2) requires a matching between a resistance and two transconductance values, thus process variations may lead to incomplete elimination of the poles and zeros. The presence of pole–zero doublets in the open-loop gain of real amplifiers could seriously degrade their performance or even cause stability problems [23]. Nevertheless, if the poles and zeros forming the doublets are sufficiently close each other and lie beyond the unity-gain frequency of the amplifier, such pole–zero cancellations negligibly modify the expression of the closed-loop amplifier bandwidth and do not appreciably change the phase margin [24]. Furthermore, it is worth noting that both

$$A(s) \cong A_0 \frac{1 + (R_C C_{C1} + r_v C_{C2})\, s + r_v R_C C_{C1} C_{C2} s^2}{\left(1 + \frac{s}{w_{p1}}\right)\left[1 + \frac{C_{C2}}{g_{m3} C_{C1}} \left[C_L + C_{C1}\left(1 + g_{m3} r_v\right)\right] s + \frac{R_C C_{C2} C_L}{g_{m3}} s^2\right]\left[1 + \frac{C_{o2}(r_v + R_C)}{g_{m2} R_C} s\right]} \tag{1}$$

poles (and zeros) are real for typical parameter values, and hence the pole–zero cancellations are less sensitive to process variations and mismatches.

Examining the $s$-coefficients of the second-order polynomial in the numerator of the open-loop gain transfer function in (1) it can be easily shown that

$$(r_v C_{C2} + R_C C_{C1})^2 \gg r_v R_C C_{C1} C_{C2} \tag{3}$$

which implies that the poles and zeros involved in the two pole–zero cancellations are always real for any value of $r_V$ and $R_C$. Furthermore, the first pole–zero doublet is positioned at a much lower frequency than the other one. Hence, imposing the first dominant pole–zero doublet to be placed beyond the unity-gain frequency of the open-loop amplifier gain (i.e., $p_1, z_1 > \omega_{\mathrm{GBW}}$), yields the following condition:

$$\frac{1}{r_v C_{C2} + R_C C_{C1}} > \frac{g_{m1}}{C_{C1}}. \tag{4}$$

Substituting the expressions of $r_V$ and $R_C$ given in (2) into relationship (4), we find a limit value of the Miller capacitor $C_{C1}$ which can be written as

$$C_{C1} > \frac{g_{m1}}{2g_{m3}} C_{C2} \left[ 1 + \sqrt{1 + \frac{8g_{m3}}{g_{m1}} \left( \frac{C_L}{C_{C2}} \right)} \right] \cong \sqrt{2 \frac{g_{m1}}{g_{m3}} C_{C2} C_L} \tag{5}$$

where the rightmost approximation holds for high values of the ratio $C_L/C_{C2}$. Note that this condition can always be met since it is convenient to use low values of $C_{C2}$, as can be easily seen from (2)–(5). Equation (5) implies also an upper limit to the maximum achievable gain–bandwidth product.

## III. Experimental Results and Performance Comparison

To prove the effectiveness of the proposed compensation technique and show its advantage over other previously reported solutions, we fabricated an OTA in a standard 0.5-$\mu$m CMOS (AMI-MOSIS) process. The amplifier was designed to drive a load of 500 pF with a 3-V supply voltage.

The simplified schematic of the implemented three-stage amplifier is shown in Fig. 3. The first stage is made up of a pMOS differential pair (M1-M2) with a current mirror load (M3-M4). The second inverting stage is realized by common source M6-M5, while the last noninverting stage is implemented through transistors M7-M10. The additional feedforward stage $g_{mf}$ in Fig. 2 is implemented by exploiting the active load transistor M10 in the last stage, whose gate is connected to the output of the first stage. Thanks to this connection, transistors M9-M10 act as a pseudo class AB output stage, which is able to drive the load capacitor $C_L$ with a current much higher than the output branch quiescent current. As a result, the amplifier slew rate is determined by the maximum available current from the first stage (charging $C_{C1}$ and $C_{C2}$).

As already mentioned, the presence of the additional feedforward stage $g_{mf}$ does not appreciably modify the location of the poles and zeros in the transfer function (1). Therefore, the value of $g_{mf}$ can be almost freely chosen. Among the possible alternatives, we choose to set $g_{mf} = g_{m3}$ in order to obtain a symmetrical push-pull output stage.

TABLE I
Transistors Dimensions

| Transistor | Aspect ratio |
|---|---|
| M6, M8, M9, M12 | 4x(30/1.8) |
| M1, M2 | 18/0.6 |
| M3, M4 | 30/0.6 |
| M5, M7, M10 | 2x(30/0.6) |
| M11 | 2x(30/1.8) |
| M13 | 15/1.8 |
| M14 | 1.5/1.8 |

TABLE II
OTA Main Performance Parameters

| | |
|---|---|
| Technology | 0.5 μm CMOS |
| Power Supply (V) | 3 |
| Loading Capacitance (pF) | 500 |
| Area (mm$^2$) | 0.025 |
| Total Bias Current (μA) | 88 |
| Input Offset Voltage (mV) | 7.3 |
| Input White Noise (nV/ $\sqrt{\text{Hz}}$ )† | 22 |
| DC Gain (dB)† | 109 |
| Gain-bandwidth Product (MHz) | 2.87 |
| Phase Margin (deg) | 65° |
| CMRR @ DC (dB) † | 80 |
| PSRR @ DC (dB) † | 77 |
| Positive/Negative Slew Rate (V/μs) †† | 1.6 / -1.5 |
| Positive/Negative Settling Time at 1% (ns ) †† | 680 / 890 |
| HD2/HD3 @ 100 kHz, 100 mVpp (dB) †† | -59 / -54 |
| HD2/HD3 @ 100 kHz, 500 mVpp (dB) †† | -55 / -52 |

† post layout simulation
†† in unity gain configuration

Finally, the voltage buffer is implemented by common drain M13-M14. Therefore, the output resistance $r_V$ is almost equal to $1/g_{mVF}$.

To achieve the target gain-bandwidth product of 2 MHz, we set $g_{m1} = 140$ $\mu$A/V and $C_{C1} = 11$ pF. Subsequently, setting $g_{m2} = g_{m3} = g_{mf} = 500$ $\mu$A/V and $C_{C2} = 0.3$ pF, using (2) we find $R_C = 2.56$ k$\Omega$ and $r_V = 90.1$ k$\Omega$ (i.e., $g_{mVF} = 11$ $\mu$A/V). These values satisfy (5), which assures the pole–zero cancellations to take place beyond the gain-bandwidth product. The drain current of M1-M2 is set equal to 10 $\mu$A, the drain current of the second and last stage is 20 $\mu$A, while the current of the common drain stage is 2.5 $\mu$A, thus achieving a total current consumption of 82.5 $\mu$A (plus other 10 $\mu$A required by the biasing network). During the simulation step, $C_{C1}$ and $R_C$ have been slightly tuned to 10 pF and 3 k$\Omega$, respectively, obtaining a phase margin of about 70°.

Transistors dimensions are reported in Table I. Fig. 4 shows the simulated post-layout open-loop frequency response of the amplifier. The dc gain was equal to 109 dB, the gain-bandwidth product was 2.5 MHz with a phase margin of 68°.

Fig. 5 shows a microphotograph of the fabricated chip. The implemented amplifiers were experimentally tested for both dc and ac specifications. Fig. 6 shows the step response in unity-gain configuration to a 200-kHz 500-$\mathrm{mV}_{pp}$ input step. The measured results are summarized in Table II. To measure the gain-bandwidth product and the phase margin we used the indirect method proposed in [25] which allows us to determine the open-loop parameters of an amplifier by measuring its closed-loop 3-dB cutoff frequency and the corresponding phase.

TABLE III
PERFORMANCE COMPARISON OF DIFFERENT MULTISTAGE AMPLIFIERS

| | $C_L$ (pF) | $V_{DD}$ (V) | $I_{TOT}$ (mA) | *Power* (mW) | *GBW* (MHz) | *SR*[a] (V/μs) | *Comp. Capacitors* (pF) | $FOM_S$ (MHz·pF)/mW | $FOM_L$ (V/μs·pF/mW) | $IFOM_S$ (MHz·pF/mA) | $IFOM_L$ (V/μs·pF/mA) |
|---|---|---|---|---|---|---|---|---|---|---|---|
| MNMC [8] | 100 | 8 | 9.5 | 76 | 100 | 35 | $C_{C1}$= - $C_{C2}$= - | 132 | 46 | 1053 | 368 |
| NGCC [9] | 20 | 2 | 0.34 | 0.68 | 0.61 | 2.5 | $C_{C1}$= - $C_{C2}$= - | 18 | 74 | 36 | 148 |
| NMCFNR[10] | 100 | 2 | 0.2 | 0.406 | 1.8 | 0.79 | $C_{C1}$=30 $C_{C2}$=5.3 | 443 | 195 | 886 | 390 |
| DFCFC [11] | 1000 | 2 | 0.2 | 0.426 | 1 | 0.36 | $C_{C1}$=55 $C_{C2}$=3 | 2347 | 845 | 4694 | 1690 |
| AFFC [13] | 100 | 1.5 | 0.17 | 0.25 | 5.5 | 0.36 | $C_{C1}$=5.4 $C_{C2}$=4 | 2200 | 564 | 3235 | 212 |
| ACBCF [14] | 500 | 2 | 0.162 | 0.324 | 1.9 | 1 | $C_{C1}$=10 $C_{C2}$=3 | 2932 | 1543 | 5864 | 3086 |
| TCFC [15] | 150 | 1.5 | 0.03 | 0.045 | 2.85 | 1.035 | $C_{C1}$=1.1 $C_{C2}$=0.92 | 9500 | 3450 | 14250 | 5175 |
| DPZCF [16] | 500 | 1.5 | 0.15 | 0.225 | 1.4 | 2 | $C_{C1}$=30 $C_{C2}$=20 | 3111 | 4444 | 4667 | 6666 |
| RNMC with VB NR [18] | 15 | 3 | 0.48 | 1.44 | 19.46 | 13.8 | $C_{C1}$=3 $C_{C2}$=0.7 | 209 | 149 | 608 | 431 |
| SMFFC [22] | 120 | 2 | 0.21 | 0.42 | 9 | 3.4 | $C_{C1}$=4 (one) | 2571 | 971 | 5143 | 1943 |
| This work | **500** | **3** | **0.083** | **0.249** | **2.87** | **1.55** | **$C_{C1}$=10 $C_{C2}$=0.3** | **5764** | **3112** | **17292** | **9338** |

a. average value

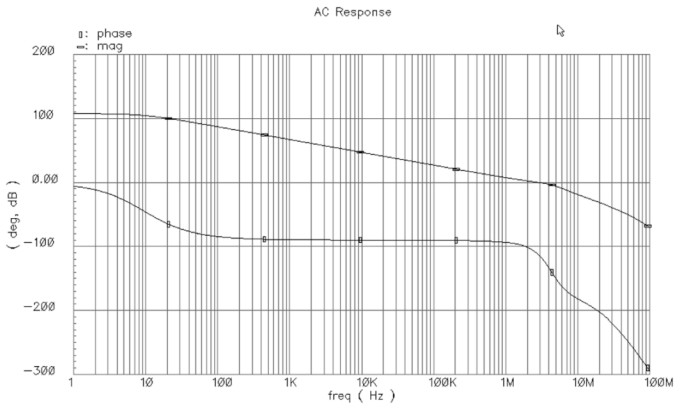


Fig. 4. Simulated open-loop frequency response.

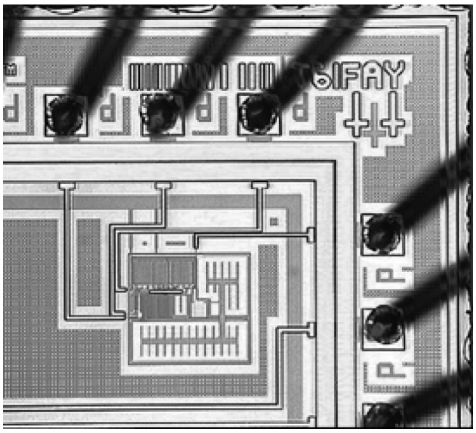

Fig. 5. Chip microphotograph of the OTA.

The performance of different amplifiers are usually compared using two figures of merit (FOMs), referring to the small-signal and large-signal behavior, given by [11]–[16]

$$\mathrm{FOM}_S = \frac{\omega_{\mathrm{GBW}} \cdot C_L}{\mathrm{Power}} \tag{6}$$

$$\mathrm{FOM}_L = \frac{\mathrm{SR} \cdot C_L}{\mathrm{Power}} \tag{7}$$

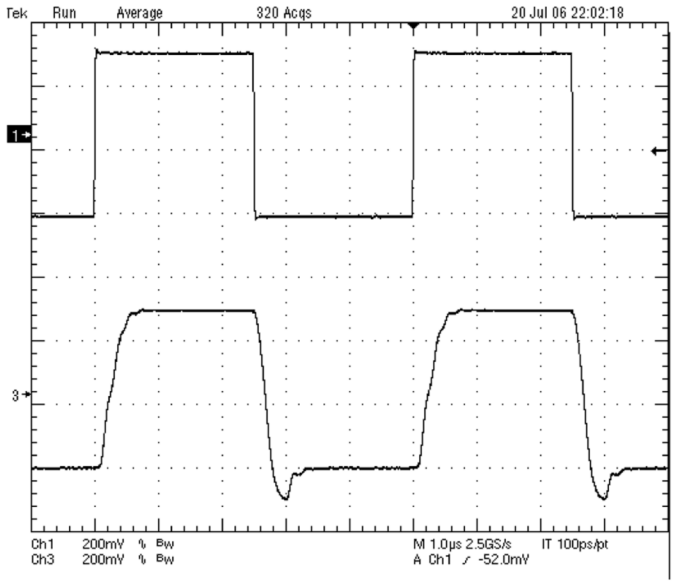


Fig. 6. Measured unity-gain transient response.

where SR is the average amplifier slew rate and $Power$ is the dc power consumption. The higher is the value of both $\mathrm{FOM}_S$ and $\mathrm{FOM}_L$, the better is the amplifier performance. However, these FOMs may lead to imprecise results because they depend upon the supply voltage. Since $\omega_{\mathrm{GBW}}$ and SR depend on the quiescent currents flowing in the relevant transistors, in order to allow a fair comparison, two more precise FOMs were proposed in [14], [15]

$$\mathrm{IFOM}_S = \frac{\omega_{\mathrm{GBW}} \cdot C_L}{I_{dd}} \tag{8}$$

$$\mathrm{IFOM}_L = \frac{\mathrm{SR} \cdot C_L}{I_{dd}}. \tag{9}$$

By using these formulas, a performance comparison with other multistage amplifier topologies is reported in Table III. It is clear that the proposed solution shows an improvement in both small-signal and large-signal performances, while maintaining a relatively simple circuit architecture.

## IV. Conclusion

A novel compensation technique exploiting a voltage buffer and a nulling resistor, along with a feedforward stage, was presented. The solution shows better performance than the basic RNMC topology because the use of the voltage buffer plus the resistor allows to extend the maximum achievable bandwidth, while improving phase margin. Moreover, the additional feedforward stage $g_{mf}$ in conjunction with the last stage forms a push-pull output stage which is capable of driving the loading capacitor with a current much greater than the quiescent one.

The compensation is achieved through a double pole–zero cancellation. Since both cancellations occur beyond the gain-bandwidth product, the technique is robust against any imperfect matching of the poles and zeroes due to process variations and mismatches.

Experimental measurements on a fabricated amplifier and a comparison with other previously reported solutions confirmed the effectiveness of the proposed approach.

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