ON-CHIP CURRENT SENSING TECHNIQUE FOR CMOS MONOLITHIC SWITCH-MODE POWER CONVERTERS

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ABSTRACT

An on-chip current sensing technique, which is suitable for monolithic switch-mode power converter, is presented in this paper. This current sensing technique has been fabricated with a standard 0.6 μm CMOS process. Experimental results show that the switching converter can operate from 300 kHz to 1 MHz with the duty-ratio ranging from 0.2 to 1. The supply voltage of this current sensing circuit is from 3 V to 4.2 V, which is suitable for lithium ion battery applications. The discrepancy between the sensed signal and the inductor current is less than 4 %, corresponding to 10 mA with load current 300 mA.

1. INTRODUCTION

In today's consumer market, battery-operated portable electronic devices are in great demand. Portable systems require high-efficiency low-voltage DC-DC converters to efficiently generate low-voltage supply from a single battery source for maximizing the system run time. In order to decrease the size and weight of these devices, miniaturization of the power modules is essential. As a result, the trend is to focus on the CMOS implementation of converters with low power consumption.

In both voltage-mode and current-mode switch-mode power converters (SMPC), the sensing signal of the output current is necessary as it can detect openload, short-circuit and over-current situations for both energy saving and protection purposes. In particular, for the current-mode control schemes, their controllers require the sensing of the inductor current throughout the whole switching period. Therefore, an accurate current sensing circuit is necessary for all current-mode SMPC. At present, there are different current sensing techniques, which have been published or implemented [1-6]. However, each of these methods suffers from some major disadvantages, which limit their applications.

The most common method for sensing the output current of the current-mode converters is using a sensing resistor in series with the inductor or power transistor. The main concern of this approach is its high power dissipation, as all of the inductor current or drain current of the power transistor must pass through the sensing resistor. The problem becomes more severe for low-voltage high current applications. Another common method is using an integrator to determine the inductor current. This control scheme is sometimes claimed as a sensorless/lossless current-mode control [1]. However, it would increase the complexity of designing different kinds of converters as different topologies have different integrals. Moreover, the accuracy of this current sensing scheme is influenced by different factors, such as the time-constant value tolerance of the filter and manufacturing tolerances on the inductor. The third sensing technique is using the on-resistance of the power MOSFET instead of the sensing resistor [2]. The main concern of this sensing scheme is the value of R_{on} required for good control of the converters. If R_{on} is small (for example less than 100 mΩ for high efficiency), then the sensing signal is not large enough for control purposes and an additional operational amplifier (current sense amplifier) may be required. On the other hand, if R_{on} is large (for example 1 Ω), then its high power dissipation would reduce overall efficiency of the converters, especially for low-voltage high-current applications. Moreover, R_{on} varies with temperature and different processes. Some sensing techniques use the current transformer for sensing a current signal, but this is not suitable for portable electronic device applications due to the large transformer size and weight. There are also many other current sensing schemes that have been published or implemented. For example, using the duty-cycle signal information for current sensing is only suitable for high current applications [3]. As described above, each of the current sensing schemes has its own drawbacks and limitations in monolithic switch-mode power converter applications.

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The conventional on-chip current sensing scheme is addressed in Section 2. The operational principle of the proposed on-chip current sensing circuit is discussed in Section 3. Simulation results and measurement results are included in Section 4 and Section 5, respectively, to justify the proposed internal current sensing scheme. Finally, the summary is given in Section 6.

2. CONVENTIONAL ON-CHIP CURRENT SENSING SCHEME

One of the on-chip current sensing techniques implemented in the BiCMOS process is shown in Figure 1 [4]. The aspect ratio of transistor M_1 is much larger than that of M_2, for example 5000:1, and M_2 functions as a sense transistor such that the drain current of M_2 is 1/5000 of the drain current of M_1 if the voltage at node A is equal to that of node B. In this case, the bipolar Q_1 and Q_2 are used to force the V_{DS} of M_1 and M_2 to equal and function as a voltage mirror together with the current sources I_1 and I_2. If the voltage at node V_A is exactly the same as at node V_B, then the drain current of M_2 is exactly 1/5000 that of M_1. However, the bipolar voltage mirror cannot provide a good voltage mirror and thus the accuracy of the sensing circuit is seriously degraded.

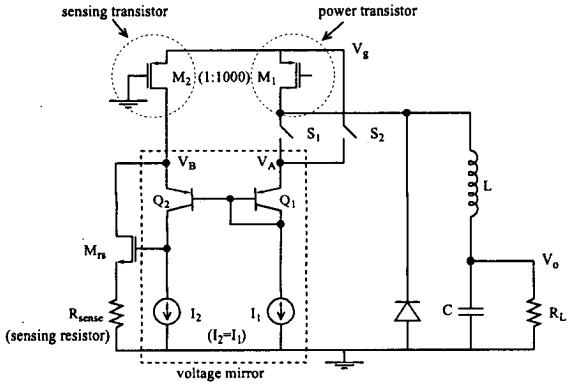

Figure 1: An on-chip current sensing circuit implemented by BiCMOS process

There are other simple sensing circuits, which are implemented by BiCMOS process, such as SENSEFET used in DMOS smart power IC applications [5], or a sensing transistor used together with BiCMOS integrated circuits [6]. However, they cannot provide accurate sensing performance and are only used for detecting openload, short-circuit and over-current purposes.

3. PROPOSED ON-CHIP CURRENT SENSING SCHEME

From the previous discussion, the accuracy of the current sensing circuit shown in Figure 1 is mainly dependent on the voltage at V_A and V_B. In order to achieve a high accuracy, an operational amplifier is used to force the voltage at node A and node B to be the same [7]. The proposed on-chip current sensing scheme is shown in Figure 2.

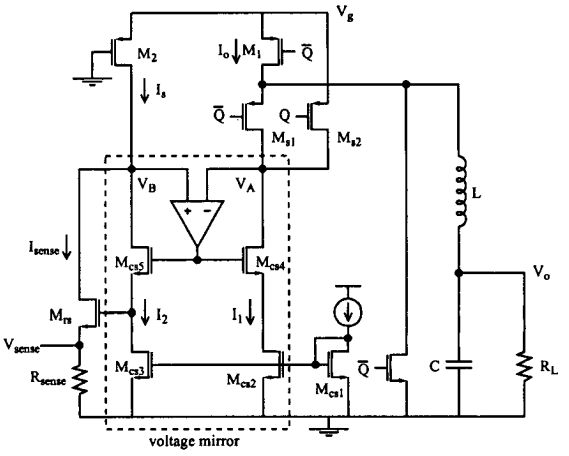

Figure 2: The proposed on-chip current sensing circuit

In Figure 2, two current sources, I_1 and I_2, of small and equal magnitude pull the current from node V_A and V_B. An output current I_o, which flows through the power transistor M_1, is mirrored to the sense transistor M_2. Any change in V_A will force a similar change in V_B due to the virtual short-circuit provided by the operational amplifier. Thus, the drain-to-source voltage V_{DS} of transistors M_1 and M_2 are almost the same, as well as their drain current density. However, the transistors M_1 and M_2 are scaled so that power transistor M_1 on the output side of the circuit has an aspect ratio much great than that of transistor M_2 on the sensing side, for example 1000:1. As a result, the current I_s on the sensing side is much smaller than, and proportional to, the current I_o on the output side. The output sensing current I_{sense}, which passes through the internal resistor R_{sense}, is the difference between the sensing current I_s flowing through the transistor M_2 and the current I_2 flowing through the small biasing current source. Therefore, the current I_{sense} flowing through the internal resistor R_{sense} is proportional to and substantially much smaller than the current I_o flowing through the load.

For the current-mode Buck converter application, the sensing voltage V_{sense} is useful in the control feedback loop only during the ON-state (the ramp up portion of the inductor current). Thus, only the signal from the power transistor M_1 during turn ON is useful, and therefore, the gate of the transistor M_2 is always coupled to ground. The switches M_{S1} and M_{S2} are used such that the node V_A would not be shorted to the ground during the OFF-states of the switching cycle. As a result, there will not be a large current flowing through the sensing resistor R_{sense}. In

addition, the transistor M_{rs} should always operate in the saturation region such that there is enough drain-to-source V_{DS} drop across M_{rs} and V_{sense} will not go to V_g.

4. SIMULATION RESULTS

The simulations are based on the circuit shown in Figure 2. Ideal gate signals are used to drive the power transistors and the two switches, M_{s1} and M_{s2} for the PWM control of the DC-DC Buck converter. The simulation results of the sensing signal and the scale inductor current are shown in Figure 3. The scaled inductor current is divided by the factor 1000/400, where 1000 is the transistor size ratio M_1/M_2 and 400 is the resistance of R_{sense}, such that the sensing signal in voltage can be compared easily with the inductor current. It shows that the sensed signal is matched to the inductor current. The 3-mV difference between the scaled inductor current and sensing signal in Figure 3 is mainly due to the current difference between I_s and I_2 in Figure 2. The sensing current I_{sense} is given by

$$I_{sense} = I_s - I_2. \qquad (1)$$

However, the difference between I_s and I_2 is not a problem from the control point of view. The most important point is that the sensing signal can trace the inductor current well. There is also a delay time, in this case 200 to 300 ns, in the sensing signal each time the inductor current ramps up. This is mainly due to the response time of the operational amplifier and the turn-on time of the transistor M_{rs} at the beginning of each switching cycle. This is also not a critical problem for controlling purposes as the duty ratio of the DC-DC buck converter is typically larger then 0.2 for most of the applications.

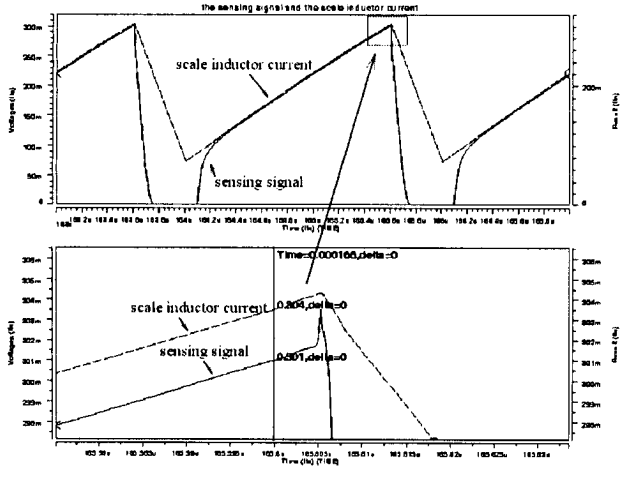

Figure 3: Simulation of the sensing signal and the scaled inductor current

5. MEASUREMENT RESULTS

The current sensing scheme is implemented by AMS* 0.6 μm CMOS process and its micrograph is shown in Figure 4. The size of whole chip is 2.034 mm^2 and the current sensing circuit is 0.0742 mm^2. Most of the chip area is used for the power PMOS and NMOS transistors.

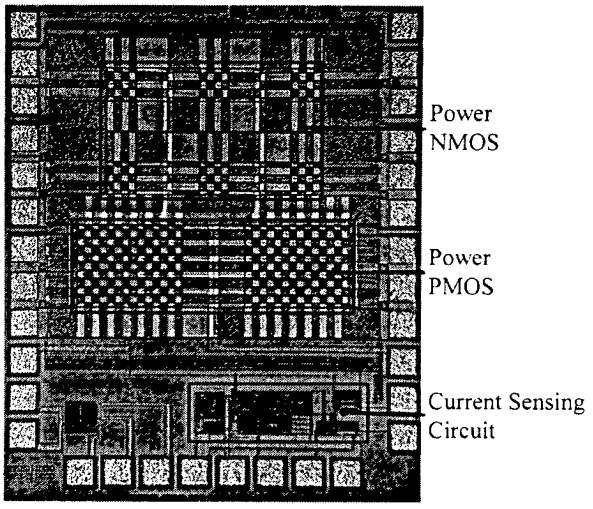

Figure 4: The micrograph of the proposed current sensing circuit

The testing of this current sensing scheme is based on the open-loop DC-DC Buck converter. The experimental setup is shown in Figure 5. A dual high-speed MOSFET drivers Texas Instruments TPS2813P is used for driving two power MOSFETs of the current sensing circuit and controlling the converter. The switching frequency and the duty-ratio is dependent on the input of the IC chip TPS2813P and controlled by the signal generator.

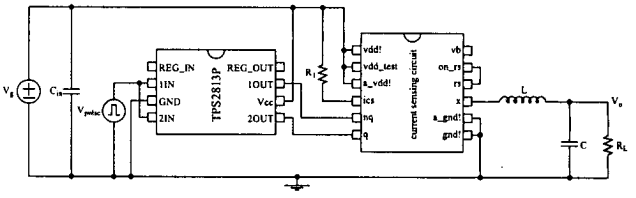

Figure 5: Experimental setup of the proposed current sensing scheme

Figure 6 shows the measurement results of the sensing signal and the inductor current with different switching frequencies and different duty-ratios at supply voltage 3.6 V. The inductor current ranged from 50 mA to 500 mA.

* Austria Miko Systeme International AG, Austria

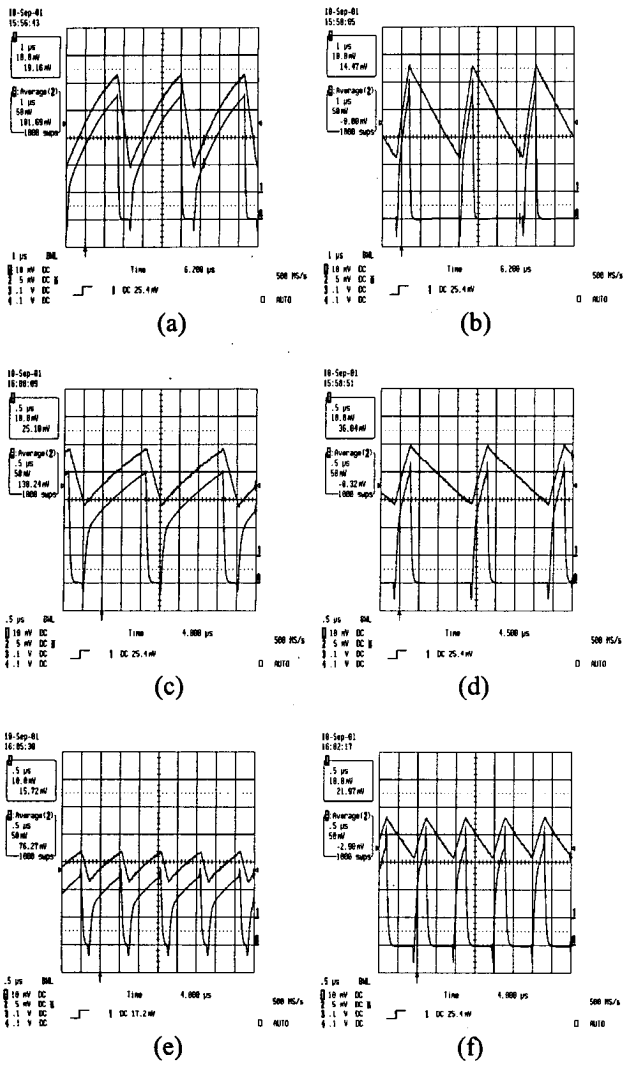

Figure 6: Sensing signal (50 mV/div) and inductor current (100 mA/div) (a) duty-ratio=0.8, (b) duty-ratio=0.2 at switching frequency=300 kHz; (c) duty-ratio=0.8, (d) duty-ratio=0.2 at switching frequency=500 kHz; (e) duty-ratio=0.8, (f) duty-ratio=0.3 at switching frequency=1 MHz.

In Figure 6, channel 1 represents the inductor current, which is measured by the current probe. Channel A represents the sensing signal, which is the voltage across the resistor R_{sense}. The channel 1 is shifted up by one division compared with channel A in the oscilloscope such that the comparism of the two waveforms can be seen more clearly. The measurement results show that the sensing signal is matched to the inductor current at different switching frequencies and different duty-ratios. The discrepancy between the sensing signal and the inductor current is less than 4 %, which corresponds to 10 mA with loading current of 300 mA.

6. CONCLUSIONS

In this paper, the proposed current sensing scheme is addressed including the principles of operation, design issues, circuit implementations, simulations and measurement results. The results show that the performance of the proposed current sensing technique is more accurate and simpler than the conventional methods. In addition, this technique is not strongly dependent on other parameter variations, such as frequency, temperature and external components. This sensing technique is also suitable for all kinds of applications and provides high efficiency. Besides, this sensing technique can be simply fabricated using any standard CMOS process. From the measurement results, the proposed current sensing scheme can successfully operate from 300 kHz to 1 MHz with the duty-ratio ranging from 0.2 to 1 with less than 4 % discrepancy.

ACKNOWLEDGEMENTS

This work was supported by Research Grant Council of Hong Kong SAR, China (Project No. HKUST 6022/01E).

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