A Wideband Inductorless LNA With Local Feedback and Noise Cancelling for Low-Power Low-Voltage Applications

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***Abstract*—A wideband noise-cancelling low-noise amplifier (LNA) without the use of inductors is designed for low-voltage and low-power applications. Based on the common-gate–common-source (CG-CS) topology, a new approach employing local negative feedback is introduced between the parallel CG and CS stages. The moderate gain at the source of the cascode transistor in the CS stage is utilized to boost the transconductance of the CG transistor. This leads to an LNA with higher gain and lower noise figure (NF) compared with the conventional CG-CS LNA, particularly under low power and voltage constraints. By adjusting the local open-loop gain, the NF can be optimized by distributing the power consumption among transistors and resistors based on their contribution to the NF. The optimal value of the local open-loop gain can be obtained by taking into account the effect of phase shift at high frequency. The linearity is improved by employing two types of distortion-cancelling techniques. Fabricated in a 0.13-μm RF CMOS process, the LNA achieves a voltage gain of 19 dB and an NF of 2.8–3.4 dB over a 3-dB bandwidth of 0.2–3.8 GHz. It consumes 5.7 mA from a 1-V supply and occupies an active area of only 0.025 mm^2.**

***Index Terms*—g_m boost, inductorless, local feedback, low power, low voltage, noise cancelling, wideband low-noise amplifier (LNA).**

I. Introduction

RECENTLY, software-defined and reconfigurable multi-standard radio receivers have drawn close attention and are considered for future radios [1]–[3]. This type of radio requires multiple narrowband low-noise amplifiers (LNAs) or a wideband LNA that covers multiple frequency bands. A single wideband LNA shared among different standards is preferred to save power and reduce complexity. Such an LNA should achieve good impedance matching, high gain, and low noise figure (NF) across a wide frequency band.

The fast-evolving scaled CMOS technologies demonstrate excellent performance including high f_T, $f_{\max}$, and low $\mathrm{NF}_{\min}$, providing a good margin for the design of high-performance LNAs with low cost [4]. However, traditional LNAs with on-chip inductors occupy a large area which counters the benefit brought by the scaled digital CMOS [5]. Furthermore, although inductors resonant with parasitic capacitors lead to higher gain and better NF, the lack of accurate inductor modeling complicates the circuit design, resulting in possible trial-and-error tape-outs. Off-chip inductors have higher Q values than on-chip inductors. However, they increase the cost and reduce the yield. Thus, employing an inductorless LNA becomes an attractive choice for many low-cost applications.

The supply voltage of mainstream digital circuits scales with technology, e.g., 1.2-V supply for 0.13-μm digital CMOS. However, RF analog circuits often fall behind the scaling trend because a higher supply voltage is preferred to obtain higher gain and better linearity, which reduces the reliability due to the low breakdown voltage of nano-MOSFETs. The problem is particularly severe in inductorless designs because the inductors are substituted by resistors, which require extra voltage drops. Moreover, compared with the traditional LNAs with inductors, the wideband LNAs with resistors always consume more power to compensate the inadequate capability.

Several wideband inductorless LNAs have been published in recent years. They can be classified into two categories according to their topologies. The first type is common-source (CS) amplifier with resistive [6] or active feedback [7], [8]. The second type is common-gate (CG) amplifier combined with techniques of g_m boosting [9], [10] or noise cancelling [11], [12]. Nevertheless, they suffer from critical tradeoffs between, for example, gain and matching, or supply voltage and NF. The limitations of the aforementioned LNAs will be described quantitatively in Section II.

To overcome the shortcomings of previous LNA topologies, a new wideband inductorless LNA for low-voltage low-power applications is proposed in this paper. Based on the CG-CS topology, a local negative feedback is introduced between CG and CS stages. The gain at the source of the cascode transistor in the CS stage is utilized to boost the g_m of the CG transistor to bring both power consumption and supply voltage down. This paper is organized as follows. Section II reviews the previous inductorless-LNA design approaches, focusing on the supply voltage, power consumption, and NF issues, and puts forward our new idea. Section III gives a detailed description of the proposed LNA design including NF optimization and distortion cancellation. In Sections IV and V, the LNA circuit design, implementation, and experimental results are described. Finally, the conclusions are given in Section VI.

II. Limitations of Previous Work and the Proposed Idea

In this section, the shortcomings of two types of common wideband inductorless CMOS LNA topologies are analyzed in order to highlight the critical tradeoff between voltage, power,

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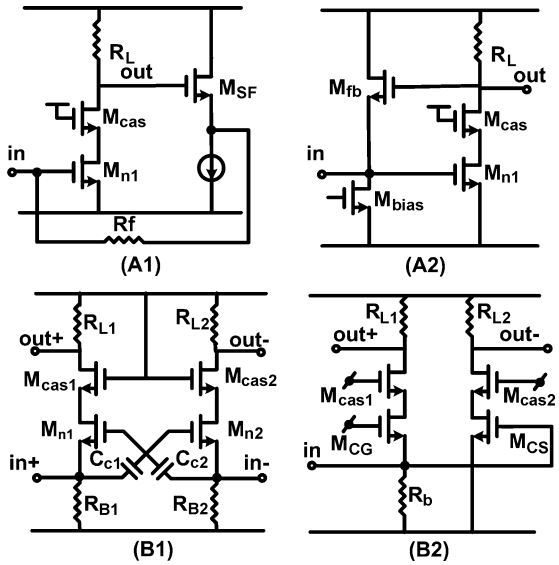

Fig. 1. (A1) CS LNA with resistive feedback. (A2) CS LNA with active feedback. (B1) CG LNA with g_m boosting. (B2) CG-CS LNA with noise cancelling.

and NF when inductors are eliminated. Then, the idea of the proposed LNA will be brought forth with comparison with the two classical types of LNA.

A. CS LNA With Resistive or Active Feedback

As shown in Fig. 1(A1) and (A2), the CS LNA achieves impedance matching by the global resistive or active feedback, which is defined as the feedback between the LNA output and input nodes; e.g., in A2, the condition for impedance matching can be expressed as

$$R_s = \frac{1}{g_{m\mathrm{fb}}(1 + AV_{\mathrm{open}})}. \tag{1}$$

Here, AV_{open} is the open loop gain at the output node. However, the impedance matching degrades due to gain roll-off at higher frequency because the feedback signal is taken from the output node, which has relatively high gain and low bandwidth. At the same time, driven by the large signal swing of the output, the nonlinear feedback transistor M_{fb} or the source follower transistor M_{SF} degrades the linearity of the LNA severely [7].

B. CG LNA With g_m Boosting or Noise Cancelling

A capacitive cross-coupling CG LNA is presented in [9], which utilizes the differential input signal to boost the g_m of CG transistors, as shown in Fig. 1(B1). The power and the NF are both improved by a factor of two. However, the voltage gain $(A_v = 2g_mR_L = R_L/R_S)$ is still restricted by the impedance matching condition $(R_s = 1/2g_m)$ and cannot get quite high due to the limitation of the voltage drops on R_L and R_B. The CG-CS LNA combined with noise cancelling exhibits good input impedance matching and low NF [11]–[13], as shown in Fig. 1(B2). The g_m of M_{CG} is set by the 50-Ω impedance matching. The balanced outputs and noise cancelling of the CG transistor can be achieved simultaneously under the condition

$$g_{\mathrm{mCG}}R_{L1} = g_{\mathrm{mCS}}R_{L2}. \tag{2}$$

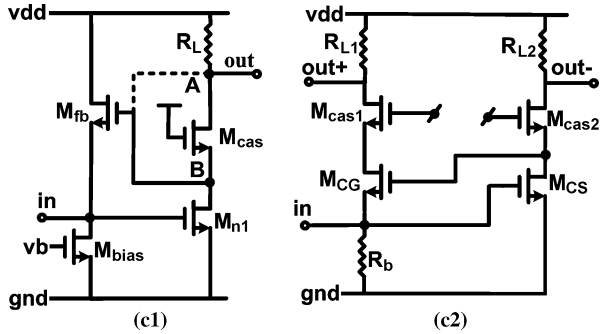

Fig. 2. Proposed improved version of the topologies in Fig. 1(A2) and (B2). (C1) CS LNA with local feedback. (C2) CG-CS LNA with local feedback.

However, this topology suffers from critical tradeoff between NF and supply voltage. A simple calculation can reveal this problem. Assuming a supply voltage of 1.2 V, overdrive voltages of 0.2 V, and drain–source voltages (vds) of 0.3 V to ensure saturation-region operation, the current flowing in the CG stage can be calculated approximately by $I_D = g_m \times V_{od}/2 = 20\,\mathrm{mS} \times 0.2/2 = 2\,\mathrm{mA}$ and the sum of the two resistors (R_b and R_{L1}) would be restricted as $(1.2\,\mathrm{V} - 2 \times 0.3\,\mathrm{V})/2\,\mathrm{mA} = 300\,\Omega$. The low value of these resistors result in NFs about 1–2 dB higher as expressed in

$$F_{\mathrm{res}} - 1 = \frac{R_s}{R_b} + \frac{R_s}{R_{L1}} \geq \frac{4R_s}{R_b + R_{L1}} = \frac{4 \times 50}{300} = 0.67. \tag{3}$$

In [11], a high supply voltage (1.8 V) is adopted in the 90-nm CMOS process to reduce the NF. In [12], the cascode transistors are removed with the sacrifice of reverse isolation to enable operation under 1.2 V. However, a rather high power (20 mW) is consumed to reduce the NF to about 3 dB. In [13], the resistor R_b is replaced with an off-chip inductor, which increases integration cost.

C. Proposed New Versions With Local Feedback

The problem of CS feedback LNA lies in the fact that the output node is overburdened by a large gain and limited bandwidth. To overcome it, a local feedback technique is proposed to replace the global feedback. As seen in Fig. 2(C1), the feedback signal is taken from the source of the cascode transistor (node B) instead of the output node (node A). Due to the high bandwidth of node B, the local feedback holds to be effective up to a quite high frequency. Simulation results demonstrate that the bandwidth of node B is much higher than that of node A, as shown in Fig. 3(a). As a result, the LNA with local feedback achieves a flatter S11 (< -15 dB) than that with global feedback, as shown in Fig. 3(b).

To address the problem of the CG-CS LNA [Fig. 1(B2)], the same local feedback can be applied here to boost the CG transistor, as shown in Fig. 2(C2). The transconductance of M_{CG} benefits from the negative feedback and is boosted by a factor. The current of the CG stage can be reduced by the same factor, and a large voltage headroom is released to allow the use of large resistors.

It is interesting to compare the two improved topologies [Fig. 2(C1) and (C2)]. With the same local feedback, the two

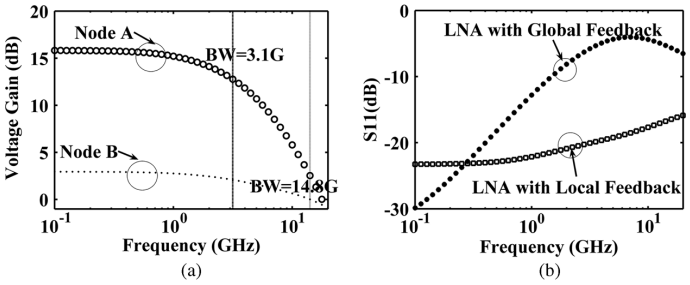

Fig. 3. Comparison between the topologies in Figs. 1(A2) and 2(C1). (a) Simulated bandwidth of nodes A and B. (b) Simulated S11 of LNA with global feedback and LNA with local feedback.

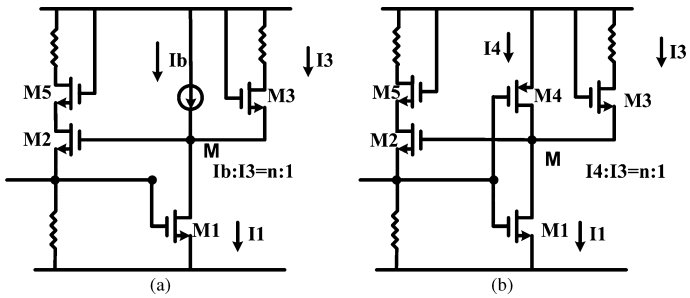

Fig. 4. Adjustable local feedback implemented by (a) a current source and (b) a pMOS amplifier.

look like each other except that the signal at the drain of the feedback transistor is taken out as a positive output in the latter one. In fact, the differential outputs not only double the voltage gain but also enable the cancellation of the noise of the feedback transistor (or CG transistor). Therefore, the topology in Fig. 2(C2) is a better choice in terms of gain and noise. To make Fig. 2(C2) a flexible design, a current source is added in parallel with M3, as shown in Fig. 4(a). This technique called current steering was reported in [6] and [8] to alleviate the large voltage drop on R_{L2}. In this paper, it has another use: acting as a controller of the local feedback. The open loop gain $(A_{\rm VM})$ and bandwidth (ω_M) of node M can be adjusted by changing the current ratio (n) of the current source and the cascode transistor in a certain range as expressed in (4) and (5). A more effective solution is shown in Fig. 4(b). The current source is replaced by a pMOS FET to reuse the current of the CS stage as well as amplify the signal together with nMOS M_1.

Local open loop gain

$$A_{\rm VM} = \frac{g_{m1} + g_{m4}}{g_{m3}} \approx \frac{I_1 + I_4}{I_3} = 1 + 2n. \tag{4}$$

Bandwidth of node M

$$\omega_M = \frac{g_{m3}}{C_{\rm dbM_1} + C_{\rm gdM_1} + C_{\rm dbM_4} + C_{\rm gdM_4} + C_{\rm gsM_3}} = \frac{g_{m1} + g_{m4}}{C_{\rm dbM_1} + C_{\rm gdM_1} + C_{\rm dbM_4} + C_{\rm gdM_4} + C_{\rm gsM_3}} \frac{1}{A_{\rm VM}}. \tag{5}$$

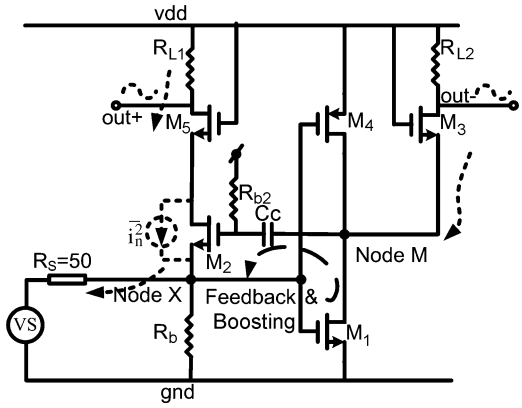

Fig. 5. Simplified schematic of the proposed LNA.

III. Proposed Inductorless LNA

A. Basic Principle of Proposed LNA

The proposed LNA, as shown in Fig. 5, employs noise cancelling to eliminate the noise from the CG transistor (M_2) and cascode transistor (M_3). The principle of noise cancellation can be briefly explained as follows [15], [16]. The channel noise of transistor M_2, which is the dotted current source, undergoes subtraction at output nodes (out+ and out−) due to the two correlated but out-of-phase noise voltages at V_x and $V_{\rm out+}$.

The local feedback is adopted to accommodate low-voltage and low-power applications. From the perspective of the CG stage, the g_m of M_2 benefits from the negative feedback and is boosted by a factor of $1 + A_{\rm VM}$. From the perspective of the CS stage, the current steering enhances the gain and NF while bringing down the voltage drop on R_{L2}. The expression of input-impedance-matching condition, the voltage gain, and the NF of the proposed LNA are given in the following sections. A detailed derivation is presented in Appendices A and B.

1) Input Impedance Matching: The impedance matching is achieved when

$$R_s = \frac{1}{g_{m2}(1 + A_{\rm VM})}. \tag{6}$$

In this formula, R_S is the source impedance and typically equals 50 Ω. The transconductance needed for input impedance matching is reduced by a factor of $1 + A_{\rm VM}$ compared with the traditional CG-CS-type LNA [11].

2) Voltage Gain: Within the negative feedback loop, the detailed analysis is a little complicated, but the result is quite simple, as shown in (7) when the impedance matching condition (6) is satisfied

$$A_V = \frac{R_{L1}}{R_s} + (g_{m1} + g_{m4})R_{L2}. \tag{7}$$

The differential outputs are balanced when

$$\frac{R_{L1}}{R_s} = (g_{m1} + g_{m4})R_{L2}. \tag{8}$$

Equation (8) is also the condition for noise cancellation.

Under this situation, the voltage gain can be rewritten as

$$A_V = \frac{2R_{L1}}{R_s} = 2(g_{m1} + g_{m4})R_{L2}. \tag{9}$$

3) Noise Factor: The noise factor under input-impedance-matching and output-balance conditions can be expressed as

$$\begin{aligned} F =& 1 + \frac{\gamma_1}{\alpha_1}\frac{g_{m1}}{(g_{m1}+g_{m4})^2 R_s} + \frac{\gamma_4}{\alpha_4}\frac{g_{m4}}{(g_{m1}+g_{m4})^2 R_s} \\ &+ \frac{1}{R_s(g_{m1}+g_{m4})^2 R_{L2}} + \frac{R_s}{R_b} + \frac{R_s}{R_{L1}} \\ &+ \frac{\gamma_3}{\alpha_3}\frac{1}{4R_s g_{m3}(1+A_{\rm VM})^2}\epsilon_{\rm mis}^2 + \frac{\gamma_2}{\alpha_2}\frac{1}{4(1+A_{\rm VM})}\epsilon_{\rm mis}^2. \end{aligned} \tag{10}$$

In (10), the second and third terms refer to the noise contribution of M_1 and M_4. They take up the largest part in the noise factor. The next three terms depict the influence on the NF of resistors including load resistors R_{L2} and R_{L1} and bias resistor R_b. The last two terms refer to the noise contribution of M_3 and M_2. Due to the interaction between the CG and CS stages brought by the local feedback, the noise current from M_3 and M_2 couples to both out+ and out−. Luckily, they can be cancelled totally when the two stages have exactly the same gain (8). The gain mismatch $\epsilon_{\rm mis}$ between the CG and CS stages leaves part of the noise not cancelled, which again would be suppressed largely by the open-loop gain $A_{\rm VM}$. The derivation in detail is given in Appendixes A and B.

B. NF Optimization Under Voltage and Power Constraints

First, the expression of the noise factor is rewritten as to highlight the impact of the voltage and power of every component on the noise factor. Expression (11) is transformed from (10) by the substitution of g_m with $2I_{\rm ds}/V_{\rm ov}$ and of R with V_R/I_R (the second and third terms in (10) are combined with the approximation of $\gamma_1/\alpha_1 \approx \gamma_4/\alpha_4$)

$$\begin{aligned} F =& 1 + \frac{\gamma_1}{\alpha_1}\frac{1}{\left(\frac{2I_{M_1}}{V_{{\rm ov},M_1}} + \frac{2I_{M_4}}{V_{{\rm ov},M_4}}\right)R_S} \\ &+ \frac{I_{R_{L2}}}{\left(\frac{2I_{M_1}}{V_{{\rm ov},M_1}} + \frac{2I_{M_4}}{V_{{\rm ov},M_4}}\right)^2 R_S V_{L2}} + \frac{R_s I_{R_b}}{V_{R_b}} \\ &+ \frac{R_s I_{R_{L1}}}{V_{R_{L1}}} + \frac{\gamma_3}{\alpha_3}\frac{1}{4R_s(1+A_{\rm VM})^2\frac{2I_{M_3}}{V_{{\rm ov},M_3}}}\epsilon_{\rm mis}^2 \\ &+ \frac{\gamma_2}{\alpha_2}\frac{1}{4(1+A_{\rm VM})}\epsilon_{\rm mis}^2. \end{aligned} \tag{11}$$

It can be seen from (11) that the sensitivities of the NF to the power (voltage and current) consumed by transistors and resistors are not the same. For example, M_1 and M_4 are power hungry because a high g_m is desired to reduce their noise contribution. While M_2 and M_3 have little demand for power due to the noise cancellation, but may be restricted by dc operation or impedance-matching requirements, on the other hand, large voltage and small current are preferred by resistors.

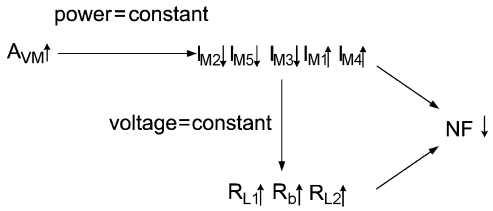

Fig. 6. Relationship between $A_{\rm VM}$ and NF.

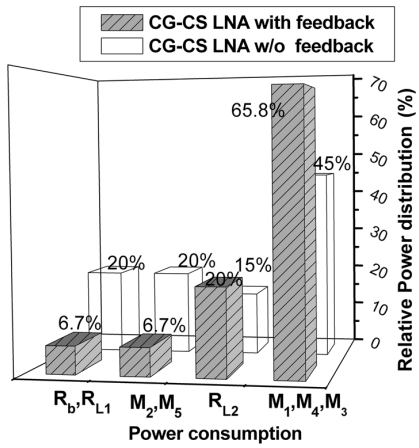

Fig. 7. Comparison of power distribution between the CG-CS LNA with local feedback and that without local feedback.

In the previous CG-CS LNAs without feedback, the power and voltage of every transistor or resistor cannot be deeply optimized due to the dc limitation of the topology. In this design, the current steering in the CS stage and the interaction between the CG and CS stages introduced by the local feedback provide an opportunity to distribute the power consumption and voltage drop among transistors and resistors toward the optimization. The relationship between $A_{\rm VM}$ and NF can be described briefly, as shown in Fig. 6. The local open loop gain $A_{\rm VM}$ is also rewritten to show this relationship in

$$A_{\rm VM} = \frac{\frac{I_{M_1}}{V_{{\rm ov},M_1}} + \frac{I_{M_4}}{V_{{\rm ov},M_4}}}{\frac{I_{M_3}}{V_{{\rm ov},M_3}}} \approx \frac{I_{M_1} + I_{M_4}}{I_{M_3}} \tag{12}$$

$$A_{\rm VM} = \frac{1}{g_{m2}R_S} - 1 = \frac{V_{{\rm ov},M_2}}{2I_{M_2}R_S} - 1. \tag{13}$$

Circuit simulation is carried out to verify the idea. Under a 1-V supply voltage, a 6-mW power constraint, and with the condition of input impedance matching and gain balance, the traditional CG-CS LNA without feedback ($A_{\rm VM} = 0$) and the proposed LNA with feedback ($A_{\rm VM} = 2$) are designed and optimized individually to achieve an NF as low as they can. Then, they are compared in terms of power distribution and noise contribution. The proposed LNA gives a more favorable power distribution for NF, as shown in Fig. 7. In addition, as expected, the main noise contributions from M_1, M_4, R_{L1}, and R_b in the proposed one are reduced by a large extent, as shown in Fig. 8.

Under the condition of noise cancellation, the two types of LNAs are simulated at different power levels and under different supply voltages (1.8 and 1 V). As shown in Figs. 9 and 10, both of them demonstrate a trend of reduced NF with the increase of

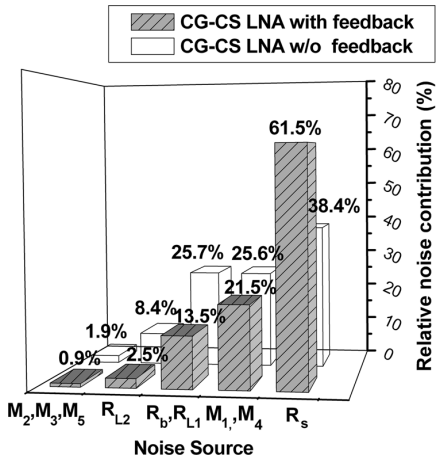

Fig. 8. Comparison of noise distribution between CG-CS LNA with local feedback and that without local feedback. (R_s denotes the source resistance.)

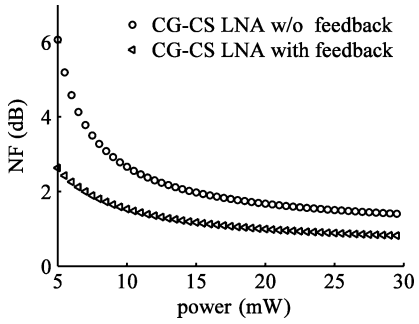

Fig. 9. NF at different power levels under a 1.8-V supply voltage. (Both types are simulated under the condition of input impedance matching and gain balance.)

power and approach a limit when the power gets infinite. Under high supply voltage (1.8 V), the proposed LNA with feedback gives a much lower NF at a low power level, but shows almost the same limit as the one without feedback. Under a low supply voltage (1 V), the proposed one not only shows superiority at a low power level but also has a lower limit than the traditional one. Therefore, the proposed LNA shows a distinct advantage for low-voltage and low-power applications than the previous LNA.

According to the aforementioned description, it seems that the higher the $A_{\rm VM}$ we choose, the lower the NF becomes. However, when the frequency gets high, a large $A_{\rm VM}$ will increase the NF for the sake of phase shift and signal loss. A high $A_{\rm VM}$ generates a low frequency pole ω_M at node M. Moreover, the input capacitance of M_1 and M_4 goes up dramatically because of the $C_{\rm gd}$ multiplied by the high Miller factor and creates another low frequency pole ω_X at node X. The different poles that

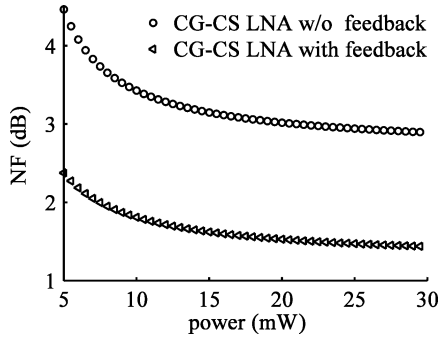

Fig. 10. NF at different power levels under a 1-V supply voltage. (Both types are simulated under the condition of input impedance matching and gain balance.)

the CG and CS stages undergo will introduce a phase shift between two stages, which have an adverse impact on the noise cancellation because ideal cancellation requires that the voltages of out+ and out− have exactly the same magnitude and opposite phases. The phase shift is calculated and given in Appendix C, and it is found that the big value of $A_{\rm VM}$ should be responsible for the large phase shift. Furthermore, a large part of the signal current shunts down to ground at node M if the value of $g_{m3}/(g_{\rm ds1}+g_{\rm ds4})$ is too low, which reduces the output voltage of the signal.

The noise contributions of all the transistors and resistors with different values of $A_{\rm VM}$ at a frequency of 4 GHz are calculated, simulated, and shown in Fig. 11. It can be seen that although a higher $A_{\rm VM}$ reduces the noise contribution of M_1+M_4 and R_t (R_b, R_{L1}, and R_{L2}), it damages the noise-cancelling condition and increases the noise from M_2 and M_3. The optimal $A_{\rm VM}$ can be obtained by equalizing its derivative to zero, as shown by (14) at the bottom of the page. The value of $A_{\rm VM}$ chosen around 2.5 is suitable for NF optimization at high frequency according to the calculation and simulation.

C. Linearity Analysis and Distortion Cancellation

To calculate the third-order input intercept point (IIP3) of the LNA, it is assumed that the RF input signal of the LNA consists of two closely spaced signals at frequencies of ω_1 and ω_2 both with an amplitude of v_s. Thus, due to the third-order nonlinearity in the LNA, the third-order intermodulation product (IM3) at frequencies of $(2\omega_1-\omega_2)$ and $(2\omega_2-\omega_1)$ are generated. The calculation of the IIP3 of the LNA is divided into two steps: 1) Calculate and simulate the second- and third-order nonlinear currents generated by each transistor, and 2) calculate the transfer function of the nonlinear current to the output voltage.

$$\left.\frac{\partial\left(\overline{v_{n,M_1}^2}+\overline{v_{n,M_4}^2}+\overline{v_{n,M_2}^2}+\overline{v_{n,M_3}^2}+\overline{v_{n,R_b}^2}+\overline{v_{n,R_{L1}}^2}+\overline{v_{n,R_{L2}}^2}+\overline{v_{n,R_S}^2}\right)\Big/\overline{v_{n,R_S}^2}}{\partial A_{\rm VM}}\right|_{\omega=\omega_h}=0 \tag{14}$$

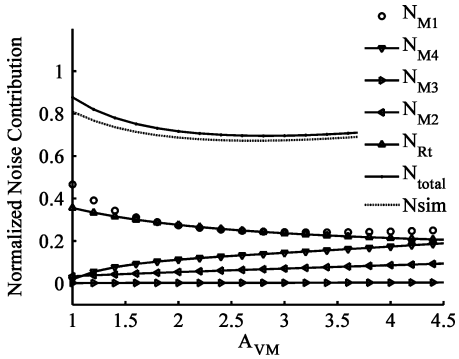

Fig. 11. Relationship between the noise contribution of transistors and resistors and $A_{\rm VM}$ at 4 GHz (normalized to the noise contribution by R_S). $A_{\rm VM}$ is varied with constant power and supply voltage, under the conditions of input impedance matching (6) and gain balance (8).

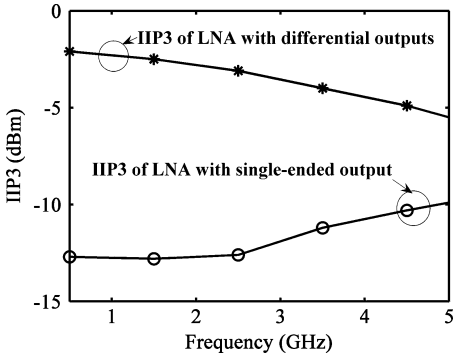

Fig. 12. Comparison of simulated IIP3 values between the LNA with differential outputs and that with single-ended output.

1) Nonlinearity of a Single Transistor: To analyze the nonlinearity of the whole circuit, the nonlinearity of a single transistor is studied first. Generally, it is assumed that the distortion mainly comes from the nonlinearity of the transconductance, while the distortion from the nonlinearity of output conductance is omitted for simplicity. It is found in the simulation that this assumption is not quite accurate when a large resistor is applied as load. With the nonlinearity of the output conductance and the cross terms taken into account, the drain current $i_{\rm ds}$ can be expressed as a 2-D Tailor approximation [18], [19]

$$\begin{aligned} i_{\rm ds} = {} & g_m v_{\rm gs} + K_{2g_m} v_{\rm gs}^2 + K_{3g_m} v_{\rm gs}^3 + g_o v_{\rm ds} + K_{2g_o} v_{\rm ds}^2 \\ & + K_{3g_o} v_{\rm ds}^3 + K_{2g_m g_o} v_{\rm gs} v_{\rm ds} + K_{32g_m g_o} v_{\rm gs}^2 v_{\rm ds} \\ & + K_{3g_m 2g_o} v_{\rm gs} v_{\rm gs}^2 \end{aligned} \tag{15}$$

where g_m and g_o are the linear transconductance and output conductance, respectively. K_{2g_m}, K_{3g_m}, K_{2g_o}, and K_{3g_o} are the second- and third-order nonlinear transconductance and output conductance. $K_{2g_m g_o}$, $K_{32g_m g_o}$, and $K_{3g_m 2g_o}$ are the second- and third-order cross terms. This expression has two input variables ($v_{\rm gs}$ and $v_{\rm ds}$); therefore, it is complicated to analyze the whole circuit. If the load is a linear resistor (R_L), $v_{\rm ds}$ can be substituted by $-i_{\rm ds}R_L$. Substituting this into (15), an implicit function of $i_{\rm ds}$ about $v_{\rm gs}(i_{\rm ds} = f(v_{\rm gs}, i_{\rm ds}))$ can be obtained. Then, $i_{\rm ds}$ can be expressed in a Tailor expansion of $v_{\rm gs}$

$$i_{\rm ds} = K_1 v_{\rm gs} + K_2 v_{\rm gs}^2 + K_3 v_{\rm gs}^3 \tag{16}$$

where

$$K_1 = g_m (1 + R_L g_o)^{-1} \tag{17}$$

$$\begin{aligned} K_2 = {} & \left(K_{2g_m} + K_{2g_o} K_1^2 R_L^2 - K_{2g_m g_o} K_1 R_L\right) \\ & \times (1 + R_L g_o)^{-1} \end{aligned} \tag{18}$$

$$\begin{aligned} K_3 = {} & \left(K_{3g_m} - K_{3g_o} K_1^3 R_L^3 + 2K_{2g_o} K_1 K_2 R_L^2 \right. \\ & - K_{2g_m g_o} K_2 R_L + K_{3g_m 2g_o} K_1^2 R_L^2 \\ & \left. - K_{32g_m g_o} K_1 R_L\right)(1 + R_L g_o)^{-1}. \end{aligned} \tag{19}$$

These coefficients can be obtained through circuit simulation after the circuit topology and dc bias are specified.

2) Nonlinearity of the LNA: The main distortion comes from four transistors, namely, M_2, M_3, M_1, and M_4. The IM3 currents due to the four transistors can be modeled by three current sources, i.e., $i_{2\omega 1-\omega 2,M2}$, $i_{2\omega 1-\omega 2,M3}$, and $i_{2\omega 1-\omega 2,M1\&M4}$ (the combination of the IM3 current of M_1 and M_4). Two kinds of cancellation scheme are used to reduce their contribution to IM3.

3) Distortion Cancellation by Transfer Function: The transfer functions of $i_{2\omega 1-\omega 2,M2}$ and $i_{2\omega 1-\omega 2,M3}$ to the differential outputs are equal to zero ideally as a result of distortion cancellation. The mechanism of distortion cancellation is the same as the noise cancellation, observing that the distortion current can also be modeled as a current source connected between the drain and source nodes [16]. Based on the transfer functions [(A10) and (A16) in Appendix A], the output IM3 voltage due to M_2 and M_3 can be expressed as

$$\begin{aligned} & v_{{\rm out},2\omega_1-\omega_2,M_2} \\ & \quad = i_{2\omega_1-\omega_2,M_2} TF_{i_2 \to v_{\rm out}} \\ & \quad = i_{2\omega_1-\omega_2,M_2} \frac{1}{2}\left(R_{L1} - R_s(g_{m1} + g_{m4})R_{L2}\right) \end{aligned} \tag{20}$$

$$\begin{aligned} & v_{{\rm out},2\omega_1-\omega_2,M_3} \\ & \quad = i_{2\omega_1-\omega_2,M_3} TF_{i_3 \to v_{\rm out}} \\ & \quad = i_{2\omega_1-\omega_2,M_3} \frac{T}{1+T}\left(\frac{R_{L1}}{R_s(g_{m1} + g_{m4})} - R_{L2}\right) \end{aligned} \tag{21}$$

where T is the loop transmission, which is defined in (A1). The IM3 voltages from M_2 and M_3 can be cancelled totally with balanced differential outputs. The IIP3 values of the LNA with cancellation (differential outputs) and that without cancellation (single-ended output) are simulated as shown in Fig. 12. The effect of cancellation is deteriorated at a high frequency due to phase shift, which is similar to noise cancellation.

4) Second-Order Distortion Cancellation of NMOS–PMOS Pair: The distortion from M_1 and M_4 cannot be cancelled by the transfer function. The IM3 current $i_{2\omega 1-\omega 2,M1\&M4}$ has two origins. The first one is from the third nonlinear coefficient $K_{3,M1\&M4}$ of M_1 and M_4. The second one is caused by the second-order nonlinear coefficient $K_{2,M1\&M4}$ of M_1 and M_4 in the feedback loop. The second-order nonlinear currents of M_2 and M_3 ($i_{2\omega 1,M2}$ and $i_{2\omega 1,M3}$) will generate second-order voltages $v_{X,2\omega 1,M2}$ and $v_{X,2\omega 1,M3}$ at the gates of M_1 and M_4 due to the loop transmission, which, together with the signal $v_{X,\omega 2}$, would produce a third-order nonlinearity through the

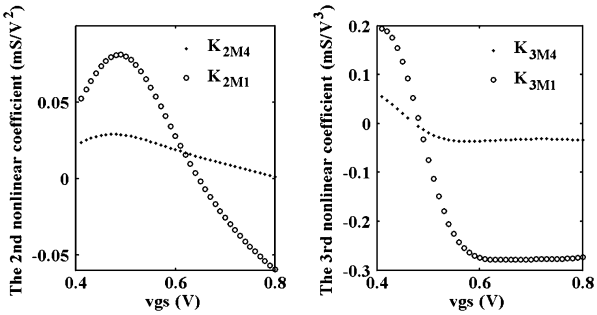

Fig. 13. Second and third nonlinear coefficients of nMOS (M_1) and pMOS (M_4).

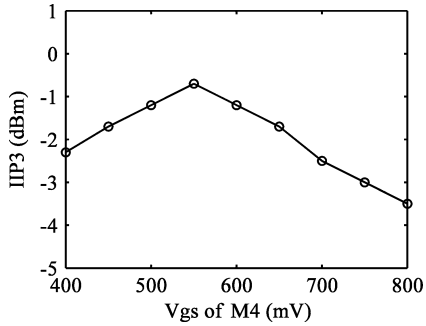

Fig. 14. Simulated IIP3 versus dc bias $V_{\rm gs}$ of M_4 at 1 GHz.

second-order nonlinear coefficient of the CS transistors (M_1 and M_4). The output IM3 voltage can be expressed as

$$v_{\text{out},2\omega_1-\omega_2,M_1\&M_4} = TF_{i1\to v_{\text{out}}}\left(\frac{3K_{3,M_1\&M_4}}{4}v_{X,\omega 1}^3 + K_{2,M_1\&M_4}v_{X,\omega 1} \times \left(v_{\text{X},2\omega 1,M_2} + v_{X,2\omega_1,M_3} + v_{X,2\omega 1,M_1\&M_4}\right)\right) \quad (22)$$

where

$$v_{X,2\omega_1,M_2} = \frac{Z_s(j2\omega_1)}{2}i_{2\omega_1,M_2} = \frac{Z_s(j2\omega_1)}{4}K_{2,M_2}(1+A_{\text{VM}})^2 v_{X,\omega_1}^2 \quad (23)$$

$$v_{X,2\omega_1,M_3} = \frac{T(j2\omega_1)}{K_{1,M_1\&M_4}(1+T(j2\omega_1))}i_{2\omega_1,M_3} = \frac{T(j2\omega_1)}{2K_{1,M_1\&M_4}(1+T(j2\omega_1))}K_{2,M_3}A_{\text{VM}}^2 v_{X,\omega_1}^2 \quad (24)$$

$$v_{X,2\omega_1,M_1\&M_4} = \frac{T(j2\omega_1)}{2K_{1,M_1\&M_4}(1+T(j2\omega_1))}K_{2,M_1\&M_4}v_{X,\omega_1}^2. \quad (25)$$

Expression (22) can be simplified as

$$v_{\text{out},2\omega_1-\omega_2,M_1\&M_4} = v_{\text{X},\omega_1}^3 TF_{i1\to v_{\text{out}}}p_3 \times \left(K_{3,M_1\&M_4} + K_{2,M_1\&M_4} \times (p_1K_{2,M_2} + p_2K_{2,M_3}) + p_4K_{2,M_1\&M_4}^2\right) \quad (26)$$

where p_1, p_2, p_3, and p_4 are loop-related parameters.

The second term in (26) has a relatively higher proportion than the first one because of the large second nonlinear current of M_2 and M_3. Similar to the differential pair, the NMOS–PMOS pair has a characteristic of second-nonlinear-coefficient cancellation [20] as shown in

$$\begin{aligned} i_{\text{out}} &= i_{\text{ds},n} + i_{\text{ds},p} \\ &= \left(K_{1,M_1}v_X + K_{2,M_1}v_X^2 + K_{3,M_1}v_X^3\right) \\ &\quad - \left(K_{1,M_4}(-v_X) + K_{2,M_4}(-v_X)^2 + K_{3,M_4}(-v_X)^3\right) \\ &= \left(K_{1,M_1} + K_{1,M_4}\right)v_X + \left(K_{2,M_1} - K_{2,M_4}\right)v_X^2 \\ &\quad + \left(K_{3,M_1} + K_{3,M_4}\right)v_X^3 \\ &= K_{1,M_1\&M_4}v_X + K_{2,M_1\&M_4}v_X^2 + K_{3,M_1\&M_4}v_X^3. \end{aligned} \quad (27)$$

$K_{2,M1\&M4}$ can be adjusted to zero if the second nonlinearities of M_1 and M_4 cancel each other. The second and third nonlinear coefficients of nMOS and pMOS are simulated and shown in Fig. 13. It can be seen that the pMOS has a much lower K_3 than that of the NMOS. Thus, M_4 can be regarded as an auxiliary transistor to cancel the second-order nonlinearity of nMOS with minor impact on the third-order nonlinearity. It is expected to cancel $K_{2,M1}$ by adjusting the bias and size of M_4 with the current slightly changed. Furthermore, it is found in the simulation that the first and second terms in the first bracket of (26) have opposite signs and that the minimum IM3 can be achieved when they cancel each other. Simulation demonstrates about a 3-dB improvement by optimizing the gate bias of M_4, as shown in Fig. 14.

IV. Circuit Design and Implementation

The design flow of the inductorless wideband LNA under voltage and power constraints is described briefly as follows. The value of A_{VM} is to be decided first, considering the target of the NF and the bandwidth requirement. Then, the g_m and the current of the CG stage are set according to the input impedance matching condition expressed in (6). The current of M_1 is determined under the power constraint. Next, size the cascode transistor M_3 and pMOS M_4 and sweep and choose a proper gate bias of M_1 and M_4 to minimize the value of (26) while satisfying the expression for the open-loop gain of (4). Last, the load resistors R_{L1} and R_{L2} are chosen to achieve a proper gain in the desired bandwidth. Their ratio should satisfy (8) to realize the cancellation of the noise and distortion. The cascode transistor M_5 can be removed for even lower voltage applications because it is found in the simulation that the high output resistance of small transistor M_2 has provided high reverse isolation. The design values of the LNA are summarized in Table I.

In this design, the 0.2–4-GHz wideband noise-cancelling LNA was designed in a 0.13-μm CMOS technology, as shown in Fig. 15. The supply voltage was chosen as 1 V to validate the performance of the LNA under low voltage. MIM capacitors and polyresistors are used for ac coupling and dc bias. The LNA was protected by electrostatic-discharge diodes. The bond-wire inductance and external capacitance together with input capacitance constituted a third-order π network to approximately achieve a maximum flat transfer function [3]. To facilitate measurements, two source followers with 50-Ω output resistance are added to the differential outputs of the LNA as buffers. In order to achieve reliable IIP3 measurement results,

TABLE I
DESIGN VALUES OF THE LNA

M1	2μm/0.13μm × 40	R_{L1}	300Ω
M2	2μm/0.13μm × 6	R_{L2}	120Ω
M3	2μm/0.13μm × 20	R_b	800Ω
M4	2μm/0.13μm × 36	$C_{b1,2,3}$	10pF
$M_{buf1,2}$	2μm/0.13μm × 20	I_1	0.5mA
A_{VM}	2.5	I_2	5.2mA

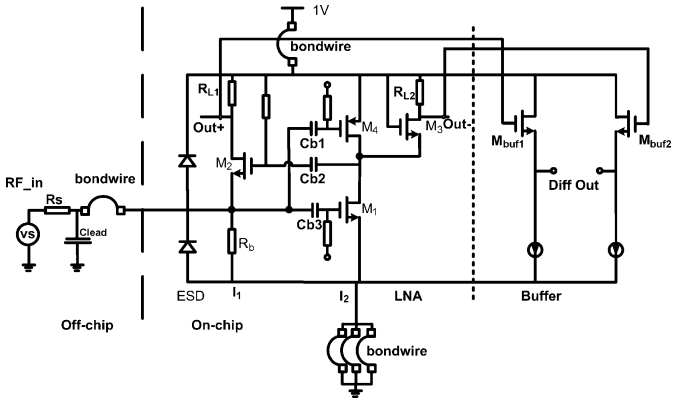

Fig. 15. Complete schematic of the proposed LNA (including buffer).

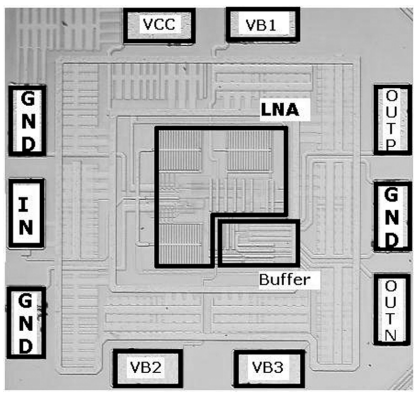

Fig. 16. Microphotograph of the LNA.

the buffers were designed to have a high overdrive voltage. The chip microphotograph, as shown in Fig. 16, occupies an area of $560 \times 520\ \mu\text{m}^2$, while the LNA core is only about $180 \times 140\ \mu\text{m}^2$. For some applications, full differential operation is preferred to eliminate parasitic effects. The differential LNA can be realized from the proposed topology directly by replicating the circuit for the other half. The four outputs can be reduced to two by combining the currents with the same polarity [13], as shown in Fig. 17.

V. EXPERIMENTAL RESULTS

The LNA has been fabricated in TSMC 0.13-μm CMOS process and is mounted on a printed circuit board (PCB) for measurement. The pads of input, output, and bias are all connected to the PCB by bond wires. To facilitate single-ended measurement, a wideband off-chip balun is employed to convert the differential outputs to the single-ended output.

The measured S-parameters of the LNA are shown in Fig. 18. Because of the wideband impedance matching provided by the

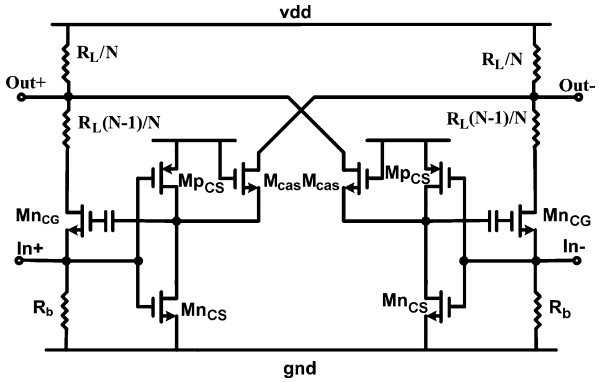

Fig. 17. Full differential version of the proposed LNA.

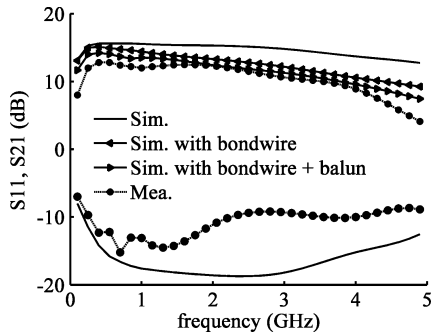

Fig. 18. Measured and simulated S-parameters of the proposed LNA.

CG FET, the measured S_{11} remains below -9 dB up to 5 GHz. Measured power gain (S21) achieves a maximum of 13-dB gain at 600 MHz and remains at a 3-dB flatness from 0.2 to 3.8 GHz. The measured power gain is about 2.6–4.8 dB lower than the simulated S_{21} across the band. To investigate this discrepancy, the impact of the VDD and GND bond wires and off-chip balun are also taken into consideration and simulated, as shown in Fig. 18. The inductances of bond wires and the coupling between them complicate the analysis. Therefore, a 3-D electromagnetic simulator HFSS is utilized to obtain the S-parameter of bond wires. Then, their Sp model is incorporated into the LNA for circuit simulation. Simulation demonstrates that the degeneration of M_1 by three GND bond wires and that of M_4 by one VDD bond wire cause as high as a 3.4-dB loss at 4 GHz. In practical use, the LNA will be followed by an on-chip mixer with voltage-type inputs, and matching to 50 Ω at the outputs is not needed. Hence, the actual voltage gain is 6 dB higher than that of S_{21} due to the voltage halving at the matched outputs. Thus, the actual voltage gain would have reached 19 dB. Fig. 19 shows that the measured NF is below 3.4 dB from 200 MHz to 3.8 GHz. Although it is about 1 dB higher than the simulated NF, the shape and the flatness of the curve are almost the same as the simulated one. Hence, it can be believed to reflect the actual NF of the LNA. The effect of VDD/GND bond wires is not quite notable. The underestimation of the thermal noise of the FET models (BSIM3) and the loss near the input port of the LNA may account for the discrepancy. The IIP3 of the LNA is measured at 900 M, 2 GHz, and 3 GHz, as shown in Fig. 20. As the frequency increases, the distortion cancellation is deteriorated by the large phase shift. Therefore, the IIP3 drops from

TABLE II
PERFORMANCE COMPARISON OF RECENTLY PUBLISHED WIDEBAND LNAS

Ref	JSSC06 [3]	CICC05 [11]	ISSCC07 [7]	JSSC08 [22]	JSSC08 [12]	RFIC05 [24]	ISSCC06 [6]	ISSC07 [8]	This work	
Process (nm)	90	130	90	130	65	130	90	130	130	
Frequency (GHz)	0.8-6	0.9-5	0-6	0.8-2.1	0.2-5.2	0.1-0.9	0.5-8.2	1-7	0.2-3.8	0.2-3.8
S11 (dB)	<-10	<-10	<-10	<-15	<-10	<-10	<-10	<-10	<-9	<-9
Gain (dB)	20^{VG}	19^{VG}	17.4^{PG}	14.5^{PG}	15.6^{VG}	13^{VG}	25^{VG}	17^{VG}	19^{VG**}	14.8^{VG**}
NF (dB)	3.5	3.5	2.5	2.5	3.5	4	2.6	2.4	2.8-3.4	3.5-4.1
IIP3 (dBm)	-3.5	1	-10	16	0	-10.2	-16	-4.1	-4.2	-3.8
Supply (V)	2.5	1.8	1.2	1.5	1.2	1.2	2.7	1.4	1	0.85
Power (mW)	12.5	12	9.8	17.4	20	0.72	42	25	5.7	3.2
No. of inductors	2	4	0	0	0	0	0	0	0	

VG: Voltage gain.
PG: Power gain.
** The insertion loss (6 dB) from the buffer is deembedded.

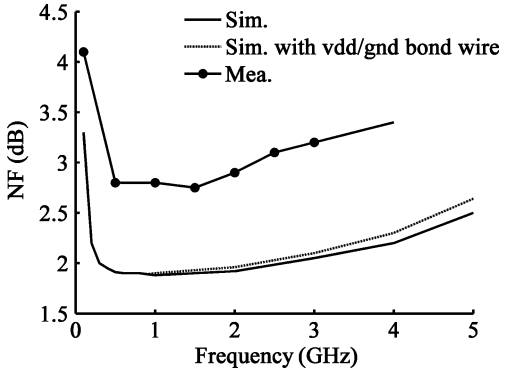

Fig. 19. Measured and simulated NFs of the proposed LNA.

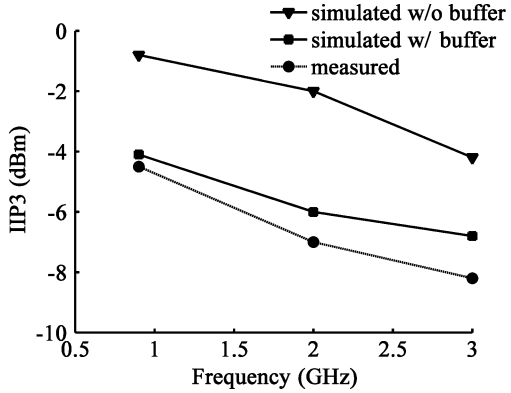

Fig. 20. Measured and simulated IIP3 values of the proposed LNA.

−4.4 to −8 dB. Due to the limitation of the nonlinear buffer, the measured IIP3 is about 4 dB lower than the simulated one without the buffer.

Table II summarizes the performance of the proposed LNA along with published results. The measured performances at 1- and 0.85-V supplies are both given. Due to the limitation of the process and the pursuit of high gain, the 3-dB bandwidth of this design is not as wide as some other designs. However, without the use of on- or off-chip inductors, our proposed LNA can achieve comparable NF and voltage gain at the lowest power consumption and under the lowest voltage among all the designs except that of [24], which is designed for subgigahertz applications.

VI. CONCLUSION

In this paper, a wideband noise-cancelling LNA without the use of on- or off-chip inductors has been designed for low-voltage low-power applications. To alleviate the conflict between supply voltage, power, and NF in previous inductorless LNA designs, a local negative feedback is introduced between the CG and CS stages. The NF is optimized by distributing the power consumption among all components according to their contribution to the NF. The linearity is improved by utilizing two kinds of distortion-cancelling techniques through the transfer function and second-order distortion cancellation of the NMOS–PMOS pair, respectively. Fabricated in a TSMC 0.13-μm RF-CMOS process, the LNA achieves a voltage gain of 19 dB and an NF of 2.8–3.4 dB over a −3-dB bandwidth of 0.2–3.8 GHz. It consumes 5.7 mW from a 1-V supply and occupies an active area of only 0.025 mm^2. Benefiting from the technique introduced in this paper, the proposed LNA achieves comparable and even better NF and gain than those of reported inductorless LNAs at even lower power consumption and lower supply voltage.

APPENDIX A
DERIVATION OF THE TRANSFER FUNCTION

The noise or distortion current i_p of a transistor M_i can be modeled as a current source i_{p,M_i} connected with its drain and source. The transfer functions of these current sources to the output voltages can be derived to help in the NF and distortion analyses. The output conductance g_o and substrate transconductance g_{mb} are neglected for simplicity.

1) Loop Transmission T [as shown in Fig. 21(a)]: According to the theory of feedback [25], the loop is broken at node M,

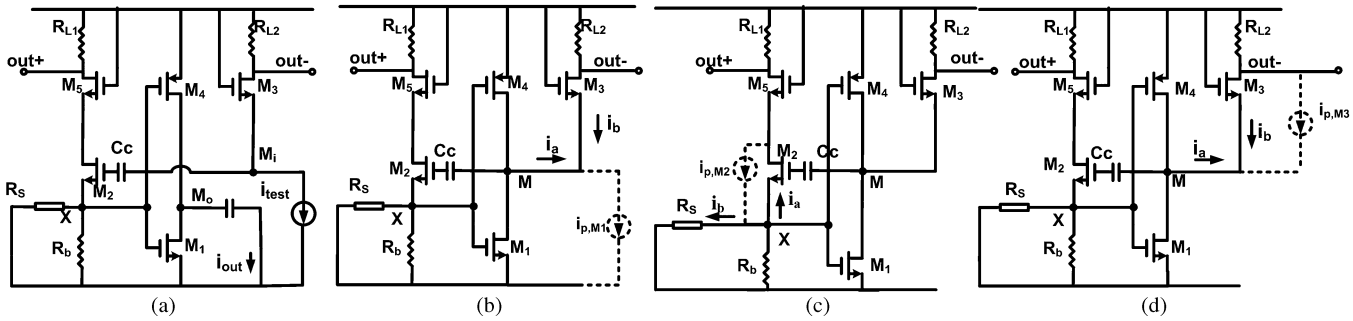

Fig. 21. Equivalent circuits for derivation of transfer function. (a) Loop transmission T. (b) $TF_{i_1\to v_{\rm out}}$. (c) $TF_{i_2\to v_{\rm out}}$. (d) $TF_{i_3\to v_{\rm out}}$.

which is split into two nodes: M_i and M_o. Then, a test current is applied at node M_i to measure the ac short-circuit current at node M_o. The loop transmission can be obtained as

$$T=\frac{i_{\rm out}}{i_{\rm test}}=\frac{g_{m2}R_s}{1+g_{m2}R_s}\frac{g_{m1}+g_{m4}}{g_{m3}}=\frac{A_{\rm VM}}{A_{\rm VM}+2}. \quad \text{(A1)}$$

2) $TF_{i_1\to v_{\rm out}}$ and $TF_{i_4\to v_{\rm out}}$ [as shown in Fig. 21(b)]: The current in parallel with M_1 is denoted by i_{p,M_1}. As shown in Fig. 21(b), the following can be obtained:

$$i_{p,M1}=i_b+i_a \quad \text{(A2)}$$
$$i_a=i_bT. \quad \text{(A3)}$$

Therefore, $i_b=i_{p,M_1}/(1+T)$ and $i_a=i_{p,M_1}T/(1+T)$.

The output noise voltage can be derived as

$$\begin{aligned} v_{{\rm out},M_1}&=v_{\rm out+}-v_{\rm out-}\\ &=\frac{i_a}{(g_{m1}+g_{m4})R_s}R_{L1}-(-i_bR_{L2})\\ &=\frac{i_{p,M_1}}{1+T}\left(T\frac{R_{L1}}{(g_{m1}+g_{m4})R_S}+R_{L2}\right). \end{aligned} \quad \text{(A4)}$$

Observing the symmetry between M_1 and M_4, it is easy to obtain the transfer functions of M_1 and M_4 as

$$\begin{aligned} TF_{i_1\to v_{\rm out}}&=TF_{i_4\to v_{\rm out}}=\frac{v_{{\rm out},M_1}}{i_{p,M_1}}\\ &=\frac{1}{1+T}\left(T\frac{R_{L1}}{(g_{m1}+g_{m4})R_S}+R_{L2}\right). \end{aligned} \quad \text{(A5)}$$

Under the condition of gain balance (8), (A5) can be simplified as

$$TF_{i_1\to v_{\rm out}}=TF_{i_4\to v_{\rm out}}=\frac{R_{L1}}{(g_{m1}+g_{m4})R_S}=R_{L2}. \quad \text{(A6)}$$

3) $TF_{i_2\to v_{\rm out}}$ [as shown in Fig. 21(c)]: The current i_{p,m_2} couples to both out+ and out−

$$i_{p,M_2}=i_a+i_b \quad \text{(A7)}$$
$$\begin{aligned} i_a&=(v_X-v_M)g_{m2}\\ &=\left(i_bR_S+\frac{i_bR_S(g_{m1}+g_{m4})}{g_{m3}}\right)g_{m2}\\ &=i_bR_S(A_{\rm VM}+1)g_{m2}=i_b. \end{aligned} \quad \text{(A8)}$$

The output voltage can be expressed as

$$v_{{\rm out},M_2}=\frac{i_{p,M_2}}{2}\left(R_{L1}-R_S(g_{m1}+g_{m4})R_{L2}\right). \quad \text{(A9)}$$

Hence

$$TF_{i_2\to v_{\rm out}}=\frac{1}{2}\left(R_{L1}-R_S(g_{m1}+g_{m4})R_{L2}\right). \quad \text{(A10)}$$

$\epsilon_{\rm mis}$ is defined to depict the gain imbalance of the differential outputs due to mismatch

$$\begin{aligned} \epsilon_{\rm mis}&=\frac{|Gain_{\rm CG}-Gain_{\rm CS}|}{(Gain_{\rm CG}+Gain_{\rm CS})/2}\\ &=\frac{\left|\frac{R_{L1}}{R_S}-(g_{m1}+g_{m4})R_{L2}\right|}{\left(\frac{R_{L1}}{R_S}+(g_{m1}+g_{m4})R_{L2}\right)/2}\\ &\approx\frac{|R_{L1}-R_S(g_{m1}+g_{m4})R_{L2}|}{R_S(g_{m1}+g_{m4})R_{L2}}. \end{aligned} \quad \text{(A11)}$$

Therefore

$$TF_{i_2\to v_{\rm out}}=\frac{1}{2}R_S(g_{m1}+g_{m4})R_{L2}\epsilon_{\rm mis}. \quad \text{(A12)}$$

4) $TF_{i_3\to v_{\rm out}}$ [as shown in Fig. 21(d)]: Without feedback, the noise contribution from M_3 can be neglected because of the high impedance degeneration provided by the output resistance $(r_{\rm ds1})$ of M_1. However, the feedback reduces the degeneration impedance, and the current $i_{p,M3}$ couples to both out+ and out−

$$i_{p,M3}=-(i_b+i_a) \quad \text{(A13)}$$
$$i_a=+i_bT. \quad \text{(A14)}$$

The output voltage of M_3 can be obtained as

$$\begin{aligned} v_{{\rm out},M_3}&=v_{\rm out+}-v_{\rm out-}\\ &=\frac{i_a}{(g_{m1}+g_{m4})R_s}R_{L1}-i_aR_{L2}\\ &=\frac{i_{p,M_3}}{1+T}T\left(\frac{R_{L1}}{(g_{m1}+g_{m4})R_S}-R_{L2}\right) \end{aligned} \quad \text{(A15)}$$
$$\begin{aligned} TF_{i_3\to v_{\rm out}}&=\frac{1}{1+T}T\left(\frac{R_{L1}}{(g_{m1}+g_{m4})R_S}-R_{L2}\right)\\ &=\frac{1}{1+T}TR_{L2}\epsilon_{\rm mis}. \end{aligned} \quad \text{(A16)}$$

5) $TF_{v_s \to v_{\text{out}}}$*:*

$$\frac{v_{\text{out,vs}}}{v_X} = \frac{R_{L1}}{R_S} + (g_{m1} + g_{m4})R_{L2}. \tag{A17}$$

Under the condition of input impedance matching, the following can be given:

$$v_s = 2v_X. \tag{A18}$$

Therefore

$$\begin{aligned} TF_{\text{vs}\to v_{\text{out}}} &= \frac{v_{\text{out,vs}}}{v_s} = \frac{v_{\text{out,vs}}}{2v_X} \\ &= \frac{1}{2}\left(\frac{R_{L1}}{R_S} + (g_{m1} + g_{m4})R_{L2}\right) \\ &= \frac{R_{L1}}{R_S} = (g_{m1} + g_{m4})R_{L2}. \end{aligned} \tag{A19}$$

APPENDIX B
NOISE FACTOR ANALYSIS OF THE PROPOSED LNA

It is assumed that the noise mainly comes from the thermal noise of resistors and the channel thermal noise of transistors, which can be expressed as

$$\overline{v_{n,R_i}^2} = 4kTR_i \tag{B1}$$

$$\overline{i_{n,M_i}^2} = 4kT\gamma/\alpha g_{mi}. \tag{B2}$$

The noise factor can be expressed as the division of the total equivalent mean-square output noise voltage and that caused by the source resistance (R_S), as shown in (B3) at the bottom of the page. Using the transfer function derived in Appendix A, the equivalent mean-square output noise voltage of transistors and resistors can be calculated, e.g.,

$$\overline{v_{n,\text{out},M_1}^2} = 4kT\gamma_1/\alpha_1 g_{m1}\left(TF_{i_1\to v_{\text{out}}}\right)^2. \tag{B4}$$

Finally, the noise factor is deduced as

$$\begin{aligned} F = 1 &+ \frac{\gamma_1}{\alpha_1}\frac{g_{m1}}{(g_{m1}+g_{m4})^2 R_s} + \frac{\gamma_4}{\alpha_4}\frac{g_{m4}}{(g_{m1}+g_{m4})^2 R_s} \\ &+ \frac{1}{R_s(g_{m1}+g_{m4})^2 R_{L2}} + \frac{R_s}{R_b} + \frac{R_s}{R_{L1}} \\ &+ \frac{\gamma_3}{\alpha_3}\frac{1}{4R_s g_{m3}(1+A_{\text{VM}})^2}\epsilon_{\text{mis}}^2 + \frac{\gamma_2}{\alpha_2}\frac{1}{4(1+A_{\text{VM}})}\epsilon_{\text{mis}}^2. \end{aligned} \tag{B5}$$

APPENDIX C
PHASE-SHIFT CALCULATION

The transfer function should take the parasitic capacitance and bond-wire inductance into account at high frequency as shown in the following:

$$\begin{aligned} TF_{i2\to v_{\text{out}}} &= \frac{v_{\text{out}}(j\omega)}{i_2} = \frac{v_{\text{out}+}(j\omega) - v_{\text{out}-}(j\omega)}{i_2} \\ &= \frac{1}{1+k}\left(\frac{R_{L1}}{1+j\omega R_{L1}C_{\text{out}+}} - \frac{R_S}{1+j\omega R_S C_X}(G_{m1}+G_{m4})\right. \\ &\qquad \left.\times\frac{g_{m3}}{g_{m3}+j\omega C_M}\frac{R_{L2}}{1+j\omega R_{L2}C_{\text{out}-}}\right) \end{aligned} \tag{C1}$$

where $k = Z_S g_{m2}(1+((G_{m1}+G_{m4})/y_{m3}))$ and $k = 1$ at low frequency

$$\begin{aligned} TF_{i3\to v_{\text{out}}} &= \frac{v_{\text{out}}(j\omega)}{i_3} = \frac{v_{\text{out}+}(j\omega) - v_{\text{out}-}(j\omega)}{i_3} \\ &= \frac{T(j\omega)}{(1+T(j\omega))}\left(\frac{1+j\omega R_S C_X}{(G_{m1}+G_{m4})R_S}\frac{R_{L1}}{1+j\omega R_{L1}C_{\text{out}+}}\right. \\ &\qquad \left.-\frac{g_{m3}}{g_{m3}+j\omega C_M}\frac{R_{L2}}{1+j\omega R_{L2}C_{\text{out}-}}\right) \end{aligned} \tag{C2}$$

where $T(j\omega)$ is the loop transmission of the local negative feedback and can be expressed as

$$T(j\omega) = \frac{g_{m2}Z_S}{1+g_{m2}Z_s}\frac{G_{m1}+G_{m4}}{y_{m3}} \tag{C3}$$

in which

$$Z_s = \frac{R_S}{1+j\omega R_S C_X} \tag{C4}$$

$$y_{m3} = g_{m3} + j\omega C_M \tag{C5}$$

where C_X and C_M are parasitic capacitances at nodes X and M, respectively, and

$$G_{m1} = \frac{g_{m1}}{1+jg_{m1}\omega L_{\text{gnd}}} \tag{C6}$$

$$G_{m4} = \frac{g_{m4}}{1+jg_{m4}\omega L_{\text{vdd}}}. \tag{C7}$$

According to the design value, the following approximation is taken:

$$\frac{L_{\text{vdd}}}{L_{\text{gnd}}} \approx \frac{g_{m1}}{g_{m4}} = 3. \tag{C8}$$

$$F = 1 + \frac{\overline{v_{n,\text{out},M_1}^2} + \overline{v_{n,\text{out},M_4}^2} + \overline{v_{n,\text{out},R_{L2}}^2} + \overline{v_{n,\text{out},R_{L1}}^2} + \overline{v_{n,\text{out},R_b}^2} + \overline{v_{n,\text{out},M_3}^2} + \overline{v_{n,\text{out},M_2}^2}}{\overline{v_{n,\text{out},R_S}^2}} \tag{B3}$$

$$\omega_X = \frac{1}{R_s\left(C_{\mathrm{gs}M_1} + C_{\mathrm{gs}M_4} + (1+A_{\mathrm{VM}})\left(C_{\mathrm{gd}M_1} + C_{\mathrm{gd}M_4}\right) + C_{\mathrm{esd+pad}}\right)} \tag{C11}$$

Therefore

$$G_{m1} + G_{m4} = \frac{g_{m1} + g_{m4}}{1 + j g_{m1} \omega L_{\mathrm{gnd}}}. \tag{C9}$$

The phase shift can be extracted approximately as

$$\phi_{\mathrm{dif}} = \mathrm{atan}\left(\frac{\omega}{\omega_X}\right) + \mathrm{atan}\left(\frac{\omega}{\omega_M}\right) + \mathrm{atan}\left(\frac{\omega}{\omega_{\mathrm{bw}}}\right) + \mathrm{atan}\left(\frac{\omega}{\omega_{L1}}\right) - \mathrm{atan}\left(\frac{\omega}{\omega_{L2}}\right) \tag{C10}$$

where ω_X is expressed as (C11), as shown at the top of the page, and

$$\omega_M = \frac{g_{m3}}{C_{\mathrm{gd}M_1} + C_{\mathrm{gd}M_4} + C_{\mathrm{db}M_1} + C_{\mathrm{db}M_4} + C_{\mathrm{gs}M_3}} \tag{C12}$$

$$\omega_{\mathrm{bw}} = \frac{1}{g_{m1} L_{\mathrm{gnd}}} \tag{C13}$$

$$\omega_{L1} = \frac{1}{R_{L1}\left(C_{L1} + C_{\mathrm{db}M_5} + C_{\mathrm{gd}M_5}\right)} \tag{C14}$$

$$\omega_{L2} = \frac{1}{R_{L2}\left(C_{L2} + C_{\mathrm{db}M_3} + C_{\mathrm{db}M_3}\right)}. \tag{C15}$$

It can be seen in (C11) and (C12) that a small A_{VM} is preferred to increase the bandwidths ω_X and ω_M which contribute mostly to the phase shift.

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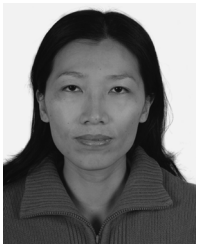

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