An Overview of Sigma Delta ADCs and DAC Devices

R.W. Stewart [1]

Abstract

In this paper we present a review and intuitive introduction to oversampling DSP techniques and the theory and advantages of sigma delta ($\Sigma-\Delta$) devices for digital to analog conversion (DAC) and analogue to digital conversion (ADC). The paper initially introduces conventional Nyquist sampling rate DSP, followed by an overview of decimation, interpolation, and a discussion of the advantages of using oversampling to reduce the anti-alias and reconstruction filter specifications. It is then discussed why oversampling can be used to increase the resolution of an N-bit signal to N+1 bits, by sampling at 4 x's the Nyquist rate to reduce the in-band ADC quantisation noise. Sigma-delta ($\Sigma-\Delta$) noise shaping techniques are then introduced and a brief overview of some currently available devices is presented. Finally we comment on a few of the active research areas related to $\Sigma-\Delta$ devices.

1. Introduction

Over the last few years sigma-delta ($\Sigma-\Delta$) analogue to digital converters (ADC) and digital to analogue converters (DACs) have become widely available, particularly for low frequency applications such as high fidelity audio, speech processing, metering applications and voiceband data telecommunications [2], [3], [6], [9], [25]. One of the key advantages of $\Sigma-\Delta$ ADCs is that they do not require high precision and accurately trimmed analogue components. In fact the circuitry for a $\Sigma-\Delta$ ADC only requires analogue components of a comparator and an integrating component. As a result $\Sigma-\Delta$ ADC and DAC devices can be implemented with CMOS circuitry, and hence mixed analog/digital DSP microprocessors can be realised using 1-2µm technologies. These small geometries are necessary to accommodate the relatively large chip area occupied by the interpolating and decimating digital filters required for $\Sigma-\Delta$ DACs and ADCs. Semiconductor geometries below 1µm will make on DSP-chip $\Sigma-\Delta$ devices even more attractive and available.

As examples of current technology, $\Sigma-\Delta$ DAC devices of between 16 and 20 bits resolution for hifidelity audio applications are achievable [2], [3], [6], [8], [9], [13]. 24 bits of resolution is also possible for low frequency biomedical signal analysis ADCs.

$\Sigma-\Delta$ devices are based on *oversampling techniques*, and on (quantisation) *noise shaping*. Oversampling generally can bring two advantages. First, the specification of the anti-alias filter is reduced from the Nyquist specification (i.e.the sharp cut-off analog filters required with Nyquist can be replaced with slow roll-off single pole RC circuits). Second, the N bits resolution obtained from an ADC can be increased to N+1 by oversampling the signal by a factor of 4, and subsequently digitally low pass filtering to the Nyquist rate. Noise shaping is a technique whereby the feedback architecture of a $\Sigma-\Delta$ converter allows the analogue input signal of interest to pass unfiltered through the converter, but to high pass filter the quantisation noise. Hence if the quantisation noise has been high pass filtered (or pushed out of the baseband), then the baseband signal of interest can be extracted by digital low pass filtering.

The trade-off when using $\Sigma-\Delta$ devices is an increase the digital processing requirements against a reduction in the analogue components and complexity. Therefore although the expensive analogue anti-alias and reconstruction filters of a traditional Nyquist rate PCM systems are circumvented, the necessary low pass

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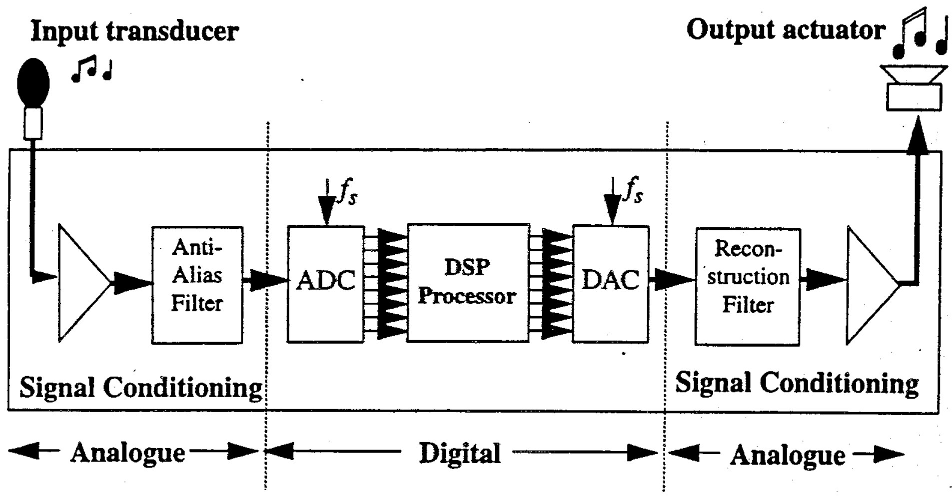

Figure 1: A generic input/output DSP system configured for audio.

filtering to half of the Nyquist rate is done digitally for Σ–Δ ADCs and DACs. The low pass filtering can require a number of stages of comb filters, and even PCM FIR filters and is actually quite an expensive requirement (in digital circuitry terms). However the advantages of Σ–Δ devices far outweighs the disadvantages and they are now well established in the DSP marketplace for analogue to digital, and digital to analogue conversion.

2. Nyquist Rate PCM Systems

Consider the generic Nyquist rate DSP input/output system shown in Figure 1. An input signal is firstly conditioned by amplifying to give it the correct dynamic range for the ADC, followed by an analogue anti-alias filter to cut off all frequencies above $f_s/2$. After the signal has been processed by the DSP processor (typically a linear filtering operation of some sort), the signal is output to the DAC, then to the analogue reconstruction filter which removes the high frequency (aliased) components that are present in the DAC output, and then to a signal conditioning stage (linear amplifier) before being output to an appropriate actuator. The DAC and ADC are usually multi-bit PCM devices which will have linear input/output characteristics. Should the characteristic be A- or μ law encoded then a digital decoding and encoding to a linear signal is necessary in the DSP processor.

For good performance the anti-alias and reconstruction filters require to have sharp cut-offs (ideally brick wall filters) at $f_s/2$, half of the Nyquist rate. The analogue filter chosen will depend on the particular application. For example a simple 4th order (24dB/octave roll-off) may be suitable for an average quality 8kHz telecommunications application, however for high fidelity-audio applications that require 16 bits of good quality resolution 96dB/octave or higher roll-off filters may be required.

One of the main costs in a DSP system can be the analogue anti-alias and reconstruction filters which can be quite expensive compared to the digital devices required. Therefore *oversampling* techniques were introduced with the intention of reducing the specification of the analogue components at the expense of increasing the requirements of the digital technology.

3. Oversampling

Oversampling simply means that a signal has been sampled at a rate higher than dictated by the Nyquist criteria. In DSP systems oversampling is done at integral multiples of the Nyquist rate, f_N, and usually by power of two factor such as 4 X's, 8 X's or 64 X's. When oversampling the specification (and therefore the cost) of the analogue anti-alias and reconstruction filters can be reduced, as the original signal is usually less likely to have frequency components above $Rf_N/2$ (where R is oversampling factor) than it is to have frequency components above $f_N/2$.

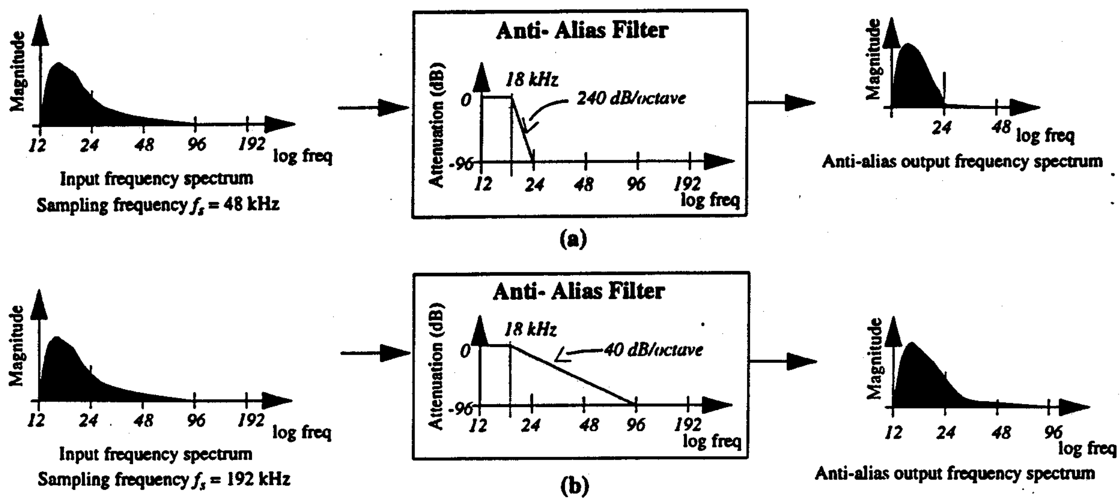

Figure 2: (a) For a particular audio application, sampling at 48 kHz requires that the anti-alias has a sharp cut-off at 18kHz to attentuate by 96dB at 24kHz. (b) For a system that oversamples by a factor of 4, i.e. at 192 kHz the anti-alias analogue filter has a reduced roll-off specification as only frequency components above 96 kHz must be removed to avoid baseband aliasing. Thereafter a digital low pass filter can be designed to filter off the frequencies between 18 and 24 kHz prior to a 4 x's downsampling.

3.1 Oversampling for Analogue to Digital Conversion

As an example of oversampling for ADC, consider a particular digital audio system where the sampling rate is 48kHz and the Nyquist criterion requires to be satisfied by attenuating by at least 96 dB (equivalent to a 16 bit dynamic range) all frequencies above 24kHz that may be output by certain musical instruments or interfering electronic equipment. If it is decided that the low pass filter will cut off at 18 kHz, and if 96dB attenuation is required at 24kHz, then a filter with a roll-off of 240 dB/octave as shown in Figure 2(a) would be suitable. Clearly this is a 40th order filter and somewhat difficult to reliably design in analogue circuitry! (Please note the figures used here are for example purposes only and do not reflect actual digital audio systems!) However if we oversample the music signal by 4 x's, i.e. at $4 \times 48\ \text{kHz} = 192\ \text{kHz}$, then an analogue anti-alias filter with a roll-off of only 40 dB/octave starting at 18 kHz and providing more than 96dB attenuation at half of the oversampled rate of 96 kHz is required as shown in Figure 2(b). (In actual fact the roll-off could be even lower as it is very unlikely there will be any significant frequency components above 30 kHz in the original analogue music.)

If an oversampled digital audio signal is input to a DSP processor, clearly the processing rate must now run at the oversampled rate. This requires R x's the computation of its Nyquist rate counterpart (i.e. the impulse response length of all digital filters in now increased by a factor of R), and at a frequency R x's higher. Hence the DSP processor would require to by R^2 x's faster to do the same useful processing as an equivalent Nyquist rate sampled system. This is clearly not very desirable and a considerable disadvantage. Therefore the oversampled signal is *decimated* to the Nyquist rate, first by digital low pass filtering, then by downsampling by a factor of R. In the above example any frequency components that exist between 18 and 96 kHz after the analog anti-alias filter can be removed with a *digital* low pass filter, prior to downsampling by a factor of 4. Hence the complexity of the analogue low pass anti-alias filter has been reduced by effectively adding a digital low pass stage of anti-alias filtering. Decimation is illustrated for a system oversampled by a factor of 4 in Figure 3. After decimating the signal, the DSP processor can be presented with a Nyquist rate signal.

In general therefore a key design trade-off for oversampling ADCs is the digital implementation cost of the sharp cut-off digital low pass filter versus cost of the sharp cut-off analogue anti-alias filter.

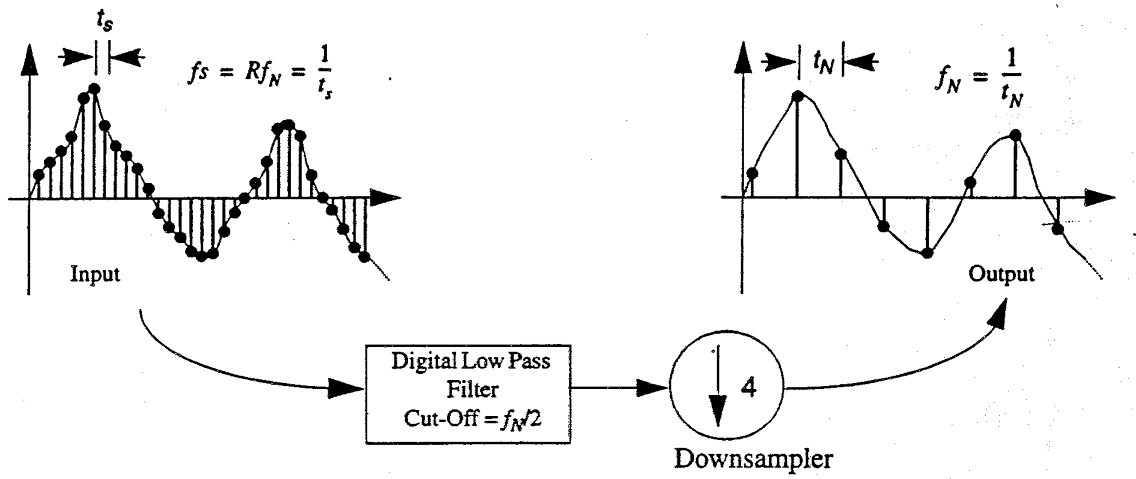

Figure 3: Decimation of a 4 x's oversampled signal by low pass digital filtering then downsampling by retaining every 4th sample.

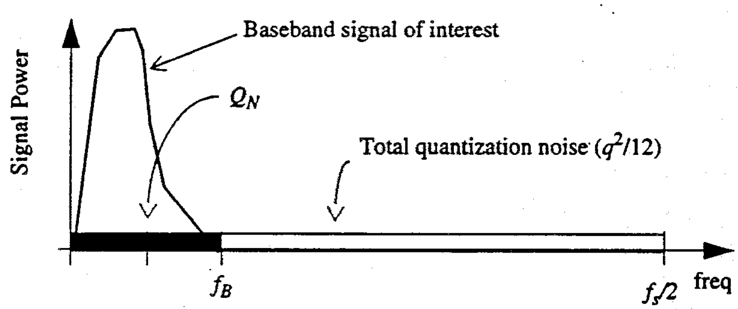

Figure 4: Oversampling a signal to increase resolution.

3.2 Oversampling for Digital to Analogue Conversion

For an input/output DSP system the specification of the reconstruction filter is usually the same as the anti-alias filter and therefore the same cost will be associated with implementing this analogue filter. However we can again use oversampling techniques to reduce this requirement by trading-off the analogue reconstruction filter specification with *digital reconstruction filtering*. Therefore the interpolation will be performed at the output, which requires low pass filters and upsamplers (effectively the opposite of Figure 3.)

4. Oversampling to Increase Signal Resolution

As well as reducing the cost, oversampling can be used to increase the resolution of an ADC or DAC. If an ADC has a quantization level of q volts the in band quantization noise power, Q_N, is often calculated as:

$$Q_N = \frac{2q^2 f_B}{12 f_s} \tag{1}$$

as illustrated in Figure 4 and where the quantisation signal is assumed to be random. In order to increase the signal to quantisation noise ratio we can either increase the number of bits in the ADC (reduce q) or increase the sampling rate f_s above Nyquist. From Figure 4 it can be seen that oversampling a signal by a factor of 4 x's the Nyquist rate reduces the in-band quantization noise (assumed to be a flat spectrum between 0 Hz and $f_s/2$ Hz) by 1/4 [1]. This noise power is equivalent to an ADC with step size $q/2$ and hence baseband signal resolution has been increased by 1 bit [26]. In theory therefore if a single bit ADC with an appropriately low noise floor

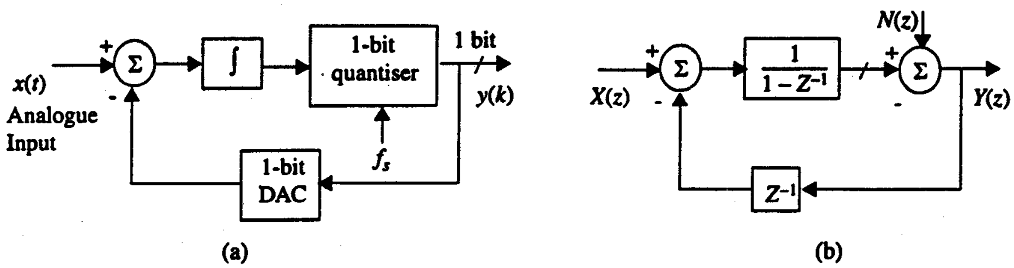

Figure 5: (a) First order Σ–Δ converter. (b) Digital model of first order Σ–Δ converter where the analogue integrator and DAC are digital models, and the quantiser is modeled as an additive white noise source.

were used and oversampled by a factor of 4^{15} ($\approx 10^9$) then a 16 bit resolution signal could be realized! Clearly this sampling rate is not practically realisable. However at a more intuitively useful level, if an 8 bit ADC converter was used to oversample a signal by a factor of 16 x's the Nyquist rate, then when using a digital low pass filter to decimate the signal to the Nyquist rate, approximately 10 bits of resolution could be extracted from the digital output signal.

5. Σ–Δ Quantisation Noise Shaping

Σ–Δ converters use noise shaping techniques whereby the in-band quantization noise from oversampling can be high pass filtered, and the oversampling factor required to increase signal resolution can be reduced from the 4x's per single bit level discussed above. Figure 5(a) shows a simple first order Σ–Δ ADC converter. The only analogue elements required are an integrator, a summer, and a 1 bit ADC (or two level quantiser) and single bit DAC in the feedback loop.

Figure 5(a) is in fact a non-linear system and extremely difficult to analyse, and therefore an all-digital linear model, as shown in Figure 5(b), is often used. In this model the quantiser is modelled as an additive random noise source, where once again the quantisation noise has been assumed to be random. Although this model does not adequately model many of the subtilties of the Σ–Δ converter, it is useful for many forms of preliminary analysis. The Z-domain representation of the single bit digital output signal in Figure 5(b) is:

$$Y(z) = X(z) + (1 - z^{-1})N(z) \tag{2}$$

Therefore the digital model indicates that the input signal has been sampled and then passed through the sigma delta loop unaltered, whereas the quantisation noise signal, $n(k)$, has been effectively high pass filtered by the $(1 - z^{-1})$ differentiator. Therefore this noise shaping has increased the baseband signal to noise ratio by virtue of attenuating quantisation noise at low frequencies. By cascading several first order converters, higher order Σ–Δ ADCs can be realised where the high pass filtering effect is further increased. For example the output of a 3rd order Σ–Δ loop is approximately:

$$Y(z) = X(z) + (1 - z^{-1})^3 N(z) \tag{3}$$

(Note that higher that the design of higher order Σ–Δ loops is not quite as straightforward as cascading first order loops which is likely to have stability problems [1].)

As an illustration of noise shaping consider a high fidelity audio application where the required baseband sampling rate is 48000 Hz, Figure 6(a) shows the approximate (smoothed) quantisation noise spectrum from a 1 bit ADC (i.e. a two level quantiser) oversampled by a factor of 64. Therefore noting that the shaded area represents the baseband (0 - 24 kHz), by decimating this signal by a factor of 64, then we can achieve around 4 bits of resolution. However if a 1st order Σ–Δ loop is used with the same two level quantiser, then because of the noise shaping properties, the output spectrum of the quantisation noise (still of 1 bit resolution) is as shown in Figure 6(b). If this signal is decimated, then noting the level of baseband quantisation noise is almost -70 dB below the maximum, then around 12 bits of resolution could be output by a digital low pass decimation filter.

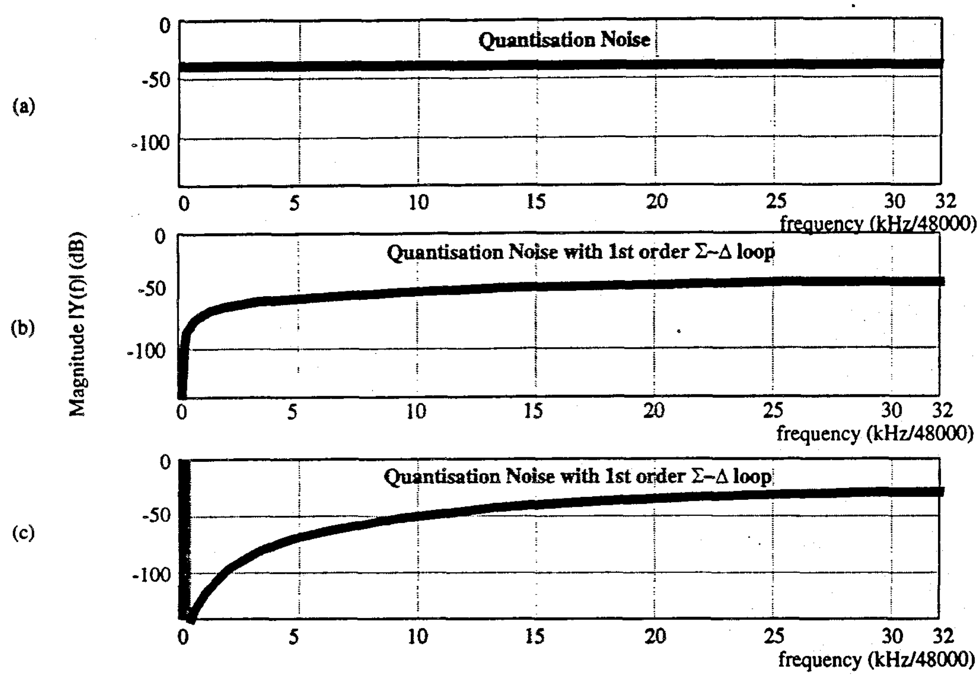

Figure 6: Quantisation noise spectra obtained by oversampling by 64 x's using a two level quantiser (a) With no noise shaping, (b) with a first order $\Sigma-\Delta$ converter and (c) with a third order $\Sigma-\Delta$ converter. In all figures the shaded area represents the basedband signal from 0-24 kHz.

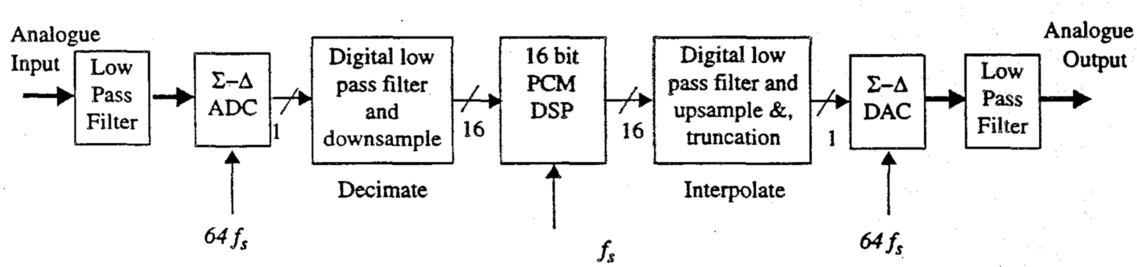

Figure 7: Using Σ-Δ devices for Nyquist rate PCM DSP Computation.

When a 3rd order $\Sigma-\Delta$ loop is used, this further lowers the quantisation noise in the baseband (although increasing it at higher MHz frequencies) and allows almost 96dB of dynamic range or 16 bits resolution for the decimated Nyquist rate baseband signal.

5.1 $\Sigma-\Delta$ DSP Systems

Figure 7 shows the stages of analogue and digital low pass filtering (decimation and interpolation) that are required for converting the $\Sigma-\Delta$ signal to and from PCM for processing by a Nyquist rate DSP processor. Both decimation and interpolation are required. Therefore although the $\Sigma-\Delta$ devices and the analogue anti-alias and reconstruction filters are low cost, digital decimation and interpolation stages are required.

6. Σ–Δ Devices

There are now many companies currently producing Σ–Δ (or Δ–Σ)[1] DACs, ADCs and mixed signal DSP processors with on chip codecs. In Table 1 we present some key parameters on a few devices currently available from some of the larger semiconductor companies. The table only gives a representative selection of available ADCs, DACs and CODECs, and readers are advised to contact the respective companies for a fuller of list of the components and devices currently available. The table gives the quoted data sheet upper baseband sampling rate (rounded to the nearest "application" rate in some cases) and anticipated device bit resolution. Also given is the oversampling ratio used, the order of the noise shaping used, and the Σ–Δ quantiser resolution. ONe of the most useful figures on the data sheets is the total harmonic distortion + noise (THD+N), and other forms of signal to noise ratios. However in general different companies using different schemes to calculate their SNR dB figures, and therefore given the variability in methods (and the variability on data sheets from the same company in one case!) they have not been stated in this table..

Device	Baseband Output	Over-sampling	Noise Shaping
Motorola DSP56ADC16 CODEC [10]	100kHz x 16 bits 400kHz x 12 bits	64 x's	3rd x 1 bit
Burr Brown PCM1710 DAC [4]	48 kHz x 20 bits	384 x's (clock)	4th x 5 levels
Burr Brown PCM1760 / DF1760 ADC [5]	48 kHz x 20 bits	64 x's	4th x 4 bit
Texas Instruments TLC320AD58C ADC [8]	48kHz x 18 bits	64 x's	4th x 1 bit
National Semiconductor ADC16071/16471 DAC	48kHz x 16 bits	64 x's	4th x 1 bit
Nippon Precision Circuits SM5872A/B DAC [13]	44.1 x 16 bits	384 x's/ 189 x's	4th x 1 bit
Crystal Semiconductor CS4215 ADC/DAC [2]	48 kHz x 16 bits	64 x's	3rd x 1 bit
Crystal Semiconductor CS4328 DAC [2]	48kHz x 18bits	64 x's	5th x 1 bit
Crystal Semiconductor CS5390 [2]	48kHz x 20 bits	64 x's	5th x 1 bit
Analog Devices AD776 [6]	100 kHz x 16 bits 400kHz x 12 bits	64 x's	3rd x 1 bit
Analog Devices AD1879 Dual ADC [6]	48kHz x 18 bits	64 x's	5th x 1 bit
Analog Devices AD28msp02 CODEC [6]	8 kHz x 16 bits	128 x's	5th x 1 bit
Philips SAA7360GP ADC[9]	48kHz x 18 bits	128 x's	3rd x 1 bit
Philips SAA7350(A) DAC [9]	48kHz x 20 bits	128 x's	3rd x 1 bit

Table 1: A selection of Σ–Δ devices currently available from some semiconductor manufacturers. (For more detailed information on the above and the many other devices refer to the referenced data sheet or contact the company directly.)

Because Σ–Δ devices are suitable for CMOS implementation, mixed signal, single chip DSP processors are now becoming available. In Table 2 some information on mixed signal DSP processors from Motorola, Analog Devices, and Crystal Semiconductors is given. Undoubtedly as device sizes continue to shrink, and Σ–Δ design advances, mixed signal DSP processors will be available for a wide variety of applications ranging from biomedical (100Hz sampling rates), through voiceband (8kHz sampling rates), to hifidelity (48kHz sampling rates) and ultimately video devices (MHz sampling rates).

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1. Sigma-delta devices are interchangeably referred to as delta sigma, however the two terms mean exactly the same and the name alternatives has been put down to an "unfortunate" misunderstanding [1].

Mixed Signal DSP Processor	Analogue I/O	Applications	Analogue Characteristics	On-Chip Features
Crystal Semiconductor CS4920 Multi standard Audio Decoder [2]	44.1kHz x 16 bits 128x' oversampling On chip Σ–Δ DAC 3rd x 1 bit	Digital Audio Decompression: MPEG/Dolby AC-2	88dB (Dynamic Range) 0.01% THD	16.9 MIPs 24 x 24 multiplier 6K x 24 bit RAM PLL
Motorola DSP56156[11]	8kHz x 13 bits 125 x's oversampling 2nd x 1 bit Σ–Δ Codec	Telecomms/ Voiceband	60 dB S/(N+D)	30 MIPs 16 x 16 multiplier 4Kx 16 bit RAM 14K x 16 bit ROM
Analog Device ADSP 21msp59 [7]	8kHz x 13 bits On chip CODEC 125 x's oversampling	Telecomms/ Voiceband	65 dB SNR +THD	26 MIPs 16 x 16 multiplier 4K x 24 bit RAM 4K x 24 bit ROM

Table 2: Mixed signal DSP processors with on-chip Σ–Δ ADC and DACs.

7. Conclusions and Current Research Directions

In this paper a brief introduction to the principles of oversampling, noise shaping and sigma delta devices has been given. Over the last few years the low cost and availability of quality Σ–Δ devices has had a considerable impact on the hifidelity and voiceband audio. Σ–Δ ADC can also now provide almost 24 bits of resolution for low frequency (100's of Hz) biomedical applications and easily produce 20 bit level accuracy for hifidelity audio systems. An example of the availability and convenience of the Σ–Δ solution is the *very low* cost Motorola DSP56002 EVM module which features not only a 40MHz DSP56002 processor and serial PC interface circuitry, but also a Crystal CS4215 CODEC chip providing all anti-alias, reconstruction filtering, stereo 16 bit analogue input and output, direct microphone and headphone inputs and outputs on a single 44 pin device of less than 1 cm^2 in area.

Finally although Σ–Δ is now at an advanced state of implementation, there are many research areas currently being undertaken, including:

- The investigation of dithering, psychoacoustic noise shaping and chaos techniques for Σ–Δ conversion [17], [18].
- Novel strategies for achieving high order Σ–Δ codecs [28].
- Σ–Δ computation architectures where all DSP processing is done at the oversampling rate using only single bit data [16], [22], [24].
- Noise shaping and noise immunity strategies for Σ–Δ based basestation communication for mobile telephones [31].
- FPGA (Field Programmable Gate Arrays) and Σ–Δ ASIC architectures [29], [30].
- Bandpass noise shaping sigma delta techniques for direct radio IF to digital conversion [23].

This last area looks to be particularly promising by setting up a bandpass noise shaping characteristic of the Σ–Δ converter (rather than the well known low pass noise shaping of Figure 6(b)) such that Σ–Δ devices can not only prove ADC capabilities, but also an effective demodulation. In [23] a 455 kHz IF radio carrier frequency with a 10kHz bandwidth was extract with SNR of 65dB and using an oversampling ratio just above 90 x's.

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