High-Frequency Scalable Electrical Model and Analysis of a Through Silicon Via (TSV)

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***Abstract*—We propose a high-frequency scalable electrical model of a through silicon via (TSV). The proposed model includes not only the TSV, but also the bump and the redistribution layer (RDL), which are additional components when using TSVs for 3-D integrated circuit (IC) design. The proposed model is developed with analytic $RLGC$ equations derived from the physical configuration. Each analytic equation is proposed as a function of design parameters of the TSV, bump, and RDL, and is therefore, scalable. The scalability of the proposed model is verified by simulation from the 3-D field solver with parameter variations, such as TSV diameter, pitch between TSVs, and TSV height. The proposed model is experimentally validated through measurements up to 20 GHz with fabricated test vehicles of a TSV channel, which includes TSVs, bumps, and RDLs. Based on the proposed scalable model, we analyze the electrical behaviors of a TSV channel with design parameter variations in the frequency domain. According to the frequency-domain analysis, the capacitive effect of a TSV is dominant under 2 GHz. On the other hand, as frequency increases over 2 GHz, the inductive effect from the RDLs becomes significant. The frequency dependent loss of a TSV channel, which is capacitive and resistive, is also analyzed in the time domain by eye-diagram measurements. Due to the frequency dependent loss, the voltage and timing margins decrease as the data rate increases.**

***Index Terms*—Scalable model, three-dimensional (3-D) integrated circuit (IC), through silicon via (TSV), TSV channel.**

I. Introduction

RECENTLY, silicon-based semiconductor devices have scaled down to 20 nm to increase system density and reduce the power consumption following trends based on Moore's law and more [1]. As technology advances in the nanometer era, individual chips are improving in packaging density and system performance. Unfortunately, scaling the minimum feature size of the transistor slows down due to the limitations of interconnect performance, leakage power consumption, process variation, and cost for further advancement [2], [3]. As a new paradigm to overcome the limited semiconductor device technology from the saturated minimum feature size, 3-D integration is leading the technology trends. The concept of 3-D integrated circuits (3-D ICs) is shown in Fig. 1. In 3-D IC, through silicon via (TSV) is the core technology that provides a vertical interconnection with greatly reduced interconnection length among the stacked dies, as shown in Fig. 2. As the system complexity increases, the number of input/output (I/O) pins increases exponentially according to Rent's rule [4]. Since the TSV passes through the silicon substrate vertically, the locations of I/O pins are not limited, thus, we can support the increasing demands of the I/O pins with TSVs. Therefore, to realize highly-dense packaging and to improve I/O channel bandwidth for high-speed integrated circuits, 3-D IC technology using TSVs has become a promising solution [5].

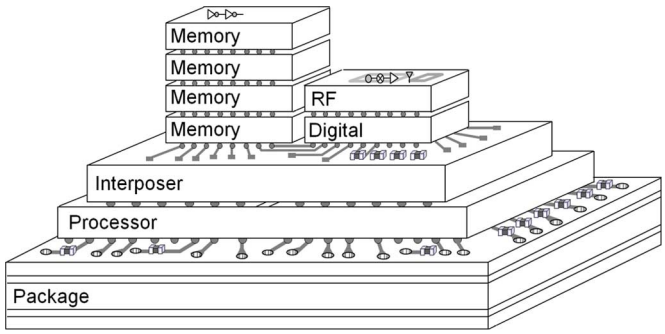

Fig. 1. A 3-D IC; a vertical integration of homo- and heterogeneous dies, such as memory, RF, digital, processor die, and interposer, to realize highly dense packaging for high-speed integrated circuit systems.

To design high-speed I/O channels with TSVs and perform signal integrity analysis for the advanced 3-D IC design, it is essential to electrically model TSVs using design parameters such as geometric and material information up to the gigahertz range. Then, the electrical model can be combined with other circuits so that the overall electrical performances of the system can be estimated. In addition, we can reduce the high computational time required by 3-D field solvers. Therefore, much research has been done to model and analyze TSVs. In the previous research [6], an equivalent circuit model of the TSV, which is valid up to 20 GHz, has been proposed. However, analytic equations were not presented in the proposed equivalent circuit model. Thus, it cannot provide physical insights for the electrical behavior of the TSV. In other previous works [7]–[13], electrical modeling and characterization of the TSV have been done, however, they

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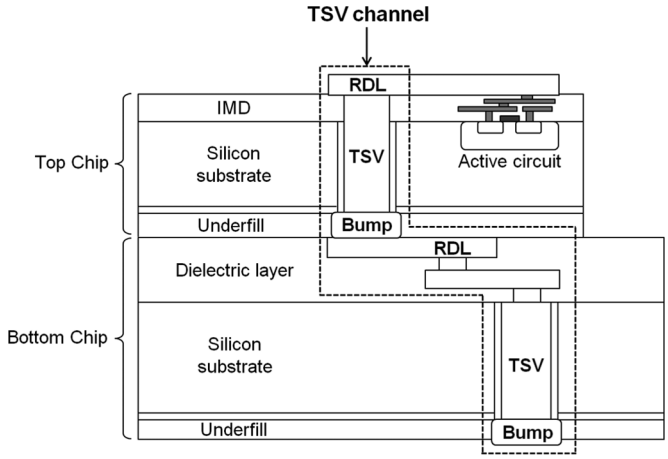

Fig. 2. A cross-sectional view of a vertical interconnect through the stacked dies. The TSV channel in 3-D IC includes a TSV, bump, and RDL. The TSV and bump provide a vertical interconnect through the silicon substrate, and the RDL provides a horizontal interconnect between top and bottom chip TSVs with different pitches.

did not consider all the parasitic components of the TSV. For example, the capacitance between TSVs in the inter-metal dielectric (IMD) layer or bottom oxide layer and the capacitance between the TSV and bump were not considered in the proposed model. The influence of those ignored parasitic components increases as the operating frequency increases, and has to be considered in TSV modeling for high-speed I/O design that includes TSVs.

With various targets or applications in 3-D IC design, the model has to estimate the electrical behavior of the TSV even with different physical dimensions and material properties. Thus, it is necessary to propose a scalable model of the TSV with analytic equations. Hence, if the physical dimension or material is changed, the model can be applied to the changes in design. Furthermore, to propose the model with analytic equations is important because the analytic model can be expanded and applied to evaluate electrical performances such as power consumption, delay, and skew along the TSV-based interconnect. In addition, it provides insights of a TSV that includes the physical meaning of each parasitic component. Therefore, it helps to understand the electrical behavior of the TSV.

For an applicable and practical model of the TSV, the TSV channel which includes not only the TSVs, but also the bumps, and the redistribution layers (RDLs) has to be modeled and should be analyzed. Heterogeneous dies which have different layouts such as the I/O pin locations can be vertically integrated. As shown in Fig. 2, the bump provides a joint between the stacked chips, and the RDL provides a horizontal interconnection to redistribute the signals between heterogeneous dies. When designing the I/O channel with TSVs in 3-D IC, the bump and RDL are essential components that should be considered with the TSV. Therefore, modeling and analysis of a TSV with the bump and RDL is important for advanced 3-D IC design.

In this paper, the high-frequency scalable electrical model of a TSV is proposed with analytic $RLGC$ equations. The electrical behaviors of a TSV are analyzed with the proposed model. The analytic equations of the scalable model are proposed in terms of design parameters, such as physical dimensions and material properties. Thus, each analytic equation fully represents the physical meaning of each parasitic component of a TSV. The scalability of the proposed model for a TSV is verified by simulation with parametric variations from the 3-D field solver. The bump and RDL are also modeled with analytic equations by applying the verified equations in [14]–[16]. As a result, a high-frequency scalable electrical model of the TSV channel is proposed. To experimentally verify the proposed model, a series of test vehicles of a TSV channel are fabricated. The proposed model is experimentally verified with *S*-parameter measurements up to 20 GHz. Therefore, the electrical characteristics of a TSV channel are analyzed in the frequency domain with the verified scalable model with variations in design parameters. From this analysis, the capacitive and resistive electrical behaviors of a TSV channel are characterized. In addition, the design parameters that dominantly affect the TSV channel characteristic are analyzed in different frequency ranges. Furthermore, the overall electrical behavior of the TSV channel is analyzed with fabricated test vehicles in the time domain. The time-domain analysis of the TSV channel is done with eye diagram measurements for up to 10 Gb/s input signals of pseudo-random bit data patterns.

II. Scalable Modeling of a TSV Channel

In this section, a high-frequency scalable electrical model of a TSV channel, which includes not only the TSV but also the bump and RDL, is proposed. This scalable model is represented with analytic $RLGC$ equations based on the lumped model. Since the model is derived from the physical structure, it fully expresses the physical meaning of each parasitic component with the proposed closed-form equations. For the scalability of the model, the model is proposed with structural parameters and material properties as variables of the analytic $RLGC$ equations. The design parameters of the TSV channel are listed in Table I and its material properties are listed in Table II.

A. Modeling of a Through Silicon Via With Bumps

Fig. 3(a) shows the structure and its parameters of a signal TSV, a ground TSV and bumps in a single-ended signaling configuration with the via-last process. With this structure, a high-frequency scalable electrical model of TSVs with bumps is proposed in Fig. 3(b). The analytic $RLGC$ equations are derived from the physical configuration with the design parameters. Therefore, each $RLGC$ equation is a function of the variables from the design parameters.

As shown in Fig. 3(b), the scalable electrical model is proposed by lumped modeling. The total lengths of the TSV interconnect including the TSV and bump are going down under tens of micrometers order as the process technology advances. Since this length is short enough compared to the wavelength of several or tens of gigahertz operating frequency, the lumped approximation is valid and a single lumped stage is sufficient for the TSV model. Even though the model is proposed with analytic equations resulting in scalable with design parameters, the proposed model is based on the via-last process. Thus, in case

TABLE I
MODEL PARAMETERS WITH THEIR SYMBOLS FOR THE PROPOSED SCALABLE ELECTRICAL MODEL OF TSVS WITH BUMPS IN 3-D IC, WHICH INCLUDE STRUCTURAL PARAMETERS AND MATERIAL PARAMETERS

Parameter	Symbol	Parameter	Symbol
TSV diameter [μm]	d_{TSV}	Conductivity of silicon substrate [S/m]	σ_{Si}
TSV height [μm]	h_{TSV}	Resistivity of TSV [$\Omega \cdot m$]	ρ_{TSV}
TSV-to-TSV pitch [μm]	p_{TSV}	Resistivity of bump [$\Omega \cdot m$]	ρ_{Bump}
Insulator thickness [μm]	t_{ox}	Resistivity of RDL [$\Omega \cdot m$]	ρ_{RDL}
Bump diameter [μm]	d_{Bump}	Relative permittivity of silicon substrate	$\varepsilon_{\mathrm{r,Si}}$
Bump height [μm]	h_{Bump}	Relative permittivity of insulator	$\varepsilon_{\mathrm{r,Insulator}}$
IMD height [μm]	h_{IMD}	Relative permittivity of IMD	$\varepsilon_{\mathrm{r,IMD}}$
Bottom SiO_2 thickness [μm]	$t_{\mathrm{ox,bot}}$	Relative permittivity of underfill	$\varepsilon_{\mathrm{r,Underfill}}$
RDL width [μm]	w_{RDL}	Relative permeability of TSV	$\mu_{\mathrm{r,TSV}}$
RDL thickness [μm]	t_{RDL}	Relative permeability of bump	$\mu_{\mathrm{r,Bump}}$
Space between RDL [μm]	S_{RDL}	Relative permeability of RDL	$\mu_{\mathrm{r,RDL}}$

TABLE II
MATERIAL PROPERTIES OF THE DESIGNED TEST VEHICLES

Symbol	Value	Symbol	Value
σ_{Si}	10 [S/m]	$\varepsilon_{\mathrm{r,IMD}}$	4
ρ_{TSV}	$1.68\mathrm{x}10^{-8}$ [$\Omega \cdot m$]	$\varepsilon_{\mathrm{r,ox,bot}}$	4
ρ_{Bump}	$1.68\mathrm{x}10^{-8}$ [$\Omega \cdot m$]	$\varepsilon_{\mathrm{r,Underfill}}$	7
ρ_{RDL}	$1.68\mathrm{x}10^{-8}$ [$\Omega \cdot m$]	$\mu_{\mathrm{r,TSV}}$	1
$\varepsilon_{\mathrm{r,Si}}$	11.9	$\mu_{\mathrm{r,Bump}}$	1
$\varepsilon_{\mathrm{r,ox}}$	4	$\mu_{\mathrm{r,RDL}}$	1

of the via-first or middle process, parasitic capacitances such as C_{IMD} has to be neglected or other parasitic has to be additionally considered in order to accurately estimate the electrical behaviors of a TSV. In addition, if there are active circuits between TSVs, the field distribution that assumed can be changed. However, the main electrical characteristics and the loss mechanism of a TSV channel are valid enough with the proposed model.

To electrically isolate the TSV from the conductive silicon substrate, an insulation layer surrounding the TSV is necessary. Due to this insulation layer, there is an insulator capacitance, $C_{\mathrm{Insulator}}$, as shown in Fig. 4. Since the TSV is filled with metal and the silicon substrate is conductive, the insulator capacitance can be derived from the coaxial-cable capacitance model [17]. Thus, $C_{\mathrm{Insulator}}$ is a function of d_{TSV}, h_{TSV}, and t_{ox}, as shown in (1). Since the insulator capacitance of a TSV is separated into two parallel parts, as shown in Fig. 3(b), the equation of $C_{\mathrm{Insulator}}$ is expressed as half of the whole insulator capacitance of a TSV

$$C_{\mathrm{Insulator}} = \frac{1}{2}\left\{2\pi \times \varepsilon_0 \varepsilon_{r,\mathrm{Insulator}} \times \frac{h_{\mathrm{TSV}} - h_{\mathrm{IMD}}}{\ln\left(\frac{d_{\mathrm{TSV}}/2 + t_{\mathrm{ox}}}{d_{\mathrm{TSV}}/2}\right)}\right\}[F]. \tag{1}$$

One of the bump-to-silicon substrate capacitances of the upper side of the silicon substrate, C_{Bump1}, has to be added to $C_{\mathrm{Insulator}}$ of the proposed equivalent circuit model, as shown in Fig. 3(b). This capacitance can be modeled as a parallel-plate capacitor. As shown in Fig. 5(a), the area, where the electric fields are formed, corresponds to where the bump overlies

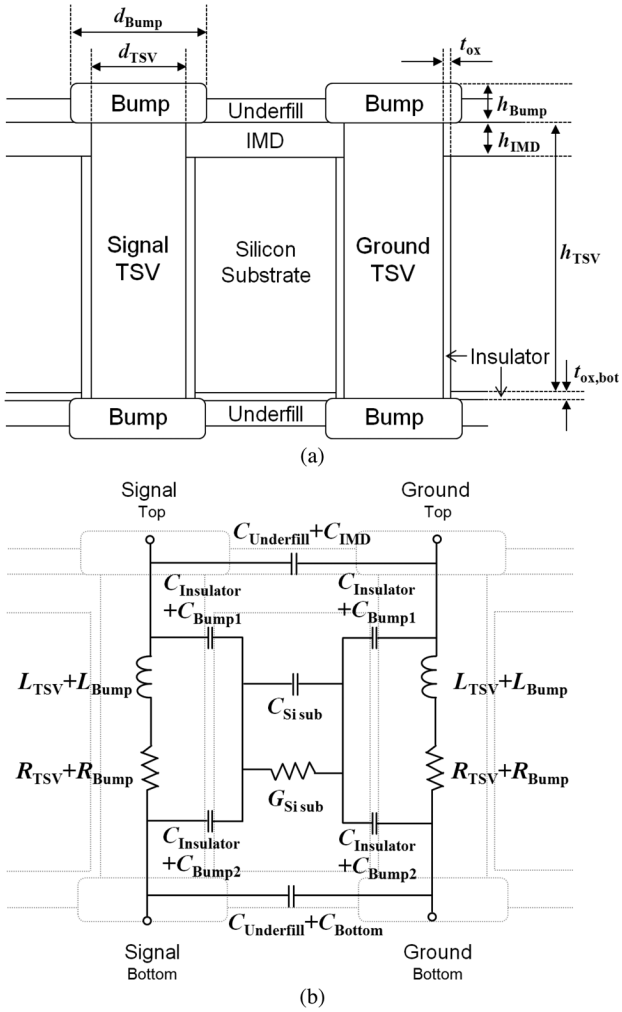

Fig. 3. (a) Structure of a signal TSV and a ground TSV with bumps with the via-last process and their structural parameters, and (b) the proposed scalable electrical model with labeled $RLGC$ components.

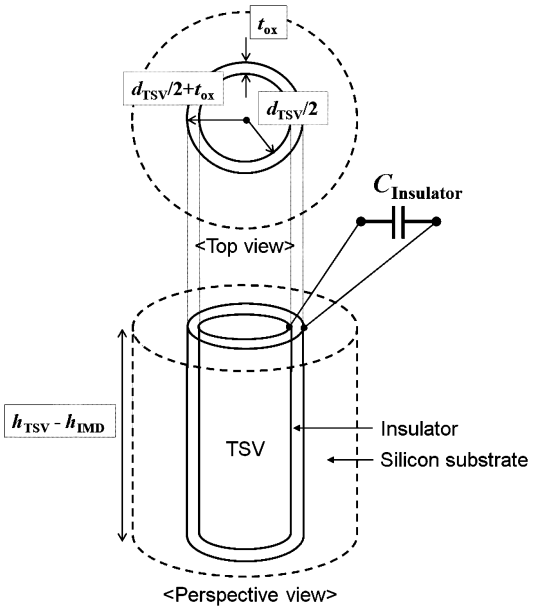

Fig. 4. Top view and a perspective view of a TSV which passes through the silicon substrate vertically. The TSV is surrounded by an insulator to be isolated from the conductive silicon substrate. Thus, $C_{\mathrm{Insulator}}$ is derived from the coaxial-cable capacitance model which is determined by d_{TSV}, t_{ox}, h_{TSV}, and h_{IMD}.

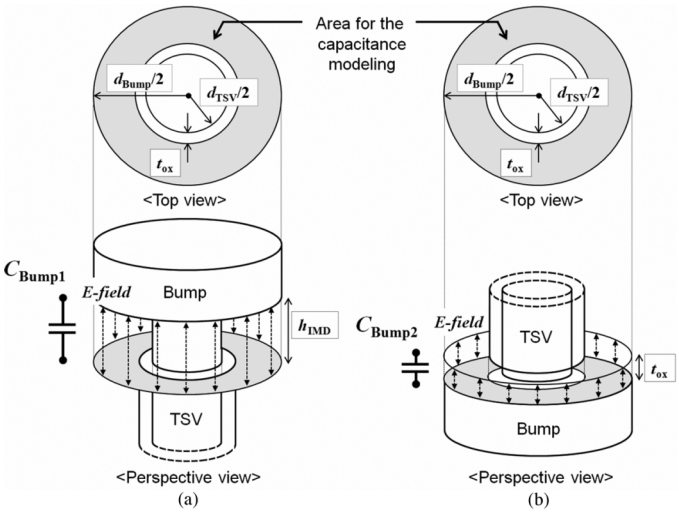

Fig. 5. A top view and a perspective view of (a) the upper part and (b) the bottom part of a TSV with a bump to calculate the area where the electric fields are formed between the bump and the silicon substrate to model C_{Bump1} and C_{Bump2}. They have parallel-plate capacitor configurations.

the silicon substrate through the inter-metal dielectric (IMD) layer. Thus, C_{Bump1} is proportional to this area and inversely proportional to the IMD height, h_{IMD}. As a result, C_{Bump1} can be calculated with (2), which depends on d_{TSV}, d_{Bump}, and h_{IMD}.

$$C_{\mathrm{Bump1}} = \varepsilon_0 \varepsilon_{r,\mathrm{IMD}} \times \frac{\pi \times \left\{(d_{\mathrm{Bump}}/2)^2 - (d_{\mathrm{TSV}}/2 + t_{\mathrm{ox}})^2\right\}}{h_{\mathrm{IMD}}}[F]. \quad (2)$$

In a similar manner, another bump-to-silicon substrate capacitance due to the bottom oxide layer on the bottom side of

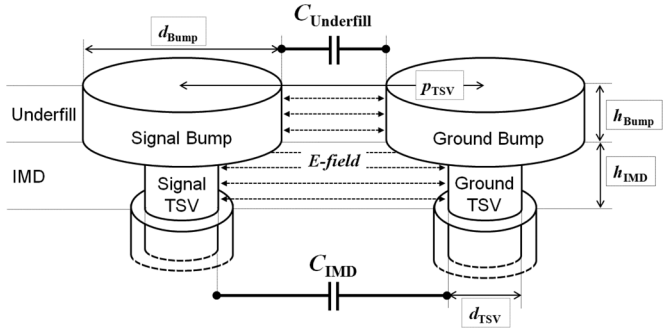

Fig. 6. The upper part of a TSV and a bump with electric fields formed between the signal and ground TSVs and bumps to model $C_{\mathrm{Underfill}}$ and C_{IMD}. The TSV/Bump signal and ground pairs are in a parallel-wire capacitor configuration. $C_{\mathrm{Underfill}}$ is formed due to the underfill between bumps, and C_{IMD} is formed due to the IMD between TSVs.

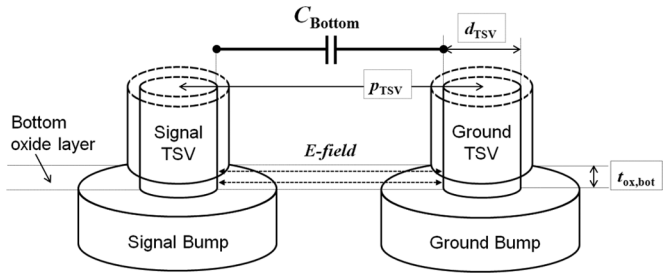

Fig. 7. The bottom part of a TSV and a bump with the electric fields formed between signal and ground TSVs to model C_{Bottom}, which are in the parallel-wire capacitor configuration. C_{Bottom} is formed due to the bottom oxide layer between TSVs.

the silicon substrate, C_{Bump2}, has to be added to $C_{\mathrm{Insulator}}$. This bottom oxide layer is formed by the oxidation after back-grinding of the silicon substrate. This process is necessary to expose the TSV and connect it with another die. C_{Bump2} is also derived from the parallel-plate capacitor model, as shown in Fig. 5(b). Therefore, d_{TSV}, d_{Bump}, h_{Bump}, and the bottom oxide thickness, $t_{\mathrm{ox,bot}}$, determines C_{Bump2}, as shown in

$$C_{\mathrm{Bump2}} = \varepsilon_0 \varepsilon_{r,\mathrm{ox}} \times \frac{\pi \times \left\{(d_{\mathrm{Bump}}/2)^2 - (d_{\mathrm{TSV}}/2 + t_{\mathrm{ox,bot}})^2\right\}}{t_{\mathrm{ox,bot}}}[F]. \quad (3)$$

With the via-last process, the capacitance between the signal and ground bumps from the underfill, $C_{\mathrm{Underfill}}$, the capacitances between the signal and ground TSVs from the IMD layer, C_{IMD}, and the bottom oxide layer, C_{Bottom}, have to be modeled. As shown in Figs. 6 and 7, the cross-sectional areas of the TSV and bump are circular. Hence, $C_{\mathrm{Underfill}}$, C_{IMD}, and C_{Bottom} are derived from the model of the parallel-wires capacitance [18]. The capacitances are determined by the distance between the signal and ground TSVs or bumps, p_{TSV}, the diameter of the TSV and bump, d_{TSV} and d_{Bump}, and the height of the underfill, IMD layer and bottom oxide, h_{Bump}, h_{IMD}, and $t_{\mathrm{ox,bot}}$. If d_{TSV} and d_{Bump} are very small in comparison with the distance of separation, $p_{\mathrm{TSV}}/d_{\mathrm{TSV}}$ (or d_{Bump}) $\gg$1, the natural logarithm replaces the inverse hyper cosine to simplify the

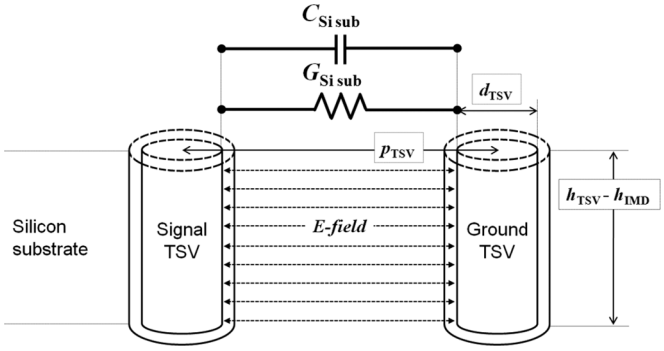

Fig. 8. A TSV passing through the silicon substrate with the electric fields formed between signal and ground TSVs to model $C_{\text{Si sub}}$ and $G_{\text{Si sub}}$. The parallel-wire capacitor configuration is implemented.

calculation. However, since the TSV in 3-D IC is for denser integration with fine pitch, we assume that the ratio of p_{TSV} and d_{TSV} or d_{Bump}, $p_{\text{TSV}}/d_{\text{TSV}}$ (or d_{Bump}), is less than 10. Therefore, $C_{\text{Underfill}}$, C_{IMD}, and C_{Bottom} are modeled as shown in

$$C_{\text{Underfill}} = \frac{\pi \times \varepsilon_0 \varepsilon_{r,\text{Underfill}}}{\cosh^{-1}\left(\frac{p_{\text{TSV}}}{d_{\text{Bump}}}\right)} \times h_{\text{Bump}}[F] \tag{4}$$

$$C_{\text{IMD}} = \frac{\pi \times \varepsilon_0 \varepsilon_{r,\text{IMD}}}{\cosh^{-1}\left(\frac{p_{\text{TSV}}}{d_{\text{TSV}}}\right)} \times h_{\text{IMD}}[F] \tag{5}$$

$$C_{\text{Bottom}} = \frac{\pi \times \varepsilon_0 \varepsilon_{r,\text{ox,bot}}}{\cosh^{-1}\left(\frac{p_{\text{TSV}}}{d_{\text{TSV}}}\right)} \times t_{\text{ox,bot}}[F]. \tag{6}$$

There is another parasitic capacitance contributed to the lateral side of the bump. This capacitance is formed between the lateral side of the bump and the conductive silicon substrate. It has to be added to $C_{\text{Insulator}}$ of the proposed model. It can be calculated from the conformal mapping method of the vertical plate. This method transforms a 3-D interconnect into a parallel plate configuration [14]. However, with d_{TSV} of 30 μm, d_{Bump} of 70 μm, h_{Bump} of 10 μm and h_{IMD} of 6 μm, this capacitance is about 10 fF. Thus, it is ignored as the value of $C_{\text{Insulator}}$ is in the order of a pF. As a result, this fringe capacitance is ignored in this proposed model.

Since the silicon is a semiconductor, there are capacitance and conductance between the signal and ground TSVs, as shown in Fig. 8. In a similar manner as modeling $C_{\text{Underfill}}$, C_{IMD}, and C_{Bottom}, the capacitance of the silicon substrate, $C_{\text{Si sub}}$, is modeled by applying the parallel-wires capacitance model in (7). Thus, $C_{\text{Si sub}}$ is expressed as a function of d_{TSV}, p_{TSV}, h_{TSV}, and h_{IMD}. The $h_{\text{TSV}} - h_{\text{IMD}}$ term in Fig. 8 expresses the valid height where the electric fields are formed between the signal and ground TSVs in the silicon substrate. In addition, a material property, the relative permittivity of the silicon substrate, $\varepsilon_{\text{r,Si}}$, is also a variable of $C_{\text{Si sub}}$

$$C_{Si\ \text{sub}} = \frac{\pi \times \varepsilon_0 \varepsilon_{r,Si}}{\cosh^{-1}\left(\frac{p_{\text{TSV}}}{d_{\text{TSV}}}\right)} \times (h_{\text{TSV}} - h_{\text{IMD}})[F]. \tag{7}$$

In most circuit designs, the dielectric losses can be ignored since the conductor losses are dominant. However, as frequencies increase, it is important to consider the dielectric losses which vary with frequency. When dielectric losses are accounted for, the dielectric constant of the material becomes complex: $\varepsilon = \varepsilon' - j\varepsilon''$. Since the imaginary portion represents the losses, $1/\rho = 2\pi f \varepsilon''$ becomes the equivalent loss mechanism, where ρ is the effective resistivity of the dielectric material and f is the frequency. Thus, the loss tangent can characterize the loss in dielectrics with $tan|\delta d| = 1/2\rho\pi f\varepsilon = \varepsilon''/\varepsilon'$ and then the relationship between capacitance and conductance can be established as $G = \varepsilon''/\varepsilon'(2\pi f C)$, resulting in the relationship in (8) [19]. Thus, the conductance of the silicon substrate, $G_{\text{Si sub}}$, is proposed in (9). The physical origin of $G_{\text{Si sub}}$ is the silicon conductivity, σ_{Si}, which is predominantly determined by the majority carrier concentration. Therefore, it is another significant design parameter, which dominantly affects the insertion loss of a TSV

$$\frac{C_{Si\ \text{sub}}}{G_{Si\ \text{sub}}} = \frac{\varepsilon_{Si}}{\sigma_{Si}} \tag{8}$$

$$G_{Si\ \text{sub}} = \frac{\pi \times \sigma_{Si}}{\cosh^{-1}\left(\frac{p_{\text{TSV}}}{d_{\text{TSV}}}\right)} \times (h_{\text{TSV}} - h_{\text{IMD}})[S]. \tag{9}$$

The resistances of the TSV and bump, R_{TSV} and R_{Bump}, are also modeled with structural parameters, as shown in (10) and (11). High-frequency current flows close to the surface of the conductor due to the formation of the eddy current, which is called the "skin effect." To model R_{TSV} and R_{Bump} with a nonuniform current distribution at high frequencies, the depth of penetration, which is the skin depth, has to be determined to calculate the resistance of the TSV and bump. The skin depth is defined by material properties, such as the permeability in H/m and the conductivity in S/m, and also the frequency in Hz [19]. Therefore, the analytic equations of R_{TSV} and R_{Bump} are presented in (10) and (11), shown at the bottom of the next page.

In addition, there is another effect that induces current flow on the surface of the conductor, but is nonuniformly distributed around the perimeter by attracting currents to the inside-facing surfaces of the conductors, so called "proximity effect" [20]. This effect begins to appear after the skin effect onset frequency. The proximity factor, k_{p}, increases as round conducting wires such as TSVs are brought closely together. For TSVs and bumps, the magnitude of the proximity factor, k_{p}, is determined by the ratio $p_{\text{TSV}}/d_{\text{TSV}}$ or $p_{\text{Bump}}/d_{\text{Bump}}$ [21]. If other TSVs are located near the single-ended signal TSV, then this proximity effect between two TSVs or bumps does not have to be considered. Then, k_{p} is removed from the proposed equations.

As the operating frequency increases, the impedance of the inductance becomes more dominant than that of the resistance. Thus, the inductances of the TSV and bump, L_{TSV} and L_{Bump}, are modeled in (12) and (13). They are derived from the loop inductance model between two parallel conducting wires. The L_{TSV} and L_{Bump} terms are equivalently separated into the signal and ground nodes, as shown in Fig. 3(b). L_{TSV} and

L_{Bump} are also calculated using structural parameters, such as d_{TSV}, p_{TSV}, h_{TSV}, d_{Bump}, and h_{Bump} and material properties, such as the permeability of the TSV, $\mu_{\mathrm{r,TSV}}$ [17]

$$L_{\mathrm{TSV}} = \frac{1}{2}\left\{\frac{\mu_0\mu_{r,\mathrm{TSV}}}{2\pi} \times h_{\mathrm{TSV}} \times \ln\left(\frac{p_{\mathrm{TSV}}}{d_{\mathrm{TSV}}/2}\right)\right\}[\mathrm{H}] \tag{12}$$

$$L_{\mathrm{Bump}} = \frac{1}{2}\left\{\frac{\mu_0\mu_{r,\mathrm{Bump}}}{2\pi} \times h_{\mathrm{Bump}} \times \ln\left(\frac{p_{\mathrm{TSV}}}{d_{\mathrm{Bump}}/2}\right)\right\}[\mathrm{H}] \tag{13}$$

B. Modeling of the Redistribution Layer Interconnect

The RDL is a metal interconnect that provides horizontal interconnections between differently-sized stacked dies. For example, if two different dies with via-last processed TSVs are integrated vertically, RDL redistributes the signals to connect I/Os or power/grounds between dies. In a similar manner, to model a single-ended signal TSV with bumps, analytic $RLGC$ equations for the equivalent circuit model of a single-ended signal RDL are also proposed to estimate the electrical characteristics.

A single-ended signal RDL structure is shown in Fig. 9(a), and the proposed equivalent circuit model is shown in Fig. 9(b).

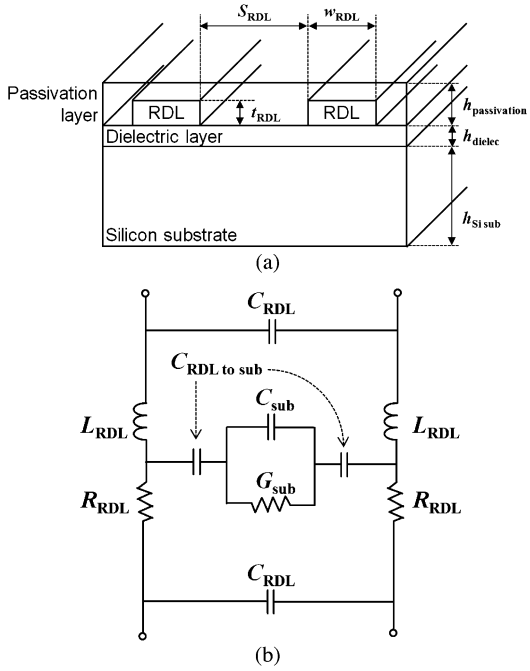

Fig. 9. (a) The structure of a single-ended signal RDL that has a signal RDL and a ground RDL on the dielectric layer labeled with its structural parameters, and (b) the proposed equivalent circuit model and $RLGC$ components of a single-ended signal RDL.

The resistance of an RDL, R_{RDL}, is also analytically modeled from the physical structure. Because the current flows along the

$$R_{\mathrm{TSV}} = \sqrt{(R_{\mathrm{dc,TSV}})^2 + (R_{\mathrm{ac,TSV}})^2}[\Omega]$$

where

$$\begin{aligned} R_{\mathrm{dc,TSV}} &= \rho_{\mathrm{TSV}} \times \frac{h_{\mathrm{TSV}}}{\pi \times \left(\frac{d_{\mathrm{TSV}}}{2}\right)^2}[\Omega] \\ R_{\mathrm{ac,TSV}} &= k_p\left(\rho_{\mathrm{TSV}} \times \frac{h_{\mathrm{TSV}}}{2\pi \times \frac{d_{\mathrm{TSV}}}{2} \times \delta_{\mathrm{skin\ \ depth,TSV}} - \pi\delta^2_{\mathrm{skin\ \ depth,TSV}}}\right)[\Omega] \\ \delta_{\mathrm{skindepth,TSV}} &= \frac{1}{\sqrt{\pi f \mu_{\mathrm{TSV}}\sigma_{\mathrm{TSV}}}}[\mathrm{m}] \\ R_{\mathrm{Bump}} &= \sqrt{(R_{\mathrm{dc,Bump}})^2 + (R_{\mathrm{ac,Bump}})^2}[\Omega] \end{aligned} \tag{10}$$

where

$$\begin{aligned} R_{\mathrm{dc,Bump}} &= \rho_{\mathrm{Bump}} \times \frac{h_{\mathrm{Bump}}}{\pi \times \left(\frac{d_{\mathrm{Bump}}}{2}\right)^2}[\Omega] \\ R_{\mathrm{ac,Bump}} &= k_p\left(\rho_{\mathrm{Bump}} \times \frac{h_{\mathrm{Bump}}}{2\pi \times \frac{d_{\mathrm{Bump}}}{2} \times \delta_{\mathrm{skindepth,Bump}} - \pi\delta^2_{\mathrm{skin\ \ depth,Bump}}}\right)[\Omega] \\ \delta_{\mathrm{skin\ \ depth,Bump}} &= \frac{1}{\sqrt{\pi f \mu_{\mathrm{Bump}}\sigma_{\mathrm{Bump}}}}[\mathrm{m}] \end{aligned} \tag{11}$$

surface of the RDL as frequency increases, frequency dependence is considered by calculating the skin depth [19]. Therefore, R_{RDL} is modeled in (14)

$$R_{\mathrm{RDL}} = \sqrt{(R_{\mathrm{dc,RDL}})^2 + (R_{\mathrm{ac,RDL}})^2}[\Omega/\mathrm{m}]$$

where

$$\begin{aligned} R_{\mathrm{dc,RDL}} &= \rho_{\mathrm{RDL}} \frac{1}{w_{\mathrm{RDL}} \times t_{\mathrm{RDL}}}[\Omega/\mathrm{m}] \\ R_{\mathrm{ac,RDL}} &= \rho_{\mathrm{RDL}} \frac{1}{w_{\mathrm{RDL}} \times \delta_{\mathrm{skindepth,RDL}}}[\Omega/\mathrm{m}] \\ \delta_{\text{skin depth,RDL}} &= \frac{1}{\sqrt{\pi f \mu_{\mathrm{RDL}} \sigma_{\mathrm{RDL}}}}[\mathrm{m}]. \end{aligned} \tag{14}$$

Notice that R_{RDL} is calculated by assuming that the current distribution is concentrated on the bottom edge of the RDL, which is caused by the E-fields between the signal RDL and the conductive silicon substrate pulling the charge to the bottom edge. If the space between the signal and ground RDLs, which are in parallel, is smaller than the height between the signal RDL and the silicon substrate, the current distribution concentrates at the lateral edge of the RDLs. Therefore, $R_{\mathrm{ac,RDL}}$ is calculated differently with t_{RDL}, and not with w_{RDL}.

As shown in (15), the inductance of the RDL, L_{RDL}, is modeled with the loop inductance model by approximation to the "two-wire transmission line model," which is equivalently balanced to the proposed model [22]

$$\begin{aligned} L_{\mathrm{RDL}} &= \frac{1}{2}(L_{\mathrm{signal}} + L_{\mathrm{ground}} - 2M) \\ &= \frac{1}{2}\left(\frac{\mu_0\mu_{r,\mathrm{RDL}}}{2\pi}\left[ln\left(\frac{2l_{\mathrm{RDL}}}{t_{\mathrm{RDL}}}\right) - \frac{3}{4}\right]\right. \\ &\quad + \frac{\mu_0\mu_{r,\mathrm{RDL}}}{2\pi}\left[ln\left(\frac{2l_{\mathrm{RDL}}}{t_{\mathrm{RDL}}}\right) - \frac{3}{4}\right] \\ &\quad \left. - 2\frac{\mu_0\mu_{r,\mathrm{RDL}}}{2\pi}\left[ln\left(\frac{2l_{\mathrm{RDL}}}{S_{\mathrm{RDL}}}\right) - 1\right]\right)[\mathrm{H/m}] \\ &= \frac{1}{2}\left(\frac{\mu_0\mu_{r,\mathrm{RDL}}}{2\pi}\left[2 \cdot \ln\left(\frac{S_{\mathrm{RDL}}}{t_{\mathrm{RDL}}}\right) + \frac{1}{2}\right]\right)[\mathrm{H/m}]. \end{aligned} \tag{15}$$

The structure of the RDL is similar to the on-chip metal, which is formed in IMD layer on the lossy silicon substrate. Thus, the RDL model can be derived from the on-chip metal interconnect model. To model the parasitic capacitances of the RDL, the fringe capacitances between the RDLs of the air, passivation layer, and dielectric layer have to be considered, as shown in Fig. 10(a). If the material between RDLs is changed, only the material property is altered in the proposed equations. The conformal mapping method is used to model those fringe capacitances between RDLs [14]. As a result, the capacitance between RDLs, C_{RDL}, is proposed as a superposition of all the fringe capacitances in parallel in

$$C_{\mathrm{RDL}} = C_{\mathrm{air}} + C_{\mathrm{passivation}} + C_{\mathrm{dielec}}[\mathrm{F/m}]$$

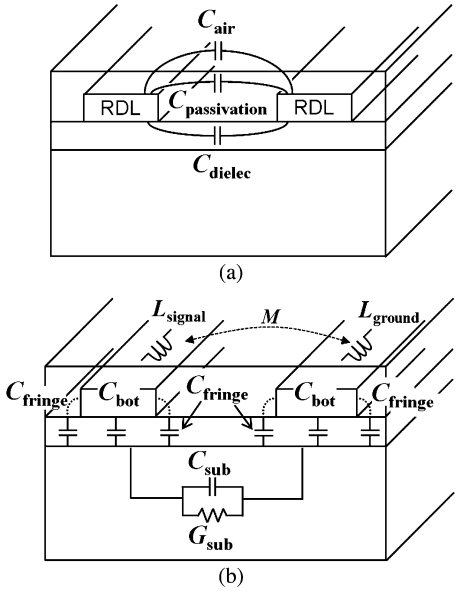

Fig. 10. The single-ended signal RDL structure (a) with the RDL capacitance components, which are calculated using the superposition of C_{air}, $C_{\mathrm{passivation}}$, and C_{dielec}, and (b) with the RDL inductance components, L_{signal} and L_{ground}, RDL-to-silicon substrate capacitances, C_{bot} and C_{fringe}, and the silicon substrate capacitance and conductance, C_{sub} and G_{sub}.

where

$$\begin{aligned} C_{\mathrm{air}} &= \varepsilon_0\varepsilon_{r,\mathrm{air}}\frac{K'(k_0)}{K(k_0)}[\mathrm{F/m}] \\ C_{\mathrm{passivation}} &= \varepsilon_0(\varepsilon_{r,\mathrm{passivation}} - \varepsilon_{r,\mathrm{air}})\frac{K'(k_1)}{K(k_1)}[\mathrm{F/m}] \\ C_{\mathrm{dielec}} &= \varepsilon_0(\varepsilon_{r,\mathrm{dielec}} - \varepsilon_{r,\mathrm{passivation}})\frac{K'(k_2)}{K(k_2)}[\mathrm{F/m}] \\ k_0 &= \sqrt{1 - \left(\frac{w_{\mathrm{RDL}}}{S_{\mathrm{RDL}}}\right)^2} \\ k_1 &= \sqrt{1 - \frac{sinh^2\left(\frac{\pi \cdot w_{\mathrm{RDL}}}{2h_{\mathrm{passivation}}}\right)}{sinh^2\left(\frac{\pi \cdot S_{\mathrm{RDL}}}{2h_{\mathrm{passivation}}}\right)}} \\ k_2 &= \sqrt{1 - \frac{sinh^2\left(\frac{\pi \cdot w_{\mathrm{RDL}}}{2h_{\mathrm{dielec}}}\right)}{sinh^2\left(\frac{\pi \cdot S_{\mathrm{RDL}}}{2h_{\mathrm{dielec}}}\right)}} \end{aligned} \tag{16}$$

where K is complete elliptical integral of the first kind.

Since the RDL is formed on the conductive silicon substrate, electromagnetic fields are formed between the RDL and the conductive silicon substrate. Therefore, the capacitance of the RDL-to-silicon substrate, $C_{\mathrm{RDL\_to\_sub}}$, which is shown in Fig. 10(b), is calculated with the conformal mapping method in (17) [15]

$$\begin{aligned} C_{\mathrm{RDL\_to\_sub}} &= C_{\mathrm{bot}} + 2C_{\mathrm{fringe}} \\ &= \varepsilon_0\varepsilon_{r,SiO_2} \times \frac{w_{\mathrm{RDL}}}{h_{\mathrm{dielec}}} \\ &\quad + \varepsilon_0\varepsilon_{r,SiO_2}\frac{K\left(k_{[VP]}\right)}{K'\left(k_{[VP]}\right)}[\mathrm{F/m}] \end{aligned}$$

where

$$k_{[VP]} = \sqrt{1 - \left(\frac{h_{\text{dielec}}}{h_{\text{dielec}} + t_{\text{RDL}}}\right)^2}. \tag{17}$$

When the signal propagates along the RDL, the electric field can penetrate into not only the dielectric layer but also the silicon substrate between the signal and ground RDLs. Hence, the capacitance and conductance of the silicon substrate under the RDLs, C_{sub} and G_{sub}, is also modeled. The C_{sub} is modeled with the effective penetration depth of the electric field into the silicon substrate, h_{eff}, as shown in (18) [16]. With the relationship between the capacitance and the conductance, as shown in (8), G_{sub} is derived from C_{sub}, which is presented in (19)

$$C_{\text{sub}} = \varepsilon_0 \varepsilon_{r,\text{eff}} \frac{w_{\text{RDL}}}{h_{\text{eff}}} [\text{F/m}] \tag{18}$$

$$G_{\text{sub}} = \sigma_{\text{eff}} \frac{w_{\text{RDL}}}{h_{\text{eff}}} [\text{S/m}] \tag{19}$$

where

$$\varepsilon_{r,\text{eff}} = \frac{\varepsilon_{r,Si} + 1}{2} + \frac{\varepsilon_{r,Si} - 1}{2\sqrt{1 + 10\left(\frac{h}{w_{\text{RDL}}}\right)}}$$

$$\sigma_{\text{eff}} = \frac{\sigma_{Si}}{2} + \frac{\sigma_{Si}}{2\sqrt{1 + 10\left(\frac{h}{w_{\text{RDL}}}\right)}}$$

$$h_{\text{eff}} = \frac{w_{\text{RDL}}}{2\pi} ln\left(\frac{8h}{w_{\text{RDL}}} + \frac{w_{\text{RDL}}}{4h}\right)$$

$$h = h_{\text{dielec}} + h_{Si\ \text{sub.}}$$

III. Verification of the Proposed High-Frequency Scalable Electrical Model of a TSV Channel

To verify the proposed scalable model of a TSV channel, *S*-parameters from the proposed model and a 3-D field solver are compared in this section. From these comparisons with d_{TSV}, h_{TSV}, and p_{TSV}, varying the proposed model is validated up to 20 GHz from well matched results. The proposed model is experimentally validated with a series of fabricated test vehicles, which include the TSVs, bumps, and RDLs. The proposed model of a TSV with bumps and RDLs is experimentally verified with S-parameter measurements up to 20 GHz.

A. Simulation-Based Verification of the Proposed Scalable Model of a TSV With Bumps

The scalability of the proposed TSV channel model is verified by simulation with the 3-D field solver, HFSS of Ansoft. Among many design parameters, d_{TSV}, h_{TSV}, and p_{TSV} are swept to validate the scalability of the proposed model up to 20 GHz.

As shown in Fig. 11(a), the proposed scalable model is verified with d_{TSV} changed. As d_{TSV} varies from 10 μm to 30 μm, the S_{21} magnitude increases over the entire frequency range. The proposed scalable model estimates the change of the S_{21} magnitude and S_{21} phase well as compared to those computed from the 3-D field solver with d_{TSV} variation. The proposed model with h_{TSV} variation is also validated, as shown in Fig. 11(b). As h_{TSV} increases, the insertion loss, as shown by the S_{21} magnitude, increases. These results are due to the increased capacitance and conductance of the silicon substrate, resulting in the decreased impedance between signal and ground TSVs. The proposed scalable model estimates the S_{21} magnitude and S_{21} phase well as compared to the 3-D field solver when h_{TSV} is varied from 30 μm to 70 μm. As shown in Fig. 11(c), the proposed scalable model with p_{TSV} variation is also validated. As p_{TSV} varies from 100 μm to 140 μm, there is a good agreement between the proposed scalable model and the 3-D field solver up to 20 GHz.

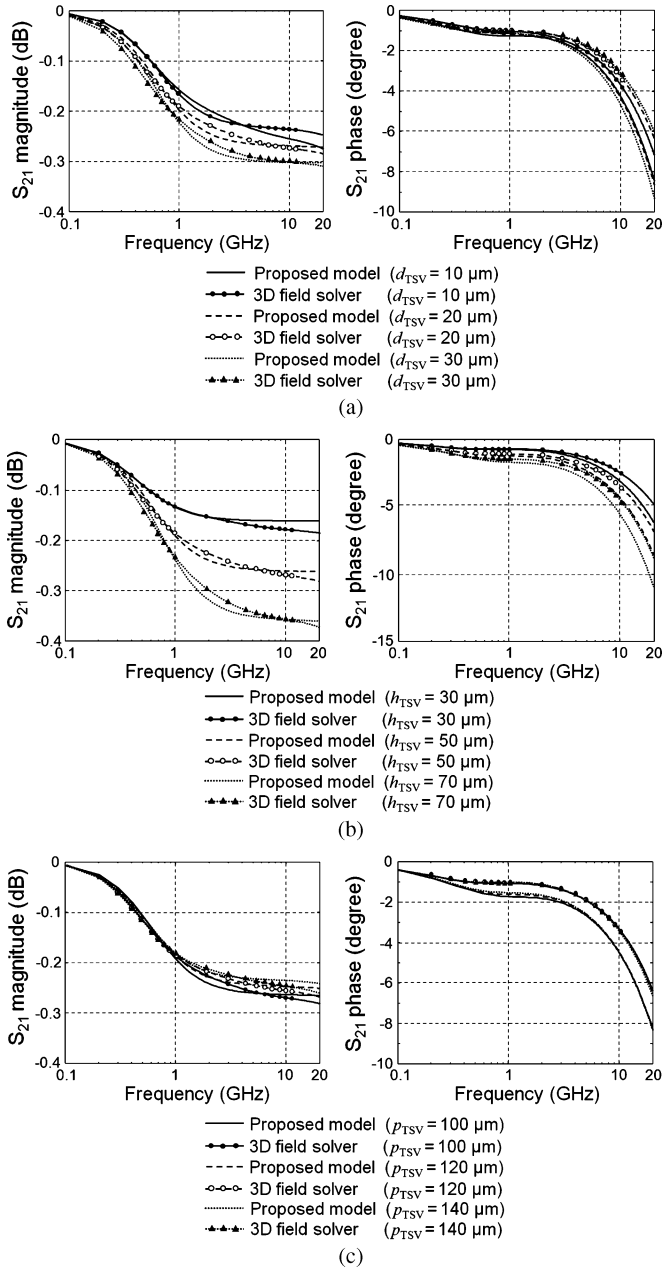

Fig. 11. S_{21} magnitudes and phases for the verification of the proposed scalable model of TSVs with bumps by comparing the proposed model to the simulation with a 3-D field solver: (a) TSV diameter (d_{TSV}), (b) TSV height (h_{TSV}), and (c) TSV-to-TSV pitch (p_{TSV}). The other TSV and bump dimensions are fixed as d_{TSV} of 30 μm, h_{TSV} of 50 μm, p_{TSV} of 100 μm, t_{ox} of 0.5 μm, d_{Bump} of 50 μm, h_{Bump} of 10 μm, and h_{IMD} of 10 μm.

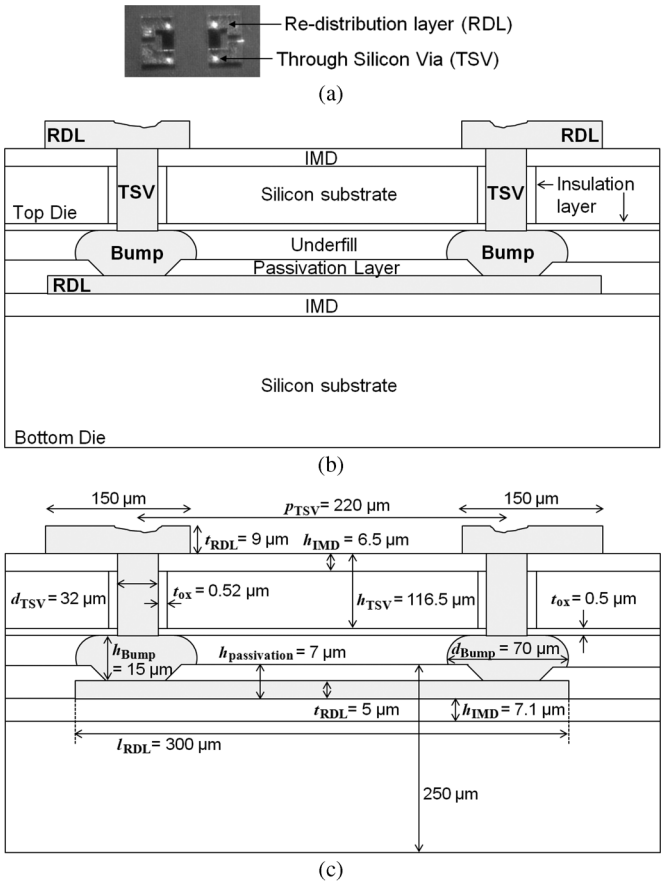

Fig. 12. (a) A top-view photograph of the test chip, (b) the cross-sectional view and (c) the detail dimensions of the fabricated test vehicle, which is the TSV channel including the TSVs, bumps, and RDLs. The RDL on the bottom die provides horizontal connection between TSVs on the top die.

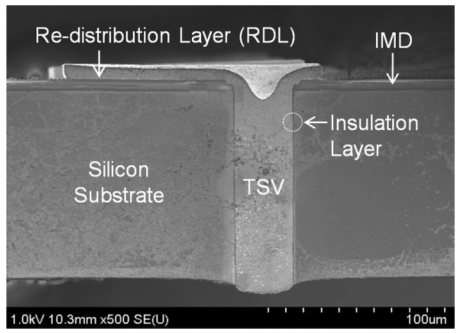

Fig. 13. An SEM image of the fabricated TSV with RDL, which is connected to the TSV on the IMD layer. The TSV and RDL are formed with copper (Cu). The IMD layer and the insulation layer are formed with silicon dioxide (SiO_2). The TSV, which is filled with Cu and surrounded by SiO_2 passes through the silicon substrate vertically with the via-last process.

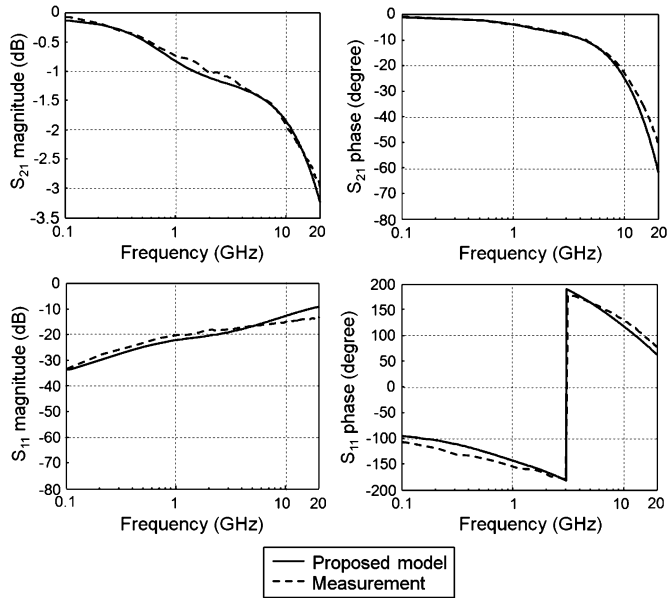

Fig. 14. Verification of the proposed model by comparing the measured *S*-parameters with the calculated S parameters from the model of the fabricated single-ended signal TSV channel, which includes not only TSVs, but also bumps and RDLs.

It should be observed, however, that there is an additional inductive effect from the inductance of the lumped ports when simulating with the 3-D field solver, which causes increments of the slope of the S_{21} magnitudes over 10 GHz. Thus, there are some discrepancies between the calculated results from the proposed model and the simulation results from the 3-D field solver over 10 GHz, as shown in Fig. 11(a), (b), and (c).

B. Experimental Verification of the Proposed Model of a TSV With Bumps and RDLs

To experimentally validate the proposed equivalent circuit model of the TSV, a series of test vehicles were fabricated, as shown in Fig. 12. In Fig. 12(a), there is a picture of the top view of the fabricated test vehicle. The fabricated vehicles are composed of two signal and ground TSV pairs and two signal and ground RDL pairs on the top die, as shown in Fig. 12(b). There is a signal and ground RDL pair on the bottom die, which provides a connection between the two TSV pairs. There are bumps that connect the TSV on the top die and the RDL on the bottom die. Therefore, a test vehicle of a TSV channel, which is stacked with two dies, is designed with TSVs, bumps, and RDLs, with dimensions provided in Fig. 12(c). As shown in Fig. 13, the TSV is formed as a vertical hole through the silicon substrate with the via-last process, which is then filled with copper and surrounded by a thin SiO_2 layer. The RDL is formed as a horizontal layer with copper on the IMD layer, which is connected to the TSV.

The proposed scalable model is experimentally verified with S-parameter measurements using on-chip cascade probes and a vector network analyzer (VNA), the Agilent N2530A. Measurement results are compared to those from the proposed equivalent circuit model of the fabricated test vehicle. The comparisons of the magnitudes and phases of both the S_{21} and S_{11} from the proposed model and measurement are shown in Fig. 14. The proposed model and the measurement are well correlated up to 20 GHz. As a result, we experimentally verified the proposed electrical model of the TSV channel. It should be noted that the model for the verification includes the mutual effect between two TSV pairs on the top die.

With the confirmed model, the electrical behavior of a TSV channel is analyzed. In addition, the proposed analytic and closed-form equations can be used to estimate the power consumption, delay, and skew of a TSV channel. The equations

can also be combined with other circuits to evaluate the signal performance in 3-D IC design. Since the model is scalable, it can estimate the electrical behavior depending on design parameters.

In the next section, the electrical characteristics of the TSV channel are analyzed with the experimentally verified model. Therefore, we analyze how each design parameter affects the electrical behavior of the TSV channel, and which $RLGC$ component dominantly determines insertion losses of the TSV channel in different frequency ranges.

IV. Analysis of Electrical Characteristics of a TSV Channel

In this section, the electrical characteristics of a TSV channel are analyzed with the proposed scalable equivalent circuit model, which is experimentally verified in the previous section. The configuration of the TSV channel, which is used for the analysis in this section, is the same as that of the fabricated test vehicle. In the frequency-domain analysis, the dominant design parameters are determined in specific frequency ranges by analyzing the insertion losses with S_{21} magnitudes. Among the many design parameters, the electrical characteristics of TSVs with bumps and RDLs are analyzed with $t_{\rm ox}$, $p_{\rm TSV}$, $d_{\rm TSV}$, $h_{\rm TSV}$, RDL length ($l_{\rm RDL}$), and $\sigma_{\rm Si}$. The frequency dependent loss of the TSV channel is analyzed by categorizing the measured frequency range into three parts: region [A] for 0–2 GHz, region [B] for 2–10 GHz and region [C] for 10–20 GHz. Hence, the design parameter which dominantly influences the electrical characteristic of a TSV channel is determined in each frequency range. In addition, eye diagram measurements with data rates up to 10 Gb/s are conducted for the time-domain analysis of the TSV channel. From the voltage and timing margin variations as the data rate increases or the design parameter varies, the electrical behaviors of the TSV channel are analyzed.

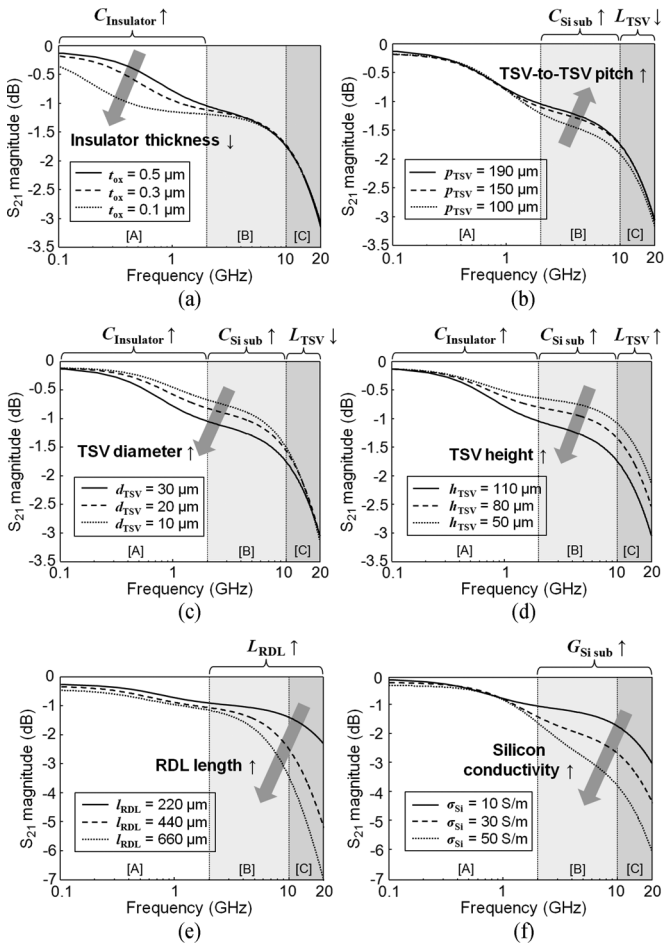

Fig. 15. S_{21} magnitudes from the proposed equivalent circuit model of a TSV channel with (a) TSV Insulator thickness variation; (b) TSV-to-TSV pitch variation; (c) TSV diameter variation; (d) TSV height variation; (e) RDL length variation; and (f) conductivity of the silicon substrate.

A. Frequency-Domain Analysis for Electrical Characterization of a TSV Channel

For the TSV structure, an insulation layer has to be formed to isolate the TSV from the conductive silicon substrate. The capacitance, $C_{\rm Insulator}$ is directly affected by variation in $t_{\rm ox}$ which is explained in the proposed equation in Section II. Thus, $C_{\rm Insulator}$ increases as $t_{\rm ox}$ decreases. As $t_{\rm ox}$ decreases from 0.5 μm to 0.1 μm, $C_{\rm Insulator}$ increases from 0.8 to 3.9 pF. The insertion loss through the TSV is dominated by the leakage through the conductive silicon substrate after passing through the insulator. As a result, an increase of $C_{\rm Insulator}$ results in increased insertion loss due to the lowered impedance along the leakage path to the silicon substrate given by the equation, $Z = 1/j\omega C$. Therefore, the insertion loss through a TSV can be reduced by increasing the thickness of the insulator. However, with current technology to form an insulation layer around a TSV, the thickness of the insulator, which is generally SiO_2, is limited to under 0.5 μm. This is due to process limitations in oxidizing a via with a high aspect ratio, which is also related to cost. In addition, the value of $C_{\rm Insulator}$ is relatively big as compared to that of other parasitic capacitances of a few fF such as the $C_{\rm Underfill}$, $C_{\rm IMD}$, and $C_{\rm Bottom}$. In a similar manner, if the thickness of the bottom oxide, $t_{\rm ox,bot}$, decreases, the impedance of $C_{\rm Bump2}$ rapidly decreases as frequency increases. With $t_{\rm ox,bot}$ of 0.5 μm, $C_{\rm Bump2}$ is 0.2 pF. Thus, if $t_{\rm ox,bot}$ decreases and $d_{\rm Bump}$ increases, $C_{\rm Bump2}$ can bring more significant impact than $C_{\rm Insulator}$ in region [A].

Therefore, the capacitive effect due to the insulation layer dominates the capacitive characteristic in the low frequency range, region [A], as shown in Fig. 15(a). In this region, the insertion loss rapidly increases as frequency increases due to the decreasing impedance of $C_{\rm Insulator}$.

As the pitch between the signal and ground TSVs decreases, the physical distance between signal and ground decreases. Hence, the silicon substrate capacitance and conductance of a TSV, $C_{\rm Si\,sub}$ and $G_{\rm Si\,sub}$ increase, which results in an increased insertion loss. As shown in Fig. 15(b), as $p_{\rm TSV}$ decreases from 190 μm to 100 μm, $C_{\rm Si\,sub}$ increases from 5 to 6.7 fF. Since $C_{\rm Si\,sub}$ is less than 10 fF, which is a relatively small capacitance as compared to $C_{\rm Insulator}$, which has a capacitance of a few pF, this capacitive effect appears at relatively higher frequency than that of $C_{\rm Insulator}$. In addition, there is another loss term from the silicon substrate under the RDL, $G_{\rm sub}$. It also contributes to the insertion loss through the TSV channel. If the height between the RDL and the silicon substrate becomes smaller and the length of the RDL increases, the effect from $G_{\rm sub}$ increases.

Thus, the resistive losses from the RDL itself and the silicon substrate under the RDLs become significant as the length of the RDL increases beyond a mm, and the width and thickness of the RDL decreases in 3-D IC design.

The significant factor that determines the amount of resistive loss through a TSV is the silicon substrate because it is conductive and TSVs are formed passing through it vertically. However, there is another resistive loss factor from the TSV itself, $R_{\rm TSV}$. The resistive loss from $R_{\rm TSV}$, in the case that it is made from copper, is negligible due to the comparatively small value of resistance, which is a few $\rm m\Omega$. If the metal filling the TSV is tungsten or poly silicon, which has a higher resistivity than copper, the resistive loss due to $R_{\rm TSV}$ will contribute more to the overall resistive loss through the TSV interconnect.

There is no significant change in the insertion loss for region [C], even with the decrease of $p_{\rm TSV}$ resulting in an increase of $C_{\rm Si\ sub}$ and $G_{\rm Si\ sub}$, which dominantly affect the loss term. This is due to the decrease in inductances such as $L_{\rm TSV}$, $L_{\rm Bump}$, and $L_{\rm RDL}$, as $p_{\rm TSV}$ decreases. A decrease in the inductance of the TSV channel reduces the insertion loss in region [C]. Thus, the effects on the insertion loss from the decreased inductance and increased $C_{\rm Si\ sub}$ and $G_{\rm si\ sub}$ compensate each other in region [C] and make the loss steady even with the $p_{\rm TSV}$ varying.

As a result, pitch variation dominantly affects the electrical characteristic of a TSV channel in region [B]. In addition, this effect is gradually reduced as frequency increases over 10 GHz due to the increased inductance effect from the TSVs, bumps, and RDLs.

Variation in $d_{\rm TSV}$ changes almost all the $RLGC$ components of the proposed equivalent circuit model of a TSV channel. With increasing $d_{\rm TSV}$, the effective distance between the signal and ground TSV decreases, when $p_{\rm TSV}$ is fixed. Therefore, $C_{\rm Si\ sub}$ and $G_{\rm Si\ sub}$ increase, which increases the insertion loss. In addition, $C_{\rm Insulator}$ increases due to an increase of the effective area where the TSV faces the silicon substrate through the insulation layer. Therefore, overall insertion loss in region [A] and [B] increases as $d_{\rm TSV}$ increases, as shown in Fig. 15(c).

In a similar manner with the previous analysis for $p_{\rm TSV}$ variation, the decreased inductance effect from $L_{\rm TSV}$, which makes the insertion loss constant even with the increase of $C_{\rm Si\ sub}$ and $G_{\rm Si\ sub}$, is shown in region [C], Fig. 15(c). As $d_{\rm TSV}$ increases from 10 μm to 30 μm, $L_{\rm TSV}$ decreases from 20.8 pH to 14.7 pH. Thus, there are no big insertion loss changes even with $d_{\rm TSV}$ variation in region [C]. In addition, $R_{\rm TSV}$ also decreases as $d_{\rm TSV}$ increases. However, this resistance is too small to be considered as discussed in the previous analysis for $p_{\rm TSV}$ variation. Thus, the overall characteristic of the TSV channel with $d_{\rm TSV}$ increasing results in the increased insertion loss, which is dominantly determined by $C_{\rm Si\ sub}$ and $G_{\rm Si\ sub}$. In summary, $d_{\rm TSV}$ affects the frequency dependent loss of the TSV channel in almost all frequency ranges, but is dominant in regions [A] and [B].

As shown in Fig. 15(d), the insertion loss of the TSV channel increases in all frequency ranges as $h_{\rm TSV}$ increases from 50 μm to 110 μm, because it not only increases $C_{\rm Insulator}$ and $C_{\rm Si\ sub}$, but also increases $L_{\rm TSV}$. Therefore, the increasing $h_{\rm TSV}$ increases the insertion loss in all frequency ranges, regions [A], [B], and [C]. In a similar manner to the analysis of $t_{\rm ox}$ variation, $C_{\rm Insulator}$ dominantly affects the insertion loss in region [A]. In region [B], $C_{\rm Si\ sub}$ and $G_{\rm Si\ sub}$ are the dominant factors that determine the insertion loss as analyzed for both $p_{\rm TSV}$ and $d_{\rm TSV}$. In region [C], the inductances of the TSV channel start to affect the insertion loss.

As shown in Fig. 15(e), as $l_{\rm RDL}$ increases from 220 μm to 660 μm, the insertion losses in regions [B] and [C] increase due to an increase in $L_{\rm RDL}$ and $R_{\rm RDL}$. From this analysis, it is apparent that regions [B] and [C] are dominantly affected by the inductive characteristic of the RDL. As $l_{\rm RDL}$ increases from 220 μm to 660 μm, LTSV increases from 150 pH to 452 pH. As the operating frequency increases over a few Gb/s, the RDL routing becomes a critical design issue for high-speed 3-D IC channel design to guarantee signal quality.

Silicon conductivity, $\sigma_{\rm Si}$, is a material property that has a considerable influence on the electrical characteristics of the TSV channel. Because it changes $G_{\rm Si\ sub}$ and $G_{\rm sub}$, which determines overall insertion loss of a TSV channel. As $\sigma_{\rm Si}$ increases from 10 S/m to 50 S/m, $G_{\rm Si\ sub}$ increases from 1.4 mS to 6.98 mS. As a result, the insertion loss of the TSV channel increases. The $\sigma_{\rm Si}$ change does not dominantly affect the insertion loss in region [A], however, in regions [B] and [C], it does. Therefore, the important design parameters of the TSV channel in 3-D IC are not only the physical parameters but also the material properties.

In summary, the electrical characteristics of the TSV channel are analyzed with insertion loss data up to 20 GHz. The TSV channel has capacitive and resistive characteristics, and is also frequency dependent. The overall loss of the TSV channel is determined to be dominated by the conductance of the silicon substrate. If the RDL length increases to the mm range, the RDL contributes significantly to the loss of the TSV channel. The overall electrical behavior has a capacitive characteristic from the parasitic capacitances whose impedances change as frequency varies. However, the frequency dependence is determined to be dominated by the parasitic inductances of the TSV channel over 10 GHz. As a result, the capacitive TSV effect is dominant in the lower frequency range, and the inductive RDL effect becomes dominant in the higher frequency range.

With these analyses, we summarize the design parameters and $RLGC$ components which have a major impact on the frequency dependent loss of the TSV channel. As shown in Fig. 16, there are design parameters which dominantly determine the frequency dependent loss of the TSV channel; $t_{\rm ox}$, $t_{\rm ox,bot}$, and $d_{\rm TSV}$ in region [A], $p_{\rm TSV}$ and $h_{\rm TSV}$ in region [B], $h_{\rm TSV}$ and $l_{\rm RDL}$ in region [C]. Additionally, the dominant $RLGC$ components of the proposed model of the TSV channel are summarized; $C_{\rm Insulator}$ in region [A], $C_{\rm Si\ sub}$ in region [B], $L_{\rm TSV}$ and $L_{\rm RDL}$ in region [C]. Other RLGC components which have a minor impact in each frequency range are summarized; $C_{\rm Bump2}$ have a minor impact in region [A], $C_{\rm Underfill}$, $C_{\rm IMD}$, $C_{\rm Bottom}$, $C_{\rm RDL}$, $C_{\rm RDL\_to\_sub}$, and $C_{\rm sub}$, have a minor impact in region [B] and [C].

B. Time-Domain Analysis of the Frequency Dependent Loss of the TSV Channel

For the time-domain analysis, eye diagram measurements are conducted on the fabricated TSV channel, which includes the

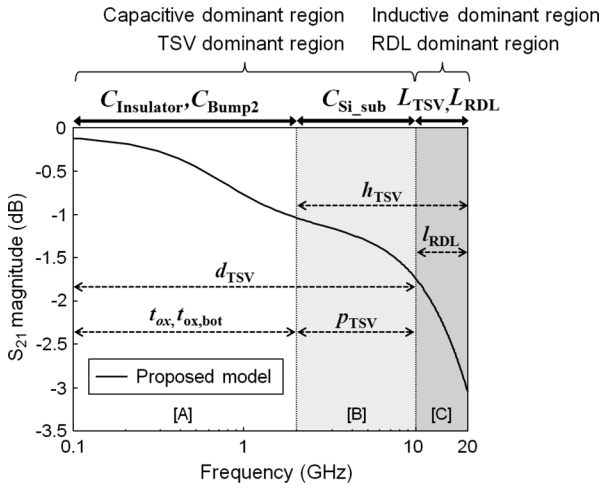

Fig. 16. S_{21} magnitude from the proposed model showing dominant design parameters and $RLGC$ components, which determine the insertion loss for the different frequency ranges: in the lower frequency range, the capacitive TSV effect dominates; in the higher frequency ranges, the RDL effect, which is inductive, becomes dominant.

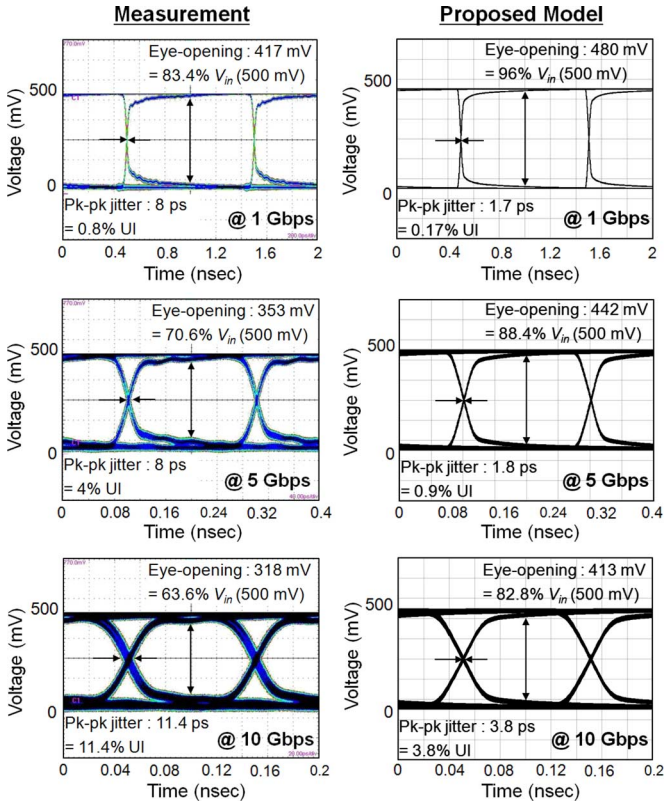

Fig. 17. Eye diagrams from the measurement and the proposed model with 1 Gb/s, 5 Gb/s, and 10 Gb/s random data of $2^{31}-1$ bits traveling through the fabricated TSV channel. As the data rate increases, the normalized eye opening decreases and the normalized pk-pk jitter increases due to the frequency dependent loss of the TSV channel, which are capacitive and resistive.

TSVs, bumps, and RDLs. The input signal is a $2^{31}-1$ pseudo-random bit sequence with an amplitude of 500 $\mathrm{mV_{p-p}}$. The output waveforms are monitored using a digital sampling oscilloscope, Tektronix/TDS8000B, equipped with a 20 GHz sampling module.

The eye diagrams from the measurement and the proposed model with data rates of 1 Gb/s, 5 Gb/s, and 10 Gb/s with random data of $2^{31}-1$ bits transmitting through the fabricated TSV channel are shown in Fig. 17. The shapes of the eye diagrams from the measurement and the proposed model are well matched. However, there are some differences in the eye opening and the pk-pk jitter between the measurement and the proposed model. Those differences are due to the cables used for the measurement that bring additional 1.4 dB, 3.6 dB, and 4.3 dB losses at 500 MHz, 2.5 GHz, and 5 GHz, respectively. Therefore, the eye openings with 1 Gb/s, 5 Gb/s, and 10 Gb/s random data are smaller than that from the proposed model by several tens of mV. In addition, the measured pk-pk jitter is larger than that from the proposed model by 6–7 ps, because there is random jitter produced from the measurement equipment, the pulse pattern generator (PPG), and jitter additionally caused by the two cables used for the measurements.

From the measured eye diagrams in Fig. 17, as the data rate increases, the voltage and timing margins decrease, which are presented with the normalized eye-opening and pk-pk jitter. The normalized eye-opening and pk-pk jitter are 83.4% and 0.8%, respectively, for data rates of 1 Gb/s. As the data rate is increased to 5 Gb/s and 10 Gb/s, the normalized eye-opening decreases to 70.6% and 63.6% and the normalized pk-pk jitter increases to 4% and 11.4%. Signals through the TSV channel, however, have open eyes because of the short interconnection length of the TSV and RDL, even with a data rate of 10 Gb/s.

Since the TSV channel has capacitive and resistive characteristics as analyzed in the previous section on the frequency-domain analysis, it has a frequency dependent loss. In addition, because the energy of the signal is predominantly concentrated at the Nyquist frequency, the insertion loss is not constant in frequency domain, however, increases as the data rate increases. Thus, the amount of signal degradation through the TSV channel increases as the frequency increases. For example, the energy of the signal with a data rate of 1 Gb/s is mostly concentrated at 0.5 GHz. From the measurement results, the insertion loss at 0.5 GHz for the TSV channel is -0.5 dB. However, with a data rate of 10 Gb/s, the TSV channel has insertion loss at the Nyquist frequency, 5 GHz, of -1.5 dB. Thus, the frequency dependent loss in the frequency domain directly results in the increase of the rise time of the signal in the time domain as operating frequency increases. Furthermore, if the frequency dependent loss of the TSV channel becomes severe, it can cause inter-symbol interference (ISI), which is the signal degradation of the timing and signal integrity margins [19].

However, as 3-D integration density increases, the number of dies, which have to be vertically integrated in one system, increases. Thus, high-speed I/O signals pass through many TSVs. This can cause an additional capacitive load due to the increasing parasitic capacitances of the TSVs. It results in an increased rise time and timing jitter of the signal. Based on the model and analysis of the TSV channel in the previous sections, as d_{TSV} and h_{TSV} becomes smaller or t_{ox} becomes thicker, the capacitive load from the TSV can be reduced. Therefore, we can sharpen the rising edge of the signal for better system performance and increases the bandwidth of the TSV interconnect with d_{TSV}, h_{TSV}, and t_{ox} varying. In a similar manner, if there are more than two RDL layers and are densely routed,

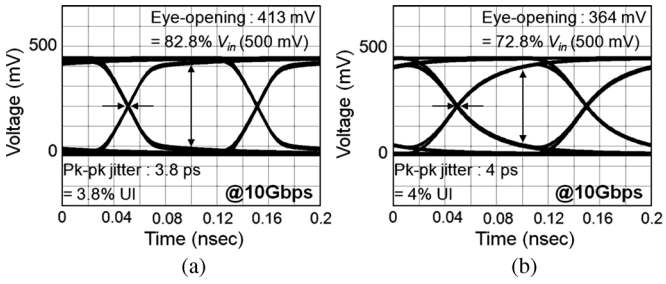

Fig. 18. Eye diagrams of the proposed model with 10 Gb/s pseudo-random data traveling through (a) 2 TSV pairs and RDLs; and (b) 8 TSV pairs and RDLs.

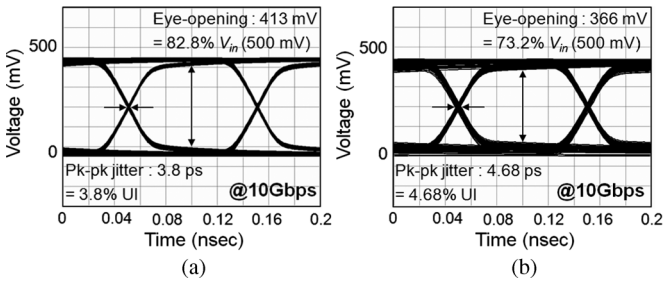

Fig. 19. Eye diagrams of the proposed model with 10 Gb/s random data traveling through 2 TSV pairs and RDLs with (a) $t_{\rm ox}$ of 0.5 μm; and (b) $t_{\rm ox}$ of 0.1μm.

the capacitive load from the RDLs also increases. In this case, we can also reduce the capacitance from the RDLs by reducing $w_{\rm RDL}$, increasing $S_{\rm RDL}$, minimizing the routed length of RDL, etc. In the case of 3-D architectures whose RDL has to be long and implemented with many layers, the capacitive loading from the RDL becomes significantly more severe than that from the TSV.

Eye diagrams which are computed with the proposed model are shown in Fig. 18, for signals passing through a different number of TSV pairs and RDLs. As the number of TSVs that the signal is traveling increases from 2 to 8, and the length of RDL increases from 500 μm to 2 mm, the eye-opening decreases 10% and the pk-pk jitter increases 0.2%. We can confirm the effect from the increased capacitance of the TSV channel with these computed eye diagrams from the proposed model. Even though the eye is still clearly open, if the coupling ratio among the TSVs increases significantly or the RDL coupling increases from the long and dense routing, the eye can become more degraded.

In addition, as analyzed in the frequency-domain analysis, if the thickness of the insulator, $t_{\rm ox}$, becomes thinner, the insertion loss of the low frequency components, especially under 2 GHz, increases, even though the high frequency components almost does not change. Hence, as shown in Fig. 19, the slope of the rising edge, where the high frequency components are concentrated, does not change, when the $t_{\rm ox}$ is decreased from 0.5 μm to 0.1 μm.

Therefore, we analyzed and confirmed the frequency dependent loss of a TSV channel in the time domain, which was characterized in the frequency domain in the previous section.

V. Conclusion

We proposed a high-frequency scalable model of the TSV. The proposed model was developed with analytic $RLGC$ equations which were derived from the physical configuration. The scalability of the proposed model of the TSV was validated by simulation with the 3-D field solver. To experimentally verify the proposed model of the TSV, a series of test vehicles, which include TSVs, bumps and RDLs, were fabricated. The proposed model of the TSV with bumps and RDLs, so called TSV channel, was validated by S-parameter measurement up to 20 GHz with the fabricated test vehicles. Based on the proposed scalable model of the TSV channel, we analyzed the electrical characteristics from $\rm S_{21}$ magnitudes with design parameter variations of the TSV channel. The electrical behaviors of the TSV channel were analyzed in the frequency and time domains. Then, dominant design parameters of the TSV channel were extracted in different frequency ranges. In the low frequencies, the TSV dominantly affects the overall characteristic of the TSV channel, and is capacitively-dominant. As the frequency increases, the electrical characteristics are dominantly affected by the RDL, which is inductively-dominant. For the time domain analysis, eye diagram measurements were conducted with the fabricated TSV channel with a PRBS input signal up to 10 Gb/s. Due to the frequency dependent loss of the TSV channel, the signal through the TSV channel was degraded as the data rate was increased. It resulted in decreased voltage and timing margins, which were represented with the normalized eye opening and pk-pk jitter.

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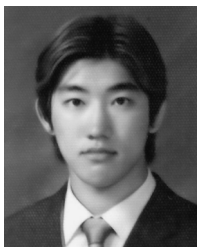

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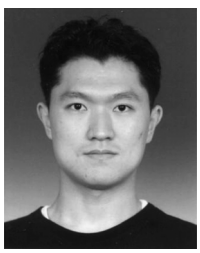

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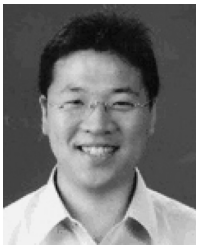

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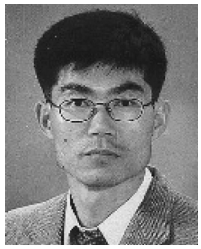

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