Digital Phase-Locked Loops

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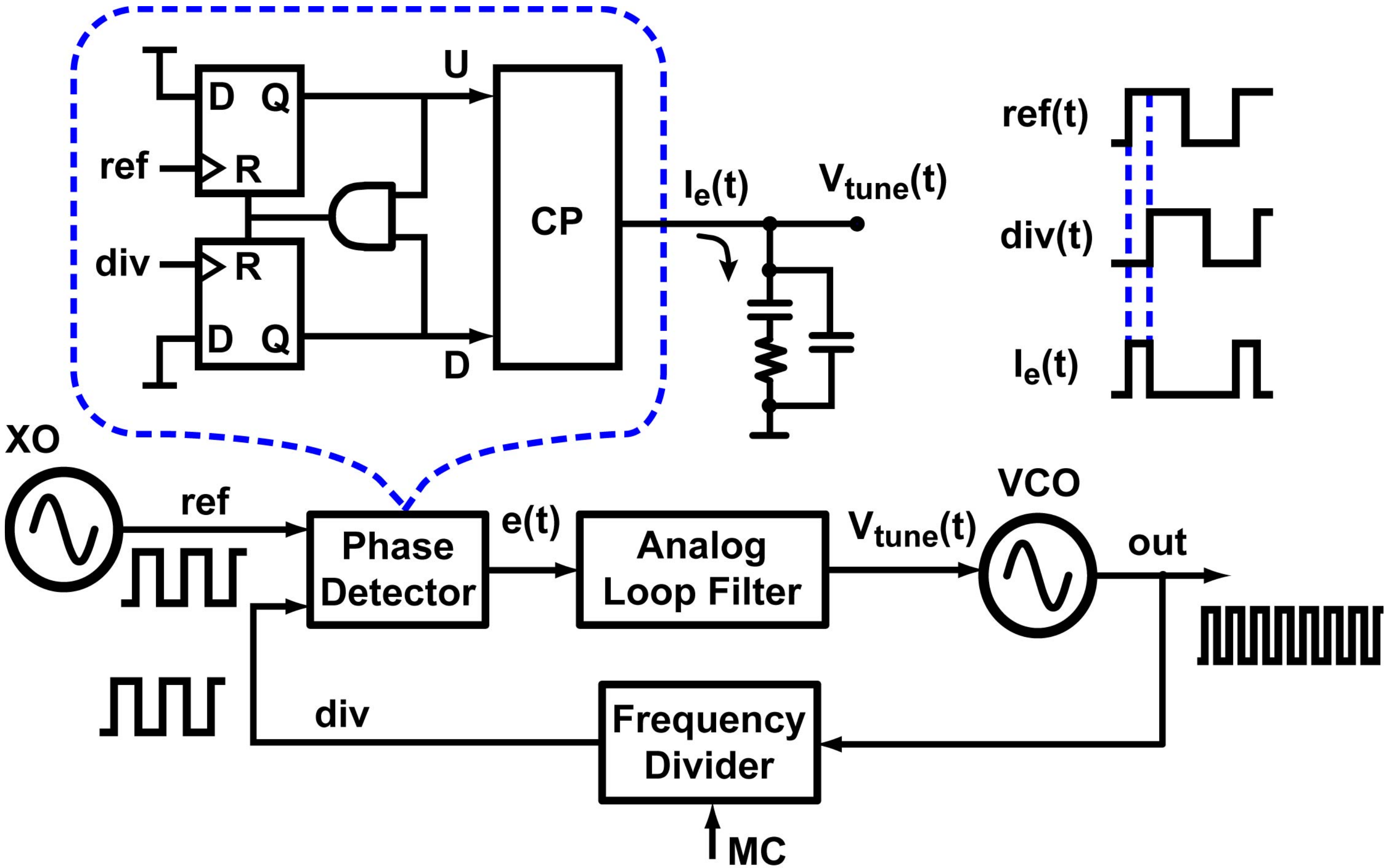
POLITECNICO MILANO 1863

San Diego, 8 April 2018

Most Typical PLL Implementation



Motivation to Investigate Digital PLLs

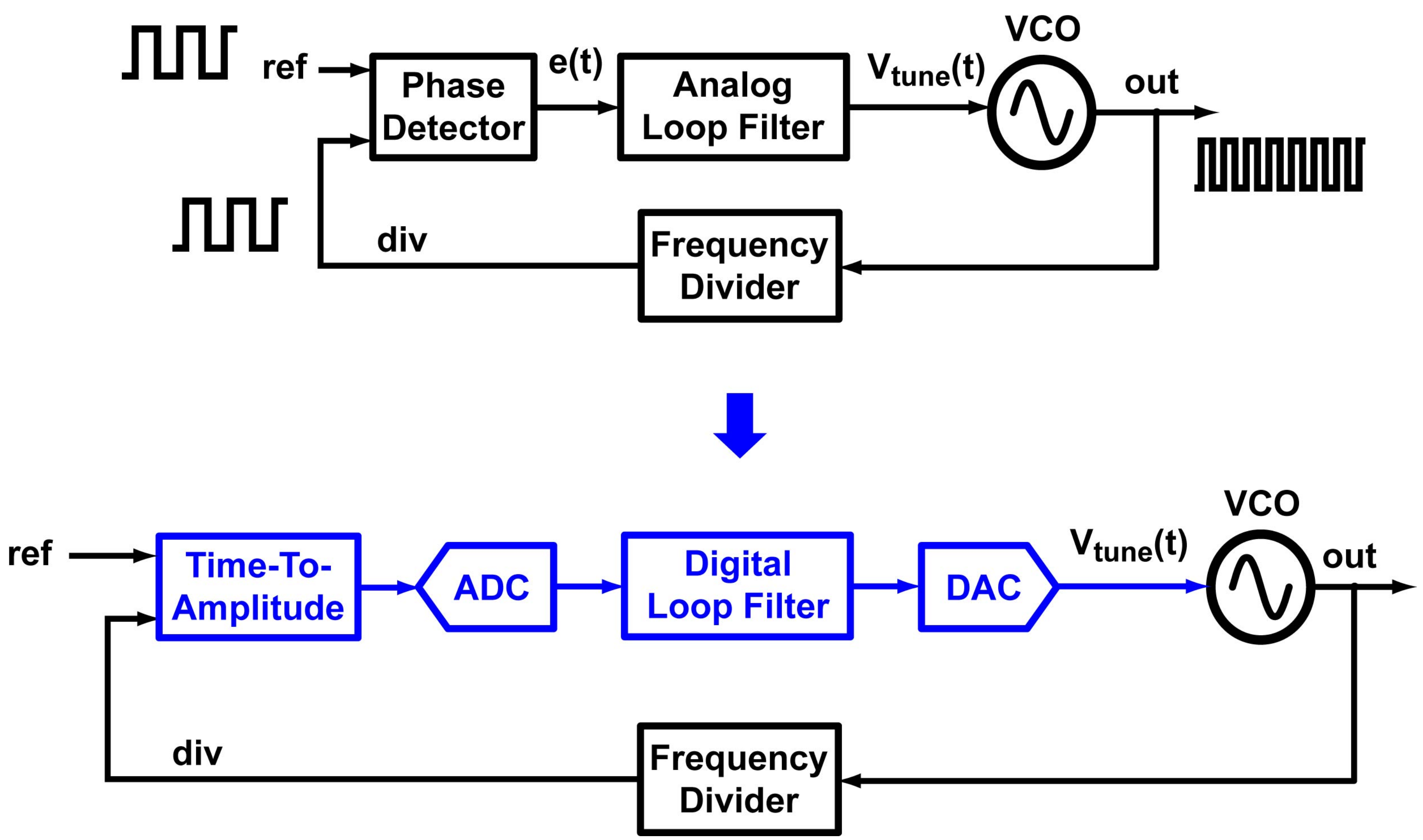
- The analog filter takes up large area and suffers from leakage current
- The charge pump suffers from mismatch, limited output resistance and adds noise
- Therefore, area and power of analog PLLs do not scale down with process
- The application of spur/noise cancellation techniques in analog PLLs is problematic
- Cost of design/verification doesn’t go down

Outline of Talk

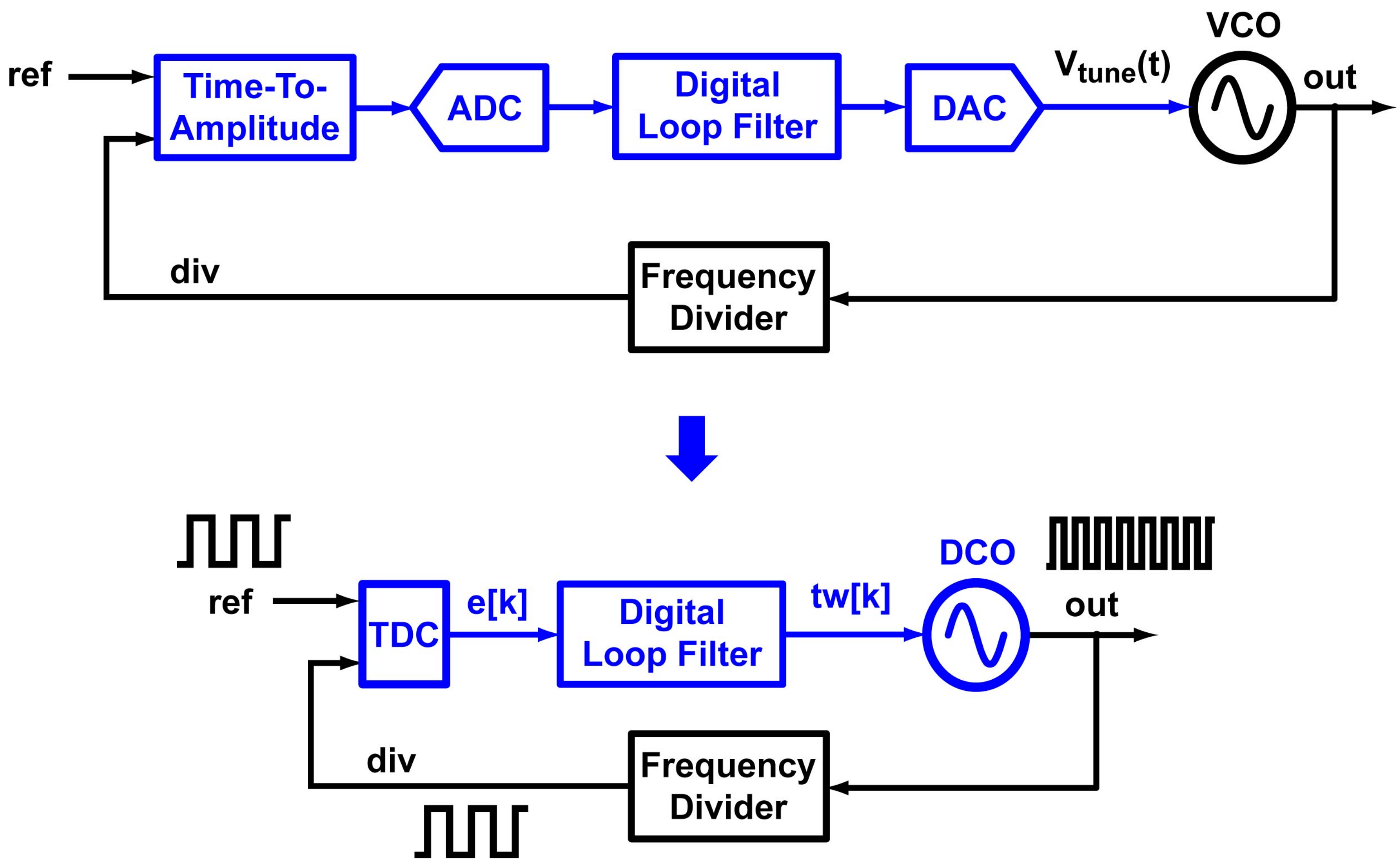
- From analog to digital PLLs
- Analysis and design of digital PLLs
- Multi-bit TDC vs bang-bang PD
- Automatic control of loop BW
- Fractional-N synthesis with digital PLLs
- Examples of practical implementations

From Analog to Digital PLLs

From Analog to Digital PLL

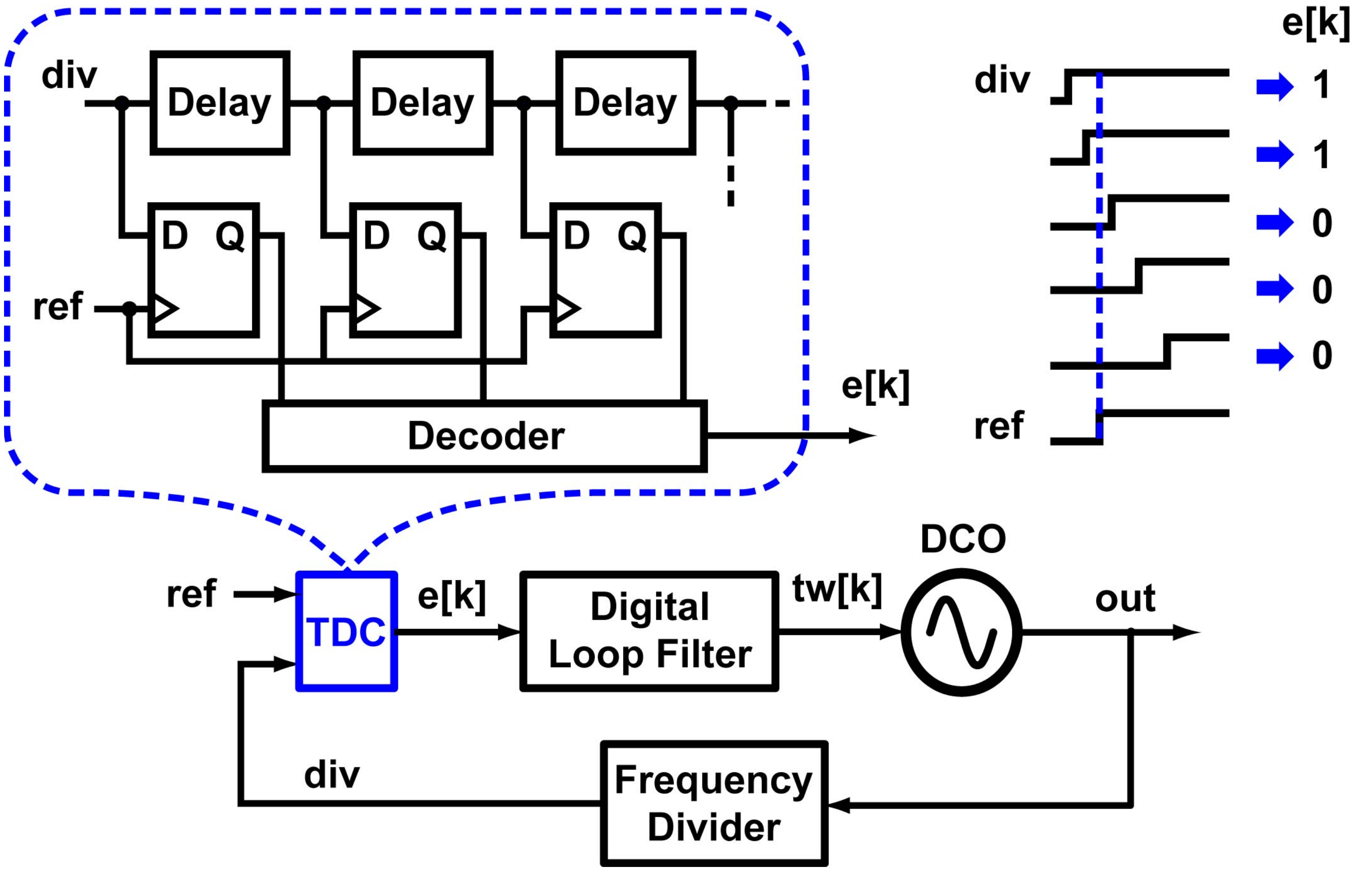


Going "More Digital"

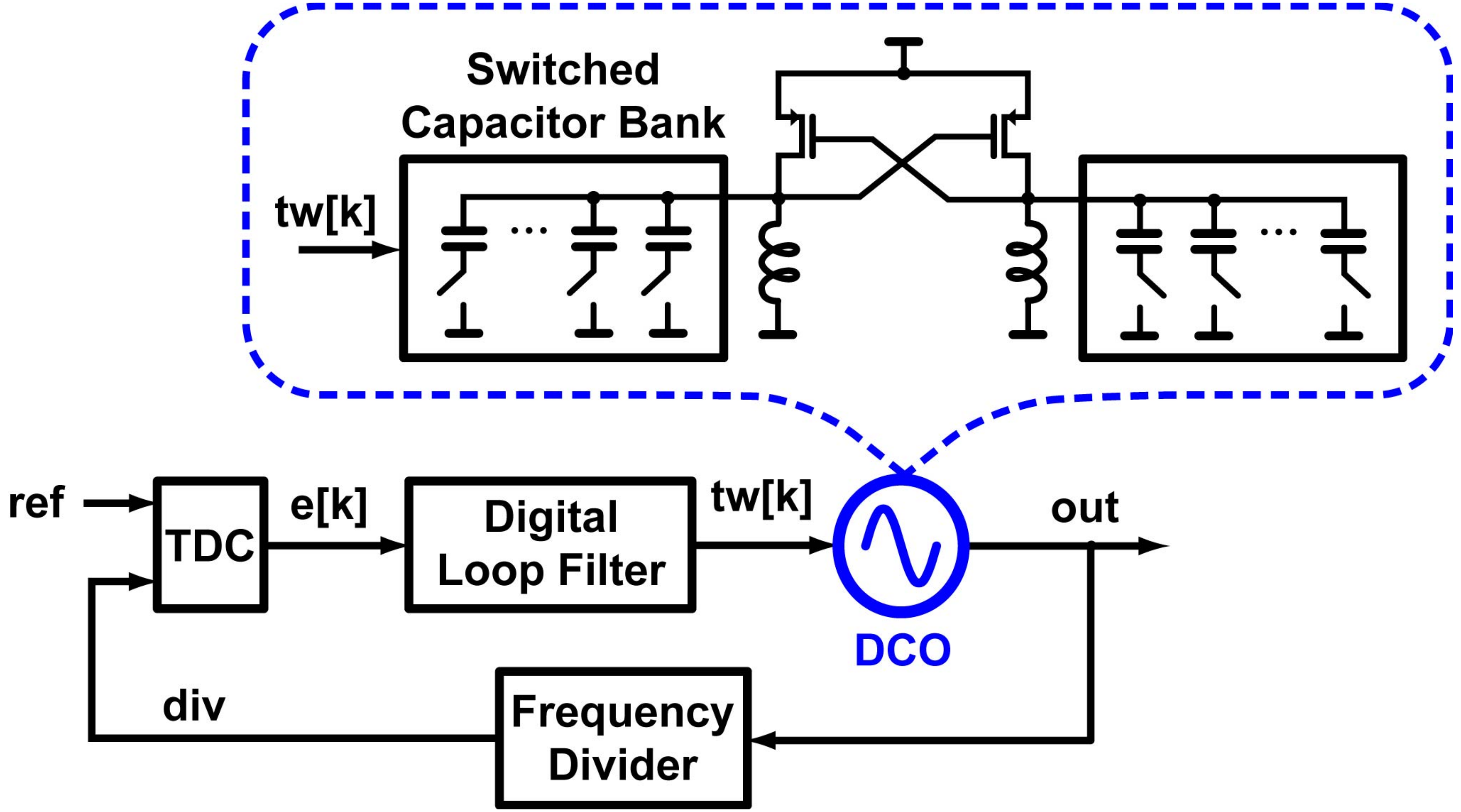


[R.B. Staszewski, *ISSCC*, '04]
[R. Tonietto, *ESSCIRC*, '06]
[C.-M. Hsu, *ISSCC*, '08]

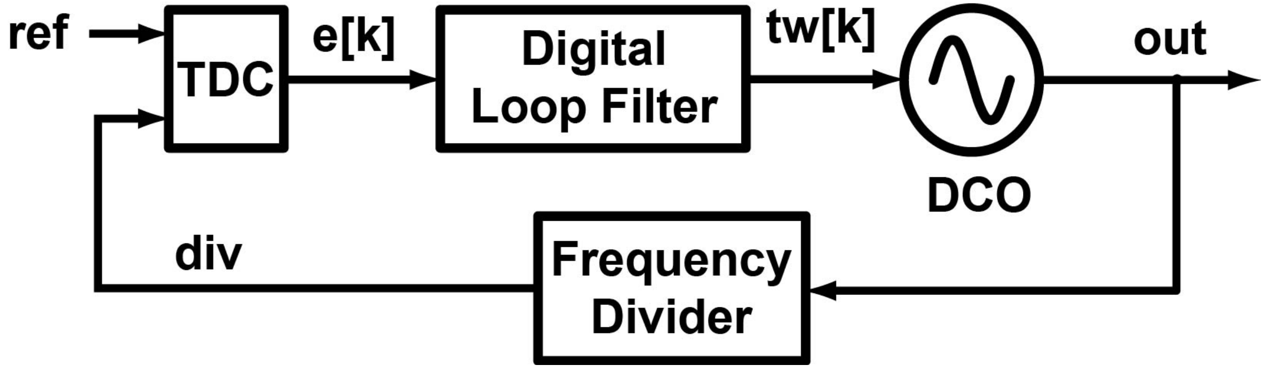
Time-To-Digital Conversion



Digitally-Controlled Oscillator



Opportunities and Challenges of DPLL

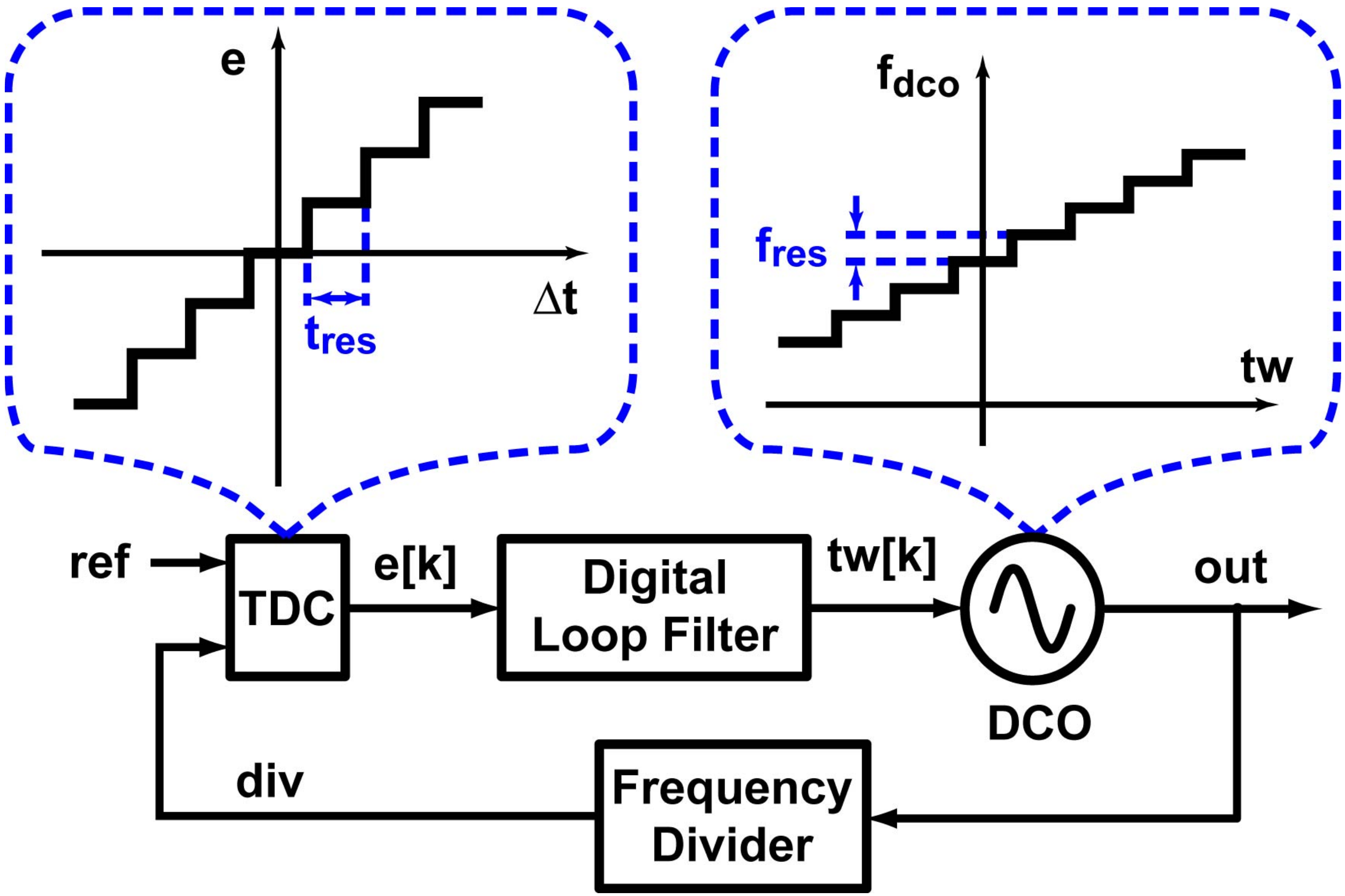


- **Loop filter** scales down
- **No charge pump** (noise, power, area)
- Friendly to **calibration algorithms**
- Issue: **quantization noise**

Analysis and Design of Digital PLLs

TDC and DCO Quantization

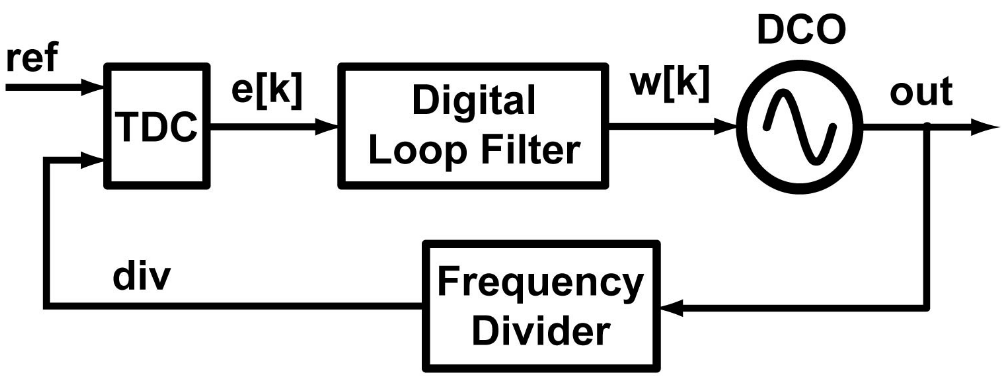
Mid-tread Quantizer



Deriving a Model at Reference Rate

- $t_v[k]$ is timestamp of divider positive edges
- $\Delta t[k]$ is time error at TDC input

Digital PLL Model



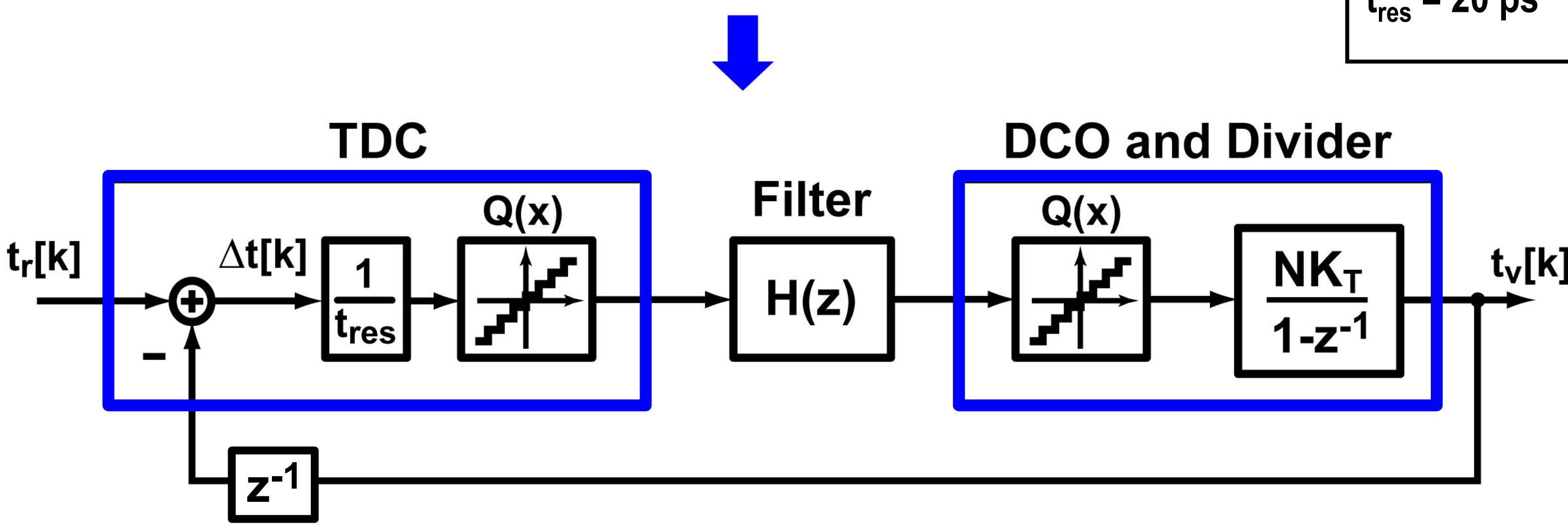
Example

f_{v0} = 3.6 GHz

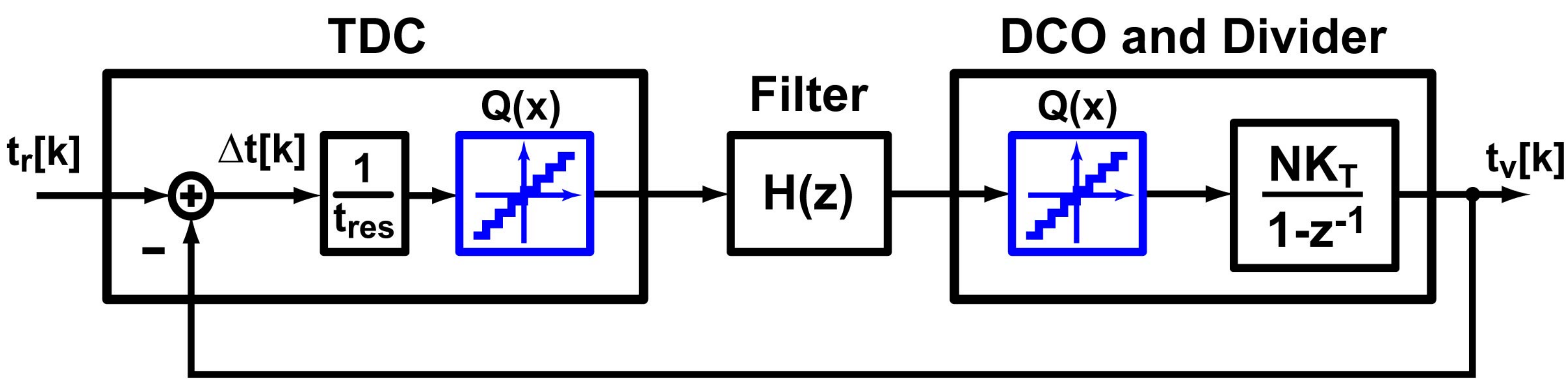
f_{res} = 12 kHz

K_T = 0.9 fs/unit cap

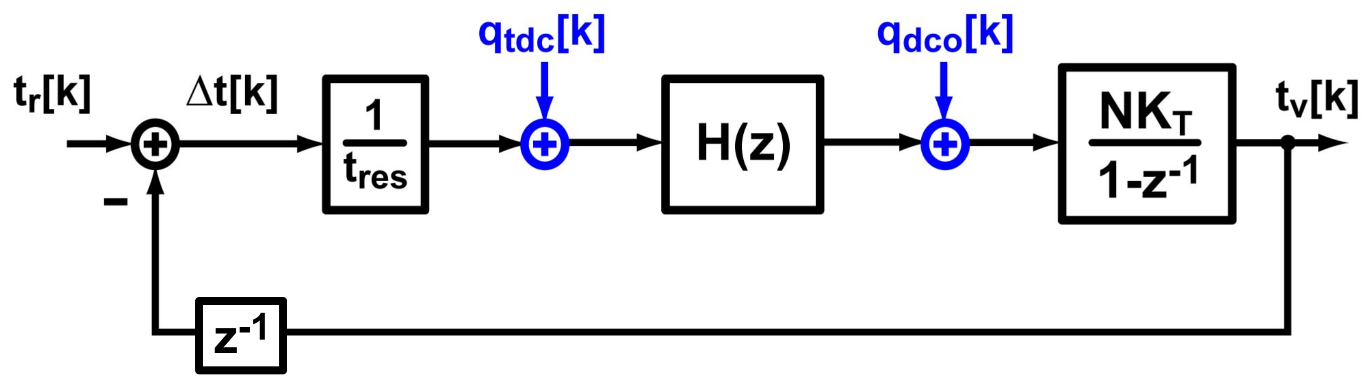
t_{res} = 20 ps



First Approximation

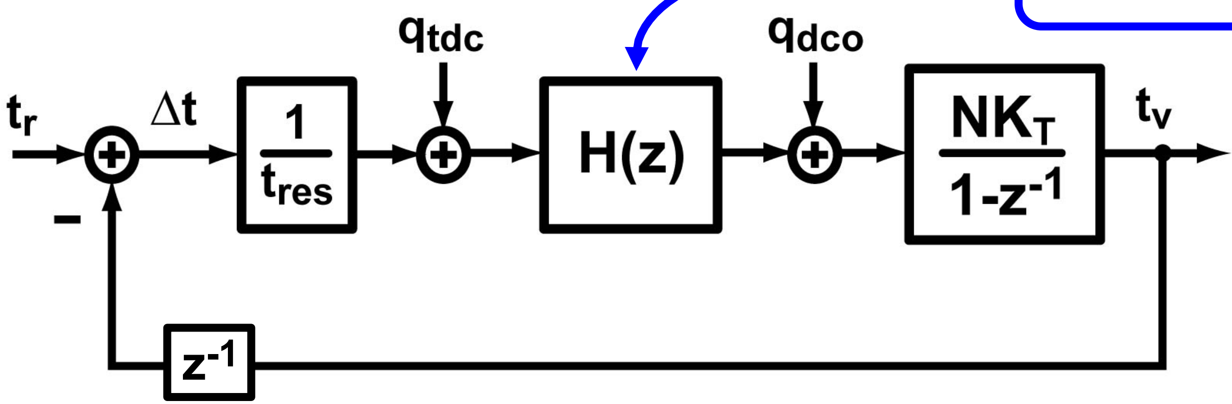


Linear Model:



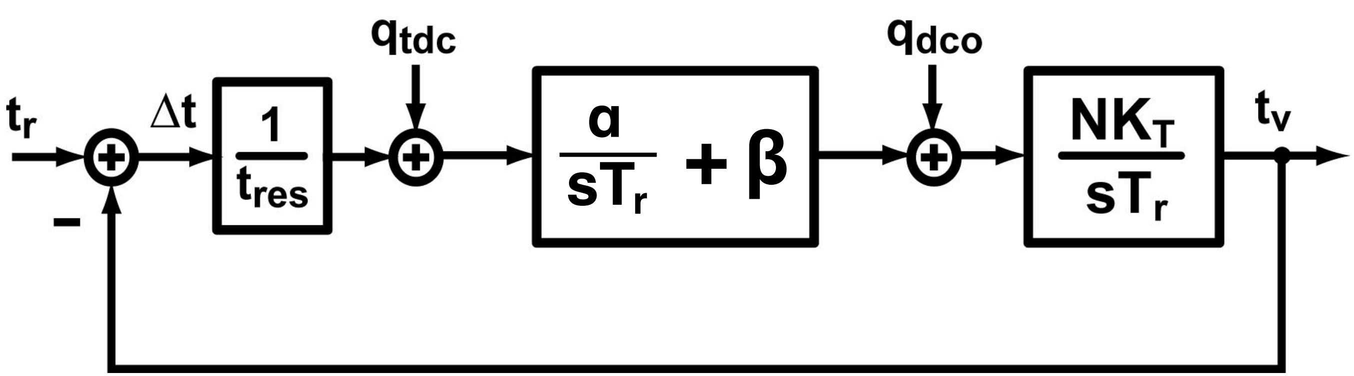
Second Approximation

$$H(z) = \frac{\alpha}{1-z^{-1}} + \beta$$

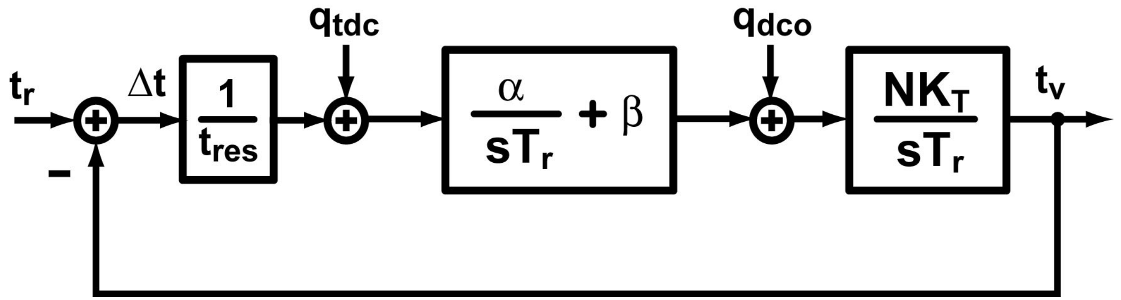


Narrowband approximation

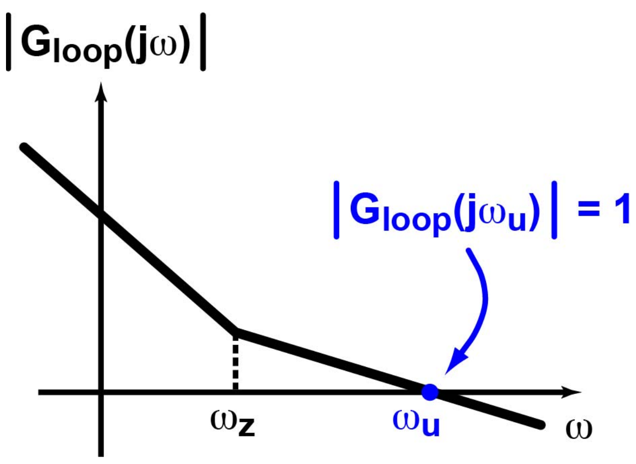
$$z^{-1} = e^{-sT_r} \cong 1 - sT_r$$



Loop Bandwidth

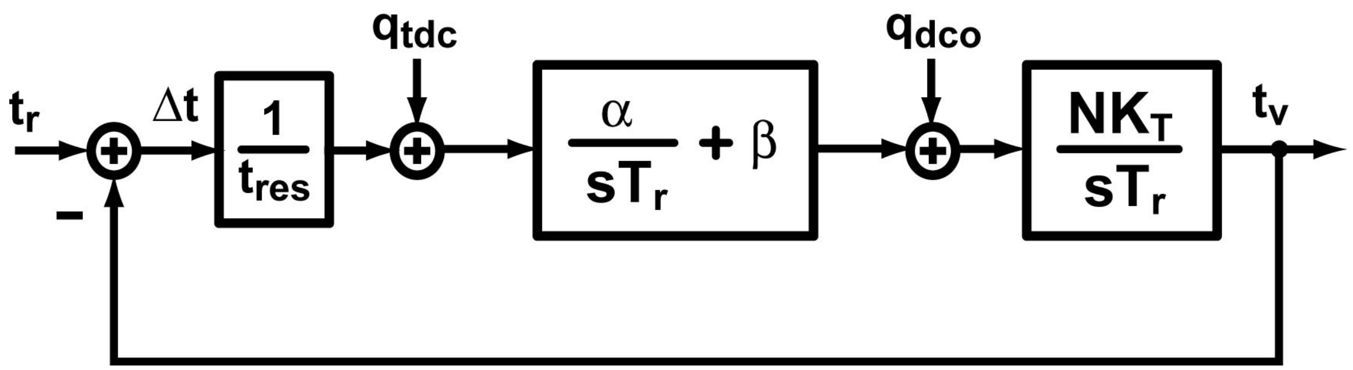


$$G_{loop}(s) = \left(1 + \frac{\alpha}{\beta}\frac{1}{sT_r}\right) \cdot \frac{N\beta K_T}{sT_r t_{res}}$$



$$\omega_u \cong \frac{N\beta K_T}{T_r t_{res}}, \qquad \omega_z = \frac{\alpha}{\beta} \cdot \frac{1}{T_r}$$

TDC Resolution vs. Bandwidth Trade-Off



$$\omega_u \cong \frac{N\beta K_T}{T_r t_{res}}$$

f_{v0} = 3.6 GHz

f_r = 50 MHz

K_T = 0.9 fs/unit cap

β = 4

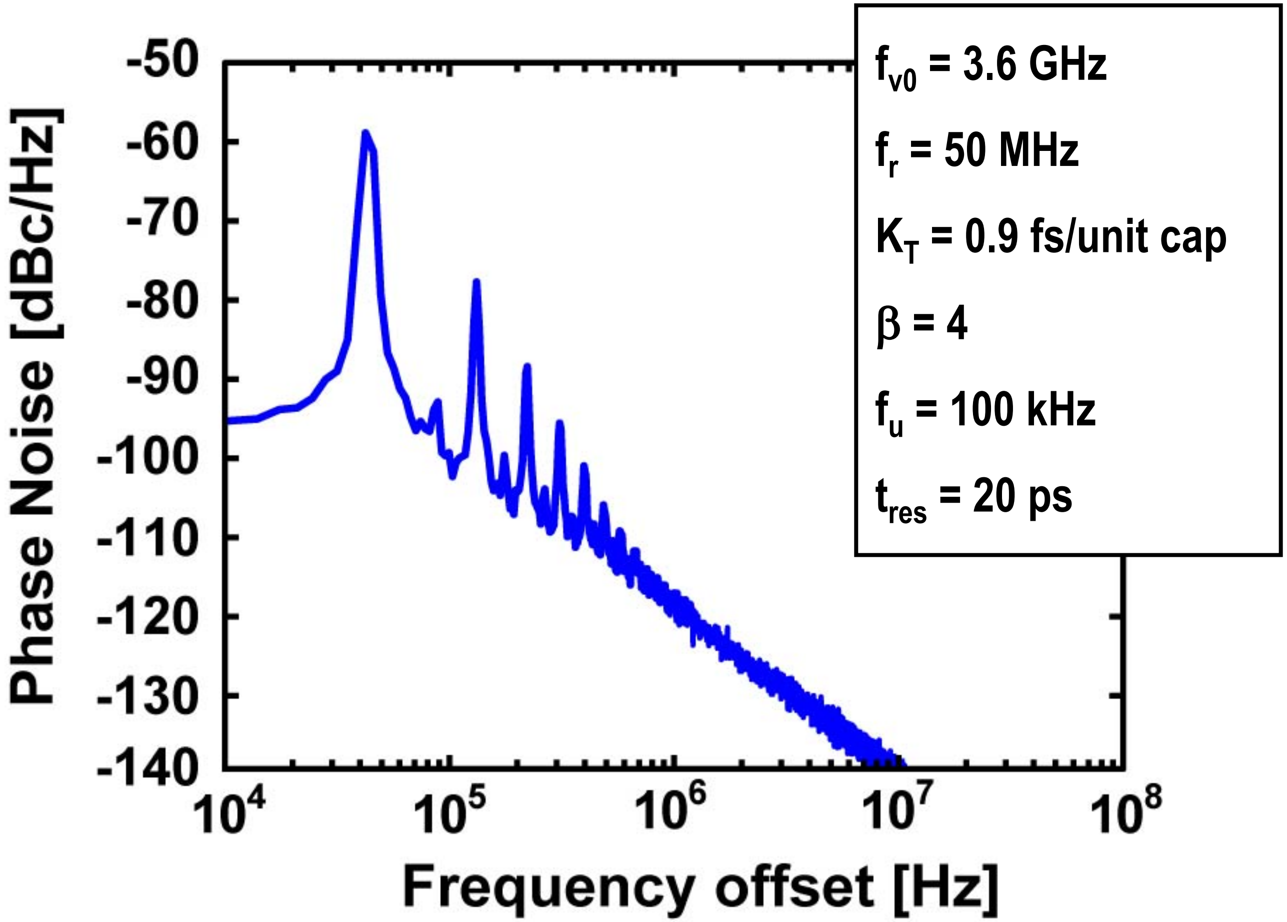
f_u = 100 kHz

t_{res} = 20 ps

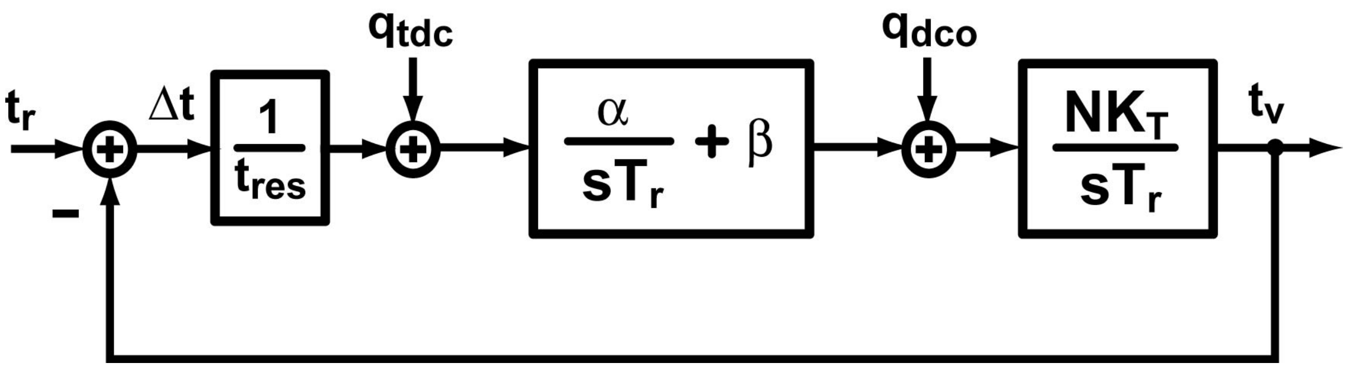
- **Wider BW demands smaller t_{res}**

Output Spectrum with no added noise

- **Large tones indicates that q_{tdc} is periodic**



Quantization Noise of Standard DPLL



- If $q_{tdc}[k]$ has uniform distribution and $q_{dco}[k]$ is negligible, then quantization noise is

$$\sigma_{\Delta t} = \frac{t_{res}}{\sqrt{12}}$$

$t_{res} = 20$ ps

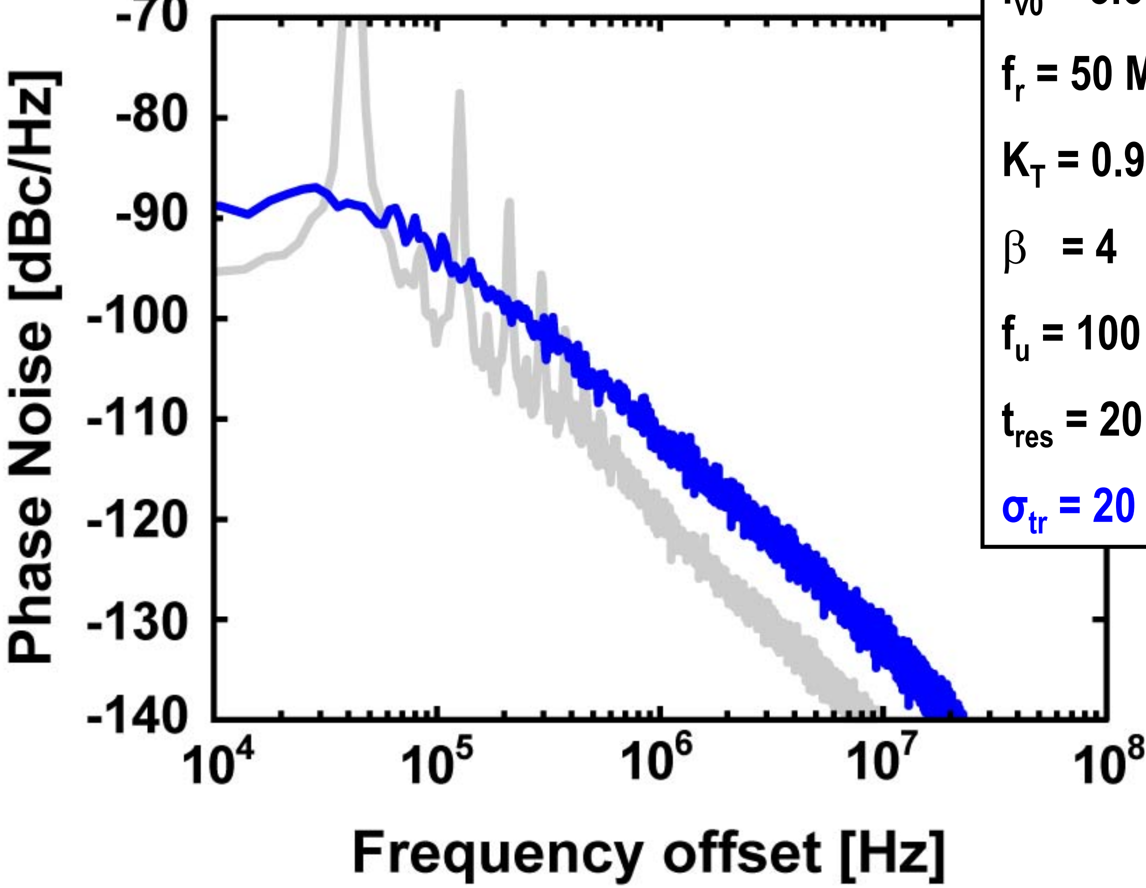
$f_{v0} = 3.6$ GHz

$\sigma_{\Delta t} = 5.8$ ps

$\Phi_{rms} = -18$dBc

Output Spectrum with added noise

- **White reference noise added**



f_{v0} = 3.6 GHz

f_r = 50 MHz

K_T = 0.9 fs/unit cap

β = 4

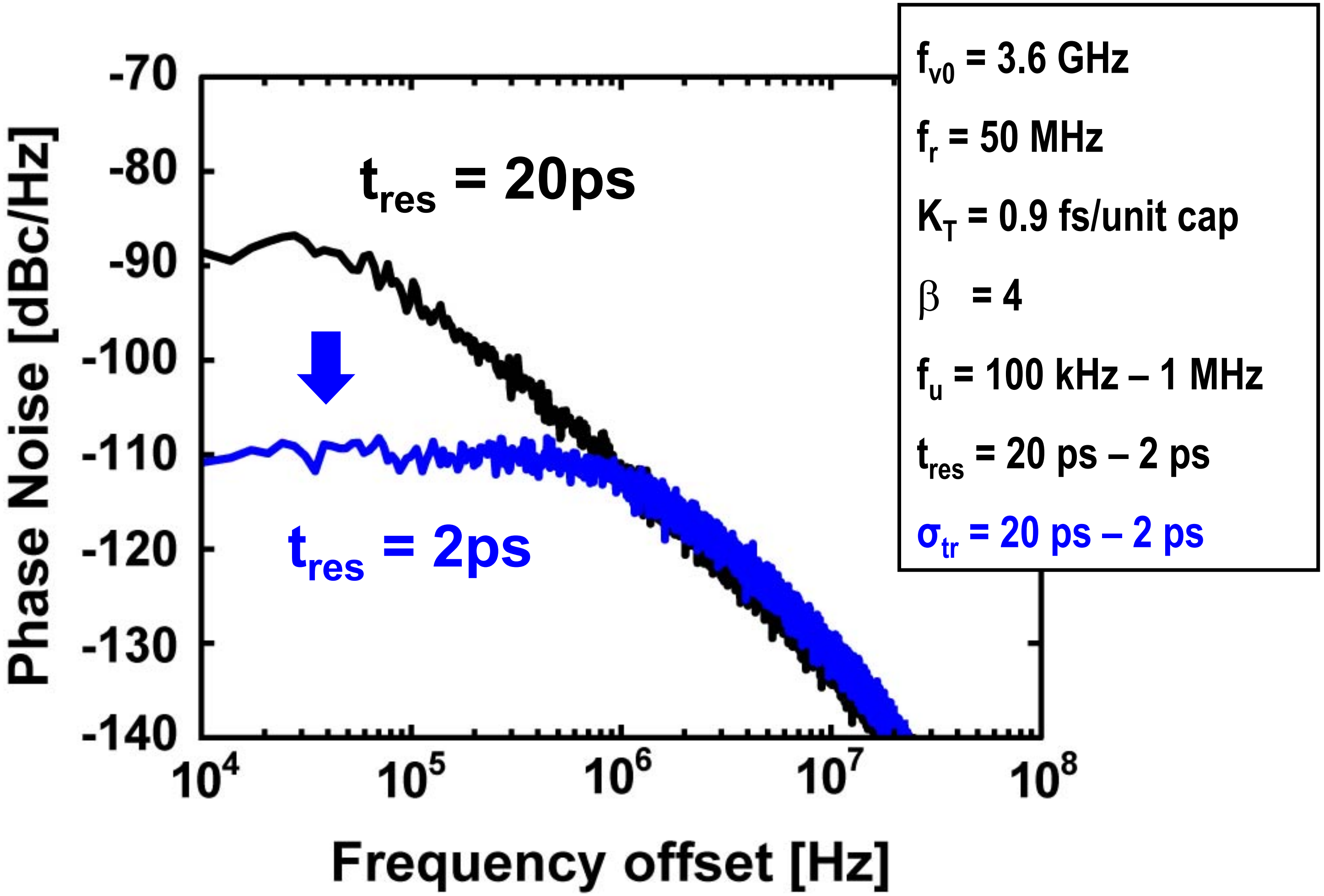
f_u = 100 kHz

t_{res} = 20 ps

σ_{tr} = 20 ps

Output Spectrum of Digital PLL

- **TDC resolution vs. bandwidth trade-off**



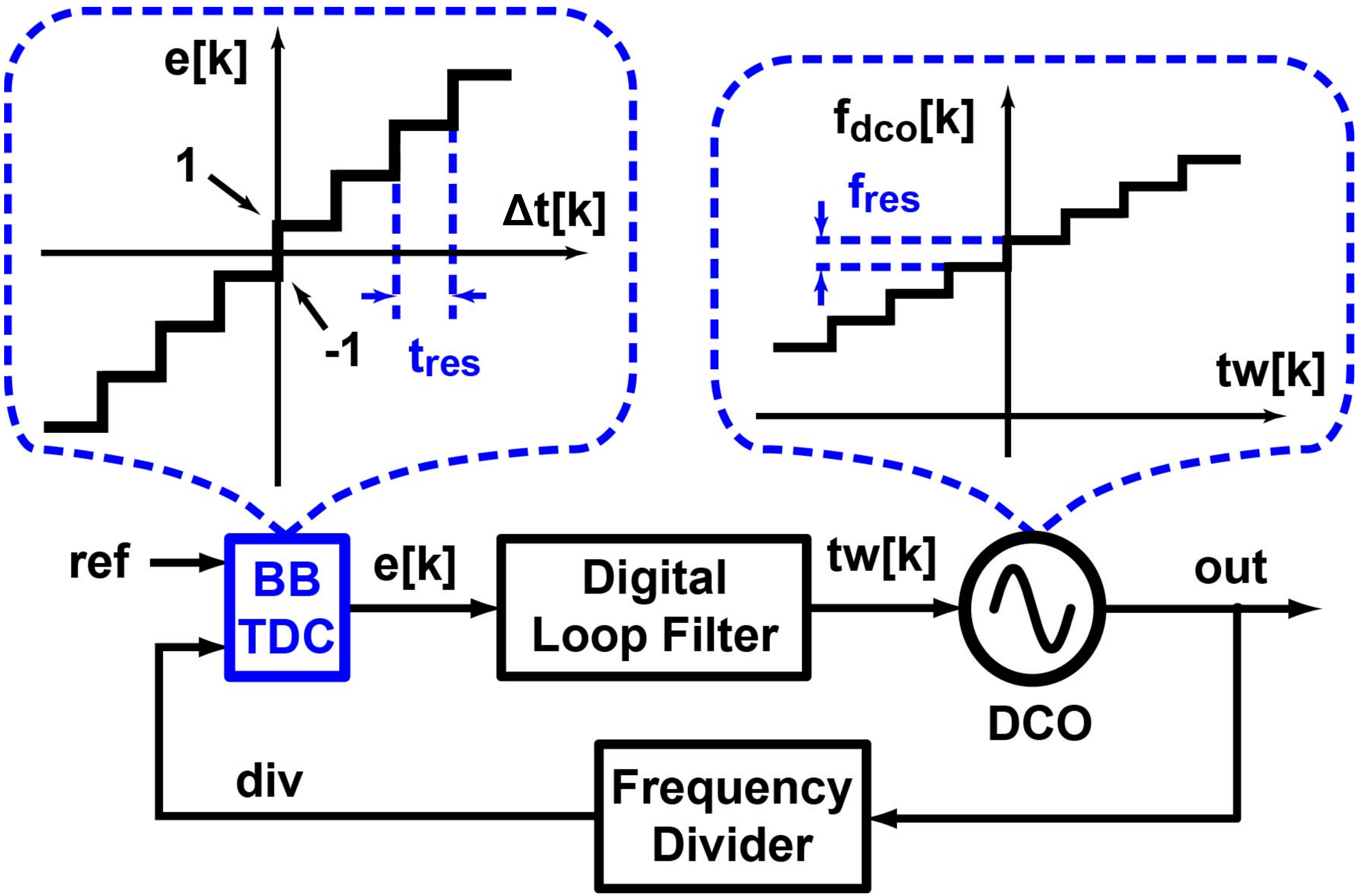
Summary

- In standard DPLLs, PLL bandwidth is inversely proportional to TDC resolution
- Quantization noise is mainly limited by TDC resolution and it has to be lower than random noise
- In wireless applications, ps or sub-ps TDC resolution may be required
- This has driven significant effort in the design of very high-resolution TDCs

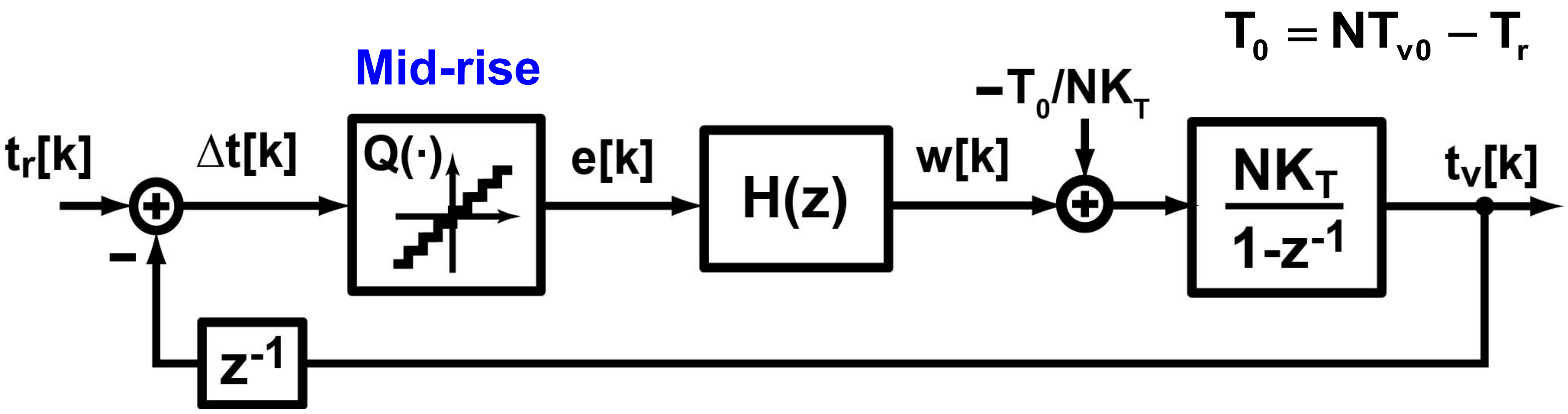
Multi-bit TDC vs. Bang-Bang Phase Detector

Mid-rise Coarse TDC or “Bang-Bang” PD

Mid-rise Quantizer



Model of Bang-Bang DPLL

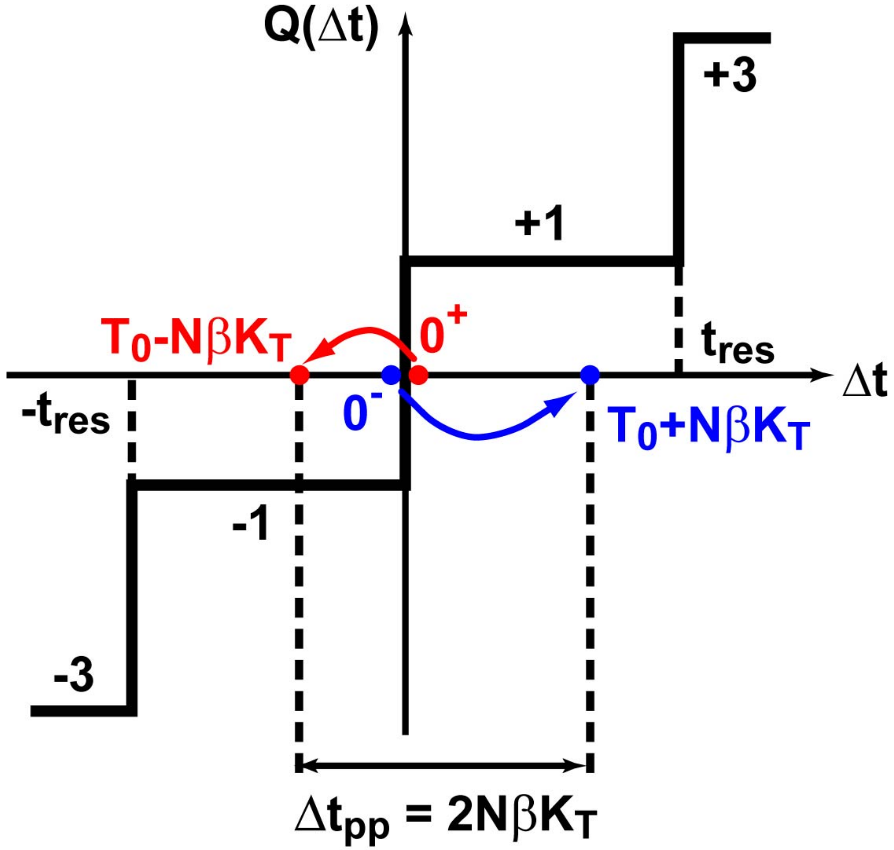


- **For H(z) = β:**

$$\Delta t[k+1] - \Delta t[k] = T_0 - N\beta K_T \cdot Q\left(\Delta t[k]/t_{res}\right)$$

Quantization Noise of Bang-Bang DPLL

$$\Delta t[k+1] - \Delta t[k] = T_0 - N\beta K_T \cdot Q\left(\Delta t[k]/t_{res}\right)$$

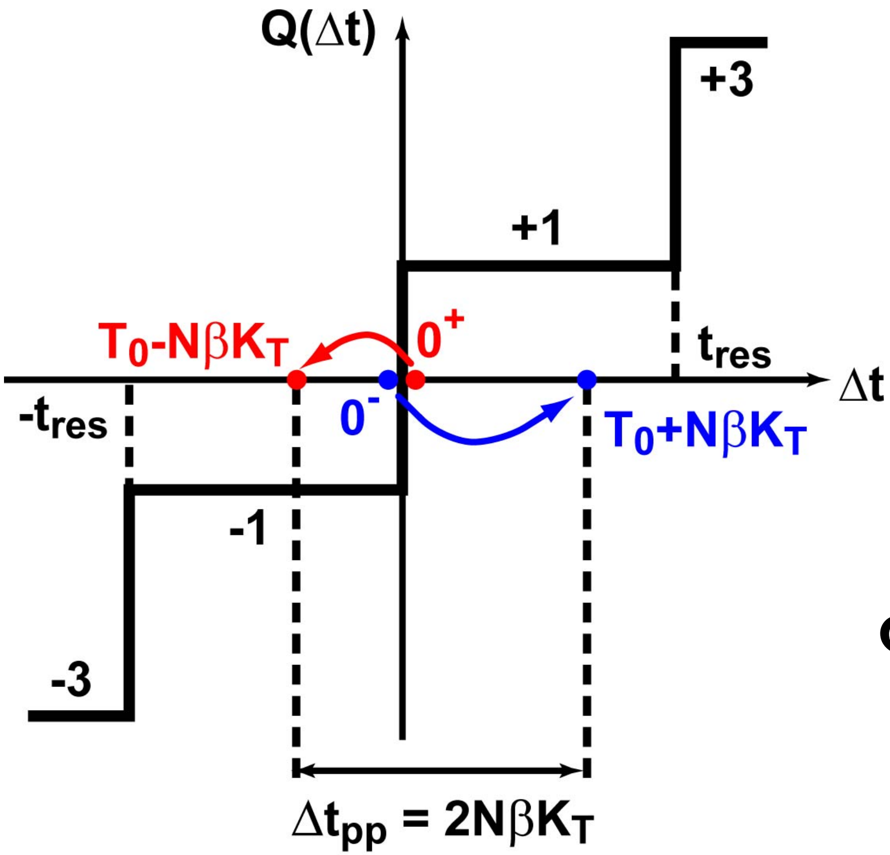


Assuming coarse TDC

$$t_{res} > T_0 + N\beta K_T$$

Quantization Noise of Bang-Bang DPLL

$$\Delta t[k+1] - \Delta t[k] = T_0 - N\beta K_T \cdot Q\left(\Delta t[k]/t_{res}\right)$$



Irrational ($T_0/N\beta K_T$)

⬇

p(Δt) is uniform

⬇

$$\sigma_{\Delta t,lc} = \frac{\Delta t_{pp}}{\sqrt{12}} = \frac{N\beta K_T}{\sqrt{3}}$$

Tradeoffs in Quantization Noise in BB-DPLLs

- For $H(z) = \left(\frac{\alpha}{1-z^{-1}} + \beta\right) \cdot z^{-D}$:

[N. Da Dalt, *TCAS-I*, '05]

$$\sigma_{\Delta t,lc} = (1+D) \cdot \frac{N\beta K_T}{\sqrt{3}}$$

- Loop quantization no longer limited by t_{res} (TDC resolution), but only by βK_T (DCO granularity)
- Quantization increases as filter latency D (number of clock cycles)

Quantization Noise: Mid-Tread vs Mid-Rise

Mid-Tread

$$\sigma_{\Delta t} = \frac{t_{res}}{\sqrt{12}}$$

t_{res} = 20 ps

f_{v0} = 3.6 GHz

$\sigma_{\Delta t}$ = 5.8 ps

Φ_{rms} = -18dBc

Mid-Rise or “Bang-Bang”

$$\sigma_{\Delta t,lc} = (1+D) \cdot \frac{N\beta K_T}{\sqrt{3}}$$

K_T = 0.92 fs/b

f_{v0} = 3.6 GHz

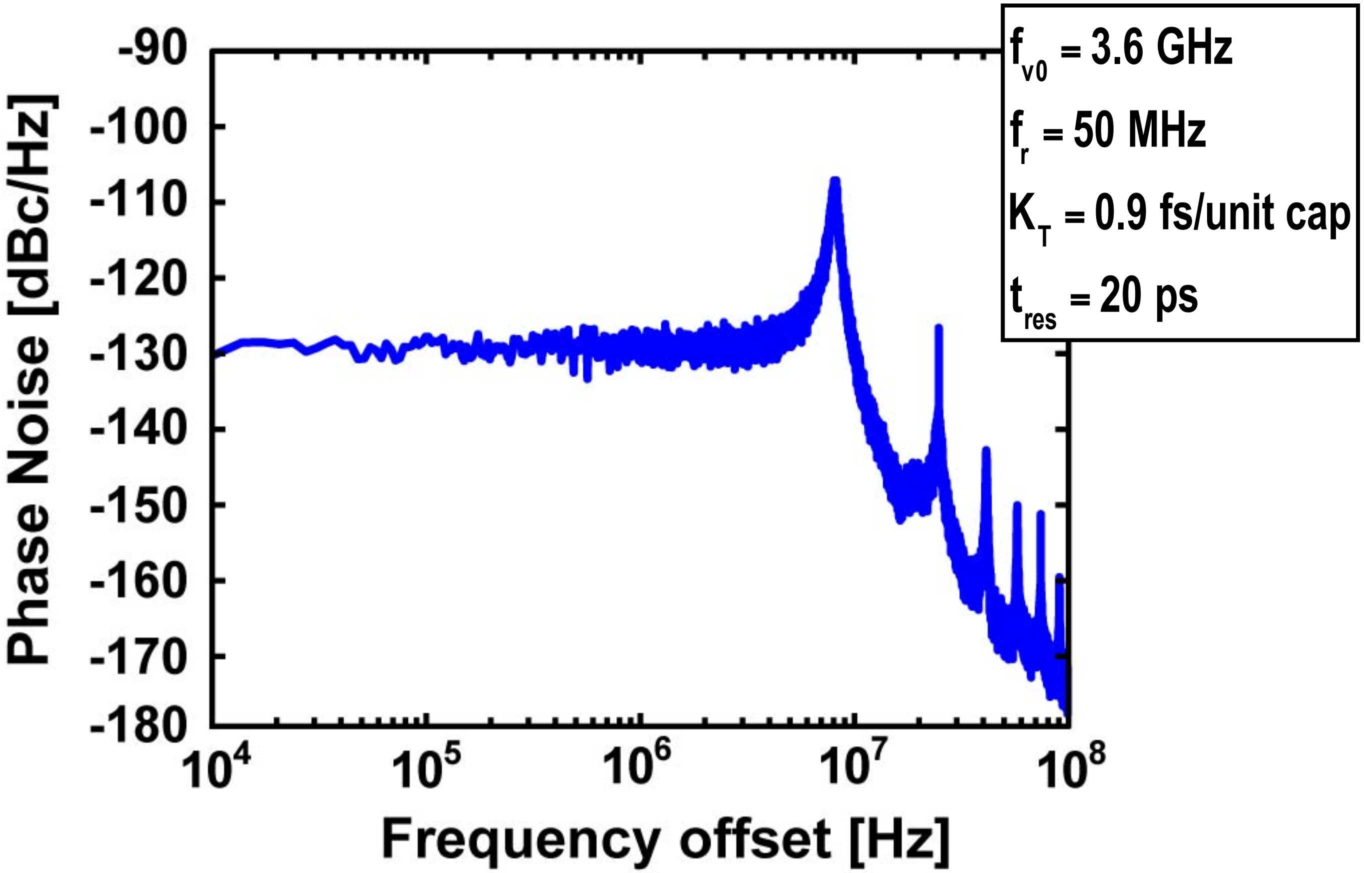
N = 72, D = 1

$\sigma_{\Delta t}$ = 0.344 ps

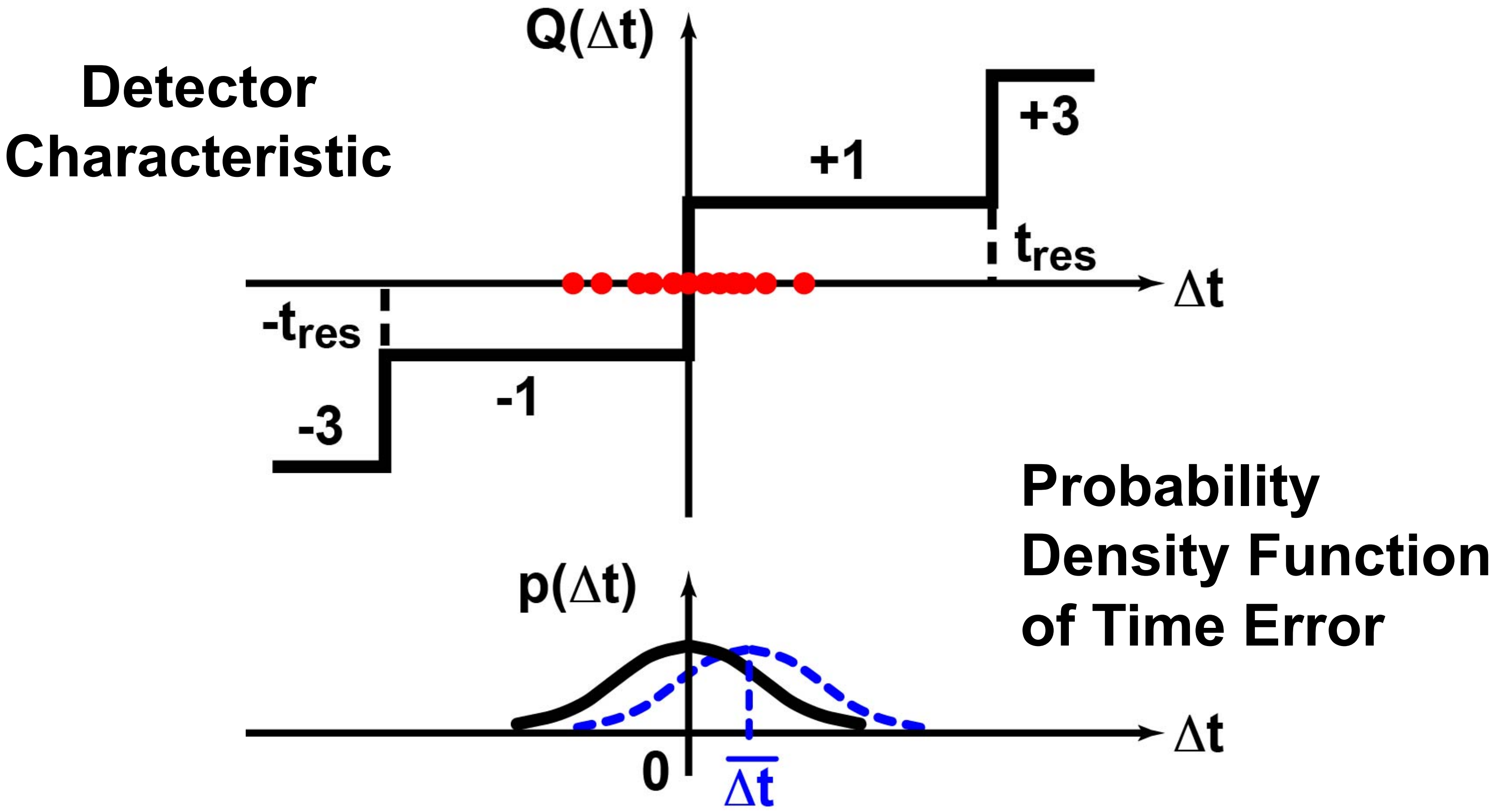
Φ_{rms} = -42dBc

Output Spectrum of Bang-Bang DPLL

- **Periodic quantization error (a.k.a. limit cycle)**

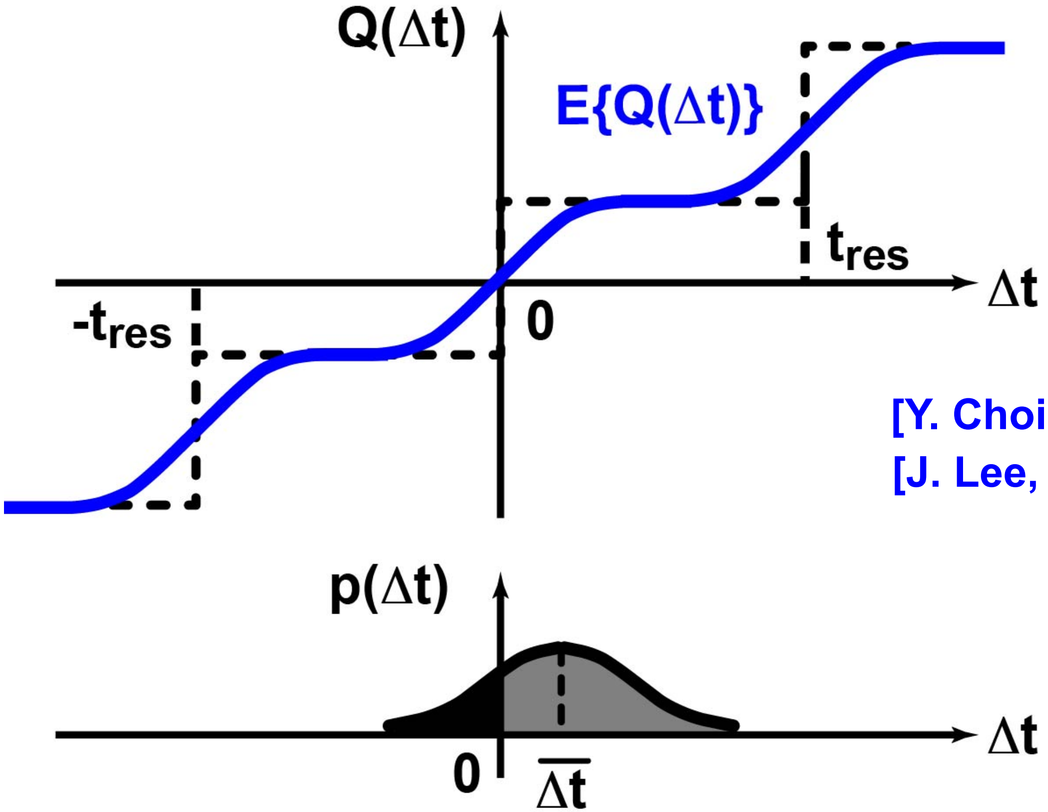


Phase Detector under Random Noise Regime



Averaged detector output follows the averaged time error (within a certain range)

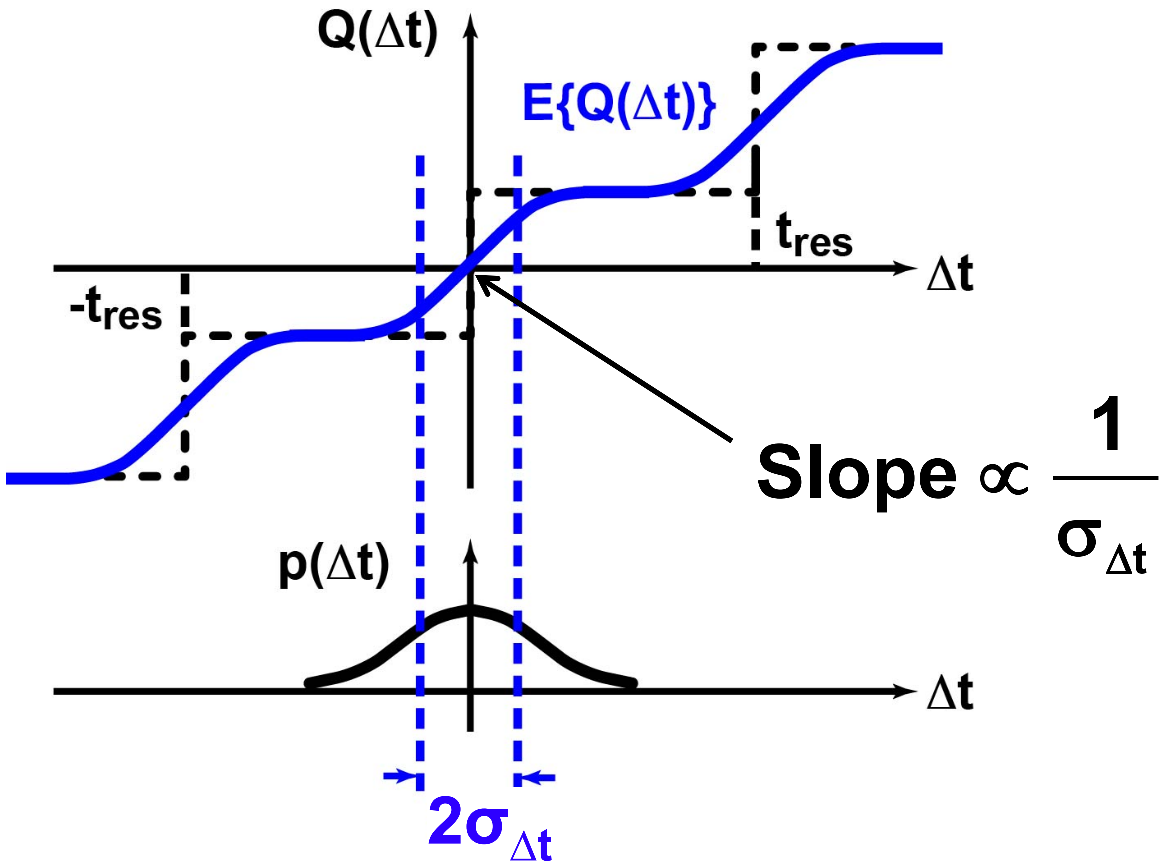
Detector Characteristic gets Smoothened



[Y. Choi, *TCAS-II*, Nov. '03]
[J. Lee, *JSSC*, Sep. '04]

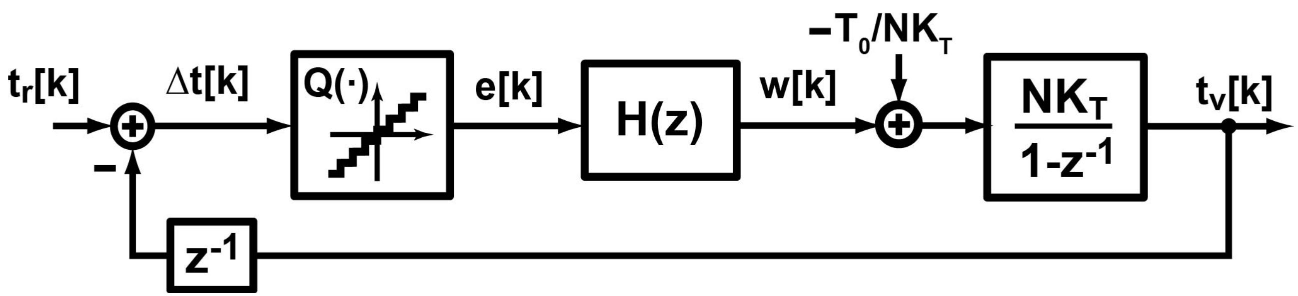
$$F\left(\overline{\Delta t}\right) = E\{Q(\Delta t)\} = \int_{-\overline{\Delta t}}^{+\infty} p\left(\Delta t\right) d\Delta t - \int_{-\infty}^{-\overline{\Delta t}} p\left(\Delta t\right) d\Delta t$$

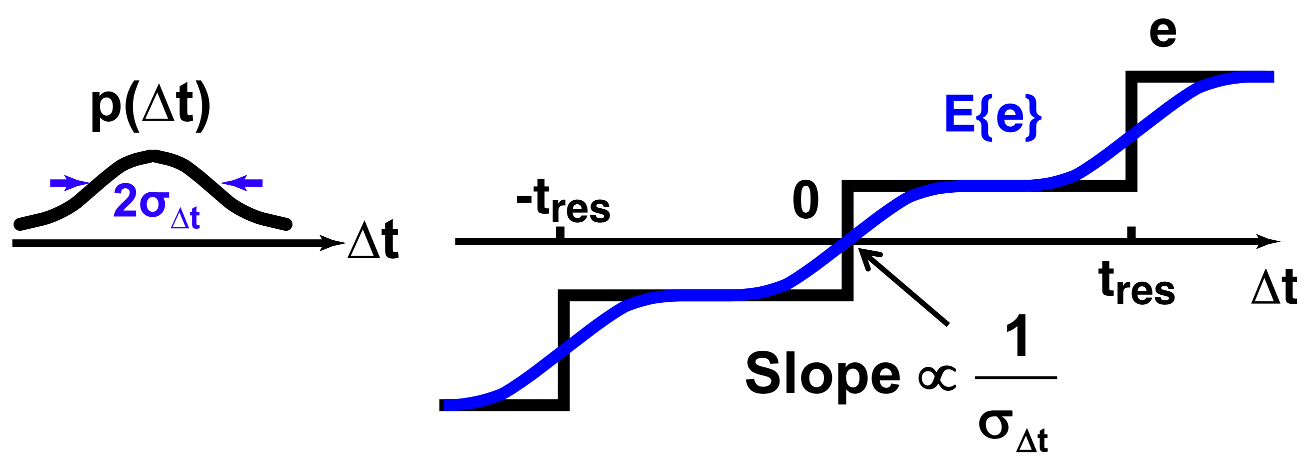
Gain of Phase Detector



The gain of the detector is inversely proportional to the detector input jitter (within a certain range)

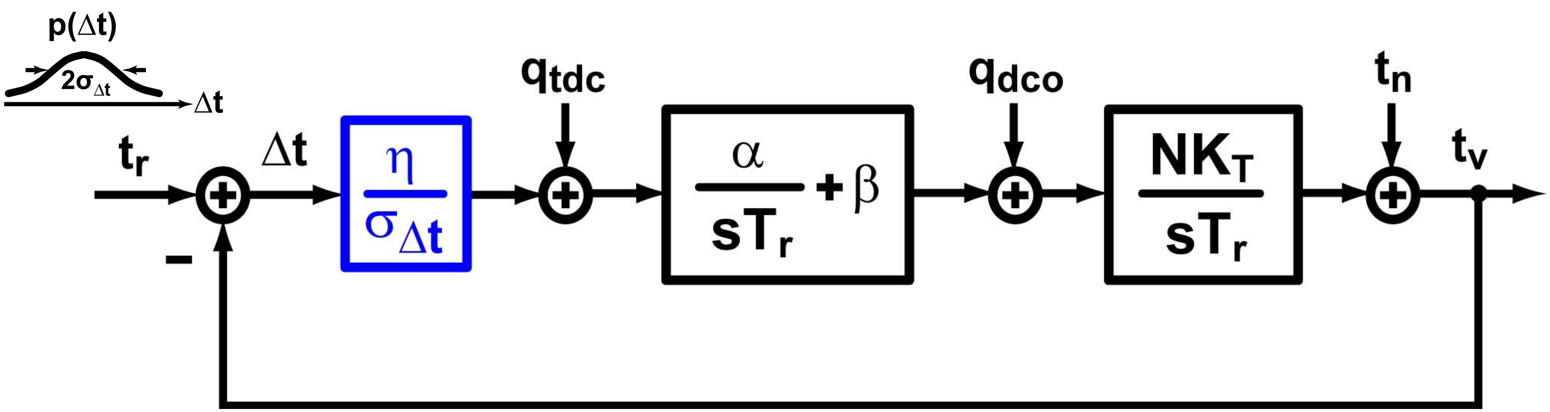
Bang-Bang DPLL in "Random-Noise Regime"



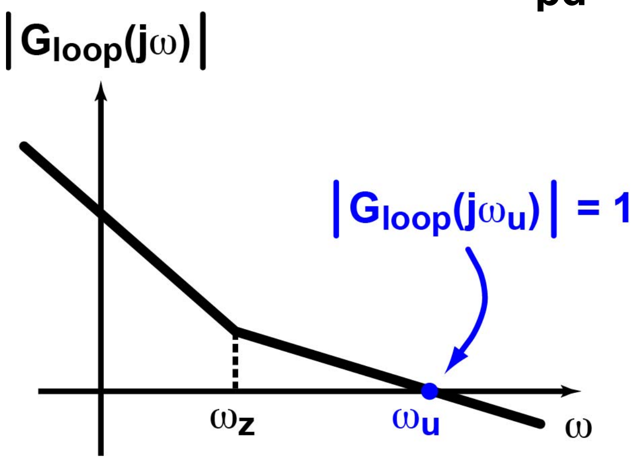


- **If Δt has Gaussian distribution (i.e. noise dominates over quantization), the average of e[k] is locally proportional to Δt**

Equivalent Linear Model

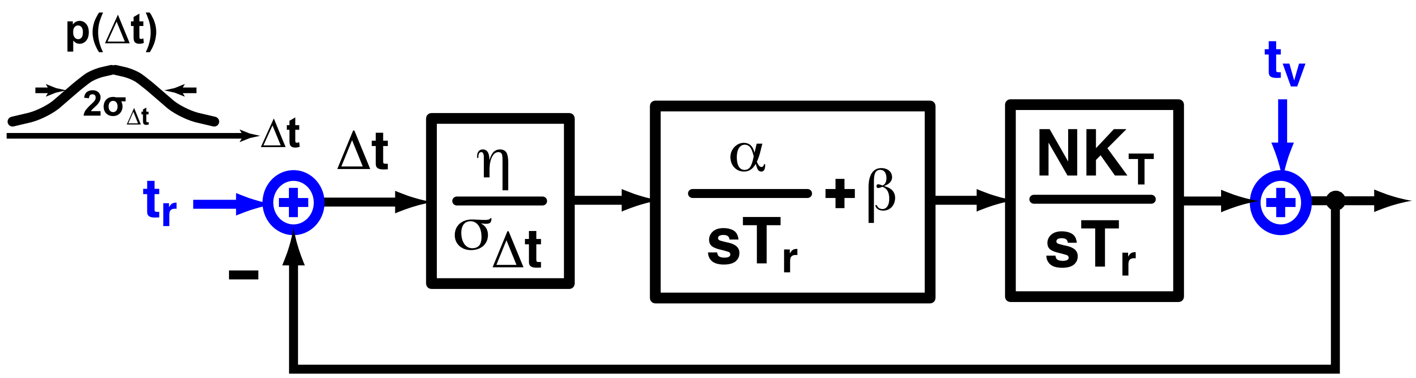


$$K_{pd} = \frac{\eta}{\sigma_{\Delta t}}, \quad \text{where} \quad \eta = \sqrt{\frac{2}{\pi}}$$



$$\omega_u \cong \frac{\eta N \beta K_T}{T_r \sigma_{\Delta t}}, \qquad \omega_z = \frac{\alpha}{\beta} \cdot \frac{1}{T_r}$$

Loop Bandwidth of Bang-Bang DPLL



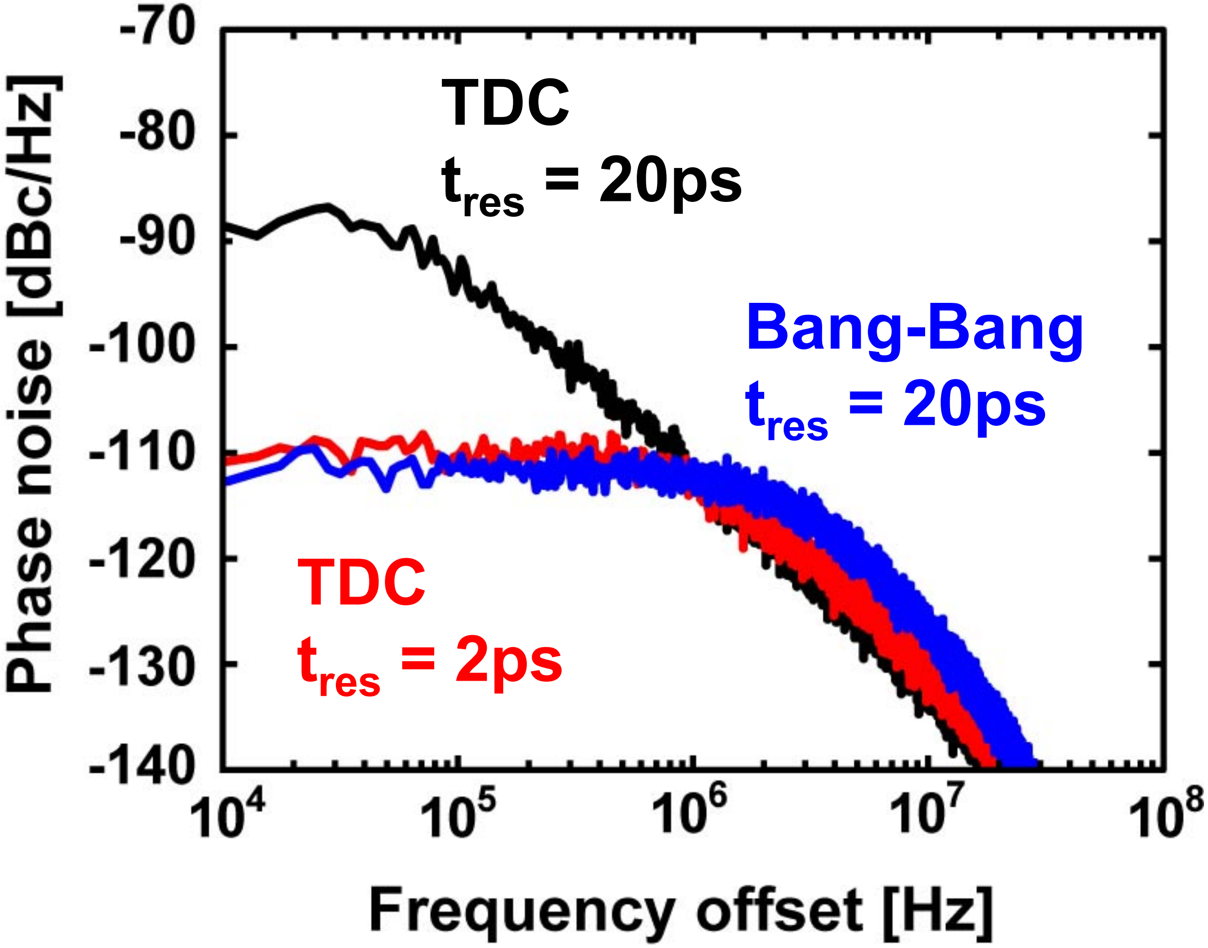
$$\omega_u \cong \eta \frac{N\beta K_T}{T_r \sigma_{\Delta t}}$$

f_r = 50 MHz
$N\beta K_T$ = 260 ps/unit
f_u = 1 MHz
$\sigma_{\Delta t}$ = 1.65 ps

- **Valid in random-noise regime**
- **Wide BW can be achieved with a coarse TDC**

[M. Zanuso, *TCAS-II*, '09]

Standard DPLL vs. Bang-Bang PLL

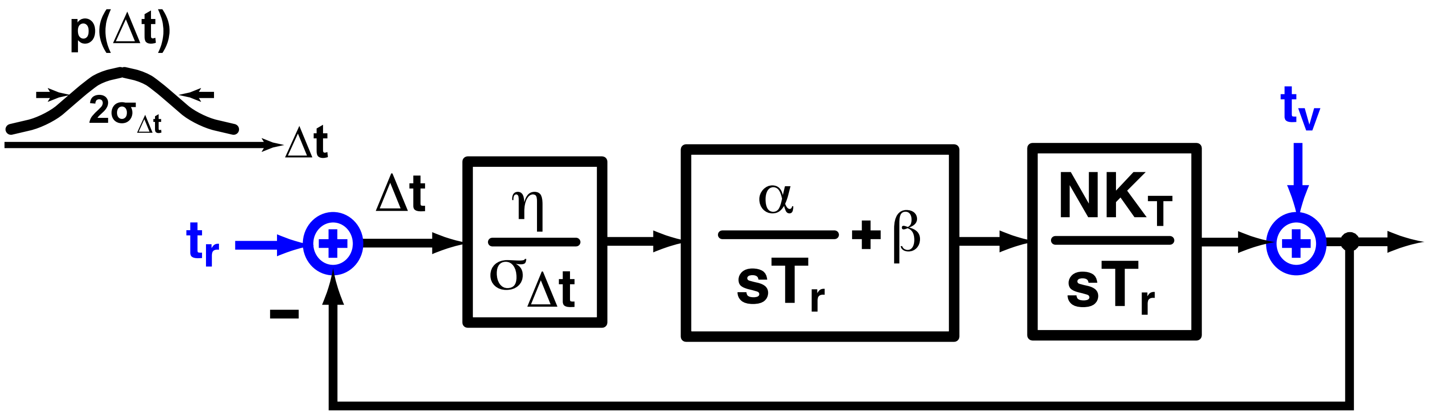


Summary

- In bang-bang DPLLs, quantization error and loop BW are NOT limited by TDC resolution
- At wide loop bandwidths, bang-bang DPLLs allows same noise performance as those employing high-resolution TDCs
- Given their lower power consumption, bang-bang DPLLs offer better noise/power trade-off than standard DPLLs

Automatic Control of Loop BW

Loop BW sensitive to Noise

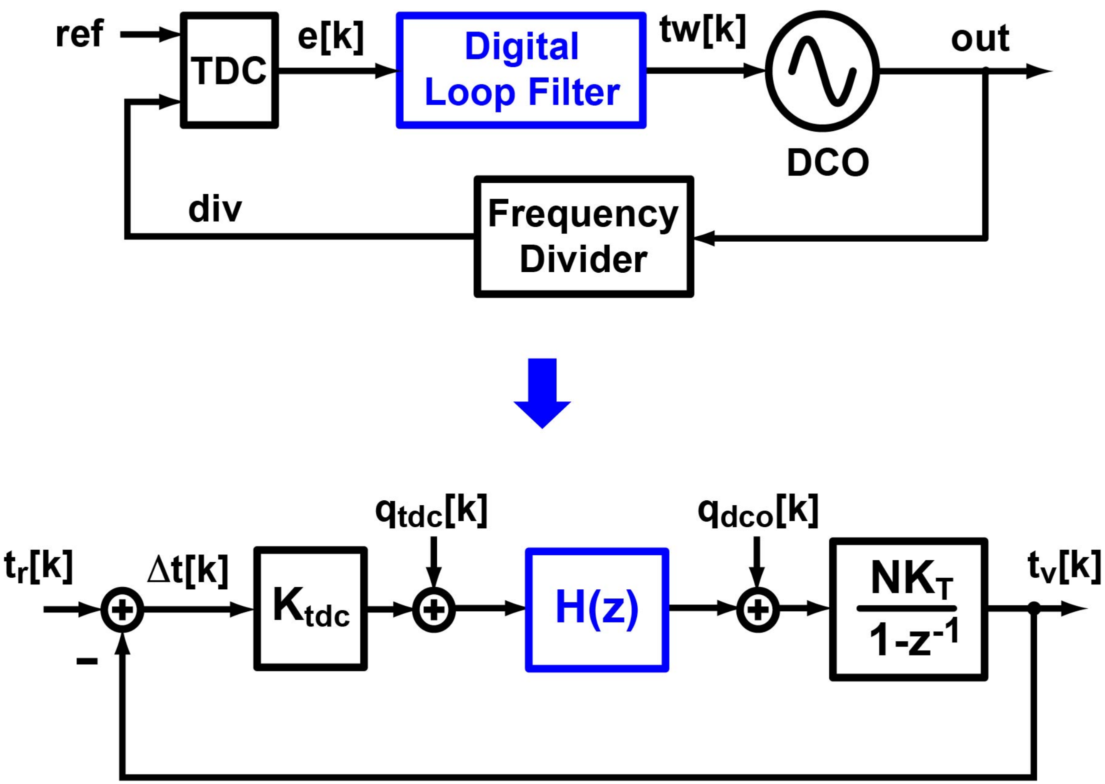


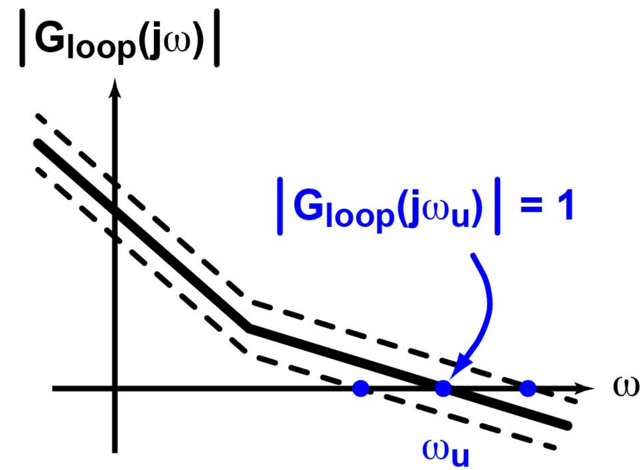
(From previous slide)

$$\omega_u \cong \frac{\eta N \beta K_T}{T_r \sigma_{\Delta t}}$$

- **The loop BW of BBPLLs is inversely proportional to jitter**

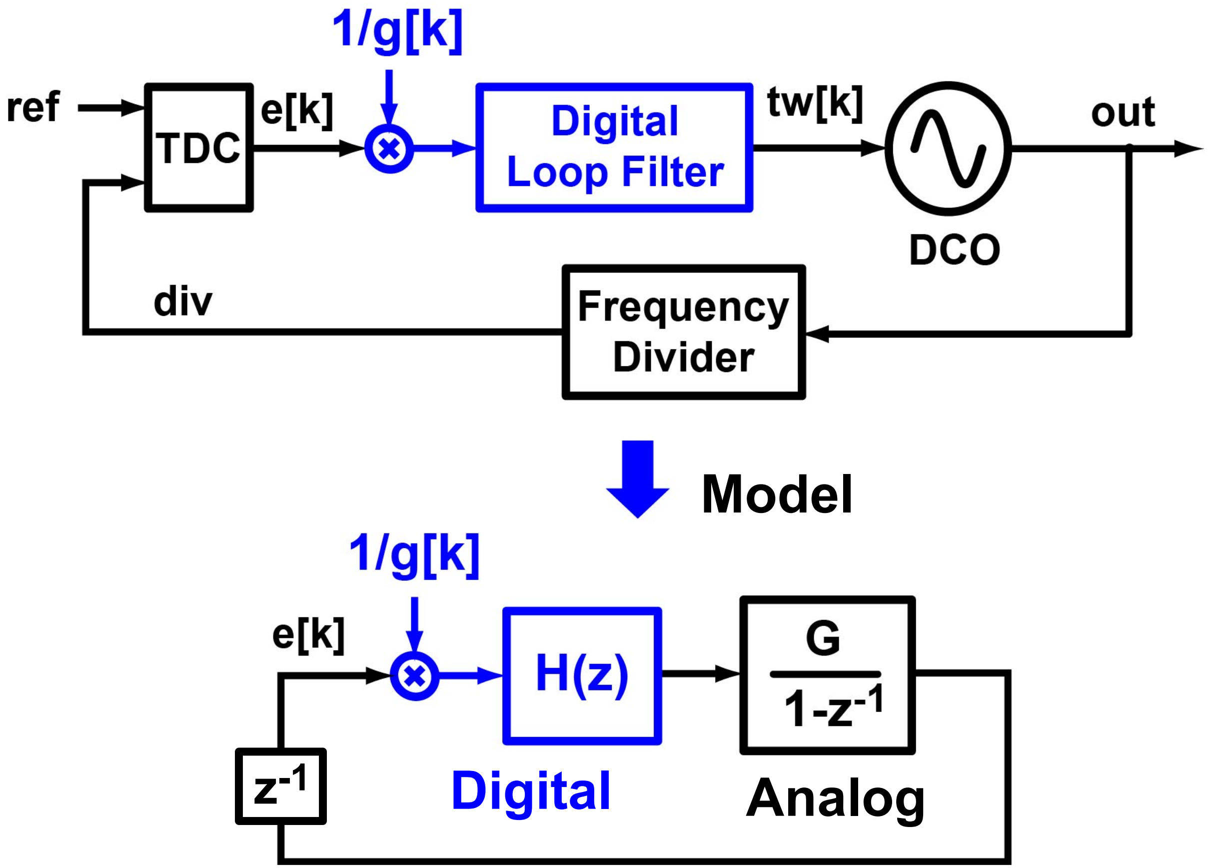
Loop BW sensitive to Analog Parameters





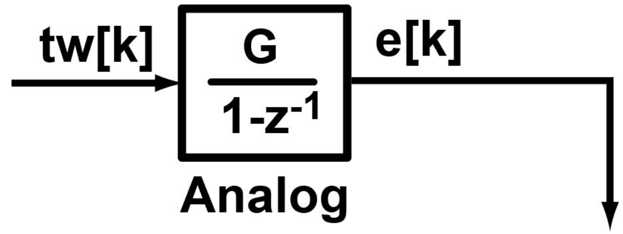
- **In any PLL, loop BW depends on PVT and output frequency (via K_{tdc} and K_T)**

Solution: Loop Gain Normalization

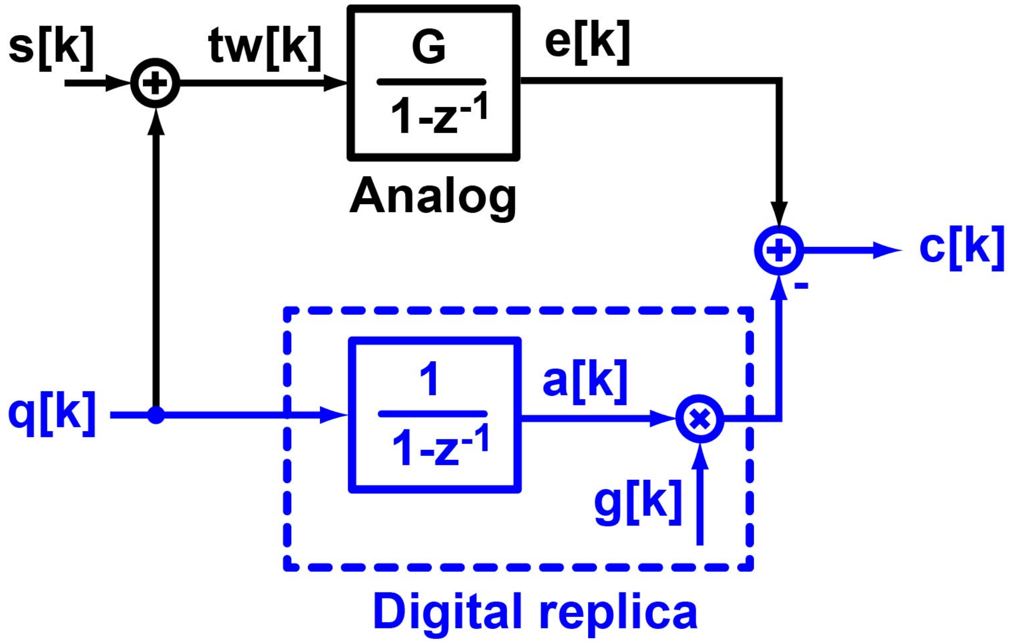


- **If g[k] = G, loop gain and BW are now insensitive to PVT**

How to Estimate Gain "G" (I)



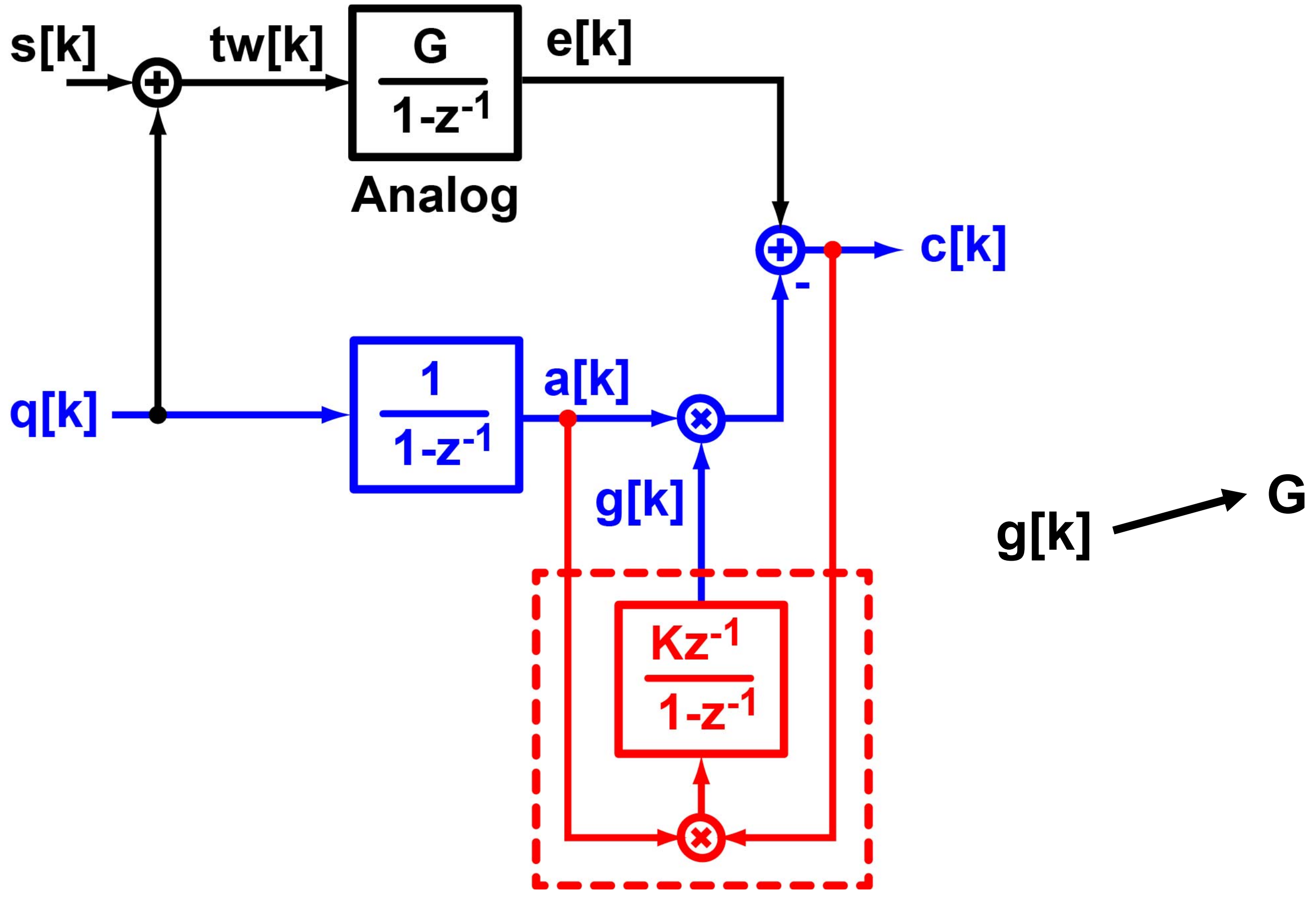
How to Estimate Gain "G" (II)



- We build a digital replica of analog section
- and feed a training sequence q[k]

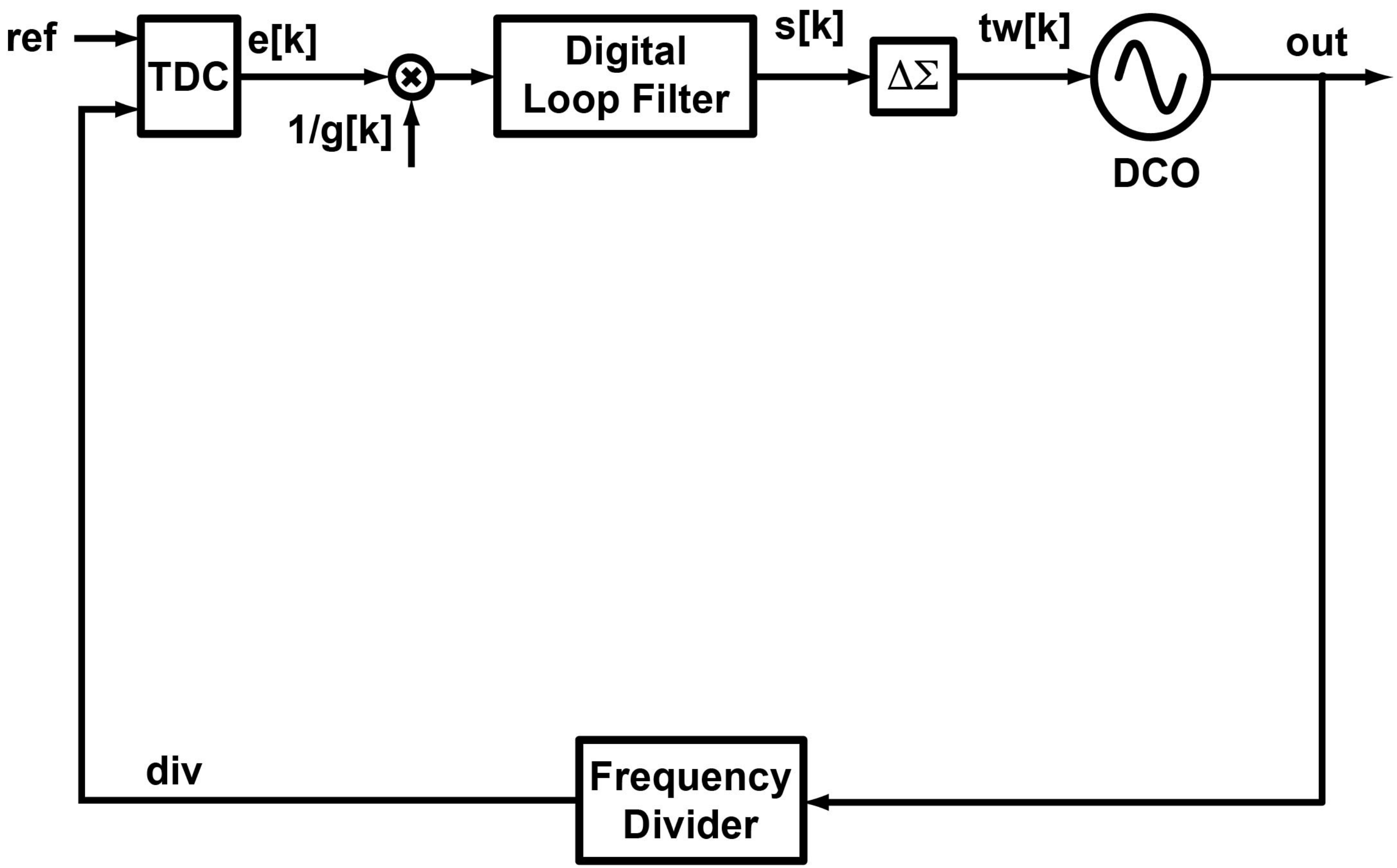
[Marzin, *ISSCC*, 2014]

How to Estimate Gain "G" (III)



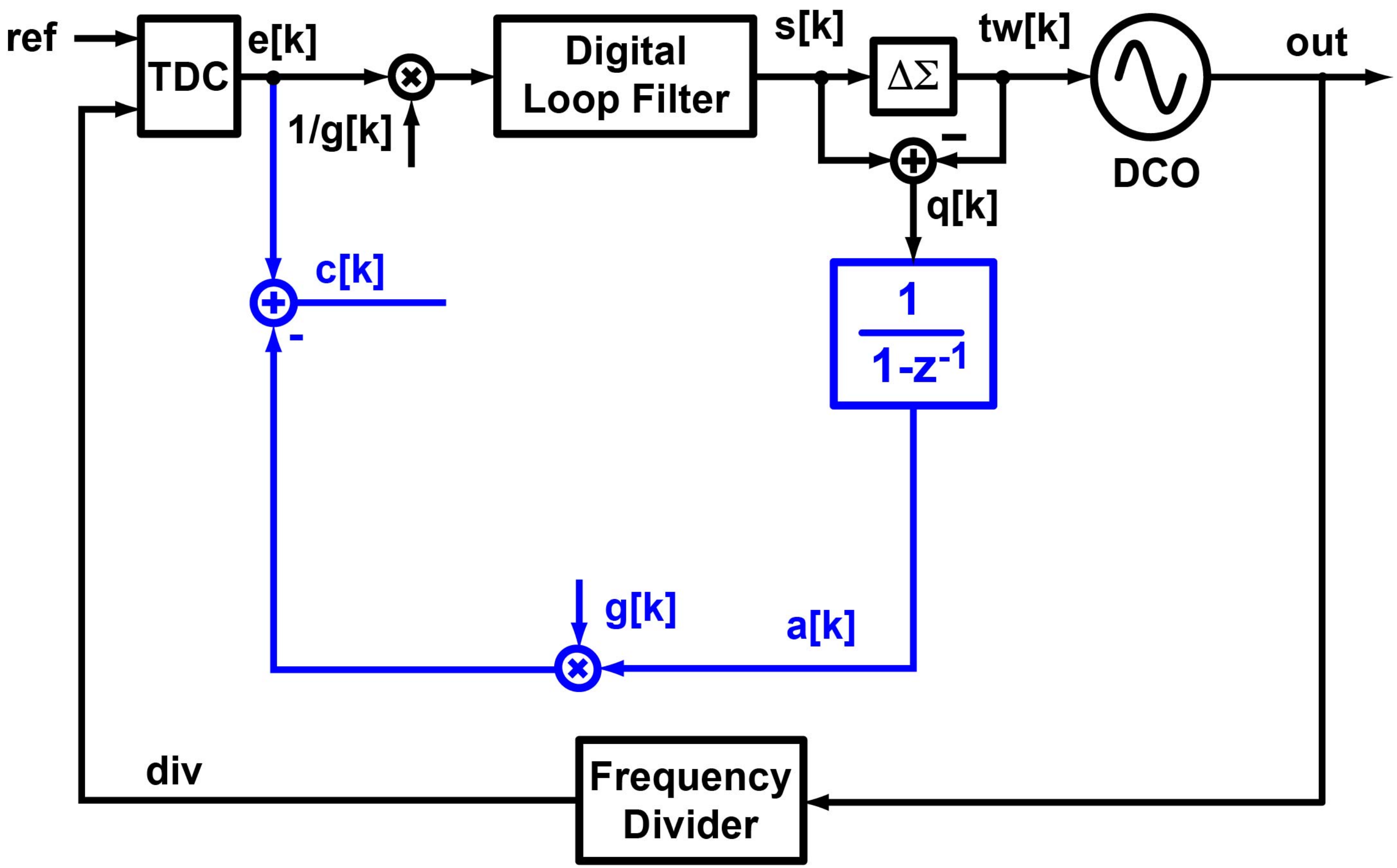
- **Feedback equalizes gains of the two paths**

Digital PLL with BW Calibration (I)



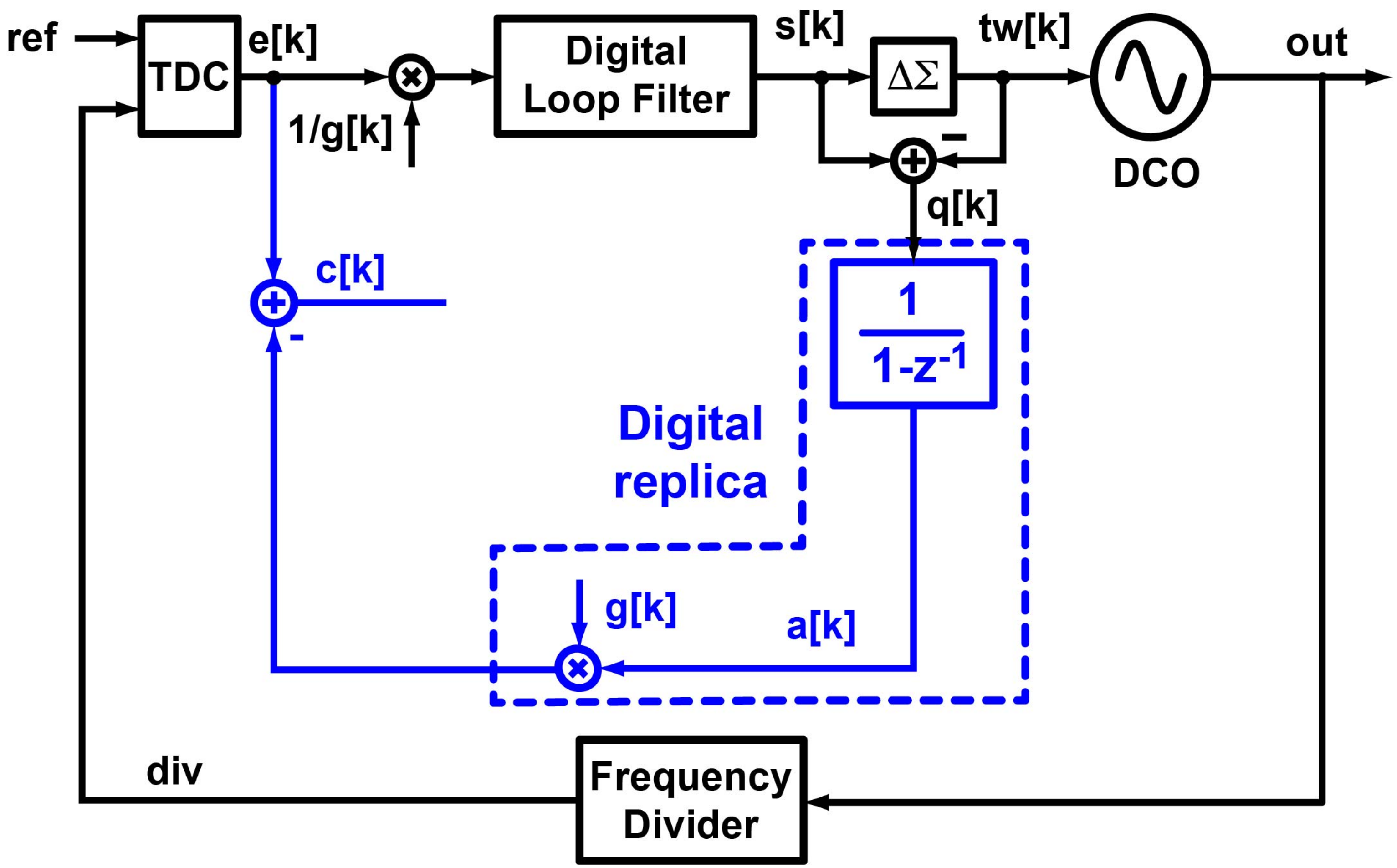
- **ΔΣ quantization used as training sequence**

Digital PLL with BW Calibration (II)



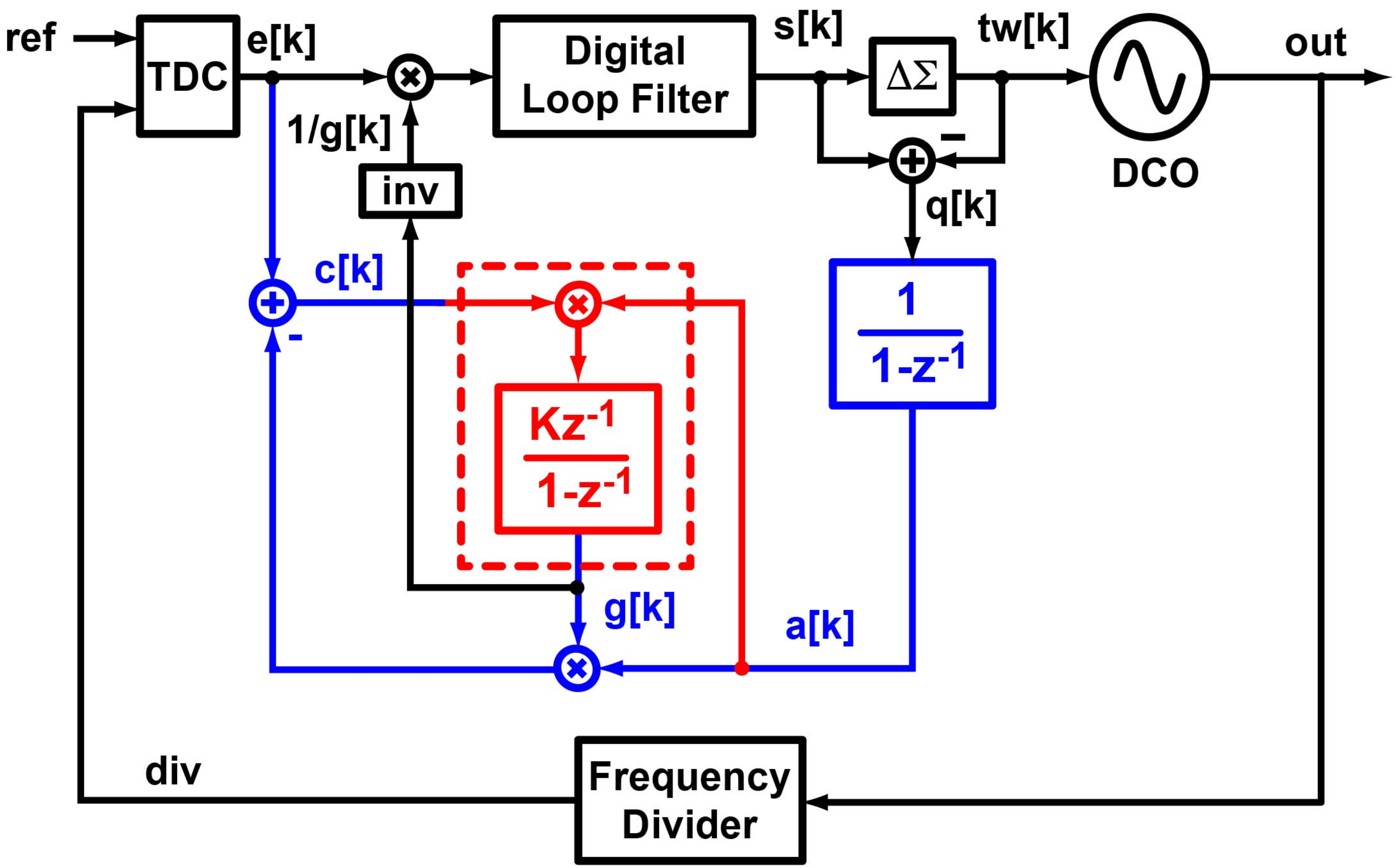
- **ΔΣ quantization used as training sequence**

Digital PLL with BW Calibration (III)



- **ΔΣ quantization used as training sequence**

Digital PLL with BW Calibration (IV)



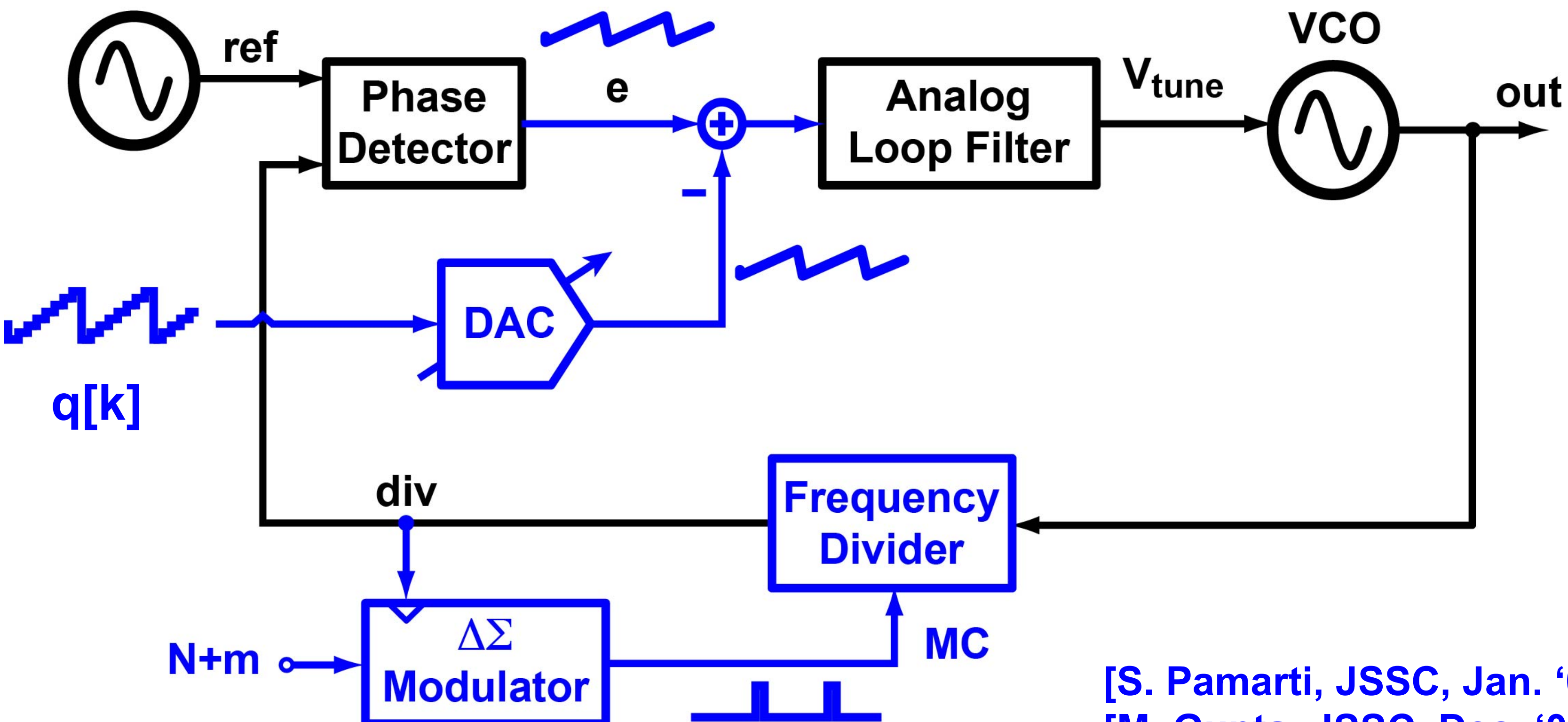
- **ΔΣ quantization used as training sequence**

Summary

- **Loop gain and BW of DPLLs (and bang-bang DPLLs) can be made independent of analog parameters via a background automatic regulation**
- **$\Delta\Sigma$ quantization error is used as training sequence (no added noise)**
- **Loop gain is estimated with correlation**

Fractional-N Frequency Synthesis with Digital PLLs

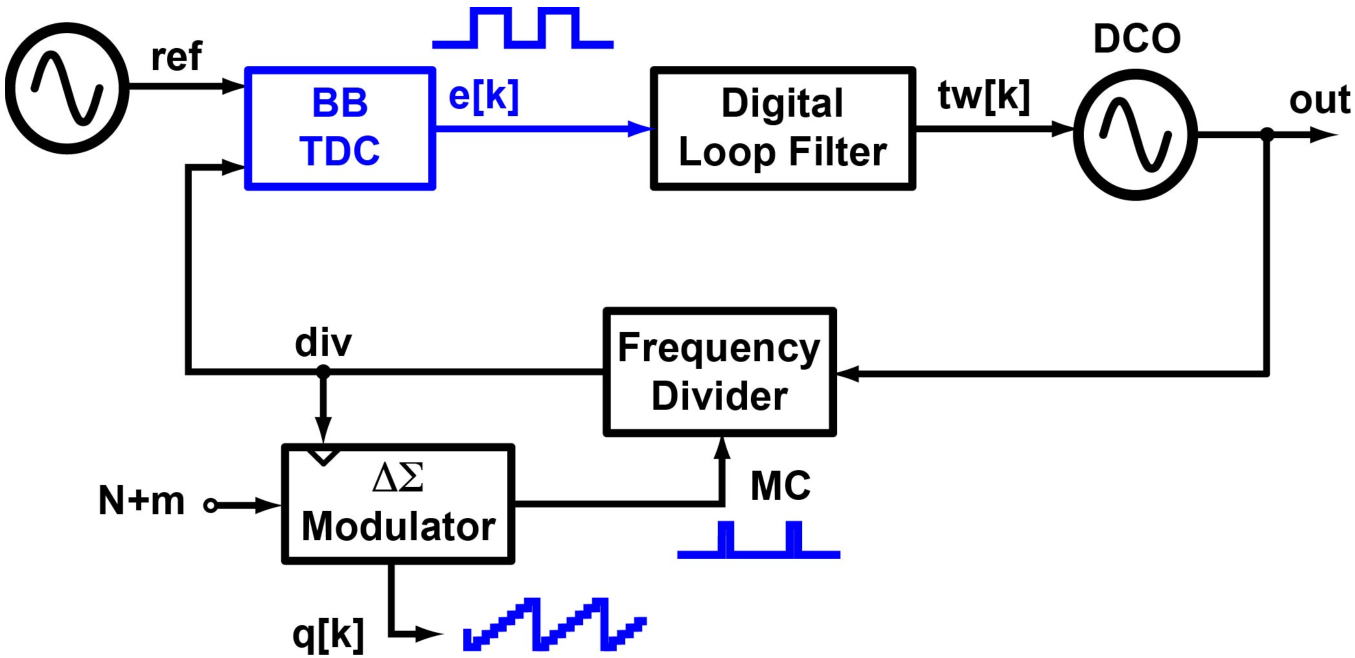
Conventional Fractional-N Synthesizer



[S. Pamarti, JSSC, Jan. ‘04]
[M. Gupta, JSSC, Dec. ‘06]

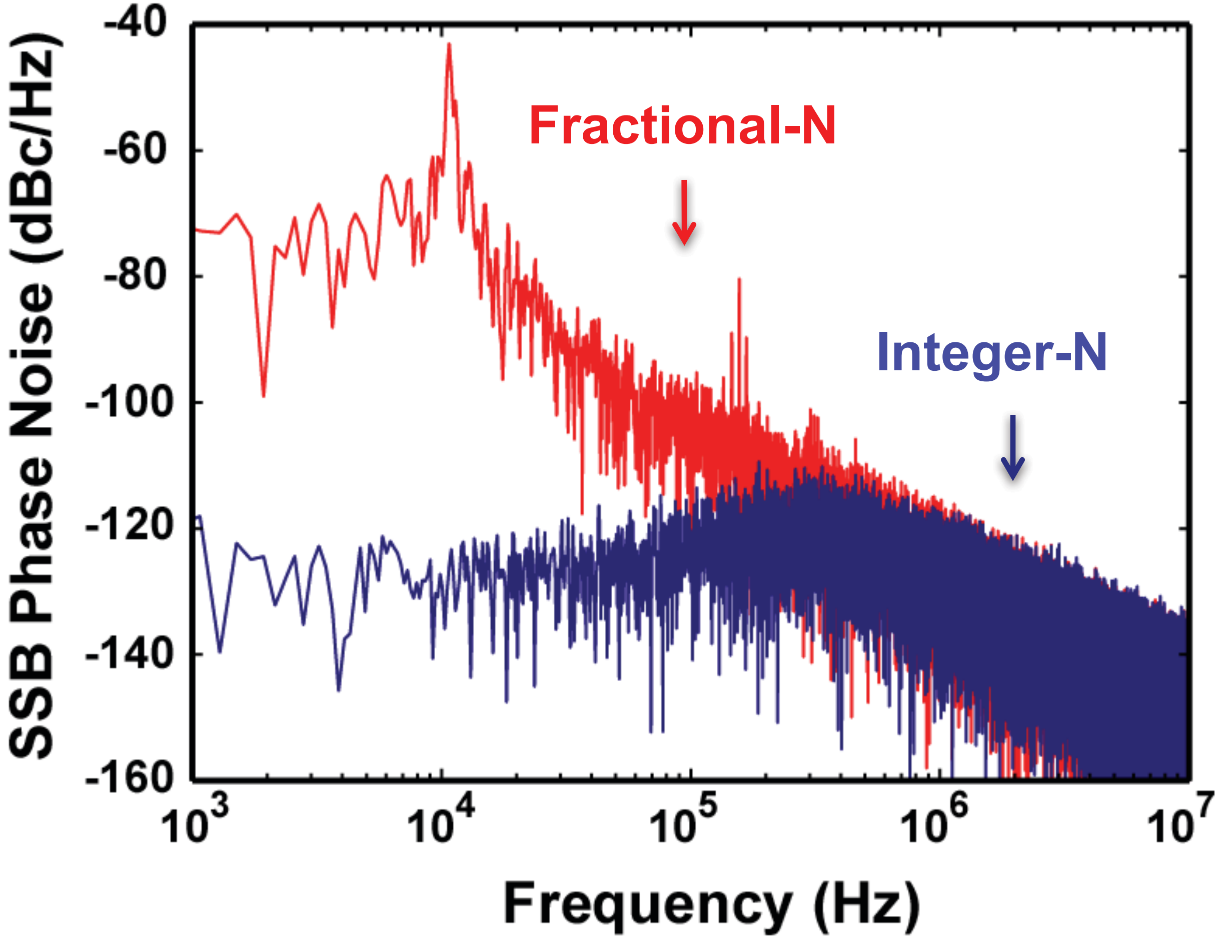
- **Quantization of ΔΣ is subtracted at PD out**
- **Needs calibration of DAC gain**

Fractional-N with Bang-Bang Phase Detect

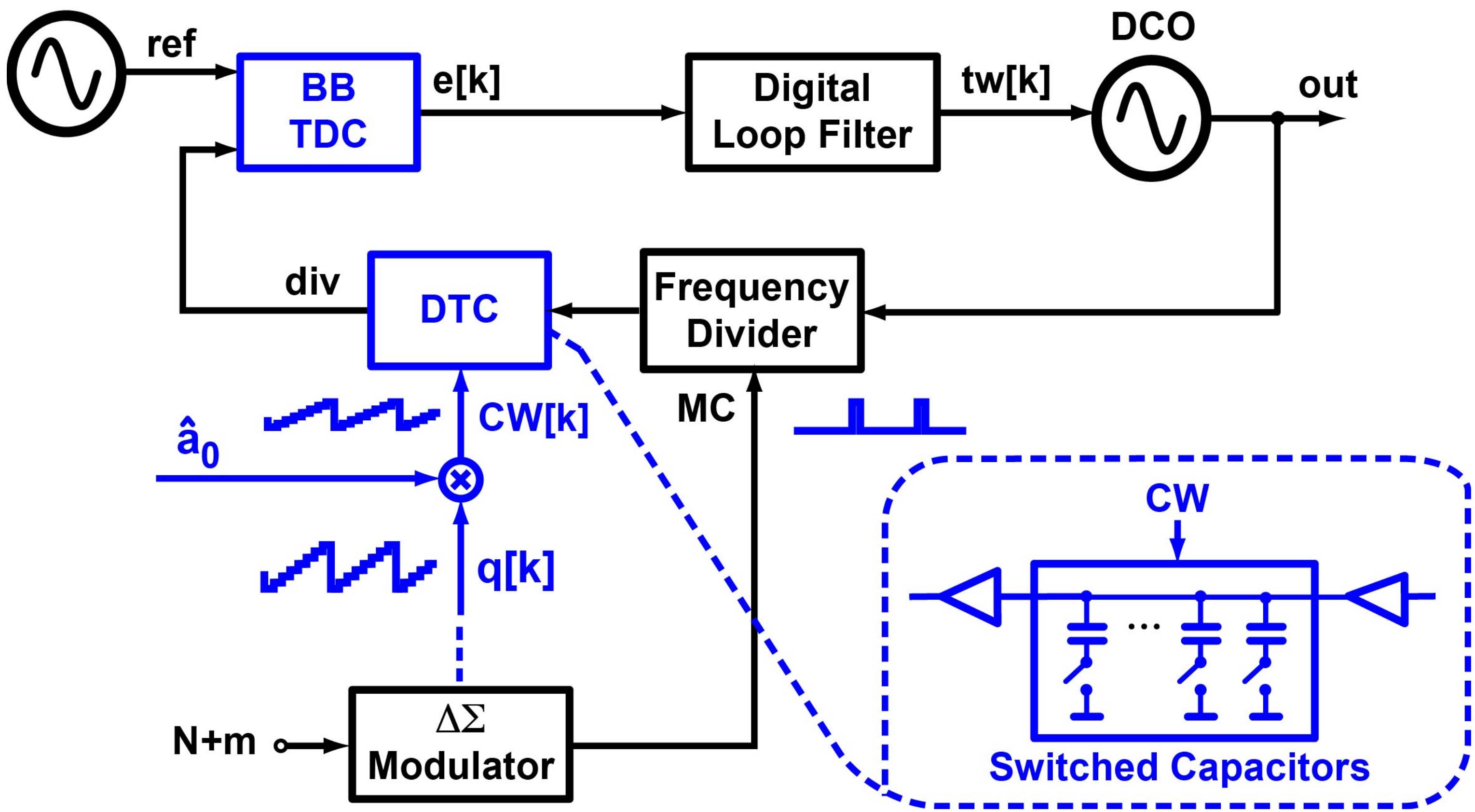


- The application of bang-bang TDC to fractional-N case is **not straightforward**
- Quantization noise saturates the detector, which works in the **limit-cycle regime**

Spectrum of Bang-Bang Fractional-N



Solution: Fractional-N Bang-Bang

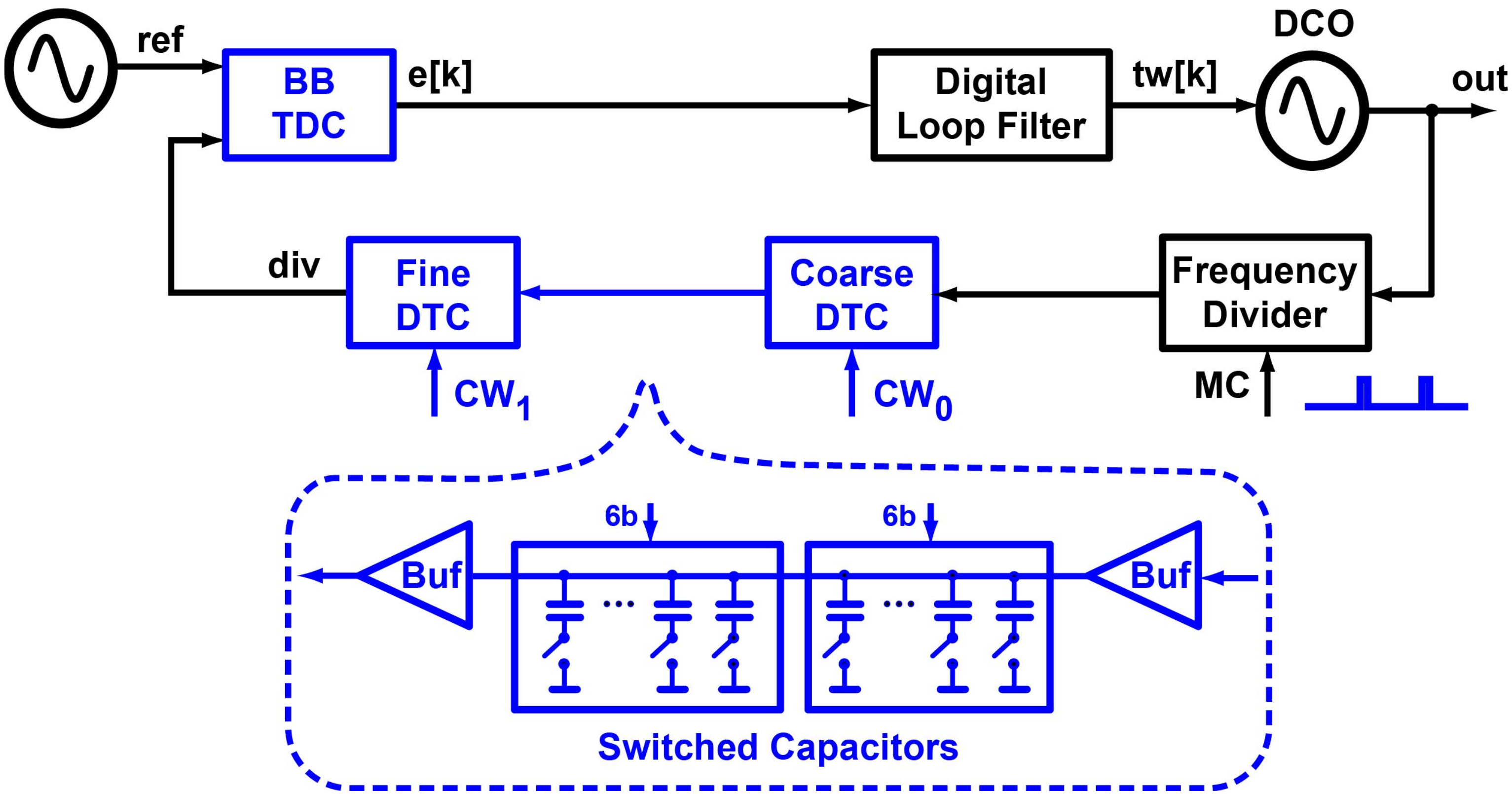


- ΔΣ noise is cancelled out via a low-power high-resolution DTC

[Tasca, *ISSCC*, 2011]

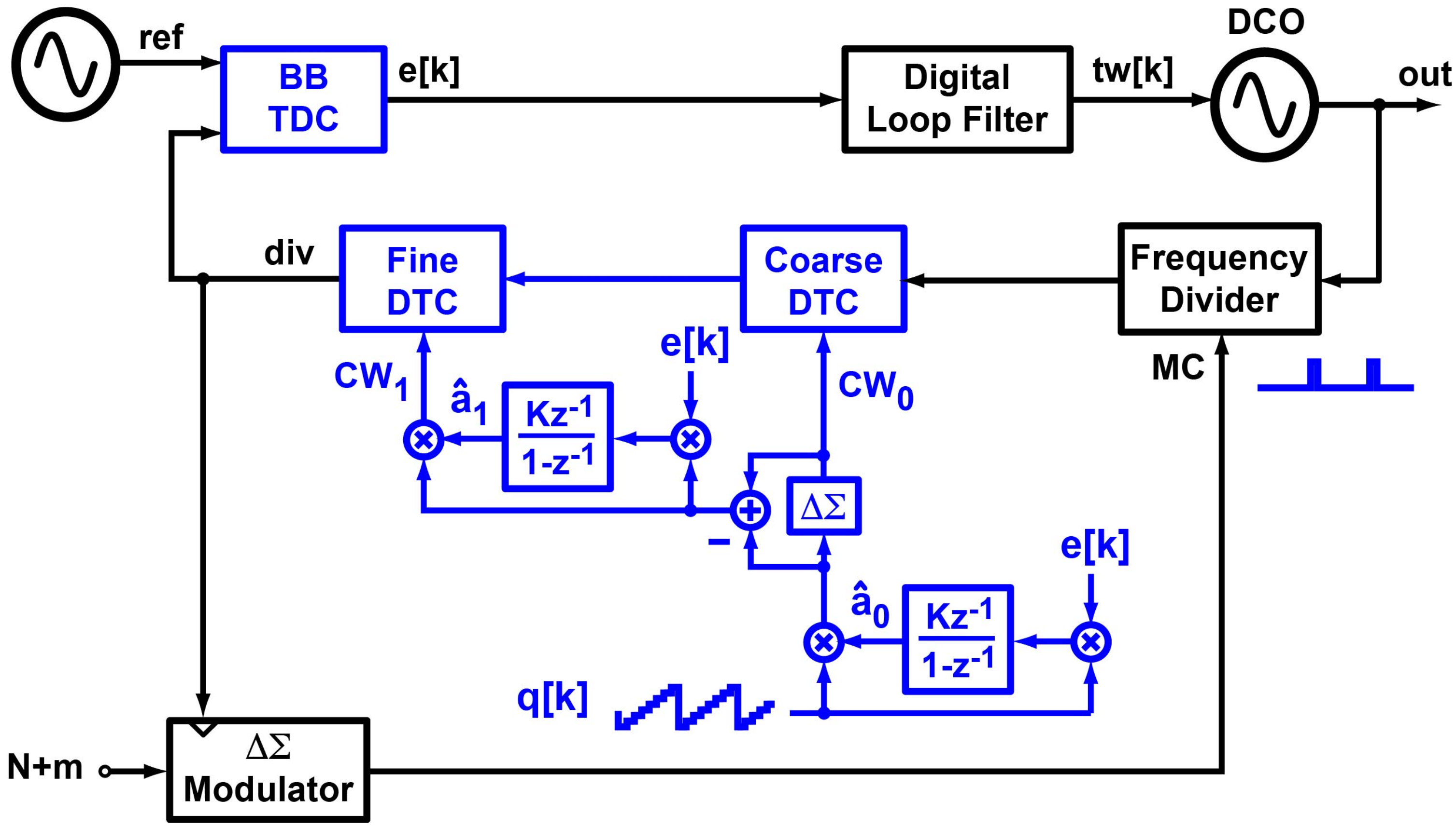
Examples of Practical Implementations

Bang-Bang DPLL for Frequency Synthesis (I)



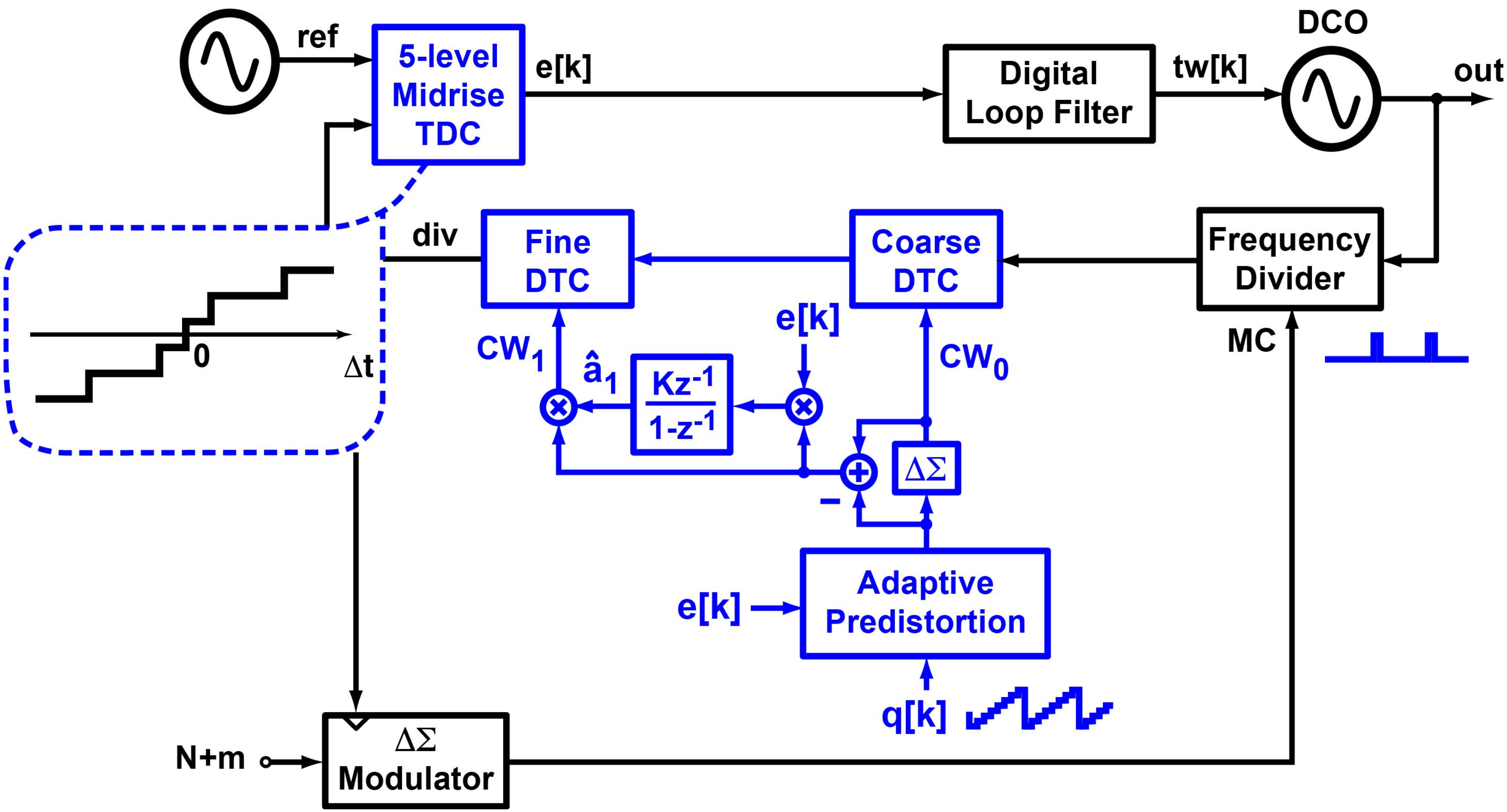
- **DTC segmented in two 6-bit banks**
- **10 equivalent bits**

Bang-Bang DPLL for Frequency Synthesis (II)



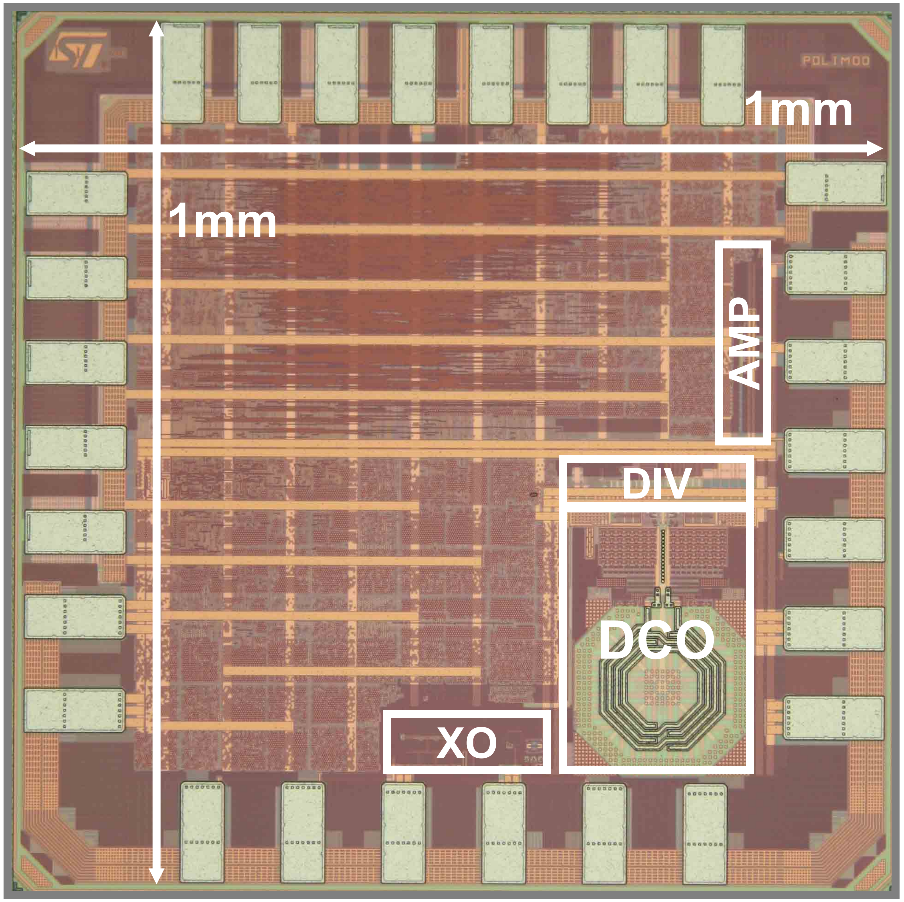
- **Feedback to estimate coarse DTC gain a_0 and fine DTC gain a_1**

Bang-Bang DPLL for Frequency Synthesis



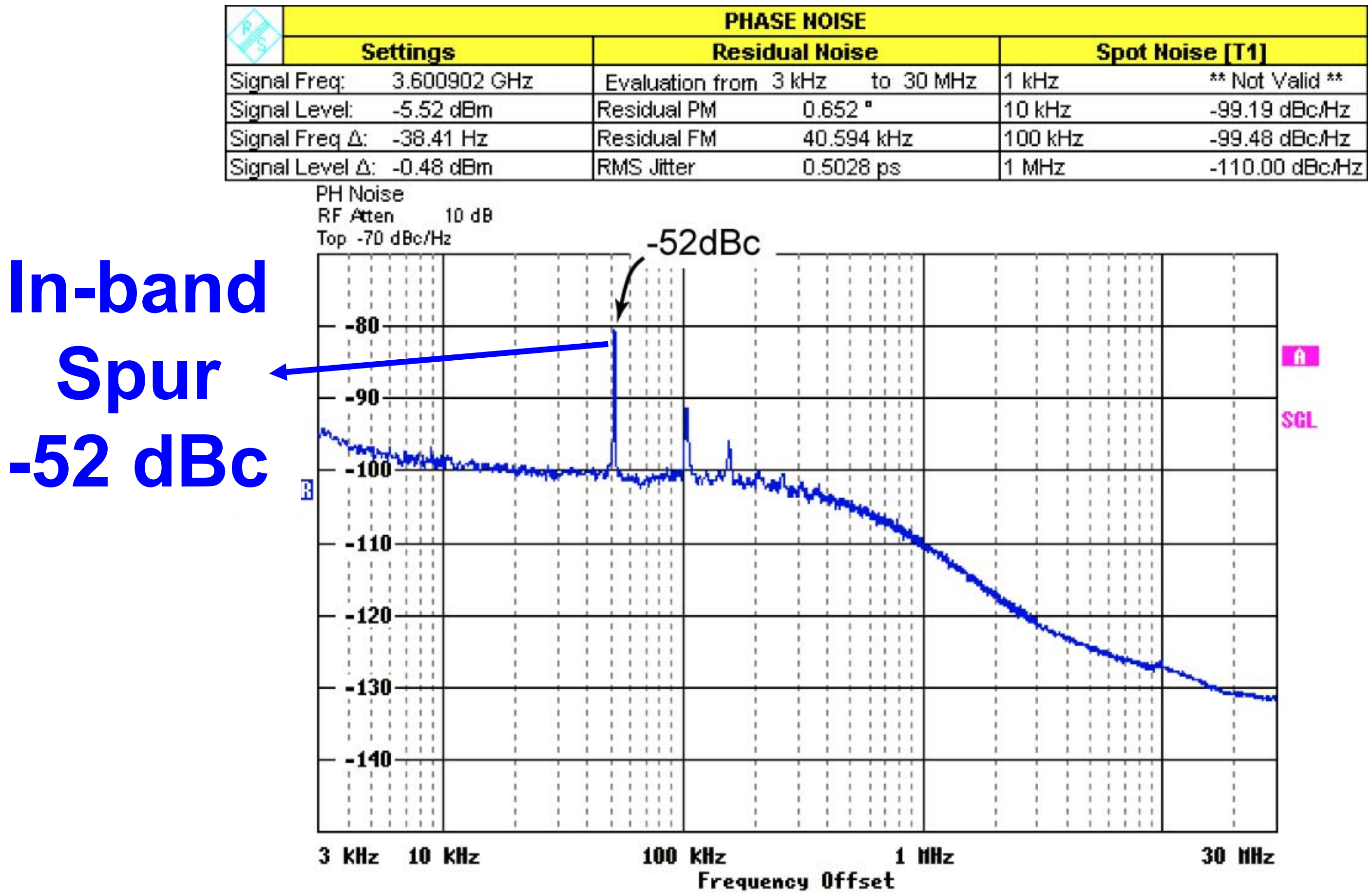
- Adaptive predistortion to reduce spurs
- 5-level TDC to speed up lock [Levantino, *JSSC*, 2014]

Die Photograph



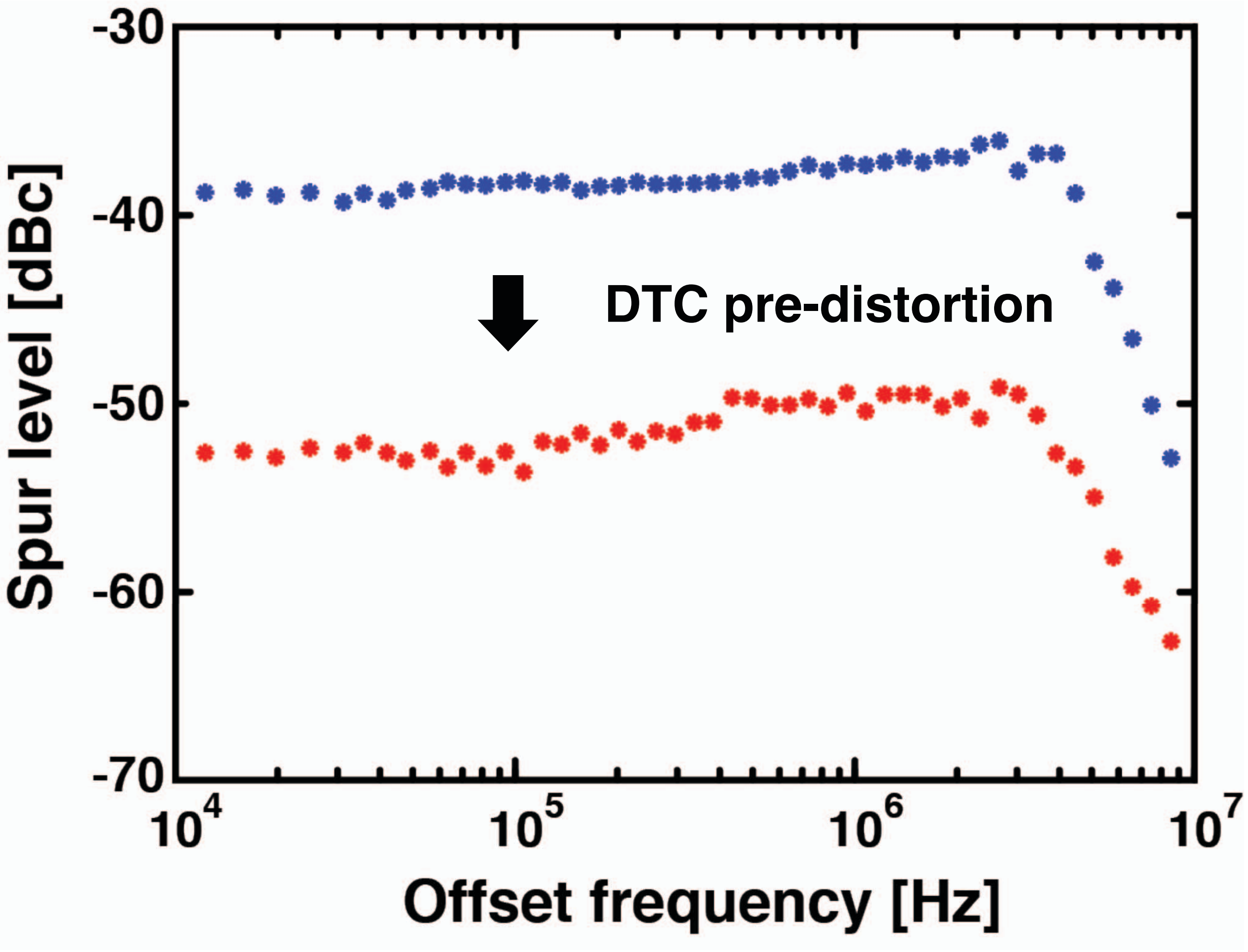
- Bang-Bang DPLL
- 65nm CMOS
- Active area: 0.52mm^2
- Supply: 1.2V
- Power: 4.2mW
- 2.9-4.0GHz out
- 40MHz ref

Measured Spectrum of Bang-Bang PLL

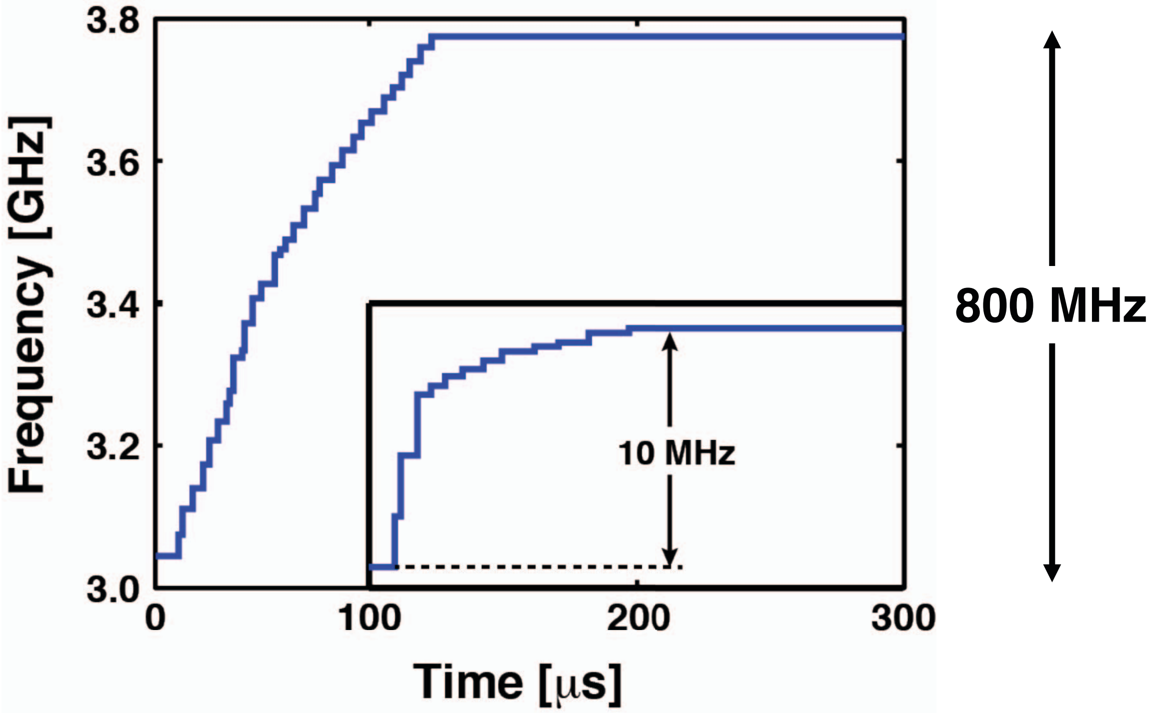


- Frequency is **50kHz offset from 3.6GHz**

Measured Spur Level of Bang-Bang DPLL



Lock Time of Bang-Bang DPLL

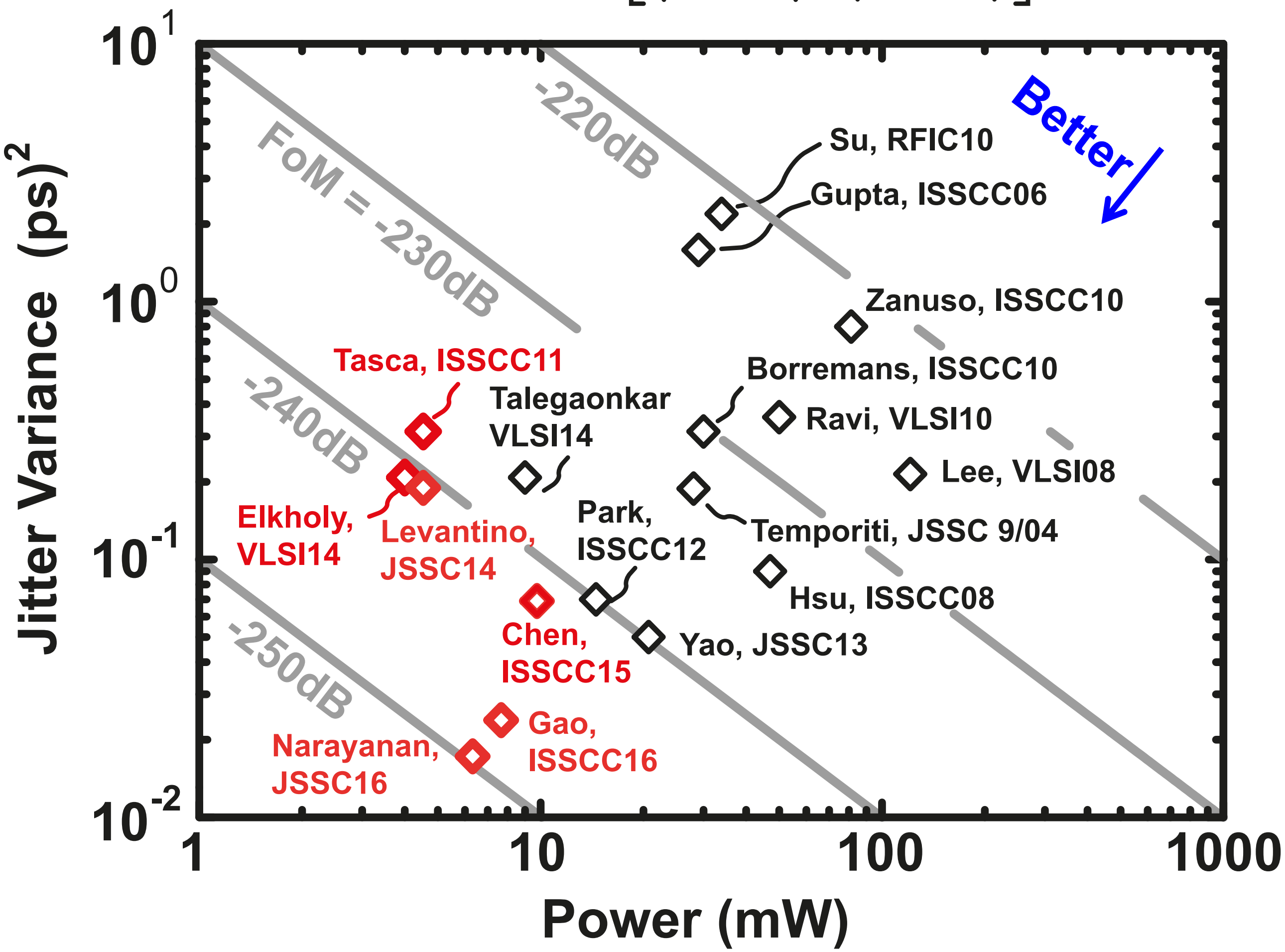


- **The presence of the coarse midrise TDC allows fast lock of the bang-bang DPLL**
- **Lock time is below 150 μs**

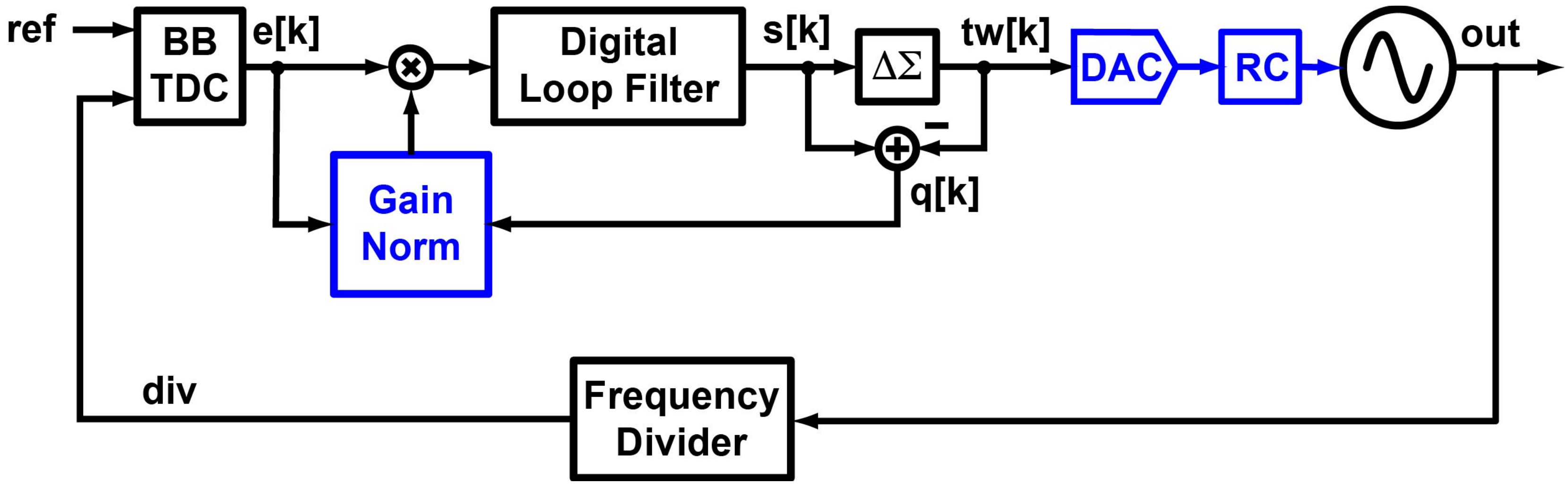
[Levantino, *ESSCIRC,* 2016]

PLL Figure of Merit (Fractional-N LC DPLL)

$$\text{FoM} = 10 \cdot \log\left[\left(\frac{\text{Jitter}}{1\text{s}}\right)^2 \cdot \left(\frac{\text{Power}}{1\text{mW}}\right)\right]$$



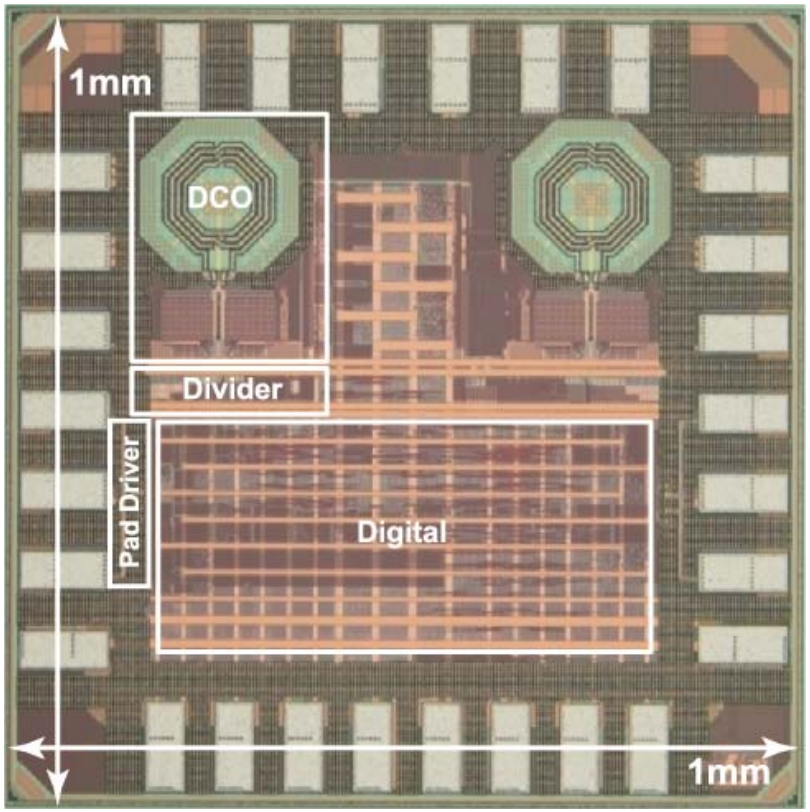
Bang-Bang DPLL w/Automatic BW Regulator



- **Resistor-string DAC and RC filter provides fine frequency resolution and good filtering of quantization noise**
- **Gain normalization for automatic BW regulation**

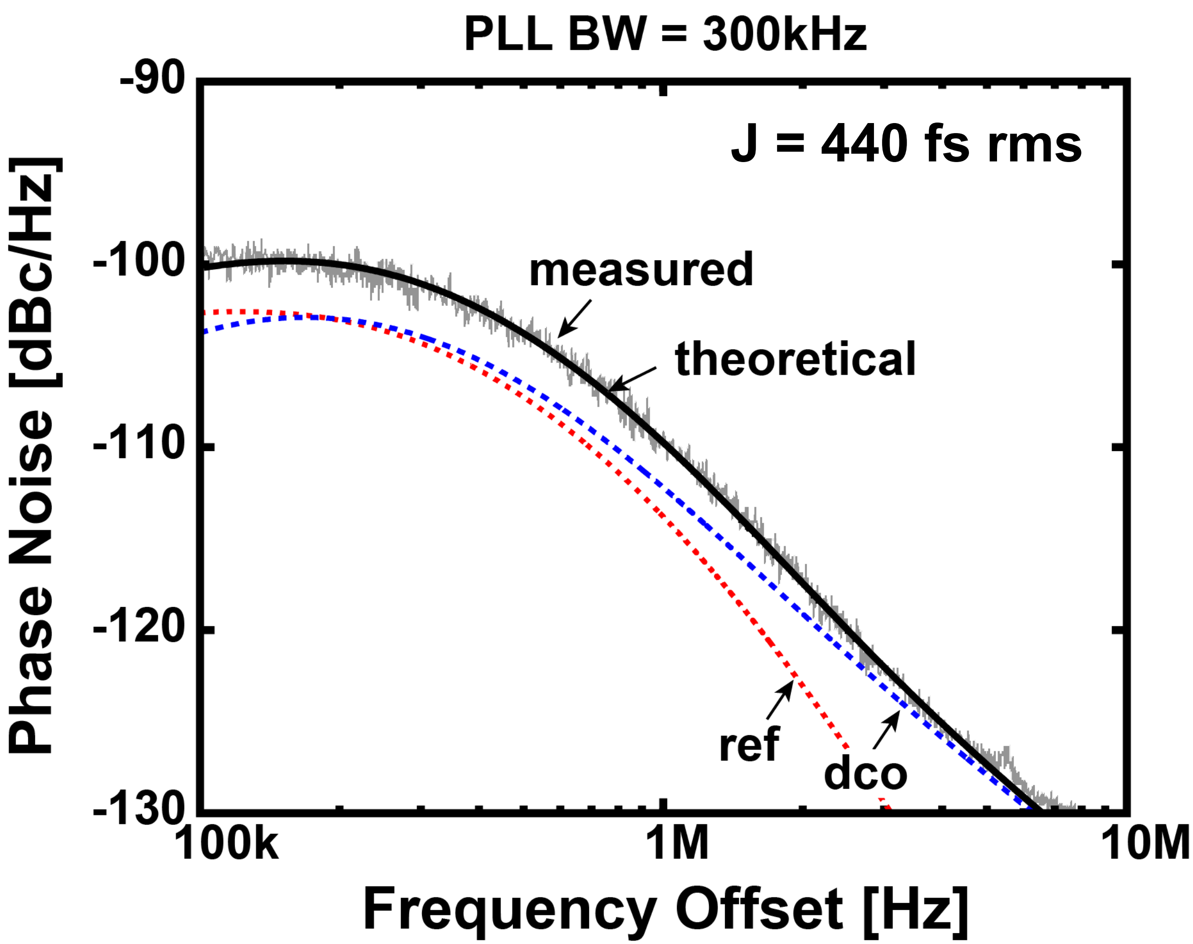
[Marzin, *ISSCC*, 2014]

Test Chip

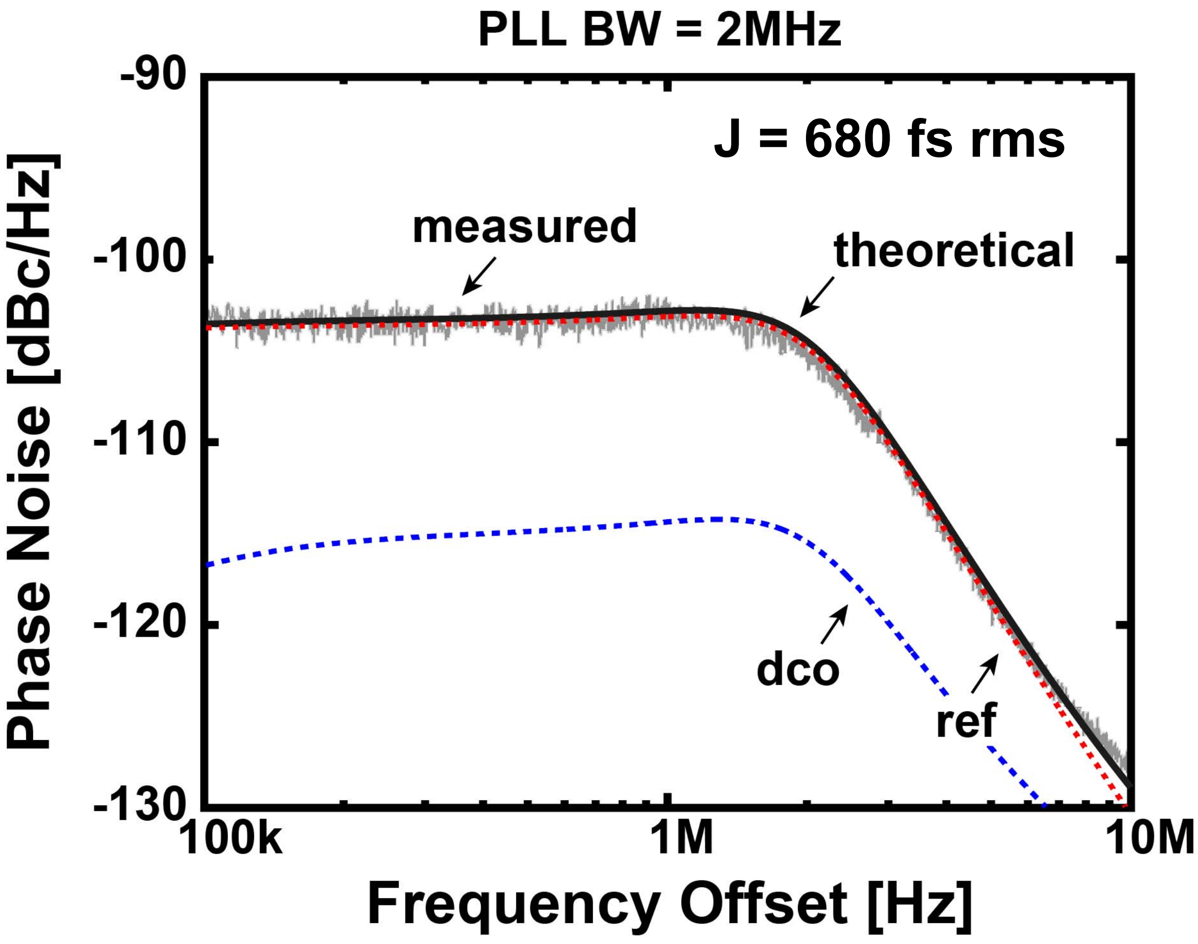


- **Bang-Bang DPLL**
- **65nm CMOS**
- **Active area: $0.2mm^2$**
- **Supply voltage: 1.2V**
- **Power: 4.5mW**
- **Calibration loop dissipation: 0.04mW**
- **Frequency range: 3-4GHz**

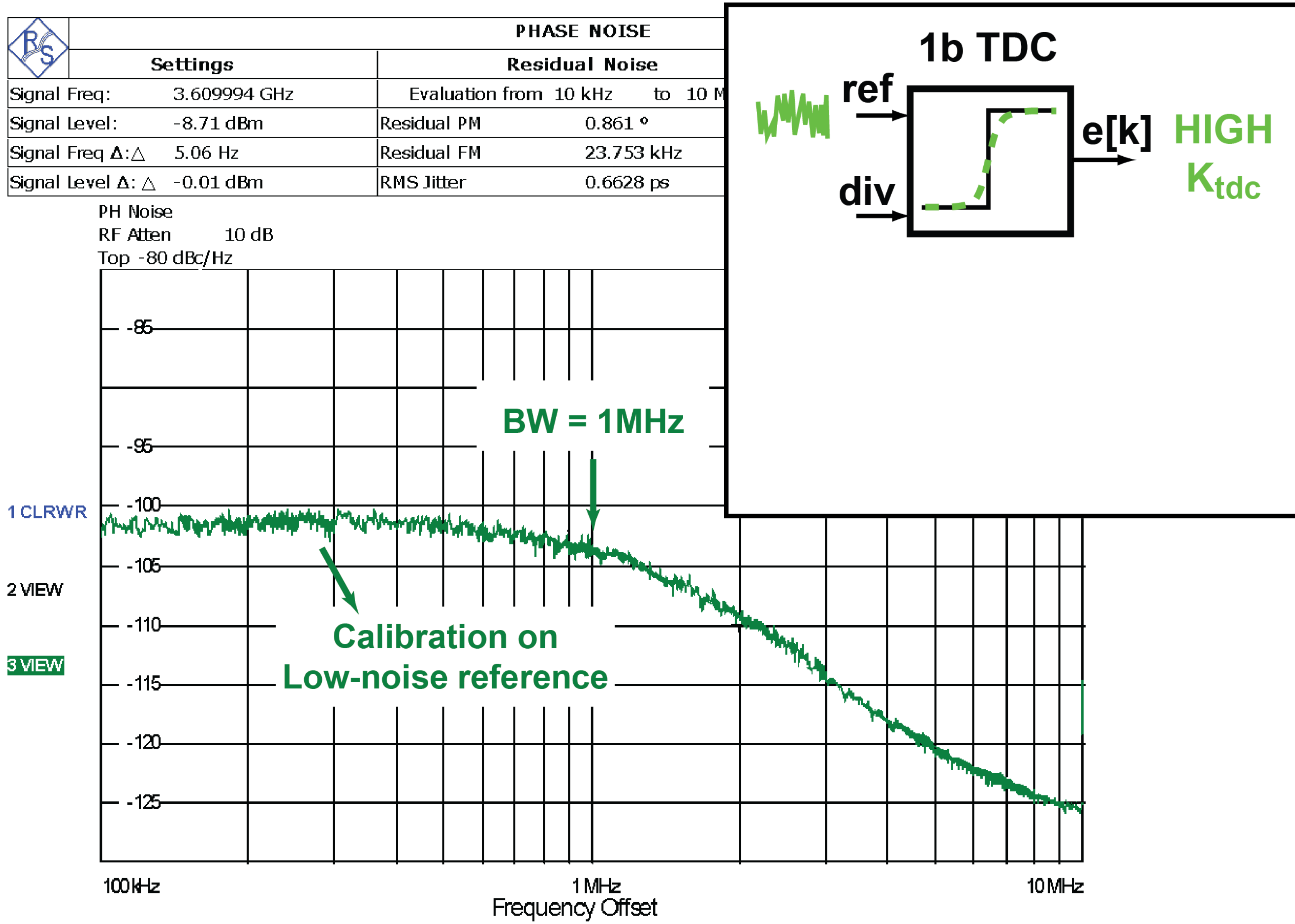
Measured Spectrum (300-kHz BW)



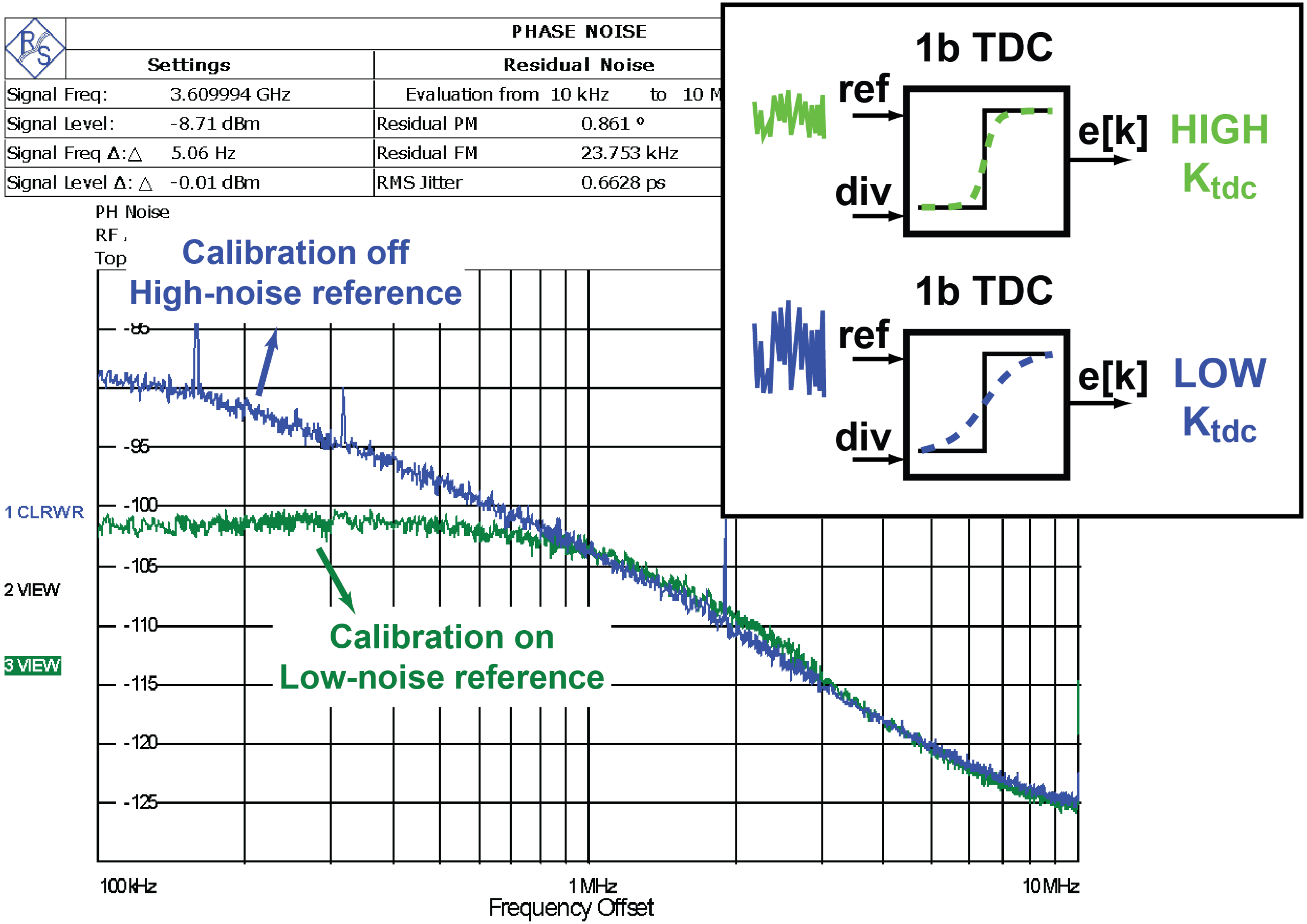
Measured Spectrum (2-MHz BW)



PN with Low Reference Noise

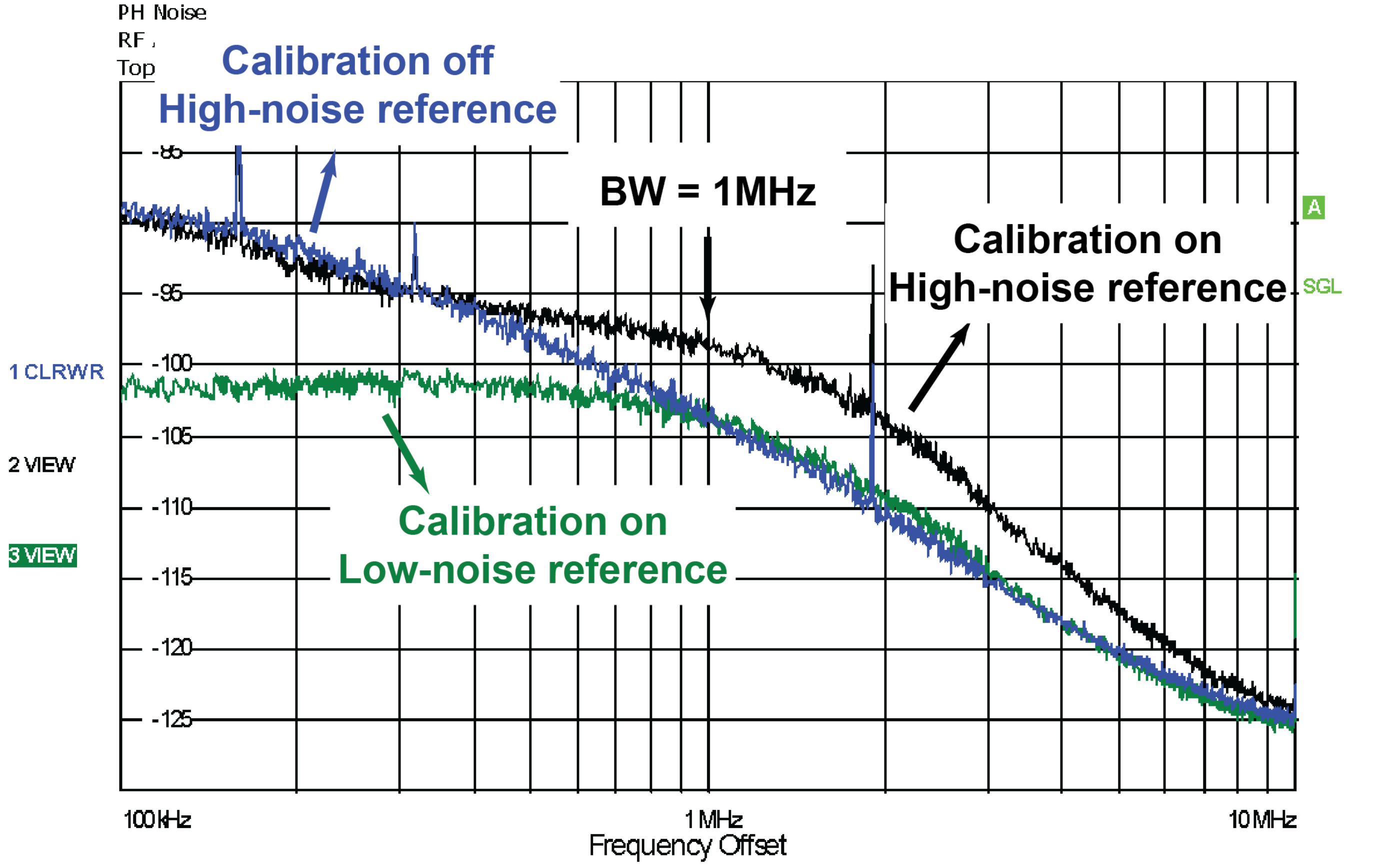


PN with High Reference Noise w/o Cal.



PN with High Reference Noise with Cal.

PHASE NOISE					
Settings		Residual Noise		Spot Noise [T3]	
Signal Freq:	3.609994 GHz	Evaluation from 10 kHz to 10 MHz		1 kHz	** Not Valid **
Signal Level:	-8.71 dBm	Residual PM	0.861 °	10 kHz	** Not Valid **
Signal Freq Δ:△	5.06 Hz	Residual FM	23.753 kHz	100 kHz	-101.73 dBc/Hz
Signal Level Δ: △	-0.01 dBm	RMS Jitter	0.6628 ps	1 MHz	-103.65 dBc/Hz



Summary

- DPLLs with bang-bang detectors (i.e. coarse TDCs with mid-rise quantization) can be employed even in fractional-N frequency synthesis
- In practice, they require a DTC block with fine resolution, whose performance can be improved leveraging oversampling techniques and digital pre-distortion
- DTCs are easier to be designed than TDCs
- Fractional-N BBPLLs maintain the superior efficiency (noise/power trade-off) over conventional DPLLs

Conclusions

- **Digital PLLs** exploit CMOS scaling and allow accurate **cancellation of fractional spurs** and **automatic bandwidth control**
- In Bang-Bang DPLLs assisted by DTC, performance is only limited by **DCO and DTC resolution**
- **Bang-Bang DPLLs assisted by DTC** allow same phase-noise performance and fractional-spur level as standard DPLLs at much lower power consumption

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