FA 14.1: A Compact Power-Efficient 3V CMOS Rail-to-Rail Input/Output Operational Amplifier for VLSI Cell Libraries

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The design of low-cost mixed/mode VLSI systems requires compact power-efficient library cells with a good performance. Digital library cells fully benefit from the continuing downscaling of CMOS processes, since these cells contain minimum-size components. Analog library cells, such as the opamp, cannot be designed using minimum-size transistors, for reasons of gain, offset, etc. Moreover, low-voltage rail-to-rail requirements complicate the design. To obtain compact low-voltage analog cells with a good performance, simple power-efficient designs need to be developed.

In principle, the two-stage opamp is suitable for a compact design. Published two-stage rail-to-rail opamps, however, contain complex class-AB output stages that use excessive die area [1]. Moreover, the class-AB control contributes significantly to the offset of the amplifier. This can be avoided, at the expense of die area, by inserting an intermediate stage between the input and the output stage [2].

This paper presents a compact two-stage 3V CMOS opamp that is suitable as a VLSI library cell because of its small die area. The opamp, shown in Figure 1, contains a rail-to-rail input stage, M_1-M_4 [3]. The current mirrors M_{11}-M_{14} and M_{15}-M_{18} add the signals of the rail-to-rail input stage. Both current mirrors are biased by one side of the floating current source, I_{b3}. This provides a constant current, I_{b3}, in the cascode transistors, M_{14} and M_{16}, independent of the bias currents of the n-channel and p-channel input pair.

The constant current in the cascode transistors of the summing circuit biases the class-AB driver circuit, M_{19}-M_{20} [4]. This avoids a contribution to the noise and offset of the opamp of two independent current sources, that would otherwise be necessary to bias the floating class-AB driver.

The class-AB driver circuit biases the output transistors M_{25}-M_{26}. The floating architecture of the class-AB control has the same advantages as the floating current source: it does not contribute to the noise and offset of the amplifier. The result is that the offset and the noise of the opamp are of the same order as the offset and noise of a three stage opamp.

Using the topology described above, two opamps are realized. The first is shown in Figure 2. The input pairs, M_1-M_4, operate in strong inversion, which combines a relatively large gm and relatively small input transistors. To obtain a constant transconductance over the whole common-mode input range, the current switches, M_5 and M_8, and the 3x current mirrors, M_6-M_7 and M_9-M_{10}, are added to the input stage [5].

The biasing circuit, M_{29}-M_{31}, switches off M_8 at supply voltages lower than 2.9V. This prevents M_5-M_{10} from forming a positive feedback loop at supply voltages larger than 2.9V.

The summing circuit, M_{11}-M_{18}, and the class-AB output stage, M_{19}-M_{26}, are biased by a floating current source, M_{27}-M_{28}. The value of the floating current source is determined by the translinear loops M_{21}, M_{22}, M_{28}, M_{11} and M_{23}, M_{24}, M_{27}, M_{17}. The mirrors M_{11}-M_{14} and M_{15}-M_{18} are loaded by the input pairs. This means that the gate-source voltage of M_{11} and M_{17} vary as a function of the common-mode input voltage. However, the current of the floating current source changes only 3%, because an increase of the gate-source voltage of one mirror compensates for a decrease in the other mirror.

The floating current source has the same structure as the class-AB driver circuit, M_{19}-M_{20}. Therefore, the supply voltage dependence of the floating current source and class-AB driver largely compensate each other. The result is a quiescent current independent of the supply voltage.

The opamp is frequency compensated using the Miller technique [4]. The capacitors, C_{M1} and C_{M2}, split the poles around the output transistors M_{25} and M_{26}, ensuring a 20dB per decade roll off of the amplitude characteristic.

In Figure 3, a second realization of the compact rail-to-rail opamp is shown. This opamp is basically the same as the opamp shown in Figure 2, except for the frequency compensation. This opamp is compensated by including the cascode stages, M_{14} and M_{16}, in the Miller loops, increasing the unity-gain frequency from 2.6MHz to 6.4MHz.

The opamps are realized in a 0.8µm BiCMOS process. The n-channel transistors and p-channel transistors have threshold voltages of 0.64V and -0.75V, respectively. Micrographs of the compact opamp with Miller compensation and the op-amp with cascoded Miller compensation are shown in Figure 4 and Figure 5, respectively. A list of specifications is given in Table 1. Opamp1 contains the Miller compensation. Opamp2 contains the cascoded Miller compensation. At supply voltages from 2.5V to 2.9V the common-mode input range is from V_{SS}-0.4V to V_{DD}-1.4V. At supply voltages above 2.9V, the input stage has a common-mode input range from V_{SS}-0.4V to V_{DD}+0.5V. The CMMR of the opamps is 43dB in the transition regions of the current switches. It increases up to 70dB, when the common-mode input voltage is near one of the supply rails. The Bode plots of the compact opamp with Miller compensation and the compact opamp with cascoded Miller compensation are shown in Figures 6 and 7, respectively.

References

[1] Botma, J. H., et al., "A Low-Voltage CMOS Operational Amplifier with a Rail-to-Rail Constant-gm Input Stage and a Class AB Rail-to-Rail Output Stage", Proceedings ISCAS 93, pp. 1314-1317.

[2] Pardoen, M. D., M. G. Degrauwe, "A Rail-to-Rail Input/Output CMOS Power Amplifier", IEEE J. Solid-State Circuits, vol. SC-25, pp. 501-504, Dec., 1990.

[3] Huijsing, J. H., J. P. Tero, "Combination driver-summing circuit for rail-to-rail differential amplifier", US Pat. Appl. Ser. No. 36774, filed March 25, 1993.

[4] Montecelli, D. M., "A Quad CMOS Single-Supply Op Amp with Rail-to-Rail Output Swing", IEEE J. Solid-State Circuits, vol. SC-21, pp 1026-1034, Dec., 1986.

[5] Hogervorst, R., et al., "CMOS Low-Voltage Operational Amplifiers with Constant-gm Rail-to-Rail Input Stage", Proceedings ISCAS 92, pp. 2876-2879

[6] Huijsing, J. H., D. Linebarger, "Low-voltage operational amplifier with rail-to-rail input and output ranges", IEEE J. Solid-State Circuits, vol. SC-20, pp. 1144-1150, Dec., 1985.

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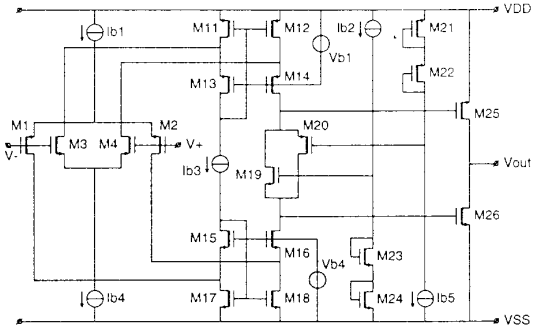

Figure 1: Basic topology of rail-to-rail opamp.

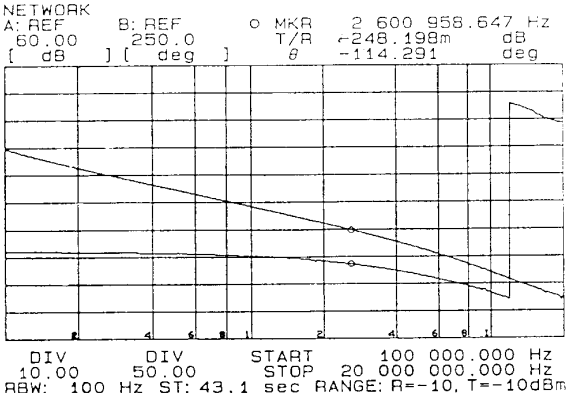

Figure 6: Frequency response of opamp with Miller compensation.

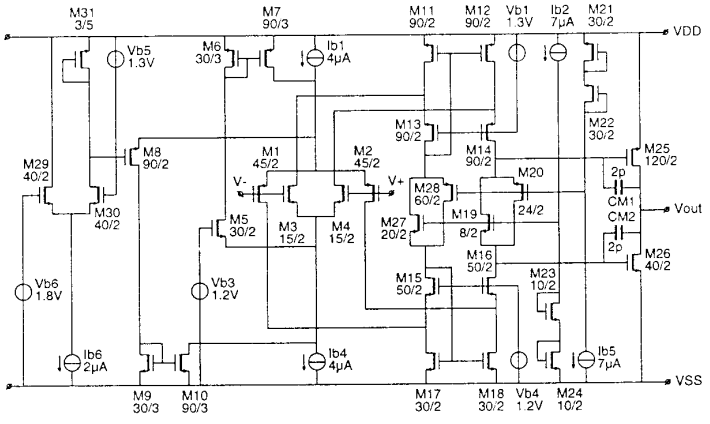

Figure 2: Opamp with Miller compensation.

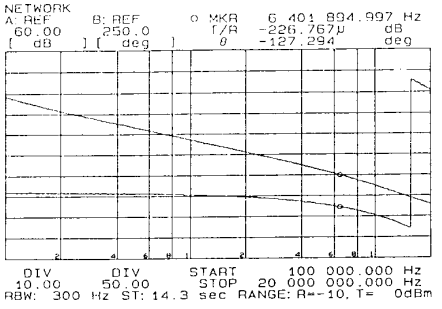

Figure 7: Frequency response of opamp with cascoded Miller compensation.

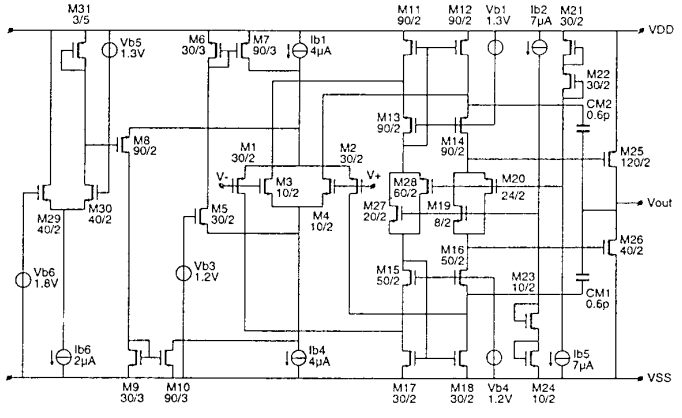

Figure 3: Opamp with cascoded Miller compensation.
Figures 4 and 5: See page 345.

Parameter	opamp1	opamp2	Unit
Die area	0.04	0.04	mm^2
Supply:			
voltage range	2.5-6.0	2.5-6.0	V
quiescent current	180	180	μA
Peak output	±3	±3	mA
Offset voltage	4.0	5.0	mV
Input noise at 10kHz	22	31	$nV/\sqrt{Hz}$
Open-loop gain	87	85	dB
Unity-gain:			
frequency	2.6	6.4	MHz
margin	66	53	°

Table 1: Measurement results. (V_{supply}=3.3V, R_{load}=10kΩ, C_{load}=10pF, T_A=27°C)