A Sub-1 ppm/°C Precision Bandgap Reference With Adjusted-Temperature-Curvature Compensation

Hou-Ming Chen, Chang-Chi Lee, Shih-Han Jheng, Wei-Chih Chen, and Bo-Yi Lee

***Abstract*— This paper presents a precision bandgap reference with an innovative adjusted-temperature-curvature compensation circuit that obtains a good temperature coefficient (TC) over a wide temperature range. The proposed compensation circuit for enhancing the voltage accuracy of the bandgap reference combines an addition circuit, subtraction circuit, and current mirror to achieve an adjusted piecewise linear temperature current over an entire temperature range. The proposed bandgap reference was designed and fabricated using a standard Taiwan Semiconductor Manufacturing Company (TSMC) 0.18 μm 1P6M CMOS technology. Measurements on eight samples indicated that the proposed bandgap reference achieved a TC that varies from 1.67 to 10.55 ppm/°C from −40 °C to 140 °C with a supply voltage of 1.8 V. The measured 547 mV reference voltage achieved a precision line regulation that is less than 0.08%/V for supply voltages between 1.3 and 1.8 V. The proposed circuit dissipated 28 μA with a supply voltage of 1.8 V, and an active area of 0.0094 mm^2. The circuit was designed to operate on a low supply voltage down to 1.3 V.**

***Index Terms*— Adjusted-temperature-curvature (ATC) compensation, bandgap reference, line regulation, piecewise linear temperature current and temperature coefficient (TC).**

I. Introduction

BANDGAP references are widely used in analog circuits, digital circuits, and mixed-signal circuits, such as operational amplifiers, linear regulators, DRAM, A/D converters, phase-locked loops, and power converters because of their high accuracy and temperature-independence [1]–[28]. The performance of such circuits is often limited by the precision of their reference voltages over supply voltage, temperature, and process variations. Many studies [19]–[28] have been conducted to achieve a high-precision bandgap reference. Because conventional bandgap references [1]–[9] are limited by the common-collector structure of the parasitic vertical bipolar junction transistor (BJT), the minimum supply voltage must be higher than 1.25 V. In contemporary battery-operated products such as smart phones, tablets, and cameras, low voltage and low power are two essential design features that extend battery service times. The classic methods proposed in [10]–[28] achieve a sub-1 V reference voltage by using a combination of a reference current and a resistor.

In recent years, the temperature drift of the reference voltage has been a critical challenge in numerous prominent studies [19]–[28] that have the proposed temperature compensation techniques that obtain a good temperature coefficient (TC) (3.4–12 ppm/°C) over a wide temperature range. Different types of highly resistive poly resistors [5] have been incorporated into the compensation design aimed at canceling the nonlinear temperature dependence of the emitter–base voltage $V_{\rm EB}$. To reduce the temperature drift, Zhou *et al.* [7] realized exponential curvature compensation with many higher order terms over a temperature range and a logarithmic curvature compensation term proportional to $V_T \ln T$ in higher temperature ranges. A piecewise-nonlinear curvature-corrected technique [20] was adopted to generate a corrected current that contains zero, exponential with temperature, and proportional to the square temperature in the lower, middle, and higher temperature ranges. Andreou *et al.* [22] used the unequal current densities of BJTs to achieve a higher order cancellation of the base–emitter voltage nonlinearity over a considerably wider temperature range. Ma and Yu [24] used MOS transistors operating in weak inversion regions to cancel nonlinear temperature dependence. The previously cited techniques [1]–[28] can effectively improve the bandgap reference voltage with convex curves.

This paper proposes an innovative adjusted-temperature-curvature (ATC) compensation circuit for reducing the temperature drift of the bandgap reference and achieves a good TC over a wide temperature range. The proposed technique employs addition and subtraction circuits to compensate any curvatures in different temperature ranges. The experimental results indicated that the proposed curvature-compensation technique improves the TC from 1.483 to 0.2 ppm/°C in the temperature range of −40 °C to 140 °C. The precision output voltage achieved a line regulation performance of 0.08%/V for input voltages between 1.3 and 1.8 V at a maximum quiescent current of 28 μA. The circuit operates at supply voltages down to 1.3 V and occupies 125×75 μm^2 in standard TSMC 0.18 μm 1P6M CMOS technology.

The remainder of this paper is organized as follows. Section II describes the principal operation of basic bandgap reference. Section III describes the proposed high-precision bandgap reference, which contains an existing sub-1 V bandgap reference and the proposed ATC compensation circuit. Section IV presents the experimental results, which confirm the effectiveness of the proposed ATC compensation circuits. The conclusions are provided in Section V.

II. Principal Operation of Basic Bandgap Reference

Most related studies [1]–[8], [10]–[14], [16]–[23] have used the well-established characteristics of BJTs to implement temperature-independent bandgap reference circuits.

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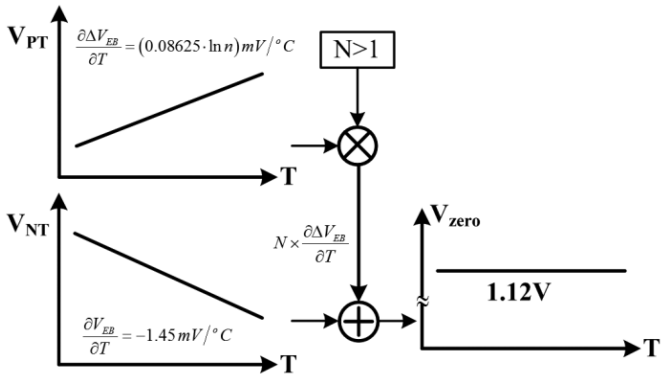

Fig. 1. Temperature dependence of an ideal zero-TC voltage.

The emitter–base voltage $V_{\rm EB}$ is generated from a p-n junction diode with a negative TC. For a BJT, the base–emitter voltage $V_{\rm EB}$ can be expressed as

$$V_{\rm EB} = V_T \ln \frac{I_C}{I_S} = \frac{kT}{q} \ln \frac{I_C}{I_S} \tag{1}$$

where $V_T = kT/q$ is the thermal voltage, T is the absolute temperature in Kelvin (K), and I_C is the collector current. The junction saturation current I_S is proportional to $\mu k T n_i^2$, where μ denotes the mobility of minority carriers and n_i is the intrinsic minority carrier concentration of silicon. The temperature dependence of these quantities is represented as $\mu \propto \mu_0 T^m$, where $m \approx -3/2$, and $n_i^2 \propto T^3 \exp(-Eg/kT)$, where $E_g \approx 1.12$ eV is the bandgap energy of silicon. However, the derivative of $V_{\rm EB}$ relative to T is provided in (3), where $\partial V_{\rm EB}/\partial T$ exhibits a negative TC of -1.45 mV/°C with $V_{\rm EB} = 750$ mV and $T = 300$ K.

The difference between the emitter–base voltages of the two BJTs can be written as $V_T \ln n$ by using unequal transistor sizes. Thus, the $\Delta V_{\rm EB}$ exhibits a positive TC that is equal to (3). With the nonlinear temperature characteristics of the emitter–base voltage obtained as stated previously, an ideal zero-TC voltage $V_{\rm ZERO}$ can be achieved by combining two opposite-TC voltages ($V_{\rm PT}$ and $V_{\rm NT}$) and an appropriate weight, as shown in Fig. 1. In an integrated implementation, TC is typically zero at one temperature and positive or negative at other temperatures as shown in Fig. 2. Two curvature types (convex and concave curves) of reference voltages were achieved and discussed by combining two opposite-TC currents at different temperature ranges in Section III

$$\frac{\partial V_{\rm EB}}{\partial T} = \frac{V_{\rm EB} - (4+m)V_T - E_g/q}{T} = -1.45 \text{ mV/°C} \tag{2}$$

$$\begin{aligned}\frac{\partial \Delta V_{\rm EB}}{\partial T} &= \frac{\partial (V_{\rm EB1} - V_{\rm EB2})}{\partial T} = \frac{\partial \left(V_T \ln \frac{I_C}{I_s} - V_T \ln \frac{I_C}{nI_s} \right)}{\partial T} \\ &= \frac{\partial (V_T \ln n)}{\partial T} = \frac{\partial \left(\frac{kT}{q} \ln n \right)}{\partial T} = \frac{k}{q} \ln n \\ &= (0.08625 \cdot \ln n) \text{ mV/°C}.\end{aligned} \tag{3}$$

III. Proposed High-Precision Bandgap Reference With ATC Compensation

In this paper, a novel bandgap reference with an ATC compensation circuit was designed to achieve an accurate temperature-independent voltage in a wide temperature range. Fig. 2 shows the operational concept of the proposed bandgap reference, which comprises a sub-1 V bandgap reference and an ATC compensation circuit. The nonlinear temperature characteristics of the base–emitter voltage play a crucial role in the bandgap reference. The combination of two opposite-TC currents usually presents two typical curves, a convex curve and a concave curve, as shown in Fig. 2. Relevant studies [7], [19]–[27] have the proposed curvature compensation techniques aimed at reducing the temperature drift of reference voltages with a convex curve. However, these techniques were not applied to reference voltages with a concave curve. The design concept of the ATC compensation circuit is to generate a fit temperature-compensated voltage for different curvature curves, as illustrated in Fig. 2. When a reference voltage with a convex curve is formed, the ATC compensation circuit provides a negative-TC current $I_{\rm NTC1}$ in a lower temperature range and a positive-TC current $I_{\rm PTC1}$ in a higher temperature range. By contrast, if a reference voltage with a concave curve is formed, the ATC compensation circuit provides a positive-TC current $I_{\rm PTC2}$ in a lower temperature range and a negative-TC current $I_{\rm NTC2}$ in a higher temperature range. To achieve this goal, the proposed ATC compensation circuit provides a positive-TC compensation voltage $V_{\rm PTC}$ and a negative-TC compensation voltage $V_{\rm NTC}$ to the bandgap reference voltage in any temperature range. These operations effectively reduce the temperature drift and obtain a good TC, as shown in Fig. 2. The temperature-compensated voltages $V_{\rm PTC}$ and $V_{\rm NTC}$ are realized using simple circuits without the temperature-dependence resistors. The detailed fundamentals and analysis of the proposed bandgap reference are described as follows.

A. Existing Sub-1 V Bandgap Reference

Existing sub-1 V bandgap reference circuits are presented in [10]–[27]. Fig. 3 shows a schematic of a sub-1 V bandgap reference [16] that utilizes two operational amplifiers, OP1 and OP2, to form a positive-TC current $I_{\rm PT}$ and a negative-TC current $I_{\rm NT}$, respectively, as provided in (4) and (5). OP1 and OP2 were designed using a two-stage op amp including differential pair amp and common-source amp

$$\begin{aligned}I_{\rm PT} &= \frac{V_{\rm EB1} - V_{\rm EB2}}{R_1} = \frac{\Delta V_{\rm EB}}{R_1} = \frac{V_T \ln n}{R_1} \\ &\because V_A = V_C; \quad n \text{ is the parallel numbers of BJTs}\end{aligned} \tag{4}$$

$$I_{\rm NT} = \frac{V_B}{R_2} = \frac{V_{\rm EB1}}{R_2}. \tag{5}$$

The two opposite-TC currents, $I_{\rm PT}$ and $I_{\rm NT}$, are then mirrored using the current ratio of M_1–M_5, summed to form a temperature-independent current $I_{\rm ref}$. Thus, a sub-1 V reference voltage $V_{\rm ref}$ is generated by adjusting the reference current $I_{\rm ref}$ and output resistance $R_{\rm out}$, as described in

$$I_{\rm ref} = A \times I_{\rm PT} + B \times I_{\rm NT} \tag{6}$$

$$V_{\rm ref} = I_{\rm ref} \cdot R_{\rm out} = \left(\frac{A \cdot V_T \ln n}{R_1} + \frac{B \cdot V_{\rm EB1}}{R_2} \right) \cdot R_{\rm out}. \tag{7}$$

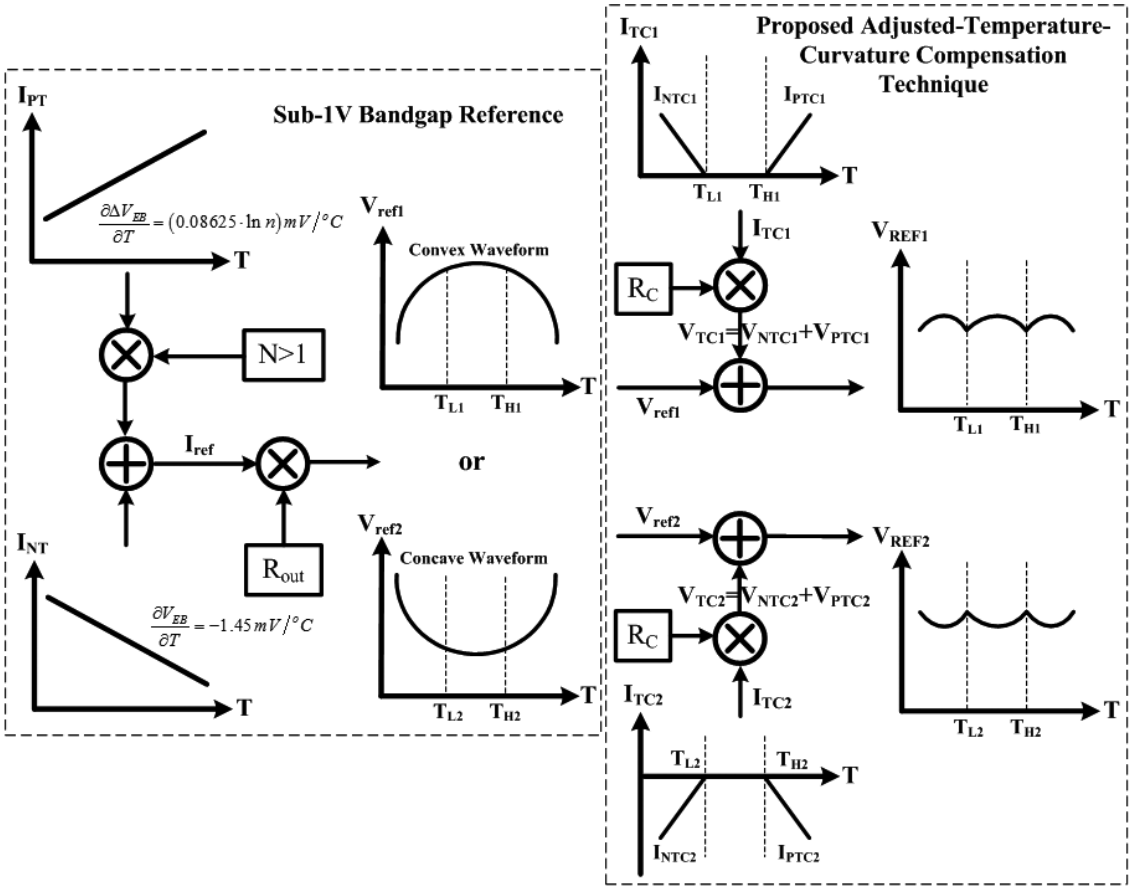

Fig. 2. Operational concept of the proposed ATC compensation technique.

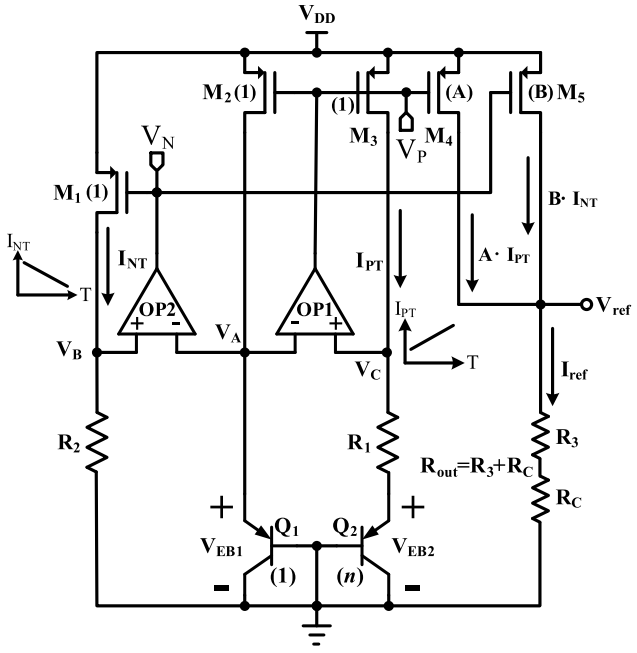

Fig. 3. Sub-1 V bandgap reference [16].

B. Proposed ATC Compensation Circuit for Reference Voltage With a Convex Curve

As mentioned previously, the proposed bandgap reference comprises a sub-1 V bandgap reference [16] and an ATC compensation circuit. Fig. 4 shows the postlayout simulation results of the reference voltage with a convex curve. The variations of two opposite-TC currents were carefully investigated in different temperature ranges containing the lower temperature range T_{LT1}, middle temperature range T_{MT1}, and higher temperature range T_{HT1} and are discussed as follows. Fig. 4(a) and (b) shows the positive-TC current I_{PT1} and the negative-TC current I_{NT1}, respectively. We identified slight variations in the temperature slopes in the three temperature ranges. First, the temperature slope 35.33 nA/°C of I_{PT1} was larger than the temperature slope −35.11 nA/°C of I_{NT1} in the lower temperature range (−40 °C–5 °C). Two opposite-TC currents, I_{PT1} and I_{NT1}, were then added to form a positive TC of 5.04 ppm/°C between −40 °C and 5 °C, as shown in Fig. 4(c). Furthermore, because the temperature slope 34.989 nA/°C of I_{PT1} approximated the −34.984 nA/°C of I_{NT1}, the obtained V_{ref} displayed a low voltage variation of 0.051 mV in T_{MT1}. The higher temperature range (70 °C–140 °C) presented a negative TC (−2.42 ppm/°C) because of the combination of I_{PT1} and I_{NT1}. Consequently, a reference voltage V_{ref} with a convex curve was determined according to the previous discussion on the temperature slope. The design details of the sub-1 V bandgap reference are provided in Table I.

Fig. 5 shows that the proposed ATC compensation circuit uses a current subtraction circuit (M_6–M_{11}) and current mirrors (M_{12}–M_{15}) to reduce the temperature drift across the

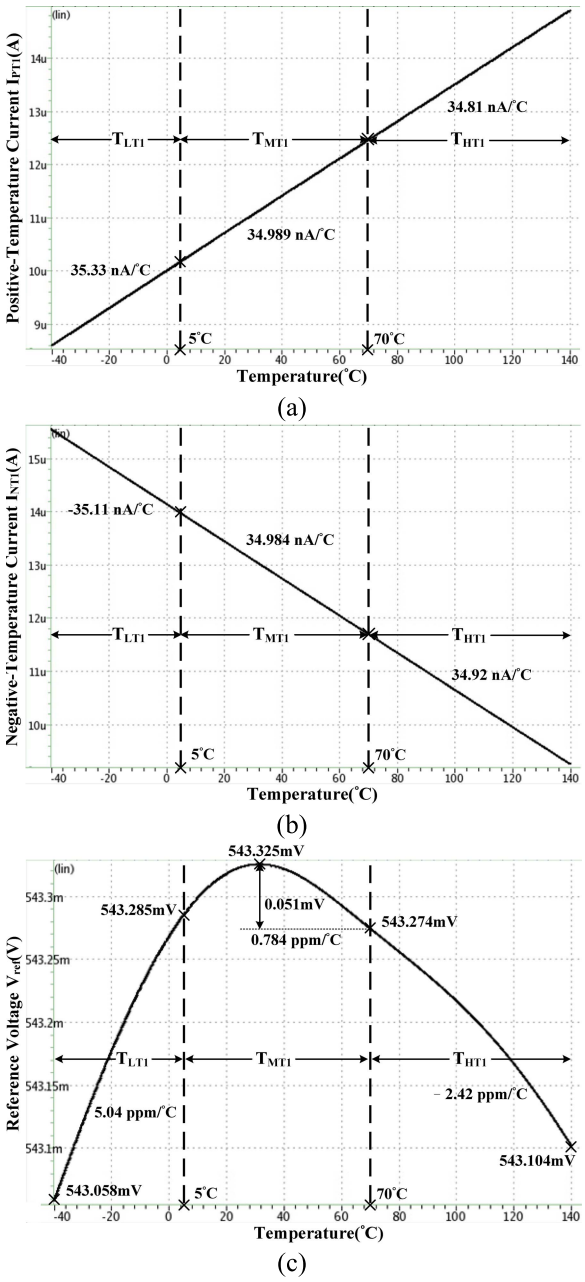

Fig. 4. Postlayout simulation results of (a) positive-TC current I_{PT1}, (b) negative-TC current I_{NT1}, and (c) reference voltage V_{ref} with a convex curve.

entire temperature range. The competitive currents $A_1 I_{PT1}$ and $A_2 I_{NT1}$ are obtained using the aspect ratio of the current mirror (M_1, M_3, M_{12}, and M_{13}). When the positive-TC current $A_1 I_{PT1}$ is larger than the negative-TC current $A_2 I_{NT1}$ between 5 °C and 140 °C, transistors M_8 and M_{LT} are OFF and no current flows into transistor M_{LT}, as shown in Fig. 6(a). However, when the current $A_1 I_{PT1}$ is smaller than the current $A_2 I_{NT1}$, transistors M_8 and M_{LT} are turned ON and the negative-TC compensation current $A_3 I_{NTC1}$ flows into resistor R_C. Therefore, the negative-TC compensation voltage V_{NTC1} is obtained to reduce the voltage variation from 0.227 to 0.026 mV, as shown in Fig. 6(c). The compensated range T_{LT1} can be shifted by scaling the ratio of the coefficients A_1 and A_2.

TABLE I

TRANSISTOR SIZES AND RESISTANCE VALUES OF THE SUB-1 V BANDGAP REFERENCE

	Convex Curve	Concave Curve
M_1 and M_5	W=8μm, L=8μm	W=2μm, L=2μm
M_2, M_3 and M_4	W=2μm, L=2μm	W=2μm, L=2μm
R_1	5kΩ	5kΩ
R_2	53.65 kΩ	53.65 kΩ
R_{out}	22.5 kΩ	22.5 kΩ
Q_1 (PNP BJT, Emitter Area)	1×(10μm×10μm)	1×(10μm×10μm)
Q_2 (PNP BJT, Emitter Area)	8×(10μm×10μm)	8×(10μm×10μm)

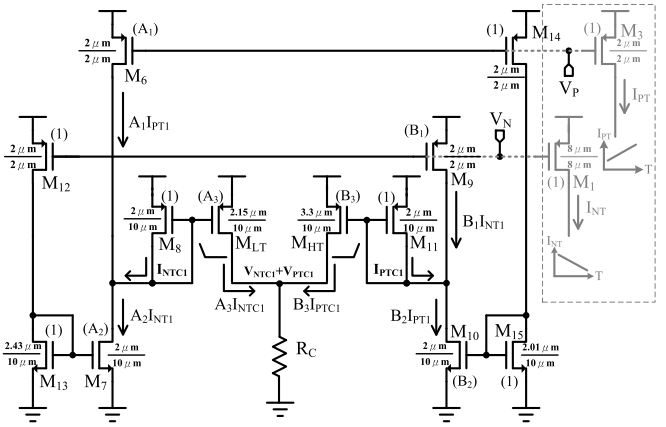

Fig. 5. Proposed ATC compensation circuit for the reference voltage with a convex curve.

The magnitude of the compensation voltage V_{NTC1} can be scaled using the ratio A_3 and resistor R_C. The proposed reference voltage V_{ref1} with the compensation voltage V_{NTC1} in T_{LT1} is provided in (8). The resistor R_C is one part of R_{out} as shown in Fig. 3

$$\begin{aligned} V_{ref1} &= I_{ref} \cdot R_{out} + A_3(A_2 \cdot I_{NT1} - A_1 \cdot I_{PT1})R_C \\ &= I_{ref} \cdot R_{out} + A_3 \cdot I_{NTC1} \cdot R_C \\ &= V_{ref} + V_{NTC1}. \end{aligned} \tag{8}$$

In the higher temperature range (70 °C–140 °C), the reference voltage V_{ref} is a negative-TC voltage, as shown in Fig. 4(c). The proposed circuit (M_9–M_{11}, M_{14}–M_{15}, and M_{HT}) generates a positive-TC voltage V_{PTC1} to correct the reference voltage V_{ref}. The current $B_1 \cdot I_{NT1}$ and $B_2 \cdot I_{PT1}$ are mirrored from the transistors (M_1, M_3, M_{14}, and M_{15}). When the positive-TC current $B_2 \cdot I_{PT1}$ is lower than the negative-TC current $B_1 \cdot I_{NT1}$, the transistors M_{11} and M_{HT} are turned OFF. Conversely, when the current $B_2 \cdot I_{PT1}$ is larger than the current $B_1 \cdot I_{NT1}$, the transistors M_{11} and M_{HT} are turned ON and the positive-TC compensation current $B_3 \cdot I_{PTC1}$ flows into resistor R_C in T_{HT1}. Thus, the voltage variation of the reference voltage V_{ref} is markedly improved from 0.17 to 0.036 mV by adding the positive-TC compensation voltage V_{PTC1}, as shown in Fig. 6(c). The compensated range T_{HT1} and magnitude of the compensation voltage V_{PTC1} can be controlled by adjusting the ratios of the B_1, B_2, and B_3 depending on the temperature

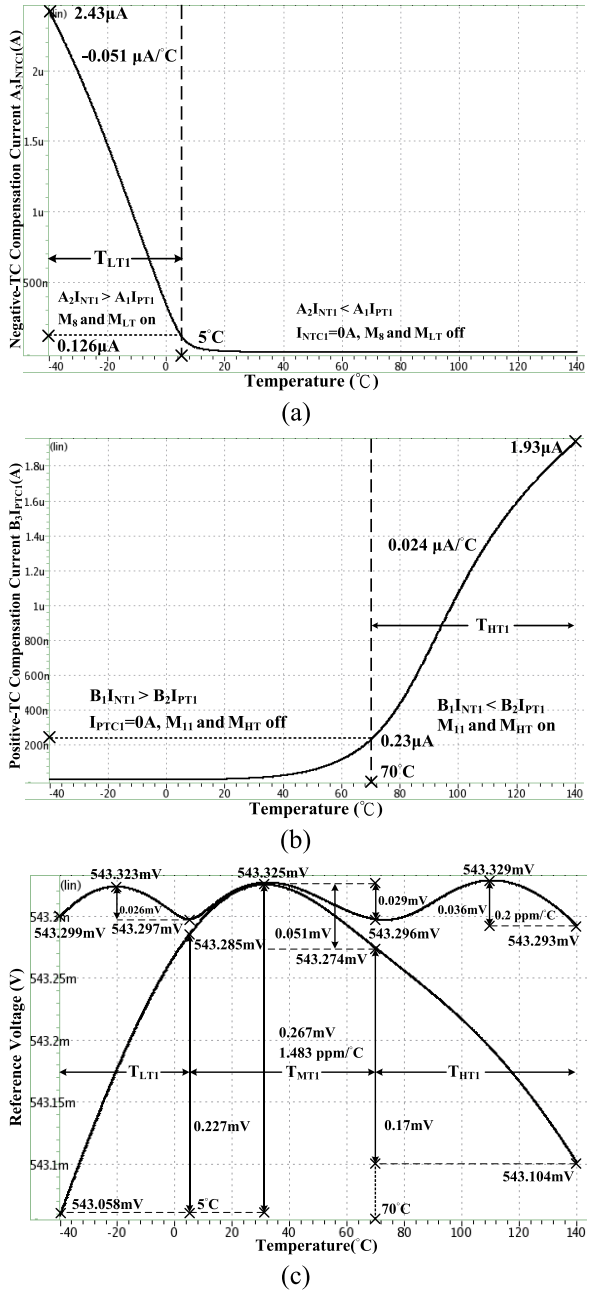

Fig. 6. Postlayout simulation results of (a) negative-TC compensation current A_3I_{NTC1}, (b) positive-TC compensation current B_3I_{PTC1}, and (c) reference voltage.

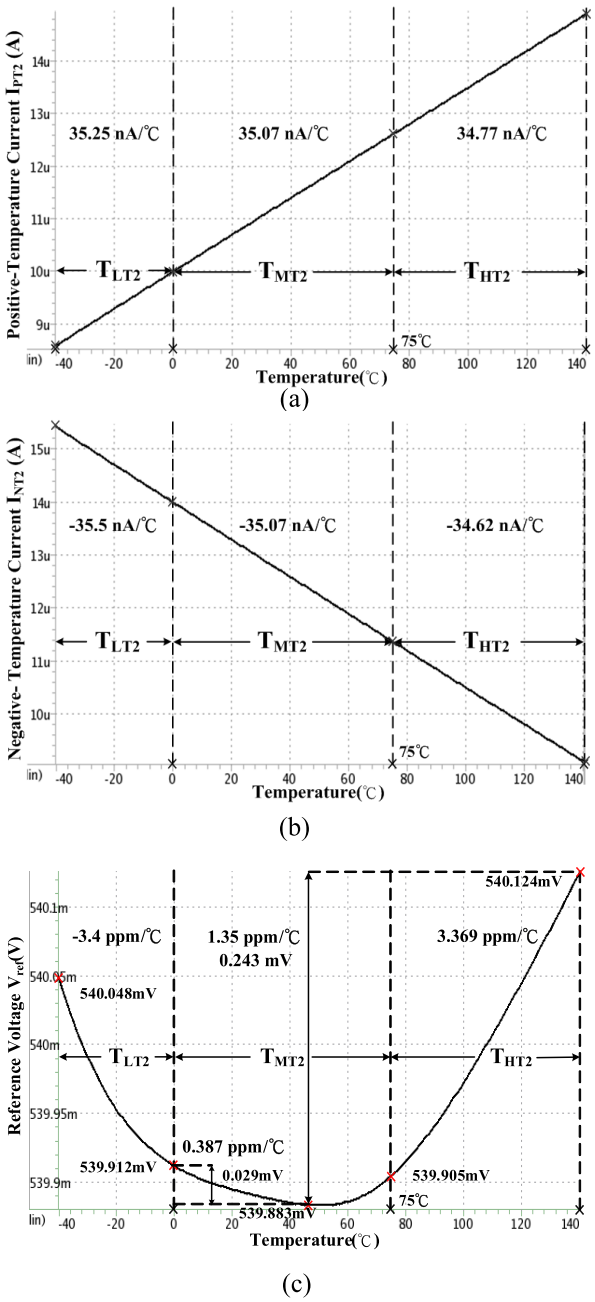

Fig. 7. Postlayout simulation results of (a) positive-TC current I_{PT2}, (b) negative-TC current I_{NT2}, and (c) reference voltage V_{ref} with a concave curve.

conditions. In T_{HT1}, the reference voltage is represented in (9). Furthermore, because of the low-voltage variation of 0.051 mV in the middle temperature range (5 °C–70 °C), as shown in Fig. 4(c), this range does not require any compensation, and the transistors M_8, M_{11}, M_{LT}, and M_{HT} are turned OFF. The output reference voltage within the middle temperature range is equal to (7). Fig. 6(c) shows the postlayout simulation results of the proposed bandgap reference, which obtained a TC of 0.2 ppm/°C. A low reference voltage variation of 0.036 mV was achieved over a 180 °C temperature range

$$\begin{aligned} V_{\text{ref1}} &= I_{\text{ref}} \cdot R_{\text{out}} + B_3(B_2 \cdot I_{\text{PT1}} - B_1 \cdot I_{\text{NT1}})R_C \\ &= I_{\text{ref}} \cdot R_{\text{out}} + B_3 \cdot I_{\text{PTC1}} \cdot R_C \\ &= V_{\text{ref}} + V_{\text{PTC1}}. \end{aligned} \tag{9}$$

C. Proposed ATC Compensation Circuit for Reference Voltage With a Concave Curve

According to the previously mentioned observation, the slope of the TC currents varies at different temperature ranges. Furthermore, operation currents of MOS transistors vary slightly with temperature. The convex curve or concave curve of the reference voltage was achieved according the designed sizes of the current mirror (M_1–M_5) in the sub-1 V bandgap reference [16]. The curvature of the reference voltage was changed from convex curve to concave curve when the W/L sizes of the transistors M_1 and M_5 were designed from 8/8 μm to 2/2 μm. Other circuits such as transistors (M_2–M_4), operational amplifiers (OP1 and OP2), BJTs (Q_1 and Q_2), and

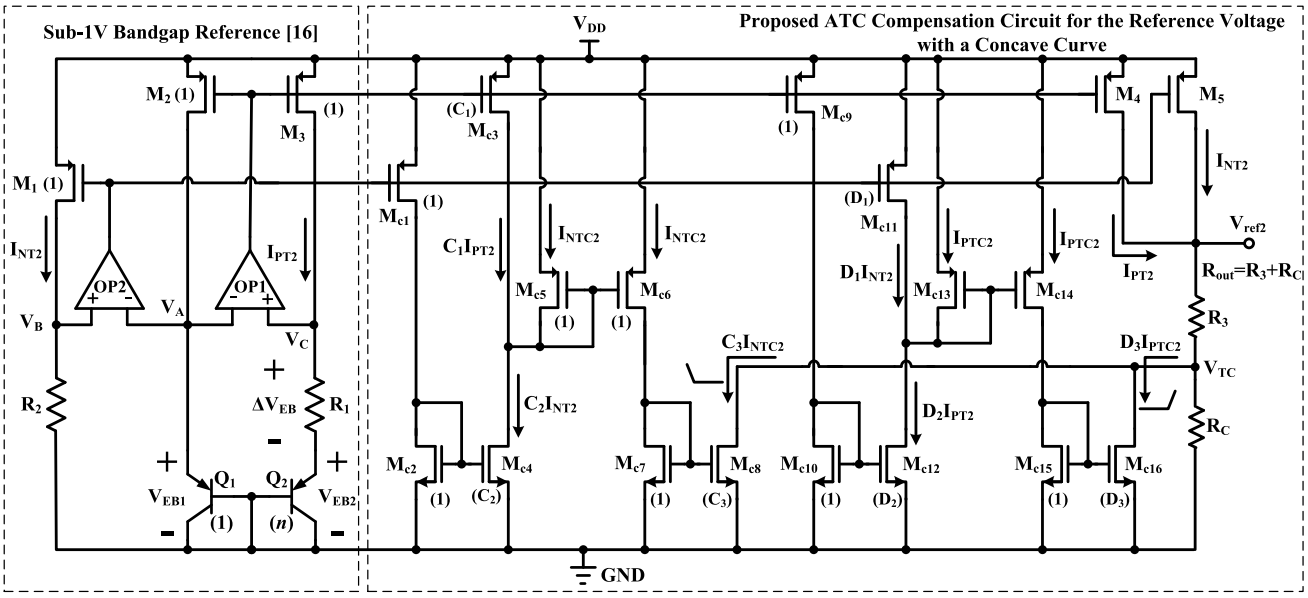

Fig. 8. Proposed bandgap reference circuit.

resistors (R_1 and R_2) kept the same designs. Table I presents the transistor sizes and resistance values of the reference voltage with concave curve. The operation of reference voltage with a concave curve is subsequently discussed by using the simulations of two opposite-TC currents as shown in Fig. 7. Because the slope −35.5 nA/°C of the negative-TC current I_{NT2} is larger than the slope 35.25 nA/°C of the positive-TC current I_{PT2}, a negative TC of −3.4 ppm/°C is achieved in the lower temperature range (−40 °C to 0 °C). The middle temperature range (0 °C–75 °C) indicates that a low voltage variation of 0.029 mV is due to the combination of two approximate temperature slopes. The third temperature range (75 °C–140 °C) achieves a positive TC of 3.369 ppm/°C because the slope −34.62 nA/°C of the negative-TC current I_{NT2} is lower than the slope 34.77 nA/°C of the positive-TC current I_{PT2}, as shown in Fig. 7. Thus, a 1.35 ppm/°C reference voltage with a concave curve can be achieved through combining the currents of the three temperature ranges.

In this paper, the proposed ATC compensation circuit (M_{c1}–M_{c16}) generates two opposite piecewise linear currents in T_{LT2} and T_{HT2} shown in Fig. 8. The currents $C_1 \cdot I_{\mathrm{PT2}}$ and $C_2 \cdot I_{\mathrm{NT2}}$ are generated using current mirrors (M_1–M_3 and M_{c1}–M_{c4}). When $C_2 \cdot I_{\mathrm{NT2}} > C_1 \cdot I_{\mathrm{PT2}}$, the transistors ($M_{c5}$–$M_{c8}$) are turned ON and a negative-TC compensation current I_{NTC2} is formed. The negative-TC compensation current $C_3 \cdot I_{\mathrm{NTC2}}$ is drained by the transistor M_{c8} from the output terminal V_{TC}. This operation is similar to a positive-TC compensation current added to the output to correct the negative-TC voltage of the reference voltage in T_{LT2}, as shown in Fig. 9. The compensated range T_{LT2} can be accurately determined by adjusting the ratios of C_1 and C_2 for different temperature curves. The proposed reference voltage can be obtained in (10) in T_{LT2}. The second term introduced in (10) effectively reduces the voltage variation from 0.145 to 0.021 mV, as shown in Fig. 9(c)

$$\begin{aligned} V_{\mathrm{ref2}} &= (I_{\mathrm{PT2}} + I_{\mathrm{NT2}}) \cdot (R_3 + R_C) - C_3 \\ &\quad \cdot (C_2 \cdot I_{\mathrm{NT2}} - C_1 \cdot I_{\mathrm{PT2}}) R_C \\ &= (I_{\mathrm{PT2}} + I_{\mathrm{NT2}}) \cdot R_{\mathrm{out}} - C_3 \cdot I_{\mathrm{NTC2}} \cdot R_C \\ &= V_{\mathrm{ref}} - V_{\mathrm{NTC2}}. \end{aligned} \tag{10}$$

In T_{HT2}, the curve of the reference voltage is a positive TC of 3.507 ppm/°C. The positive-TC compensation current $D_3 \cdot I_{\mathrm{PTC2}}$ is generated by the difference of the positive-TC current $D_2 \cdot I_{\mathrm{PT2}}$ and the negative-TC current $D_1 \cdot I_{\mathrm{NT2}}$, and multiplied by the size ratio D_3, as shown in Fig. 8. The transistor M_{c16} drains the positive-TC compensation current $D_3 \cdot I_{\mathrm{PTC2}}$ from the divider resistor R_C to reduce the temperature drift in T_{HT2}. The compensated range can be controlled by adjusting the ratios of D_1 and D_2 for different temperature conditions. The reference voltage V_{ref2} in T_{HT2} is provided in (11). The proposed compensation voltage V_{PTC2} is equal to $D_3 \cdot I_{\mathrm{PTC2}}$, multiplied by R_C, and its magnitude can be increased or reduced by adjusting the ratio D_3

$$\begin{aligned} V_{\mathrm{ref2}} &= (I_{\mathrm{PT2}} + I_{\mathrm{NT2}}) \cdot (R_3 + R_C) - D_3 \\ &\quad \cdot (D_2 \cdot I_{\mathrm{PT2}} - D_1 \cdot I_{\mathrm{NT2}}) R_C \\ &= (I_{\mathrm{PT2}} + I_{\mathrm{NT2}}) \cdot R_{\mathrm{out}} - D_3 \cdot I_{\mathrm{PTC2}} \cdot R_C \\ &= V_{\mathrm{ref}} - V_{\mathrm{PTC2}}. \end{aligned} \tag{11}$$

Because a low-voltage variation of 0.022 mV is achieved in T_{MT2}, as shown in Fig. 7(c), the proposed ATC compensation circuit does not generate any current or voltage to the output reference voltage, and the transistors (M_{c5}–M_{c8} and M_{c13}–M_{c16}) are turned OFF. The proposed reference voltage is equal to (7) in T_{MT2}. Fig. 9(c) shows the simulated reference voltage of the bandgap circuit as a function of temperature with and without the proposed ATC compensation circuit. The TC of the proposed circuit exhibits a 90.9% improvement, from 1.35 to 0.122 ppm/°C. The variation

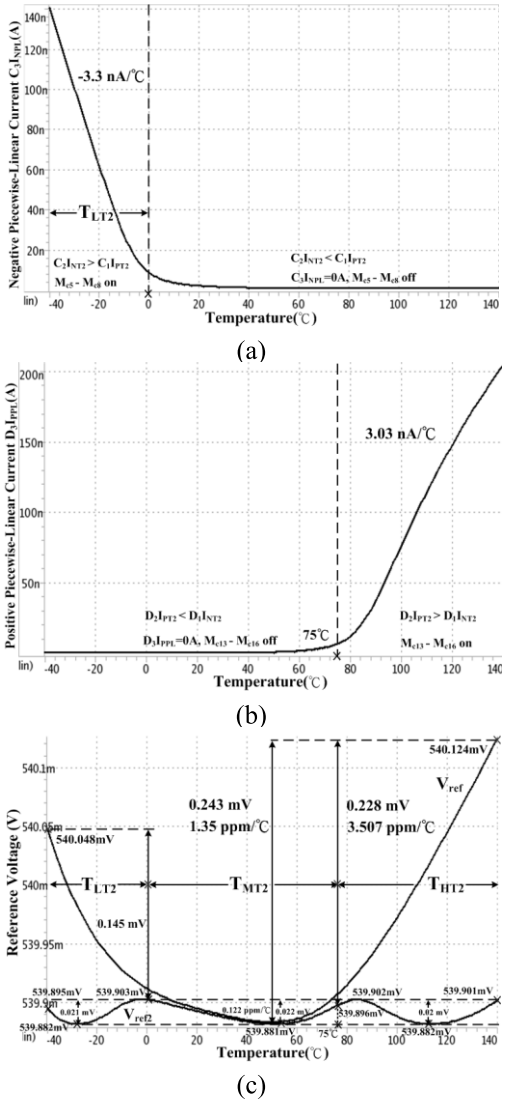

Fig. 9. Postlayout simulation results of (a) negative-TC compensation current $C_3 \cdot I_{NTC2}$, (b) positive-TC compensation current $D_3 \cdot I_{PTC2}$, and (c) reference voltage.

of the proposed reference voltage is 0.022 mV (539.881–539.903 mV) over a 180 °C temperature range. However, this paper conducted Monte Carlo simulations to determine the influence of process and mismatch variations on the proposed bandgap reference circuit. One-hundred iterations of the generated reference voltage are shown in Fig. 10. The simulation results show that the reference voltage varied from 539.945 to 539.626 mV under a worst case scenario.

IV. Experimental and Comparison Results

The proposed bandgap reference with the ATC compensation circuit was fabricated using TSMC 0.18 μm 1P6M CMOS technology. The physical micrograph of the proposed bandgap reference chip is illustrated in Fig. 11. The active chip area is 125×75 μm^2. The TC of the proposed circuit was measured using a programmable temperature chamber. Fig. 12 shows the distribution of the output voltage for eight samples that were measured from −40 °C to 140 °C with

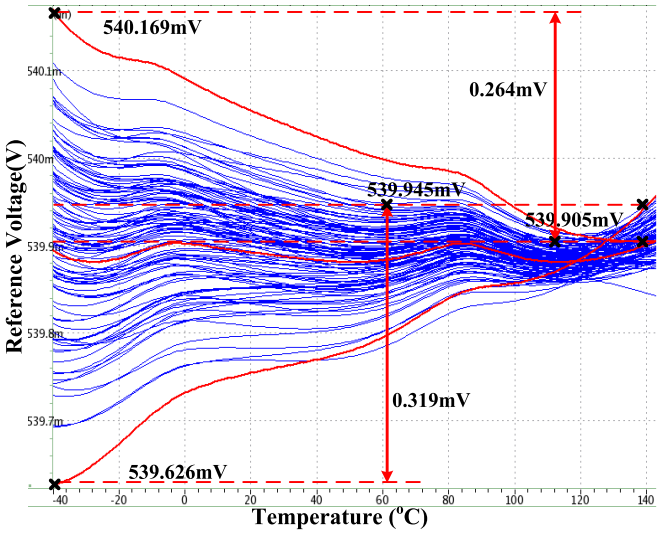

Fig. 10. Monte Carlo simulation result of the proposed bandgap reference circuit.

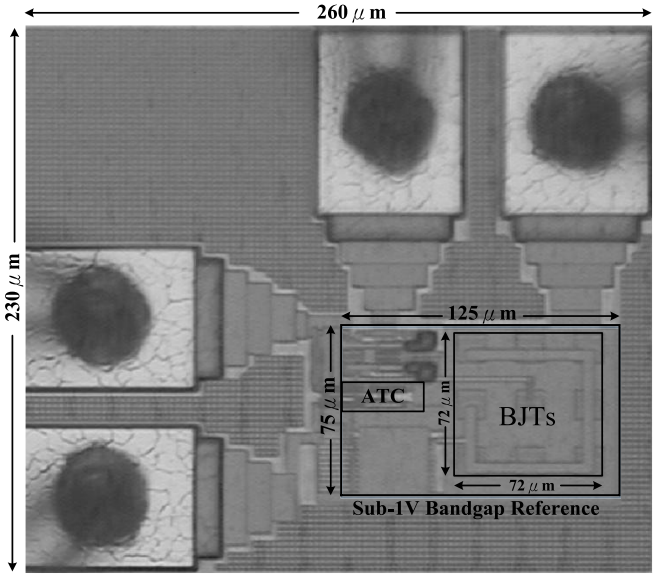

Fig. 11. Physical micrograph of the proposed bandgap reference chip.

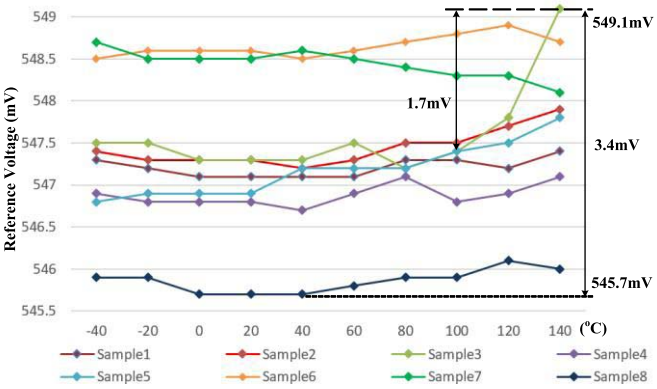

Fig. 12. Measured temperature characteristics of the proposed bandgap reference.

a 1.8 V supply voltage. The proposed bandgap reference continuously operated for 10 min at every set temperature point from −40 °C to 140 °C in increments of 20 °C. In the

TABLE II
COMPARISONS OF THE PROPOSED LOW-VOLTAGE BANDGAP REFERENCE

Specifications	2012 [22] IEEE JSSC	2013 [23] IEEE JSSC	2014 [24] IEEE CASI	2015 [25] IEEE CASI	2015 [26] IEEE CASI	This work 2016
Supply Voltage(V)	2.5	0.7-1.8	1.2	1.15	1.2	1.3-1.8
Current Consumption(μA)	38	52.5	36	0.58	120	28
Reference Voltage(mV)	617.7	548	767	720	735	547
Best TC(ppm/°C)	3.9	114	3.4	10.1	4.2	1.67
Temp Range(°C)	-15 to 150	-40 to 120	-40 to 120	10 to 80	-40 to 120	-40 to 140
Line Regulation(%/V)	0.039	N/A	0.054	0.3	N/A	0.08
Active Area(mm^2)	0.102	0.0246	0.036	0.028	0.063	0.0094
Trimming	Yes	No	Yes	No	No	NO
Technology	CMOS 0.35μm	CMOS 0.18μm	CMOS 0.18μm	CMOS 90nm	CMOS 0.13μm	CMOS 0.18μm

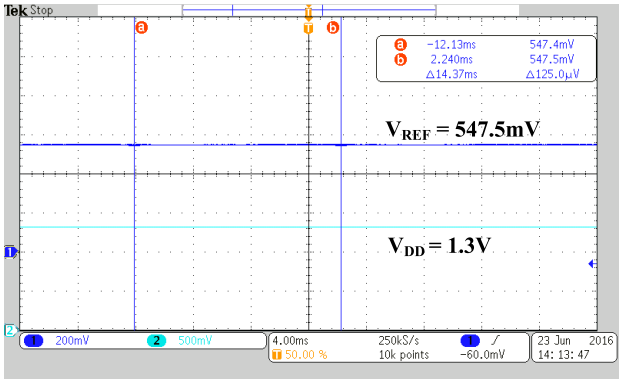

Fig. 13. Measured output voltage at different supply voltages. (a) $V_{DD} = 1.3$ V. (b) $V_{DD} = 1.8$ V.

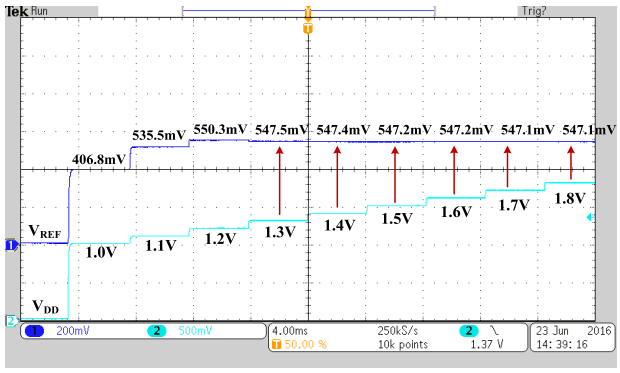

Fig. 14. Measured output voltage at each step voltage from 1 to 1.8 V.

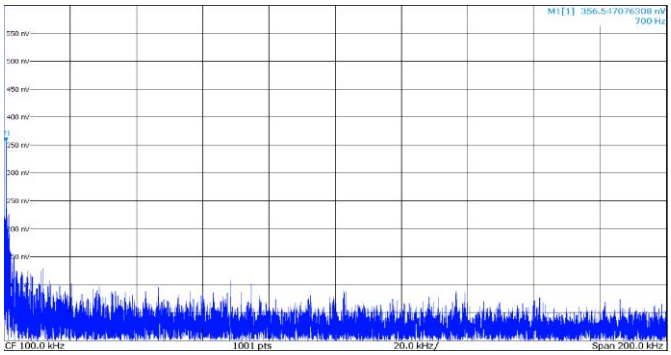

Fig. 15. Measured noise spectrum of the proposed bandgap reference at room temperature.

experimental results, the measured TCs of eight samples varied between 1.67 to 10.55 ppm/°C over the temperature range −40 °C to 140 °C. The worst TC of 10.55 ppm/°C was achieved in Sample 3 because of a large voltage variation of 1.7 mV between 100 °C and 140 °C. The maximum voltage variation of the measured temperature dependence was less than 3.4 mV among the eight samples, as shown in Fig. 12. The proposed circuit does not use any trimming resistors or transistor switches for avoiding an area increase in the proposed chip.

The measured output voltage as a function of the used supply voltage was obtained using a programmable voltage source and oscilloscope. Fig. 13 shows the measured output voltage at different supply voltages ($V_{DD} = 1.3$ and 1.8 V) at 27 °C. The experimental results indicate that a constant voltage of 547 mV with slight variation was achieved, as shown in Fig. 13. Furthermore, the output voltage of the proposed bandgap reference was also measured at each step voltage by applying a staircase sweep voltage ranging from 1 to 1.8 V, as shown in Fig. 14. The output reference voltage generated a 0.4 mV variation under a 0.5 V supply voltage variation. These results show that the line regulation of the proposed bandgap reference was lower than 0.08%/V from 1.3 to 1.8 V. Table II compares the performance of the bandgap reference described in this paper to that of previous low-voltage CMOS bandgap references [22]–[26]. A reported study [22] achieved

the optimal line regulation performance. The circuit proposed in this paper consumed only 28 μA, which is an improvement upon previous designs [22]–[26] that operate at a similar supply voltage. Fig. 15 shows the measured noise spectrum of the output voltage V_{REF} without a capacitor between 1 Hz and 200 kHz. The measured result shows that the highest noise 356.5 nV is at 700 Hz by using the signal and spectrum analyzer (R&S FSW8).

V. Conclusion

This paper presents a precision bandgap reference fabricated with a standard CMOS 0.18 μm process. The experimental bandgap reference verifies that using the proposed ATC compensation circuit provides an accurate reference voltage and good TC over a wide temperature range. The designed positive-TC compensation current and negative-TC compensation current can accurately correct the temperature drift of different curvatures as convex and concave curves. The best TC of the proposed bandgap reference is 1.67 ppm/°C at a temperature range of −40 °C to 140 °C with a 1.8 V supply voltage. This result is an improvement on currently available low-voltage bandgap references. The measured output voltage is 547 mV from a 1.3–1.8 V supply voltage at 27 °C. The proposed circuit generates 547 mV at a minimum power supply voltage of 1.3 V; therefore, it achieves effective line regulation. The maximum power consumption is 28 μA with a 1.8 V supply voltage. The active area is 0.0094 mm^2. These results display an enhancement in the performance of the voltage regulator and an effective increase in the voltage resolutions of A/D converters.

Acknowledgment

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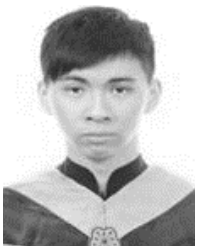

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