Symposium on VLSI Circuits
Short Course 2

Migrating Analog/Mixed-Signal (AMS) Designs to FinFET

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Qualcomm Technologies, Inc.

Migrating Mobile SoC to 14nm FinFET

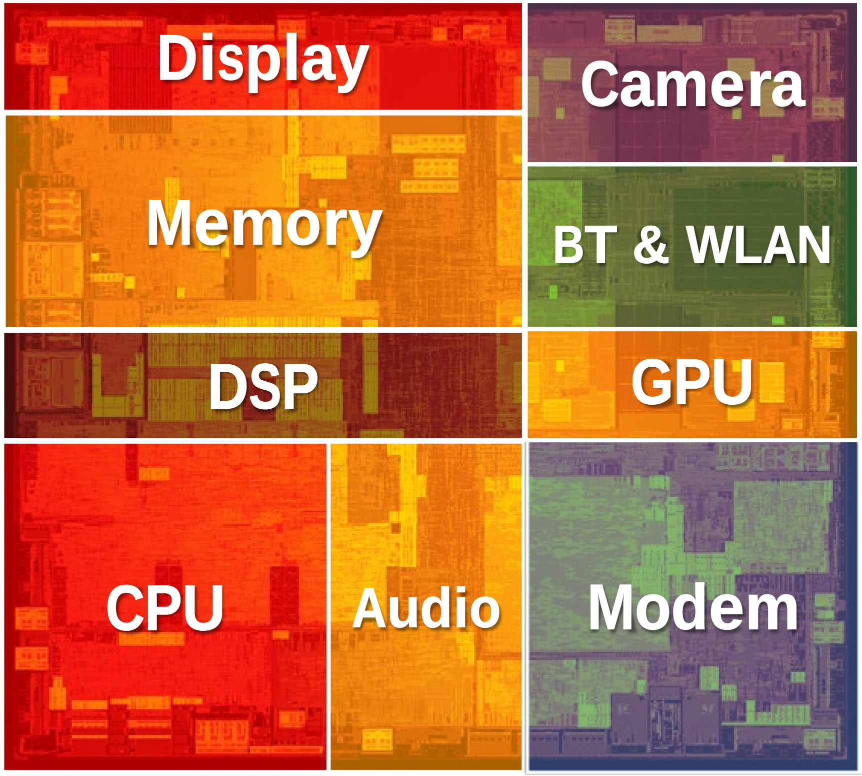
Snapdragon™ 820

- Qualcomm Technologies’ first 14nm product

AMS content

- PLLs & DLLs
- Wireline I/Os
- Data converters
- Bandgap references
- Thermal sensors
- Regulators
- ESD protection

Not drawn to scale

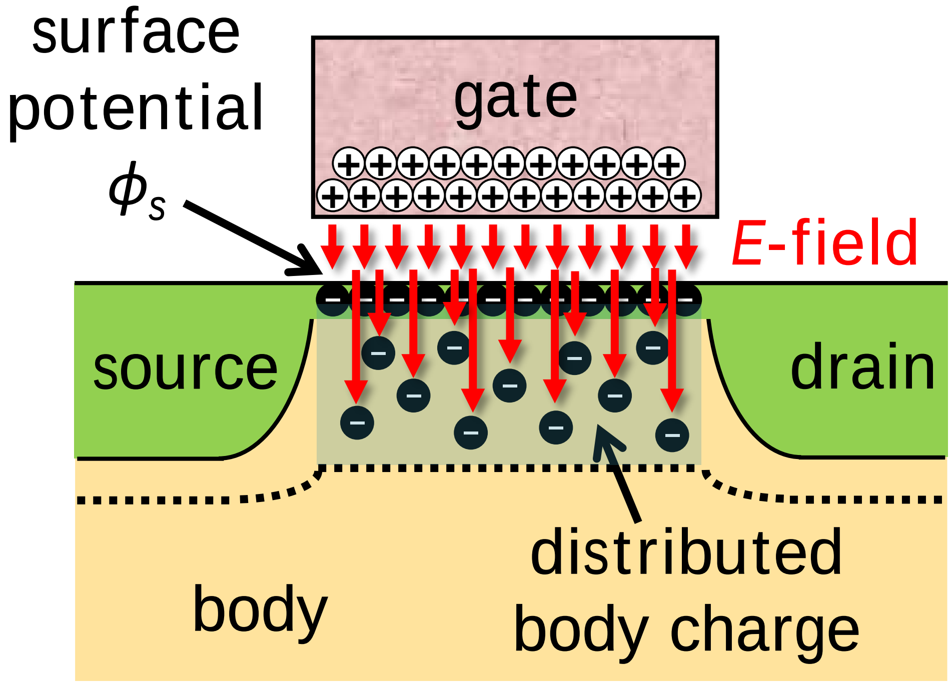


Terzioglu, Qualcomm [1]

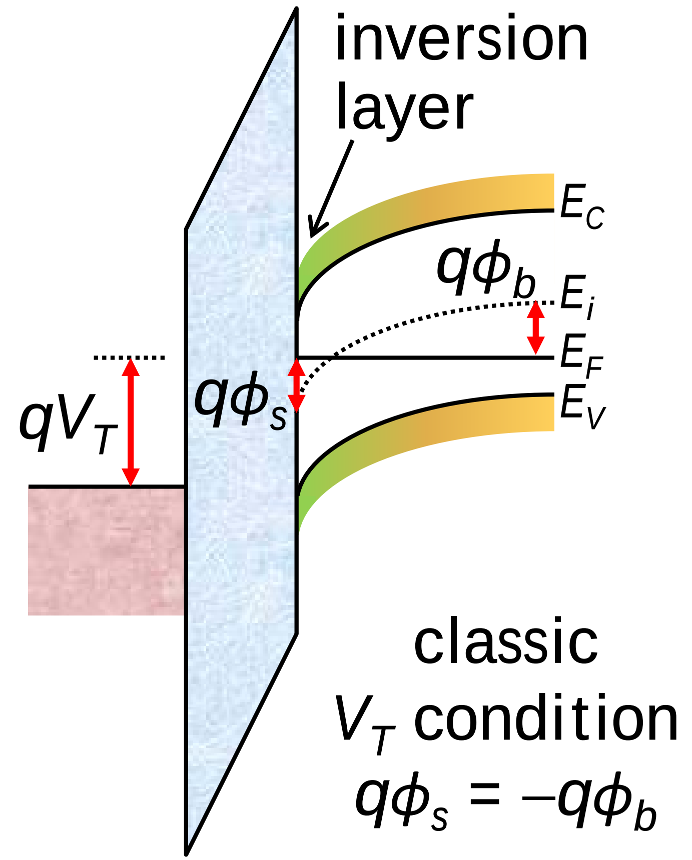
Outline

- MOSFET, Fully-Depleted & FinFET Basics
- Technology Considerations
- Analog/Mixed-Signal Design Considerations
- Conclusion

Basic MOSFET Operation

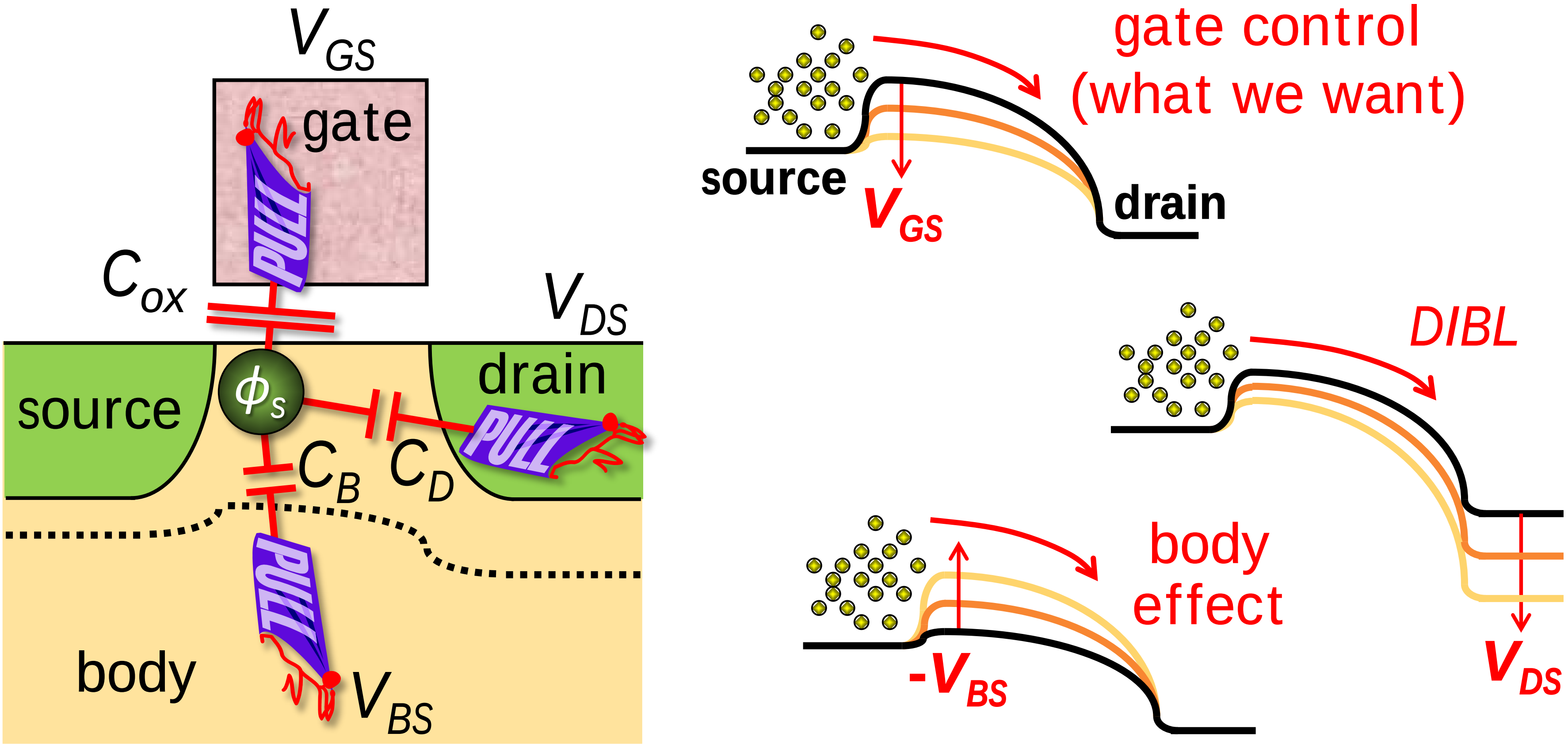


$$V_T = V_{FB} + 2\phi_b + \frac{Q_{dep}}{C_{ox}}$$



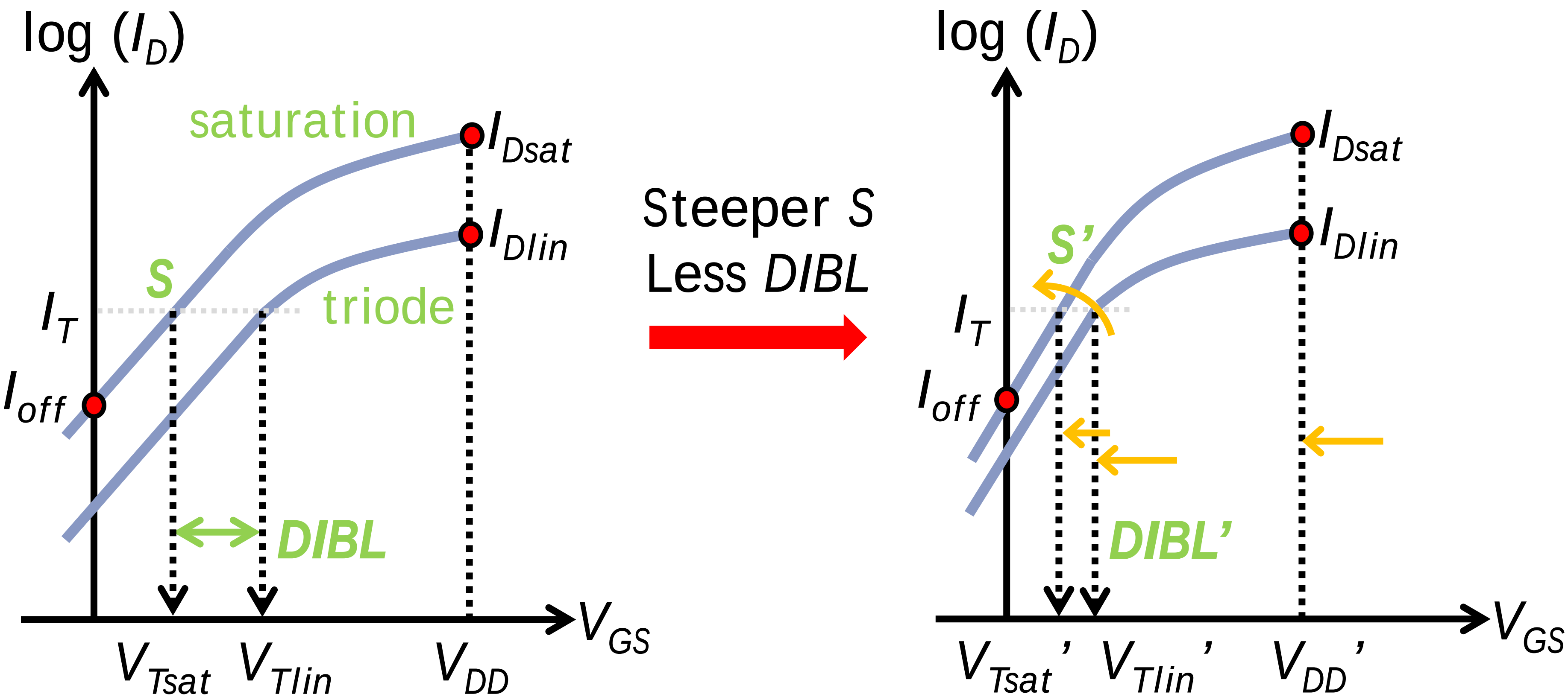
- Gate/body charge $\xrightarrow{\int}$ E-field $\xrightarrow{\int}$ energy band bending
- V_{GS} modulates surface conductivity to induce S/D short

Subthreshold Fight for Body Charge



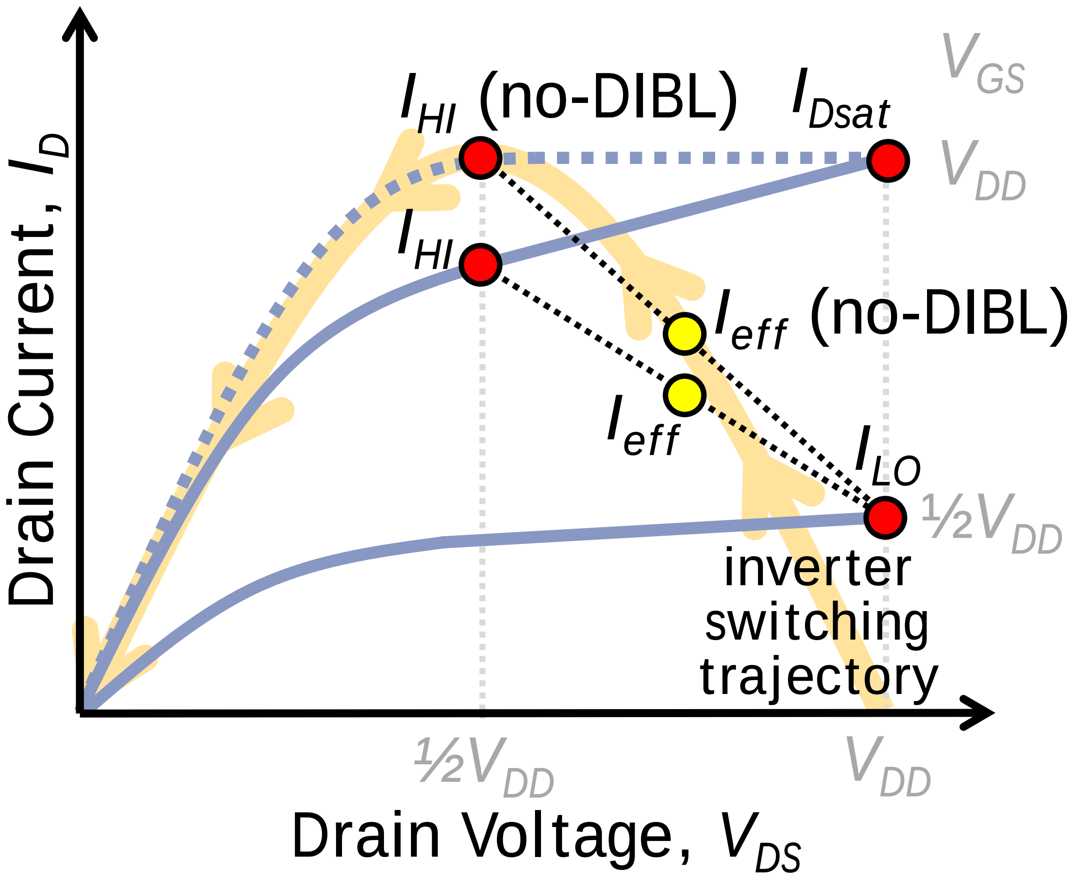
- Capacitor divider dictates source-barrier ϕ_s & I_D
- C_B, C_D << C_{ox} → weak body effect, weak *DIBL*, high I_{on}/I_{off}

Less Drain/Body Coupling, Lower Supply



- Steeper subthreshold swing S (ideally 60mV/decade @ 300K)
- Lower V_{DD}, lower power for same I_{off} & I_{Dsat}
- Fully-depleted finFET enables steeper S & less *DIBL*

Less DIBL → Stronger FET for Digital



$$I_{eff} = \frac{I_{LO} + I_{HI}}{2}$$

I_{LO} @ V_{GS}=½V_{DD}, V_{DS}=V_{DD}

I_{HI} @ V_{GS}=V_{DD}, V_{DS}=½V_{DD}

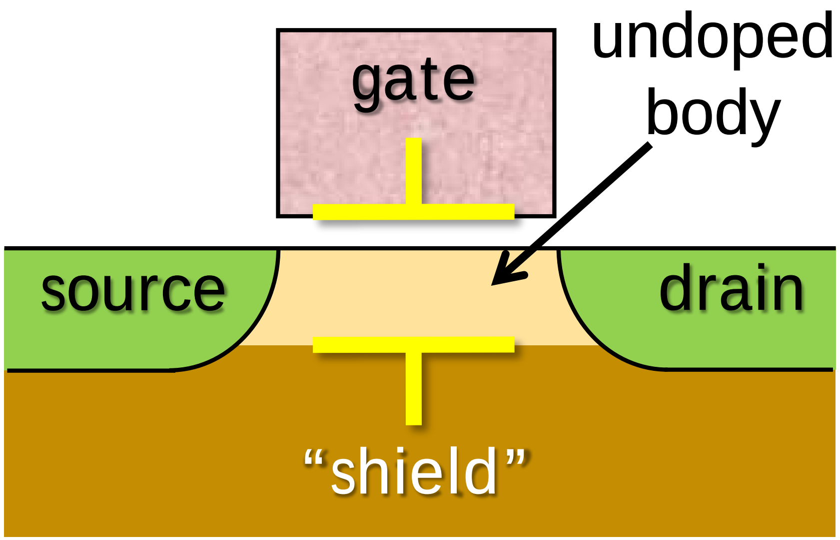
I_{eff} is better than I_{Dsat} for estimating inverter CV/I switching delay

Less DIBL → higher I_{eff} & r_{out} for same I_{Dsat}

Na *et al*., IBM [2]
Wei *et al*., Stanford [3]

Concept of Fully-Depleted

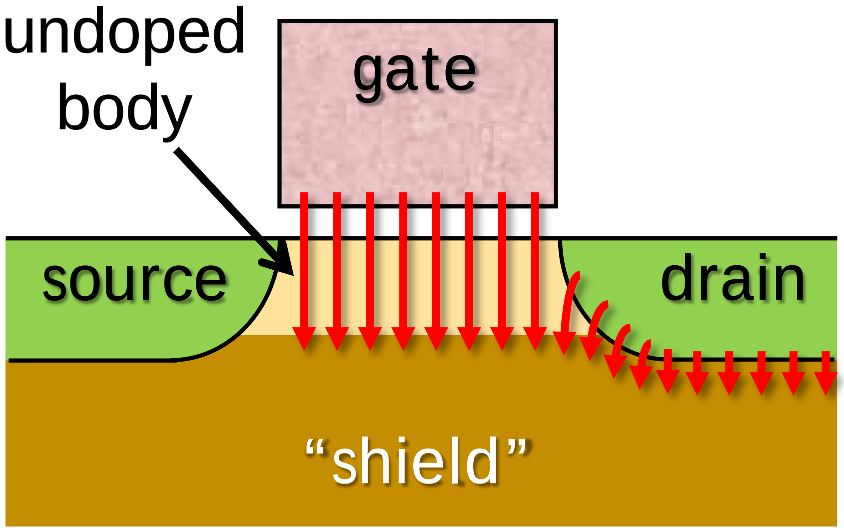
- Dopants *not* fundamental to field-effect action, just provide mirror charge to set up *E*-field to induce surface inversion
- Remove body dopants & insert heavily-doped conductive "shield" beneath undoped body to provide mirror charge (extreme retrograded-well)
- Body becomes *fully-depleted* as it has no charge to offer
- Implementations
  - Planar on bulk
  - Planar on SOI (FD-SOI)
  - 3-D (e.g., finFET) on bulk
  - 3-D on SOI



Yan *et al*., Bell Labs [4]
Fujita *et al*., Fujitsu [5]
Cheng *et al*., IBM [6]

Fully-Depleted Considerations

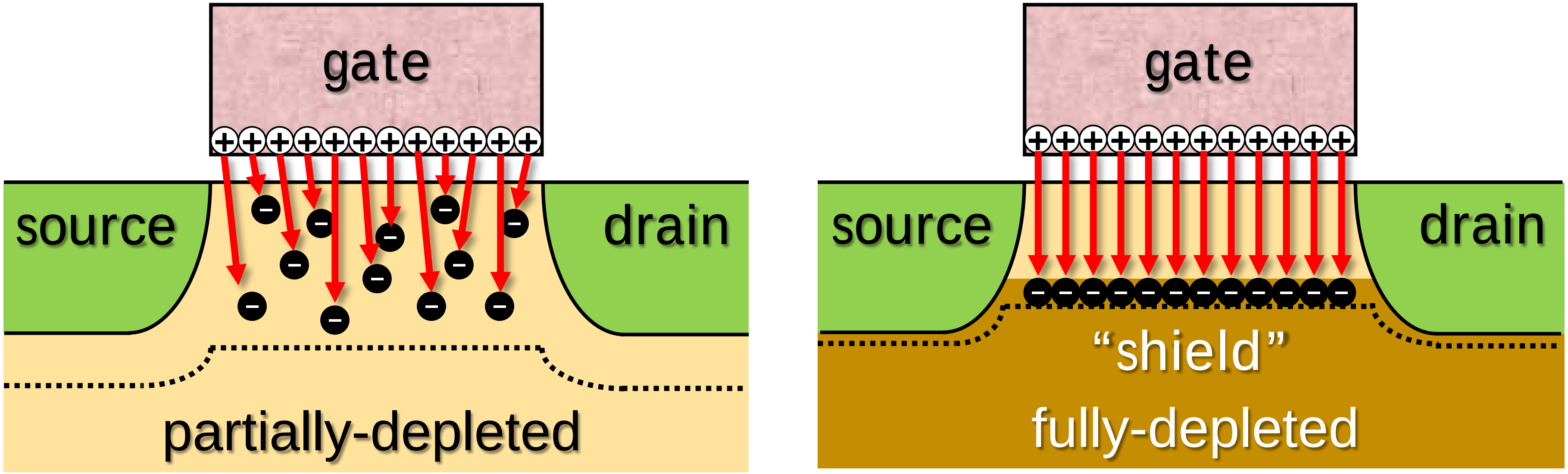
- Shield must be near drain to pull drain *E*-fields away from source barrier → less DIBL
- No dopant scattering in body → higher channel mobility
- Less ΔV_{GS} to transition from flatband to inversion, so must adjust gate work function Φ_M (¼-gap vs. band-edge)
- In practice, still need some body dopants to counterdope S/D diffusion & adjust V_T
- Classic V_T condition no longer makes sense since ϕ_b=0



Skotnicki, STMicroelectronics [7]
Chang *et al*., UC Berkeley [8]

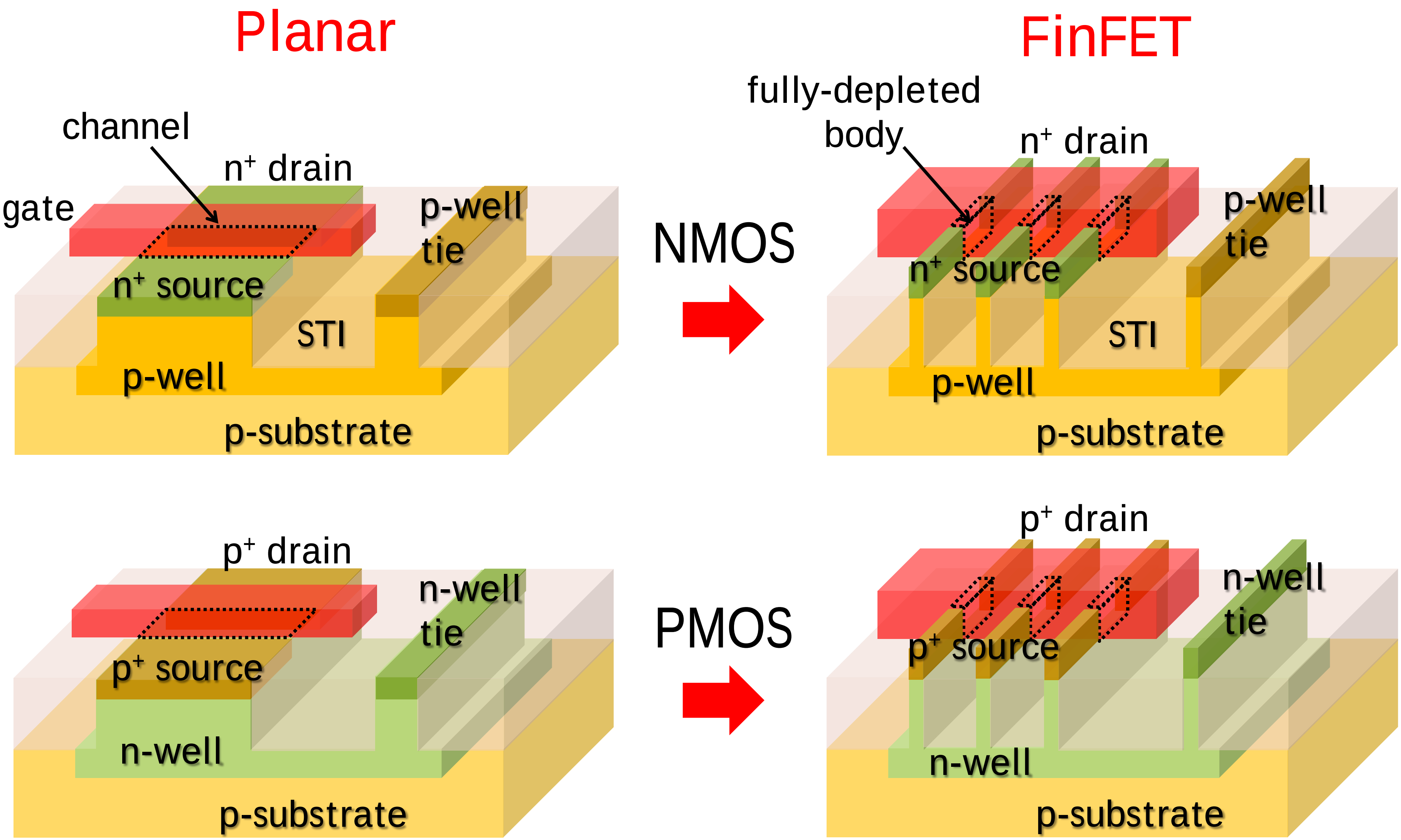
Fully-Depleted Eliminates RDF

- Body dopants vary in *number* but also in *location*
  - Variation in length of *E*-field lines integrates to variation in band-bending or V_T
- In fully-depleted, *E*-field lines have much tighter length distribution which eliminates V_T variation due to RDF
  - But V_T becomes very sensitive to *geometric* variation



Asenov, U Glasgow [9]

Migrating to Fully-Depleted FinFET



Huang *et al*., UC Berkeley [10]

Outline

- MOSFET, Fully-Depleted & FinFET Basics
- Technology Considerations
  - Mechanical Stressors
  - High-K/Metal-Gate
  - Middle-Of-Line
  - Multiple Patterning
- Analog/Mixed-Signal Design Considerations
- Conclusion

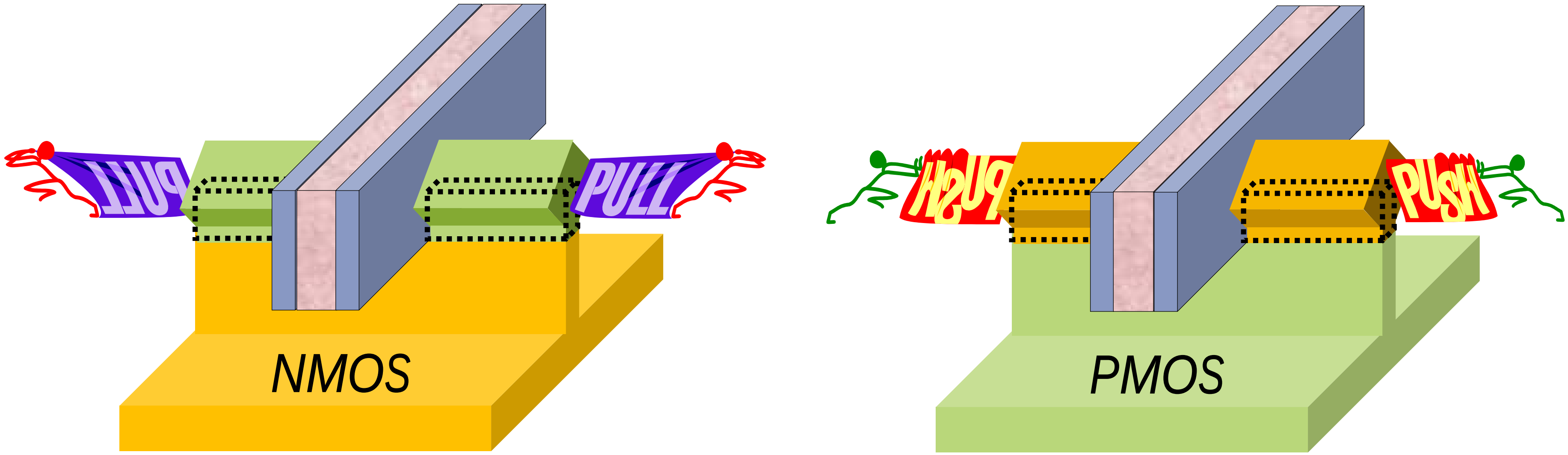
Journey to FinFETs

- 16/14nm employs many new technology elements introduced across multiple earlier nodes
- Each element adds new design complexity

Technology Element	Foundry Debut	Reason Required
Mechanical stressors	90nm	Mobility boost for more FET drive & higher I_{on}/I_{off}
HKMG replacement gate integration	28nm (HK-first) 20nm (HK-last)	Higher C_{ox} for more FET drive & channel control
Middle-of-line	20nm	Contact FET diffusion & gate with tighter CPP
Multiple-patterning	20nm	Sub-80nm pitch lithography without EUV

Mechanical Stressors

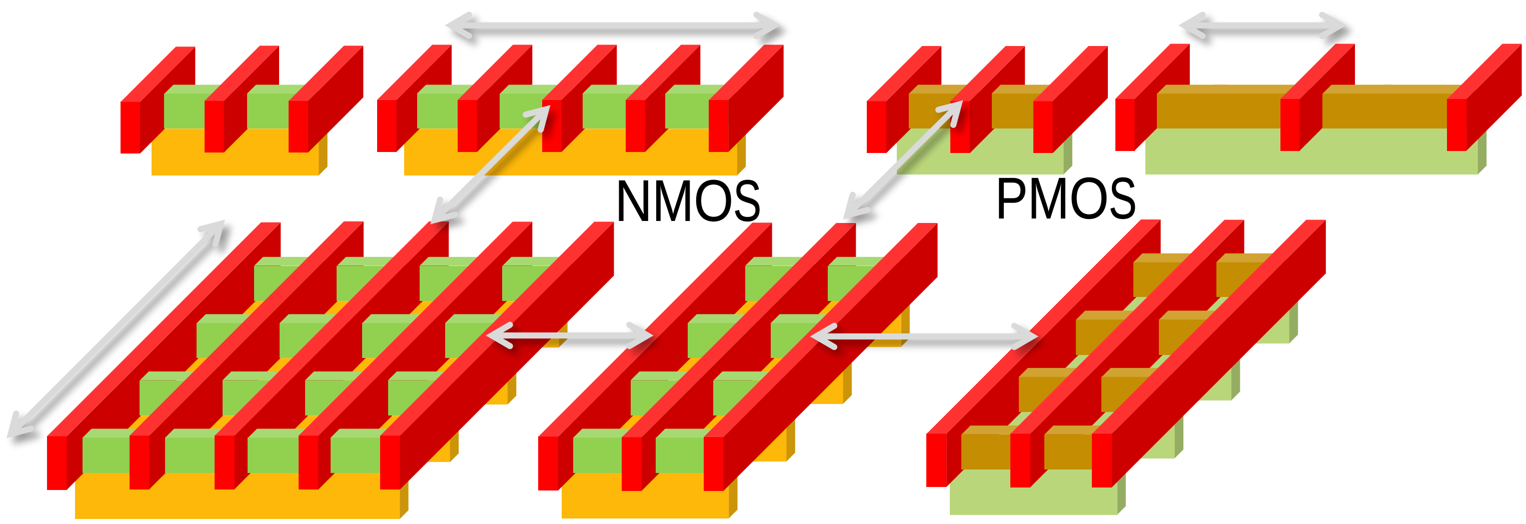
- Carrier mobility depends on lattice strain (Si is piezoresistive)
- Grow stressors to induce channel strain along *L*
  - Tensile for NMOS, compressive for PMOS
  - Techniques: STI fill, S/D epitaxy, gate stress memorization
- Anisotropic mobility & stress response
  - *L* vs. *W* direction, (100) fin top vs. (110) fin sidewall



Garcia Bardon *et al*., IMEC [11]
Liu *et al*., Globalfoundries [12]

Stress-Related Layout Effects

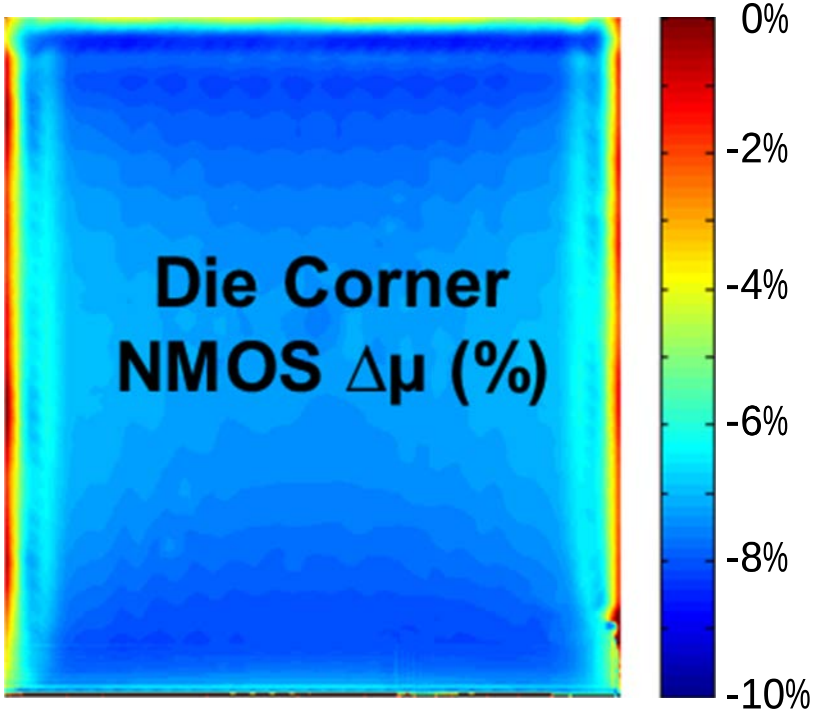
- Stressors are stronger in 16/14nm for more FET drive, so layout effects can be more severe → schematic/layout Δ
- Stress build-up in longer active, I_D/fin not constant vs. # fins
- NMOS/PMOS stress mutually weaken each other
- Interaction with stress of surrounding isolation

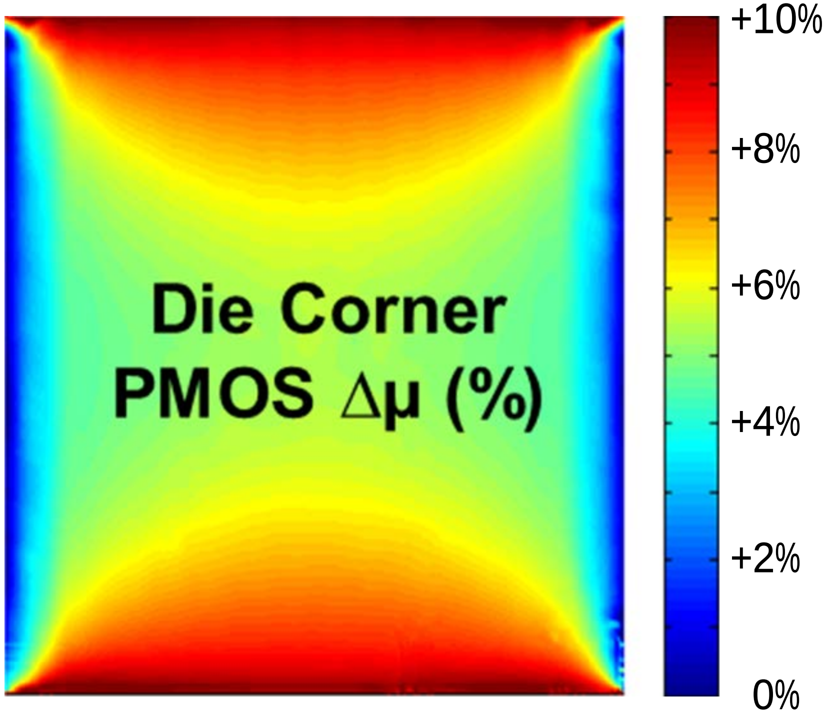


Faricelli, AMD [13]
Lee *et al.*, Samsung [14]
Sato *et al.*, IBM [15]

Electrical Chip-Package Interaction

- FET mobility sensitive to stress from die attach to package
- Package stress can impact long-range device matching (e.g., I/O impedance, bias references, data converters)

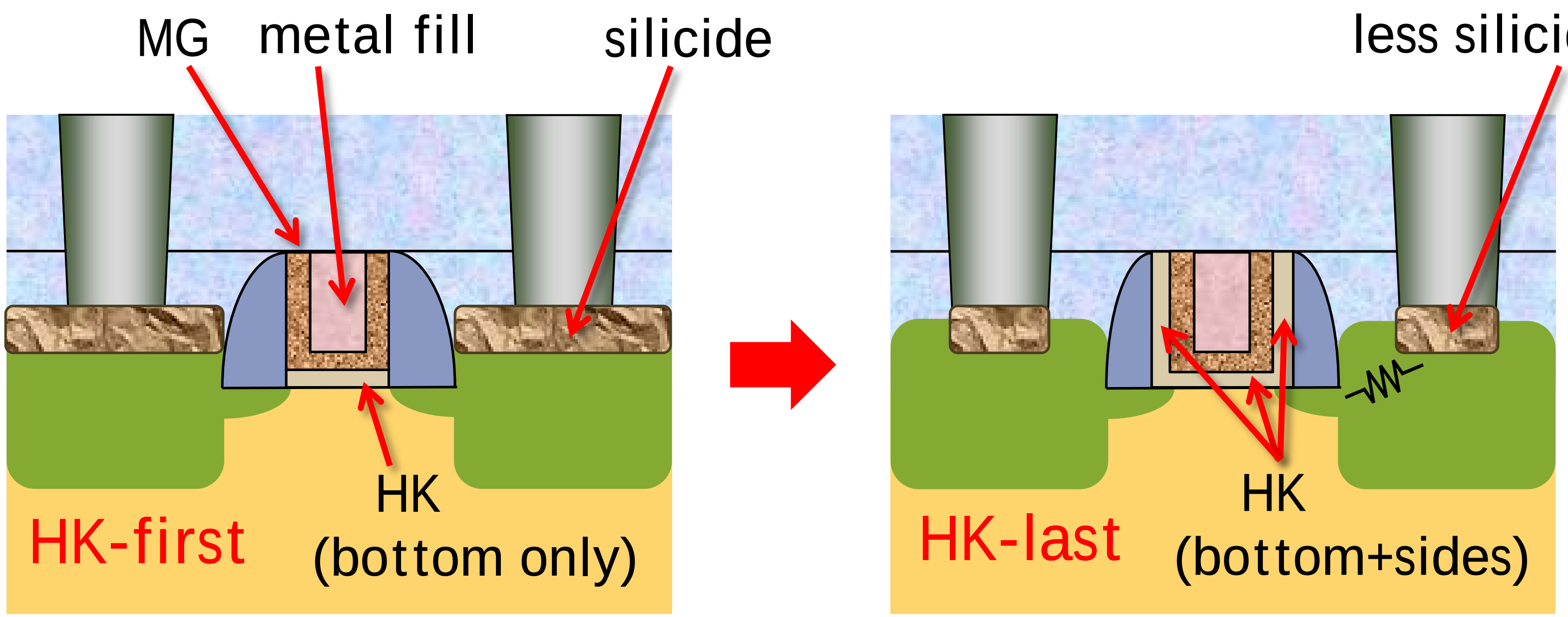




Terzioglu, Qualcomm [1]

High-*K*/Metal-Gate (HKMG)

- Higher C_{ox} without I_{gate} & poly depletion, but finicky interface
- Replace gate after S/D anneal for stable $V_T = f(\Phi_M)$
- Gate = (ALD MG stack to set Φ_M) + (metal fill to reduce R_G)
- Variation in MG grain orientation → V_T variation
- HK-first → HK-last for better gate edge control

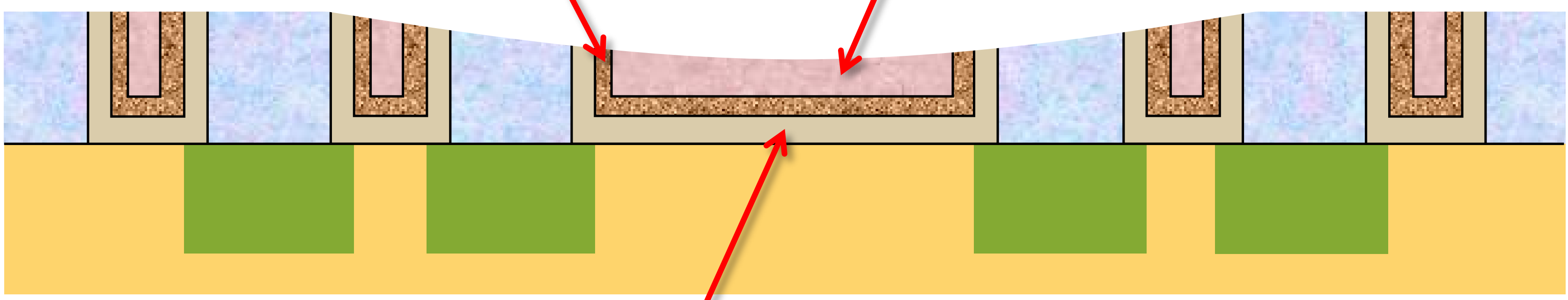


Auth *et al.*, Intel [16]

Packan *et al.*, Intel [17]

Gate Density Induced Mismatch

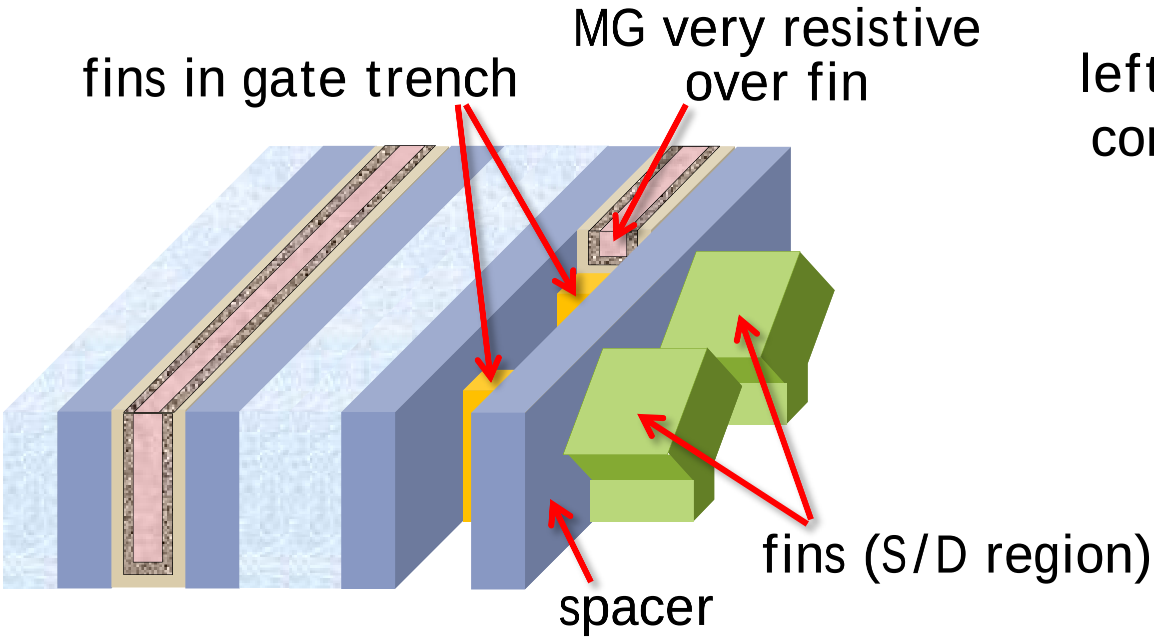
- Thin MG layer that sets gate Φ_M is very resistive
- Gate charge spills into metal fill
  → gate Φ_M is modulated by gate height & also gate *L*
- V_T varies from gate CMP dishing/erosion → matching concern
- Some gate types exposed to multiple CMP → more variation

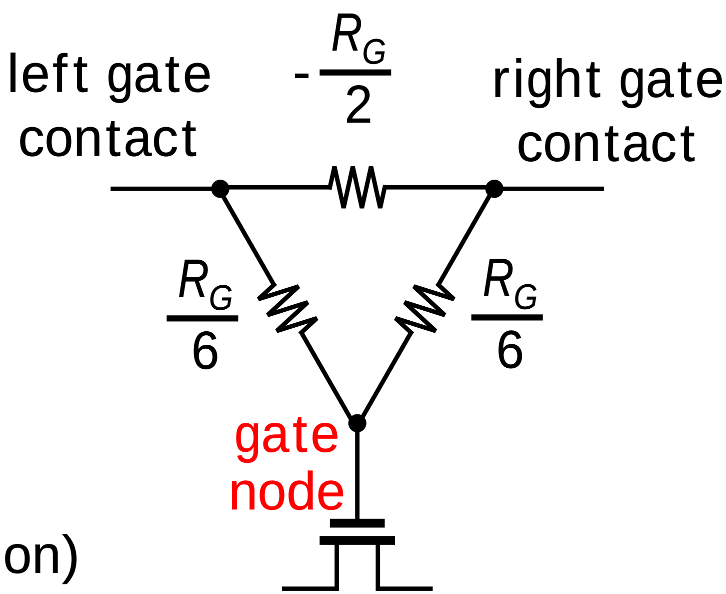


Yang *et al.*, Qualcomm [18]

Gate Resistance Very Significant

- Φ_M metal very resistive, little conductive metal fill for short L
- Δ model approximation
  - Accounts for distributed RC, reality way more complicated
  - $R_G/3$ for 1-side gate contact, $R_G/12$ for 2-side contact
  - R_G for daisy chain connection

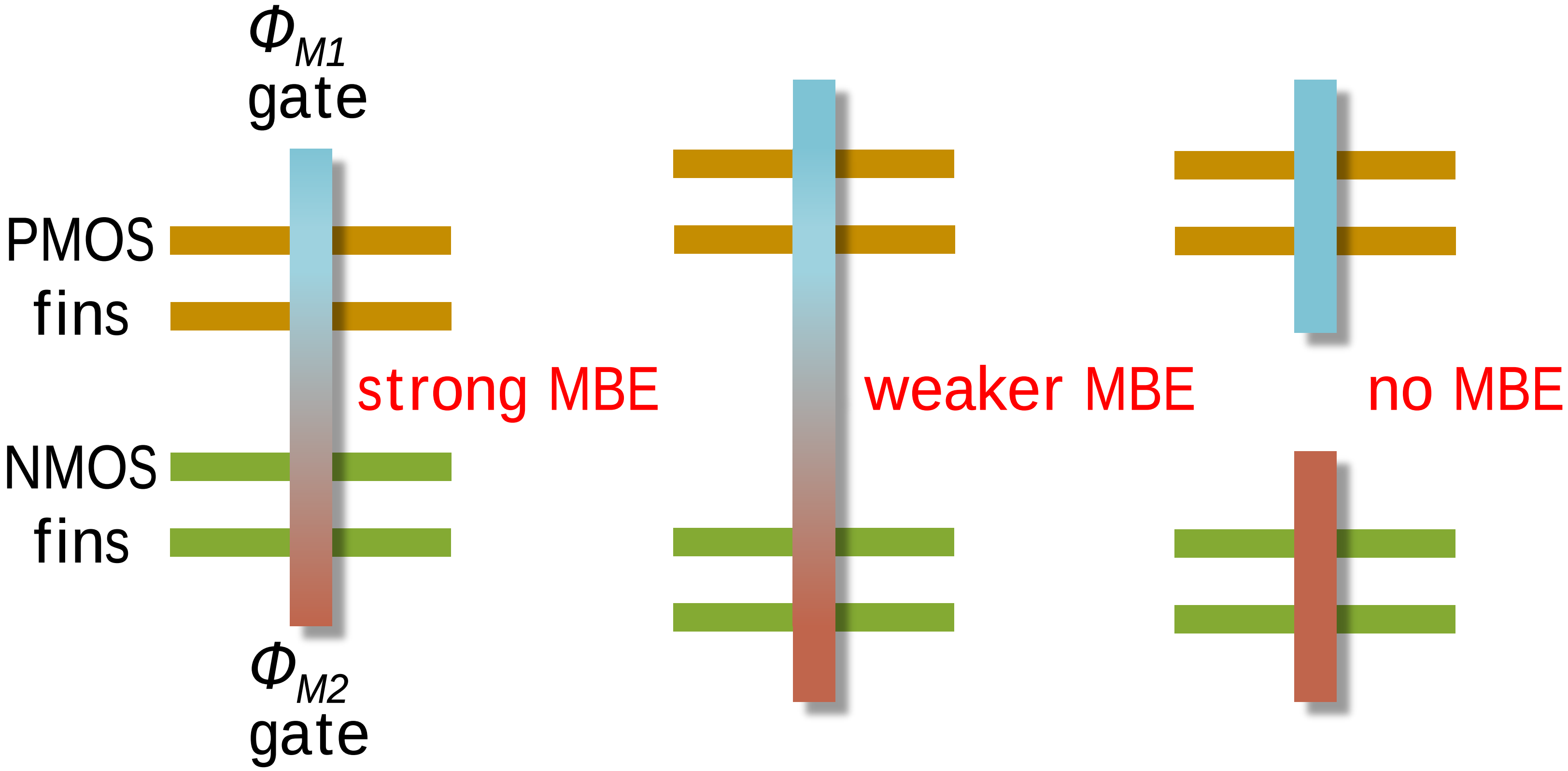




Wu & Chan, HKUST [19]

Metal-gate Boundary Effect (MBE)

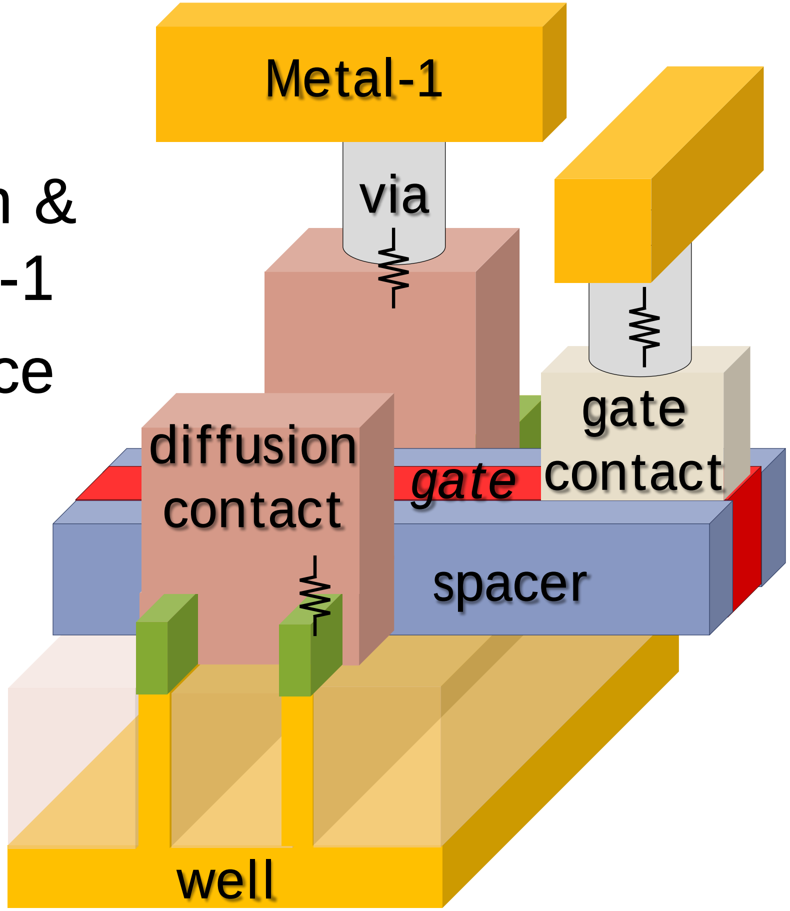
- V_T affected when near interface between two Φ_M metals
- 2 hypotheses: Φ_M metal interdiffusion, etch-related footing
- Eliminate effect using only one Φ_M in each gate → area bloat



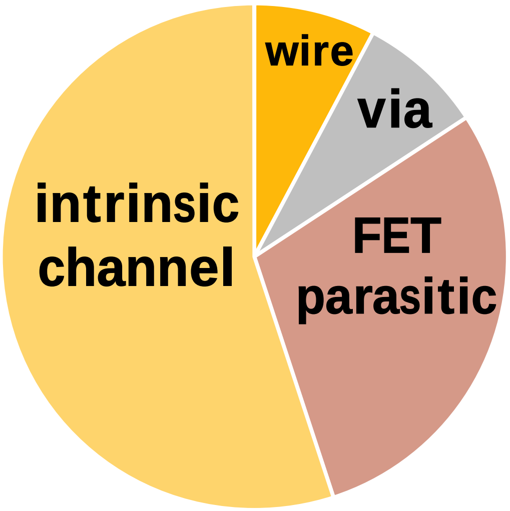
Yamaguchi *et al.*, Toshiba [20]

Complex Middle-Of-Line (MOL)

- Difficult to land diffusion & gate contacts on tight CPP using only one contact mask
- Need separate contacts to diffusion & to gate, also insert via under Metal-1
- BEOL, MOL & R_{ext} parasitic resistance are significant



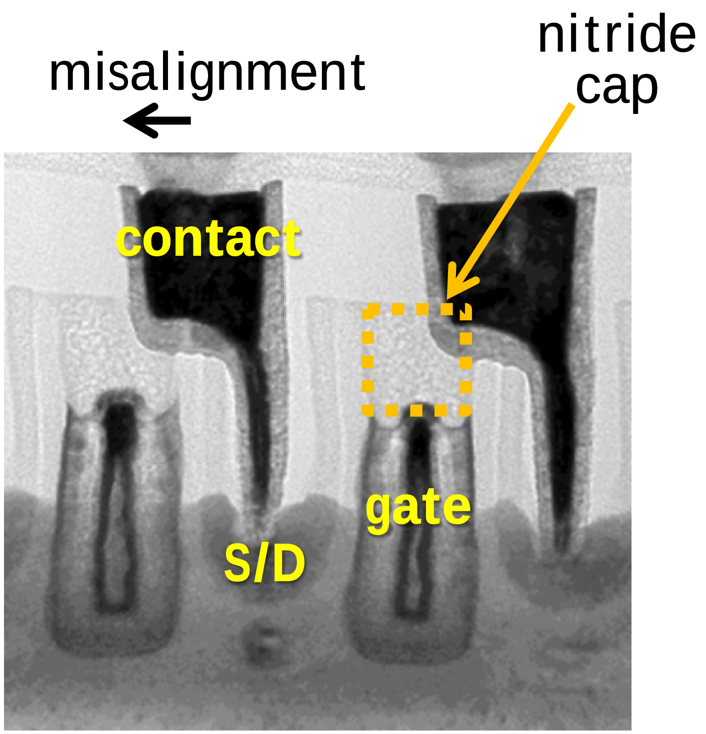
Standard cell resistance contribution

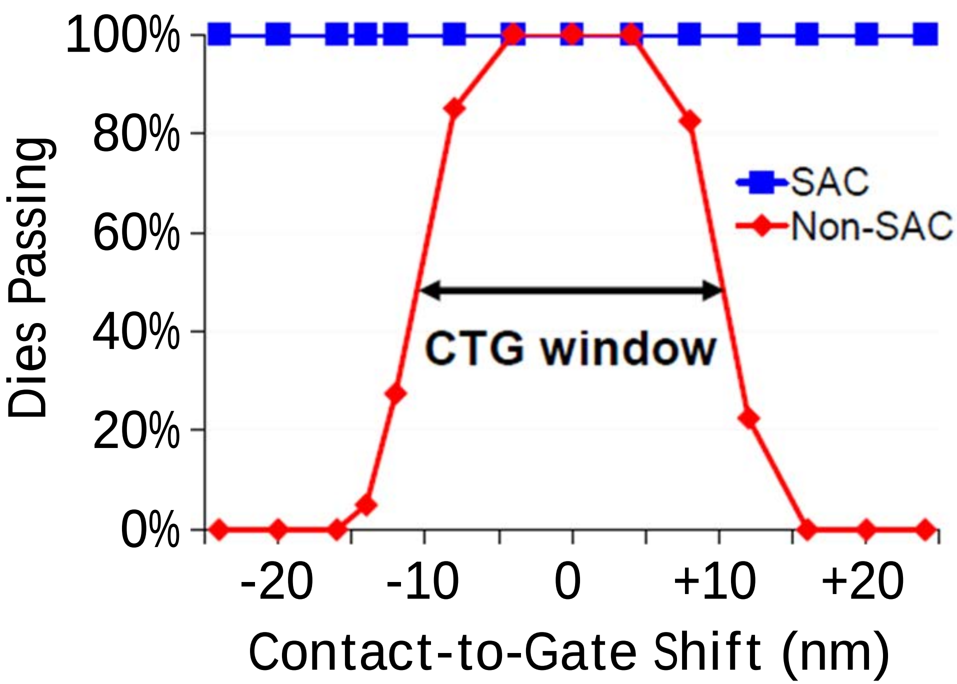


Terzioglu, Qualcomm [1]
Rashed *et al.*, Globalfoundries [21]

Self-Aligned Contact (SAC)

- Allows misaligned contact to land on gate without short
- Etch gate partially after replacement gate CMP, then deposit insulator on top of gate → protects gate during contact etch
- R_G increases & has more variation from partial (recess) etch



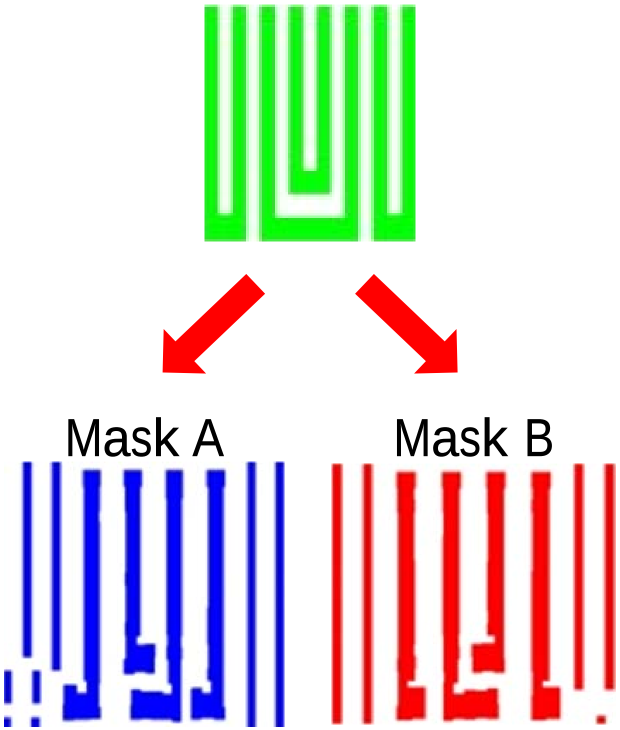


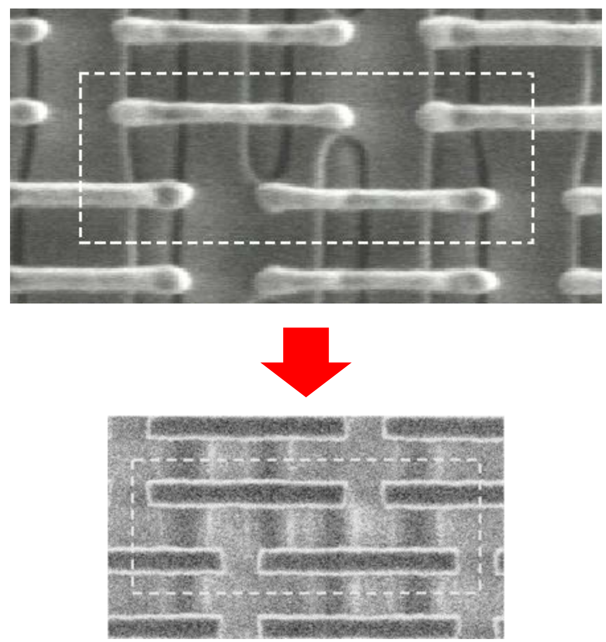
Auth *et al.*, Intel [22]

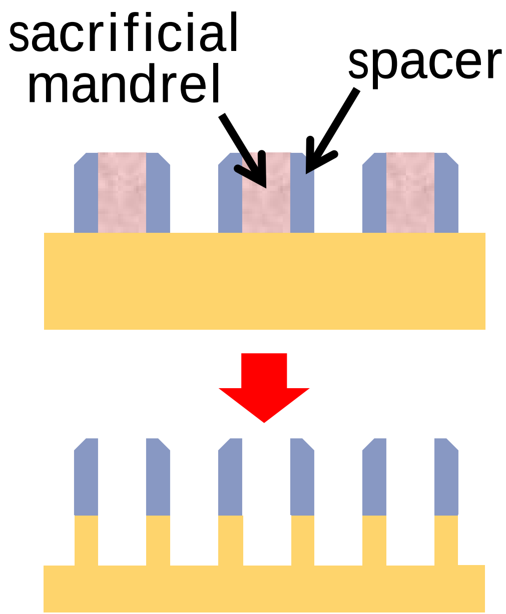
Multiple-Patterning Lithography

- Needed for sub-80nm pitch, EUV not ready for HVM

1. Pitch-split mask decomposition (coloring) → complex DRC
2. Cut masks to reduce line-end-to-end spacing
3. Spacer-based self-aligned double patterning (SADP) for fins







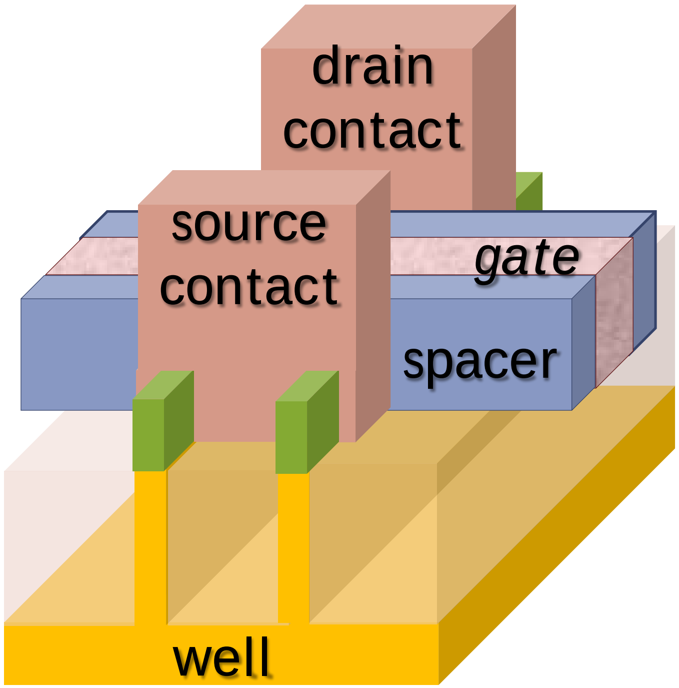
Auth *et al*., Intel [10], [22]
Dorsch, www.semi.org [23]

Outline

- MOSFET, Fully-Depleted & FinFET Basics
- Technology Considerations
- Analog/Mixed-Signal Design Considerations
  - General Principles
  - FETs
  - Passives
- Conclusion

Designing with FinFET

- More drive current for given footprint
- Quantized channel width (challenge for logic & SRAM, OK for analog)
- Better r_{out} (less DIBL) but shorter L_{max}
- Essentially no body effect
- Mismatch variation depends on fin width/ height/shape, HK grains, gate density, stress, less on RDF
- Lower C_j but higher C_{gd} & C_{gs} coupling
- Higher R_s & R_d spreading resistance
- Less junction area efficiency to wells (higher diode series R_D, latch-up)
- No native (zero-V_T) NMOS



Auth *et al*., Intel [22]
Sheu, TSMC [24]

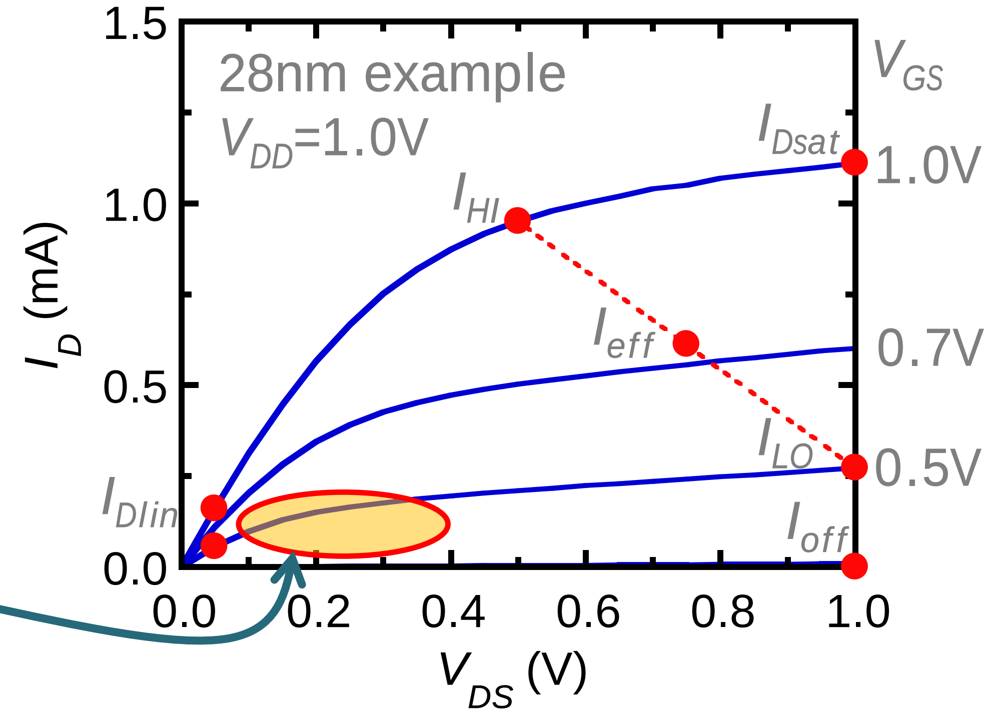
Porting AMS Circuits to FinFET

- For most part can be done with expected node-to-node tweak
- Usual caveats in bleeding-edge nodes
  - Technology & design concurrently developed for faster time-to-market
  - Models are speculative → expect late updates & late inclusion of new effects
  - Stay vigilant on Si/model updates that can break design
  - Choose logic-centric circuits/architectures (fab's priority), desensitize to or calibrate out model uncertainty
- Minimize churn with some upfront layout bloat to avoid constructs made for logic area reduction, e.g.,
  - Single gate with more than one Φ_M metal
  - Devices with no active edge dummies

Bair, AMD [25]

FET Modeling for Analog vs. Digital

- SoC technology/modeling driven by logic & SRAM
- Device targeting & model correlation at few *I*-*V* & *C*-*V* points for limited V_{DD} values

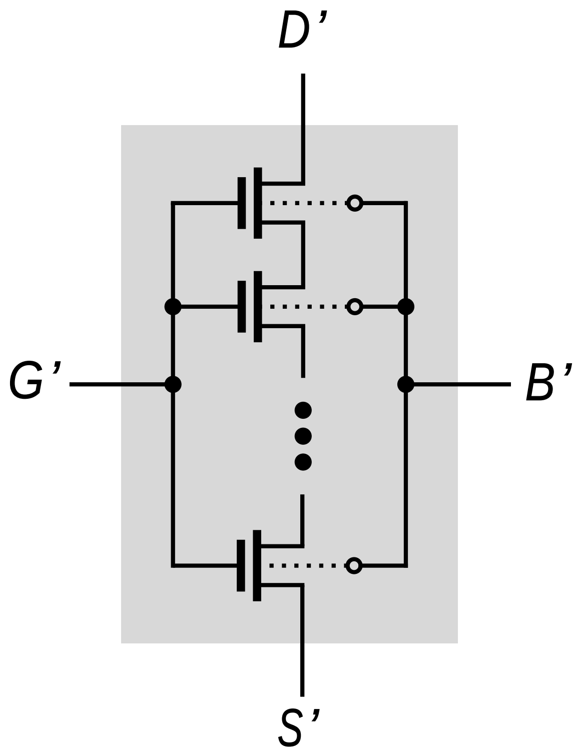


- Analog also needs accurate slope modeling (g_m, g_{ds}) which gets some attention but not priority
- Corner models (e.g., SS, FF) don't necessarily correlate to analog corners

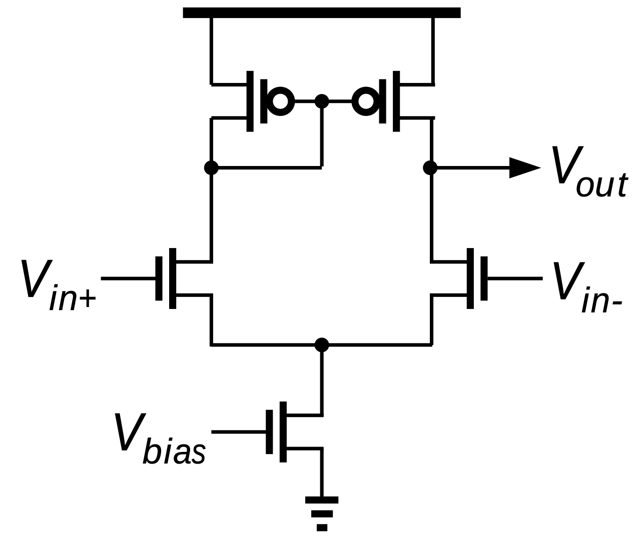
Feng *et al.*, Globalfoundries [26]
McAndrew *et al.*, Freescale [27]

Composite FET

- Need high r_{out} for accurate AC *V-to-I* conversion → long *L*
- L_{max} limited by gate litho/etch loading & HKMG integration
- Composite FET stack with shorted gate is now commonplace in current mirrors, op amps, data converters, etc.
  - Only top FET in saturation, all other FETs in triode for source degeneration
  - Not a cascode
  - Insignificant body effect
  - Intermediate parasitic C_{gd}, C_{gs} & C_j
- Designers mainly interested in composite FET characteristics
  - Co-development with EDA vendors



Don't Trust Simulator V_T - Many Still Do

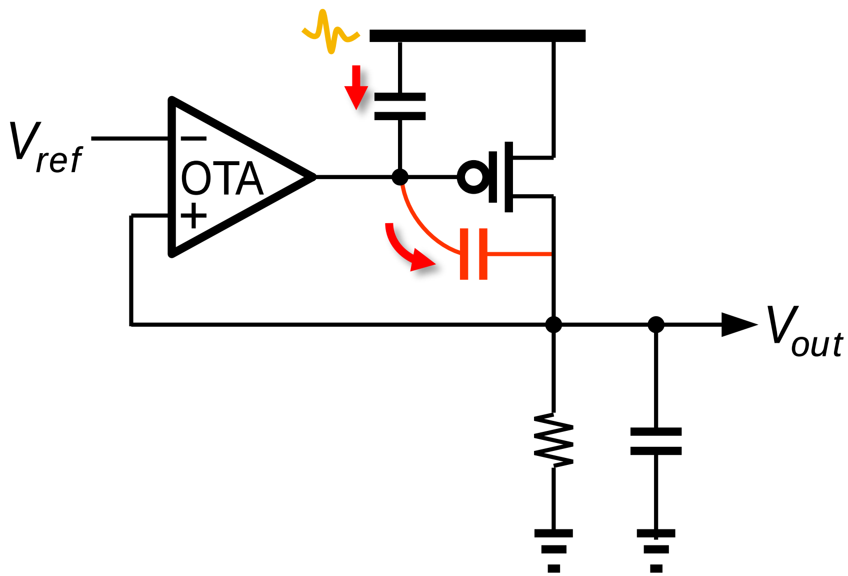


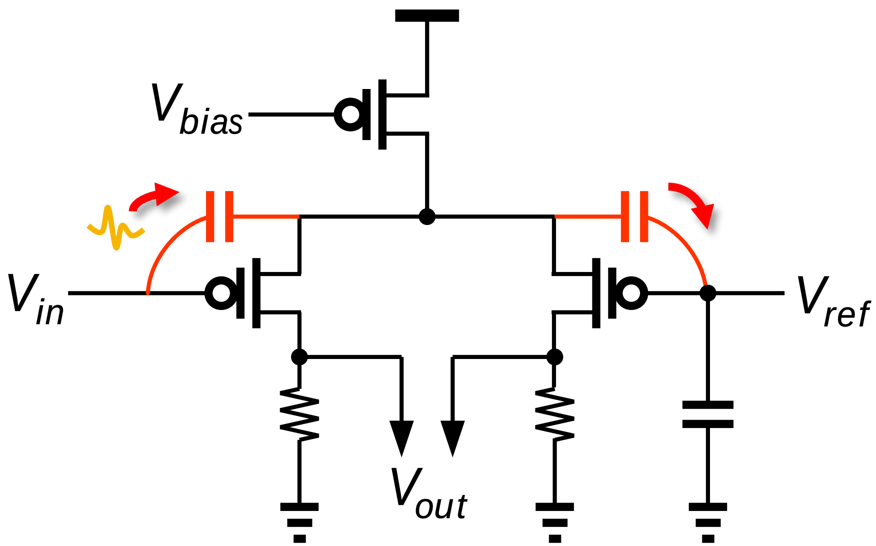
- Tough to stack >3 devices in saturation with low V_{DD}
- Can only operate devices in weak/ moderate (not strong) inversion
- Dangerous to design to "usual" V_T reported by simulator
  - Can get wrong FET sizing to ensure (V_{GS}-V_T)>0 vs. low offset (e.g., diff pair)
  - Correct goal: burn enough I_D for g_m & *BW* → g_m/I_D method
- Fab typically measures V_T using constant-current method
  - Simulators now conveniently report constant-current V_T
  - Best to treat V_T as reference point that anchors *I-V*

Loke *et al*., AMD [28]
Silveira *et al*., U República [29]

Stronger Parasitic Coupling

- S/D trench contacts & gate form vertical plate capacitors
- Worse supply rejection in LDO regulators
- Kickback noise to analog biasing signals, e.g., DDR RX
- Adding capacitance increases area & wake-up time (concern for burst-mode operation, e.g., IoT)





I/O Voltage Not Scaling With Core Supply

- Many I/Os still use 1.8V signaling despite core V_{DD} reduction
  - Many peripheral ICs remain at lower cost nodes
  - Backward compatibility is key constraint for some I/Os
- Increasingly tough to keep 1.8V thick-oxide devices
  - Thick ALD gate oxide not easy for tighter fin pitch
  - Voltage level shifters must deal with wider voltage gap
  - Some standards no longer support legacy modes in favor of higher link rate & lower power (e.g., LPDDR5)
- Need ecosystem consensus
  - Industry has migrated from 5.0V to 3.3V to 2.5V to 1.8V
  - Obvious power & area benefit to migrate to say 1.2V
  - 1.8V remains an industry-wide issue until next transition

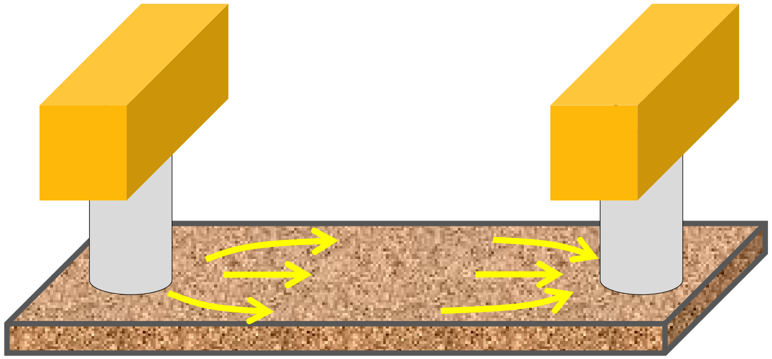
Wei *et al*., Globalfoundries [30]

16/14nm Passives

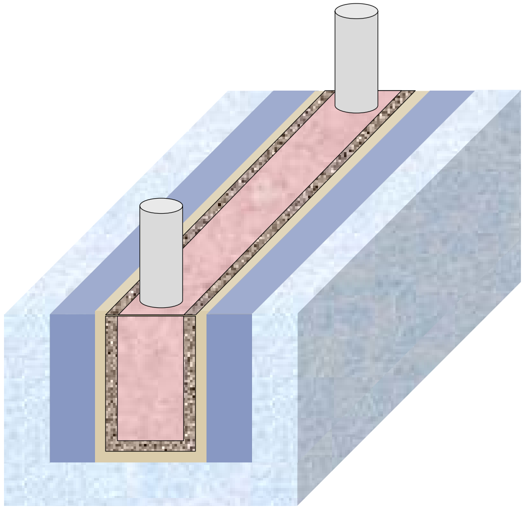
- Resistors
  - Precision MOL thin film resistor (migration from poly)
  - Metal-gate resistor
- Capacitors
  - Metal-Oxide-Metal (MOM)
  - Accumulation-mode varactor
  - Metal-Insulator-Metal (MIM) – extra cost, less common
- Inductors – typically top BEOL layers
- PNP-BJT (analog diode) & ESD diodes
- Don't assume models capture all key effects even though we're the only customer

Resistor Options

- Precision MOL resistor
  (thin metal compound on STI/ILD)
  - Difficult to build poly resistor ends in HK-last process
  - Ends not well defined, current spreading near contacts
  - Decouples resistor integration from FEOL



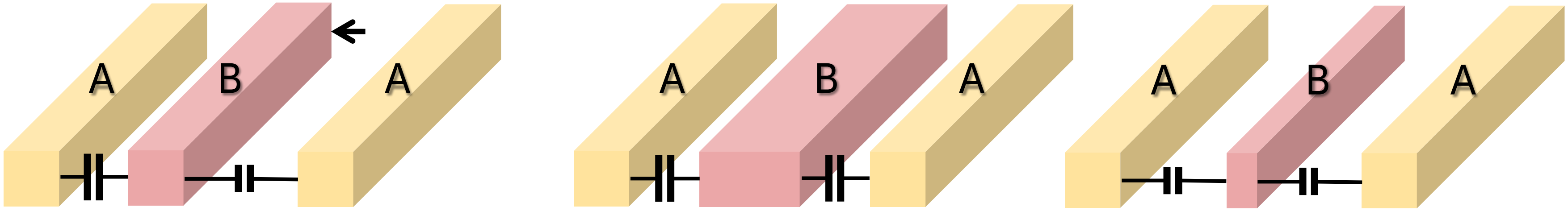
- Metal-gate resistor
  - Available for free
  - Not so well controlled
  - ρ_{sheet} depends on gate density, W, W_{max} limit



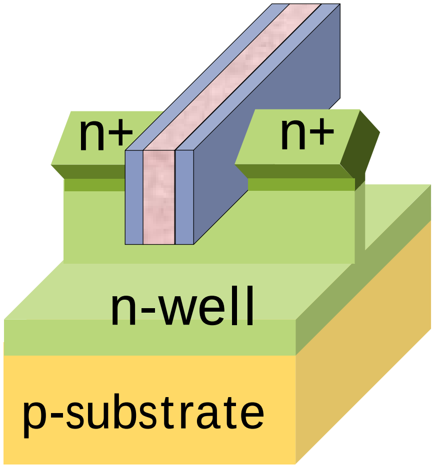
Capacitor Options

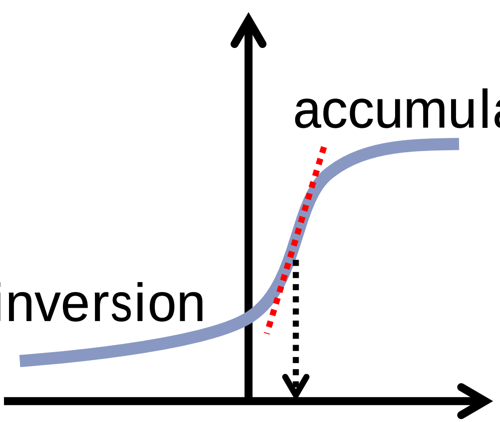
- Metal-Oxide-Metal (MOM)
  - Rarely has scaling helped analog ☺
  - Be careful with non-physical BEOL overlay corner models

reality vs. C_{max} model C_{min} model



- Accumulation-mode varactor
  - *C*-*V* transition may shift from Φ_M tuning for fully-depleted
  - Steeper transition for higher K_{VCO}

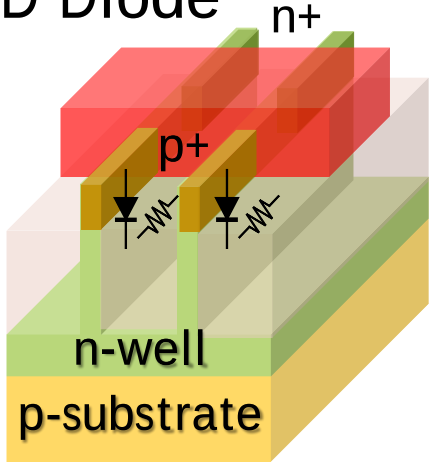




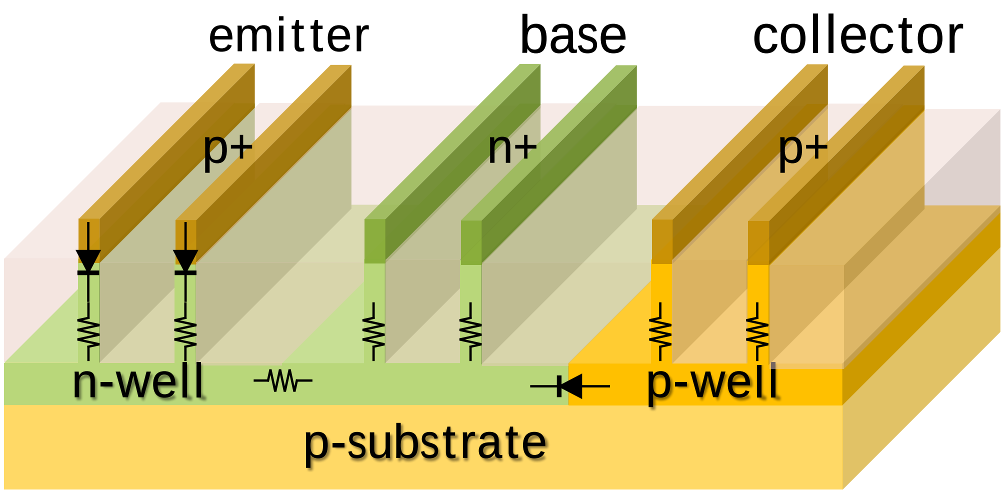
PNP-BJT & ESD Diodes

- Fin width << fin pitch
  → higher R_{series} than planar
- Hard to scale ESD area without reducing ESD HBM/CDM limits
- Maturity of ESD models often lags during technology development

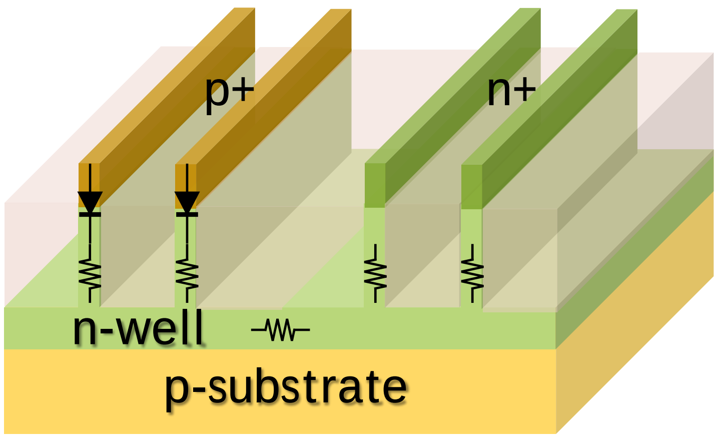
Gated ESD Diode



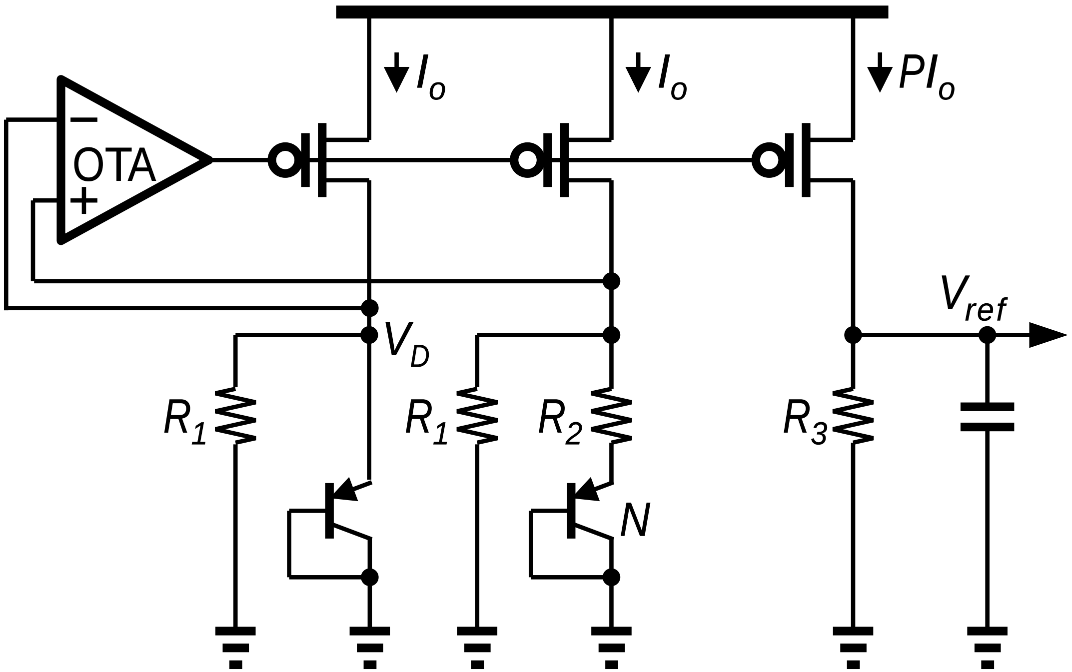
PNP-BJT

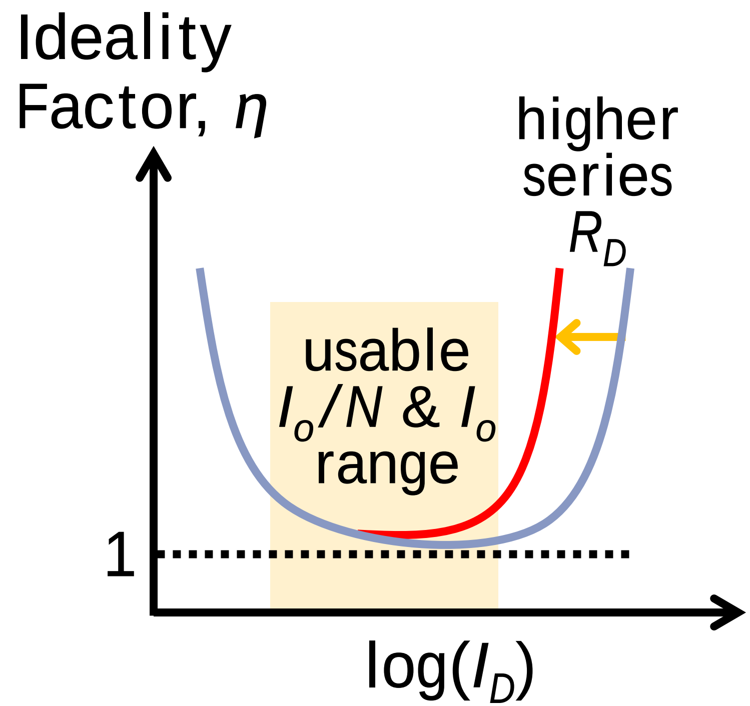


STI ESD Diode



Low-Voltage Bandgap Reference



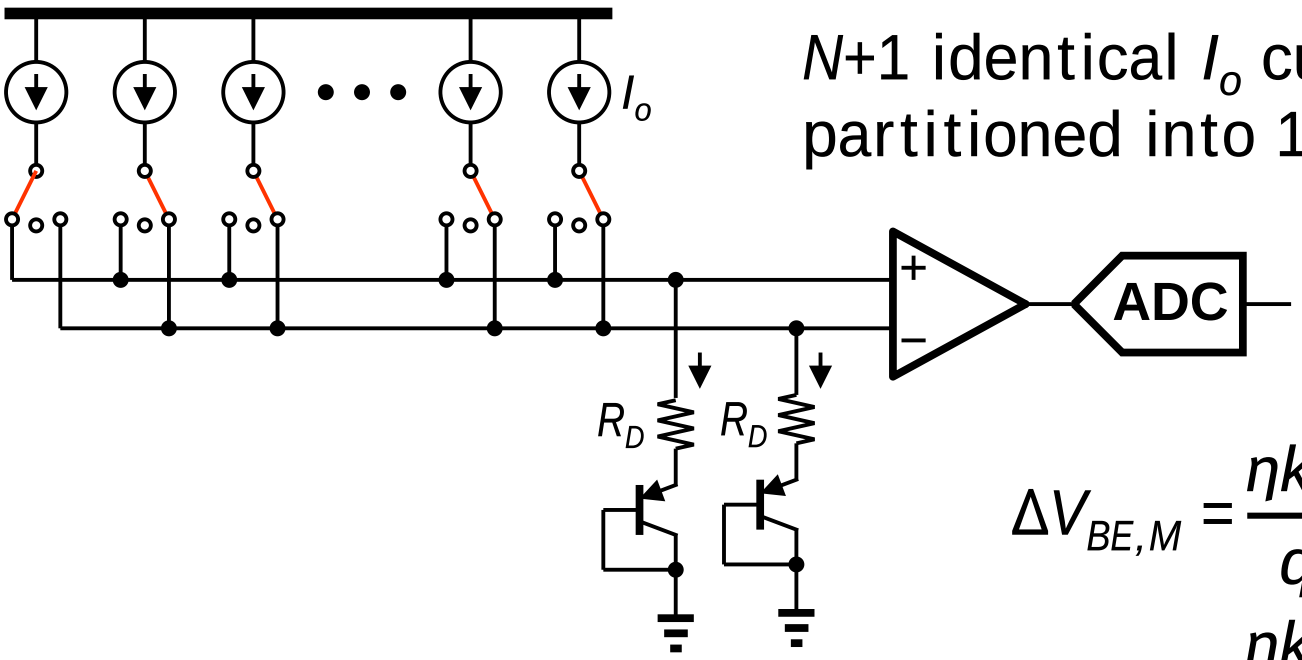


$$V_{ref} = \underbrace{\frac{PR_3}{R_1} V_D}_{\text{CTAT}} + \underbrace{\frac{PR_3}{R_2} \frac{\eta kT}{q} \ln N}_{\text{PTAT}}$$

- PTAT+CTAT using currents
- More R_D → smaller N
- Higher V_D → headroom issue

Banba *et al*., Toshiba [31]

Thermal Sensor with R_D Cancellation



N+1 identical I_o current sources partitioned into 1, M & N sources

$$\Delta V_{BE,M} = \frac{\eta kT}{q} \ln M + (M\text{-}1)\, I_o R_D$$

$$\Delta V_{BE,N} = \frac{\eta kT}{q} \ln N + (N\text{-}1)\, I_o R_D$$

$$\frac{\eta kT}{q} = \frac{(N\text{-}1)\Delta V_{BE,M} - (M\text{-}1)\Delta V_{BE,N}}{(N\text{-}1)\ln M - (M\text{-}1)\ln N}$$

- Measure ΔV_{BE} at current ratios of 1:M & 1:N to cancel diode R_D
- Swap amp inputs to cancel diode mismatch
- Average out I_o variation with Dynamic Element Matching

ON Semiconductor [32]

Conclusion

- 14nm mobile SoCs are already in production; no showstoppers to migrate AMS designs to finFET
- 16/14nm AMS design is about understanding all the precursor technologies that led to finFET as much as understanding finFET itself
- FinFET/HKMG/MOL parasitics & local layout effects have significantly increased AMS design effort
- Logic & SRAM will continue to drive CMOS scaling priorities into 10nm & 7nm, so expect AMS designs to continue adapting

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Acknowledgments

- Esin Terzioglu
- Sam Yang
- Jihong Choi
- Albert Kumar
- Tin Tin Wee
- Ray Stephany
- Lixin Ge
- Bo Yu
- Zhiqin Chen
- Stanley S.C. Song
- Steven Dillen
- Stephen Knol
- Patrick Drennan
- Ken Rim
- Chidi Chidambaram
- Yanxiang Liu
- Jun Yuan
- Masoud Roham
- Reza Jalilizeinali
- Xiaohua Kong