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JITTER IN RING OSCILLATORS

BY

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JITTER IN RING OSCILLATORS

(Order No.)

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ABSTRACT

This thesis describes a methodology for analyzing and predicting jitter (phase noise) in ring oscillators. Due to their high operating frequency and ease of integration, use of rings in jitter sensitive applications is becoming more common. One example is in data communication, where a ring is used as the voltage controlled oscillator (VCO) in a phase-locked loop (PLL). Despite the wide use of ring oscillators, their jitter performance has been poorly understood.

The first step in developing this methodology is a technique for relating various measures of jitter in PLLs. The technique establishes correspondence among time and frequency domain measures of jitter with the PLL loop open or closed. Results are given when this time/frequency technique is applied to jitter measurements from an existing PLL.

The next step is to determine the fundamental sources of jitter in rings and how they affect the measured performance. A review of analysis techniques for harmonic and relaxation oscillators shows that a different approach is needed to design for low jitter in rings. The approach taken follows naturally from the time/frequency jitter technique developed in the first part of the thesis. A major contribution is the identification of a design figure of merit which is independent of both the ring frequency and number of stages. Experimental results from several rings of different lengths demonstrate that jitter depends primarily on thermal noise sources in the delay stage, and has little to do with the number of stages in the ring.

The final result is a simple design procedure which gives explicit constraints on circuit elements as a function of desired jitter performance. The design of a low jitter ring VCO for a 155 MHz clock recovery PLL is described. Some of the inherent limitations of the

ring architecture, as well as design techniques for dealing with those limitations, are discussed. Test results are presented for the PLL, which has been fabricated in a dielectrically isolated complementary bipolar process.

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List of Symbols

B	Noise bandwidth	[Hz]
C	Capacitance	[F]
E{}	Expectation operator	
E_B	Energy supplied by negative resistor in LC oscillator	[J]
e_n	Voltage noise density	[V/$\sqrt{\text{H}}$ z]
f	Frequency; or "offset" (from carrier) frequency	[Hz]
f_L	Loop Bandwidth	[Hz]
f_o	VCO center frequency	[Hz]
f_{out}	VCO output frequency	[Hz]
f(t)	Frequency modulated over time	[Hz]
$H_n(s)$	Phase noise transfer function through PLL loop	
Hs(s)	Phase signal transfer function through PLL loop	
I	Current	[A]
I_{EE}	Differential pair tail current	[A]
I_{FAST}	Interpolator current	[A]
I_n	Noise current	[A]
I_O	DC bias current	[A]
I_R	Current threshold for regenerative switching	[A]
I_{SLOW}	Interpolator current	[A]
i_n	Current noise density	[A/$\sqrt{\text{H}}$ z]
j	$\sqrt{-1}$	
k	Boltzmann's constant	[J/K]
K_o	VCO control constant	[rad/V· s]
L	Inductance	[Hy]
m	Periods of delay in discrete time process	
n	Index of a discrete time process	
N_1	Open loop frequency domain VCO figure-of-merit	[rad^2· Hz]
P_B	Power flow from negative resistor in LC oscillator	[J]
Q	Quality factor for a second order system	
q_e	Electron charge	[coul]

R	Resistance	[Ω]
$R_{xx}(\Delta T)$	Autocorrelation of the VCO phase jitter process	[rad^2]
S	Time derivative (slope) of a waveform	[V/s]
s	Laplace complex frequency	[rad/s]
$S_\phi(f)$	Phase noise p.s.d.	[rad^2/Hz]
$S_{\phi CL}(f)$	Closed loop phase noise p.s.d.	[rad^2/Hz]
$S_{\phi OL}(f)$	Open loop phase noise p.s.d.	[rad^2/Hz]
t	Time	[s]
$t[n]$	Clock period random process	
$t_m[n]$	Random process, sum of m adjacent clock periods	
T	Temperature	[K]
T_d	Delay time through a gate	[s]
T_o	Period corresponding to center frequency f_o	[s]
V	Voltage	[V]
V_{ctl}	VCO input (control) voltage	[V]
V_{in}	Input voltage (analog representation of serial data)	[V]
V_{trig}	Voltage waveform for CSA trigger	[V]
V_0	Voltage amplitude	[V]
$V(t)$	Voltage varying over time	[V]
Y	Admittance	[S]
Z	Impedance	[Ω]
α	Noise scaling factor (from Abidi and Meyer)	
δ_t	Time error due to noise	[s]
δ_v	Voltage error due to noise	[V]
Δf	rms frequency deviation	[s]
ΔT	Delay time for jitter measurement	[s]
ε	Gate delay error	[s]
ζ	Damping factor for a second order system	
θ_i	PLL input phase	[rad]
θ_n	PLL phase noise	[rad]
θ_o	PLL output phase	[rad]
κ	Open-loop time domain VCO figure-of-merit	[$\sqrt{s}$]
λ	Emitter unbalance ratio	
ρ	VCO tuning range (ratio of maximum, minimum frequencies)	

σ	Standard deviation of a distribution	
σ^2	Variance of a distribution	
σ_t	Standard deviation of time errors	[s]
σ_v	Standard deviation of voltage errors	[s]
σ_x	Closed-loop, transmit-clock-referenced jitter	[s]
$\sigma_{\Delta T}$	Self referenced jitter at delay ΔT	[s]
$\sigma_{\Delta T(CL)}$	Closed-Loop, self referenced jitter at delay ΔT	[s]
sDT(OL)	Open-Loop, self referenced jitter at delay ΔT	[s]
τ_T	Bipolar transistor base transit time	[s]
τ_L	Time constant associated with loop bandwidth f_L	[s]
ϕ	Phase	[rad]
ϕ_o	Initial phase	[rad]
$\phi(t)$	Phase as a function of time ("unwrapped")	[rad]
ω	Angular (natural) frequency	[rad/s]
ω_n	Bandwidth of noise process	[rad/s]
ω_o	VCO center frequency	[rad/s]
ω_{out}	VCO output frequency	[rad/s]
$\omega(t)$	Natural frequency modulated over time	[rad/s]

List of abbreviations and acronyms

ATM	Asynchronous Transfer Mode
BER	Bit Error Rate
CSA	Communications Signal Analyzer
FM	Frequency Modulation
LTI	Linear Time Invariant
NRZ	Non-Return to Zero
PLL	Phase Locked Loop
PM	Phase Modulation
p.s.d.	power spectral density
PSH	Pulsed Sample and Hold
PTAT	Proportional To Absolute Temperature
SONET	Synchronous Optical NETwork
UI	Unit Interval
VCO	Voltage Controlled Oscillator
WSS	Wide Sense Stationary

1. Introduction

Structure of this thesis

This thesis is divided into seven chapters. Experimental verification is presented in the same chapter as the corresponding theoretical development, rather than being isolated in a separate chapter.

Section 1.1 of this first chapter introduces the use of PLLs for clock recovery in serial data communication, the main application for which this work was done. Other applications which are concerned with jitter are also mentioned. Section 1.2 introduces fundamental concepts for understanding phase, phase noise, and jitter, as well as their effect on the PLL. Section 1.3 introduces the different types of VCOs that are used in clock recovery PLLs. Section 1.4 is a general introduction to phase and jitter measurement techniques; Section 1.5 is a detailed specification of five jitter measures with which this thesis will be concerned. Section 1.6 establishes the motivation and goals for the work of this thesis and the value of its contributions.

Chapter 2 covers the mathematical development of a technique for relating the five jitter measures of Section 1.5. The technique is verified experimentally through measurements made on several existing PLLs and VCOs in both closed loop and open loop conditions.

Chapter 3 develops a general theoretical approach for analyzing and predicting jitter in ring oscillators. Section 3.1 reviews published jitter analysis techniques for the harmonic oscillator and the multivibrator. This review shows that neither analysis technique by itself is well suited to ring oscillators. Section 3.2 develops a methodology for analyzing jitter in rings. The methodology flows naturally from the time/frequency technique developed in Chapter 2. A major contribution is the identification of a design figure of merit which is independent of both the ring frequency and number of stages. This leads to a simple, general design methodology which is described in Section 3.3. Section 3.4 presents experimental verification of the concepts underlying the methodology.

Chapter 4 examines the jitter methodology applied to the detailed design of a ring oscillator composed of differential pair delay stages. This type of ring oscillator is commonly used at high frequencies when low jitter performance is desired. Explicit numerical relationships are developed relating noise sources to resulting jitter.

Experimental results from several rings of different lengths demonstrate the general applicability of this approach.

As an example of the procedure, the design of a low jitter ring VCO for a 155 MHz clock recovery PLL is described in Chapter 5. Some of the inherent limitations of the ring architecture, as well as design techniques for dealing with those limitations, are discussed. The PLL has been fabricated in a dielectrically isolated, complementary bipolar, 5 GHz-f_T (npn) / 4 GHz-f_T (pnp) process. Test results are presented which show good agreement to the design methodology's numerical predictions.

Chapter 6 is a summary for the designer whose interest is applying the methodology to design a low jitter ring oscillator. Starting with desired jitter performance, expressed in either the time or frequency domain, the procedure gives explicit constraints on values of circuit elements.

Chapter 7 concludes by summarizing the developments and contributions of the thesis, and pointing out possible areas for future work.

1.1 Applications

1.1.1 Clock recovery in serial data transmission

The main application for which this work was originally done is serial data transmission over a fiber optic link. One example is the AT&T Synchronous Optical Network (SONET) standard [102]; another is the emerging Asynchronous Transfer Mode (ATM) protocol [103]. This kind of system is shown conceptually in Figure 1.1. To reduce interconnection hardware, only the data is transmitted over a single fiber. At the receiving end of the link, a clock recovery circuit generates the bit clock RCLK from the serial data stream V_{in}. The clock recovery circuit also samples V_{in} to retime the serial data with respect to the recovered clock.

For this application, the ultimate goal of this thesis is to determine how well we can perform the clock recovery function. The timing diagram in Figure 1.1 shows the ideal case when clock recovery is performed perfectly: There is no phase error in the recovered clock, and RCLK samples V_{in} at the exact center of the bit period. This gives the minimum bit error rate (BER). Any deviation of RCLK from the ideal will increase BER.

In reality, there will be both static ("phase offset") and dynamic ("phase jitter" or simply "jitter") phase errors in the recovered clock, which will degrade performance and increase the BER. Reducing the bit error rate is a major motivation for reducing jitter in the recovered clock. This thesis will address techniques for reducing dynamic phase errors; static phase errors are not considered.

Increased BER is not the only negative effect of jitter in serial data communication. In a repeatered system, where the recovered clock is also used as a transmit clock for a subsequent data link, phase jitter reduces the number of links that can be cascaded before jitter becomes unacceptably large [82].

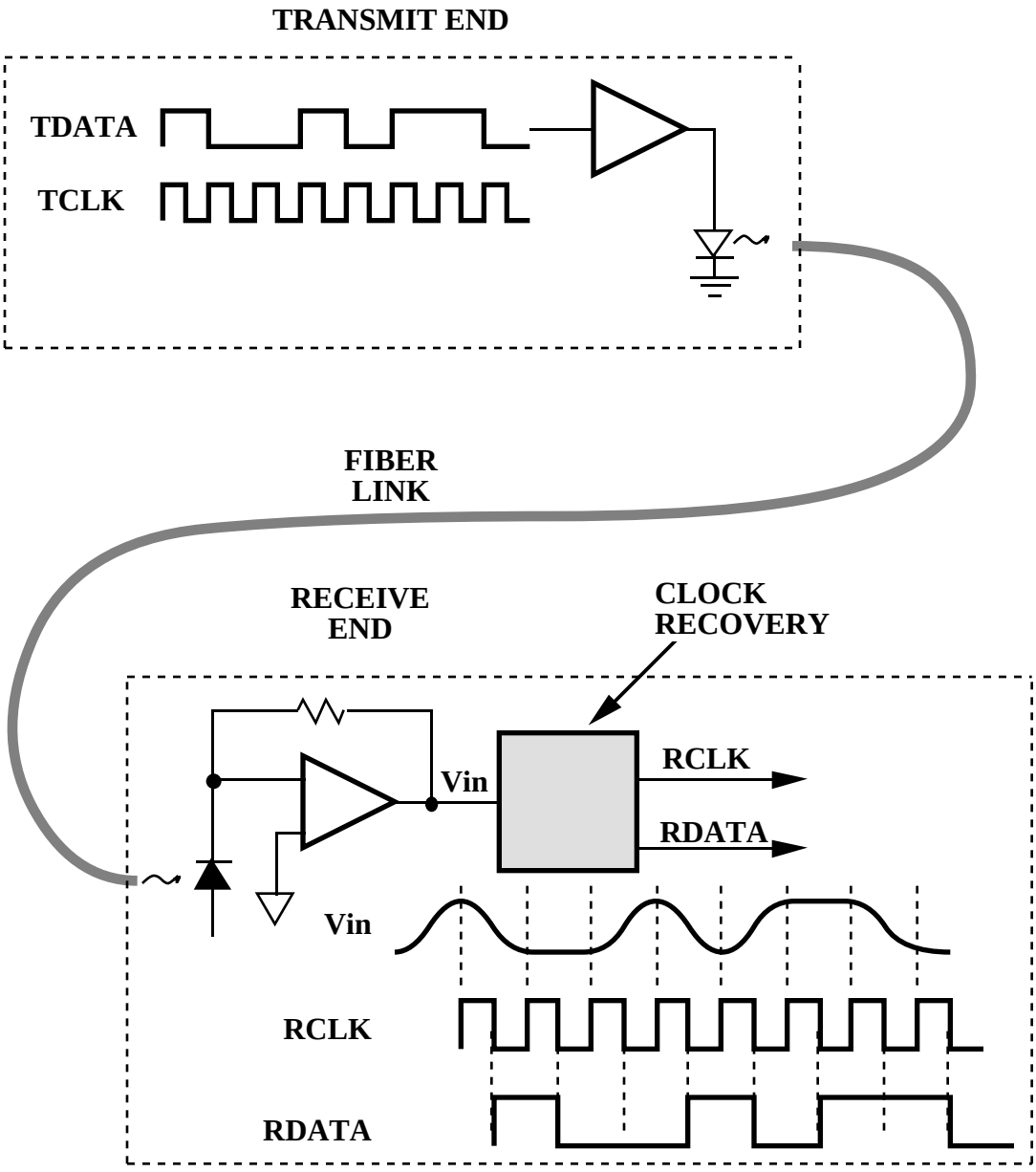


Figure 1.1.
Typical fiber optic serial data transmission system

In evaluating the BER performance of a data link, the end user must be concerned with many other possible influences on BER. Among other factors that can degrade system BER in a fiberoptic link are power loss and dispersion in the optical fiber, inadequate optical power input at the transmit end, and noisy optical-to-electronic conversion at the receive end.

To assess its contribution to BER, the clock recovery block can be tested independent of the link, as shown in Figure 1.2. The input is an ideal data waveform; the recovered clock is then compared to the transmit clock. If there were no jitter, the phase difference between the clocks would be constant (due only to static phase and propagation delay differences). In the presence of jitter, there is a distribution of phase differences. The standard deviation of this distribution σ_x is the end user's figure-of-merit for characterizing the jitter performance of the clock recovery block [93].

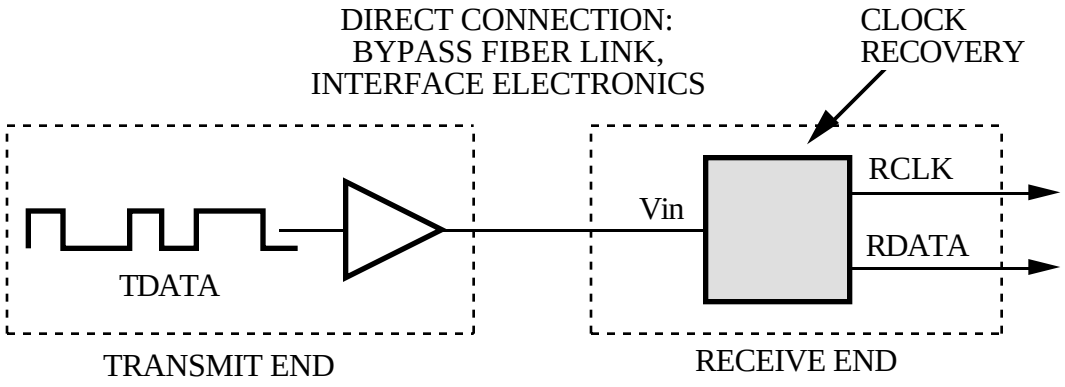


Figure 1.2.
Independent test of BER due to clock recovery function.

1.1.2 Methods of clock recovery

One method of recovering the bit clock is to apply the nonlinearly processed data waveform to a resonant circuit such as a surface acoustic wave (SAW) filter [13, 56]. Nonlinear processing is required since a non-return-to-zero (NRZ) data waveform has a spectral null at the bit frequency [60]. The disadvantage of this approach is that SAW filters are bulky (cannot be integrated) and expensive (of order $100).

An alternative approach for generating the recovered clock is to use a phase-locked loop (PLL) [13, 20, 58, 81]. This has the advantage of being integrable, and thus relatively inexpensive. This thesis will address design techniques for low jitter performance when a PLL is used for the clock recovery function.

The PLL that was the starting point for this work is the Analog Devices AD802. This PLL is designed for data reception at a frequency of 155.52 MHz. The jitter σ_x for transmission of pseudorandom data is approximately 50ps rms [93]. This is approximately 0.8% of a unit interval (UI).

1.1.3 Other Applications

Although this work was done with serial data transmission in mind, there are several other applications requiring low jitter performance from PLLs that perform a clock recovery function:

Disk drive clock recovery

Data is usually stored on magnetic media with no reference track to indicate bit boundaries. Therefore when data is read from the magnetic medium, there is a need to recover a clock signal from the data to determine the bit boundaries. (Encoding the data makes the clock recovery task somewhat easier than the NRZ data case). Low jitter is necessary since any increase in jitter increases read errors [53, 55, 59].

Generating high speed digital clocks on-chip

As digital processor and memory chips become capable of operating at clock rates exceeding 100 MHz, the problem of distributing such a high speed clock throughout a system becomes more difficult. One approach to solving this problem is to distribute a lower frequency clock, and multiply this clock to the higher frequency with an on-chip PLL [25, 36, 39, 40, 92]. Low jitter is necessary since any increase in jitter reduces timing margin for digital signals that rely on the clock.

Digital Audio

A PLL can be used to generate the high-speed clock required for delta-sigma A/D and D/A conversion in digital audio applications. Low jitter is necessary since phase noise on the clock can be aliased into the audio band to produce audible, objectionable artifacts in the reconstructed analog waveform [34, 35].

1.1.4 Summary

Many applications require low jitter PLL performance, characterized by the standard deviation of phase errors in the recovered clock σ_x. The work in this thesis grew out of the need to develop tools for low jitter PLL design, while always being able to relate jitter performance to the end user's figure of merit σ_x.

1.2 Phase and Jitter Concepts in PLL-based Clock Recovery

Figure 1.3 is a simplified block diagram of a PLL being used for clock recovery. The VCO generates the recovered clock RCLK. The phase detector compares transitions of RCLK to transitions of V_{in}, and generates an error signal proportional to the phase difference. The error signal is processed by the loop filter and applied to the VCO to drive the phase difference to zero. Ideally there is no phase error, and RCLK samples V_{in} at the exact center of the bit period, giving the minimum bit error rate.

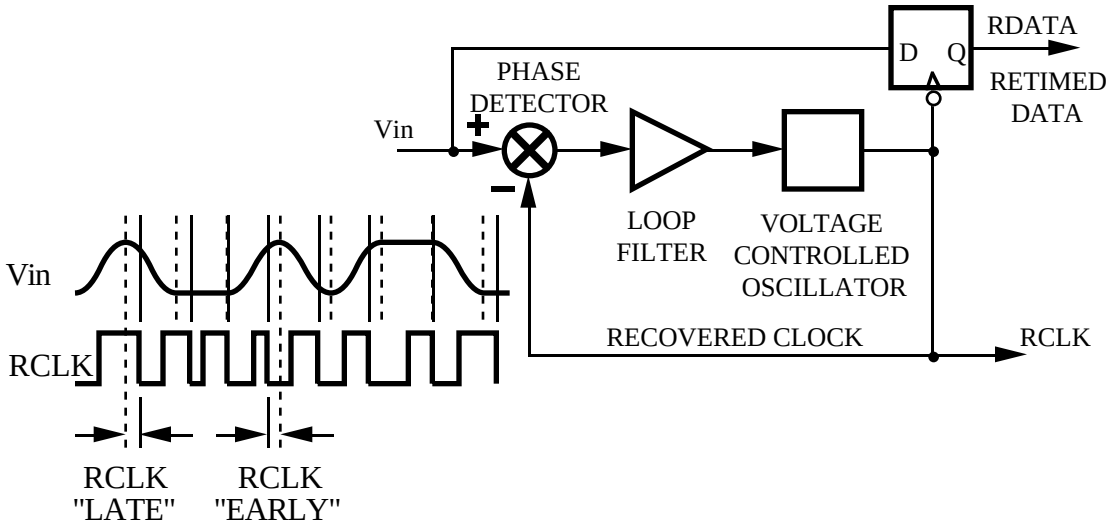


Figure 1.3. PLL used for clock and data recovery.

Any of the PLL components shown in Figure 1.3 can contribute to jitter [27, 43]. For example, design steps must be taken to ensure that the phase detector does not add data-dependent jitter [20]. When the phase detector and loop filter designs are optimized for low jitter, the remaining source of jitter is the VCO. The goal of this thesis is to achieve low jitter PLL performance by developing techniques for low jitter VCO design.

1.2.1 VCO and phase

Phase is simply a number - an angle - the argument of a trigonometric function. For example, in the case of an ideal sine waveform of amplitude V_o with constant frequency ω:

$$V(t) = V_o \sin(\underbrace{\omega t + \phi_o}_{\text{PHASE}}) \qquad (1\text{-}1)$$

Phase is simply the argument of the sine function, $\omega t + \phi_o$. Angle ϕ_o is an initial phase at the (arbitrary) time t=0.

Frequency is simply the time derivative of phase: that is, the rate at which phase changes with time. Conversely, phase is the integral of frequency. For example, in the case where frequency varies in time:

$$\phi(t) = \int_0^t \omega(t)dt + \phi_o \qquad (1\text{-}2)$$

A general VCO may be defined as shown in Figure 1.4. The input voltage V_{ctl} controls the output frequency ω_{out} ,which is given by

$$\omega_{out} = \omega_o + K_o \cdot V_{ctl} \qquad (1\text{-}3)$$

where ω_o is the center frequency and K_o is the voltage-to-frequency conversion constant (in units of rad/V· s).

Since phase is the integral of frequency, the phase at the VCO output can be obtained by integrating (1-3). Assuming the arbitrary initial phase ϕ_o to be zero, substituting (1-3) into (1-2) gives

$$\phi(t) = \int_0^t \omega_{out}(t)\ dt = \omega_o t + K_o \int_0^t V_{ctl}\, dt \qquad (1\text{-}4)$$

For example, consider the phase at the output of a free-running VCO with zero input, shown in Figure 1.5. The VCO runs at its center frequency ω_o, and phase increases uniformly in time as $\omega_o t$.

Now consider the case of Figure 1.6, where there is a white noise source at the VCO input. The phase at the VCO output is the integral of the white noise.

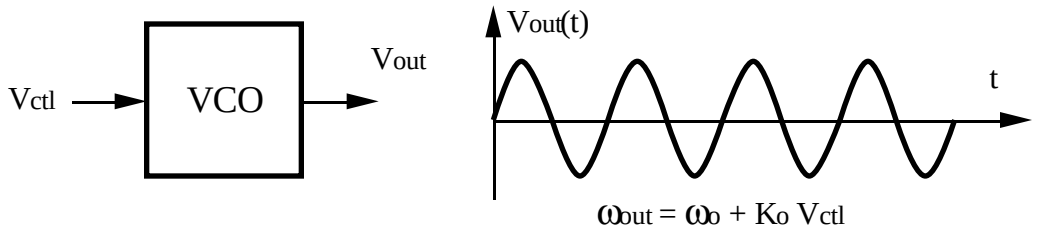


Figure 1.4. Definition of general VCO.

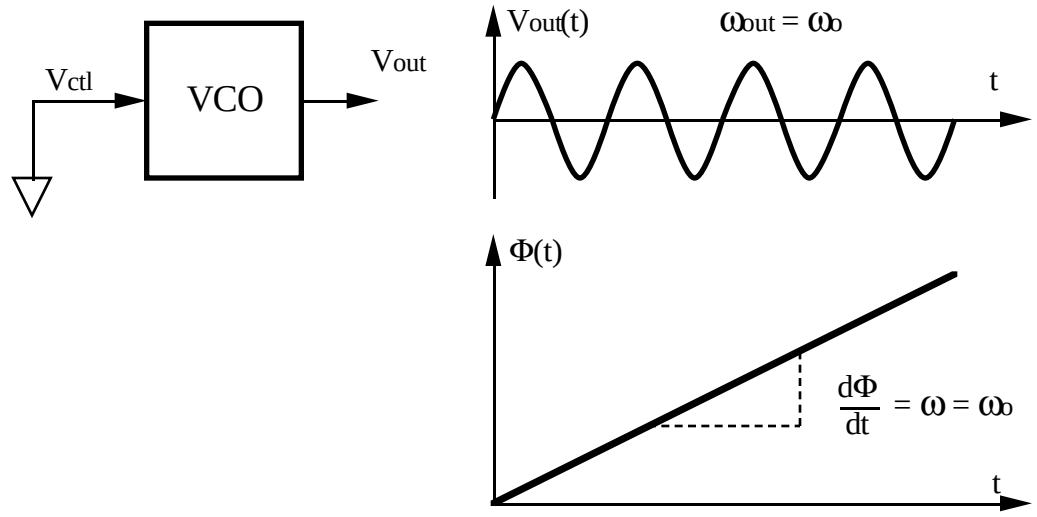


Figure 1.5. Ideal free running VCO.

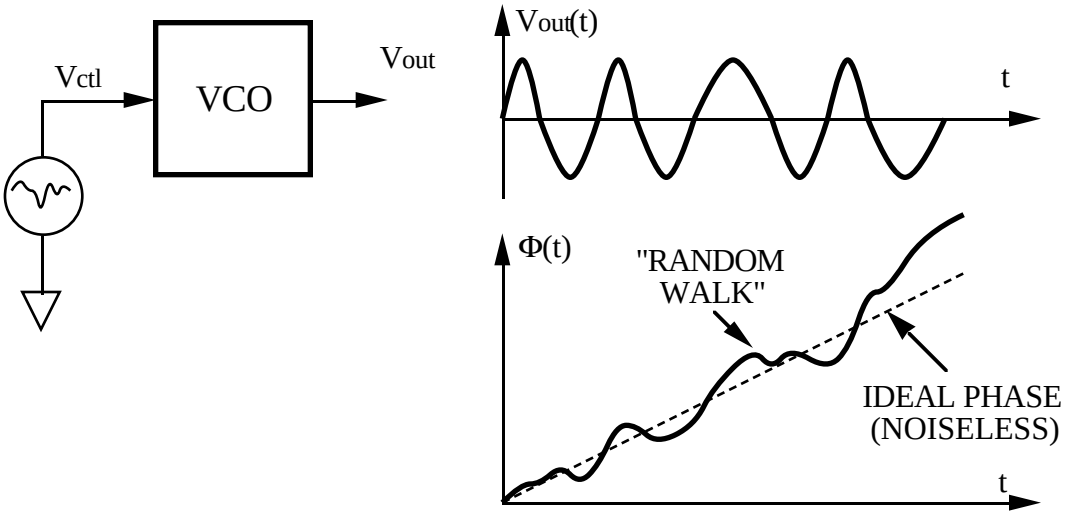


Figure 1.6. Free running VCO integrating white noise at input, giving "random walk" in phase.

As shown in the figure, the output phase executes a "random walk" about the ideal phase $\omega_o t$. The variance of this random walk increases with time, which means that the phase noise at the VCO output is nonstationary. In fact, the integration of frequency to get phase is perfect: over time there is no limit on the phase error.

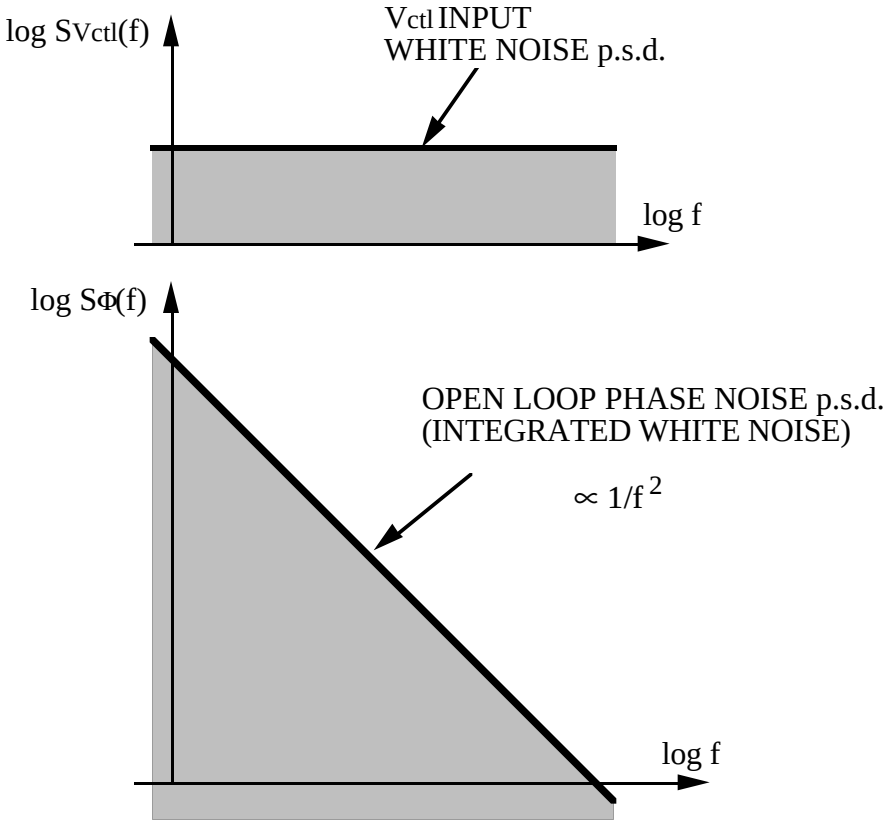


Figure 1.7. $1/f^2$ p.s.d. of integrated white noise.

Figure 1.7 shows how this nonstationarity is manifest in the (single sided) frequency domain. A white noise power spectrum is integrated to give an output phase power spectrum proportional to $1/f^2$. This nonstationarity prevents us from straightforwardly using the usual transform tools to move between the time and frequency domains. Any integral of phase noise power over all frequencies (zero to infinity) diverges due to the infinite power at zero frequency.

1.2.2 Response of PLL loop to input signal and VCO phase noise

Most work on phase noise in PLLs assumes that the dominant noise source is the poor signal-to-noise ratio at the PLL input [26, 27]. This is generally not the case in the applications we are concerned about. Usually a comparator is used to improve the amplitude resolution of the input signal threshold crossings. Therefore the signal-to-noise ratio at the PLL input is quite good and has little or no effect on jitter.

In this thesis we will assume that *the dominant source of jitter is the VCO*. Therefore we must be concerned with the phase transfer function from the VCO to the clock output. Following is a brief analysis of phase noise at the output due to the VCO.

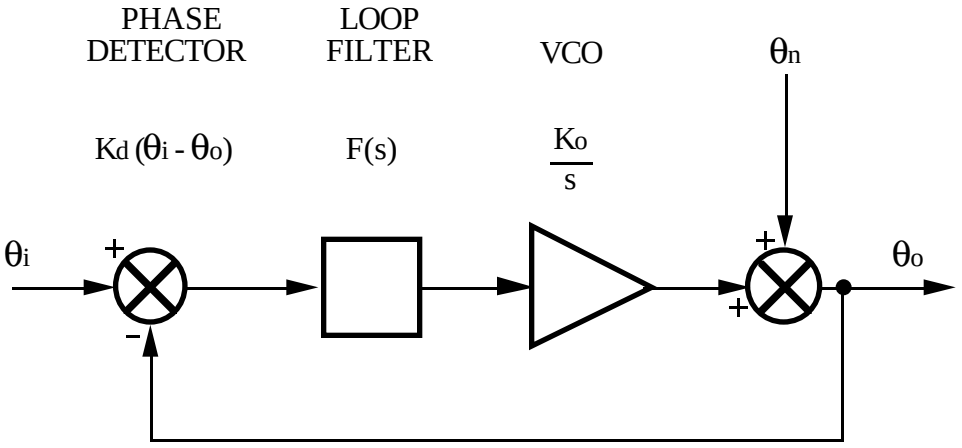


Figure 1.8. Phaselock loop as a control system.

Figure 1.8 shows a block diagram of the PLL as a control system, where the controlled variable is phase. θ_i is the input phase from the transmit clock that the PLL is trying to track. θ_o is the phase of the VCO output clock. θ_n represents the phase noise of the VCO referred to its output. K_d is the phase detector transfer function, in [V/rad]. K_o is the VCO transfer function, in [rad/V· s].

The signal transfer function $H_s(s)$ from θ_i to θ_o is

$$H_s(s) = \frac{\theta_o}{\theta_i} = \frac{K_d\, K_o\, F(s)}{s + K_d\, K_o\, F(s)} \tag{1-5}$$

The VCO output-referred phase noise transfer function $H_n(s)$ from θ_n to θ_o is

$$H_n(s) = \frac{\theta_o}{\theta_n} = \frac{s}{s + K_d\, K_o\, F(s)} \tag{1-6}$$

The loop filter usually consists of an integrator and a compensating zero [60]. After considering the effects of the loop filter (see Appendix A), the transfer functions (1-5) and (1-6) can be approximated as

$$H_s(s) = \frac{2\pi f_L}{s + 2\pi f_L} \tag{1-7}$$

$$H_n(s) = \frac{s}{s + 2\pi f_L} \tag{1-8}$$

where f_L is the loop bandwidth.

Figure 1.9 shows Bode plots of (1-7) and (1-8), which show the qualitative significance of the loop bandwidth f_L: The output phase of the PLL is able to follow input phase fluctuations that occur at a frequencies below f_L; input phase fluctuations at frequencies above f_L are attenuated at the output. Conversely, VCO phase noise that occurs at frequencies below f_L are attenuated at the output; VCO phase noise that fluctuates at frequencies above f_L are not affected by the loop and pass unattenuated to the output.

As mentioned in Section 1.2.1, θ_n can be represented by integrated white noise. When this is passed through the loop filter, the resulting power spectrum is the lowpass noise process shown in Figure 1.10.

Although the open loop VCO noise process is nonstationary, the process at the output of the closed loop VCO is stationary, due to shaping of the noise by the feedback loop. This means transform techniques can be used when the PLL loop is closed.

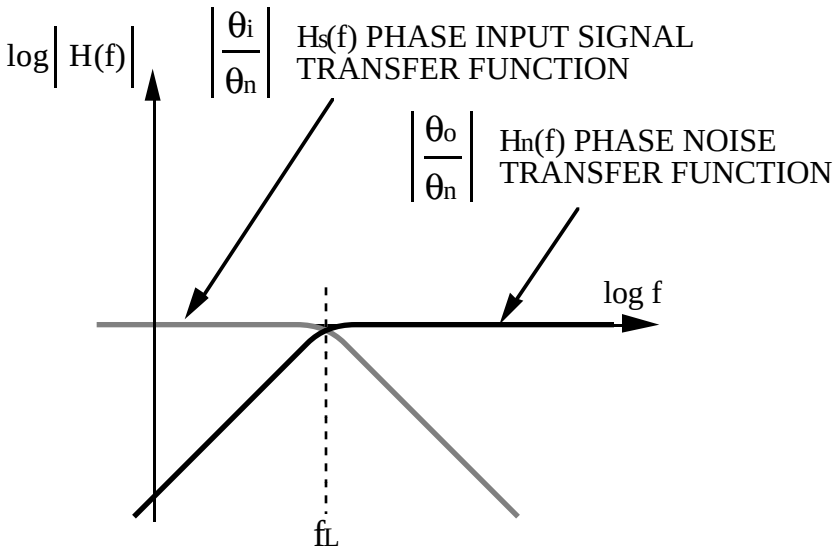


Figure 1.9. Phase signal and noise Bode plots.

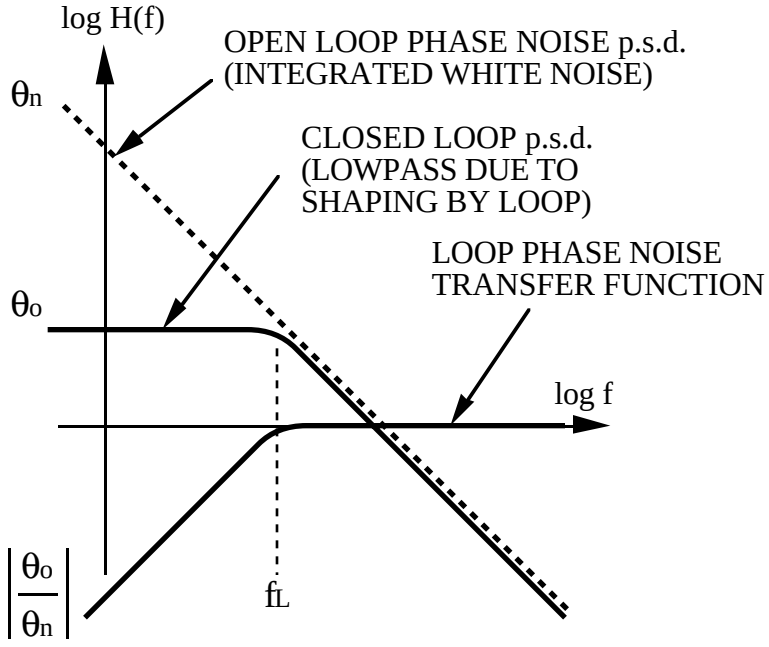


Figure 1.10. Lowpass process for shaped $1/^2$ noise.

For closed-loop operation, the work in this thesis assumes that *the PLL has already completed the acquisition process and characterization as a linear system about an operating point is valid*. In reality, acquisition is an extremely nonlinear process and must be aided by functional blocks (e.g. a frequency lock loop [20]) not shown in Figure 1.3. This assumption does not limit applicability of the results since jitter is not defined during acquisition.

The work in this thesis also assumes that *cycle slips never occur*. Cycle slips are a more "pathological" nonstationarity than $1/f^2$ noise, and make analysis extremely difficult if not impossible [26, 51]. Ignoring cycle slips does not limit applicability of the results since:

- Cycle slips are very rare when jitter is small compared to a bit interval, which is true in this case, and
- Data transmission is in discrete packets so a cycle slip error corrupts only a finite amount of data; the error can be detected and is not fatal.

1.2.3 Summary

In this thesis, we assume the VCO is dominant jitter source. An open loop VCO is a perfect phase integrator, so white noise at the voltage control input is integrated to give a nonstationary "random walk" in phase with a $1/f^2$ p.s.d. The usual transform tools cannot be applied to the open loop VCO.

When the loop is closed, we assume that acquisition is complete so a linearized loop model is valid. The action of the closed loop shapes the $1/f^2$ p.s.d., rolling it off below the loop bandwidth f_L. The shaped noise is stationary and transform tools may be used.

Cycle slips are not addressed in this thesis, but this is not a serious limitation on the applicability of the results.

1.3 Types of VCOs

This section briefly describes different types of VCOs that are used in clock recovery PLLs. They will be discussed in detail in Chapter 3.

1.3.1 LC/resonant

VCOs based on a resonant circuit (such as an LC tank or quartz crystal) are known to have excellent jitter performance [18, 19, 56, 64]. Analysis of noise in resonant-based VCOs is well developed in the literature [22, 30, 32, 57], and design techniques for realizing low jitter performance are relatively well understood.

Unfortunately the requirement of an off-chip tank or crystal defeats the purpose of integrating the PLL function. Actually, integrated inductors have been reported in the GHz frequency range [61]. Unfortunately these have low Q (of order 10) due to resistive losses, and in any case are not practical in the 100MHz to 1GHz frequency range.

1.3.2 Multivibrator

A multivibrator VCO can be fully integrable. Much work on multivibrator VCOs has concentrated on their potential for excellent linearity [29, 44, 73, 87, 88], which is an important requirement when the PLL is being used for measurement or to demodulate a PM or FM signal. However, linearity is not as critical a requirement in clock recovery.

Fully integrated clock recovery PLLs have been described using multivibrator VCOs [20, 41, 42, 70, 75]. Unfortunately, despite their excellent linearity, the jitter performance of multivibrators is known to be worse than harmonic oscillators. The literature contains some analysis of jitter in multivibrators [1, 77, 85], and some design techniques for improving jitter are available [74, 84, 86]. Nevertheless, there is a need for improvement of jitter beyond the best achieved by multivibrator VCOs

1.3.3 Ring oscillator

Voltage controlled ring oscillators have recently been explored as an alternative to the multivibrator for fully integrated, lower jitter clock recovery PLLs [5, 6, 13-15, 23, 24, 38, 45, 69, 89, 92]. Like the multivibrator, a ring oscillator is fully integrable. In addition, some of the empirical results show promise of excellent jitter performance [45]. These results, however, seem to have been achieved on an isolated, "cut-and-try" basis. There appears to have been no attempt to make a general understanding of jitter in ring VCOs. Indeed, a survey of the literature shows no theoretical analysis of jitter in rings, and thus no techniques for designing to achieve lower jitter in a ring oscillator.

1.3.4 Summary: Focus on ring oscillator design techniques

This thesis will focus on techniques for designing ring oscillators to achieve a desired (low) jitter. In particular, this thesis will address design questions such as:

- How is jitter affected by the number of delay stages in the ring? That is, at a given frequency, which is better for low jitter: many fast delay stages, or fewer slow delay stages?
- Within the delay stage itself, what affects jitter? That is, how should circuit parameters (such as bias currents, resistor values, etc.) be chosen to achieve a given desired jitter?
- What are the fundamental limits on jitter that can be achieved? That is, is there any simple relationship between jitter and system-level considerations such as power dissipation or complexity?

1.4 How to measure phase

We cannot measure phase directly; we can only observe a signal (usually voltage) which is a function of phase. This section introduces different ways of characterizing phase noise from observations of the voltage. Sections 1.4.1 through 1.4.4 give a qualitative introduction to various jitter and phase noise measurements in the time and frequency domains. A subset of these measurements will be developed more rigorously in Section 1.5.

σ_x is an advantageous figure-of-merit from the end user's point of view, since it "compresses" all information about jitter performance of the PLL into one (time domain) number. For the PLL designer, however, this compression is a disadvantage, since it obscures information about how to improve jitter performance. Fortunately for the designer, other measurement techniques can be used to characterize jitter in the time domain. Jitter can also be characterized and measured in the frequency domain, which is more appropriate for some applications and design tasks.

A design technique for low jitter PLLs should allow the designer flexibility to work in whatever domain (time or frequency) that gives the most insight into jitter performance. At the same time, the designer must always be able to relate jitter measures in different domains to the end user figure-of-merit, σ_x.

The remainder of this section describes general measurement techniques for characterizing jitter in the time and frequency domains. The goal is to use techniques that require only simple, widely available test equipment.

1.4.1 Phase measures in time and frequency domains

Although phase is a continuous time variable, it is often more convenient to measure it using a sampling approach: that is, to record the times when the phase of the waveform equals a known value. For example, as shown in Figure 1.11, when the voltage waveform crosses zero in a positive going direction we know the phase is a multiple of 2π. When there is no phase noise, frequency is constant, phase increases uniformly, and the zero crossing times are evenly spaced at intervals of the period $T_o = 1/f_o$.

In the presence of phase noise, as shown in Figure 1.12, the zero crossing times are not evenly spaced. We can characterize the phase noise by whatever is the most convenient of any of the following equivalent measures:

- variations in periods (frequency) from the ideal constant
- variations in phase from the ideal ramp
- variations in the zero crossing times from the ideal uniform series

Jitter can also be characterized in the frequency domain by the magnitude of sidebands of power spectrum near the "carrier" (center frequency) [66]. The frequency domain approach is the traditional one for measuring phase noise in a clock stability context [22, 67, 83, 100]. Although the PLL's performance is not directly specified in the frequency domain, understanding the frequency domain performance is important as guide to design for improved jitter. This is because, as mentioned in Section 1.2.2, the frequency response of the PLL loop filter shapes the open-loop phase spectrum of the VCO and determines the jitter of the recovered clock under closed-loop conditions.

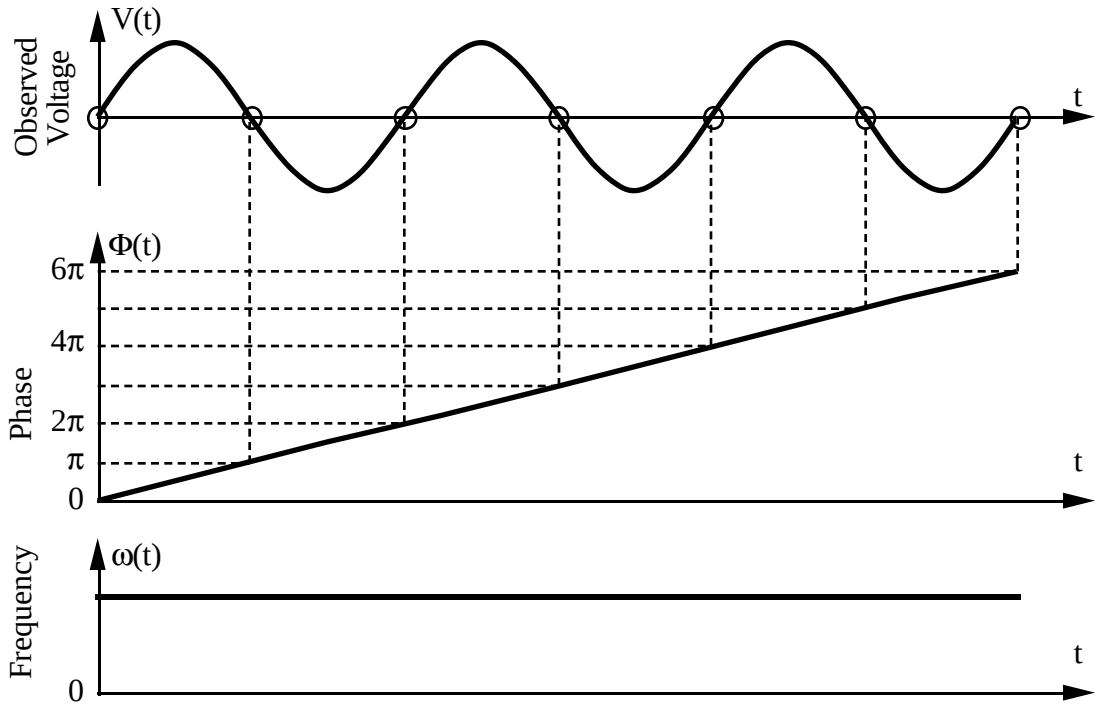


Figure 1.11. Ideal clock.

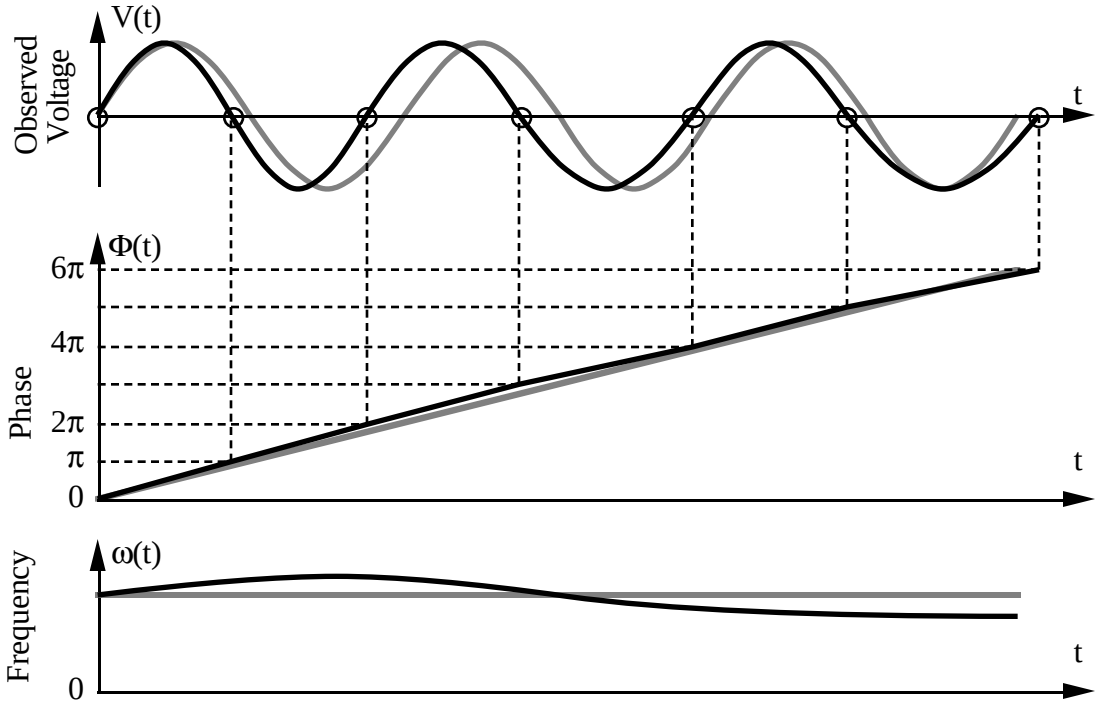


Figure 1.12. Clock with phase noise.

The phase noise power spectral density $S_\phi(f)$ is measured in the frequency domain using a spectrum analyzer or, for higher accuracy, a more expensive phase noise measurement system [97]. The measurement technique, shown in Figure 1.13, is straightforward: simply feed the clock into the spectrum analyzer. Appendix B shows that the resulting spectrum, if normalized to the carrier power, is equal to the spectrum $S_\phi(f)$ of the phase jitter process.

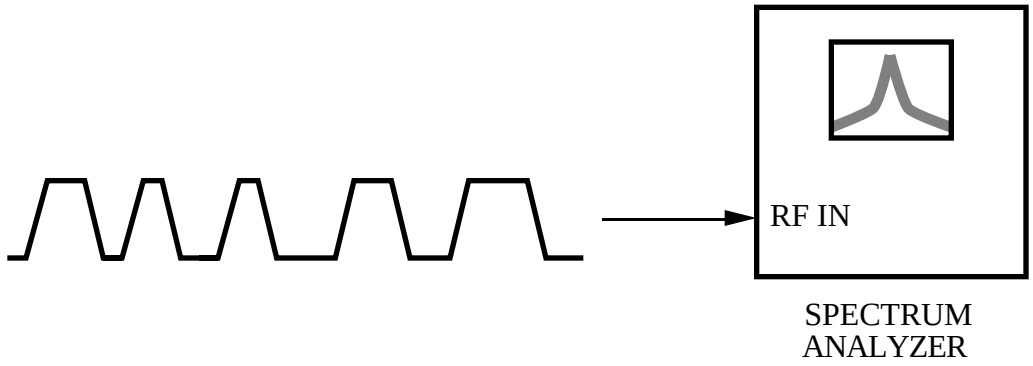


Figure 1.13. "Direct spectrum" measurement of phase noise.

1.4.2 Time domain: Two sample standard deviation

Most types of jitter can be characterized in the time domain by a two-sample standard deviation. This measurement can be made simply and accurately using a communications signal analyzer (CSA) [96]. This instrument measures the distribution of times between the threshold crossings of trigger and clock waveforms. This measurement can also be made, with more difficulty and less accuracy, by an oscilloscope with a delaying time base [33].

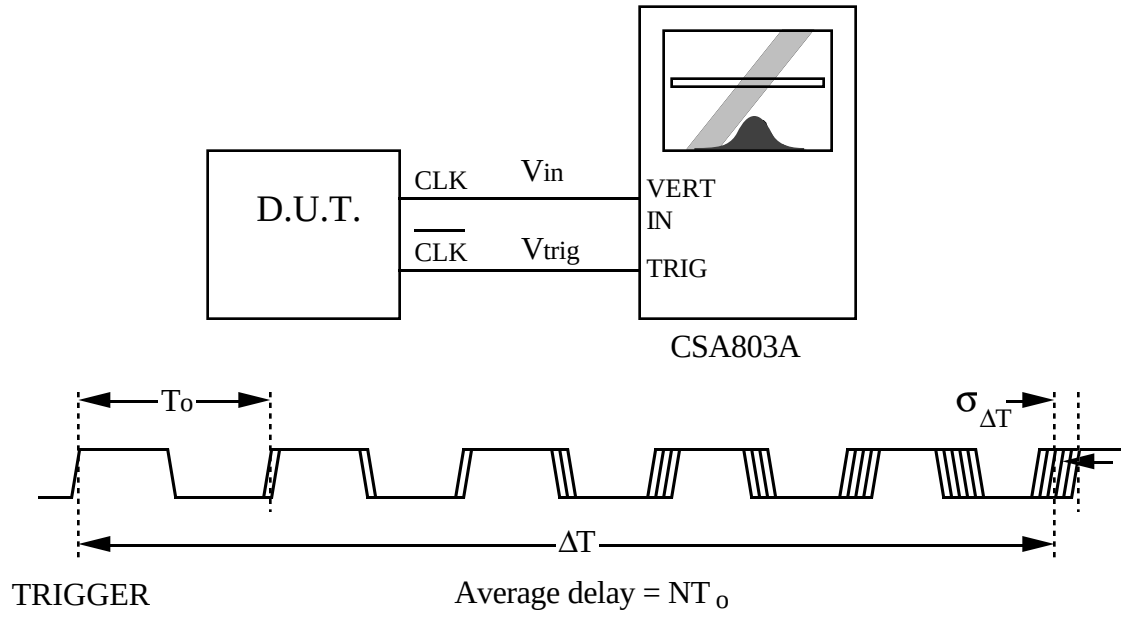


Figure 1.14. Jitter measurement over time delay ΔT.

Figure 1.14 shows the idea behind this method of measuring jitter. Input and trigger waveforms V_{in} and V_{trig} are applied to the CSA. A time "window" is defined at a delay ΔT after the triggering transition of V_{trig}. The CSA then compiles a histogram of threshold crossings of V_{in} that occur during this window. The standard deviation σ of this histogram is the result.

This two-sample standard deviation is used as the time domain jitter measure in this thesis. Different measures are obtained when different signals from the PLL are used for V_{in} and V_{trig}, with the PLL operating under different conditions.

Conditions for validity

Compiling this histogram takes a finite amount of time, usually of order seconds. If there is any drift in frequency during this time, (for example, due to thermal effects), then σ is not defined [67] and any attempt to measure a two-sample standard deviation will diverge. Drift is reduced by allowing sufficient time for device warm-up and thermal stabilization.

The CSA's internal time base is the reference which defines the interval ΔT. Therefore the jitter of this time base must be better than the clock under test. In practice, this is not a problem except at very long ΔT delays.

1.4.3 Other time domain measures

A disadvantage of the two sample standard deviation is that σ does not converge in the presence of nonstationary noise processes with frequency characteristic $1/f^n$ when $n>2$ [22]. This is most often a problem when long term frequency drift is present. For this reason a more robust statistic, called the Allan variance, has been developed [2]. There is an extensive literature relating the Allan variance to frequency domain performance.

A disadvantage of the Allan variance is that it requires at least three correlated time measurements and cannot be performed with the CSA. This conflicts with our goal of using only simple, commonly available test equipment. Therefore the Allan variance will not be used in this work.

There are many other less common time domain jitter measures that have been developed [52]. In general, like the Allan variance, these are more robust but require more complicated measurement instrumentation. For the purposes of this thesis the two-sample standard deviation is sufficiently robust and has the advantage of being reasonably simple to measure.

1.4.4 Frequency domain phase measures

Phase noise can also be characterized in the frequency domain. An ideal sine wave in the time domain corresponds to an ideal impulse in the (single sided) frequency domain, as shown in Figure 1.15.

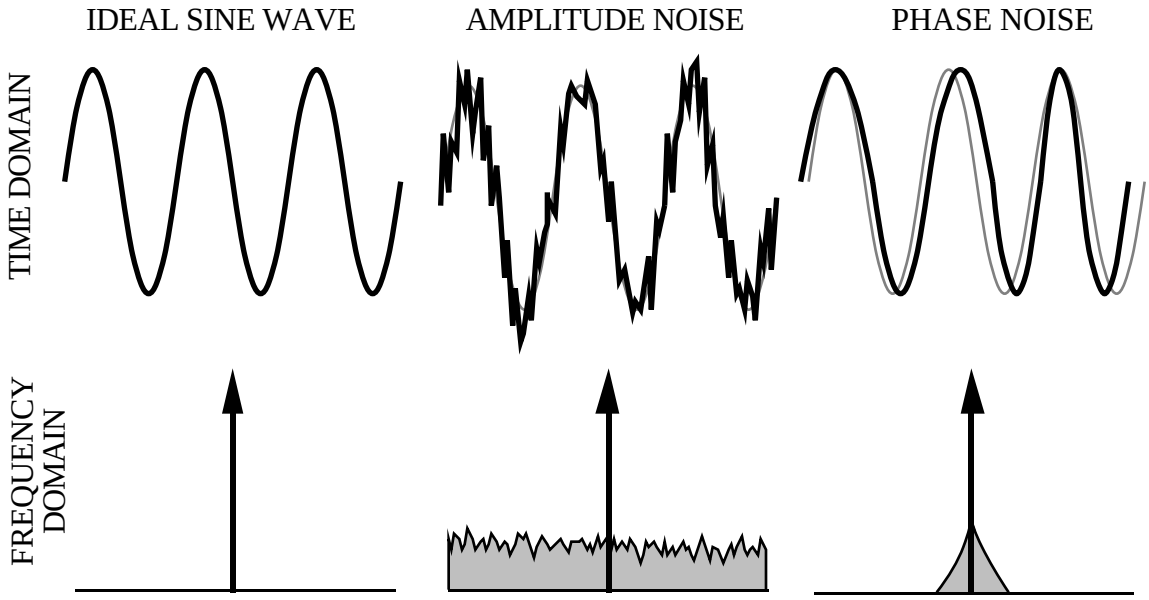


Figure 1.15. Clock jitter in time and frequency domains.

Consider the spectrum of an ideal sine wave with additive white noise, shown in Figure 1.15. The noise adds uncertainty to our measurement of the zero crossings of the waveform. We can imagine "cleaning up" the waveform with a bandpass filter. However, we will still have noise near the carrier. We can characterize the phase noise by the size and shape of the "close in" sidebands around the ideal impulse in frequency.

Actually, care must be taken in interpreting a spectrum. A magnitude spectrum "hides" information since there is no way to distinguish phase noise power from amplitude noise power. In practice, some form of limiting is used to remove amplitude fluctuations [66]. This ensures that only phase noise power is present in the waveform.

Conditions for validity

The phase noise of the spectrum analyzer's internal reference oscillator must be better than the oscillator under test. In practice, at the small offset frequencies where phase noise is measured, most spectrum analyzers have lower phase noise than multivibrator and ring oscillators.

Some spectrum analyzers may require a calibration factor when measuring the power density of noise (as opposed to spectral lines). This is because most spectrum analyzers measure amplitude with an envelope detector, which has different response to noise than to a pure spectral tone [99]. Some analyzers (such as the HP4195A [98]) automatically add the calibration factor when the display is set to units of noise density.

1.4.5 Summary

We cannot observe phase directly, but there are several ways of measuring phase and phase errors from an observable signal. These techniques can help the designer improve jitter by providing more information than the figure-of-merit σ_x. The general measures that will be addressed in this thesis are the two-sample standard deviation in the time domain, and the phase noise power spectral density in the frequency domain. Both of these measurements can be made in a straightforward fashion with commonly available telecommunications test equipment, an important point for the practicing designer.

1.5 Measures that will be related in this thesis

In addition to the time or frequency domain options for measurement, jitter can also be measured with the PLL open or closed loop. Figure 1.26 summarizes five different measurement techniques, all of which will be related to one another by this work. Following is a more detailed discussion of each of these techniques and their advantages and disadvantages.

1.5.1 Case (i): Frequency domain, VCO open loop

Measurement Technique

The open loop VCO spectrum is measured as shown in Figure 1.16. The free-running VCO output is applied to the spectrum analyzer input. The resulting spectrum, normalized to the carrier power, is $S_{\phi OL}(f)$.

Result

With the VCO operating open loop, $S_{\phi OL}(f)$ as measured on the spectrum analyzer has the characteristic shown in Figure 1.17. Since the VCO integrates phase noise, the noise power increases as $1/f^2$, where f is the offset from the center frequency. We can fit the measurement to a characteristic

$$S_{\phi OL}(f) = \frac{N_1}{f^2} \tag{1-9}$$

to define a frequency domain figure of merit N_1.

Advantage

This is a simple, quick test to obtain frequency domain figure of merit N_1.

Disadvantage

It is not immediately apparent that the frequency domain figure of merit N_1 is related to our ultimate design goal: the end user's time domain figure of merit σ_x.

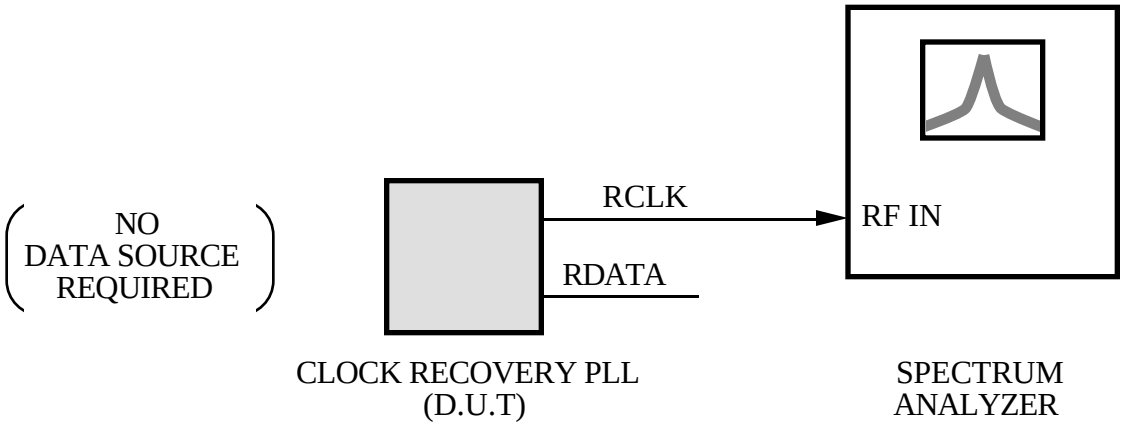


Figure 1.16. Measurement technique:
Frequency domain, open loop.

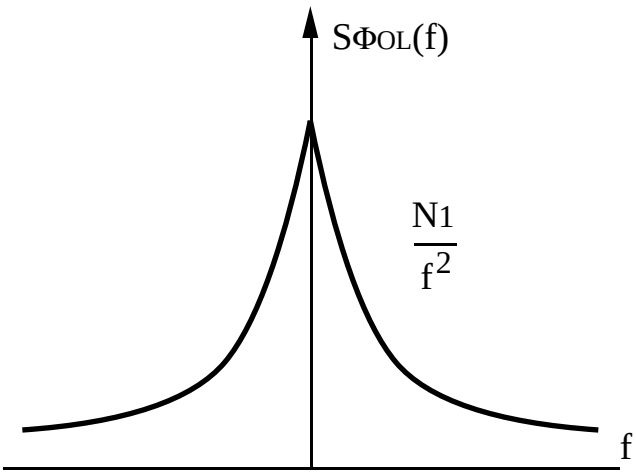


Figure 1.17. Measurement result:
Frequency domain, open loop.

1.5.2 Case (ii): Frequency domain, PLL closed loop

Measurement Technique

The closed loop VCO spectrum is measured as shown in Figure 1.18. The PLL is locked to a data source; the VCO output is applied to the spectrum analyzer input. The resulting spectrum, normalized to the carrier power, is $S_{\phi CL}(f)$.

Result

When the loop is closed around the VCO, $S_{\phi CL}(f)$ is given by the sum of jitter contributions from the transmit clock and the VCO, as shaped by loop filter. Assuming that the jitter of the transmit clock is negligible, the VCO will be the dominant contributor of phase noise at all offset frequencies [65]. $S_{\phi CL}(f)$ will have the characteristic shown in Figure 1.19. This is simply the closed loop phase noise power spectrum of Figure 1.10 translated to the carrier frequency. Since the PLL loop drives the VCO to track the transmit clock, the noise power levels off at offset frequencies below the loop bandwidth. As shown in Figure 1.10, the leveling off is due to the noise p.s.d. rolling up at the same rate as the noise transfer function rolls down.

Advantage

The effect of loop bandwidth on jitter in readily apparent in the frequency domain.

Disadvantage

The spectrum is not directly indicative of end user's time domain figure of merit σ_x.

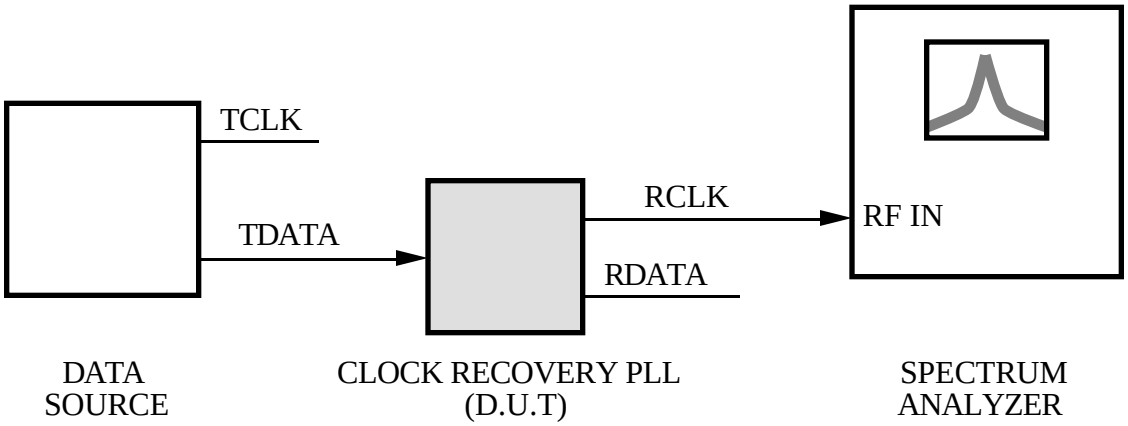


Figure 1.18. Measurement technique:
Frequency domain, closed loop.

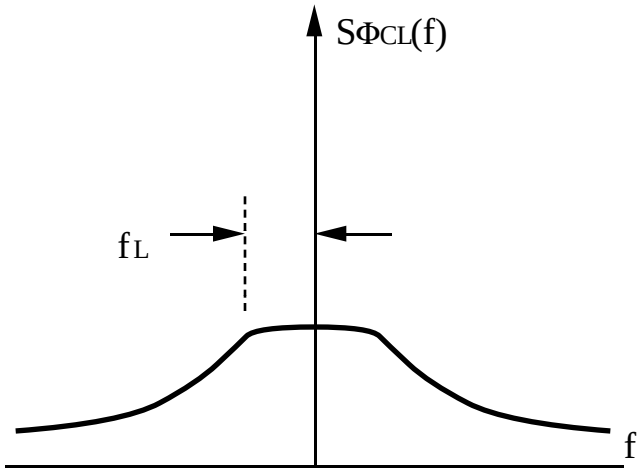


Figure 1.19. Measurement result:
Frequency domain, closed loop.

1.5.3 Case (iii): Time domain, closed loop, transmit clock referenced

Measurement technique

This measurement is made as shown in Figure 1.20. The transmit clock TCLK is used as the CSA trigger V_{trig}; the recovered clock RCLK is observed as the CSA input V_{in}. In the presence of jitter, a distribution of threshold crossing times is observed. The CSA records a histogram of this distribution as shown in Figure 1.21.

Result

The standard deviation of the distribution of threshold crossing times of RCLK, referenced to TCLK, is σ_x.

Advantage

This measurement gives the end user's figure of merit σ_x. This test is a simple, quick indicator of how well the PLL performs the clock recovery function.

Disadvantage

This test requires that the transmit clock be available at the receive end of the link. While this is not a problem in a laboratory test, in the field the transmit clock may be at the other end of several kilometers of optical fiber.

This test also requires the PLL to be operating closed loop. VCO design and simulation would be simplified if we could consider the VCO by itself (open loop), while being able to predict the closed loop σ_x.

While this test has the advantage of being simple and quick, it provides little information on improving jitter if σ_x is not satisfactory.

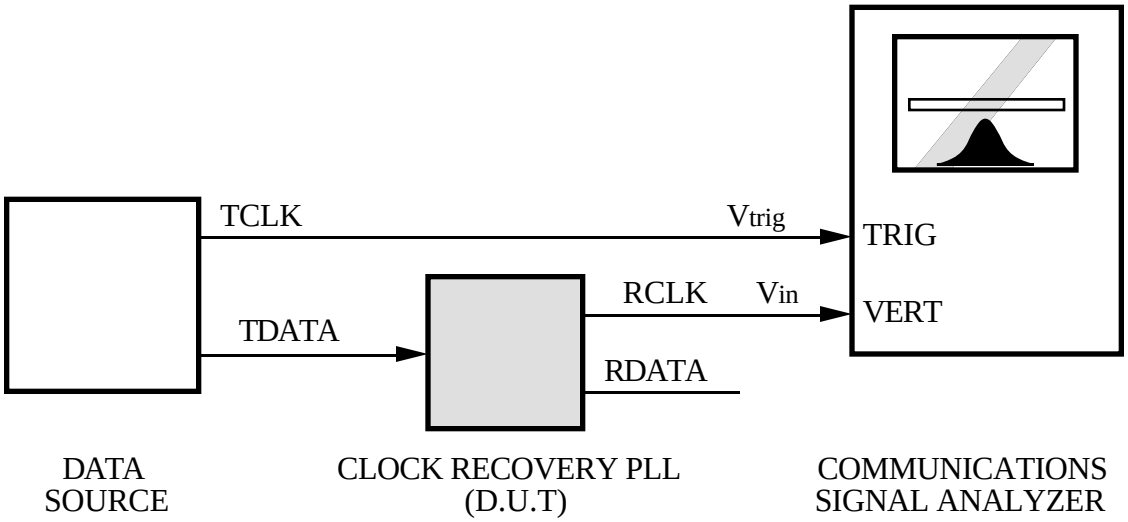


Figure 1.20. Measurement technique:
Time domain, closed loop, transmit clock referenced.

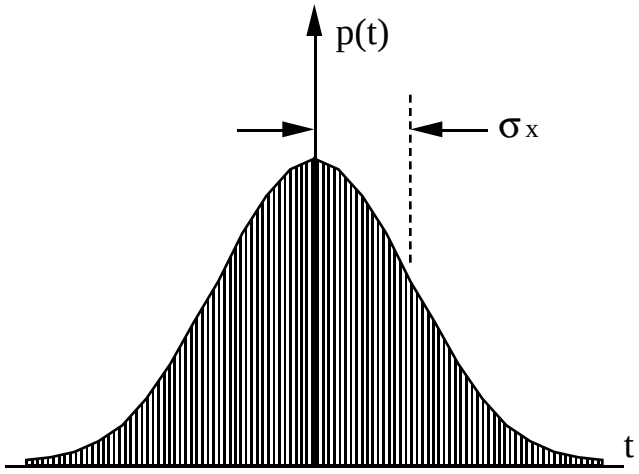


Figure 1.21. Measurement result:
Time domain, closed loop, transmit clock referenced.

1.5.4 Case (iv): Time domain, closed loop, self referenced

Measurement technique

This measurement is made as shown in Figure 1.22. The recovered clock is used as both the trigger and the input to the CSA. The CSA compares the phase difference between transitions in the clock waveform, separated by a delay ΔT derived from the CSA's internal time base. As in the previous case, a distribution of threshold crossing times is observed.

Result

In this measurement technique, however, the standard deviation $\sigma_{\Delta T}$ from the mean phase is observed to depend on the delay ΔT. The standard deviations $\sigma_{\Delta T(CL)}(\Delta T)$ can be plotted as a function of delay ΔT; a plot of the form as shown in Figure 1.23 results. Note that, unless otherwise specified, all time domain jitter plots in this thesis are on log-log axes. Jitter may be quantified by the standard deviation at one delay, or more completely by the functional relationship between $\sigma_{\Delta T(CL)}$ and ΔT.

Advantage

This measurement requires access only to the recovered clock and thus can be made even if the transmit clock is inaccessible. Also, the plot of $\sigma_{\Delta T(CL)}$ vs. ΔT provides more information than the single number σ_x.

Disadvantages

This test requires the PLL to be operating closed loop. Also, the accuracy of the $\sigma_{\Delta T(CL)}$ vs. ΔT plot may be degraded by the jitter of the CSA time base, especially for large ΔT.

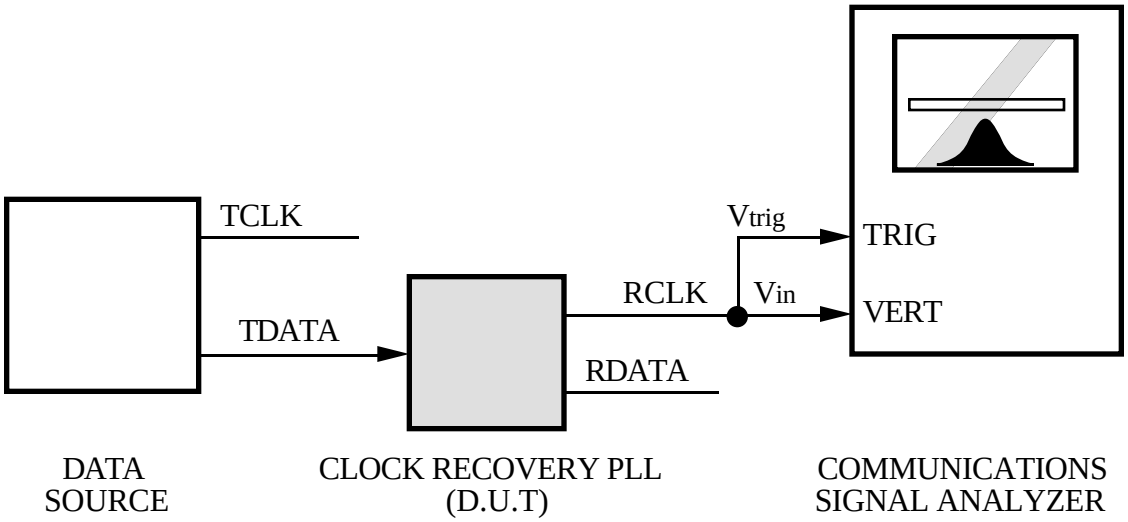


Figure 1.22. Measurement technique:
Time domain, closed loop, self referenced.

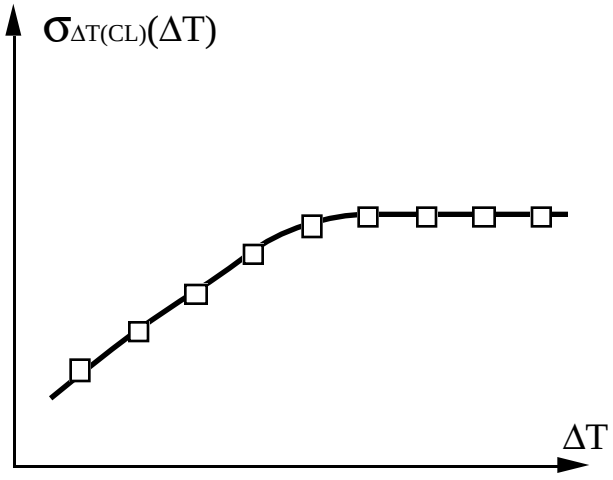


Figure 1.23. Measurement result:
Time domain, closed loop, self referenced.

1.5.5 Case (v): Time domain, open loop, self referenced

Measurement technique

This measurement is made as shown in Figure 1.24. The test is similar to that shown in Figure 1.22, except that the PLL loop is opened so that the VCO free runs.

Result

Again, the standard deviations $\sigma_{\Delta T(OL)}(\Delta T)$ are plotted as a function of delay ΔT; in this case a plot of the form as shown in Figure 1.25 results. We will see that, for a process that can be approximated in the frequency domain by equation (1-9), the plot of $\sigma_{\Delta T(OL)}(\Delta T)$ vs. ΔT will take the form

$$\sigma_{\Delta T(OL)}(\Delta T) \approx \mathcal{K}\sqrt{\Delta T} \qquad (1\text{-}10)$$

where the proportionality factor $\mathcal{K}$ is a time domain figure of merit.

Advantages

No transmit clock or data source is required. The VCO can be measured and analyzed in isolation. Again the plot of $\sigma_{\Delta T(OL)}(\Delta T)$ vs. ΔT provides more information than the single number σ_x.

Disadvantages

It is not immediately apparent that the time domain figure of merit $\mathcal{K}$ is related to the end user's time domain figure of merit σ_x. Also, as in Section 1.5.4, accuracy is limited by the jitter of the CSA time base for large ΔT.

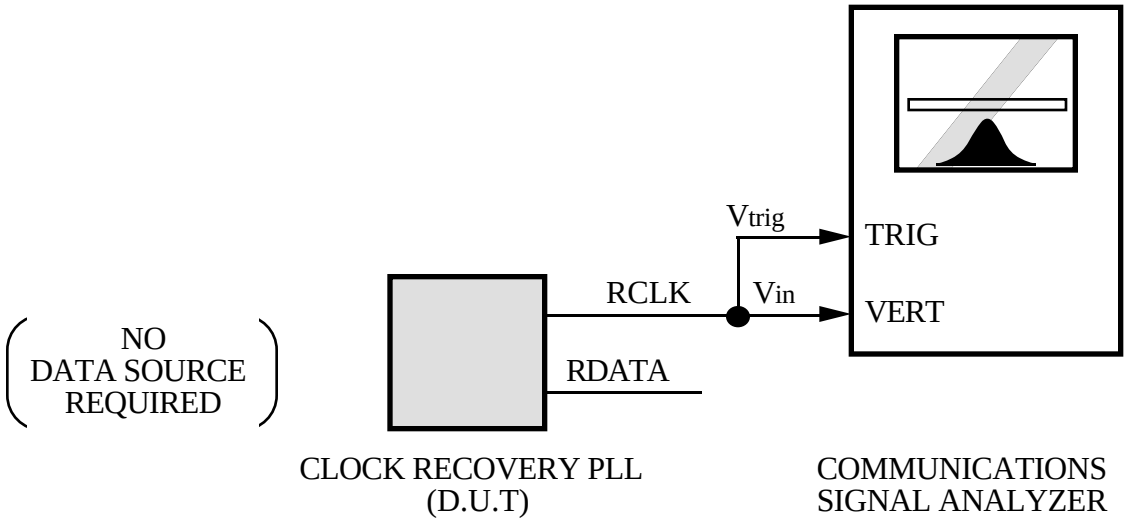


Figure 1.24. Measurement technique:
Time domain, open loop, self referenced.

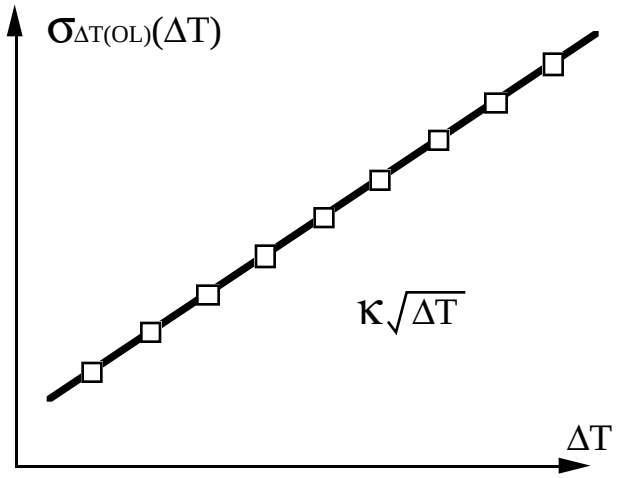


Figure 1.25. Measurement result:
Time domain, open loop, self referenced.

1.5.6 Summary

Five techniques are presented for measuring VCO contribution to PLL jitter, each with its own advantages and disadvantages. Figure 1.26 summarizes these techniques. In general, open loop measures have the advantages of being simpler and more relevant to the task of stand-alone VCO design, but have the disadvantage of being apparently unrelated to the end user's figure-of-merit σ_x. In general, closed loop measures have the advantage of being closely related to σ_x, but have the disadvantage of forcing the designer to consider the entire PLL rather than focusing only on stand-alone VCO design.

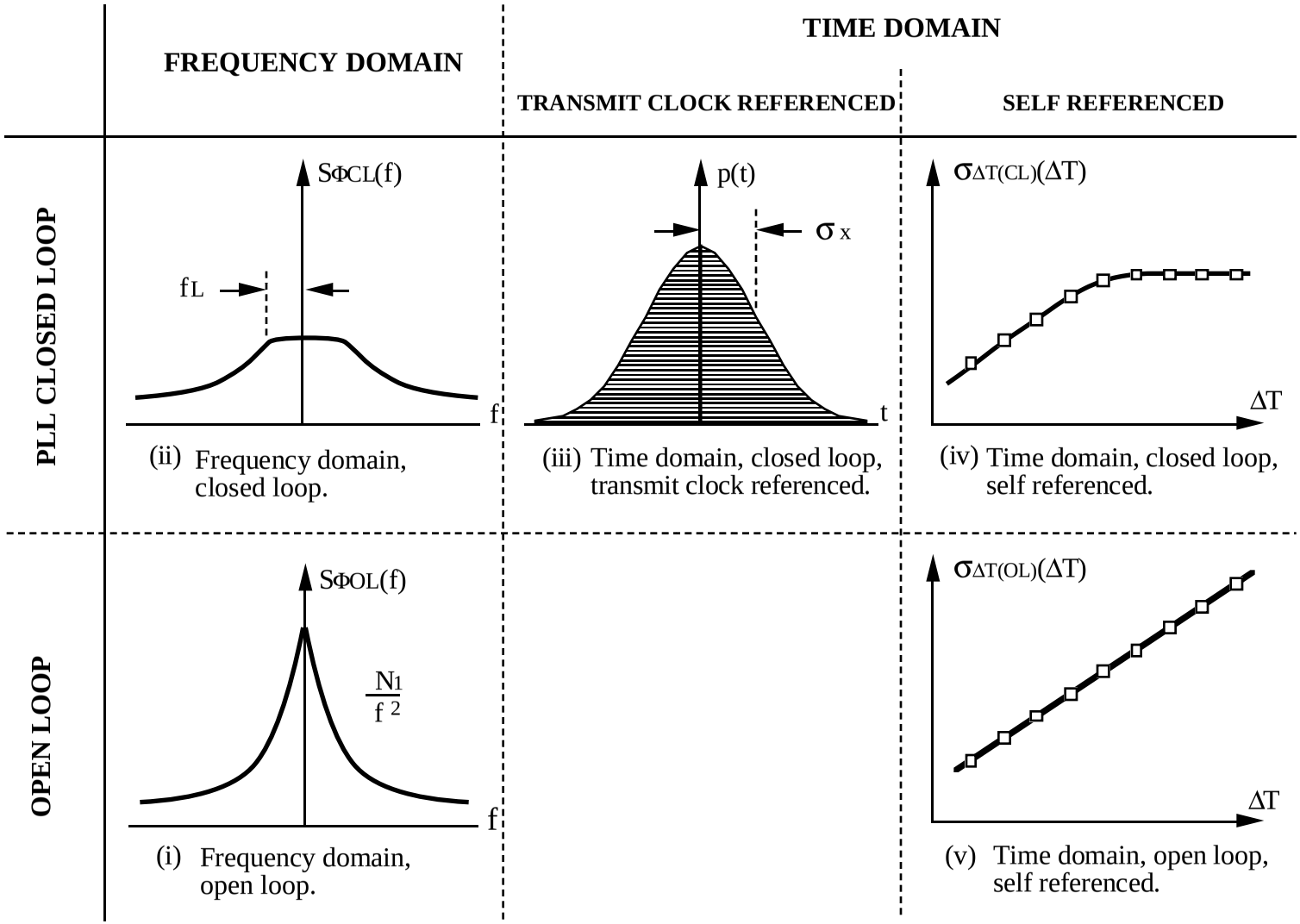


Figure 1.26. Summary of jitter measurement techniques.

1.6 Motivation and goals of this work

There are many applications for low jitter, PLL-based clock recovery. Fully integrated PLLs have a substantial cost and size advantage over PLLs requiring off-chip resonant elements. Ring oscillators have shown promise in low jitter applications, but there are no tools available to predict and design for jitter in ring oscillators.

1.6.1 Goals

Thus the primary goal of this thesis:

Develop design tools for ring VCO jitter

These tools would answer design questions posed in Section 1.3.4 regarding ring architecture, circuit design, and fundamental limits on jitter.

To ease design, the tools should also allow flexibility to work in whichever domain of Figure 1.26 gives the most insight, while relating to the final figure of merit σ_x. For example, although σ_x is defined in the time domain, insight for guiding some design decisions (e.g., effects of the loop filter and aliasing of noise sources [11, 86]) is more apparent in the frequency domain.

A secondary related goal is:

Simulation of PLL jitter

Once we have a tentative design, it is desirable to have a simulation tool to verify that design before going to the expense of fabricating silicon. Although we have modeled the PLL as a linear system, the VCO itself is a nonlinear circuit. Meaningful jitter simulation requires transient analysis with explicit noise sources [10]. Such a simulation is intractable with the full PLL circuit but is possible for the open loop VCO. Again, this requires relating performance measures from the different domains of Figure 1.26.

Achieving these goals requires:

Technique for relating time / frequency, open / closed loop jitter measures

A technique for relating jitter measures from the various domains identified in Figure 1.26 enables simplified design and simulation of a low jitter VCO. The difficulty is that design and simulation are easiest on the stand-alone, open loop VCO - where nonstationary noise precludes the use of transform tools to move between the time and frequency domains. The ultimate concern is the jitter of the closed loop PLL system. With this time/frequency technique the designer can work in whatever domain is easiest while still being able to accurately predict performance when measured by the end user.

1.6.2 Other benefits

Although the techniques in this thesis are developed for PLL ring VCO design, they are applicable to any oscillator with a $1/f^2$ p.s.d. This will be demonstrated in Chapter 4 where the time/frequency technique of Chapter 2 is applied to a harmonic oscillator spectrum and gives the same result as previous analysis.

This work also aids evaluation of actual devices. For example, in the AD802 we can open the PLL loop, set the VCO to a fixed frequency, and measure the stand alone, open loop VCO performance. From this measurement we can predict what the closed loop performance should be if limited only by the VCO jitter. Then we can compare this prediction with actual measurements to determine if other components (such as the phase detector or loop filter) are degrading the closed loop performance.

1.6.3 Summary

Chapter 2 will develop the time/frequency, open/closed loop jitter technique. In Chapters 4-6, the technique is used to develop design tools for ring VCOs at various levels of detail. The applications of these principles to simulation is implicit in the results presented in Chapters 4-6, as well as in Appendix I.

2. Technique for relating time / frequency domain jitter measures

2.1 Theoretical development

The contribution of this chapter is a mathematical technique for linking all of the performance measures shown in Figure 1.26. Note that the performance measures in the "open loop" portion of the figure correspond to nonstationary phase noise processes. This is shown in the unbounded standard deviation as delay time goes to infinity in Figure 1.25, and the nonconvergent noise power integral as offset frequency goes to zero in Figure 1.17.

Following is the derivation of these mathematical relationships.

2.1.1 Case (i): Frequency domain, VCO open loop

When the PLL loop is opened and the VCO is free running, we assume the phase noise power spectral density to be dominated by integrated white noise. With this assumption, the p.s.d. $S_{\phi OL}(f)$ at the VCO output can be modeled by

$$S_{\phi OL}(f) = \frac{N_1}{f^2} \qquad (2\text{-}1)$$

where f is the offset frequency from the "carrier" (VCO free-running frequency) [66]. The value of N_1 for a particular VCO can be determined from a spectrum analyzer measurement. Since (2-1) goes to infinity as f approaches zero, the integral of phase noise power over all frequencies does not converge. This makes sense intuitively, since the phase error of an open loop oscillator can wander arbitrarily far in its "random walk."

The spectrum analyzer measures in power density in units of [W/Hz]. This must be normalized relative to the carrier power [W], to give $S_{\phi OL}(f)$ expressed in units of [rad^2/Hz] or dBc/Hz (power below carrier). N_1 has dimensions of $rad^2 \cdot$ Hz.

2.1.2 Case (ii): Frequency domain, PLL closed loop

From Section 1.2.2 and Figures 1.9 and 1.10, however, we see that the effect of the loop filter is to make the closed loop p.s.d. of the form

$$S_{\phi CL}(f) = \frac{N_1/f_L^2}{1 + (f/f_L)^2} \qquad (2\text{-}2)$$

where f_L is the loop bandwidth, which is known by design.

2.1.3 Case (iii): Time domain, closed loop, transmit clock referenced

Under the $1/f^2$ dominated approximation, with the PLL loop closed, the phase noise process is stationary. Equation (2-2) can be integrated over all frequencies to give the variance (average power) of the jitter process, which gives the end user's measure of jitter performance, σ_x:

$$\int_{-\infty}^{+\infty} S_{\phi CL}(f) = \int_{-\infty}^{+\infty} \frac{N_1/f_L^2}{1 + (f/f_L)^2} = \frac{N_1\,\pi}{f_L} = \sigma_x^2 \qquad (2\text{-}3)$$

$$\sigma_x = \sqrt{\frac{N_1\,\pi}{f_L}} \quad \text{[rad rms]} \qquad (2\text{-}4)$$

Note the dimensions of the quantities in (2-4): when $S_{\phi CL}(f)$ is normalized to the carrier power level, and N_1 is in units of $rad^2 \cdot Hz$; then σ_x is in rms radians of phase error. This can be expressed in seconds rms by normalizing to the carrier frequency f_o:

$$\sigma_x = \frac{1}{2\pi f_o}\sqrt{\frac{N_1\,\pi}{f_L}} = \frac{1}{f_o}\sqrt{\frac{N_1}{4\pi\, f_L}} \quad \text{[s rms]} \qquad (2\text{-}5)$$

2.1.4 Case (iv): Time domain, closed loop, self referenced

There is also an indirect Fourier transform relationship between (2-2) and the plot of jitter as a function of delay in the self referenced time domain measurement.

An analysis of the jitter process in Appendix C shows that

$$\sigma_{\Delta T(CL)}^2 = 2 (\sigma_x^2 - R_{xx}(\Delta T)) \qquad (2\text{-}6)$$

where $\sigma_{\Delta T(CL)}$ is the self-referenced jitter (in radians rms) at a delay of ΔT and $R_{xx}(\Delta T)$ is the autocorrelation of the jitter process. By the Wiener-Khinchine theorem, $R_{xx}(\Delta T)$ is directly related to the p.s.d. of equation (2-2) by a Fourier transform. Applying the Fourier transform pair

$$\frac{2\tau}{1 + (2\pi f\tau)^2} \Leftrightarrow \exp(-|t|/\tau) \qquad (2\text{-}7)$$

to the p.s.d. in (2-2) gives

$$R_{xx}(\Delta T) = F^{-1} \left\{ \frac{N1/f_L^2}{1 + (f/f_L)^2} \right\} = \frac{N1\ \pi}{f_L} \exp (-2\ \pi\ f_L\ |\Delta T|) \qquad (2\text{-}8)$$

Substituting (2-8) into (2-6), and using (2-3) for σ_x^2, gives an expression for the closed-loop, self-referenced jitter $\sigma_{\Delta T(CL)}$ as a function of delay ΔT:

$$\sigma_{\Delta T(CL)}^2 = 2\ \sigma_x^2 (1 - \exp(- 2\pi\ f_L\ \Delta T)) \qquad (2\text{-}9)$$

$$\sigma_{\Delta T(CL)} = \sqrt{2}\ \sigma_x \sqrt{1 - \exp(- 2\pi\ f_L\ \Delta T)} \qquad (2\text{-}10)$$

where the absolute value of ΔT is no longer required since we only consider positive delays.

2.1.5 Case (v): Time domain, open loop, self referenced

Now all that remains is to link (2-10) with the open loop plot of $\sigma_{\Delta T(OL)}$. From the spectrum analyzer results, we see that the open loop spectrum can be considered to be the limiting case of the closed loop spectrum as f_L approaches zero. Using the Taylor series expansion of exp(x) and assuming x small,

$$\exp(x) = 1 + x + \frac{x^2}{2} + ... \approx 1 + x \qquad (2\text{-}11)$$

the limit of (2-9) as f_L approaches zero is

$$\sigma_{\Delta T(OL)}^2 = 4\,\pi\,\sigma_x^2\; f_L\,\Delta T \qquad (2\text{-}12)$$

Using the result of (2-3) for σ_x^2 gives an expression for the open-loop, self-referenced jitter $\sigma_{\Delta T(OL)}$ as a function of delay ΔT:

$$\sigma_{\Delta T(OL)}^2 = 4\pi^2\, N_1\,\Delta T \qquad (2\text{-}13)$$

$$\sigma_{\Delta T(OL)} = 2\pi\,\sqrt{N_1\,\Delta T} \quad \text{[rad rms]} \qquad (2\text{-}14)$$

Note that since N_1 is in units of $rad^2 \cdot Hz$, $\sigma_{\Delta T(OL)}$ as given by (2-14) is in radians rms. Expressing (2-14) in terms of seconds rms gives

$$\sigma_{\Delta T(OL)} = \frac{\sqrt{N_1\,\Delta T}}{f_o} \quad \text{[s rms]} \qquad (2\text{-}15)$$

From (2-15) we see that jitter is proportional to the square root of delay. This proportionality constant can be considered a figure of merit in the time domain, just as N_1 is a figure of merit in the frequency domain. This time domain proportionality constant will be called κ and is defined as:

$$\sigma_{\Delta T(OL)} = \kappa\sqrt{\Delta T} \qquad (2\text{-}16)$$

Expressing (2-15) in the form of (2-16) gives

$$\kappa = \frac{\sigma_{\Delta T(OL)}}{\sqrt{\Delta T}} = \frac{\sqrt{N_1}}{f_o} \quad [\sqrt{s}\,] \qquad (2\text{-}17)$$

Thus the link is established from the open loop frequency domain jitter measure $S_{\phi OL}(f)$ (characterized by the parameter N_1) to the open loop time domain measure $\sigma_{\Delta T}$ (characterized by the parameter κ). Figure 2.1 shows the equations linking the performance measures of Figure 1.26.

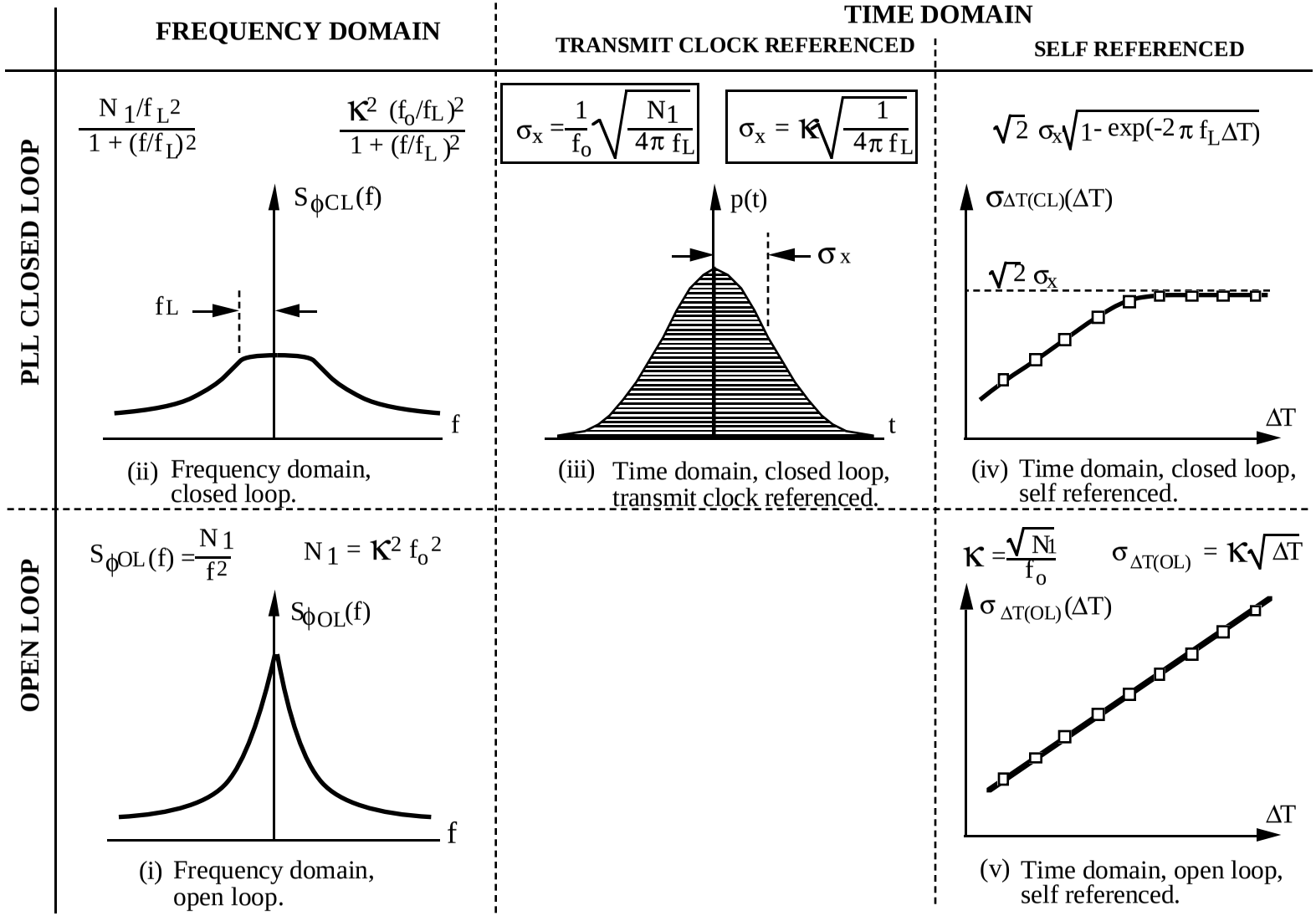


Figure 2.1. Mathematical relationships among jitter measurement techniques.

2.2 Experimental verification

In this section, the relationships developed in Section 2.1 are verified experimentally. These measurements were made using a Tektronix CSA803 communications signal analyzer [96] and a Hewlett-Packard HP4195A spectrum analyzer [98]. When set to output results in units of noise power density (dBm/Hz), the HP4195A automatically compensates for peak/noise effects mentioned in Section 1.4.4. The data acquisition software used to generate the figures in this section is described in Appendix D.

2.2.1 PLL with multivibrator VCO

In this section, the device under test is the Analog Devices AD802 clock recovery phase locked loop [93]. The AD802 uses a multivibrator-type VCO.

Figure 2.2 shows a spectrum analyzer plot for the free running VCO. The superimposed plot corresponds to a best-fit N_1 value to (2-1) for this data of

$$N_{1(meas)} = 98.1 \text{ rad}^2/\text{Hz} \qquad (2\text{-}18)$$

which gives a good fit to (2-1). Given the measured f_o = 158.1 MHz, the predicted value for the time domain figure of merit κ is given by (2-17):

$$\kappa_{(pred)} = \frac{\sqrt{N_1}}{f_o} = \frac{\sqrt{98.1\text{rad}^2/\text{Hz}}}{158.1\text{MHz}} = 6.27\text{E-}08\ [\sqrt{\text{s}}\,] \qquad (2\text{-}19)$$

Figure 2.3 shows a spectrum analyzer plot for the VCO running closed loop. The data input was a pseudorandom bit stream. The loop bandwidth under this condition was measured to be 109 kHz. The superimposed curve is the predicted p.s.d. based on (2-2) with f_L = 109kHz. Again, good qualitative agreement is seen.

Figure 2.2. AD802 Open loop spectrum.

Figure 2.3. AD802 Closed loop spectrum.

Figure 2.4. AD802: Time domain, closed loop, transmit clock referenced.

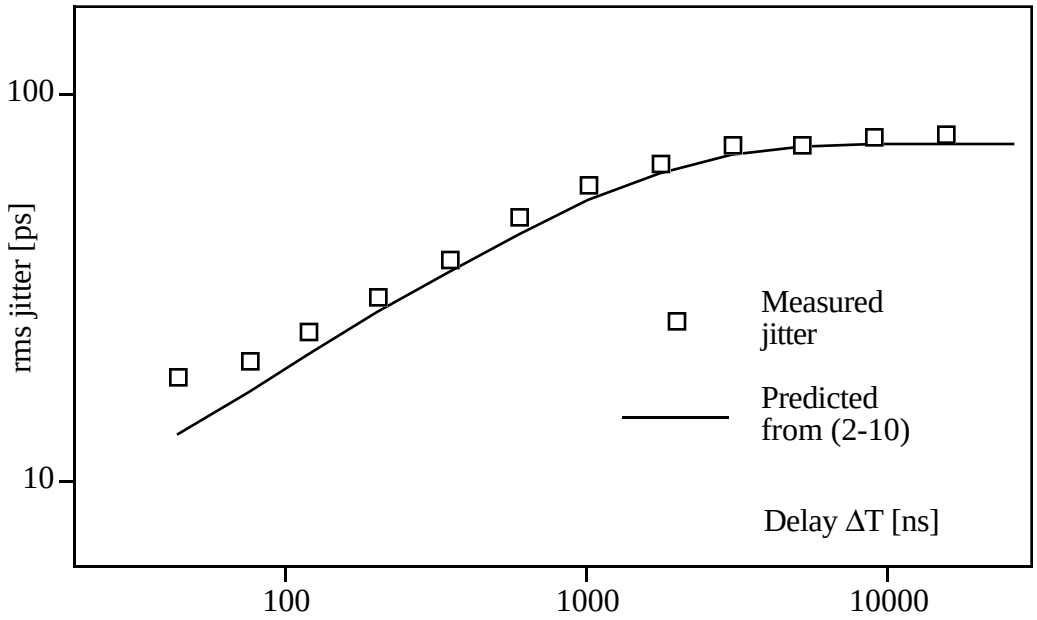


Fig. 2.5. AD802: Time domain, closed loop, self referenced.

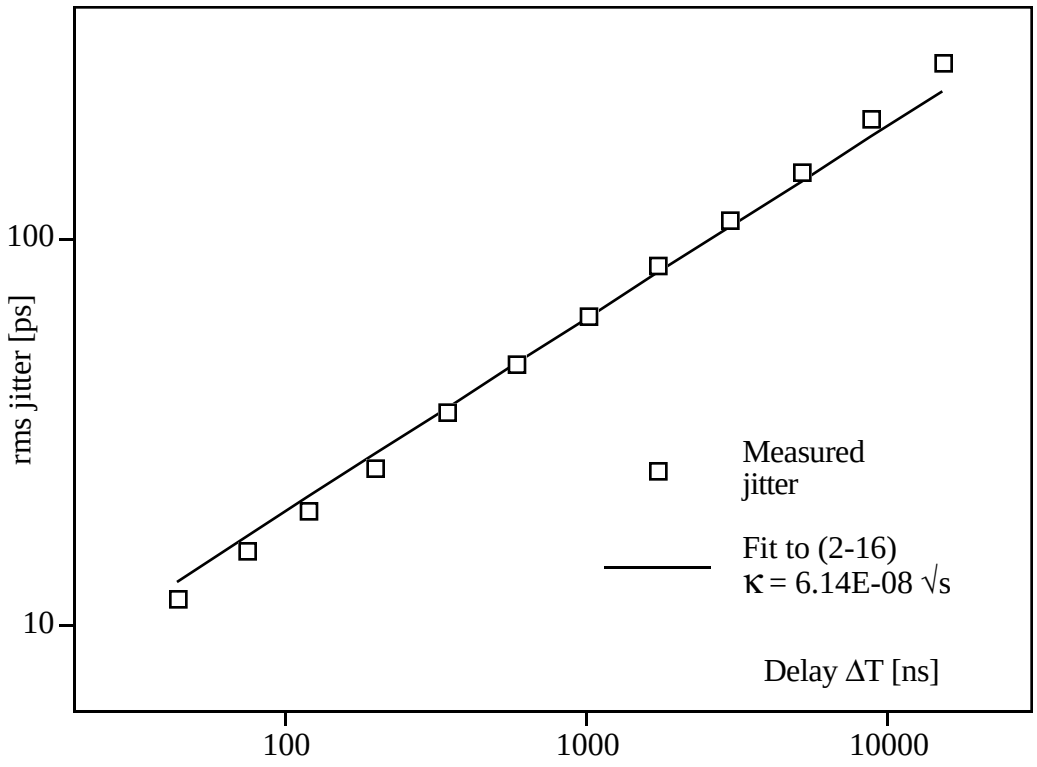


Fig. 2.6. AD802: Time domain, open loop, self referenced.

Figure 2.4 shows the measured jitter $\sigma_{x(meas)}$ of 54.3 ps rms. The predicted value from (2-5) (with f_o = 155.52 MHz since the closed loop VCO is locked to the transmit clock) is

$$\sigma_{x(pred)} = \frac{1}{f_o}\sqrt{\frac{N_1}{4\pi\, f_L}} = \frac{1}{155.52\text{MHz}}\sqrt{\frac{98.1\ \text{rad}^2/\text{Hz}}{4\pi\ 109\text{kHz}}} = 54.4\ \text{ps rms} \quad (2\text{-}20)$$

which is within 1% of the $\sigma_{x(meas)}$ measured with the CSA.

Figure 2.5 shows the measured closed-loop, self-referenced plot of jitter $\sigma_{\Delta T(CL)}$ vs. delay ΔT. The solid line is the predicted characteristic of (2-10). Agreement is within a few percent except at short delays.

Figure 2.6 shows the measured plot of self-referenced jitter with the VCO running open loop. The superimposed plot corresponds to a best-fit $\mathcal{K}$ value to (2-16) for this data of

$$\mathcal{K}_{(meas)} = 6.14\text{E-}08\ \sqrt{s} \quad (2\text{-}21)$$

This is within 2% of the $\mathcal{K}_{(pred)}$ value determined from the open-loop frequency domain p.s.d. in (2-19).

2.2.2 Ring VCO

In this section, the device under test is a 4 stage ring VCO. The circuit schematic is shown in Figure 2.7. Since there is no PLL involved only open-loop measurements are compared.

Figure 2.8 shows the spectrum analyzer plot for the free running VCO. The superimposed plot corresponds to a best-fit N_1 value to (2-1) for this data of

$$N_{1(meas)} = 12.4 \text{ rad}^2/\text{Hz} \tag{2-22}$$

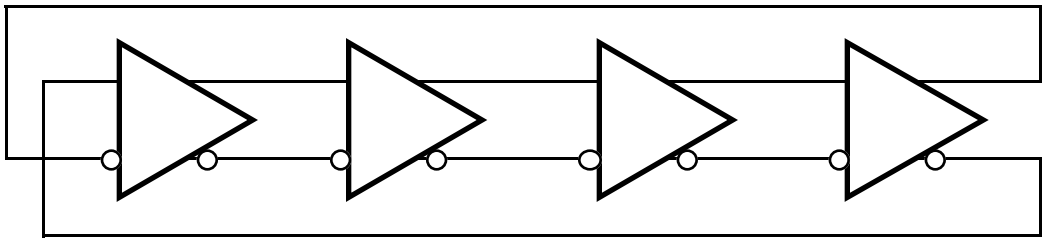
which gives a good fit to (2-1). The predicted value for the time domain figure of merit κ is given by (2-17),

$$\kappa_{(pred)} = \frac{\sqrt{12.4\text{rad}^2/\text{Hz}}}{153.85\text{MHz}} = 2.29\text{E-}08\ [\sqrt{\text{s}}\ ] \tag{2-23}$$

Figure 2.9 shows the measured self-referenced clock stability plot of jitter with the VCO running open loop. The superimposed plot corresponds to a best-fit κ value to (2-16) for this data

$$\kappa_{(meas)} = 2.37\text{E-}08\ \sqrt{\text{s}} \tag{2-24}$$

This is within 4% of the $\kappa_{(pred)}$ value determined from the open-loop frequency domain p.s.d. in (2-23).



EACH GATE:

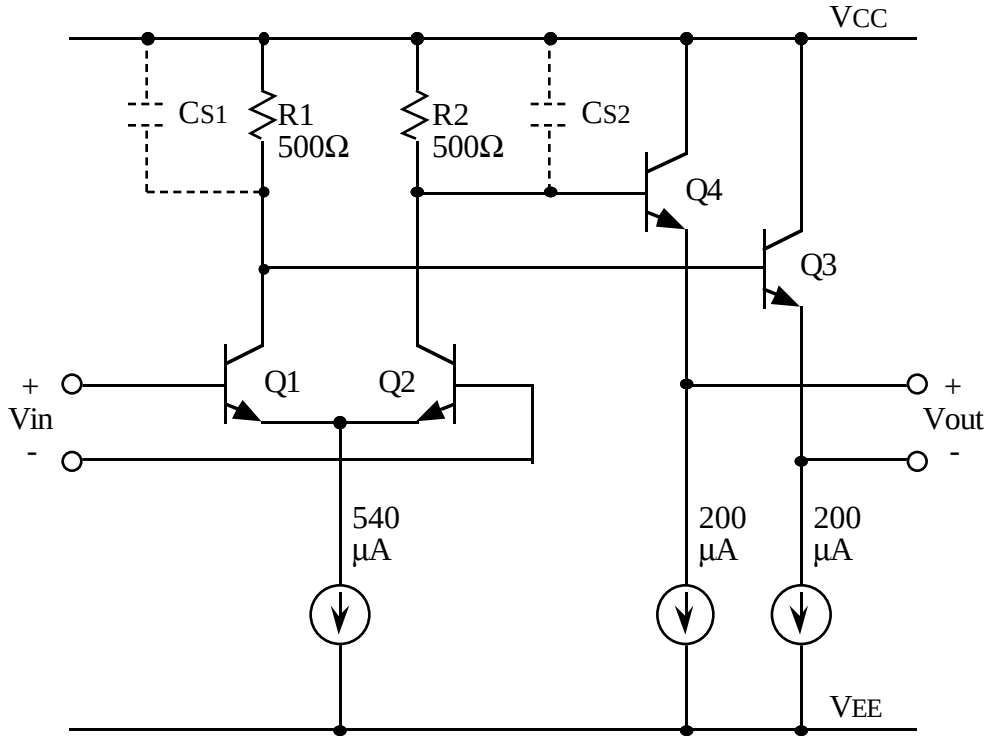


Figure 2.7. 4 stage ring VCO schematic.

Horizontal scale: 200 kHz/div (Logarithmic scale)

Fig. 2.8. 4 stage ring VCO: frequency domain, open loop.

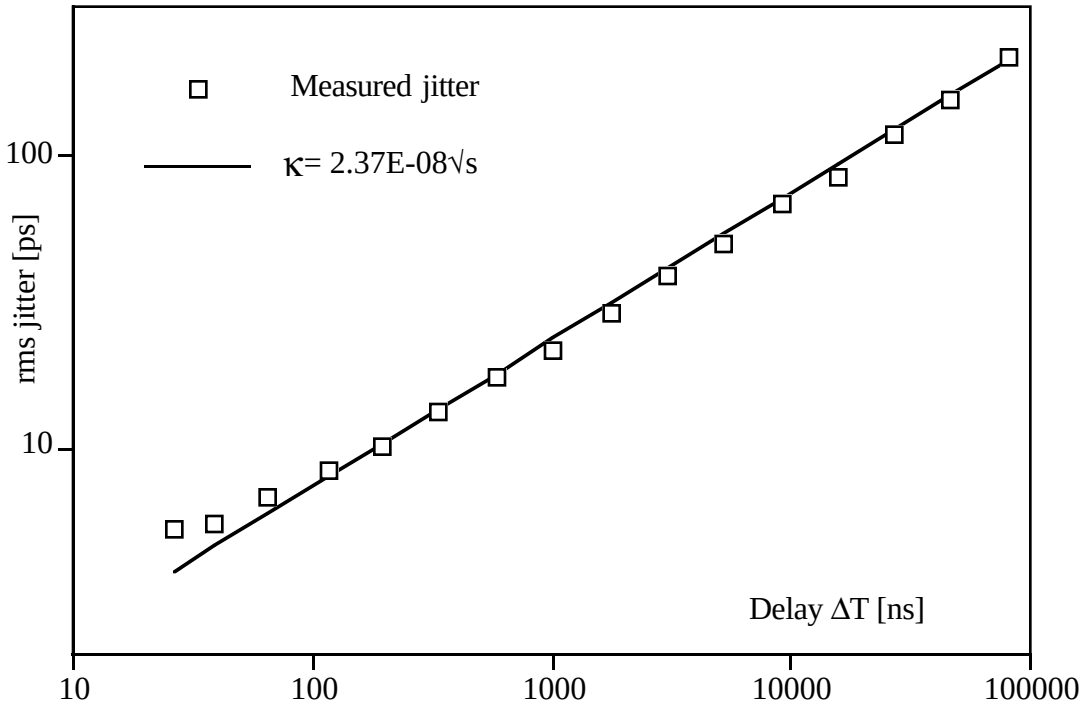


Fig. 2.9. 4 stage ring VCO: time domain, open loop, self referenced

2.2.3 Discussion of results

In all cases, agreement between the predictions of the theory and the measurements is good to within 15%. The error can be attributed to the following sources:

- The oscillator noise spectrum does not exactly follow the assumed $1/f^2$ p.s.d. model;
- When the loop is closed, noise is coupled on-chip due to switching in the phase detector logic. The phase detector is inactive when the VCO is running open loop since there is no input data.

2.3 Chapter summary

The key result of this chapter is that *knowledge of either open-loop figure-of-merit, N_1 (frequency domain) or $\mathcal{K}$ (time domain), gives complete information on the oscillator's jitter performance as measured in five different ways*. The correspondence among these different measures of jitter (in some cases involving nonstationary noise sources) is established by the time/frequency technique developed in Section 2.1. The experimental results of Section 2.2, on an existing multivibrator-VCO-based PLL and a ring VCO, show good agreement to the theoretical predictions in all jitter measures.

This technique provides several benefits to the design and test of low jitter PLLs:

- Improves the design process by allowing VCO design to take place in the domain (time/frequency, open/closed loop) that provides the most insight into sources of jitter, while allowing a direct link to the ultimate performance measure of interest.
- Provides substantial savings in simulation time since only the open loop VCO needs to be simulated during design iteration.
- Allows a stand-alone test of VCO contribution to closed loop jitter. If the measured closed loop jitter significantly exceeds the value predicted from open loop VCO measurements, this indicates that other portions of the PLL (such as phase detector noise or on-chip signal coupling) need to be investigated as sources of jitter. Conversely, if the measured closed loop jitter is close to the value predicted from open loop VCO measurements, this indicates that other portions of the PLL are working well to achieve the limit on jitter performance as imposed by the VCO.

As previously mentioned, this technique applies to any oscillator with a p.s.d. that fits a $1/f^2$ model.

3. Analysis of jitter in ring oscillators

This chapter presents a framework for a theoretical understanding of jitter in ring oscillators. As an introduction, Section 3.1 reviews some published theoretical techniques for harmonic and relaxation oscillators. Section 3.2 develops the theoretical framework, and Section 3.3 deals with some of the details involved in applying it to actual circuit design. Section 3.4 gives experimental results when the framework is applied to a specific ring oscillator.

3.1 Review of jitter analysis in different types of oscillators

Analysis of phase noise and jitter was originally driven by requirements for stability of oscillators used as references for high accuracy time measurement [4, 67]. In this application, variations in frequency over long periods of time ("instability" or "drift") are generally more harmful to performance than variations over shorter periods of time ("jitter"). This may be why theoretical understanding of jitter in rings has lagged behind that in other types of oscillators: since rings are most prone to drift-type instabilities, they have not been used in high accuracy applications. In general the design goal for frequency stability is to make the oscillator period depend on as few parameters as possible, with those critical parameters as well controlled as possible.

Following is an overview of different types of oscillators. Note that the strategy for analyzing jitter depends on the type of oscillator.

3.1.1 Harmonic oscillators

Harmonic oscillators are characterized by an equivalence to two energy storage elements, operating in resonance, to give a periodic output signal. The actual resonant element might be an LC tank or a quartz crystal.

In any case the frequency usually depends on few critical elements, for example, in the LC tank case the L and C values. Tight control of the L and C values leads to good frequency stability.

Analysis of jitter for harmonic oscillators has been approached in the frequency domain [30, 47, 62, 76, 90, 91]. The high Q of the circuit resonance filters thermal (Johnson) noise into a narrow band near the fundamental frequency. This method of analysis is most closely related to the measurement of phase noise in the frequency domain.

As an example of this approach, Golay [30] considers the resonant circuit shown in Figure 3.1. L and C represent the two energy storage modes of the resonator. Resistor R/2 represents the energy losses inherent in any real resonator. Negative resistor $-R_B/2$ supplies energy to balance losses in R/2, thereby keeping the oscillator signal amplitude constant. A key feature of Golay's analysis is the explicit inclusion of a servo circuit that monitors the amplitude of the oscillation and adjusts the value of the negative resistor to stabilize the amplitude at a desired value V_o.

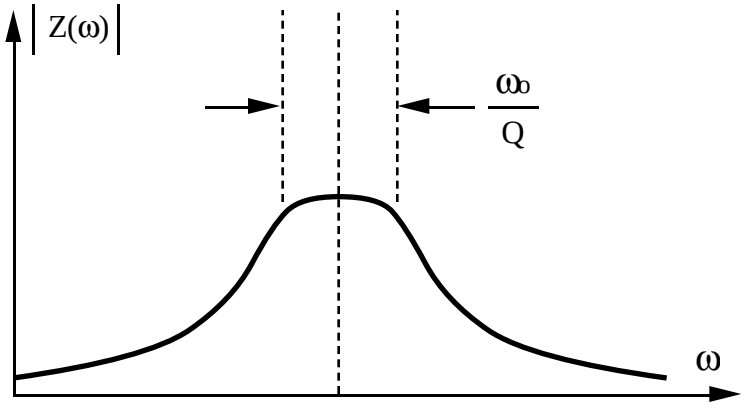
Figure 3.2 shows the magnitude of the impedance of the L(R/2)C network. The resonant frequency ω_o and the quality factor Q are given by

$$\omega_o = \frac{1}{\sqrt{LC}}\sqrt{1 - 2\zeta^2} \approx \frac{1}{\sqrt{LC}} \qquad (3\text{-}1)$$

$$Q \approx \sqrt{\frac{R^2C}{L}} \qquad (3\text{-}2)$$

These are well known results for a second order system where $Q >> 1$ (or, equivalently, the damping factor $\zeta << 1$).

Figure 3.1. L(R/2)C resonant circuit analyzed by Golay.
(After [30], Figure 1. © IRE 1960)



$$\omega_o \approx \frac{1}{\sqrt{LC}} \qquad Q \approx \sqrt{\frac{R^2C}{L}}$$

Figure 3.2.
Impedance of resonant circuit vs. frequency

Golay notes a useful approximation to the impedance for frequencies more than ω_o/Q away from the resonant frequency. The admittance of the LC is

$$Y = j\omega C + \frac{1}{j\omega L} \tag{3-3}$$

Expanding this in a Taylor series about ω_o and keeping only the first order term gives

$$Y \approx j2(\omega_o - \omega)C \tag{3-4}$$

or, in terms of impedance

$$Z \approx \frac{1}{j2(\omega_o - \omega)C} \tag{3-5}$$

Golay then continues the analysis in the frequency domain, considering the thermal noise of the resistor R/2 to be filtered into a narrow band near ω_o. The analysis then makes use of the "narrow-band approximation" [7, 66, 71] to separate the noise into in-phase and quadrature components. Only the quadrature component contributes to jitter; the in-phase component contributes only amplitude noise and can be removed with a limiter. Golay's result is the rms frequency error observed during measurement time ΔT:

$$\Delta f = \frac{1}{2\pi RC}\sqrt{\frac{2kT}{E_B}} \tag{3-6}$$

where Δf is the rms deviation from the ideal $f_o = 1/2\pi\omega_o$, k is Boltzmann's constant, T absolute temperature, and E_B the energy supplied by the negative resistor during the measurement time ΔT:

$$E_B = P_B \Delta T \tag{3-7}$$

Here, P_B is the power supplied by the negative resistor. Note that this is equal to the power dissipated in the loss mechanism resistance.

Summary

We will return to the results of (3-6) and (3-7) in Section 4.4. For now, the point is that the analysis is best approached in the frequency domain, since the oscillation frequency is determined by a resonant circuit that acts as a linear filter to thermal noise.

3.1.2 Relaxation oscillator

Oscillators of this type are characterized by using only one energy storage element to determine frequency. Additional circuitry senses the state of this element and controls its excitation to give a periodic output signal. Verhoeven [86] has classified many types of oscillators based on this concept.

As in the harmonic case, the frequency usually depends on few critical elements, usually a capacitance value, a charging/discharging current, and a reference voltage. These values can usually be controlled well enough to give reasonably good frequency stability [29, 44].

For this type of oscillator, jitter analysis has been approached in the time domain [1, 77]. For example, Abidi and Meyer [1] consider the classic emitter-coupled multivibrator shown in Figure 3.3. The capacitor C is the one energy storage element. This emitter-coupled multivibrator is the type of VCO in the AD802.

Abidi and Meyer's analysis notes that small-signal linear techniques are inadequate since the regenerative switching changes the "operating point" of the circuit over several orders of magnitude. The circuit is equivalent to the Schmitt trigger circuits shown in Figure 3.4. The generalized equivalent circuit used in their analysis is shown in Figure 3.5. The voltage and current waveforms are shown in Figure 3.6. The analysis proceeds by integrating the differential equation for the energy storage element, assuming jitter is caused by the single stationary noise source I_n. Their result gives the standard deviation in the time interval from t_1 (when the voltage ramp changes direction) to t_2 (when the current reaches the regeneration threshold) as:

$$\sigma = \alpha \frac{RC}{I_O - I_R} \sigma(I_n) \qquad (3\text{-}8)$$

Figure 3.3. Classic emitter-coupled multivibrator.
(After [1] Figure 1. © IEEE 1983)

Figure 3.4.
Schmitt trigger representations of emitter-coupled multivibrator.
(After [1] Figure 2. © IEEE 1983)

Figure 3.5. Equivalent circuit for noise analysis.
(After [1] Figure 7. © IEEE 1983)

Figure 3.6.
Waveforms in multivibrator equivalent circuit.
(After [1] Figures 4, 5. © IEEE 1983)

where α is a constant between 0.5 and 1, I_O is the bias current, I_R is the current at the onset of regeneration, and $\sigma(I_n)$ is the standard deviation of the noise current.

It should be noted that the jitter observed in the AD802 was two orders of magnitude greater than that predicted by (3-8). Although pursuit of this discrepancy is beyond the scope of this thesis, there are some possible reasons that may be explored:

- Since Abidi and Meyer only determine the jitter in the time until regeneration, they assume that this is much greater than the time to complete switching after regeneration. This is true at the 1 kHz clock rates treated in their paper. However at 155 MHz the pre- and post-regeneration times may be comparable and there would be additional jitter sources to consider.
- It may not be valid to assume that all noise sources involved in jitter can be referred to a single stationary I_n at the collector. Their measurements verifying (3-8) were made by swamping internal noise sources with an external noise current. While this verifies (3-8) assuming that I_n is dominant, it says little about whether the assumption is true for real circuits. Abidi and Meyer assume that, of Q1 and Q2 in Figure 3.5, one is reverse biased and the other acts as a follower, so that noise sources see only unity gain. In fact, at the onset of regeneration, both Q1 and Q2 are forward biased. In this case, Q1 and Q2 act as an emitter-coupled pair and noise sources see a gain greater than unity.

Verhoeven [86] has considered the effects of the changing gain during regenerative switching, which is used in many relaxation oscillator designs to increase speed. In some cases, regenerative switching actually increases jitter: although the speed of switching is increased, there is a greater increase in the uncertainty in the time at which switching begins.

Summary

The multivibrator analysis is best approached in the time domain, since the jitter in the oscillation period is determined by a nonlinear switching process.

3.1.3 Ring oscillator

Perhaps another reason that analysis of jitter in ring oscillators has lagged is that the ring does not fit into either of these frameworks easily. Figure 3.7 shows a typical ring oscillator schematic. The number of energy storage elements is not as explicit; in fact there are many "energy storage elements" since the ring is composed of multiple stages. In addition, the delay of each stage in turn depends on several stray and junction capacitances as well as parameters such as carrier transit time. Absolute frequency stability is therefore poor, since it depends on the stage delay which is not well controlled and is quite sensitive to environmental influences such as temperature. The result is usually a significant frequency drift and long term instability. This is not a problem when the ring is used as the VCO in a PLL, since the loop controls the absolute frequency and tracks out the ring's long-term instabilities such as frequency drift due to temperature changes. However, the ring is "on its own" for jitter on time scales shorter than the PLL loop bandwidth.

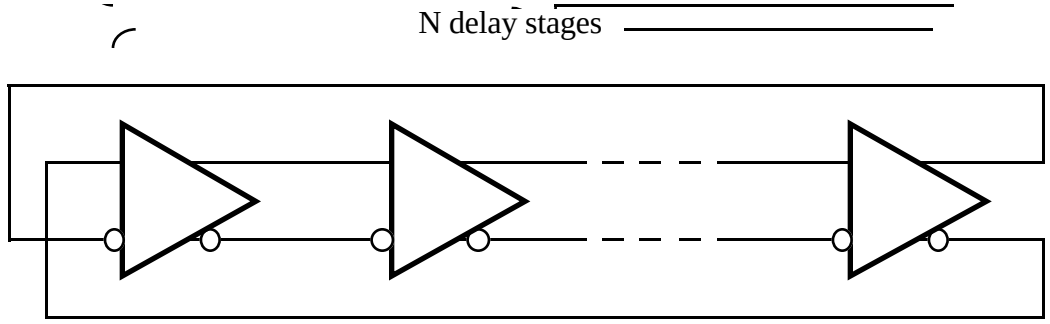


Figure 3.7. Typical ring oscillator schematic.

Neither of the approaches from Sections 3.1.1 or 3.1.2 is well suited to analysis of jitter in the ring oscillator - a different approach is needed. The analysis approach follows from the techniques used to measure jitter, which were discussed in chapter 2.

3.2 Jitter model theoretical development

The approach taken in this thesis is in the time domain, and follows from the open loop, self referenced, two-sample standard deviation method of characterizing jitter developed in Section 2.1.5. The problem is to relate measurements of jitter over long time intervals to the causes of jitter, which occur over small time scales of order as small as a single gate delay.

The solution presented here is a discrete time approach which predicts measured jitter at any delay from a description of the jitter process in one gate delay (or one oscillator period, depending on the jitter mechanism). Although the eventual formulation will be in terms of gate delays around the ring oscillator, the approach is somewhat easier to grasp if it is first presented in terms of clock periods. This is also appropriate since some noise sources are better analyzed in terms of their effect on the oscillator period, rather than the individual gate delay.

The result of the time/frequency technique of Chapter 2 allow us to relate the results of a time domain jitter analysis to other measures of jitter in the frequency and time domains. This is an example of the benefit of the Chapter 2 technique: we can approach jitter analysis in whichever domain gives the simplest treatment - in this case, in the open-loop, time domain. Thus the time/frequency technique eases analysis as well as providing insight for design.

3.2.1 Approach

Since we cannot observe phase directly, we must observe a signal which is a periodic function of phase. We can consider each period of a clock signal to be a discrete event that indicates the accumulation of a uniform amount of phase (2π radians) in an amount of time that varies due to jitter.

Figure 3.8 shows a clock with jitter. We can consider each period of the clock as defining an interval of time; the n^{th} period defines an interval of time t[n]. Since the clock has jitter, the periods are in general unequal and we can consider t[n] to be a discrete time random process (where the "time" in "discrete time" refers only to the discrete nature of the index of the random process t[n], and is not necessarily related to "actual" time).

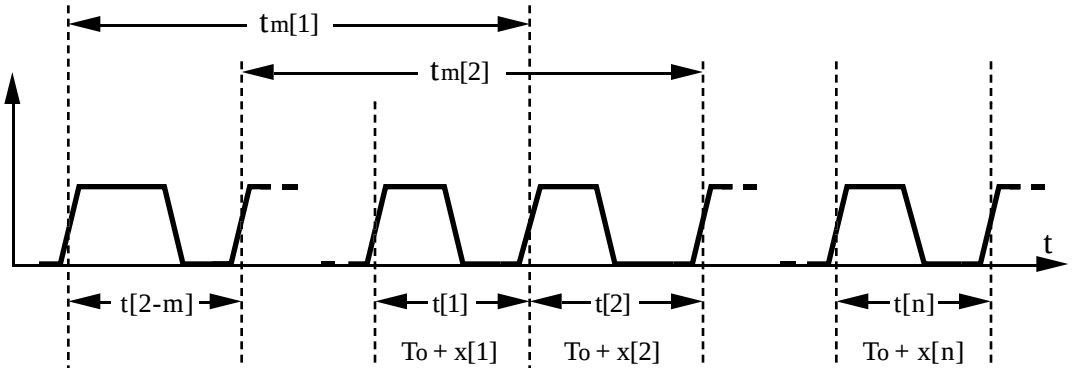


Figure 3.8. Definition of random processes for clock with jitter.

We can also express the random process t[n] as

$$t[n] = T_o + x[n] \tag{3-9}$$

where T_o is the nominal (average) period and x[n] is a zero-mean, discrete time random process that expresses the deviation of the period from the average. Note that defining x[n] to be zero-mean assumes that the mean T_o exists. If there is frequency drift, T_o will not exist if we try to define it as the mean over all time. For a finite record length (which is always the case in practice), we can always define an average T_o and a zero-mean x[n]. Lesage [49] has studied finite-record length effects in detail.

When we measure the jitter of the clock at a certain delay, we are looking at the sum of jitter across several periods. This is shown in Figure 3.8. Suppose we are looking at a delay m periods long; we can define a new random process which at each time is the sum of the previous m periods:

$$t_m[n] = \sum_{i=n-m+1}^{n} t[i] \tag{3-10}$$

This process is what is sampled when we measure jitter with the two sample standard deviation. If we can determine the statistics of the $t_m[n]$ process, we will be able to predict the measured jitter at a delay m periods long.

First, we determine the mean of $t_m[n]$. Substituting (3-9), the definition of t[n], into (3-10) gives

$$t_m[n] = mT_o + \sum_{i=n-m+1}^{n} x[i] \tag{3-11}$$

Since x[n] is zero mean, then the mean of (3-11) is

$$E_{\{\ t_m[n]_{\}} = mT_o \tag{3-12}$$

where E{} is the expectation operator. For the variance of the $t_m[n]$ process, we have

$$\sigma^2_{t\ [n]} = E\left[\sum_{i = n-m+1}^{n} \sum_{j = n-m+1}^{n} x[i]\ x[j] \right] \tag{3-13}$$

We can take the expectation operator inside the summation to get

$$\sigma^2_{t_m}[n] = \sum_{i = n-m+1}^{n} \sum_{j = n-m+1}^{n} E\{\ x[i]\ x[j]\ \} \tag{3-14}$$

Substituting the definition of the random process x[n] autocorrelation $R_{xx}[n]$, then (3-14) becomes

$$\sigma^2_{t_m}[n] = \sum_{i = n-m+1}^{n} \sum_{j = n-m+1}^{n} Rxx[i, j] \tag{3-15}$$

For random walk phase noise, Appendix E shows that the x[n] process is wide sense stationary. Hence the autocorrelation in (3-15) can be written as

$$R_{xx}[i,j] = R_{xx}[i-j] \tag{3-16}$$

Using this, we can rewrite the summation as

$$\sigma^2_{(m)} = \sum_{i = -m}^{m} (m - |i|)\ R_{xx}[i] \tag{3-17}$$

This is shown in graphical form at the top of Figure 3.9 for the case m=2.

The important result expressed in (3-17) is that the variance of the $t_m[n]$ process is simply given by summing the autocorrelation of the noise process x[n] that perturbs each period (the $R_{xx}[i,j]$ term) multiplied by the autocorrelation of an m-bin summation (the i and j summations). This is shown graphically in Figure 3.9. Note that there is no longer any dependence on the discrete time index n.

The following two sections give examples of this procedure.

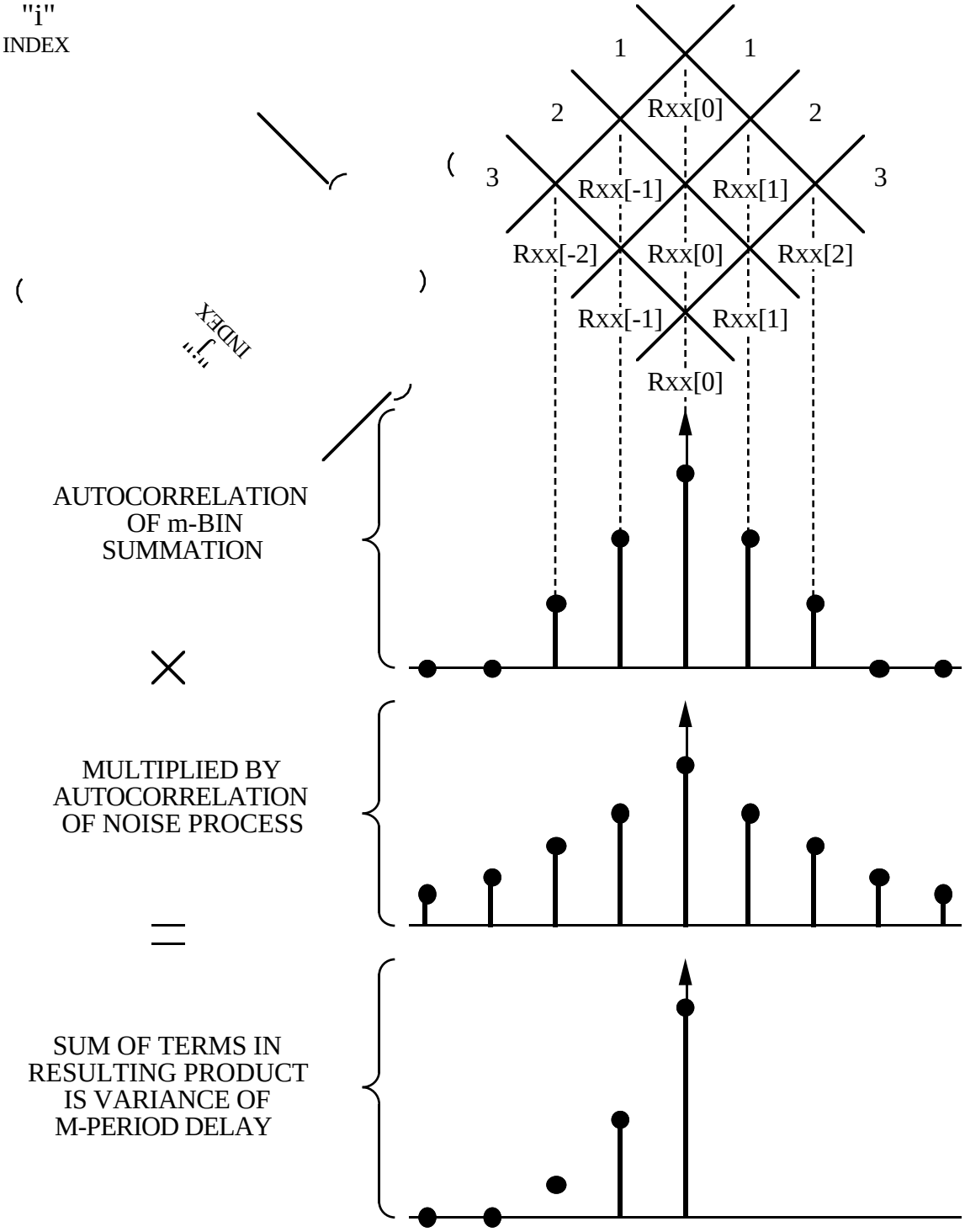


Figure 3.9. Graphical procedure for autocorrelation calculation. Triangular window follows from structure of terms in variance summation.

3.2.2 Special case: Independent delay errors give $1/f^2$ spectrum

Consider a VCO with an ideal white noise source at its input as shown in Figure 3.10. The noise source has a (single sided) voltage density of e_n V/$\sqrt{\text{Hz}}$; the VCO has a control constant of K_o [rad/V· s] and a center frequency of $\omega_o = 2\pi f_o$.

In Appendix F, the variance of the periods is shown to be

$$\sigma^2 = \left(\frac{K_o}{\omega_o}\right)^2 \frac{e_n^2 T_o}{2} = R_{xx}[0] \qquad (3\text{-}18)$$

And since we have assumed white noise, phase errors of adjacent periods are completely uncorrelated so that

$$R_{xx}[n] = 0 \quad n \neq 0 \qquad (3\text{-}19)$$

This gives the autocorrelation shown in Figure 3.11. Applying the summation of (3-17) to this autocorrelation gives for the variance as a function of m

$$\sigma^2_{(m)} = \left(\frac{K_o}{\omega_o}\right)^2 \frac{e_n^2 \, m \, T_o}{2} \qquad (3\text{-}20)$$

shown in Figure 3.12.

If we express (3-20) with the delay interval as

$$\Delta T = m \, T_o \qquad (3\text{-}21)$$

then (3-20) becomes

$$\sigma^2_{(\Delta T)} = \left(\frac{K_o}{\omega_o}\right)^2 \frac{e_n^2 \, \Delta T}{2} \qquad (3\text{-}22)$$

and the standard deviation is

$$\sigma_{(\Delta T)} = \frac{K_o}{\omega_o} \frac{1}{\sqrt{2}} e_n \sqrt{\Delta T} \qquad (3\text{-}23)$$

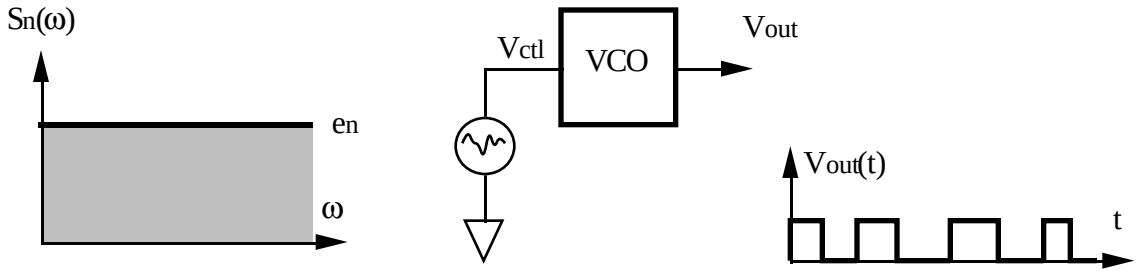


Figure 3.10. VCO with ideal white noise at input.

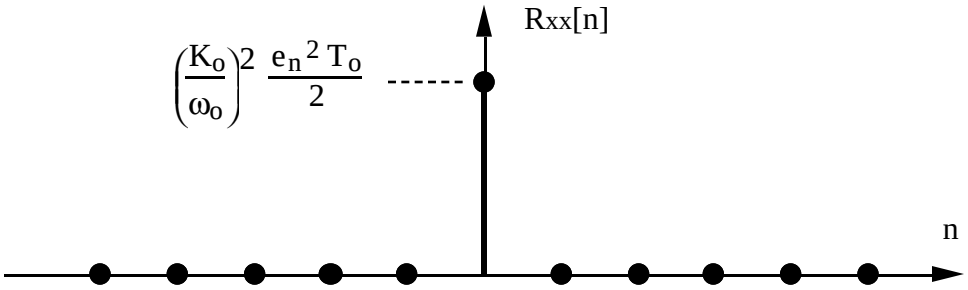


Figure 3.11. Autocorrelation of white noise.

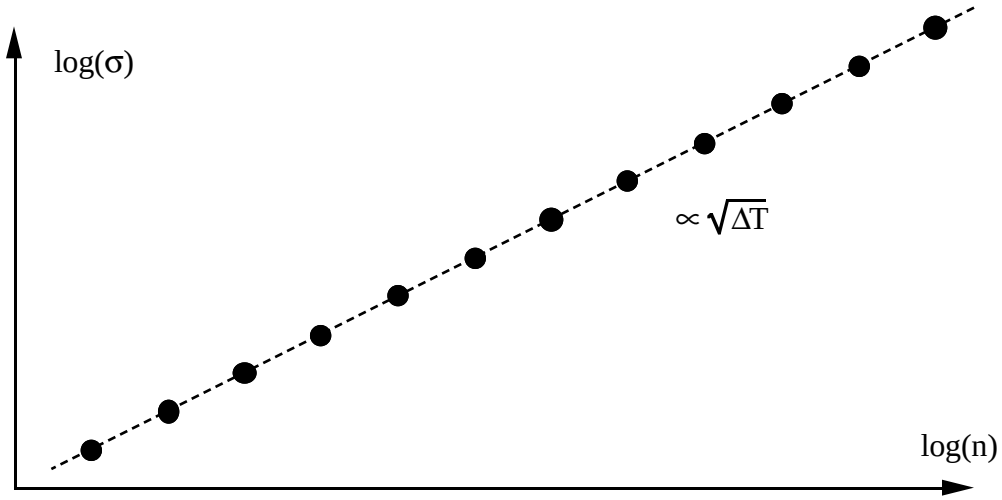


Figure 3.12. Result of summation procedure for white noise input.

Comparing to (2-16), we see that this fits into the form of

$$\sigma_{(\Delta T)} = \kappa\sqrt{\Delta T} \tag{3-24}$$

with

$$\kappa = \frac{1}{\sqrt{2}}\frac{K_o}{\omega_o}\, e_n \tag{3-25}$$

$$\kappa \approx (0.707)\,\frac{K_o}{\omega_o}\, e_n \tag{3-26}$$

Now, with the result of Chapter 2, we can relate the influence of a white noise source at the VCO input to the jitter performance in any of the measurements of Figure 2.1.

We also see from (3-26), with the time/frequency technique of Chapter 2, that white noise at the VCO input will give an open loop p.s.d. with a $1/f^2$ characteristic.

In summary, ideal white noise at the VCO input gives periods with independent errors. The autocorrelation of the process is an impulse, and the jitter (standard deviation) increases as the square root of the delay (since the variance of the sum of independent random variables is simply the sum of the variances). Since this is follows the general $\sigma_{(\Delta T)} = \kappa\sqrt{\Delta T}$ model from Chapter 2, we know that the open-loop p.s.d. will have a $1/f^2$ characteristic.

3.2.3 General case: Correlated delay errors

In practice, however, there is no such thing as a pure white noise source. This leads to correlation so that the period errors are not independent. In this section we will examine the effect of bandlimited white noise at the VCO input. The procedure is similar to the previous section but the mathematics are more involved.

Figure 3.13 shows the p.s.d. of a white noise source bandlimited at frequency ω_n. The autocorrelation of this noise source is shown in Figure 3.14. The variance of the periods is derived in Appendix F and plotted in Figure 3.15. Although applying the summation procedure of equation (3-17) results in a complicated mathematical expression, insight can be gained by considering asymptotic expressions for short and long delays.

For small m (short delays), equation (F-13) approaches

$$\sigma^2_{(m)} = \left(\frac{K_o}{\omega_o}\right)^2 \frac{\omega_n \, e_n^2 \, m^2 \, T_o^2}{4} \tag{3-27}$$

Substituting $\Delta T = m \, T_o$ into (3-27) and solving for $\sigma_{(\Delta T)}$ gives

$$\sigma_{(\Delta T)} = \left(\frac{K_o}{\omega_o} \sqrt{\omega_n} \, \frac{e_n}{2}\right) \Delta T \tag{3-28}$$

From (3-28) we see that for short delays, standard deviation grows proportionally with delay. This is a faster increase than the proportionality to square root of delay as was seen in the pure white noise case.

For large m (long delays), (F-17) gives

$$\sigma^2_{(m)} = \left(\frac{K_o}{\omega_o}\right)^2 \frac{e_n^2 \, m \, T_o}{2} \tag{3-29}$$

and substituting $\Delta T = m \, T_o$ into (3-29) gives

$$\sigma_{(\Delta T)} = \frac{K_o}{\omega_o} \frac{1}{\sqrt{2}} \, e_n \sqrt{\Delta T} \tag{3-30}$$

which is the same as (3-23) from the ideal white noise case.

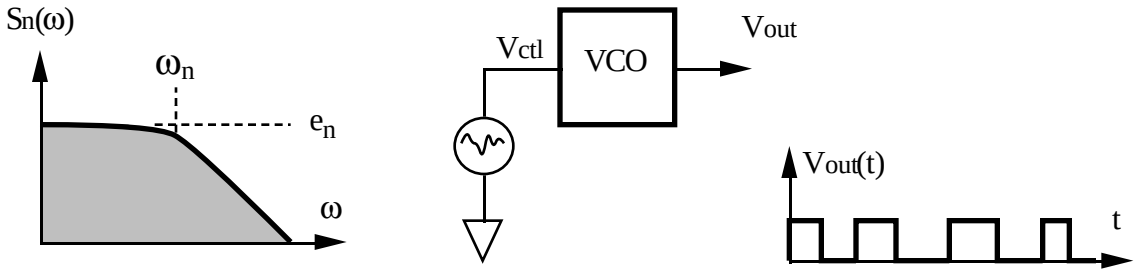


Figure 3.13. VCO with bandlimited white noise at input.

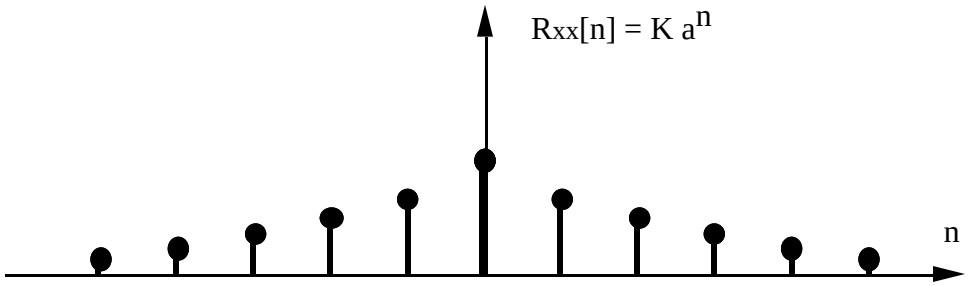


Figure 3.14. Autocorrelation of bandlimited white noise.

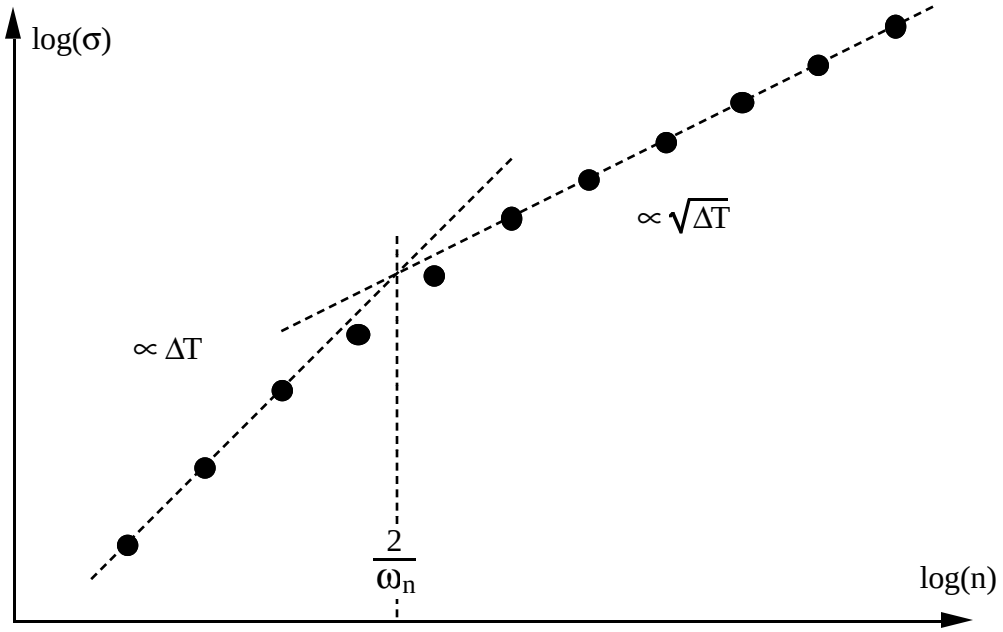


Figure 3.15. Result of summation procedure for bandlimited white noise input.

The transition between the two regions occurs where (3-28) equals (3-30)

$$\left(\frac{K_o}{\omega_o}\sqrt{\omega_n}\,\frac{e_n}{2}\right)\Delta T = \frac{K_o}{\omega_o}\,\frac{1}{\sqrt{2}}\,e_n\sqrt{\Delta T} \qquad (3\text{-}31)$$

$$\Delta T = \frac{2}{\omega_n} \qquad (3\text{-}32)$$

We can interpret this by noting that, on time scales shorter than $2/\omega_n$, the noise affecting jitter is correlated. Thus there is a coupling between periods which causes jitter to increase faster than predicted by a simple independent delay model.

Note also that for delays longer than $2/\omega_n$, *the expression for jitter is the same as in the ideal white noise case*. Thus, if we are considering jitter at delays longer than $2/\omega_n$, we need not consider the bandlimiting effects and can treat the noise as if it were white with density e_n.

Experimental verification

Figure 3.16 shows measured jitter for a VCO with bandlimited white noise applied at its input. The experiment parameters are as follows:

K_o = 2.77E+08 rad/V· s

$f_o = 2\pi$ (154.1MHz) = 9.68E+08 rad/s

e_n = 742 nV/$\sqrt{\text{Hz}}$

ω_n = 2.43E+06 rad/s

The dashed lines indicated the asymptotes predicted by (3-28) and (3-30). As can be seen, agreement to the predicted asymptotes is good, and the inflection point occurs where predicted by (3-32).

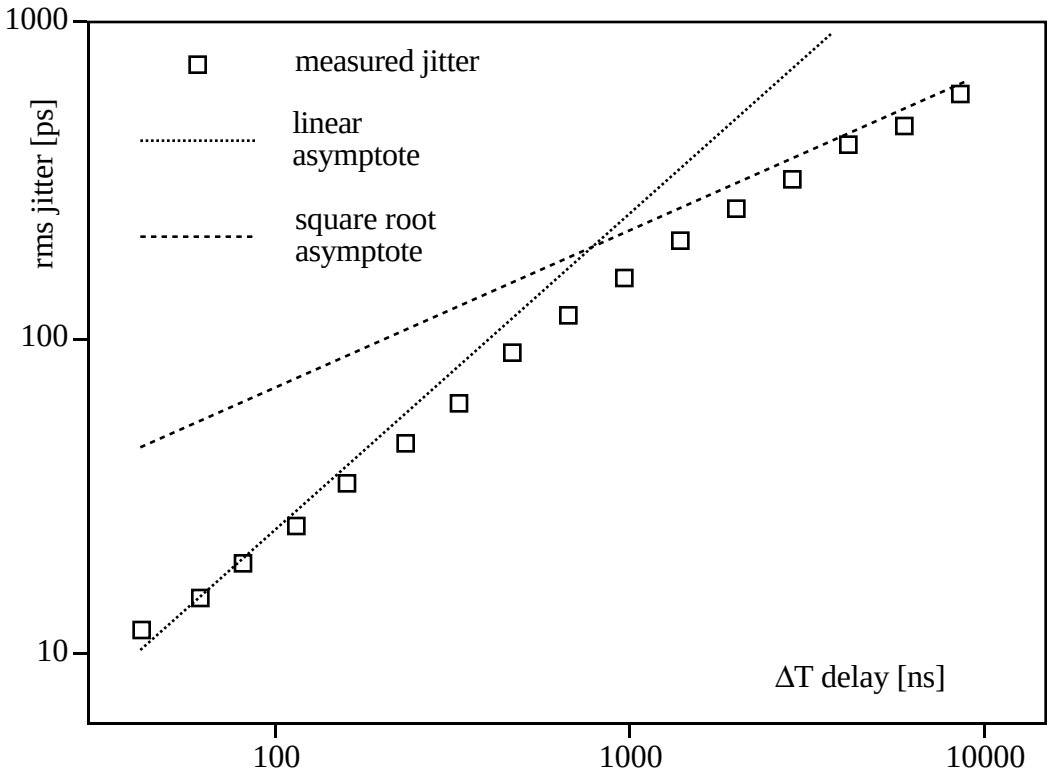


Figure 3.16. Measured jitter with bandlimited white noise at VCO input.

Summary

This is an example of the advantage of being able to relate the results of different jitter measures. The plot of σ vs. ΔT shows an inflection point between $\sigma \propto \Delta T$ and $\sigma \propto \sqrt{\Delta T}$ regions, which indicates that pure white noise is not a valid model for the jitter process. In addition, the location of the inflection point is related to the bandwidth of the noise process by (3-32). Clearly this plot gives more information than jitter at a single delay. Also, based on the deviation from the $\sigma \propto \sqrt{\Delta T}$ model at short delays, we might also expect to see some deviation from the $1/f^2$ p.s.d. model in the frequency domain.

3.2.4 Simplified procedure for long delay asymptote

The procedure in Section 3.2.1 gives jitter at any delay. Unfortunately, the autocorrelation and summation calculations are frequently cumbersome. In fact, for most design purposes, they may not be necessary.

Suppose we are designing for a given closed loop jitter σ_x. Consider the open loop jitter $\sigma_{\Delta T(OL)}(\Delta T)$. At some delay ΔT_x, the open loop jitter $\sigma_{(\Delta T)}(\Delta T_x)$ is equal to the eventual closed loop jitter σ_x. We can determine this delay by equating (2-4) and (2-14):

$$2\pi \sqrt{N_1 \Delta T_x} = \sqrt{\frac{N_1 \pi}{f_L}} \tag{3-33}$$

$$\Delta T_x = \frac{1}{4 \pi f_L} \tag{3-34}$$

The time constant τ_L corresponding to the loop bandwidth f_L is

$$\tau_L = \frac{1}{2 \pi f_L} \tag{3-35}$$

Then

$$\Delta T_x = \frac{\tau_L}{2} \tag{3-36}$$

This means that the closed loop jitter σ_x is given by the open loop, self referenced jitter $\sigma_{\Delta T(OL)}(\tau_L/2)$ measured at a delay of $\tau_L/2$, where τ_L is the loop bandwidth time constant. Typically the loop bandwidth f_L is of order 100kHz to 1 MHz, so $\tau_L/2$ is of order 100ns to 1μsec. (Also, f_L is usually lower than the bandlimited white noise corner frequency). Therefore, for predicting closed loop jitter σ_x, it is usually sufficient to consider only the region of $\sigma_{\Delta T(OL)}$ in the "long delay" (> 100ns to 1μsec) asymptote.

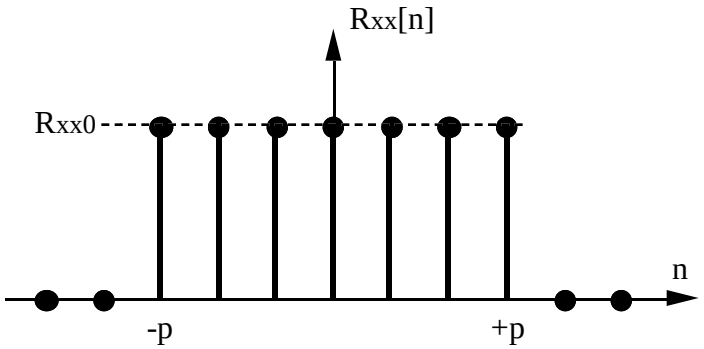


Figure 3.17. Autocorrelation for asymptote example.

Consider an autocorrelation that has a value of $R_{xx}[i] = R_{xxo}$ for $|i| \le p$, as shown in Figure 3.17. Since we are looking at long delays, we will assume $m >> p$. Applying the summation of (3-17) gives

$$\sigma^2_{(m)} = \sum_{i=-p}^{p} (m - |i|)\, R_{xxo} \qquad (3\text{-}37)$$

since $R_{xx}[i]$ is nonzero only for $|i| \le p$. Solving the summation gives

$$\sigma^2_{(m)} = [\, m(2p+1) - p(p+1) \,]\, R_{xxo} \qquad (3\text{-}38)$$

When $m >> p$, the $m(2p+1)$ term dominates and the $p(p+1)$ term can be neglected, giving

$$\sigma^2_{(m)} \approx m\,(2p+1)\, R_{xxo} \qquad (3\text{-}39)$$

Note in (3-39) that $(2p+1)\, R_{xxo}$ is simply the sum of the terms in the original autocorrelation. This is true regardless of the actual shape of the autocorrelation: *the long delay asymptote can be determined simply by multiplying m by the sum of the terms in the jitter process autocorrelation.* That is why the same asymptote was seen in equations (3-20) and (3-29): although it is not obvious from Figures 3.11 and 3.14, the sum of the terms in the autocorrelations are equal.

3.2.5 Development in terms of gate delays

Actually, the results in Sections 3.2.2 and 3.2.3 could also have been derived using standard modulation and transform tools, since the noise source acts to influence the entire oscillator period. The value of Sections 3.2.2 and 3.2.3 is to illustrate the applicability of discrete time approach, which is necessary for considering noise sources that act on individual stages of a ring.

Although (3-15) was developed with the t[n] process representing periods of the clock, the result is also valid when the t[n] represent individual gate delays. For a ring with N stages, each delay adds π/N radians of phase (rather than 2π). We will see that the jitter at long delays will also approach a $\sigma \approx \mathcal{K}\sqrt{\Delta T}$ asymptote. *The figure-of-merit $\mathcal{K}$ is the key to connecting the noise analysis on a gate-delay time scale to jitter performance over time scales of order the loop bandwidth time constant.*

3.2.6 Methodology

Given the result in (3-15), the methodology for analyzing jitter in ring oscillators is straightforward.

1) From a noise analysis (specific to the circuit used for the delay stage in the ring), the standard deviation for the jitter process in one delay element can be determined.
2) Analyzing the delay-to-delay coupling dependency gives the autocorrelation of Figure 3.9.
3) The long-delay asymptote characteristic κ can be determined using the simple procedure of Section 3.2.4. This result can also be related to any of the jitter measures in Chapter 2.
4) The asymptotic κ gives the closed loop jitter σ_x using the procedure in Chapter 2.
5) If desired, the summation procedure of (3-15) can be applied to predict the jitter measured at any delay.

3.3 Applying model to circuit design

The description of the jitter process x[n] depends on the details of the specific circuit design. Fortunately, many of the noise processes that are encountered in delay stages of ring oscillators have already been analyzed in other contexts - using equation (3-15) allows these disparate results to be brought together so that different design options may be compared on the basis of the ultimate jitter in the ring.

The remainder of this section briefly mentions some of the major causes of jitter in delay elements. Section 3.3.1 covers sources of jitter in delays considered individually; Section 3.3.2 considers mechanisms for coupling between delays. Chapter 4 covers a detailed example of the framework applied to a specific type of ring oscillator.

3.3.1 Sources of jitter in individual delays

The noise source that is the major contributor to jitter depends to a large extent on what kind of gate is used as the delay element in the ring. For illustration, the simple delay stage shown in Figure 3.18 will be discussed. In practice, emitter followers are usually used to buffer the collector voltages. For now, we will consider only noise sources in the differential pair.

The input voltage V_{in} causes differential pair Q_1/Q_2 to steer the tail current I_{EE} to one of the collector loads, R_{L1} or R_{L2}. Capacitors C_{L1} and C_{L2} represent wiring stray, junction, and any explicit capacitances that may be present at the collector node. The differential output is taken between the two collectors.

Following are some of the possible noise sources to be considered. In each case a distinction will be made as to whether the noise source is fundamental (cannot be eliminated) or not (could in principle be eliminated through appropriate design).

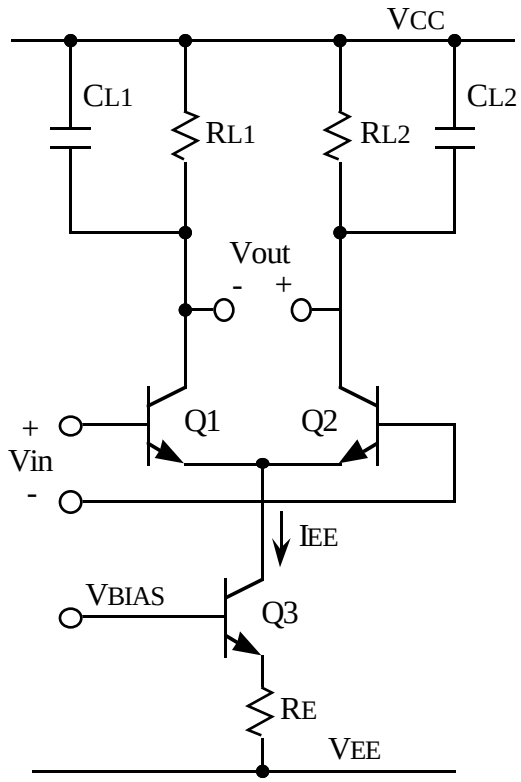


Figure 3.18.
Ring gate for noise analysis.

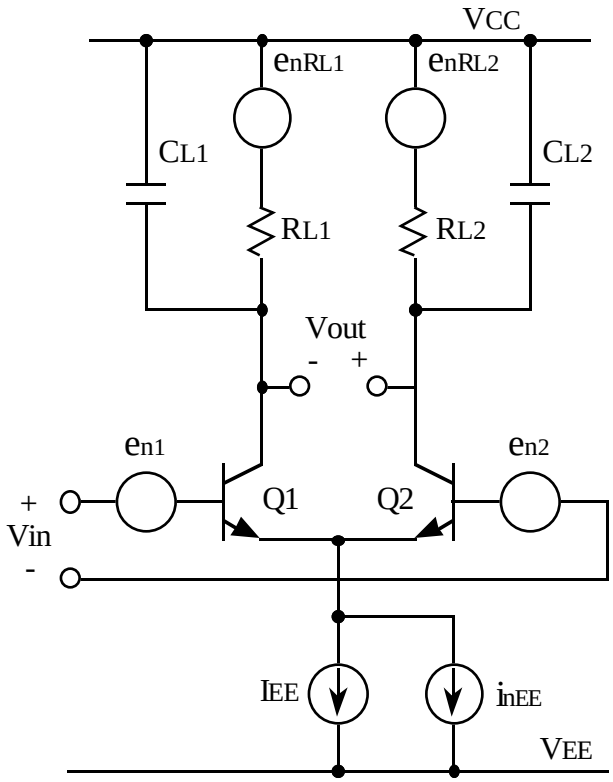


Figure 3.19.
Noise sources in ring gate.

Thermal noise in collector load

Thermal noise is always present and imposes a lower limit on achievable jitter. These noise sources are represented by e_{nRL1} and e_{nRL2} in Figure 3.19.

The sources appear directly at the output, but are bandlimited by the $R_{L1}\cdot C_{L1}$ and $R_{L2}\cdot C_{L2}$ poles. This is a fundamental source of jitter that cannot be eliminated.

Thermal noise / shot noise of tail current

Noise is also present in the tail current of the differential pair. This is represented by noise source i_{nEE} in Figure 3.19. The type of noise depends on the nature of the current source. If the tail current source is degenerated (as shown with R_E in Figure 3.18), the output noise will be dominated by the thermal noise of the degeneration resistor. If not degenerated, the noise is dominated by the shot noise of the DC current I_{EE} [8].

When V_{in} is large enough to fully switch the differential pair, the current noise is passed to the output, but is bandlimited by the either the $R_{L1}\cdot C_{L1}$ or $R_{L2}\cdot C_{L2}$ pole.

When V_{in} is small, the differential pair is approximately balanced. The tail current noise is a common mode error and does not affect the differential V_{out}.

Tail current noise is also a fundamental source of jitter that cannot be eliminated; only changed by changing the current source.

Sampling of thermal noise at inputs

There is also thermal noise in series with the inputs of the differential pair. This is represented by noise sources e_{n1} and e_{n2} in Figure 3.19. This noise is due to thermal noise of the Q1/Q2 transistor base resistances [31] as well as other wideband noise sources going back to V_{out} of the preceding stage of the ring. The thermal noise is sampled by the switching action of the differential pair. This type of behavior is seen whenever high gain is used to sharpen a threshold crossing [86].

These noise sources only contribute error to the output when the input signals cross through the active region of the differential pair. The voltage noise at the input, through the transconductance of the differential pair, creates a current noise at the output which is integrated on C_{L1} and C_{L2}. This is a fundamental source of jitter: it cannot be eliminated but can be reduced, for example by using large geometry transistors to reduce base resistance.

Additional noise from regenerative switching

Although regenerative switching is not shown in Figure 3.18, it should be noted that if regeneration is used to speed switching, increased jitter may result. This has been investigated in detail in the literature [11, 77, 86]. Regenerative switching does make the transition of the switching waveform through the threshold faster than the simple differential pair, but may actually make the time at which the transition occurs more uncertain. The reason is that the maximum gain of the differential pair is limited, but the effective gain of the regenerative circuit becomes very large (ideally, infinite) at the onset of regeneration. Thus the effects of input noise sources such as e_{n1} and e_{n2} of Figure 3.19 are further magnified. In addition, the sampling action of the regenerative switching can alias high-frequency noise into lower frequencies near the oscillator fundamental [86].

One advantage of regenerative switching is that it does tend to force the circuit to a consistent initial condition [46], which prevents a further increase in jitter due to the period-to-period coupling mechanisms that will be discussed in the next section.

The increased sensitivity to input noise sources is not a fundamental source - it can be avoided by taking regenerative switching out of the critical signal path. This is in fact what is suggested for relaxation type oscillators in [74, 86].

3.3.2 Causes of period-to-period coupling that increase jitter

All of the noise sources discussed in the previous section act on individual gate delays. They would be taken in to account to determine the $R_{xx}[0]$ term of the autocorrelation developed in Section 3.2.1. There are also mechanisms whereby jitter in one gate delay can affect jitter in other gate delays. This type of effect will be referred to as "period-to-period" coupling. These must be taken into account to determine the other terms of the $R_{xx}[i]$ autocorrelation.

The causes for period-to-period coupling of jitter errors may be broadly classified into two types, "extrinsic" and "intrinsic." An extrinsic cause is imposed from outside the ring, and in principle the outside influence can be made arbitrarily small.

Intrinsic coupling, on the other hand, is an inherent property of the ring and cannot be reduced below a certain minimum level without changing the fundamental design of the ring. In either case the effect of period-to-period coupling is an increase in jitter over that predicted by a simple model that assumes independent delay errors.

Following are some of the possible coupling mechanisms to be considered. In each case a distinction will be made as to whether the coupling source is extrinsic or intrinsic.

Power supply coupling

Any sensitivity of delay to extraneous inputs such as power supply voltage will be shown by increased jitter. Obviously this is not a fundamental limit on circuit performance, but in practice supply sensitivity is often a major source of jitter [15]. One technique of improving immunity to common mode influences (such as the power supply) is to use fully differential signal and control paths [64].

This is an example of an extrinsic influence on coupling. All gates are affected at the same time by the power supply influence. The bandwidth of the interfering signal "enforces" correlation between delay errors. This type of error is not so much jitter as an unintended modulation, and the designer seeks simply to make the effect of the unwanted influence as small as possible. In principle, the unwanted influence can be made arbitrarily small, for example (in the case of power supply coupling) by arbitrarily large bypass capacitors and decoupling networks.

Waveform "memory" coupling

For some types of delay elements, "memory" of previous jitter errors may affect future delays. Consider a simple RC delay waveform as shown in Figure 3.20. For each element in an N-stage ring, an input switching event leads to a delay T_d until the delay element threshold crossing, followed by an interval of (N-1) T_d until the input switches again. Since the exponential waveform does not fully settle to its final value, however, if there is some delay error ε in the intervening time then the delay produced by this element is affected by an amount ε'. An analysis of the exponential waveform in Appendix G shows that ε' has the same sign as ε, leading to correlation which results in increased jitter. Fortunately this is a second order effect and diminishes rapidly as the number of stages in the ring increases.

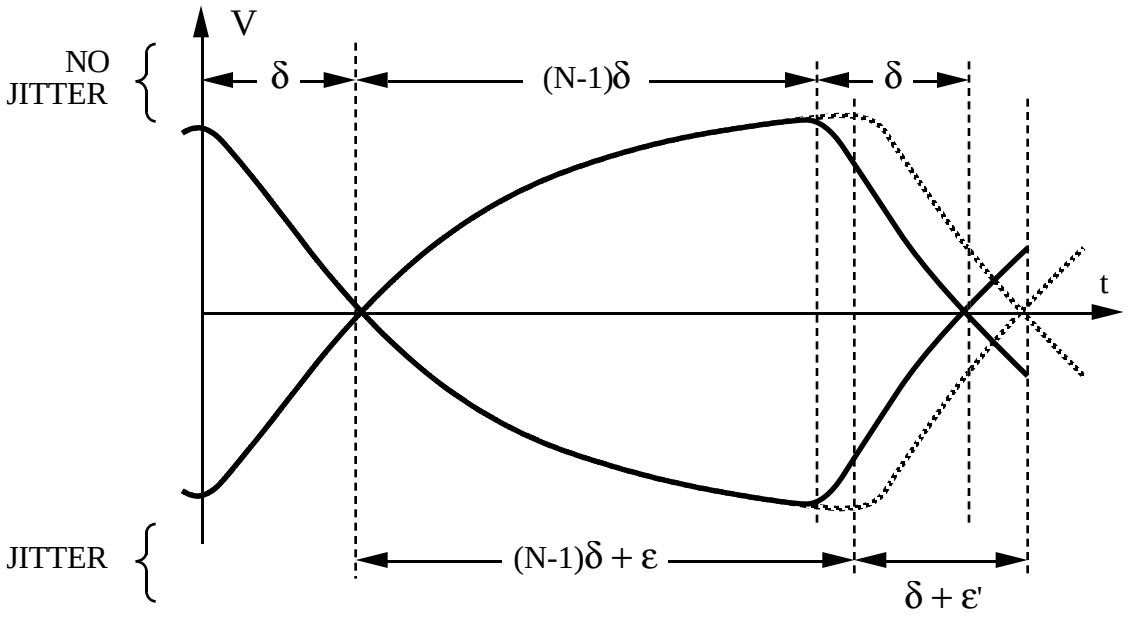


Figure 3.20. RC waveform with exponential coupling of jitter errors.

This is an intrinsic error since the source of the correlation is inherent in the gate design. However, this effect can be reduced if necessary by clamping the RC network [50] so that the exponential settling always starts from the same initial condition regardless of any previous delay errors.

Chaos

Since any real oscillator is to some extent a nonlinear system, chaotic behavior is always a possibility. Chaos has frequently been reported in oscillators in general [68, 80], and has been observed in ring oscillators as well [16]. Since the analysis of chaotic dynamics at present is still very dependent on the details of the system under study, the possibility of chaos is only mentioned here as something to be aware of if unexplained jitter is observed.

This is also an intrinsic error since the source of the correlation is inherent in the gate design and the nonlinear dynamics of the ring.

3.4 Experimental verification

The intent of these experiments is to test the assertion in Section 3.2.5 that jitter over long delays is determined by jitter acting on the individual gates.

The general schematic of the rings tested in these experiments is shown in Figure 3.21. The ring is composed of differential stages (for immunity of jitter to coupling from common-mode noise sources), with a wire inversion giving the necessary 180° phase shift around the loop. The gate circuit is shown in Figure 3.22; it is based on a delay element that has been used in a phase shifter for a clock-recovery PLL [46]. The gate speed is determined by slewing in the current-starved input differential pair; it is not f_T-limited. This gate uses regenerative switching which "resets" circuit nodes to the same initial conditions; therefore we expect to see little or no delay-to-delay coupling. Rings of 3, 4, 5, 7, and 9 stages were fabricated in a 3 GHz f_T bipolar process.

Jitter was measured in both the time and frequency domains. Since there is no PLL involved, only open loop measurements were made

Table 3.23 shows the measured center frequencies and the delays of the individual gates in each ring. Also shown are the measured N_1 and κ values, as well as the predicted N_1 and κ from the time/frequency technique of Chapter 2. The predicted values agree with the measurements to within 5%. As expected, the longer rings operate at a lower center frequency since all of the gates have approximately the same delay. *Note that the κ values are approximately the same regardless of the length of the ring.*

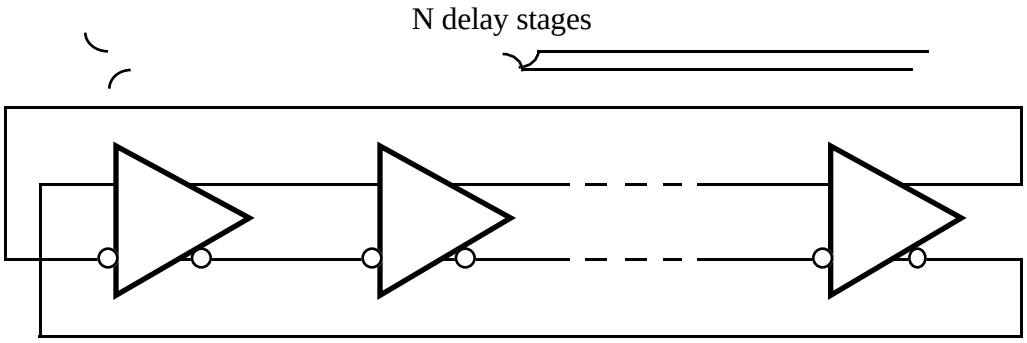


Figure 3.21. General schematic for ring experiments.

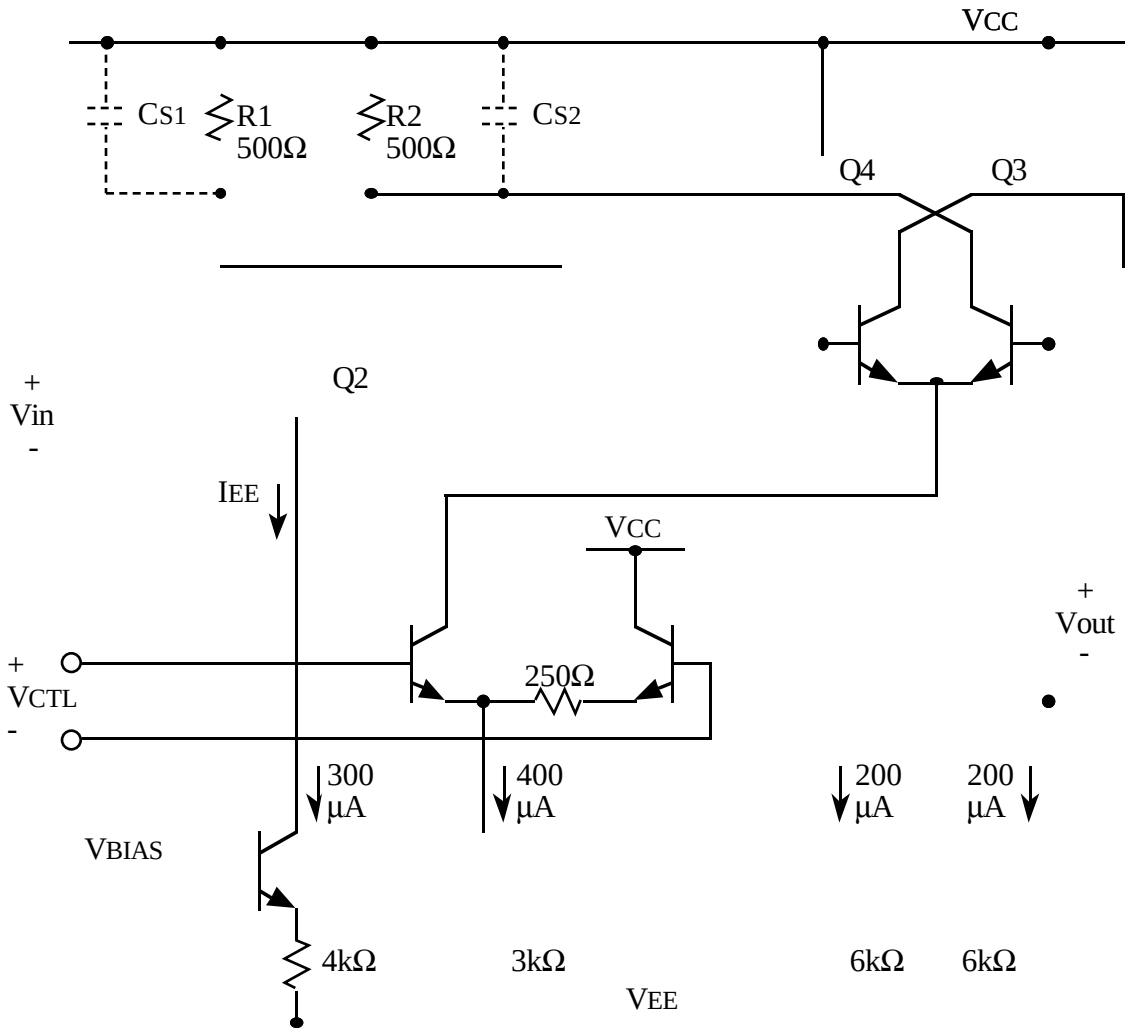


Figure 3.22. Gate delay element schematic.

Table 3.23. Ring experiment results.

RING STAGES	κ [E-08$\sqrt{}$sec] MEASURED	κ [E-08$\sqrt{}$sec] PREDICTED	N_1 [Hz] MEASURED	N_1 [Hz] PREDICTED	fo [MHz]	td [nsec]
3	4.199	4.163	16.14	16.36	96.3	1.73
4	4.402	4.306	7.93	8.26	65.3	1.91
5	4.395	4.321	6.72	6.95	60.0	1.76
7	4.354	4.425	3.36	3.26	41.4	1.73
9	4.272	4.404	2.09	1.96	32.8	1.70

The reason for this behavior is seen from Figure 3.24, which is a plot of $\sigma_{\Delta T(OL)}$ vs. ΔT for all rings. It is seen that the jitter (in ps) at a certain delay (in ns) is the same *regardless of how many stages there are in the ring*. The jitter (in terms of absolute time) depends *only on the number of gate delays traversed during the delay time*. This shows that the ability of a ring to accurately measure an interval of time depends only on the accuracy of its basic delay element. Thus if we can characterize the accuracy of the gate in terms of κ, we can predict the $\sigma_{\Delta T(OL)}$ vs. ΔT plot for a ring using that gate, regardless of the ring's length. The jitter increases as the square root of delay time, consistent with the model presented in Section 3.2.

Other measures of jitter that depend on the length of the ring (and thus the frequency) obscure this connection. Figure 3.25 shows the plots of $\sigma_{\Delta T(OL)}$ vs. ΔT with time normalized to unit intervals (periods). Since all of the rings have the same jitter in terms of absolute time, the jitter of the longer ring appears to be lower, since the period of the ring is longer. The N_1 values in Table 3.23 show that, at a given offset frequency from the fundamental, the noise density is lower for the longer rings. This is because N_1 depends on the center frequency f_o, as shown in equation (2-17).

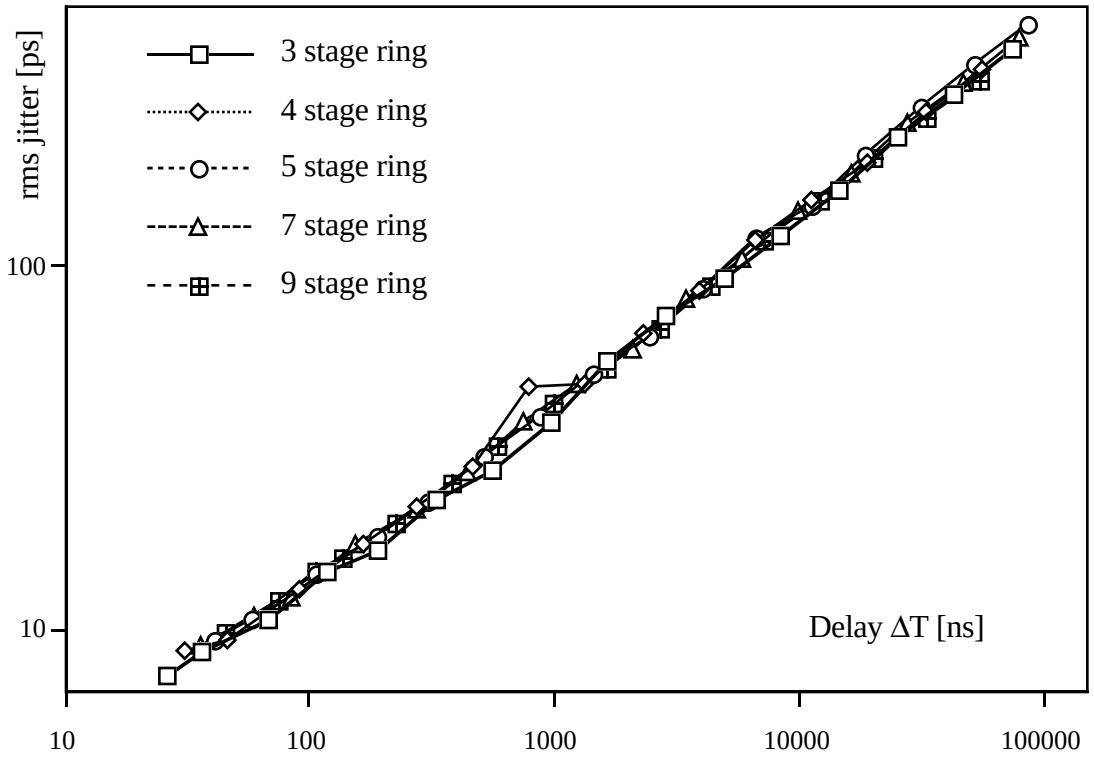


Fig. 3.24. Plot of ring jitter (absolute time) for 3, 4, 5, 7, 9 stage rings

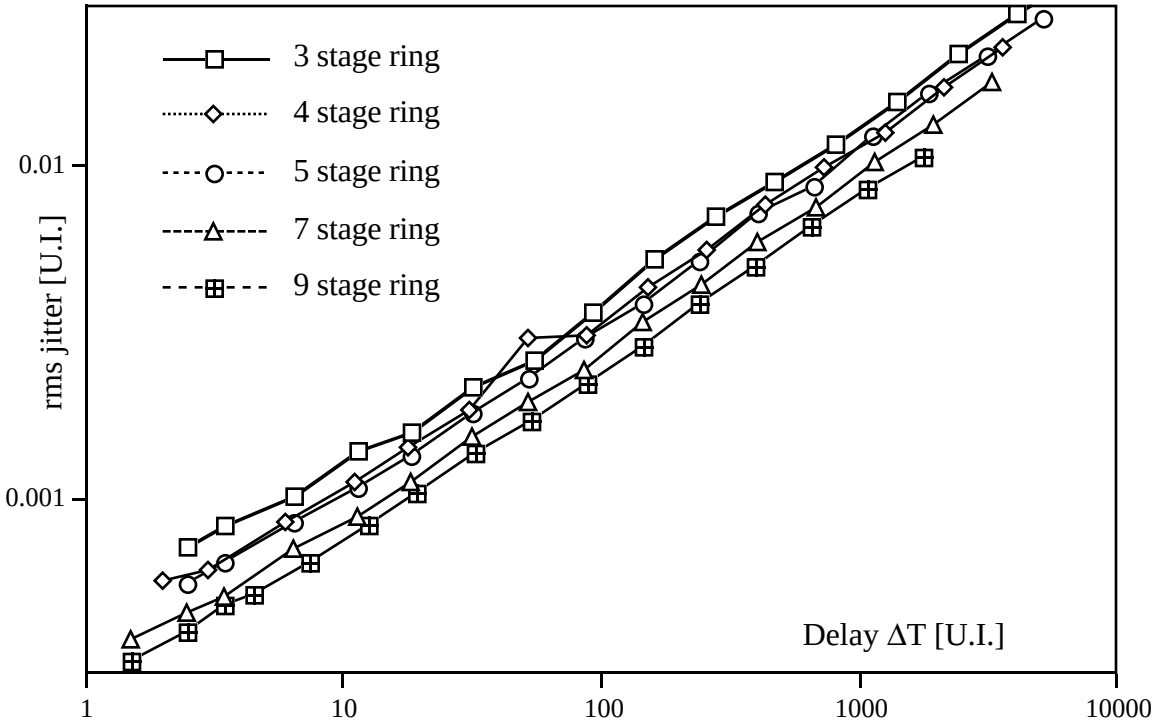


Fig. 3.25. Plot of ring jitter (normalized time) for 3, 4, 5, 7, 9 stage rings.

Summary

These experimental results confirm that the jitter of the individual gate delay, characterized by κ, can be related to the jitter behavior of the ring as a whole regardless of the length (and thus the frequency) of the ring. This allows the designer to concentrate on the design of the gate itself, while being able to predict the jitter of the ring.

3.5 Chapter summary

In this chapter we have developed a theoretical framework for analyzing and predicting jitter in ring oscillators. An approach based on a discrete-time random process representation of jitter errors allows prediction of jitter caused by different sources. The technique also allows analysis of increased jitter due to period-to-period coupling, and offers possible circuit techniques to reduce these effects. The result is a prediction of the time domain figure-of-merit κ, which can be used to determine the end user's figure-of-merit σ_x. Experimental results for rings of several different lengths confirm the validity of the general approach.

4. Sources of jitter in ring oscillators

In this chapter we will consider a detailed application of the jitter analysis method developed in Chapter 3.

4.1 Simple differential pair

The differential pair delay element that will be analyzed in this chapter is shown in Figure 4.1. We will derive the effective κ for the noise sources outlined in Section 3.3.1: thermal noise of the collector load resistors, thermal noise at the input, and noise of the tail current source. The effective κ for noise on VCO control input was derived in Section 3.2. Since this gate does not use regenerative switching, its added noise effects need not be considered.

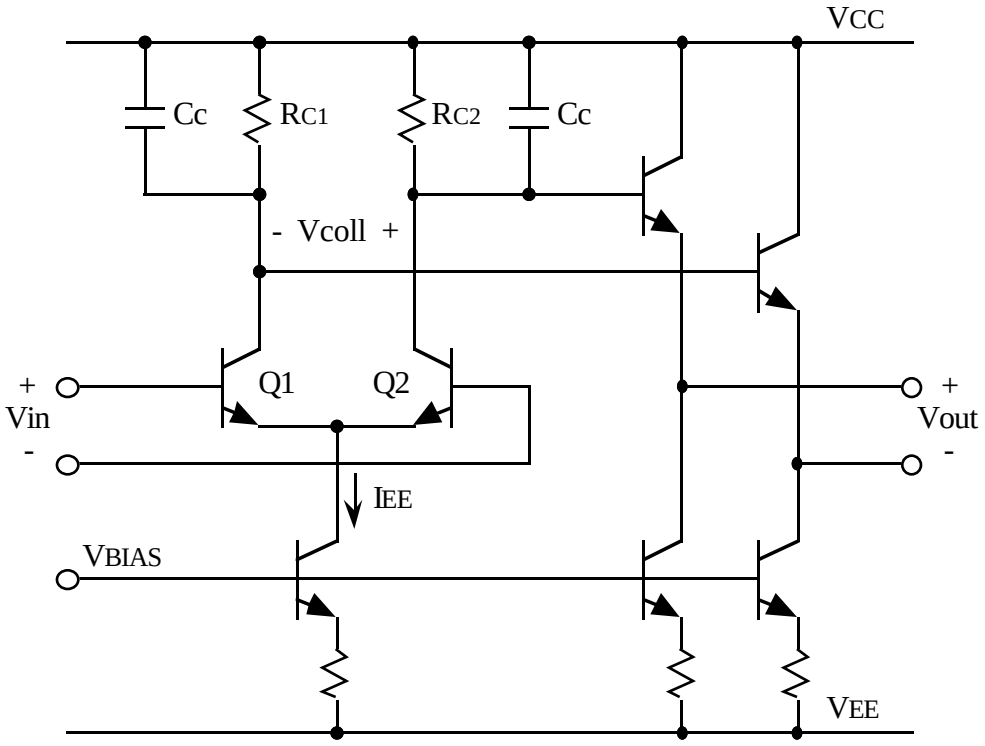


Figure 4.1. Differential pair delay gate.

The delay through the gate has two components:

1) delay through the differential pair (from V_{in} to V_{coll})
2) delay through the emitter follower buffers (from V_{coll} to V_{out})

To simplify the analysis and make the results easier to interpret, we will now make two assumptions regarding the gate delay:

For the remainder of this chapter, we will assume that *the gate delay is dominated by the delay through the differential pair*. This is generally a reasonable assumption (since the delay of the follower is of order the base transit time τ_T) and introduces an error of order less than 10%.

The delay through the differential pair is examined in Appendix H, and is approximated in equation (H-7). It depends on many factors, among them the speed of the input signals, the RC time constant of the collector loads, the transit time τ_T, and the base-collector capacitance. Generally, as long as the magnitude of the differential signal is greater than $V_T = kT/q_e$, the differential pair switches the tail current much faster than the time constant of the collector load resistance and the effective stray capacitance at the collector node. For the remainder of this chapter, therefore, we will assume that *the differential pair delay is dominated by the RC time constant of the load*. This is not quite as good an assumption, since the error introduced can be up to 20% depending on the magnitudes of the various terms in (H-7).

In principle, a noise analysis similar to the following could be applied to each component of the total gate delay: all terms in (H-7), as well as the emitter follower. For now, keeping things simple clarifies the insight to be gained from the results and eases comparisons with results from harmonic and multivibrator jitter analyses.

Following is an analysis of three noise sources in the differential pair delay.

4.1.1 Thermal noise of load resistors

The circuit can be modeled as shown in Figure 4.2. The differential pair is represented by an ideal switch that is switched at time t=0. The noise-free exponential waveforms are shown as dashed lines in Figure 4.3, and for time t>0 are given by

$$V_{c1}(t) = -I_{EE} R_C [1 - \exp(-t/R_C C_C)] \quad (4\text{-}1)$$

$$V_{c2}(t) = -I_{EE} R_C \exp(-t/R_C C_C) \quad (4\text{-}2)$$

with $R_{C1} = R_{C2} = R_C$. The differential output signal is given by

$$V_{out}(t) = V_{c2}(t) - V_{c1}(t) = I_{EE} R_C [1 - 2 \exp(-t/R_C C_C)] \quad (4\text{-}3)$$

The definition of the delay time T_d is when the differential output voltage crosses zero. For the noise-free waveform, T_d is given by

$$V_{out}(T_d) = 0 = I_{EE} R_C [1 - 2 \exp(-T_d/R_C C_C)] \quad (4\text{-}4)$$

Solving (4-4) for T_d gives

$$T_d = \ln(2) R_C C_C \approx (0.693) R_C C_C \quad (4\text{-}5)$$

The slope of the differential output is given by taking the derivative of (4-4) with respect to time:

$$S(t) = \frac{d}{dt} I_{EE} R_C [1 - 2 \exp(-T_d/R_C C_C)] \quad (4\text{-}6)$$

$$S(t) = \frac{2 I_{EE}}{C_C} \exp(-T_d/R_C C_C) \quad (4\text{-}7)$$

And the slope at the zero crossing is given by substituting (4-5) into (4-7)

$$S(T_d) = \frac{I_{EE}}{C_C} \quad (4\text{-}8)$$

The solid lines in Figure 4.3 represent the actual collector waveforms, including the exaggerated effect of typical thermal noise waveforms $v_{n1}(t)$ and $v_{n2}(t)$ from e_{nRc1} and e_{nRc2}. By superposition, the noise waveforms simply "ride" on the ideal exponential. The result is, at the time of the ideal differential waveform zero crossing, there is a voltage error δv. This causes a time error in the threshold crossing δt.

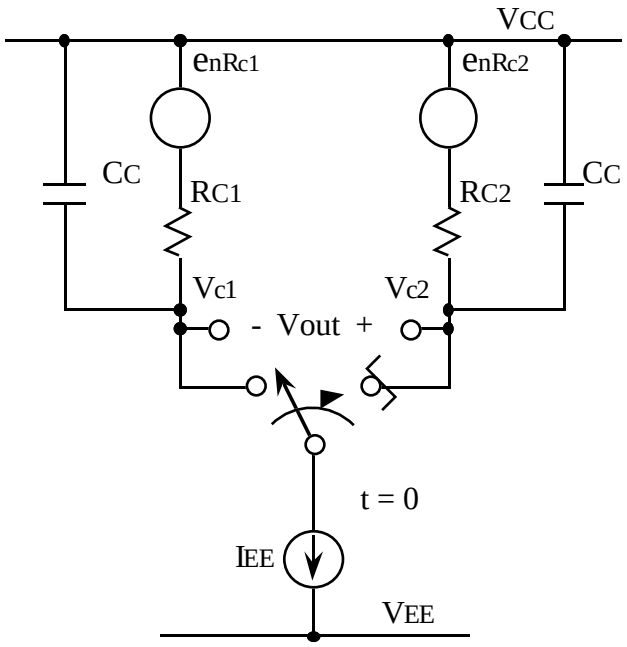


Figure 4.2. Collector resistance thermal noise model.

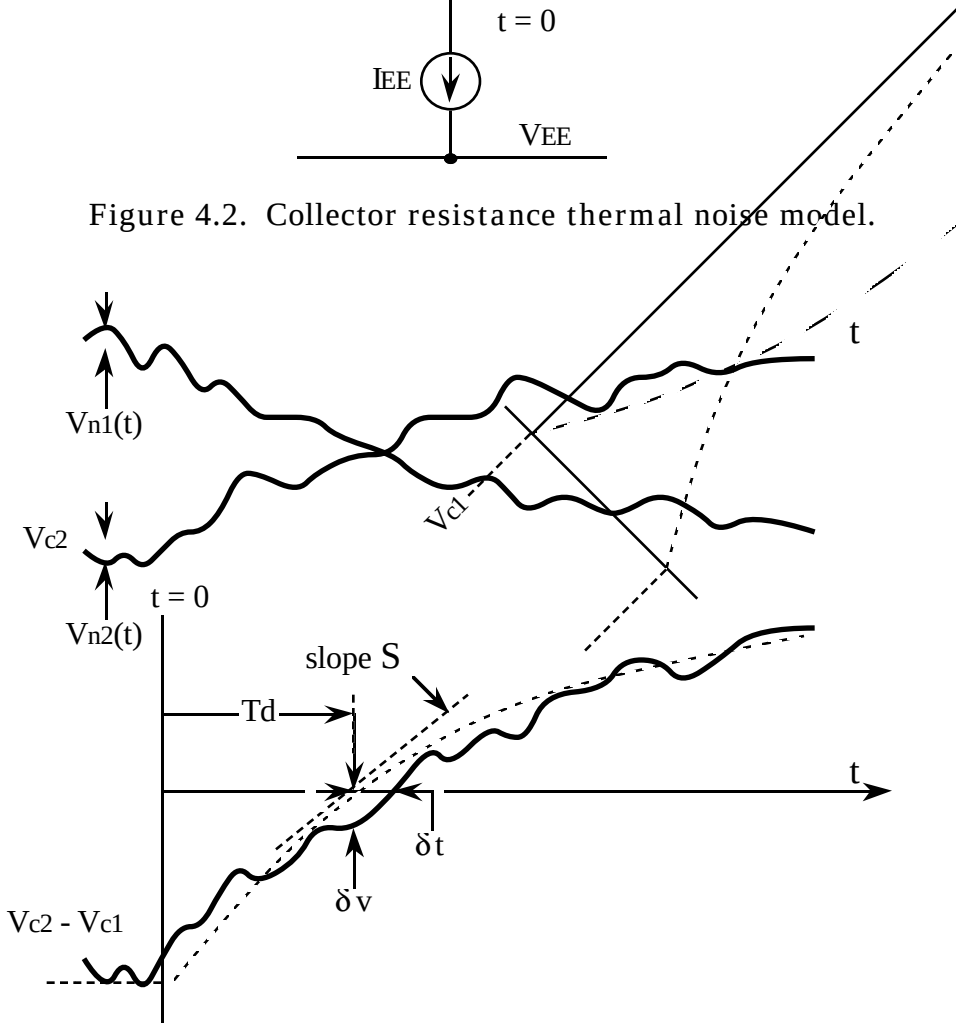


Figure 4.3. Collector resistance thermal noise waveforms.

If we assume the noise to be much less than the exponential signal, then δv and δt are related by the slope $S(T_d)$:

$$\delta t = \frac{\delta v}{S(T_d)} \tag{4-9}$$

And the standard deviations of time and voltage errors σ_t and σ_v are also related by the slope:

$$\sigma_t = \frac{\sigma_v}{S(T_d)} \tag{4-10}$$

The standard deviation of the differential voltage error is simply the root sum of the individual standard deviations σ_{v1} and σ_{v2}. These are given by the Johnson noise equation

$$\sigma_{v1} = \sigma_{v2} = \sigma = \sqrt{4\ k\ T\ R\ B} \tag{4-11}$$

where R is the resistance and B the effective noise bandwidth.

For a single pole circuit, the noise bandwidth is given by the 3-dB bandwidth multiplied by $\pi/2$ [71]:

$$B = \frac{\pi}{2}\frac{1}{2\pi RC} = \frac{1}{4RC} \tag{4-12}$$

Substituting into (4-11) gives the well known result

$$\sigma = \sqrt{\frac{k\ T}{C}} \tag{4-13}$$

With $C = C_C$ in (4-13), we have

$$\sigma_{v1} = \sigma_{v2} = \sqrt{\frac{k\ T}{C_C}} \tag{4-14}$$

and the standard deviation of the differential voltage is

$$\sigma_v = \sqrt{\frac{2\ k\ T}{C_C}} \tag{4-15}$$

Using (4-15) and (4-8) in (4-10) gives for the standard deviation of the time error (the jitter):

$$\sigma_t = \frac{\sigma_v}{S(T_d)} = \sqrt{\frac{2\ k\ T}{C_C}}\frac{C_C}{I_{EE}} \tag{4-16}$$

$$\sigma_t = \sqrt{\frac{2\ k\ T\ C_C}{I_{EE}^2}} \tag{4-17}$$

If we assume the gate delay errors to be independent, then the asymptotic κ is equal to the κ for the individual gate delay. This is given by dividing σ_t by the square root of the delay in (4-5)

$$\kappa = \frac{\sigma_t}{\sqrt{T_d}} = \sqrt{\frac{2\ k\ T\ C_C}{I_{EE}^2}} \frac{1}{\sqrt{\ln(2)\ R_C C_C}} \tag{4-18}$$

$$\kappa = \sqrt{\frac{2}{\ln(2)}} \sqrt{\frac{k\ T}{I_{EE}^2\ R_C}} \tag{4-19}$$

$$\kappa \approx (1.699) \sqrt{\frac{k\ T}{I_{EE}^2\ R_C}} \tag{4-20}$$

κ has dimensions of $\sqrt{s}$, and from (4-20) we see that this comes about by taking the square root of an energy (kT) divided by a power ($I_{EE}^2\ R_C$). The rms thermal energy kT represents an uncertainty in the energy of the collector load. $I_{EE}^2\ R_C$ represents the DC power dissipation (energy flow) in the collector load. The intuitive meaning of (4-20) is that it characterizes the gate's ability to resolve time (jitter) by an energy uncertainty (kT) as a fraction of the energy flow over time ($I_{EE}^2\ R_C$).

Equation (4-20) also indicates that jitter is improved by increasing the DC power dissipation. This is similar to the results of the noise analyses for harmonic and relaxation oscillators [30, 86].

4.1.2 Tail current noise

For noise in the tail current, the circuit can be modeled as shown in Figure 4.4. Again, the differential pair is represented by an ideal switch. The noise-free exponential waveforms are shown as dashed lines in Figure 4.5, and are as given in (4-1) and (4-2). The ideal differential output waveform, delay time, and slope at the zero crossing are also the same.

The solid lines in Figure 4.5 represent the actual collector waveforms, including the exaggerated effect of typical noise waveforms $v_{n1}(t)$ and $v_{n2}(t)$ due to the tail current noise source i_n. In this case the noise source is switched so the analysis appears to be more complicated. To make the noise contributions clearer, the actual noise waveforms $v_{n1}(t)$ and $v_{n2}(t)$ are also shown in Figure 4.5.

Again, the strategy is to determine the time error in the threshold crossing δt from the voltage error δv using the slope $S(T_d)$. The noise voltages $v_{n1}(t)$ and $v_{n2}(t)$ both contribute to δv, but in different ways.

Prior to switching, the tail current and the noise current both flow through to R_{C1}. The current noise density i_n drops across R_{C1} to give a voltage noise density, which integrated over the noise bandwidth $1/4R_CC_C$ gives a standard deviation of $v_{n1}(t<0)$ as

$$\sigma_{vn1}(t<0) = \frac{i_n}{2}\sqrt{\frac{R_C}{C_C}} \qquad (4\text{-}21)$$

As can be seen from Figure 4.5, when the switch is thrown at t=0, noise no longer affects v_{n1}, which begins an exponential decay with time constant R_CC_C. The standard deviation of v_{n1} for t>0 therefore has the form of a sampled noise term, decaying exponentially:

$$\sigma_{vn1}(t>0) = \frac{i_n}{2}\sqrt{\frac{R_C}{C_C}}\ \exp(-t/R_CC_C) \qquad (4\text{-}22)$$

At the same time as v_{n1} begins its exponential decay, v_{n2} begins growing. Analysis shows that, assuming i_n white, the standard deviation of v_{n2}

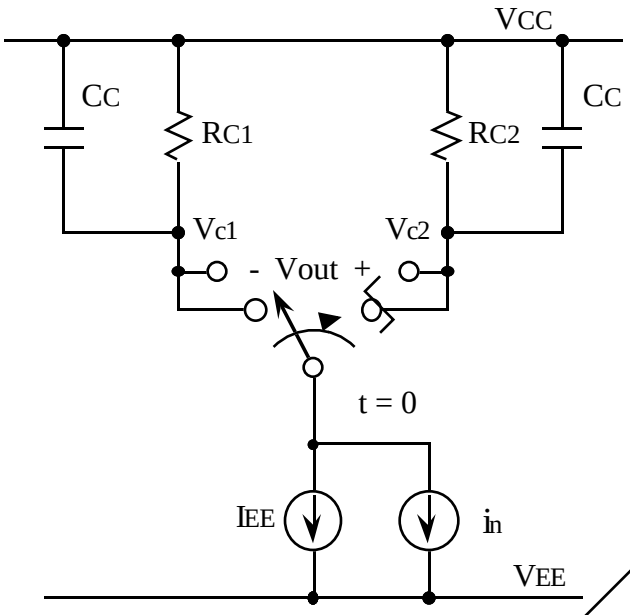


Figure 4.4. Tail current source noise model.

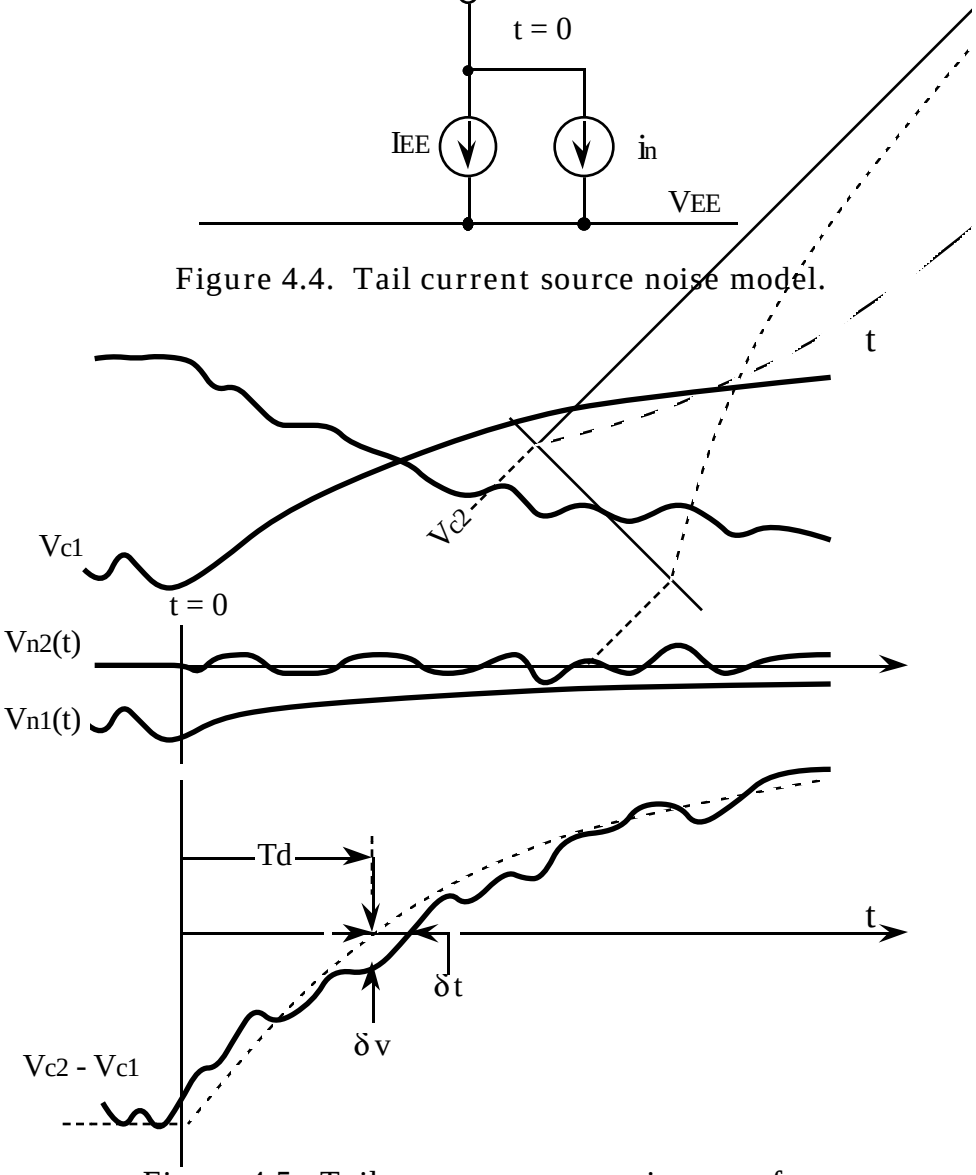


Figure 4.5. Tail current source noise waveforms.

for t>0 is given by

$$\sigma_{vn2}(t>0) = \frac{i_n}{2}\sqrt{\frac{R_C}{C_C}}\sqrt{1 - \exp(-2t/R_C C_C)} \qquad (4\text{-}23)$$

This has the form of an exponential buildup to a steady-state rms noise.

Taking the root sum of (4-22) and (4-23) to find the standard deviation of the differential voltage gives

$$\sigma_v(t) = \frac{i_n}{2}\sqrt{\frac{R_C}{C_C}}\sqrt{1 - \exp(-2t/R_C C_C) + \exp(-2t/R_C C_C)} \qquad (4\text{-}24)$$

$$\sigma_v(t) = \frac{i_n}{2}\sqrt{\frac{R_C}{C_C}} \qquad (4\text{-}25)$$

Intuitively, this makes sense, since there is only one noise source and the total thermodynamic energy uncertainty in the system must remain unchanged regardless of switching.

The standard deviation of the time uncertainty is obtained by dividing (4-25) by the slope at T_d:

$$\sigma_t = \frac{\sigma_v}{S(T_d)} = \frac{i_n}{2}\sqrt{\frac{R_C}{C_C}}\frac{C_C}{I_{EE}} \qquad (4\text{-}26)$$

$$\sigma_t = \frac{1}{2}\sqrt{R_C\, C_C}\,\frac{i_n}{I_{EE}} \qquad (4\text{-}27)$$

Again, dividing σ_t by the square root of the delay in (4-5) to get the asymptotic κ gives

$$\kappa = \frac{\sigma_t}{\sqrt{T_d}} = \frac{1}{2}\frac{\sqrt{R_C\, C_C}}{\sqrt{\ln(2)\, R_C C_C}}\frac{i_n}{I_{EE}} \qquad (4\text{-}28)$$

$$\kappa = \frac{1}{2\sqrt{\ln(2)}}\frac{i_n}{I_{EE}} \qquad (4\text{-}29)$$

In this case the $\sqrt{s}$ dimensions of κ come from dividing the current noise density (in $A/\sqrt{Hz}$) by the current. It is interesting to consider (4-29) when expressions for i_n are substituted for shot and thermal noise.

When the shot noise density

$$i_n = \sqrt{2\, q_e\, I_{EE}} \qquad (4\text{-}30)$$

is substituted into (4-29), we have

$$\kappa = \frac{1}{2\sqrt{\ln(2)}} \frac{\sqrt{2\ q_e\ I_{E\,E}}}{I_{EE}} \tag{4-31}$$

$$\kappa = \frac{1}{\sqrt{2\ \ln(2)}} \sqrt{\frac{q_e}{I_{EE}}} \tag{4-32}$$

$$\kappa \approx (0.849) \sqrt{\frac{q_e}{I_{EE}}} \tag{4-33}$$

This is similar to (4-20), where κ was given by a smallest resolvable energy as a fraction of energy flow. In (4-33), the gate's ability to resolve time is characterized by the smallest resolvable unit of charge (q_e) as a fraction of the charge flow over time (I_{EE}).

If the tail current source is degenerated, then the thermal noise density of the degeneration resistor R_E should be used:

$$i_n = \sqrt{\frac{4\ k\ T}{R_E}} \tag{4-34}$$

When this is substituted into (4-29), we have

$$\kappa = \frac{1}{2\sqrt{\ln(2)}} \frac{1}{I_{EE}} \sqrt{\frac{4\ k\ T}{R_E}} \tag{4-35}$$

$$\kappa = \frac{1}{\sqrt{\ln(2)}} \sqrt{\frac{k\ T}{I_{EE}{}^2\ R_E}} \tag{4-36}$$

$$\kappa \approx (1.201) \sqrt{\frac{k\ T}{I_{EE}{}^2\ R_E}} \tag{4-37}$$

In this case, (4-37) is similar to (4-20) in that the gate's ability to resolve time is characterized by the energy uncertainty (kT) as a fraction of the energy flow over time ($I_{EE}{}^2\ R_E$) in the element that determines the current.

Both (4-33) and (4-37) indicate that jitter is improved by increasing the DC power dissipation, similar to the result of (4-20). For lowest jitter, the current source should be degenerated so thermal noise (not shot noise) is the limiting factor.

4.1.3 Switching of input noise

The circuit of Figure 4.6 will be used for modeling the jitter effects of wideband noise at the differential pair inputs. We will assume all noise sources to be white, and lumped into a single source with density e_n.

The transfer function of a bipolar differential pair is given by

$$I_{out(diff)} = I_{EE} \tanh\left(\frac{V_{in(diff)}}{2\ V_T}\right) \qquad (4\text{-}38)$$

where tanh is the hyperbolic tangent function, and $V_T = kT/q_e$ [31]. The incremental gain is given by

$$g_m = \frac{dI_{out(diff)}}{dV_{in(diff)}} = \frac{I_{EE}}{2\ V_T}\ \mathrm{sech}^2\left(\frac{V_{in(diff)}}{2\ V_T}\right) \qquad (4\text{-}39)$$

where sech is the hyperbolic secant.

For input signals that are large compared to V_T, the gain to the output current is small. Thus the input voltage noise has little effect when the input signals are far apart.

As the input signals cross over during switching, however, the gain rises. During this time, the input voltage noise produces a noise current which is integrated on the collector capacitors. Although the integration is "leaky" due to the discharge path through R_C, some of the integrated noise still remains when the collector voltages cross approximately T_d later.

The strategy for analyzing this noise source is first to determine the standard deviation of the integrated noise current, and then determine how much of this influence remains when the output voltages cross.

Appendix I shows how this noise source can be modeled as a series of pulses of duration dt. The standard deviation of the voltage pulses is given by

$$\sigma_v = \frac{e_n}{\sqrt{2\ dt}} \qquad (4\text{-}40)$$

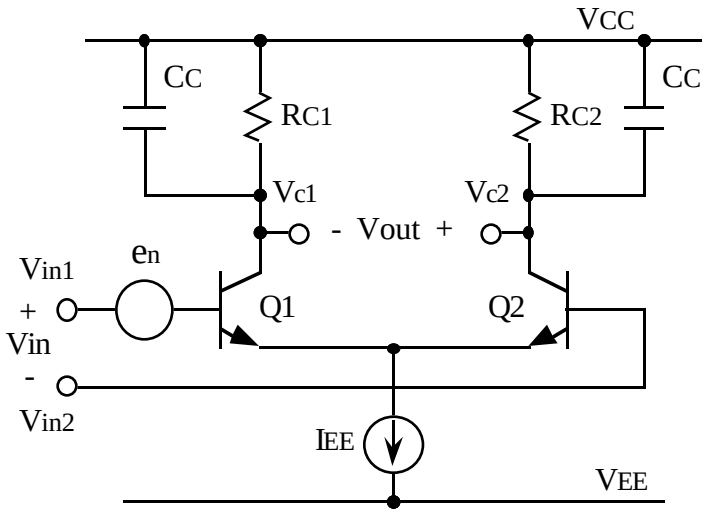


Figure 4.6. Differential input noise switching model.

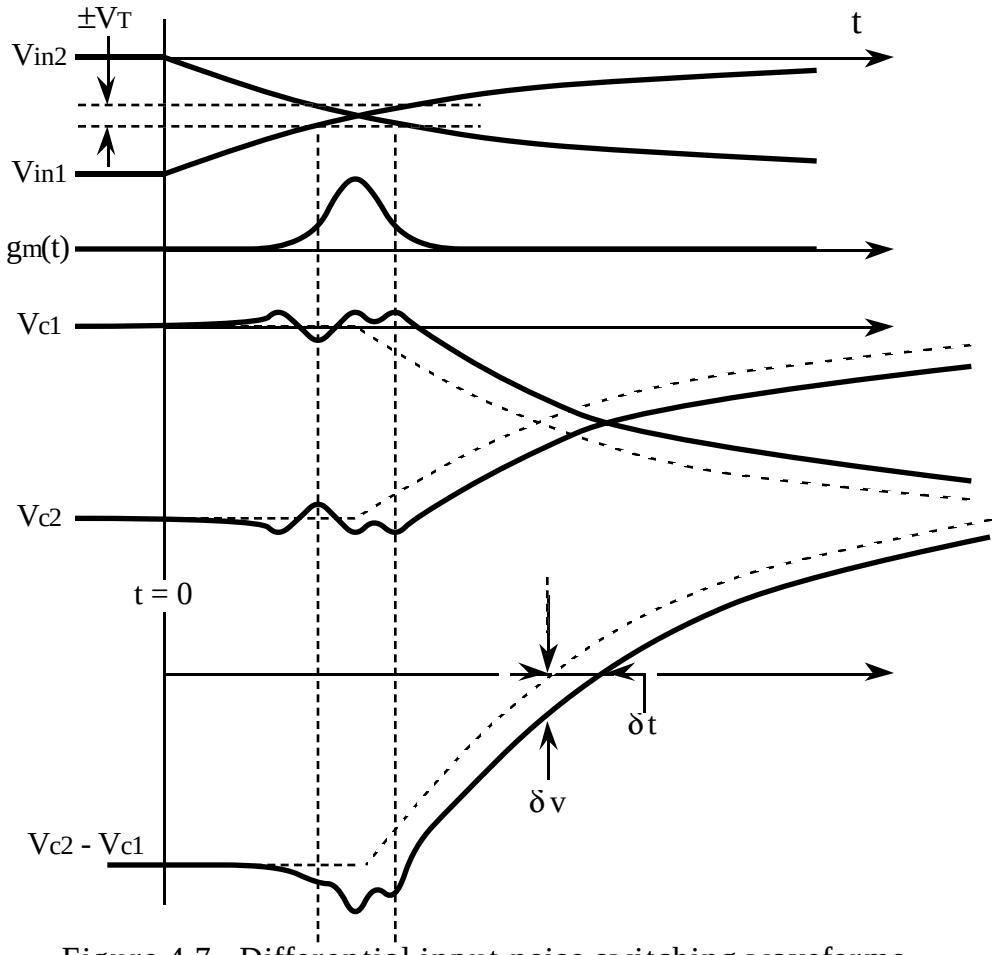


Figure 4.7. Differential input noise switching waveforms.

Each voltage pulse produces a corresponding current pulse of rms amplitude

$$\sigma_i = g_m(t)\,\sigma_v = \frac{g_m(t)\,e_n}{\sqrt{2\,dt}} \tag{4-41}$$

the standard deviation of the corresponding amount of charge is

$$\sigma_q = \sigma_i\,dt = \frac{g_m(t)\,e_n}{\sqrt{2}}\sqrt{dt} \tag{4-42}$$

The variance is

$$\sigma_q^2 = \frac{g_m(t)^2\,e_n^2}{2}\,dt \tag{4-43}$$

Assume for the moment that all charge is integrated on the capacitors, with no loss from R_C. Then the variance of the total amount of charge is simply the sum of the individual variances. In the limit as dt approaches zero (ideal white noise), the sum becomes an integral:

$$\sigma_{q(TOTAL)}^2 = \int_{-\infty}^{\infty} \frac{g_m(t)^2\,e_n^2}{2}\,dt \tag{4-44}$$

$$\sigma_{q(TOTAL)}^2 = \frac{e_n^2}{2}\int_{-\infty}^{\infty} g_m(t)^2\,dt \tag{4-45}$$

If we assume that $V_{in(diff)}$ is linear with a slope of I_{EE}/C_C over the region where $g_m(t)$ is significant, then

$$V_{in(diff)}(t) \approx \frac{I_{EE}\,t}{C_C} \tag{4-46}$$

Substituting (4-46) into (4-39) gives

$$g_m(t) = \frac{I_{EE}}{2\,V_T}\,\mathrm{sech}^2\left(\frac{I_{EE}\,t}{2\,C_C\,V_T}\right) \tag{4-47}$$

Substituting (4-47) into the integral of (4-45) gives

$$\sigma_{q(TOTAL)}^2 = \frac{e_n^2}{2}\frac{I_{EE}^2}{4\,V_T^2}\int_{-\infty}^{\infty} \mathrm{sech}^4\left(\frac{I_{EE}\,t}{2\,C_C\,V_T}\right)dt \tag{4-48}$$

To integrate (4-48), use the substitution

$$u = \frac{I_{EE}\ t}{2\ C_C\ V_T} \tag{4-49}$$

$$dt = \frac{2\ C_C\ V_T}{I_{EE}}\ du \tag{4-50}$$

Substituting gives

$$\sigma_{q(TOTAL)}^2 = \frac{e_n^2\ I_{EE}\ C_C}{2}\frac{}{2\ V_T}\int_{-\infty}^{\infty} sech^4(u)\ du \tag{4-51}$$

The definite integral in (4-51) is given by

$$\int_{-\infty}^{\infty} sech^4(u)\ du\ = \frac{4}{3} \tag{4-52}$$

Which, when substituted into (4-51), gives

$$\sigma_{q(TOTAL)}^2 = \frac{e_n^2\ I_{EE}\ C_C}{3\ V_T} \tag{4-53}$$

The rms standard deviation of charge is

$$\sigma_{q(TOTAL)} = e_n \sqrt{\frac{I_{EE}\ C_C}{3\ V_T}} \tag{4-54}$$

The standard deviation of voltage is

$$\sigma_{v(TOTAL)} = \frac{\sigma_{q(TOTAL)}}{C_C} = e_n \sqrt{\frac{I_{EE}}{3\ C_C\ V_T}} \tag{4-55}$$

This is the error voltage that is integrated onto the capacitor at the input zero crossing, during an elapsed time that is much less than the gate delay. It will decay as an exponential with time constant $R_C C_C$:

$$\sigma_v(t) = \sigma_{v(TOTAL)} \exp(-t/R_C C_C) \tag{4-56}$$

Evaluating for the contribution remaining at the output zero crossing at time $t = T_d = \ln(2) R_C C_C$:

$$\sigma_v(T_d) = \frac{\sigma_{v(TOTAL)}}{2} \tag{4-57}$$

$$\sigma_v(T_d) = \frac{e_n}{2}\sqrt{\frac{I_{EE}}{3\ C_C\ V_T}} \tag{4-58}$$

Again, the time uncertainty is obtained by dividing by the slope

$$\sigma_t = \frac{\sigma_v(T_d)}{S} = \frac{e_n}{2}\sqrt{\frac{I_{EE}}{3\ C_C\ V_T}}\frac{C_C}{I_{EE}} \tag{4-59}$$

$$\sigma_t = \frac{e_n}{2}\sqrt{\frac{C_C}{3\ I_{EE}\ V_T}} \tag{4-60}$$

And dividing by the square root of Td gives the asymptotic κ:

$$\kappa = \frac{\sigma_t}{\sqrt{T_d}} = \frac{e_n}{2}\sqrt{\frac{C_C}{3\ I_{EE}\ V_T}}\frac{1}{\sqrt{\ln(2)\ R_C C_C}} \tag{4-61}$$

$$\kappa = \frac{1}{2\sqrt{3\ \ln(2)}}\ e_n\sqrt{\frac{1}{I_{EE}\ R_C\ V_T}} \tag{4-62}$$

If we assume the noise density to be dominated by thermal noise of the total base resistance r_{bT}, then substituting the base resistance noise density expression

$$e_n = \sqrt{4\ k\ T\ r_{bT}} \tag{4-63}$$

into (4-62), and using $V_T = kT/q_e$, gives

$$\kappa = \frac{1}{\sqrt{3\ \ln(2)}}\sqrt{\frac{q_e}{I_{EE}}\frac{r_{bT}}{R_C}} \tag{4-64}$$

$$\kappa \approx (0.693)\sqrt{\frac{q_e}{I_{EE}}\frac{r_{bT}}{R_C}} \tag{4-65}$$

This is similar to (4-32) in that the gate's ability to resolve time is characterized by charge (q_e) divided by current (I_{EE}). In this case, the relative magnitude of the total equivalent base resistance r_{bT} and the collector resistance R_C impose an additional scale factor. The equivalent r_{bT} must include all wideband noise sources (emitter followers, etc.) going back to the V_{out} of the previous stage.

4.1.4 Summary of noise contributions

Values for κ have been derived for three different noise sources within a single gate delay. Assuming that gate delay errors are independent, this κ is also the asymptotic κ that can be used to predict closed loop jitter using the procedure of Chapter 2. It must be kept in mind that these equations were derived under the following simplifying assumptions:

1) The gate delay is dominated by the differential pair delay
2) The differential pair delay is dominated by the single pole time constant $R_C C_C$ of the collector load
3) The magnitude of the differential signal is greater than $V_T = kT/q_e$.
4) All noise sources are white and uncorrelated
5) The magnitude of the noise is small compared to the differential signal, so that time and voltage errors near the zero crossing are related by the slope.

Therefore there may be departure from these results to the extent that these assumptions are not met.

Since each κ represents a contribution from an independent noise voltage, the κ of all sources together is just the square root of the sum of the square contribution of the individual κs. Following is a summary of the various κs:

Collector load resistor thermal noise

$$\kappa_{R_C} \approx (1.699)\sqrt{\frac{k\ T}{I_{EE}^2\ R_C}} \tag{4-66}$$

Tail current noise:

shot noise dominated

$$\kappa_{I_{EE}} \approx (0.849)\sqrt{\frac{q}{I_{EE}}} \tag{4-67}$$

thermal noise dominated

$$\kappa_{R_E} \approx (1.201)\sqrt{\frac{k\ T}{I_{EE}^2\ R_E}} \tag{4-68}$$

Switching equivalent base resistance thermal noise

$$\kappa_{r_{bT}} \approx (0.693)\ \sqrt{\frac{q}{I_{EE}}\ \frac{r_{b\,T}}{R_C}} \tag{4-69}$$

White noise at VCO input

$$\kappa_{VCO} \approx (0.707)\ \frac{K_o}{\omega_o}\ e_n \tag{4-70}$$

4.2 Experimental Verification

4.2.1 Simulation

To test the results of the mathematical techniques used to develop equations (4-66) through (4-70), an idealized differential pair was simulated as shown in Figure 4.8. Since the simulation environment allows more control over the circuit conditions, we have the advantage of ensuring that assumptions (1) through (5) in Section 4.1.4 are met. We are also able to isolate the effects of the individual noise sources, something that would be difficult if not impossible in a physical circuit.

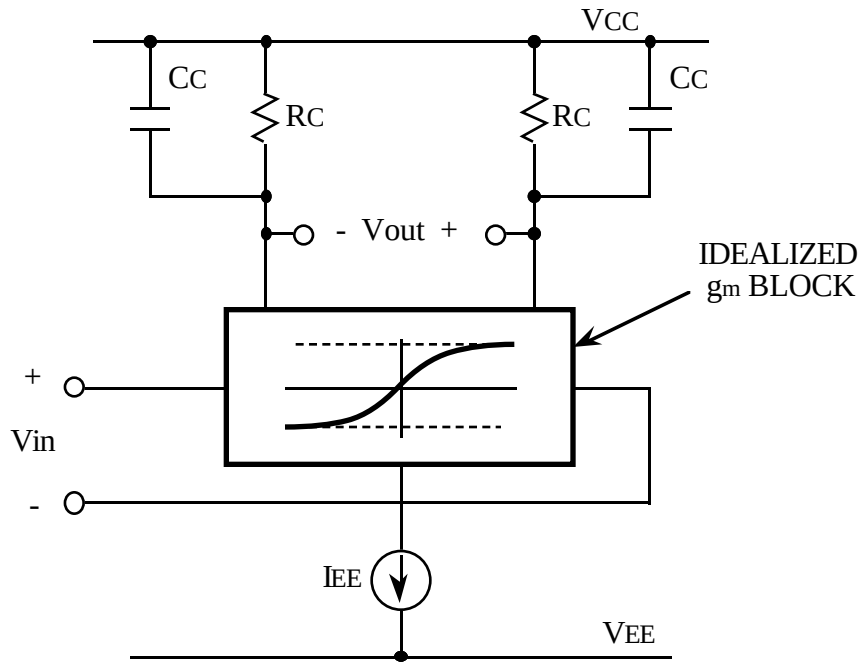


Figure 4.8. Idealized differential pair for simulation.

The noise sources were simulated using the transient noise source techniques developed in Appendix I.

Following are the results for each of the noise sources. In each case, circuit parameters were varied over an order of magnitude range around design center values.

Collector load resistor thermal noise

The simulation results are summarized in Table 4.9, and plotted in Figure 4.10. Agreement to the prediction is generally within about 10%, except when the amplitude of the signal is comparable to $V_T \approx 26mV$. In these cases the assumption that input switching is much faster than output switching is not fulfilled, and the simulated jitter is greater than the predicted. This supports the idea of making the signal as large as possible.

Tail current noise

The simulation results are summarized in Table 4.11, and plotted in Figure 4.12. Again, agreement to the prediction is generally within about 10%, except when the amplitude of the signal is comparable to $V_T \approx 26mV$. In these cases jitter is smaller, since tail current noise is a common mode error when the differential pair is balanced.

Switching equivalent base resistance thermal noise

The simulation results are summarized in Table 4.13, and plotted in Figure 4.14. Again, agreement to the prediction is generally within about 10%, except when the amplitude of the signal is comparable to $V_T \approx 26mV$. In these cases jitter is higher, since the noise has not had as much time to decay.

Summary

The simulation results generally agree with the predicted values to within 10%. The only region of significant disagreement is for signals of amplitude $\approx V_T$. This is not a limitation since lower jitter is realized with larger signal amplitudes.

R_C [kΩ]	r_{bT} [kΩ]	C_C [fF]	I_{EE} [μA]	κ [E-08 $\sqrt{sec}$] SIMULATED	PREDICTED	ERROR [%]
3.0	9.0	200	00	1.89	2.00	- 5.5
3.0	9.0	200	00	0.44	0.50	- 13.0
3.0	9.0	200	5	9.76	8.00	+22.0
12.0	9.0	200	00	1.06	1.00	+6.1
0.75	9.0	200	00	5.09	4.00	+27.0
3.0	6.0	200	00	1.76	2.00	- 12.0
3.0	2.25	200	00	1.86	2.00	- 6.8
3.0	9.0	800	00	1.78	2.00	- 11.0
3.0	9.0	50	00	1.87	2.00	- 6.5

Table 4.9. Collector resistance thermal noise simulation results.

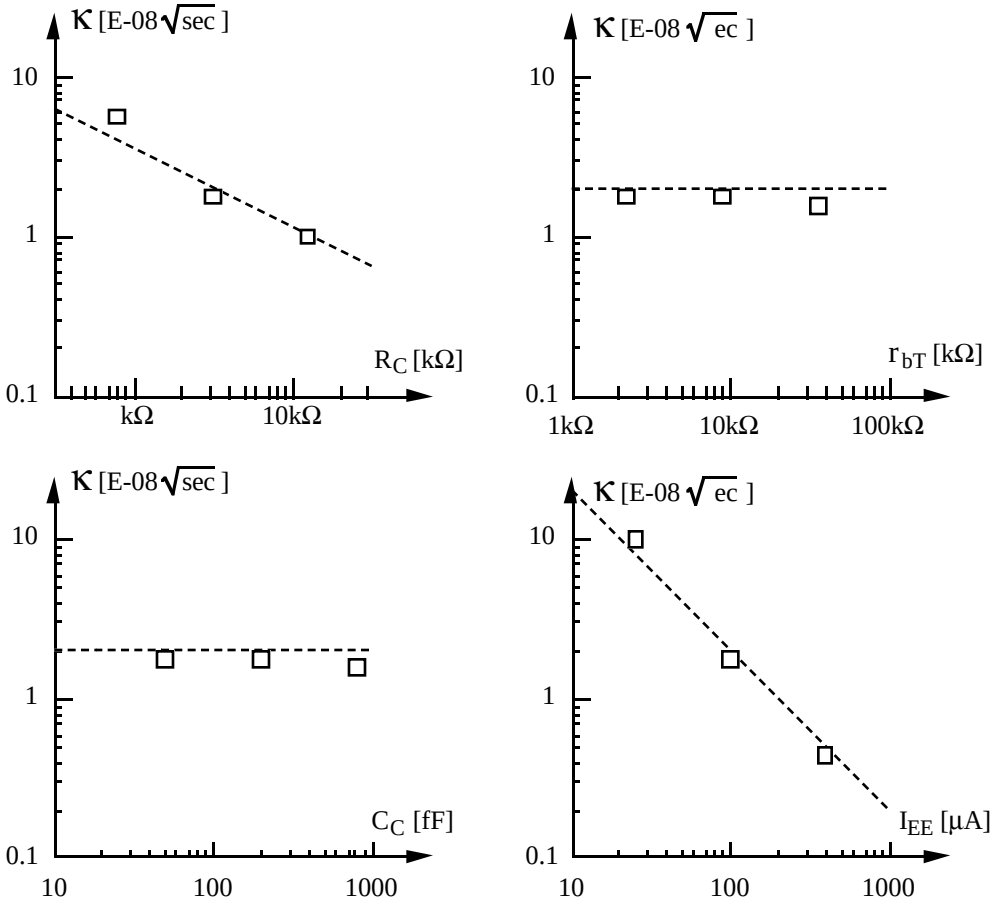


Figure 4.10. Plot of collector resistance thermal noise simulation results.

R_C [kΩ]	r_{bT} [kΩ]	C_C [fF]	I_{EE} [μA]	κ [E-08$\sqrt{sec}$] SIMULATED	PREDICTED	ERROR [%]
3.0	9.0	200	00	2.95	3.40	- 13.0
3.0	9.0	200	00	1.50	1.70	- 11.9
3.0	9.0	200	5	4.60	6.80	- 32.0
12.0	9.0	200	00	3.09	3.40	- 9.2
0.75	9.0	200	00	2.02	3.40	- 41.0
3.0	6.0	200	00	3.20	3.40	- 5.9
3.0	2.25	200	00	3.05	3.40	- 10.2
3.0	9.0	800	00	3.31	3.40	- 2.5
3.0	9.0	50	00	2.83	3.40	- 17.0

Table 4.11. Tail current noise simulation results.

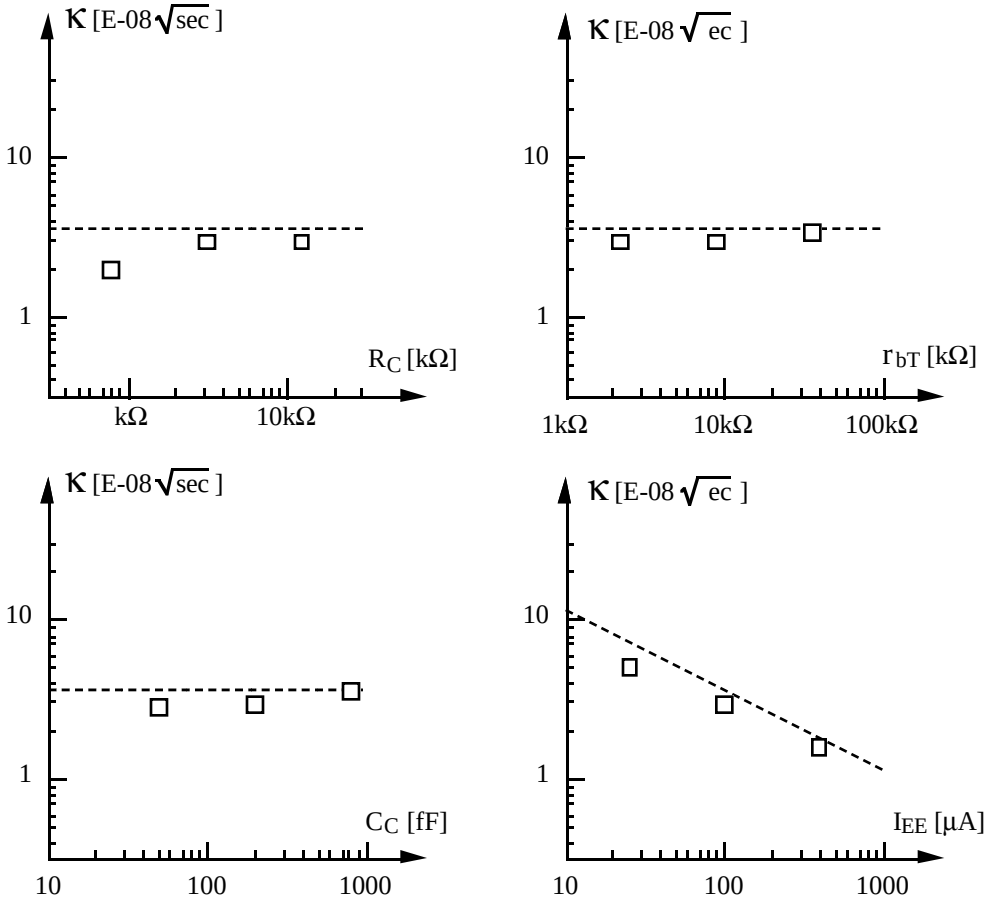


Figure 4.12. Plot of tail current noise simulation results.

R_C [kΩ]	r_{bT} [kΩ]	C_C [fF]	I_{EE} [μA]	κ [E-08$\sqrt{\text{sec}}$] SIMULATED	PREDICTED	ERROR [%]
3.0	9.0	200	00	5.43	4.81	+13.0
3.0	9.0	200	00	2.36	2.41	- 2.1
3.0	9.0	200	5	13.2	9.60	+36.0
12.0	9.0	200	00	2.28	2.41	- 5.4
0.75	9.0	200	00	12.2	9.60	+28.0
3.0	6.0	200	00	10.1	9.60	+5.1
3.0	2.25	200	00	2.48	2.41	+3.3
3.0	9.0	800	00	4.50	4.81	- 7.3
3.0	9.0	50	00	4.38	4.81	- 8.9

Table 4.13. Differential input noise simulation results.

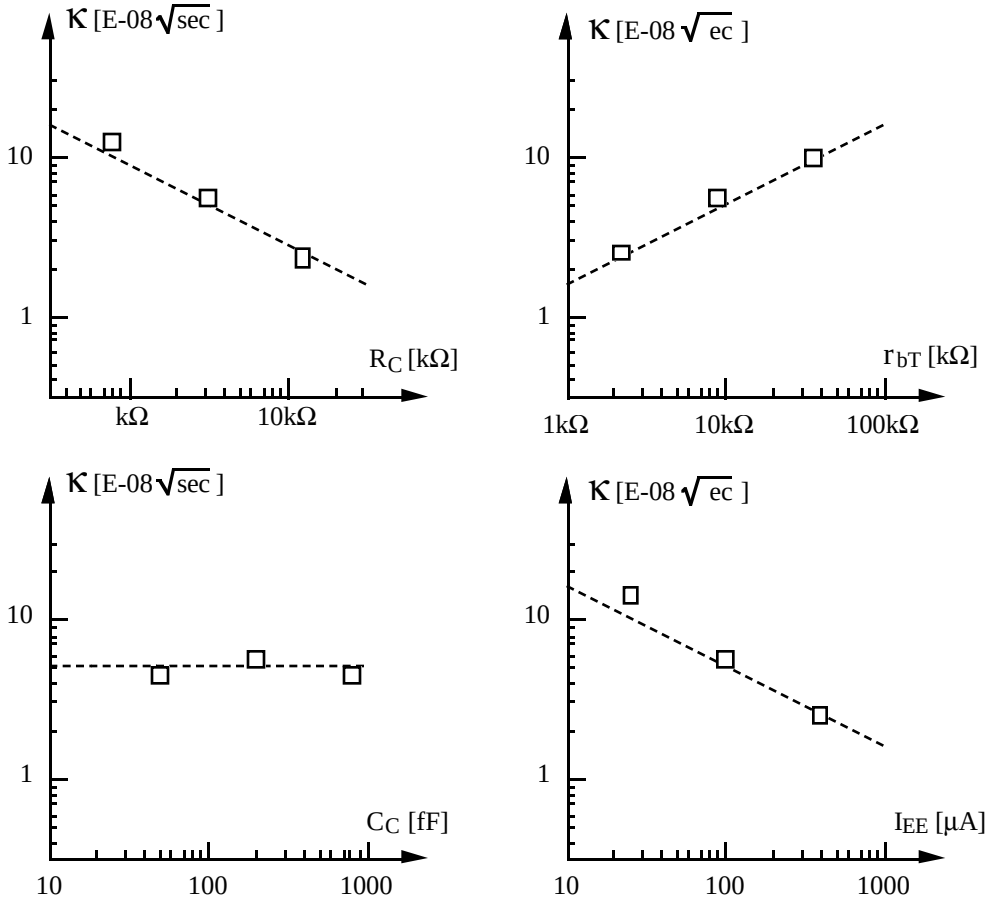


Figure 4.14. Plot of differential input noise simulation results.

4.2.2 Hardware tests

As a hardware test of this theory, ring oscillators of lengths 3, 4, 5, 7, and 9 stages were fabricated in a 3-GHz f_T Si bipolar process. Figure 4.15 shows the ring architecture; the signal path is fully differential to provide immunity to common-mode and power supply noise coupling. The gate was the simple ECL buffer as shown in Figure 4.16. The circuit is similar to that of Figure 3.22, except that in this case the regenerative switching was disabled.

Since there is no PLL involved only open loop measurements were made, in both the time and frequency domains. Table 4.17 shows the test results for center frequency as well as measured and predicted N_1 and κ. The gate delay for the 4 stage ring was significantly shorter than the other rings. This is because the other rings had a larger stray capacitance on the Q_1 and Q_2 collector nodes, due to details of the circuit implementation. This was an incidental test of κ's insensitivity to collector capacitance, which is discussed further in Section 4.3.

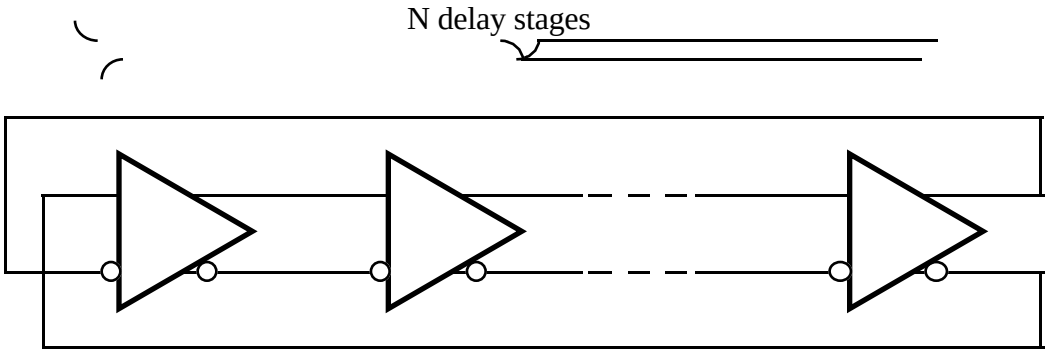


Figure 4.15. General schematic for ring experiment.

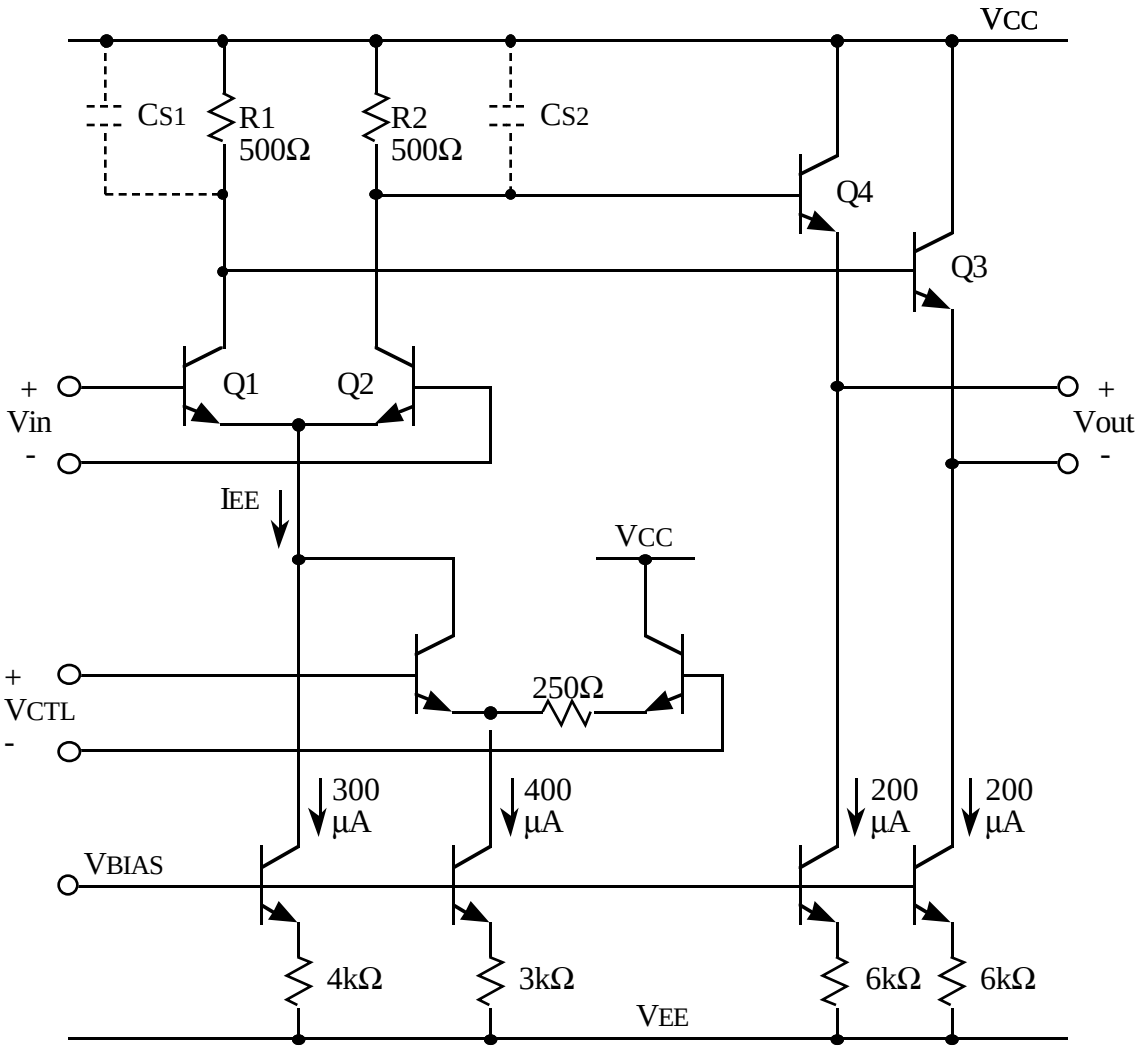


Figure 4.16. Gate delay element schematic.

Table 4.17. Ring experiment results.

RING STAGES	κ [E-08$\sqrt{s}$]	fo [MHz]	td [ps]
3	4.17	170.1	980
4	3.56	164.1	762
5	3.78	102.7	974
7	3.77	71.9	993
9	3.94	56.8	978

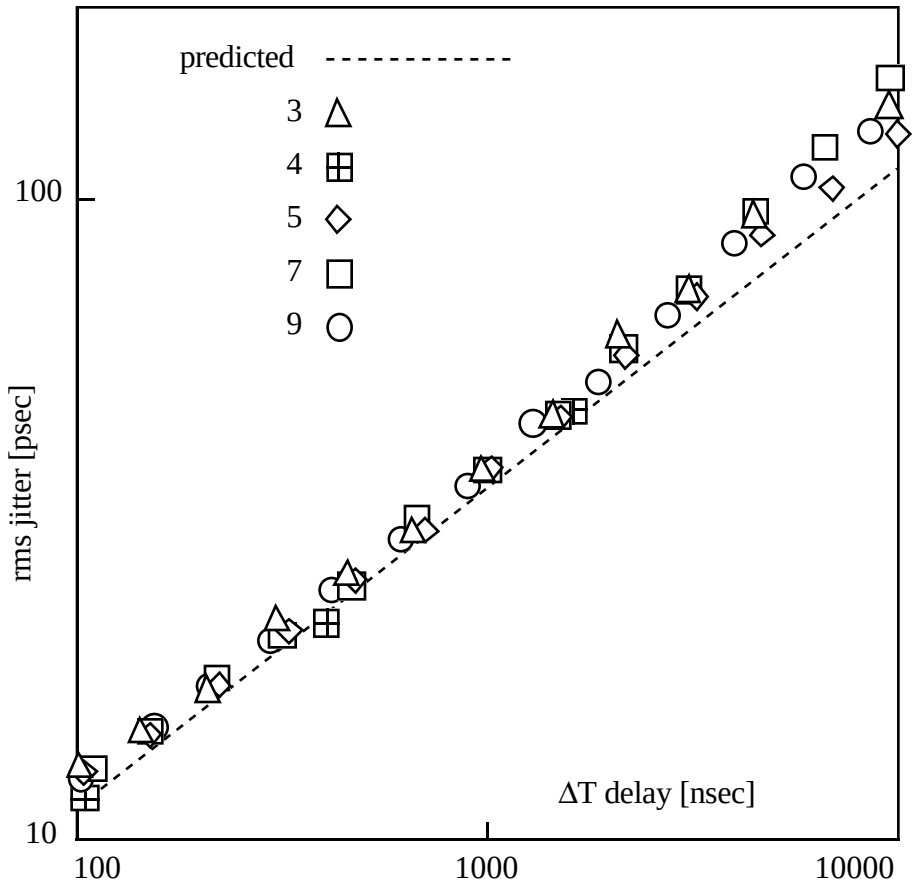


Figure 4.18. Jitter vs. delay for 3, 4, 5, 7, 9 stage rings.

Figure 4.18 shows the plots of $\sigma_{\Delta T(OL)}$ vs ΔT for the rings. The predicted value of κ, from its components, is given by substituting the circuit parameter values

$R_C = 500\ \Omega$ $\qquad$ $e_n = 11\ nV/\sqrt{Hz}$

$R_E = 4\ k\Omega$ $\qquad$ $f_o = 154.1\ MHz$

$r_{bT} = 1.65\ k\Omega$ $\qquad$ $K_o = 2.77E{+}08\ rad/V\cdot sec$

$I_{EE} = 280\ \mu A$ $\qquad$ $kT = 4.16E{-}21\ J$ at $T = 300\ K$

into equations (4-66) through (4-70). The f_o and K_o values are for the four stage ring; since the ratio is the same for all rings the κ contribution is the same as well. Substituting the numerical values gives

$$\kappa_{R_C} \approx (1.699)\sqrt{\frac{k\ T}{I_{EE}^2\ R_C}} \tag{4-71}$$

$$\kappa_{R_C} \approx (1.699)\sqrt{\frac{(4.16E{-}21\ J)}{(280\ \mu A)^2\ (500\ \Omega)}} = 1.75\ E{-}08\ \sqrt{s} \tag{4-72}$$

$$\kappa_{R_E} \approx (1.201)\sqrt{\frac{k\ T}{I_{EE}^2\ R_E}} \tag{4-73}$$

$$\kappa_{R_E} \approx (1.201)\sqrt{\frac{(4.16E{-}21\ J)}{(280\ \mu A)^2\ (4\ k\Omega)}} = 0.43\ E{-}08\ \sqrt{s} \tag{4-74}$$

$$\kappa_{r_{bT}} \approx (0.693)\ \sqrt{\frac{q}{I_{EE}}\ \frac{r_{bT}}{R_C}} \tag{4-75}$$

$$\kappa_{r_{bT}} \approx (0.693)\sqrt{\frac{(1.6E{-}19\ coul)}{(280\ \mu A)}\left(\frac{1.65\ k\Omega}{500\ \Omega}\right)} = 3.00\ E{-}08\ \sqrt{s} \tag{4-76}$$

$$\kappa_{VCO} \approx (0.707)\ \frac{K_o}{\omega_o}\ e_n \tag{4-77}$$

$$\kappa_{VCO} \approx (0.707)\frac{2.77E{+}08\ rad/V\cdot s}{2\pi\ 154.1MHz}\ 11\ nV/\sqrt{H}\,z = 0.22\ E{-}08\ \sqrt{s} \tag{4-78}$$

The total effective κ, assuming independent delays, is given by the root sum of (4-72), (4-74), (4-76), and (4-78):

$$\kappa = 3.50 \text{ E-}08 \sqrt{s} \qquad (4\text{-}79)$$

The dashed line in Figure 4.18 shows the predicted $\sigma_{\Delta T(OL)}$ corresponding to this value of κ. Good agreement is seen between this plot and the measured results.

For the 4 stage ring, jitter was also measured at different I_{EE} tail currents by changing V_{CTL} in Figure 4.16. Table 4.19 gives the measured results and the predicted κ values from (4-71) through (4-78). The results are plotted in Figure 4.20. The agreement is very good, to within 5%.

Note that the calculations in (4-71) through (4-79) assumed that delays are independent. The waveform in the gate is an unclamped exponential, and if the single pole delay model is correct then the ring should be subject to the "memory" effect discussed in Appendix G. Including this effect for the autocorrelation of the jitter process should lead to an increase over the jitter predicted by independent delays, as discussed in Section 3.2.3. Since the increase is not observed, this probably means that the single pole delay model is not completely accurate. Nevertheless, the results are in good agreement with the simple model.

Table 4.19. Measured results and predicted κ vs. I_{EE}.

I_{EE} [μA]	κ components [E-08 $\sqrt{s}$]				κ [E-08 $\sqrt{s}$]		
	κ_{rbT}	κ_{RC}	κ_{RE}	κ_{VCO}	PREDICTED	MEASURED	ERROR [%]
280	3.01	1.75	0.44	0.22	3.51	3.56	- 1.3
470	2.33	1.04	0.26	0.22	2.56	2.57	- 0.3
505	2.24	0.97	0.24	0.22	2.46	2.50	- 1.7
540	2.17	0.91	0.23	0.22	2.36	2.41	- 1.9
570	2.11	0.86	0.22	0.22	2.29	2.37	- 3.3
600	2.06	0.82	0.20	0.22	2.22	2.33	- 4.5

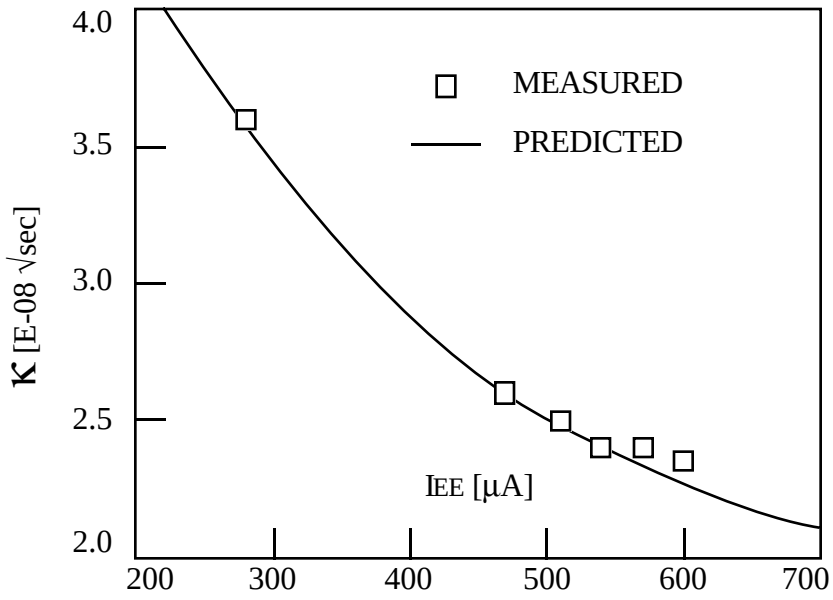


Figure 4.20. Plot of measured results and predicted κ vs. tail current I_{EE}.

4.3 Implications for design and simulation

This section discusses the result expressed in equations (4-66) through (4-70), which provide several benefits to the design process for low jitter ring oscillators.

Ring jitter dependence on circuit design values

The most important contribution of (4-66) through (4-70) is to relate circuit design parameters - component values and currents - to the figure of merit κ. Through the time/frequency technique in Chapter 2, the end user's figure of merit σ_x can be expressed as a function of κ and the loop bandwidth. Thus we can complete the link in the design process from the component values that we choose in circuit-level design, to the closed loop jitter measured by the end user at the system level.

Fundamental limits on jitter

The equations provide a simple, direct means of relating jitter performance to fundamental design parameters such as power dissipation and waveform amplitude.

For example, (4-66) and (4-68) indicate a direct link between DC power dissipation and jitter. Thus if we are designing in a low power application, we can immediately determine the best possible jitter that could be achieved at a given power dissipation.

As another example, (4-69) shows that for a given equivalent base resistance r_{bT}, there is a link between waveform amplitude $I_{EE}R_C$ and jitter. Thus if we are designing in a low voltage application with little headroom for large signal swings, we can immediately determine the best possible jitter that could be achieved at a given signal amplitude.

Identifying sources of jitter to be reduced

Since the equations give magnitudes for different sources of jitter, it is possible to determine which source is the major contributor in a given design. This allows the designer to concentrate on reducing the dominant noise sources.

The equations also ease the circuit optimization process by telling qualitatively how certain design parameters affect $\mathcal{K}$ for each source. For example, (4-66) indicates that an increase in I_{EE} will reduce $\mathcal{K}$ due to R_C by the same factor, while increasing R_C itself will provide only a square root improvement.

The equations also show the temperature dependence of jitter. This is important since it is possible to make circuit parameters (such as the tail current I_{EE}) temperature dependent as well.

$\mathcal{K}$ independent of load capacitance C_C

Note in (4-66) through (4-70), the expressions for $\mathcal{K}$ due to gate-level jitter sources, there is no dependence on the collector load capacitance C_C! This means C_C is a free parameter for designer: it can be used to design for the gate delay (and thus the ring center frequency) without affecting jitter figure of merit $\mathcal{K}$.

Also, knowledge of C_C is not necessary to confidently design for jitter characterized by a given $\mathcal{K}$. This is important since C_C may consist largely of poorly controlled stray and wiring capacitances.

Simulating jitter

The results in (4-66) through (4-70) were derived with some rather broad assumptions. For more precise predictions of jitter performance, simulation is required. Since switching of nonlinear circuit elements is involved, transient simulation with equivalent noise sources must be used. A full transient simulation of the entire ring would take much more CPU time than simulating a single gate. We would save substantial simulation time if we could predict ring performance from simulation of a single gate. In fact, with the result of the analysis in this chapter, we do this. By simulating a single gate to determine the effective $\mathcal{K}$, the (open loop) simulation result $\mathcal{K}$ can be related to the closed loop σ_x using the theory in Chapter 2.

4.4 Comparison with jitter in harmonic oscillator

This section compares κ for rings with κ derived from jitter expressions for the harmonic oscillator described in Section 3.1.1.

Recall Golay's result in (3-6) for rms frequency error:

$$\Delta f = \frac{1}{2\pi RC}\sqrt{\frac{2kT}{E_B}} \tag{4-80}$$

where E_B is the total energy dissipated in the resonator loss mechanism during the measurement interval ΔT:

$$E_B = P_B \Delta T \tag{4-81}$$

This result can be expressed in $\kappa\sqrt{\Delta T}$ form as follows:

Rutman [67] shows that the rms frequency error Δf, measured over a time interval ΔT, is related to the two sample standard deviation $\sigma_{\Delta T}$ measured over that time interval, by

$$\Delta f = f_o \frac{\sigma_{\Delta T}}{\Delta T} \tag{4-82}$$

where f_o is the average frequency. In the resonant system, this is given by (3-1), expressed here in terms of f rather than ω:

$$f_o \approx \frac{1}{2\pi\sqrt{LC}} \tag{4-83}$$

Substituting (4-81), (4-82), and (4-83) into (4-80) gives

$$\frac{1}{2\pi\sqrt{LC}}\frac{\sigma_{\Delta T}}{\Delta T} = \frac{1}{2\pi RC}\sqrt{\frac{2kT}{P_B\,\Delta T}} \tag{4-84}$$

Simplifying (4-84) and solving for $\sigma_{\Delta T}$ gives

$$\sigma_{\Delta T} = \sqrt{\frac{L}{R^2C}}\sqrt{\frac{2kT}{P_B}}\sqrt{\Delta T} \tag{4-85}$$

Substituting the expression in (3-2) for the second order system Q into (4-85) gives

$$\sigma_{\Delta T} = \frac{1}{Q}\sqrt{\frac{2kT}{P_B}}\sqrt{\Delta T} \tag{4-86}$$

Equation (4-86) fits into the $\kappa\sqrt{\Delta T}$ model with

$$\kappa = \frac{1}{Q}\sqrt{\frac{2kT}{P_B}} \qquad (4\text{-}87)$$

Note the similarity to the κ expressions for the ring oscillator, particularly those for thermal noise in (4-66) and (4-68). In all three cases, κ is proportional to the square root of a thermal energy uncertainty (kT) divided by an average power dissipation. In the harmonic oscillator case, however, κ is improved by a factor of Q. The intuitive explanation is that the peak power flow is much greater than the average dissipation P_B, due to the energy storage in the resonator elements.

To summarize, consider a harmonic oscillator with average power dissipation P_B, and a ring oscillator that dissipates an average power of P_B per stage. *The jitter performance of the harmonic oscillator as characterized by κ will be better than the ring by a factor of approximately Q*. Conversely, for the ring to achieve jitter performance as good as the harmonic oscillator, *its average power dissipation must be much higher: approximately Q· P_B per stage*.

This implies that attempts to realize low jitter by synthesizing a high Q with active elements will not work. To realize low κ, we must have the high peak power flow that can only be achieved with actual resonant energy storage elements.

The result of (4-87) can also be obtained directly from the bandpass noise spectrum and the time/frequency technique of Chapter 2. In the open loop frequency domain, we can determine an effective value of N_1 as follows:

Consider the model of the resonator shown in Figure 4.21. The LC impedance has been approximated using (3-5), expressed here in terms of offset frequency f rather than ω-ω_o:

$$Z \approx \frac{1}{j\ 4\pi f\ C} \qquad (4\text{-}88)$$

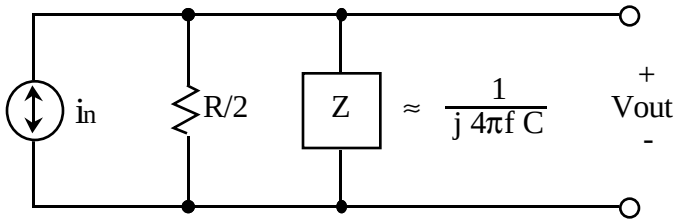


Figure 4.21. Noise model of resonator.

This approximation is valid for offset frequencies greater than f_o/Q.

The voltage noise density at the output is given by [71]

$$e_{n(out)} = i_n |Z| = \sqrt{\frac{4kT}{R/2}} \frac{1}{4\pi f\ C} \left[\frac{V}{\sqrt{Hz}}\right] \tag{4-89}$$

In terms of power dissipated in resistor R/2, we have

$$P_{n(out)} = \frac{e_{n(out)}^2}{R/2} = kT \frac{1}{(\pi fRC)^2} \left[\frac{W}{Hz}\right] \tag{4-90}$$

Here we must recognize the ambiguity of the magnitude spectrum: the p.s.d. in (4-90) makes no distinction between phase noise power and amplitude noise power. Since we have placed no special restrictions on the resonator circuit, let us assume that the power is equally distributed between phase and amplitude noise [66]. Then the phase noise power density is half of (4-90):

$$P_{\phi n(out)} = \frac{P_{n(out)}}{2} = \frac{kT}{2} \frac{1}{(\pi fRC)^2} \left[\frac{W}{Hz}\right] \tag{4-91}$$

N_1 is defined in terms of $S_{\phi OL}(f)$, the p.s.d. normalized to the carrier power. In this case, dividing (4-91) by the average power dissipation P_B gives

$$S_{\phi OL}(f) = \frac{kT}{2\ P_B} \frac{1}{(\pi RC)^2} \frac{1}{f^2} \quad [Hz^{-1}] \tag{4-92}$$

This fits into the the N_1/f^2 model, with:

$$N_1 = \frac{kT}{2\ P_B} \frac{1}{(\pi RC)^2} \tag{4-93}$$

N_1 is related to κ by (2-17); with f_o from (4-83) we have

$$\kappa = \frac{\sqrt{N_1}}{f_o} = \sqrt{\frac{kT}{2\ P_B}} \frac{1}{\pi RC}\ 2\pi \sqrt{LC} \tag{4-94}$$

$$\kappa = \sqrt{\frac{2kT}{P_B}} \sqrt{\frac{L}{R^2C}} \tag{4-95}$$

Using the second order Q of (3-2) in (4-95) gives

$$\kappa = \frac{1}{Q} \sqrt{\frac{2kT}{P_B}} \tag{4-96}$$

which is the same as (4-87), which was derived from Golay's result.

Golay's analysis proceeded entirely in the frequency domain, giving an rms frequency error in (4-80). Rutman's result in (4-82) allowed us to determine the time domain figure

of merit κ. Alternatively, using the chapter 2 time/frequency technique on the phase noise p.s.d. of (4-92) gives a direct path to κ in (4-96). The convergence to the same result provides a confirming link between the classical frequency domain analysis techniques from harmonic oscillators, and the more general approach developed in Chapters 2 and 3.

4.5 Chapter summary

This chapter has developed expressions for predicting jitter in a ring oscillator composed of differential pair delay gates. The time domain figure of merit κ, introduced in Chapter 2, provides the link to system-level jitter performance measures. With the aid of some powerful but reasonable assumptions, the resulting expressions show simple relations between noise sources and the resulting jitter. Expressions were developed for jitter due to thermal noise in the collector load resistance, shot or thermal noise in the tail current source, and switching of wideband thermal noise at the differential pair inputs. The expressions were verified with both simulation and experimental results. Comparison with the result of harmonic oscillator analysis showed convergence to the same result.

5. Design of low jitter VCO for AD806

This chapter covers the design of the low jitter voltage controlled ring oscillator for the AD806, the clock and data recovery PLL that improves on the performance of the AD802.

5.1 VCO Requirements

In this section, we first consider the requirements for the VCO that flow down from the system level. Following is a discussion of the basic ring VCO design, and then modifications of the basic design that were required.

5.1.1 Low jitter

The most important performance measure for the VCO is jitter. The desired σ_x for this design was approximately 20 ps rms, which is 0.3% of a unit interval or slightly more than 1° of phase.

The fundamental limit on jitter is thermal noise, but this is by no means the dominant source of jitter in practical VCOs. To preserve low jitter performance, care must be taken to minimize sensitivity of frequency to voltages other than the control voltage. In many high frequency VCOs most of the output "jitter" is actually modulation due to sensitivity to high frequency power supply variations.

5.1.2 Very low duty cycle distortion

This is important for proper operation of the PLL phase detector. This can be seen from the timing diagram in Figure 1.3. The phase detector tries to align rising edges of the VCO clock to data transitions, whereas the sampling of the data occurs on falling edges of the VCO clock. Any error in duty cycle translates directly into a phase error at the VCO output.

5.1.3 Quadrature

The frequency detector used in this PLL requires two clock signals in quadrature [20]. Maintaining a precise quadrature relationship is not critical. As will be seen in Section 5.2, the design approach used for this VCO provides good quadrature performance.

5.1.4 Control constant linearity

Ideally the output frequency is linearly related to the control voltage:

$$f_{OUT} = f_o + \frac{K_o}{2\pi} V_{CTL(diff)} \qquad (5\text{-}1)$$

where K_o is the control constant with units rad/V· s.

In reality, the V-to-f relationship will have some nonlinearity, and the slope of the V-to-f characteristic will vary. K_o then will not be constant but will depend on the control voltage. This variation should be avoided, since closed loop performance parameters of the PLL (for example, loop bandwidth) depend on K_0. For the same reason, K_0 should be as independent of temperature, power supply, and process variations as possible.

5.1.5 Low power

Reducing power makes the end product more attractive from a system point of view. The dielectrically isolated bipolar "XFCB" process [106] used for the AD806 features very small device geometries, down to 1.5µm x 1.5µm emitter areas. With the associated low capacitances, 155MHz operation can be obtained even at low collector currents of order 100µA. Unfortunately, as shown in Chapter 4, there is a tradeoff involved since low power operation may result in higher jitter.

5.2 Ring oscillator design

Following is the development of the basic design of the ring VCO with quadrature outputs.

5.2.1 Development of basic ring

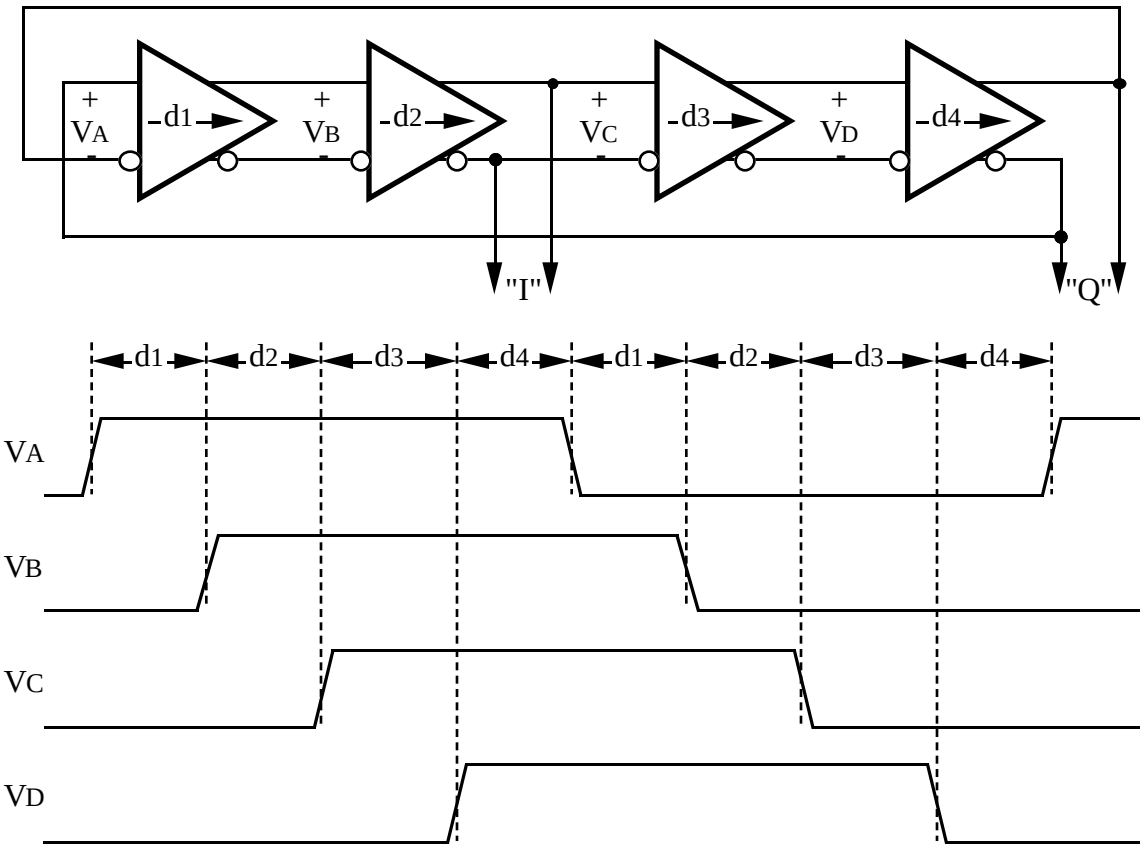


Figure 5.1. 4 stage ring schematic.

Figure 5.1 shows a four stage ring composed of differential logic gates. For oscillation to occur, there must be a net inversion around the ring; this is achieved with a wire inversion since the ring has an even number of stages. The oscillator completes one period when an edge goes around the ring twice. The frequency is determined by the delay in each of the gates:

$$f_{OUT} = \frac{1}{T} = \frac{1}{2(d_1 + d_2 + d_3 + d_4)} \qquad (5\text{-}2)$$

Note from the timing diagram in Figure 5.1 that the ring inherently provides a 50 % duty cycle, fulfilling the requirement in Section 5.1.2. Note also that V_A and V_C will be in quadrature to the extent that $d_1 + d_2 = d_3 + d_4$. This fulfills the requirement of Section 5.1.3.

Usually the frequency is controlled by making the delay depend on the control voltage - for example, having the control voltage change a current in the gate which affects the gate delay [17, 48]. The problem with this approach is that it is usually susceptible to common mode influences (most importantly, power supply voltage variations) which can also change the gate delay. This leads to modulation of the output frequency and increased jitter.

An alternative method uses gates with constant delay, and varies delay around the ring by taking a linear interpolation of signals at different stages in the ring [23, 45, 79]. The basic circuit used in this PLL uses an interpolating circuit [45] shown in Fig 5.2. This interpolating approach to realizing a voltage controlled phase delay can be traced back at least as far as the Armstrong modulator [3].

There are two differential signal pair inputs to the interpolator, one called "fast" and the other "slow." Ideally, the output is a linear combination of the two inputs

$$V_{OUT} = x\, V_{SLOW} + (1-x)\, V_{FAST} \qquad (5\text{-}3)$$

where x $(0 < x < 1)$ is a fraction determined solely by the differential control voltage $V_{CTL(diff)}$.

Referring to Figure 5.2: when $V_{CTL(diff)}$ is very negative ($< -I_B \cdot R_D$), $I_{SLOW} \approx 0$ and $I_{FAST} \approx I_B$. Q_{1A} and Q_{1B} are off; V_{OUT} is determined by Q_{2A} and Q_{2B} processing the V_{FAST} signal, and $x = 0$. Conversely, when $V_{CTL(diff)}$ is very positive, Q_{2A} and Q_{2B} are off; V_{OUT} is determined by the V_{SLOW} signal, and $x = 1$. When $V_{CTL(diff)} = 0$ (which ideally would be at the VCO center frequency), $I_{SLOW} \approx I_{FAST} \approx I_B/2$. V_{OUT} will be an equally weighted interpolation between the V_{FAST} and V_{SLOW} signals, and $x = \frac{1}{2}$.

Also shown in Figure 5.2 is an idealized timing diagram (assuming no delay in the interpolator). If the delay between the fast and slow inputs is of order of the signal rise time, the linear combination of amplitude is also a linear interpolation in delay. That is, if the delay difference between the fast and slow input is d_{FS}, the delay from V_{FAST} to V_{OUT} is $x \cdot d_{FS}$.

Figure 5.3 shows the basic design of the VCO with the interpolator block, including the delay of the interpolator itself. The ring is composed of two identical halves so that quadrature outputs are available. The advantage of using the interpolator is that, if the gate delays can be made independent of common mode influences (such as supply variations), then the delay around the ring is determined only by the differential voltage $V_{CTL(diff)}$. Hence we can achieve control of the frequency by purely differential means, while maintaining immunity to common mode influences.

Now the frequency is given by

$$f_{OUT} = \frac{1}{4\,(d_1 + x\,d_2 + d_3)} \tag{5-4}$$

The center frequency is given by

$$f_o = f_{OUT}(x = \tfrac{1}{2}) = \frac{1}{4\,d_1 + 2\,d_2 + 4\,d_3} \tag{5-5}$$

An analysis of the degenerated pair Q3A/Q3B gives x in terms of $V_{CTL(diff)}$:

$$x = \frac{I_{SLOW}}{I_B} = \frac{V_{CTL(diff)}}{2 \cdot I_B \cdot R_D} + \frac{1}{2} \tag{5-6}$$

which is valid for the linear range of the degenerated pair

$$|V_{CTL(diff)}| < I_B \cdot R_D \tag{5-7}$$

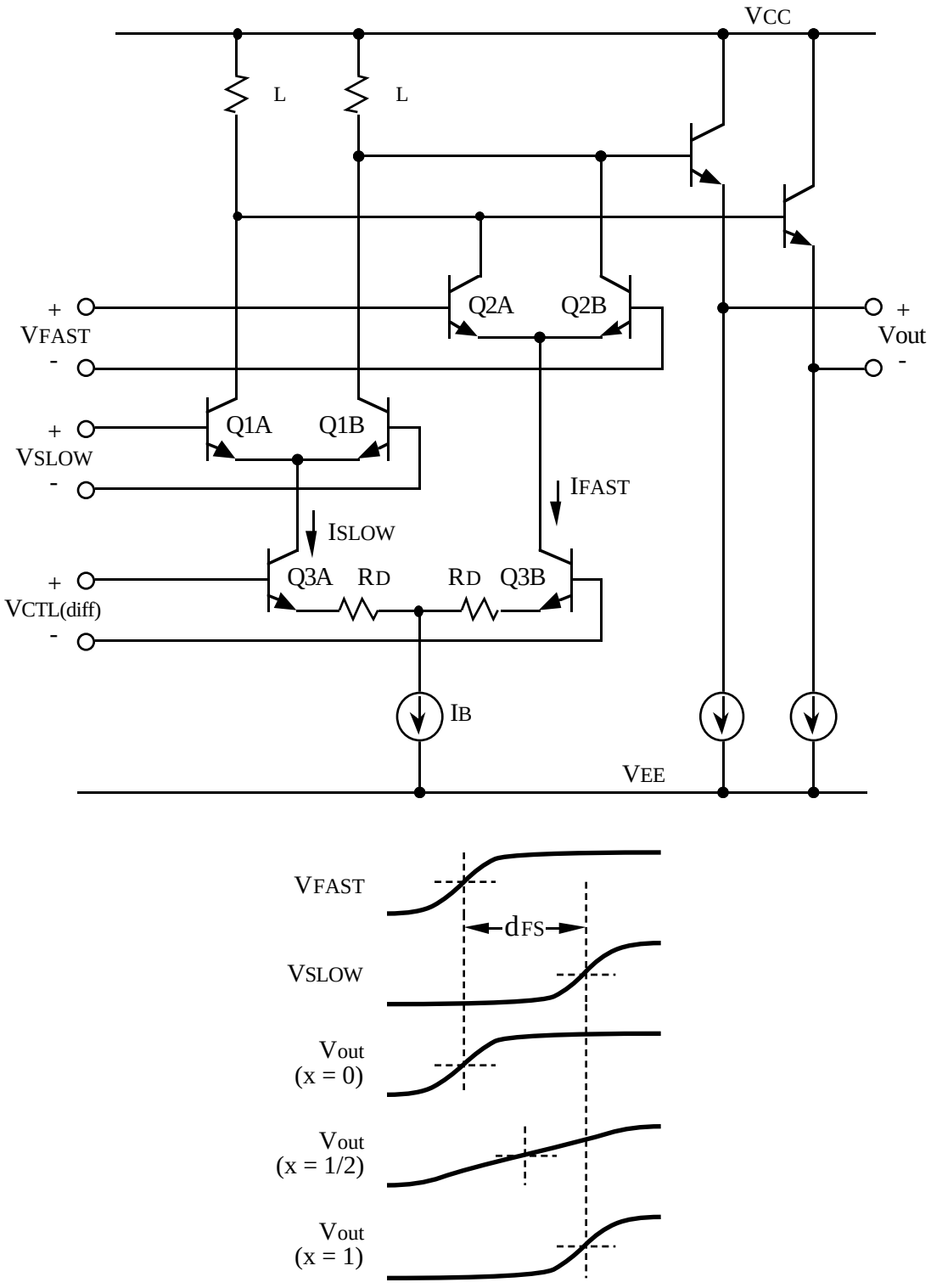


Figure 5.2. Interpolating circuit.

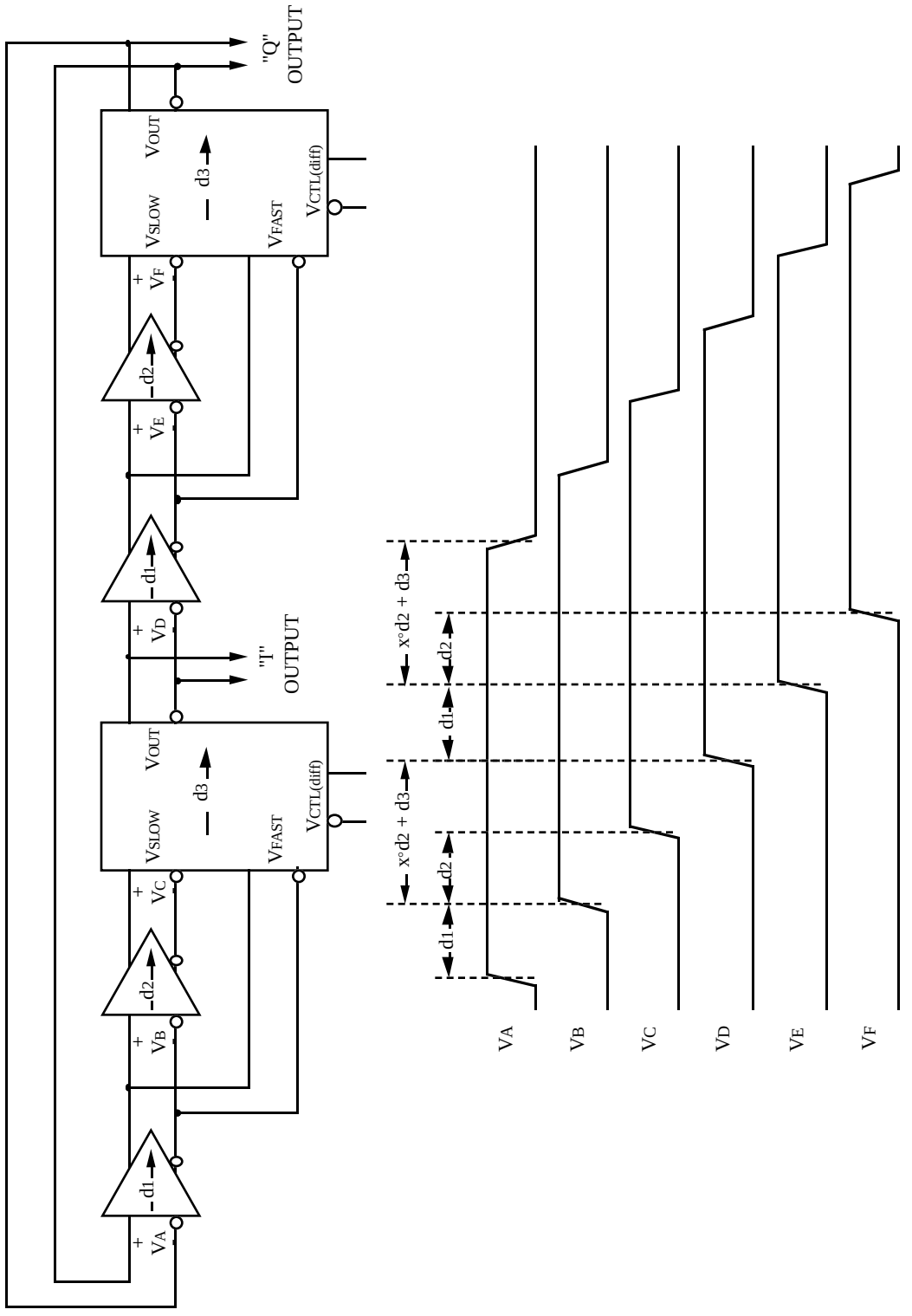


Figure 5.3. Quadrature ring VCO block diagram.

5.2.2 Drawbacks to the ring oscillator architecture

Control characteristic inherently nonlinear

A disadvantage of the interpolator VCO is that the control characteristic is inherently nonlinear with respect to x, which means that K_0 is not constant [79]. This can be seen by taking the derivative of (5-4):

$$K_o(x) = \frac{df_{OUT}}{dx} = \frac{-d_2}{4\,(d_1 + x\,d_2 + d_3)^2} \tag{5-8}$$

The magnitude of the problem can be better understood by considering it in terms of the VCO tuning range. By substituting $x = 0$ and $x = 1$ into (5-4), we see that the ratio of maximum to minimum frequency is

$$\frac{f_{MAX}}{f_{MIN}} = \frac{d_1 + d_2 + d_3}{d_1 + d_3} \tag{5-9}$$

The change of slope over this range is found by similarly substituting $x = 0$ and $x = 1$ into (5-8), giving

$$\frac{K_{0MAX}}{K_{0MIN}} = \frac{(d_1 + d_2 + d_3)^2}{(d_1 + d_3)^2} = \left(\frac{f_{MAX}}{f_{MIN}}\right)^2 \tag{5-10}$$

From (5-10) we see that if we desire a tuning range ρ, the slope of the characteristic will vary by a factor of ρ^2 over that range. For the tuning range of ± 10% required for this PLL, ρ^2 is given by

$$\rho^2 = \left(\frac{1.1}{0.9}\right)^2 = 1.49 \tag{5-11}$$

This change in slope of almost 50% is unacceptably high, since it causes a similarly large change in the loop bandwidth.

Another problem is that (5-4) is not symmetric with respect to frequency: that is, the "center frequency" corresponding to $x = \frac{1}{2}$ is not midway between f_{MIN} and f_{MAX}. Figure 5.4 shows a plot of normalized frequency and control constant vs. x for a ±10% tuning range.

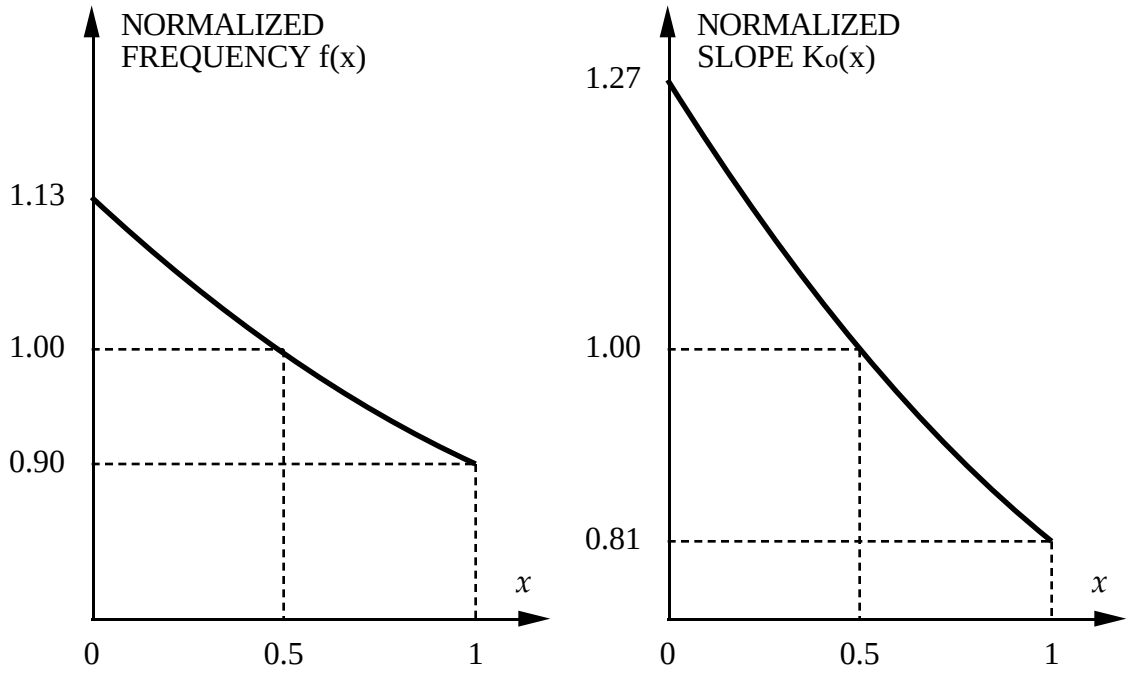


Figure 5.4. Nonlinearity of interpolating VCO V-to-f characteristic.

Frequency dependence on gate delay

The gate used in the ring is a simple ECL differential pair, shown in Figure 5.5. We have assumed that most of the delay through the gate is due to the $R_C C_C$ time constant of the collector load. Center frequency is set by trimming the effective R_C. (A minor disadvantage is that the trim is cumbersome since all gates must be trimmed by the same amount; this is realized with link trims).

Some of the gate delay, however, is due to the switching speed of the differential pair. The absolute switching time is not a well controlled parameter and depends on several conditions as shown in Appendix H. The two most troublesome influences on gate delay were temperature and changing tail current coupled from supply voltage variations.

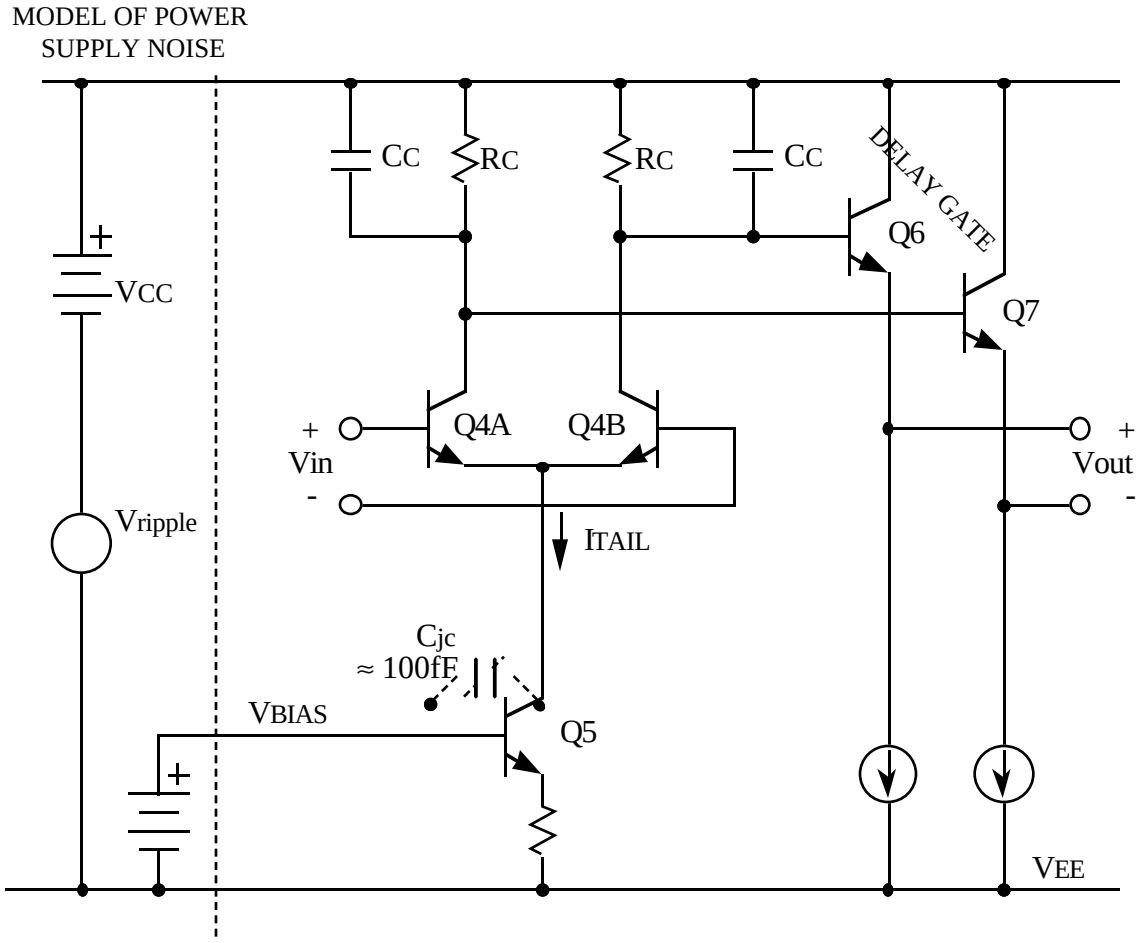


Figure 5.5. Gate schematic with C_{jc} stray capacitance.

As indicated in Appendix H, the temperature dependence of f_T causes a second order dependence of switching time on temperature. In simulation, this caused a center frequency drift of close to 20% for a 2:1 variation in absolute temperature, from -60°C to +140°C. This drift was equal to the tuning range and would have left no margin for other frequency error sources.

The switching time also shows a second order dependence on tail current, through its influence on f_T. Ideally the DC collector current of Q_5 would be the sole component of the tail current for the Q_{4A}/Q_{4B} differential pair. However, if there is AC noise on the power supply rail, the changing voltage across Q_5's base-collector capacitance C_{jc} couples an AC current onto I_{TAIL}. Since the switching time depends somewhat on the tail current, this leads to a modulation of the delay (and the ring frequency) by the power supply voltage. This will seriously degrade jitter performance and must be avoided if at all possible.

5.2.3 Improvements to ring oscillator

Three of the major design issues from the previous section were addressed in the improved design:

- Reduce tail current sensitivity to AC ripple on power supply
- Reduce delay sensitivity to temperature
- Linearize V-to-f characteristic

Following is a discussion of the design steps that were taken to improve performance in these areas.

Reduce tail current sensitivity to AC ripple on power supply

Sensitivity to power supply ripple was reduced with the decoupling network shown in Figure 5.6. Capacitor C_{BP} (of order 1 pF) provides a low impedance path to shunt AC current away from the differential pair; R_{BP} (of order 10 kΩ) raises the output impedance of the current source as seen by the differential pair. This also has the advantage of making the thermal noise of R_{BP} the dominant source of tail current noise, rather than the shot noise of Q5.

Reduce delay sensitivity to temperature

Sensitivity of delay to temperature was reduced by making the tail current proportional to absolute temperature (PTAT). The PTAT bias currents were developed using a bandgap voltage reference [12]. In simulation, this was empirically observed to reduce the delay drift by a factor of four.

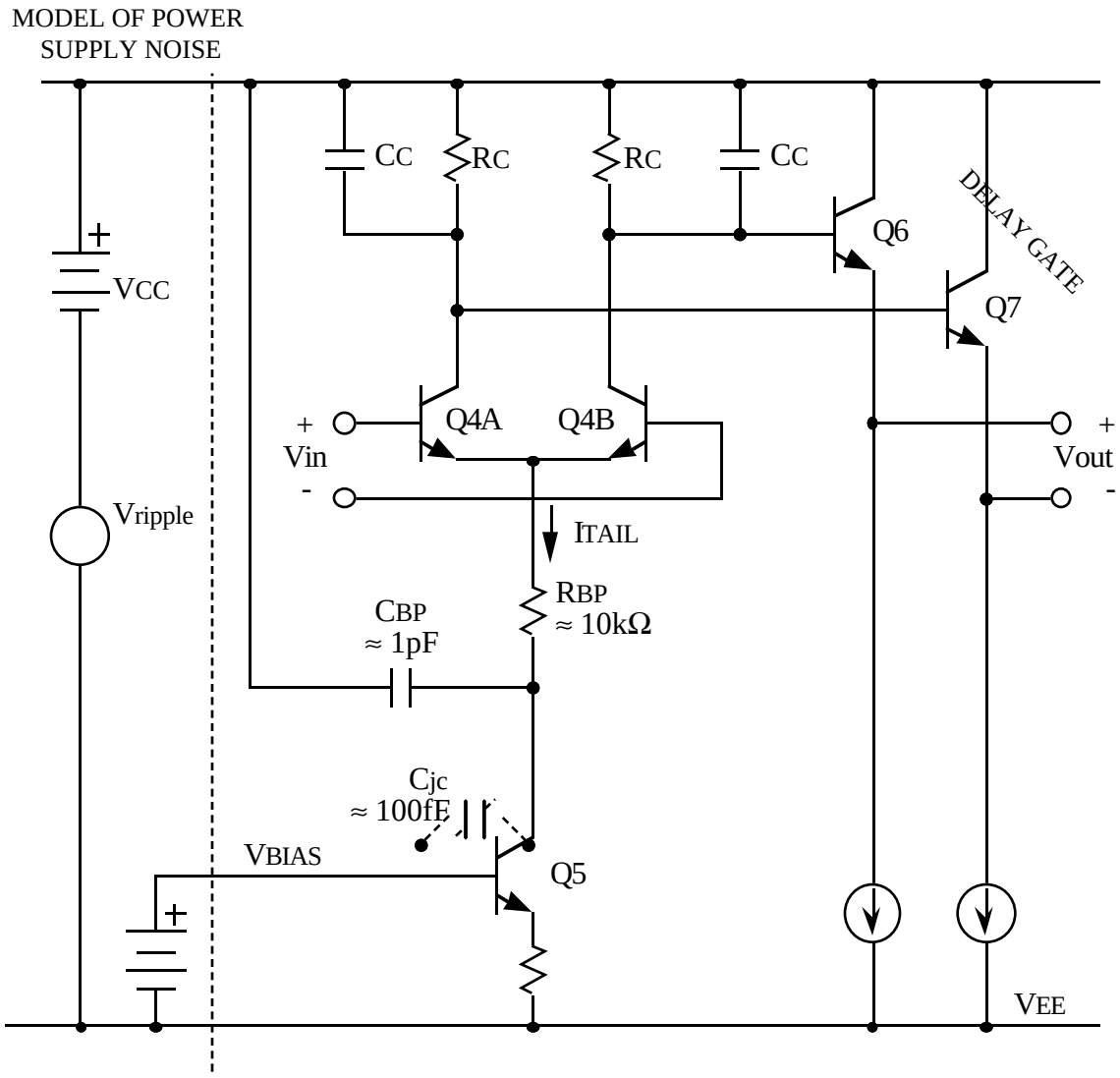


Figure 5.6. Gate schematic with bypass network.

Linearize V-to-f characteristic

Linearization of the V-to-f characteristic was realized by introducing a compensating nonlinearity in the transfer characteristic of the $V_{CTL(diff)}$ to fraction x circuit. The resulting circuit is shown in conceptual form in Figure 5.7. The circuit makes use of the translinear principle [28], which allows introduction of a well controlled nonlinearity by unbalancing the emitter areas of a differential pair.

The ±10% frequency tuning range at the VCO control input corresponds to a ±200mV voltage range for $V_{CTL(diff)}$. The saturation limit of the Q_{8A}/Q_{8B} degenerated pair set by $I_B \cdot R_D$ was chosen to be ±300mV to avoid any nonlinearity near the transition to the limit of linear operation. From (5-6), this means that x will range from 1/6 to 5/6 (rather than 0 to 1). Figure 5.8 shows the transfer characteristic from $V_{CTL(diff)}$ to currents I_{FAST} and I_{SLOW}. Also shown in Figure 5.8 is the desired characteristic for I_{FAST}' and I_{SLOW}', which are compensated for the inherent V-to-f nonlinearity shown in Figure 5.4. Compensation is achieved by using I_{SLOW}' and I_{FAST}' as the tail currents for Q_{1A}/Q_{1B} and Q_{2A}/Q_{2B} respectively in the interpolator circuit of Figure 5.2.

The amount of curvature in the compensation is controlled by the unbalance ratio λ in the emitter areas of Q_{10A} and Q_{10B}. In simulations of the uncompensated VCO, the ratio of slopes at the ends of the input range was 2:1, even larger than predicted by the simple theory of (5-10). The required unbalance to compensate follows from Gilbert's results (since the ±200mV limits correspond to a normalized input of 1/6 and 5/6), in which the ratio of endpoint slopes as a function of unbalance λ is

$$\rho = \left(\frac{1 + \frac{5}{6}(\lambda - 1)}{1 + \frac{1}{6}(\lambda - 1)} \right)^2 = 2 \qquad (5\text{-}12)$$

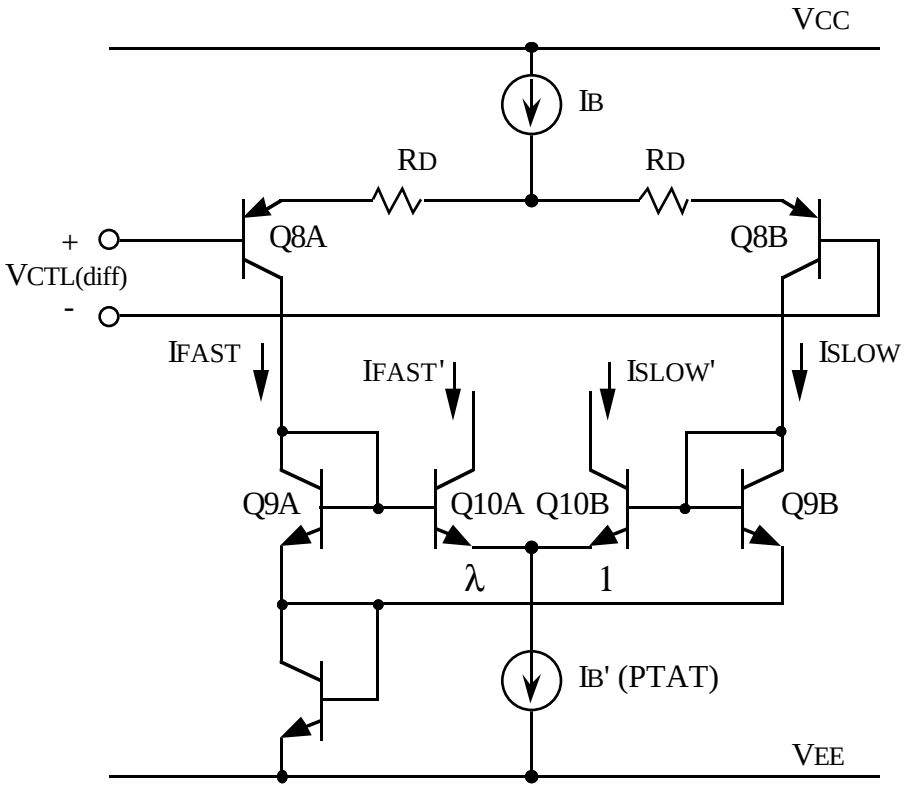
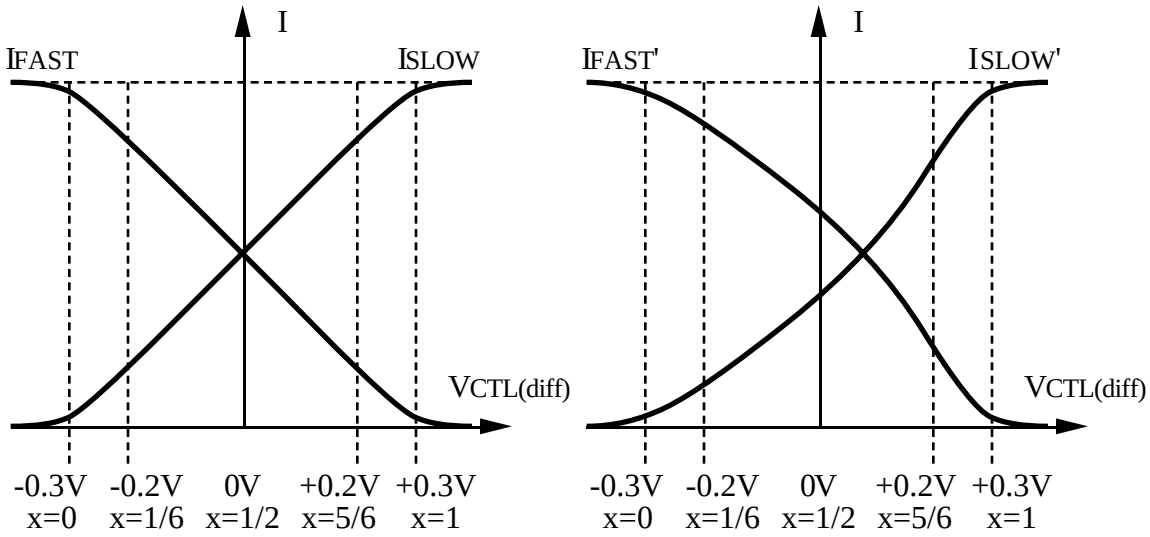


Figure 5.7. Translinear circuit for nonlinearity compensation.



Uncompensated characteristic of degenerated emitter-coupled pair.

Compensated characteristic with translinear cell.

Figure 5.8. Desired characteristic for linearity compensation

Solving (5-12) gives for the unbalance ratio a value of $\lambda = 1.70$. In practice the compensation does not need to be so exact, and in the design a value of $\lambda = 2$ was realized by connecting two identical devices in parallel for Q_{10A}.

A subtle point that should be noted is that I_B cannot be made PTAT, since we see from (5-6) and (5-8) that this would cause K_o to be temperature dependent. This shows an added benefit of using the translinear approach: the ratio of the currents I_{FAST}', I_{SLOW}' is controlled only by $V_{CTL(diff)}$ in a temperature-independent fashion, while the sum of the currents I_B' is PTAT for reducing the temperature drift of switching delay through the interpolator blocks.

5.3 Experimental Results

Figure 5.9 shows the simulated V-to-f characteristic of the VCO with and without linearity compensation. Figure 5.10 shows the measured V-to-f characteristic with $\lambda = 2$ unbalance compensation. For the compensated VCO, K_o is constant to within 5% of the center frequency value over the entire tuning range.

Figure 5.11 shows the simulated temperature drift of frequency, with and without PTAT biasing, over a –60°C to +140°C range. Figure 5.12 shows the measured temperature drift of center frequency. With PTAT bias, the average (end-to-end) temperature drift of center frequency is approximately 520 ppm/°C.

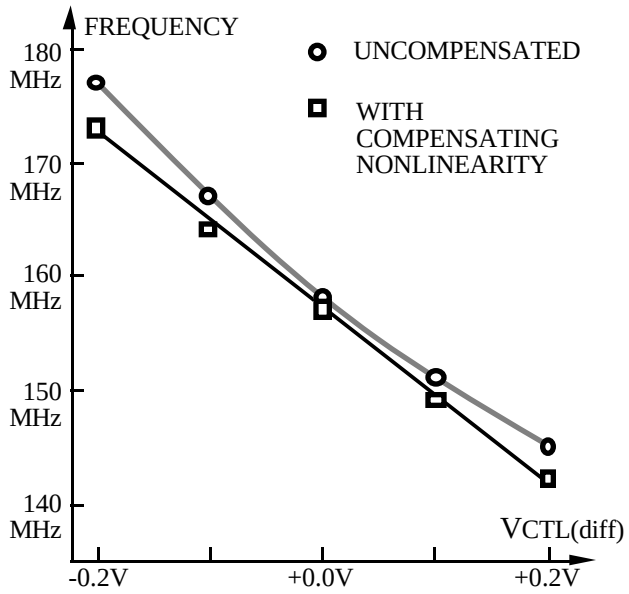


Figure 5.9.
Simulated V-to-f characteristic, with/without linearity compensation

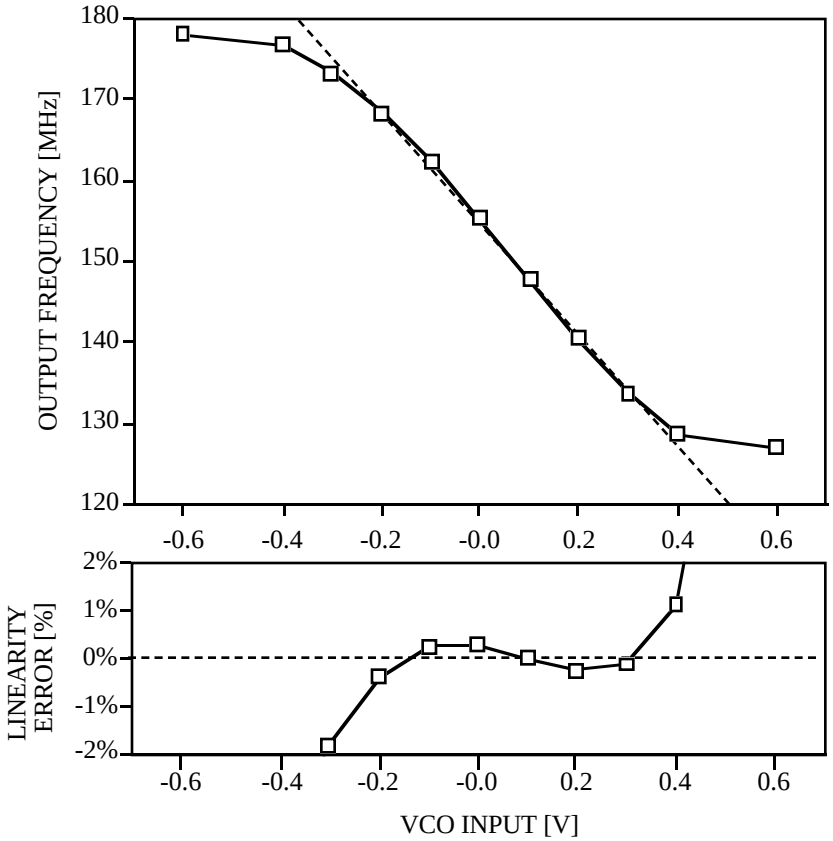


Figure 5.10. Measured VCO linearity.

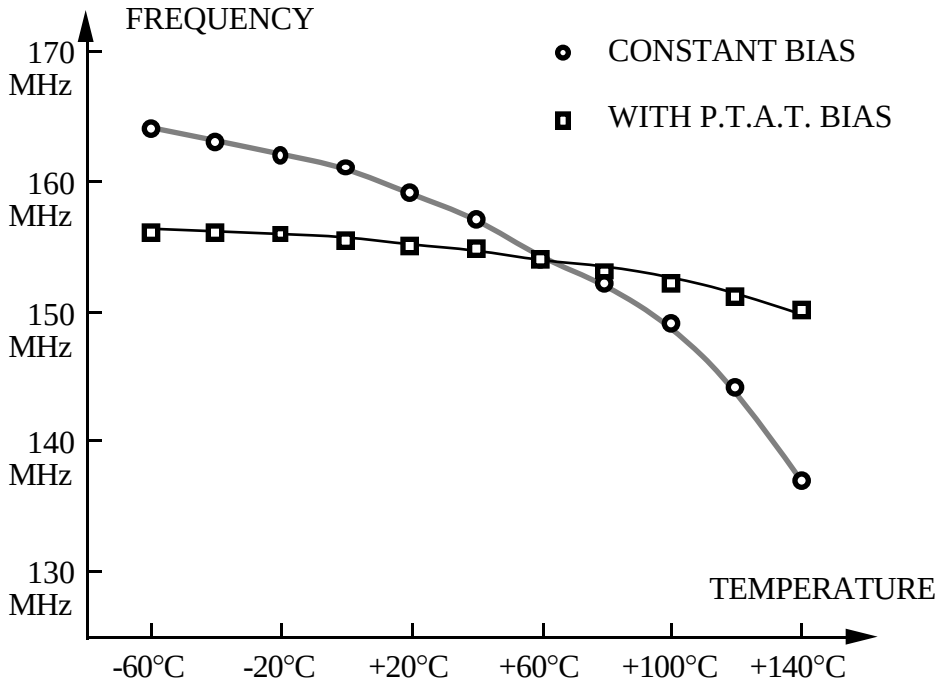


Figure 5.11. Simulated center frequency drift over temperature, with/without PTAT bias.

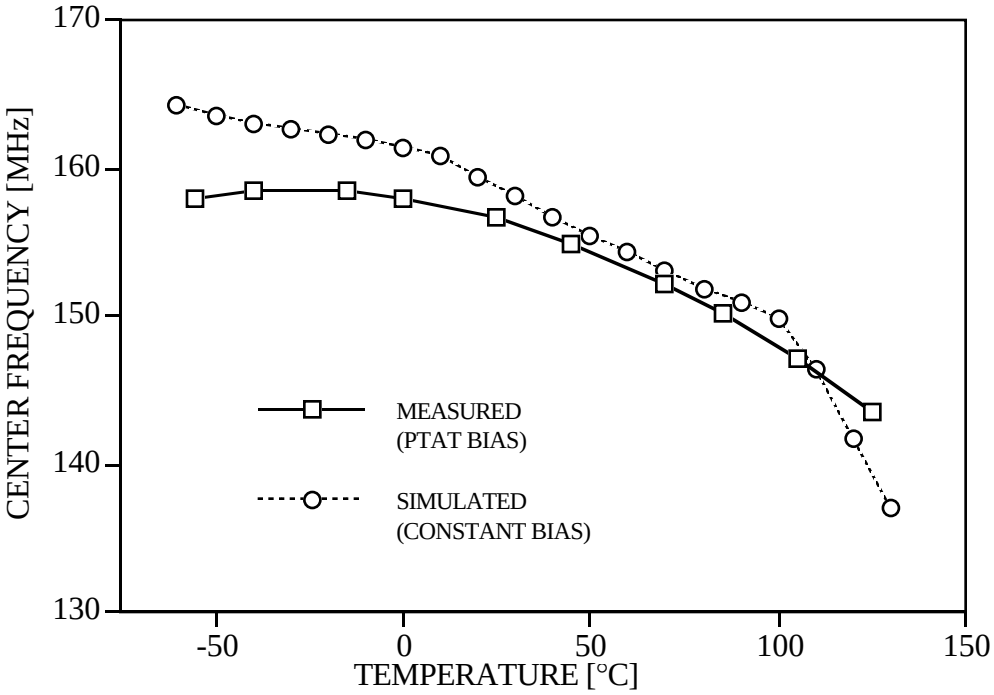


Figure 5.12. Measured temperature drift of frequency.

Figure 5.13 shows simulation of power-supply induced jitter both with and without the R_B/C_B decoupling network. The amplitude of the ripple sinusoid was 200 mV p-p. With the network, jitter is reduced on average by a factor of 10.

For the fabricated parts, the effectiveness of the decoupling network was measured by injecting noise on the power supply and looking for bit errors. No errors were seen for injected noise amplitudes up to 120mV p-p.

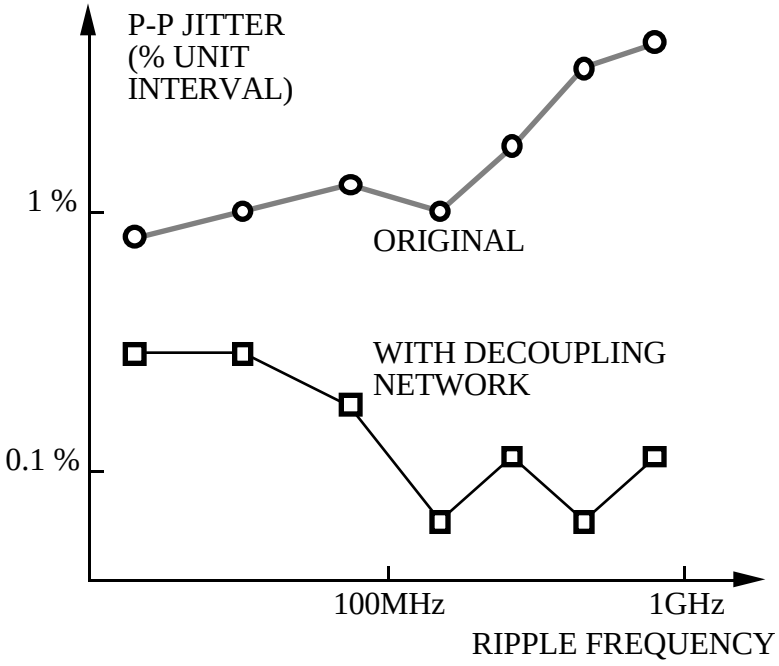


Figure 5.13.
Simulated supply-induced jitter, with/without decoupling network

The power/jitter tradeoff favored low power with moderate jitter, with a nominal tail current of I_{EE} = 100 μA. The nominal collector resistance is R_C = 3 kΩ, but this value can vary from 2 kΩ to 6 kΩ since R_C is used to trim the center frequency.

Figure 5.14 shows the open loop, self referenced jitter plot. The extracted value of the time domain figure of merit κ was 6.05E-08 $\sqrt{s}$. The predicted value from the sources in Section 4.1 is given as follows:

R_C = 1.9 kΩ e_n = 95 nV/$\sqrt{Hz}$

R_E = 9.5 kΩ f_o = 155.4 MHz

r_{bT} = 4.8 kΩ K_o = 4.41E+08 rad/V· sec

I_{EE} = 122 μA kT = 4.16E-21 J at T = 300 K

$$\kappa_{RC} \approx (1.699)\sqrt{\frac{k\ T}{I_{EE}^2\ R_C}} \tag{5-13}$$

$$\kappa_{RC} \approx (1.699)\sqrt{\frac{(4.16\text{E-}21\ \text{J})}{(122\ \mu\text{A})^2\ (1.9\ \text{k}\Omega)}} = 2.06\ \text{E-}08\ \sqrt{s} \tag{5-14}$$

$$\kappa_{RE} \approx (1.201)\sqrt{\frac{k\ T}{I_{EE}^2\ R_E}} \tag{5-15}$$

$$\kappa_{RE} \approx (1.201)\sqrt{\frac{(4.16\text{E-}21\ \text{J})}{(122\ \mu\text{A})^2\ (9.5\ \text{k}\Omega)}} = 0.65\ \text{E-}08\ \sqrt{s} \tag{5-16}$$

$$\kappa_{rbT} \approx (0.693)\ \sqrt{\frac{q}{I_{EE}}\frac{r_{bT}}{R_C}} \tag{5-17}$$

$$\kappa_{rbT} \approx (0.693)\sqrt{\frac{(1.6\text{E-}19\ \text{coul})}{(122\ \mu\text{A})}\left(\frac{4.8\ \text{k}\Omega}{1.9\ \text{k}\Omega}\right)} = 3.99\ \text{E-}08\ \sqrt{s} \tag{5-18}$$

$$\kappa_{VCO} \approx (0.707)\frac{K_o}{\omega_o}\ e_n \tag{5-19}$$

$$\kappa_{VCO} \approx (0.707)\frac{4.41\text{E+}08\ \text{rad/V}\cdot\text{s}}{2\pi\ 155.4\ \text{MHz}}(95\ \text{nV}/\sqrt{\text{Hz}}) = 3.03\ \text{E-}08\ \sqrt{s} \tag{5-20}$$

Taking the root sum of these components gives

$$\kappa \approx 5.46\ \text{E-}08\ \sqrt{s} \tag{5-21}$$

which is within 10% of the measured κ of 6.05 E-08 $\sqrt{s}$.

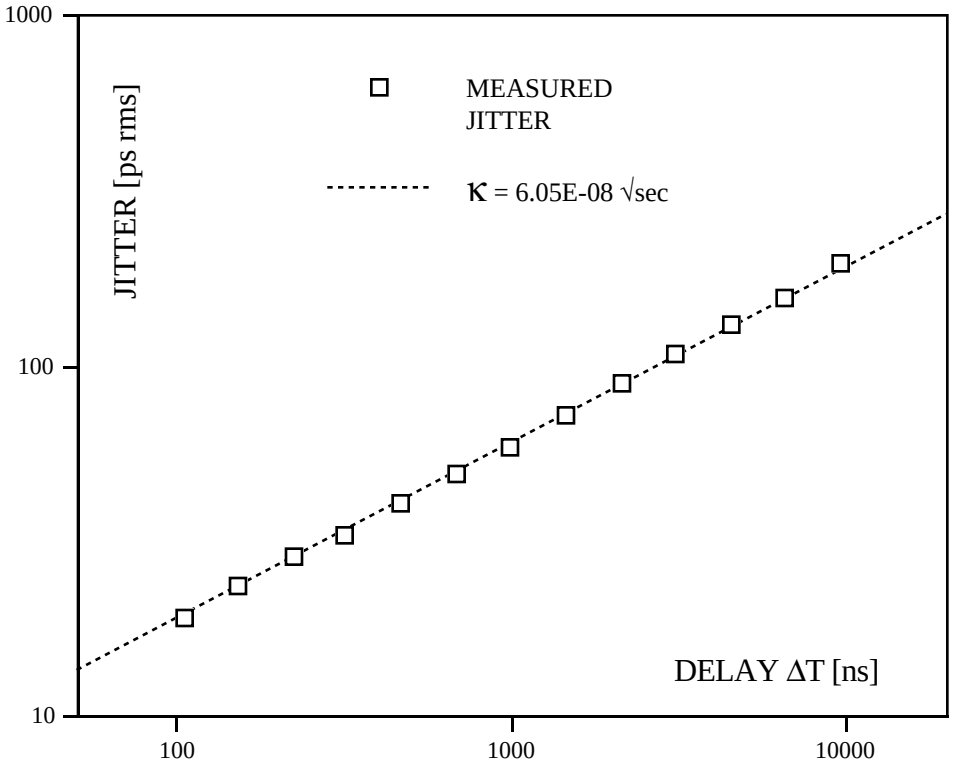


Figure 5.14. VCO open loop, self referenced jitter.

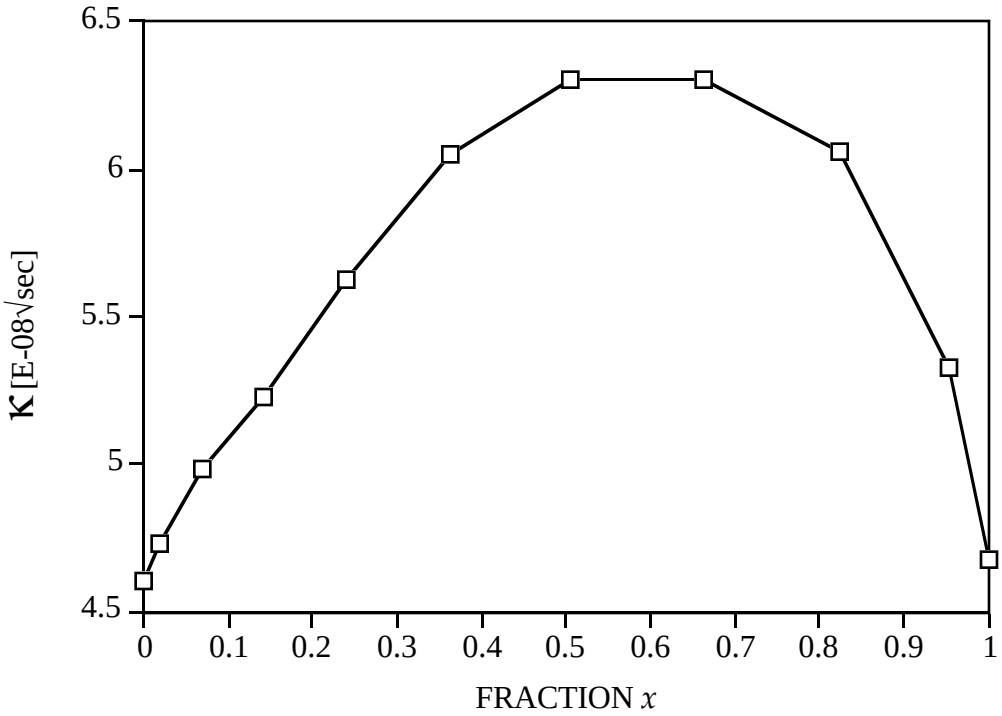


Figure 5.15. κ dependence on VCO interpolation fraction x .

Closed loop jitter

The measured closed loop $\sigma_{x(meas)}$ for pseudorandom data was 37.8 ps rms. The measured loop bandwidth (for pseudorandom data) was 228 kHz. The predicted value of σ_x from equation (2.1.3-3) and (2.1.5-7) was

$$\sigma_x = \frac{\kappa}{2\sqrt{\pi\ f_L}} \tag{5-22}$$

$$\sigma_{x(pred)} = \frac{6.05\text{E-}08\ \sqrt{s}}{2\sqrt{\pi\ (228\ \text{kHz})}} = 35.7\ \text{ps rms} \tag{5-23}$$

within 6% of the measured value.

Jitter dependence on tuning

An interesting dependence of κ on VCO tuning was observed. A plot of jitter κ vs. the interpolator tuning fraction x , shown in Figure 5.15, shows that jitter is worst near the center of the tuning range. The main reason for this effect was that the implementation of the circuit of Figure 5.7 was not optimized for noise, and contributed the excessively high e_n = 95 nV/$\sqrt{\text{Hz}}$ noise density. The variation with tuning is due to the changing gain that this noise source sees in the translinear cell of the nonlinearity compensation circuit. At either end of the range, the gain of the translinear cell is small, the effective K_o is reduced, and the κ_{VCO} contribution to jitter drops out. The resulting jitter should then be due only to κ_{RC}, κ_{RE}, and κ_{rbT}.

Taking the root sum of these components gives

$$\kappa \approx 4.54\ \text{E-}08\ \sqrt{s} \tag{5-24}$$

which is within 2% of the $\approx 4.6\text{E-}08\ \sqrt{s}$ measured at the endpoints of the tuning range when x = 0 and x = 1. Note that Figure 5.15 also supports the assertion that gate delay jitter errors are independent of ring length. From Figures 5.2 and 5.3 we see that when x = 0, the ring is effectively 4 stages long; when x = 1, the ring is 6 stages long. In both cases, however, κ is approximately 4.6E-08 $\sqrt{s}$.

The difficulty with jitter dependence on tuning range was noted, but due to time constraints in the design process, no steps were taken to correct this problem. Possible improvements are discussed in the future work section of Chapter 7.

5.4 Chapter summary

In summary, the ring oscillator architecture of Figure 5.3, with the design improvements of Section 5.2.3, meets all the VCO design requirements. The ring structure inherently provides a 50% duty cycle and quadrature outputs. Control of frequency by purely differential means provides a measure of inherent insensitivity to supply-induced jitter. A disadvantage is inherent nonlinearity, but this is compensated in a predictable manner. A bypassing network has been used to further reduce the effect of power supply variations on jitter. Temperature dependence of frequency has been reduced by providing the ring gates with a temperature compensating bias current. Test results show a linear control characteristic about the desired 155 MHz center frequency, good temperature stability, and reduced sensitivity to power-supply induced jitter.

6. Design procedure

This chapter summarizes the design procedure developed in Chapters 2 through 4, and exemplified in detail in Chapter 5.

6.1 Step 1: refer design goal to asymptotic $\mathcal{K}$

The starting point for the procedure can be given in either the time or frequency domain, depending on which end user figure of merit is the design goal. In either case, the first step is to relate the design goal to the time domain figure of merit $\mathcal{K}$.

6.1.1 Time domain: σ_x

In the time domain the desired performance is expressed as σ_x, the closed-loop transmit clock referenced jitter. From the time/frequency procedure of Chapter 2, this is related to the asymptotic $\mathcal{K}$ by

$$\mathcal{K} = 2\,\sigma_x \sqrt{\pi\ f_L} \qquad (6\text{-}1)$$

where f_L is the loop bandwidth.

For example, if a σ_x of 25 ps is desired at a loop bandwidth of 100 kHz, then the required asymptotic $\mathcal{K}$ is given by substituting into (6-1):

$$\mathcal{K} = 2\ (25\ \text{ps}) \sqrt{\pi\ (100\ \text{kHz})} \qquad (6\text{-}2)$$

$$\mathcal{K} = 2.81\ \text{E-}08 \sqrt{\text{s}} \qquad (6\text{-}3)$$

6.2.2 Frequency domain N_1

The ring oscillator may also be characterized in terms of its open loop spectrum. This is usually specified as a power spectral density $N_{f\Delta}$ at a given offset frequency f_Δ from the "carrier" (center frequency) f_o.

Again, this can be related to the asymptotic $\mathcal{K}$ using the time/frequency technique of Chapter 2. If we assume that the open loop spectrum follows the $1/f^2$ power law, then

$$N_{f\Delta} = \frac{N_1}{f_\Delta^2} \qquad (6\text{-}4)$$

Solving for N_1 gives

$$N_1 = N_{f\Delta}\, f_\Delta^2 \tag{6-5}$$

Once we have expressed the desired performance in terms of N1, (2-17) is used to determine the asymptotic κ:

$$\kappa = \frac{\sqrt{N_1}}{f_o} \tag{6-6}$$

For example, suppose the desired oscillator performance is specified as having a p.s.d. of -107 dBc at a 1MHz offset from a 155MHz center frequency.

First we convert to an equivalent N_1 (note that dBc is converted to a ratio using 10X the logarithm, since it is a power expression):

$$N_1 = 10^{(-107/10)}\,(1\text{MHz})^2 \tag{6-7}$$

$$N_1 = 20\ \text{Hz} \tag{6-8}$$

Substituting into (6-6) gives

$$\kappa = \frac{\sqrt{20\ \text{Hz}}}{155\ \text{MHz}} \tag{6-9}$$

$$\kappa = 2.88\text{E-}08\ \sqrt{s} \tag{6-10}$$

6.2 Step 2: adjust asymptotic κ to gate-level κ

Equations (4-66) through (4-70) give the κ values for various jitter sources in a single delay. As we have seen, the asymptotic κ is equal to the single delay κ only when the delay errors are independent and there are no other noise coupling mechanisms operating.

The asymptotic κ may be higher for various reasons. Appendix G shows how the correlation of delay errors raises the asymptotic κ. When the loop is closed, additional jitter may result from on-chip noise coupling. To achieve a desired asymptotic κ, the gate should therefore be designed conservatively for a lower κ.

For example, suppose we are trying to achieve the asymptotic $\kappa = 2.81\text{E-}08\ \sqrt{s}$ of (6-3) in an interpolating ring. If we design conservatively with a safety factor of 1.5, the single gate delay κ should be

$$\kappa = \frac{2.81\text{E-}08\ \sqrt{s}}{1.5} = 1.87\text{E-}08\ \sqrt{s} \tag{6-11}$$

6.3 Step 3: determine constraints on the design of the individual gate

Now that we have determined the single gate κ, we can use (4-66) through (4-70) to give constraints on circuit values. The components will root sum to give the total κ. As a starting point in the constraints, we could assign equal contributions to each of the sources. Then the root sum total will be equal to (6-11) when each of the four components is

$$\kappa = \frac{1.87\text{E-}088\sqrt{s}}{\sqrt{4}} = 0.94\text{E-}08\sqrt{s} \qquad (6\text{-}12)$$

This can be applied to each of (4-66) through (4-70) to give design constraints. For example, suppose we are designing a ring with the basic delay element shown in Figure 4.1. The current source is sufficiently degenerated so that shot noise is not the jitter source. The design goal for center frequency is f_o = 155MHz, with a control constant of K_o = 440 rad/V· s. Using kT = 4.16E-21 J at T = 300 K, (4-66) through (4-70) give:

Collector load resistor thermal noise

$$\kappa_{R_C} \approx (1.699)\sqrt{\frac{k\ T}{I_{EE}^2\ R_C}} \tag{6-13}$$

$$0.94\text{E-}08\ \sqrt{s}\ > (1.699)\sqrt{\frac{4.16\text{E-}21\text{J}}{I_{EE}^2\ R_C}} \tag{6-14}$$

$$I_{EE}^2\ R_C > 135\mu W \tag{6-15}$$

Tail current noise (thermal noise dominated)**:**

$$\kappa_{R_E} \approx (1.201)\sqrt{\frac{k\ T}{I_{EE}^2\ R_E}} \tag{6-16}$$

$$0.94\text{E-}08\ \sqrt{s}\ > (1.201)\sqrt{\frac{4.16\text{E-}21\text{J}}{I_{EE}^2\ R_E}} \tag{6-17}$$

$$I_{EE}^2\ R_C > 68\mu W \tag{6-18}$$

Switching equivalent base resistance thermal noise

$$\kappa_{r_{bT}} \approx (0.693)\ \sqrt{\frac{q}{I_{EE}}\frac{r_{b\,T}}{R_C}} \tag{6-19}$$

$$0.94\text{E-}08\ \sqrt{s}\ > (0.693)\ \sqrt{\frac{q}{I_{EE}}\frac{r_{b\,T}}{R_C}} \tag{6-20}$$

$$r_{bT} < (1150\ \frac{\Omega}{V})\ I_{EE}\ R_C \tag{6-21}$$

White noise at VCO input

$$\kappa_{VCO} \approx (0.707)\frac{K_o}{\omega_o}\ e_n \tag{6-22}$$

$$0.94\text{E-}08\ \sqrt{s}\ > (0.707)\frac{440\ \text{rad/V}\cdot\text{s}}{2\pi\ 155\text{MHz}}\ e_n \tag{6-23}$$

$$e_n < 29\ \text{nV}/\sqrt{\text{Hz}} \tag{6-24}$$

These constraints were developed assuming all sources contributed equally. Depending on the particular process in which the circuit will be implemented, some constraints may be easy to achieve and others very difficult or impossible. Since each source's contribution to jitter is clearly identified in terms of fundamental parameters such as power dissipation or waveform amplitude, it is straightforward for the designer to reallocate jitter among the various sources to make the constraints more realistic. Just as valuable, if there is no set of realizable constraints, the designer knows that the particular jitter goal cannot be achieved with a ring oscillator design in that process.

6.4 Step 4: design for ring center frequency

There are two ways the designer can control the center frequency of the ring: The number of gates in the ring, and the speed of each gate. The beauty of using κ to design for jitter is that, to first order, *κ is unchanged regardless of the number of stages in the ring or the delay of the stage as affected by the collector load capacitance C_C.*

Thus to realize a certain frequency with the delay stage of Figure 4.1, the designer is free to choose an appropriate combination of collector capacitance and number of delay elements. Each approach has its advantages and disadvantages.

Using little or no collector capacitance gives minimum delay per stage, and thus a ring with many stages. This has the disadvantages of more power consumption and less control over center frequency since the delay is largely determined by stray capacitance. This has the advantage of reducing the delay-to-delay coupling, described in Appendix G, that can increase jitter.

Using a significant amount of collector capacitance increases the delay, giving a ring with fewer stages. This has the advantage of lower power consumption and better control over center frequency. The disadvantage is the possibility of slightly increased jitter due to delay-to-delay coupling.

Obviously the particular design goals will determine the best tradeoff between these extremes.

6.5 General design techniques for low jitter

There are other general ideas that are good to keep in mind when designing for low jitter in a voltage controlled oscillator

The circuit should be designed to minimize common mode influences on frequency, particularly from the power supply. To this end, it is a good idea to keep things as differential as possible. A side benefit of differential signals is that the ring need not have an odd number of stages since wire inversion can be used to achieve the required 180° phase shift around the ring.

The oscillator frequency should be immune to the power supply over a wide range of supply variation frequencies. At very high frequencies bond wire inductance can isolate the on-chip supply rail from the low impedance provided by off-chip bypass capacitors [21]. Significant voltage ripple can occur on chip, and if the frequency is sensitive to the supply, then jitter will increase.

6.6 Chapter Summary

This chapter has summarized a design procedure for low jitter ring oscillators. Examples are given starting from desired performance specifications in both the time and frequency domains. The result of the procedure is a set of constraints on circuit elements required to achieve the desired jitter. An advantage of the method presented here is that, to first order, the ring center frequency can be adjusted independently of the jitter. Other design issues that can affect low jitter performance, such as power supply and common mode signal sensitivity, have also been discussed.

7. Summary

The main contribution of this thesis has been to develop a methodology to guide design for low-jitter, voltage controlled ring oscillators.

Chapter 1 introduced several applications for this work, the primary one being the use of PLLs for clock recovery in serial data communication. A review of fundamental PLL and phase noise concepts showed that a low jitter PLL requires a low jitter VCO. A review of the different types of VCOs used in clock recovery PLLs showed the need for design tools for low-jitter ring VCOs. After a general introduction to jitter measurement techniques in Section 1.4, Section 1.5 specified five jitter measures that were unified in this thesis.

Chapter 2 develops a time/frequency technique for relating the different measures of jitter introduced in Chapter 1. The technique is confirmed by experimental results on existing VCOs. The key contribution of this chapter is connecting the open-loop figures-of-merit, N_1 (frequency domain) and $\mathcal{K}$ (time domain), to the closed loop time domain measure σ_x. Knowledge of either N_1 or $\mathcal{K}$ gives complete information on the oscillator's jitter performance as measured in five different ways.

This technique improves the design process by allowing VCO design to take place in the domain that provides the most insight into sources of jitter. Another benefit is substantial savings in simulation time since only the open loop VCO needs to be simulated. The technique also allows a stand-alone test of VCO contribution to closed loop jitter. The technique applies to any oscillator with a p.s.d. that fits a $1/f^2$ model.

After a review of analytical techniques for harmonic and relaxation oscillators, Chapter 3 described a theoretical framework for analyzing and predicting jitter in ring oscillators. The framework follows naturally from the time/frequency technique developed in Chapter 2. The result is a prediction of the time domain figure-of-merit $\mathcal{K}$, which can be used to determine the end user's figure-of-merit σ_x. A key insight of this approach is that jitter performance of a ring, as characterized by $\mathcal{K}$, depends primarily on the individual gate and not on the number of gates in the ring. Experimental results for rings of several different lengths confirm the validity of the general approach.

Chapter 4 developed simple numerical expressions for predicting jitter in a ring oscillator composed of differential pair delay gates. The time domain figure of merit $\mathcal{K}$ provides the link to system-level jitter performance measures. The expressions were

verified with both simulation and experimental results from several rings of different lengths. Comparing the expressions for κ in rings with results from the harmonic and multivibrator cases illuminated the relative merits of the three types of oscillators in terms of jitter performance.

As an example of the procedure, the design of a low jitter ring VCO for a 155 MHz clock recovery PLL is described in Chapter 5. Design techniques for overcoming some of the inherent limitations of the ring architecture were discussed. Test results showed good agreement to the design methodology's numerical predictions.

Chapter 6 summarized the low jitter ring oscillator design methodology. Starting with desired jitter performance, expressed in either the time or frequency domain, the procedure gives explicit constraints on values of circuit elements. An advantage of this method presented here is that the jitter can be minimized essentially independently of the ring center frequency.

Future work

There are several possibilities for future work in this general area.

One would be to extend the simple numerical results of Section 4.1 to ring design in MOSFET technology. The mathematical analysis might be more difficult for the MOS differential pair. Assuming the signal to be much larger than the linear region of the bipolar differential pair greatly simplified the analysis in Section 4.1. This assumption may not be valid for the MOS differential pair, due to its larger linear input range: the simulation results in Section 4.2.1 showed the least accuracy when the input signal was comparable to the differential pair linear range. It is possible that the lower transconductance of MOSFETs might be advantageous for low jitter by imposing less amplification of noise.

This thesis has examined only sources of jitter in the $R_C C_C$ time constant of the collector load. Another way to extend the theory would be to consider other sources of jitter when the simplifying assumptions of Section 4.1 no longer apply. In principle, the general approach of Chapter 3 should still be valid, although the resulting expressions would probably not be as straightforward as those in Chapter 4.

This thesis has only examined techniques for reducing jitter within the design of a single gate. It is also possible that other techniques, such as coupling rings [54, 63] might provide lower jitter. For example, which provides lower jitter: one delay stage with a tail current of I_{EE}, or two coupled stages in parallel each with a tail current of $I_{EE}/2$? The dependence of κ on total power dissipation indicates that there might be no difference.

This thesis has not developed the full potential of these methods in terms of simulation. Like the analysis of the harmonic oscillator, most simulation of oscillator phase noise has been in the frequency domain [37, 78]. Further development of time domain (transient analysis) simulation techniques [10] beyond the individual gate level could provide additional insight to lowering jitter during design iteration.

The author hopes that the techniques and tools developed in this thesis will be enlightening for both researchers and practicing designers in the course of answering these and other interesting questions.

A. Approximate loop transfer functions

As given in (1-5) and (1-6), the expressions for phase noise $H_n(s)$ and signal $H_s(s)$ transfer functions are, respectively,

$$H_n(s) = \frac{\theta_o}{\theta_n} = \frac{s}{s + K_d K_o F(s)} \qquad \text{(A-1)}$$

$$H_s(s) = \frac{\theta_o}{\theta_i} = \frac{K_d K_o F(s)}{s + K_d K_o F(s)} = 1 - H_n(s) \qquad \text{(A-2)}$$

The AD800 series of PLLs uses a second order loop with proportional-plus-integral (lag-lead) control [26, 60]. This control is realized with the active filter shown in functional form in Figure A.1. The loop filter transfer function F(s) is

$$F(s) = \frac{s\tau_z + 1}{s + 1/\tau_{DC}} \qquad \text{(A-3)}$$

where τ_z is the zero time constant, and $1/\tau_{DC}$ represents the finite gain of the integrator.

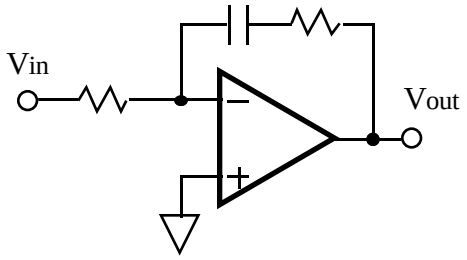


Fig. A.1. Loop filter equivalent circuit.

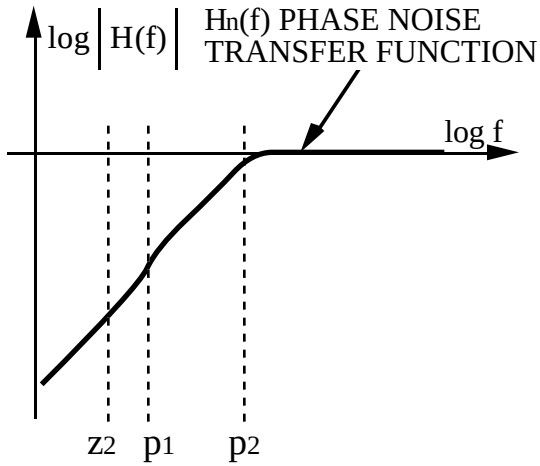


Fig. A.2. Phase noise transfer function Bode plot, with inflection points from poles and zeroes.

Substituting (A-3) into (A-1) gives

$$H_n(s) = \frac{s\left(s + \frac{1}{\tau_{DC}}\right)}{s^2 + s\left(\frac{1}{\tau_{DC}} + K_d\ K_o\ \tau_z\right) + K_d\ K_o} \qquad \text{(A-4)}$$

This transfer function has zeroes at

$$s_{z1} = 0 \quad s_{z2} = \frac{-\ 1}{\tau_{DC}} \qquad \text{(A-5)}$$

We now make two assumptions to simplify approximation of the pole frequencies:

1) $1/\tau_{DC} << K_d\ K_o\ \tau_z$

   We assume that the pole from the active filter integrator is at a very low frequency compared to $K_d\ K_o\ \tau_z$. For the AD800 series $1/\tau_{DC} \approx 1$ rad/s and $K_d\ K_o\ \tau_z \approx$ 1E+06 rad/s, so this assumption is easily met.

2) The loop is overdamped : $\zeta > 1$

   This assumption is valid since clock recovery PLLs are operated overdamped to prevent excessive peaking in the $H_s(s)$ transfer function [60]. The AD800 series is specified with $\zeta = 5$, and is typically operated with $\zeta = 10$.

With these assumptions, solving (A-4) gives for the approximate pole locations

$$s_{p1} \approx \frac{-\ 1}{\tau_z} \qquad s_{p2} \approx -\ K_d\ K_o\ \tau_z \qquad \text{(A-6)}$$

The magnitude Bode plot of (A-4) in Figure A.2 shows the approximate pole-zero cancellation of s_{p1} and s_{z2}. The transfer function can be approximated by a single pole highpass response:

$$H_n(s) \approx \frac{s}{s + K_d\ K_o\ \tau_z} \qquad \text{(A-7)}$$

This is in the form of (1-8)

$$H_n(s) = \frac{s}{s + 2\pi\ f_L} \qquad \text{(A-8)}$$

where the loop bandwidth is

$$f_L = \frac{K_d\ K_o\ \tau_z}{2\pi} \qquad \text{(A-9)}$$

Substituting (A-8) into (A-2) gives the phase signal transfer function (1-7):

$$H_s(s) = \frac{2\pi f_L}{s + 2\pi f_L} \qquad \text{(A-10)}$$

B. Power spectra relationships

This appendix considers the relationship between result of the direct spectrum measurement and the phase noise p.s.d. $S_\phi(f)$. First we will consider the case of phase modulation of a sinusoidal waveform. Then we will consider the more general case of ECL-type trapezoidal waveforms.

Sinusoidal case

In [66], Robins considers phase modulation of a carrier to develop the spectrum of phase noise in a mathematically rigorous way. Since phase modulation is nonlinear, the final result is expressed in terms of Bessel functions. Robins then uses a small angle approximation (assuming that the noise amplitude << carrier) and the resulting spectrum approaches the more familiar result of amplitude modulation. In this section, we will take a more intuitive approach by effectively making the small angle approximation first and staying with the more intuitive behavior of amplitude modulation spectra. The results are the same as Robins'.

Consider a "carrier" waveform of amplitude V_C and frequency f_c, which is perturbed by phase noise $\phi(t)$:

$$V(t) = V_C \cos [\, 2\pi f_c t + \phi(t) \,] \qquad \text{(B-1)}$$

An example of V(t) and $\phi(t)$ is shown in Figure B.1. Also shown in the figure is the p.s.d. $S_\phi(f)$ of the phase noise process, and the p.s.d. $S_V(f)$ (normalized to unit impedance) of the phase modulated carrier. Note that V(t) has dimensions [V] and $\phi(t)$ is in [rad]. Therefore $S_V(f)$ is in [W/Hz] (with an impulse in units of [W] at f_c) and $S_\phi(f)$ is in rad^2/Hz. By considering the mathematics of phase modulation from this point, Robins derives the relationship between $S_\phi(f)$ and $S_V(f)$.

We can tell from observation that V(t) is perturbed by phase noise because its zero crossing times are displaced from the ideal, uniformly spaced times. This is shown in the figure as time errors $\varepsilon_T(t)$, which are related to the phase noise process by

$$\varepsilon_T(t) = \frac{\phi(t)}{2\pi f_c} \qquad \text{(B-2)}$$

It is these variations in the crossing times which we measure as jitter. In effect, when measuring the jitter at the zero crossing times of the carrier, we are sampling the jitter

process. If we assume that the bandwidth of the jitter process is much less than the carrier frequency (in practice, true when the small angle approximation is true), then there is no aliasing and our measurements represent an accurate sample of the jitter process.

We also see that there is only phase noise (no amplitude noise) since the peaks of the V(t) waveform have uniform amplitude.

It is possible to synthesize a waveform very similar to V(t) through a process of amplitude, rather than phase, modulation. In principle, as shown in Figure B.1, we could equivalently characterize the jitter in terms of an amplitude error ε_V. Assuming that the phase error is small, we can approximate the waveform as being linear near zero. Then ε_V and ε_T near the zero crossings are related by the slope of the carrier waveform

$$\frac{\varepsilon_V}{\varepsilon_T} = V_C \, 2\pi \, f_c \qquad \text{(B-3)}$$

and substituting for ε_T from (B-2) gives

$$\varepsilon_V(t) = V_C \, \phi(t) \qquad \text{(B-4)}$$

This behavior can be realized by using the phase noise process $\phi(t)$ to amplitude modulating a carrier in quadrature with the original carrier, producing an error voltage $V_\varepsilon(t)$:

$$V_\varepsilon(t) = \phi(t) \, V_C \sin [\, 2\pi \, f_c t \,] \qquad \text{(B-5)}$$

and then adding this waveform with the original, ideal carrier:

$$V'(t) = V_C \cos [\, 2\pi \, f_c t \,] + \phi(t) \, V_C \sin [\, 2\pi \, f_c t \,] \qquad \text{(B-6)}$$

Figure B.2 shows the process of "building up" V'(t) from the $V_\varepsilon(t)$ and original carrier waveforms.

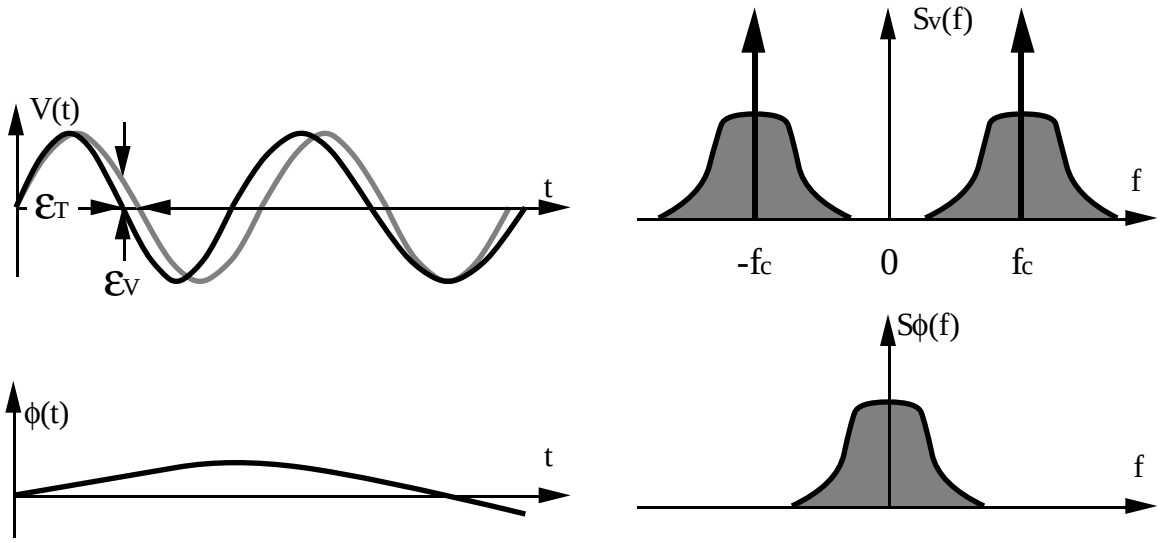


Fig. B.1. Voltage and phase waveforms with p.s.d.s.

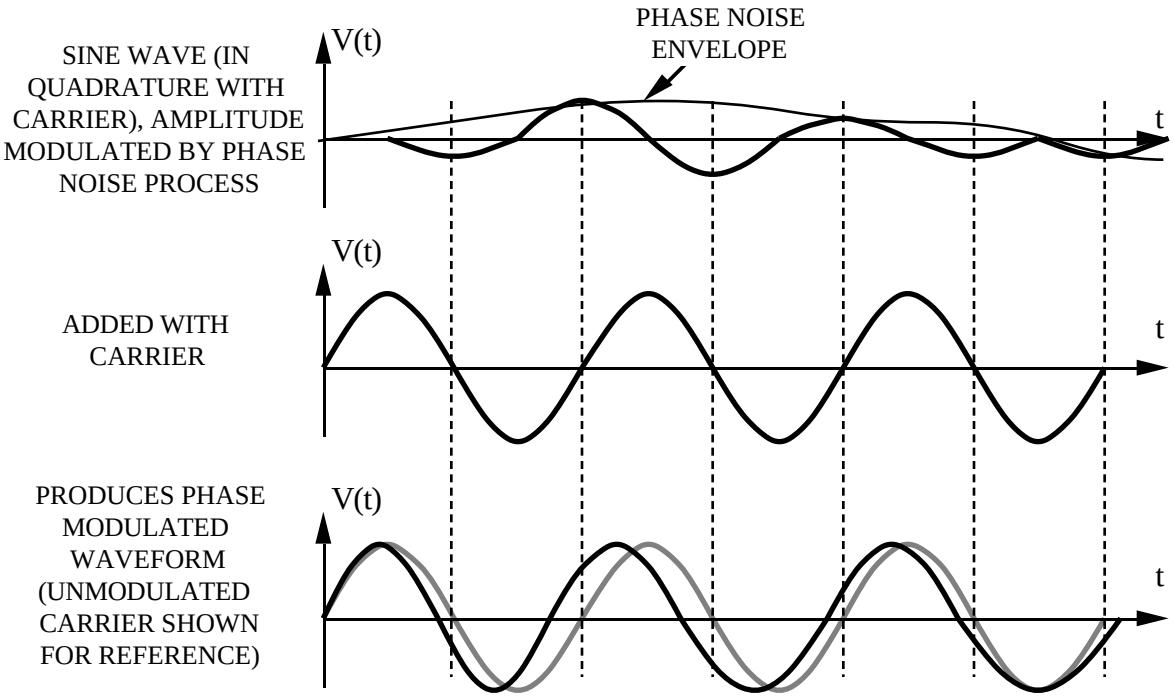


Fig. B.2. Representation of phase noise as additive amplitude noise.

From the standpoint of measuring jitter, this V'(t) waveform will have the same properties as the original V(t): the same time errors at the zero crossings (as related by (B-2) and (B-4)) and constant amplitude at the peaks (since the sine and cosine components are in quadrature). The advantage of this approach is that the spectrum of V'(t) can be determined intuitively by inspection of (B-6). Since the two terms in (B-6) are uncorrelated, their power spectra will simply add. When the single-sided spectrum is measured on a spectrum analyzer, the carrier power will be $V_C^2/2$, and the "skirt" near the carrier will be $S_\phi(f) \cdot V_C^2/2$. Thus normalizing the entire spectrum to the carrier power will yield the p.s.d. of the jitter process, $S_\phi(f)$, in rad^2/Hz.

Trapezoidal waveforms

A subtlety of the direct spectrum approach is that it only measures power contributions from frequencies near the fundamental. The waveform fed into the spectrum analyzer is often a square wave with energy at harmonics, which would seem also to contribute to changing the zero crossing time.

This is not the case, however. In this section we will show that a given time error at the zero crossing produces approximately the same power contribution near the fundamental, regardless of the waveform slope. We will consider only a plausibility argument, rather than a rigorous proof.

Consider the transitions shown in Figure B.3. In each case, the ideal transition is shown as a dashed line; the actual (due to jitter) transition is shown as a solid line. The transitions have different slopes, but the same time error ε_T at the zero crossing.

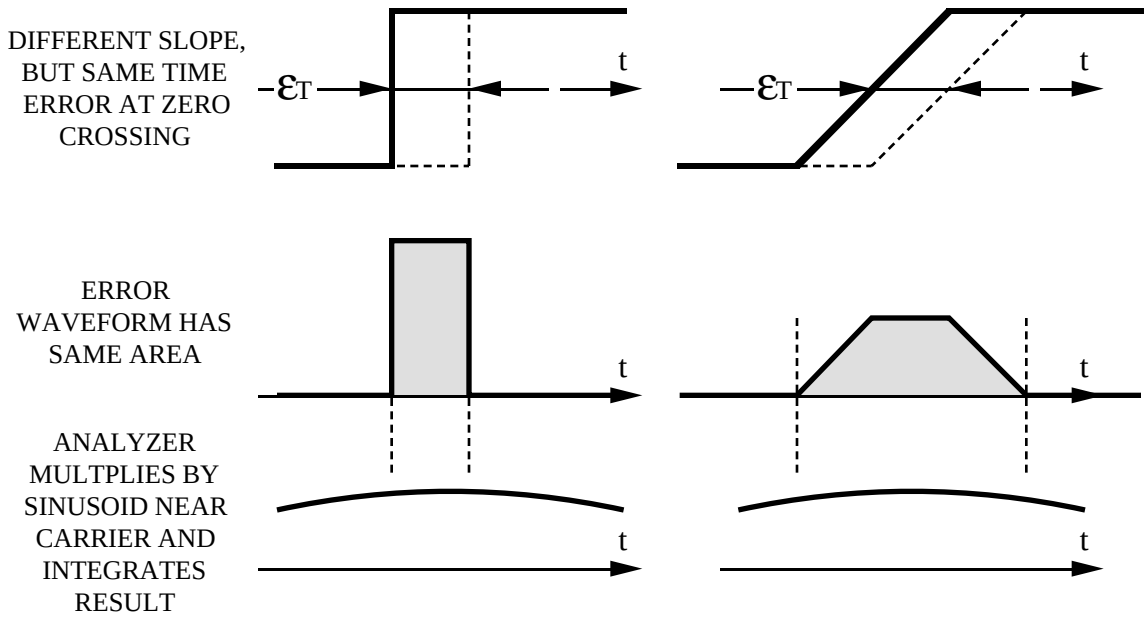


Fig. B.3. Error integrated by spectrum analyzer depends primarily on time error at zero crossing, largely unaffected by slope of waveform.

Also shown in each case is the error waveform, the difference between the actual and ideal signals. *Note that the area of the error waveforms are the same*. The spectrum analyzer takes the spectral component of each waveform by multiplying by a sine wave and integrating. As can be seen from Figure B.3, the contribution to the integral will be approximately the same regardless of the waveform slope. Hence the spectrum near the carrier will be determined primarily by the time error in the zero crossing, and will be relatively independent of the waveform slope. This is critical to preserving the link between time domain measurement and the direct spectrum measurement in the frequency domain.

C. Analysis of jitter process

When the PLL loop is closed, we can represent jitter on the recovered clock as shown in Figure C.1. Ideally the recovered clock transitions would occur at times 0, T_o, ..., nT_o, ... where T_o is the period of the transmit clock. In the presence of jitter, the transitions actually occur at time t_0, t_1, ..., t_n,.... At each transition we can define a time error in the recovered clock $\varepsilon(t_0)$, $\varepsilon(t_1)$, ..., $\varepsilon(t_n)$.... This $\varepsilon()$ process actually consists of samples of the continuous time phase noise process, expressed in units of time rather than phase angle. The figure of merit σ_x is the standard deviation of the recovered clock error $\varepsilon()$. When the loop is closed, as shown in Section 1.2, $\varepsilon()$ is wide sense stationary. Since we are only concerned with the standard deviation of $\varepsilon()$, for convenience we may also assume $\varepsilon()$ to be zero mean.

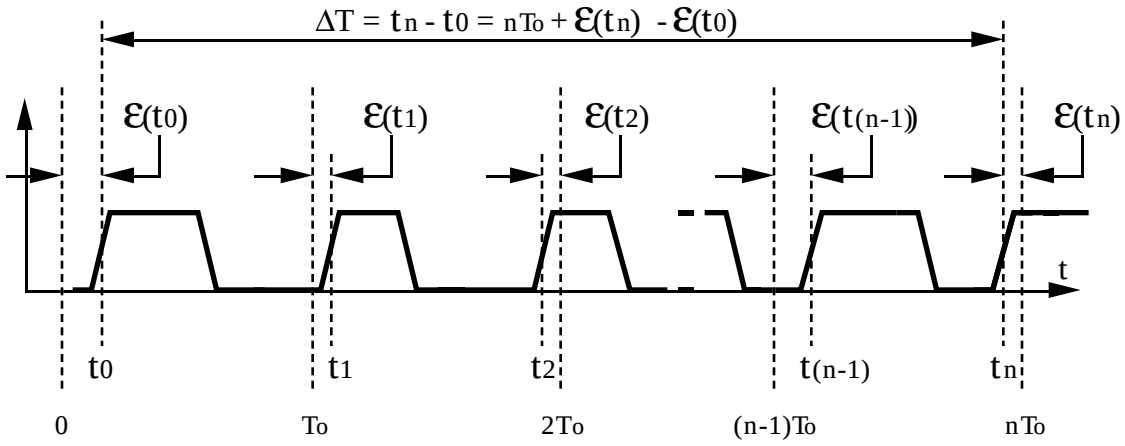


Fig. C.1. Jitter on clock recovered under closed loop conditions.

To measure $\sigma_{\Delta T(CL)}(\Delta T)$ on the CSA, we measure the standard deviation of a time interval ΔT defined by a certain number of clock periods. From Figure C.1, a specific value of ΔT for n periods of the clock would be

$$\Delta T = t_n - t_0 = nT_o + \varepsilon(t_n) - \varepsilon(t_0) \qquad \text{(C-1)}$$

Since $\varepsilon(t)$ is zero-mean, the average ΔT measured by the CSA is

$$E\{\Delta T\} = nT_o \qquad \text{(C-2)}$$

The variance $\sigma_{\Delta T(CL)}^2$ is defined as

$$\sigma_{\Delta T(CL)}^2 = E_{\{} \; (\Delta T - E\{\Delta T\})^2 _{\}} \qquad \text{(C-3)}$$

Substituting from (C-1) and (C-2) gives

$$\sigma_{\Delta T(CL)}^2 = E_{\{} \; (\varepsilon(t_n) - \varepsilon(t_0))^2 _{\}} \qquad \text{(C-4)}$$

$$\sigma_{\Delta T}^2 = E_{\{} \; \varepsilon(t_n)^2 _{\}} \quad + E_{\{} \; \varepsilon(t_0)^2 _{\}} \quad - 2 \, E_{\{} \; \varepsilon(t_n) \cdot \varepsilon(t_0) _{\}} \qquad \text{(C-5)}$$

Since $\varepsilon()$ is wide sense stationary,

$$E_{\{} \; \varepsilon(t_n)^2 _{\}} \quad = E_{\{} \; \varepsilon(t_0)^2 _{\}} \quad = \sigma_x^2 \qquad \text{(C-6)}$$

By definition of autocorrelation, assuming that the errors $\varepsilon(t_n)$, $\varepsilon(t_0)$ are much less than ΔT,

$$R_{xx}(\Delta T) = E_{\{} \; \varepsilon(t_n) \cdot \varepsilon(t_0) _{\}} \qquad \text{(C-7)}$$

Substituting (C-6) and (C-7) into (C-5) gives

$$\sigma_{\Delta T}^2 = 2 \, (\sigma_x^2 \; - R_{xx}(\Delta T)) \qquad \text{(C-8)}$$

which is used as (2-6). Although (C-8) was developed with measurements expressed in units of time (seconds), the relationship still holds for measurements in units of phase (radians), as long as consistent units are used throughout.

D. Data acquisition techniques

This appendix describes the techniques used in making the time and frequency domain jitter measurements, and extracting the figures of merit κ and N_1.

Time domain

Figure D.1 shows a sample of the time domain measurement software output. The measurement program "`jitter`" was written in HP BASIC 5.0 running on a Hewlett-Packard HP9000 series computer [104]. The data was acquired from the CSA803 over the HP-IB bus.

The user specifies the number of data points to be taken, and the minimum and maximum delay times at which jitter is to be measured. The program measures jitter at data points logarithmically spaced within the specified interval.

The program allows 5 seconds to compile the histogram at each data point. The program configures the CSA803 histogram window so that approximately 2000 "hits" (histogram data points) are accumulated. The jitter measured at each delay data point is printed.

One effect that must be compensated for is the nonzero height of the histogram box. This combines with the finite slope of the waveform to increase the measured jitter, as shown in exaggerated form in Figure D.2. This effect is compensated for by measuring the waveform slope and subtracting out its contribution. If the subtracted component is more than 10% of the measurement, the data point is flagged indicating that it may be unreliable.

The compensated measurements are plotted with a dashed line; the κ fit is plotted with a solid line. The jitter floor of the CSA803 is also plotted to provide a visual indication of when the accuracy of the CSA803 may be limiting jitter measurements.

Figure D.1. Typical time domain measurement program output.

The time domain figure of merit κ is extracted by computing $\sigma_{\Delta T}/\sqrt{\Delta T}$ for each data point, and then averaging all values together to obtain κ. In the presence of isolated anomalous measurements, this method avoids skewing of the final result that can occur with least squares techniques [105]. The predicted frequency domain N_1 is calculated using (2.1.5-7) with the extracted κ and the measured frequency f_o.

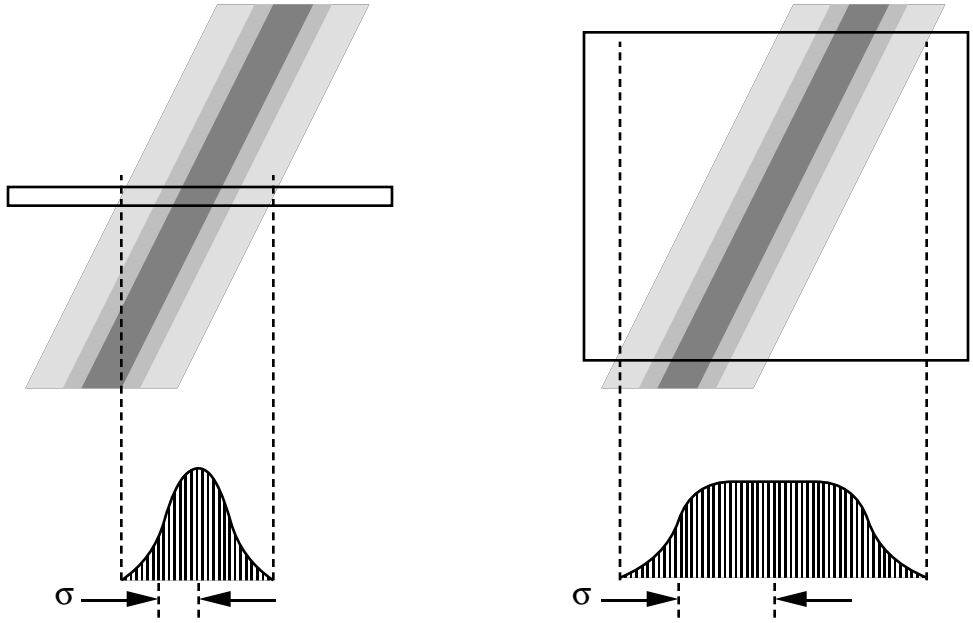


Figure D.2. Apparent increase in measured σ when height of histogram box is increased.

Figure D.3. Typical frequency domain measurement program output

Frequency domain

Figure D.3 shows a sample of the time domain measurement software output. The measurement program "`spectrum`" was written in HP BASIC 5.0 running on a Hewlett-Packard HP9000 series computer [104]. The data was acquired from the HP4195A over the HP-IB bus.

The user sets up the spectrum analyzer for a frequency span that covers the $1/f^2$ portion of the spectrum, while still being above the spectrum analyzer noise floor. The program configures the analyzer to measure noise density in units of [W/Hz]. The user must measure the carrier power separately, using the techniques detailed in [99]. When the spectrum analyzer has completed its sweep, the program reads the power density readings in each of 400 frequency bins. The readings are then normalized to the carrier power.

The normalized measurements are plotted in two ways: on a linear frequency scale, and also on a log scale of offset frequency. This gives a quick visual indication of how well the data conform to the $1/f^2$ model. The measured data is plotted with a dashed line; the N_1 fit is plotted with a solid line.

The frequency domain figure of merit N_1 is extracted by dividing the power by the offset frequency for each frequency bin, and then averaging all values together to obtain N_1. The user specifies a number of frequency bins to be excluded from this calculation ("Center bins skipped") since the $1/f^2$ model does not hold near f_o. More sophisticated spectral estimation techniques are available [9, 71] but in practice the spectra are close enough to the $1/f^2$ model that this simple technique gave good qualitative agreement to the measured data.

The "Power sum error" is the difference between the total power measured in all bins and the integrated power assuming the ideal N_1/f^2 model. This provides another qualitative indication of how well the data fit the $1/f^2$ model. The predicted time domain κ is calculated using (2-17) with the extracted N_1 and the measured frequency f_o.

E. Stationarity of two-sample variance

This appendix shows that the x[n] process for "random walk" phase noise (integrated white noise) is wide sense stationary (WSS). One of the properties of a WSS process [71] is that it has an autocorrelation that can be expressed as a function of time difference, as asserted in (3-16).

From Figures 1.12 and 3.8 and equation (1-4), we see that x[n] represents the deviation from T_o in the amount of time required to accumulate 2π radians of phase (one cycle of the clock). The integral is defined in Figure E.1: starting at time t_n, some time T_o + x[n] later phase has increased by 2π radians. Now, the <u>total</u> integrated phase error at time t_n may be arbitrarily large since white noise is being integrated into a random walk over infinite time. But x[n] represents the phase error integrated over a <u>finite</u> time interval, equal (on average) to T_o. The essence of proving x[n] to be WSS is that a finite duration integral is a stable, linear time invariant (LTI) system. The input V_{ctl} process is WSS, and for a stable LTI system a WSS input implies a WSS output [71].

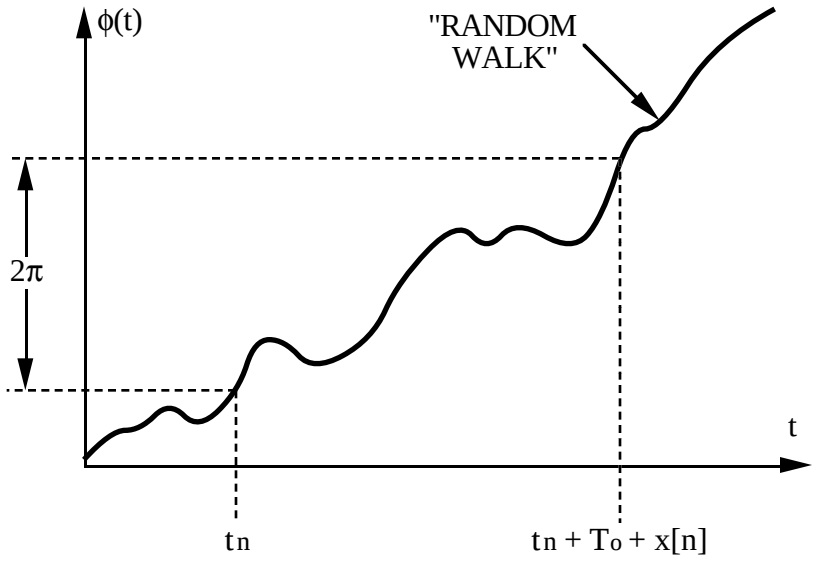


Figure E.1. Definition of x[n] for stationarity proof.

So, from time t_n to time $t_n + T_o + x[n]$, phase has increased by 2π:

$$\phi(t_n + T_o + x[n]) - \phi(t_n) = 2\pi \qquad \text{(E-1)}$$

Using the definition of phase from (1-4) with the arguments of (E-1) gives

$$2\pi = \omega_o(T_o + x[n]) + K_o \int_{t_n}^{t_n + T_o + x[n]} V_{ctl}\, dt \qquad \text{(E-2)}$$

where V_{ctl} is the white noise source at the VCO input that is being integrated in phase. Since $2\pi = \omega_o T_o$, (E-2) can be simplified to

$$x[n] = \frac{-K_o}{\omega_o} \int_{t_n}^{t_n + T_o + x[n]} V_{ctl}\, dt \qquad \text{(E-3)}$$

If we assume $x[n] << T_o$ (consistent with the small angle approximation), then (E-3) becomes

$$x[n] \approx \frac{-K_o}{\omega_o} \int_{t_n}^{t_n + T_o} V_{ctl}\, dt \qquad \text{(E-4)}$$

So x[n] is simply the integral of the (stationary) V_{ctl} process over a window of width T_o. Since a finite integral is a stable LTI system, and the input V_{ctl} is WSS white noise, the output x[n] is also WSS. Therefore the autocorrelation can be written in terms of time difference, and (3-16) is valid.

F. Variance of clock period errors

In this appendix, we first find the $R_{xx}[0]$ term of the autocorrelation for a white noise phase process. Then we determine the entire autocorrelation for the more general case of bandlimited white noise.

$R_{xx}[0]$ term for a white noise process

One property of the autocorrelation [71] is that the $R_{xx}[0]$ term is equal to the variance (rms power), which is given by integrating the p.s.d. over all frequencies:

$$R_{xx}[0] = \sigma^2 = \int_{-\infty}^{\infty} S_{xx}(f)\, df \qquad \text{(F-1)}$$

As shown in (E-4), the x[n] process is related to the integral of the control voltage over a time window of duration T_o. So from (E-4), the p.s.d. of the x[n] process is the white noise p.s.d. multiplied by the p.s.d. of an integral:

$$S_{xx}(f) = \left(\frac{K_o}{\omega_o}\right)^2 \frac{e_n^2}{2}\ T_o^2 \frac{\sin^2 \pi f T_o}{(\pi f T_o)^2} \qquad \text{(F-2)}$$

This is shown graphically in Figure F.1.

Substituting (F-2) into (F-1) and carrying out the integral gives

$$R_{xx}[0] = \sigma^2 = \left(\frac{K_o}{\omega_o}\right)^2 \frac{e_n^2\, T_o}{2} \qquad \text{(F-3)}$$

This is the result used in (3-18).

General case: bandlimited white noise

The result in (F-3) could also have been obtained by convolving the autocorrelations of the integral and white noise p.s.d.s. Since the desired result is an autocorrelation and the mathematics is simpler, this is the method that will be used for the bandlimited white noise case.

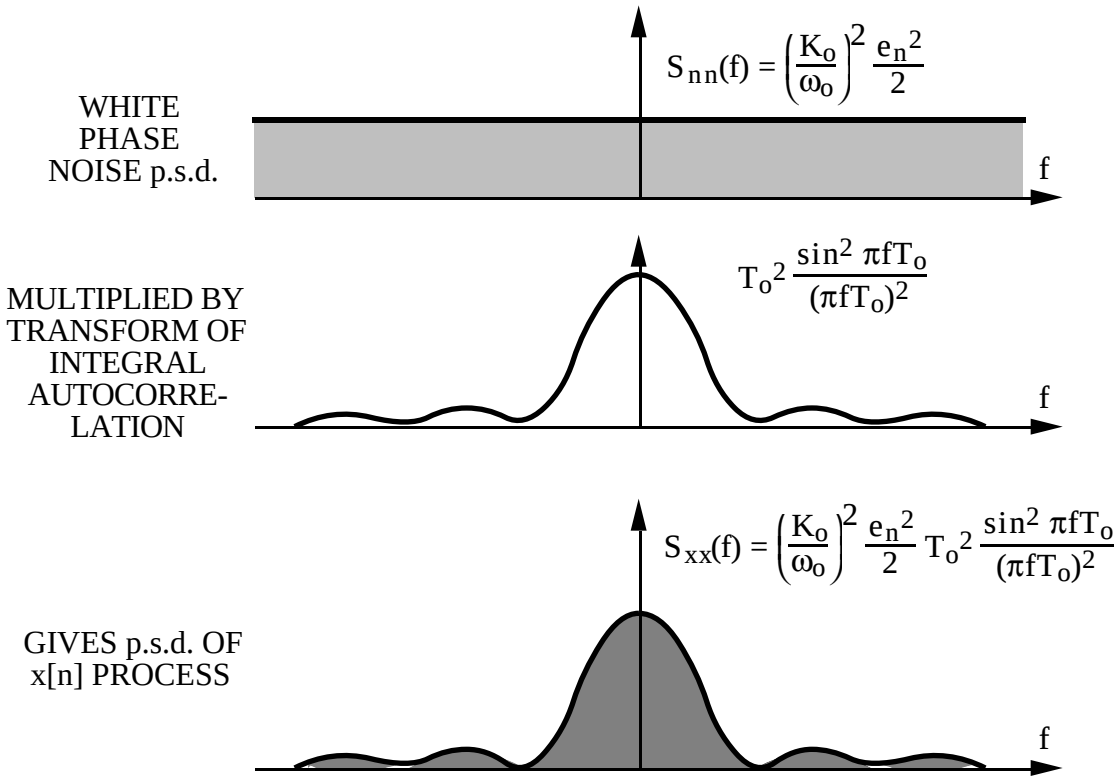


Fig. F.1. Graphical determination of p.s.d. for x[n] process.

For mathematical simplicity, we will assume that the noise remains correlated for several periods of the clock, that is, $T_o << 1/\omega_n$. With this assumption, the autocorrelation of the bandlimited white noise is

$$R_{xx}[\tau] = \left(\frac{K_o}{\omega_o}\right)^2 \frac{\omega_n \, e_n^2 \, T_o}{4} \exp(-\omega_n|\tau|) \qquad \text{(F-4)}$$

In the discrete time case, we are concerned with delays of the form

$$\tau = (i - j) \, T_o \qquad \text{(F-5)}$$

Substituting into (F-4) gives

$$R_{xx}[i - j] = \left(\frac{K_o}{\omega_o}\right)^2 \frac{\omega_n \, e_n^2 \, T_o}{4} \exp(-\omega_n \, T_o|i - j|) \qquad \text{(F-6)}$$

This is the autocorrelation used in the procedure of equation (3-17). To simplify the mathematics, (F-6) can be expressed in the form

$$R_{xx}[i - j] = K \; a^{|i - j|} \qquad \text{(F-7)}$$

where K and a are given by

$$K = \left(\frac{K_o}{\omega_o}\right)^2 \frac{\omega_n \, e_n^2 \, T_o}{4} \qquad \text{(F-8)}$$

$$a = \exp(-\omega_n T_o) \qquad \text{(F-9)}$$

Substituting into (3-17) gives

$$\sigma^2_{(m)} = K \sum_{i=-m}^{m} (m - |i|) \, a^{\,i} \qquad \text{(F-10)}$$

Using the symmetry in summation provided by the absolute value, we can write (F-10) as

$$\sigma^2_{(m)} = Km + 2K \sum_{i=1}^{m} (m - i) \, a^{\,i} \qquad \text{(F-11)}$$

We will now examine the asymptotes that (F-11) approaches for small and large values of m.

For small m ($1 << m << -1/\ln(a)$), $a^i \approx 1$. Using the formula for sum of arithmetic series gives

$$\sigma^2_{(m)} \approx Km + 2K \sum_{i=1}^{m} (m - i) \qquad \text{(F-12)}$$

$$\sigma^2_{(m)} \approx (m+1)^2 K \approx m^2 K \qquad \text{(F-13)}$$

With the values for K from (F-8), (F-13) gives the result in (3-27).

For large m, we can expand (F-11) to

$$\sigma^2_{(m)} = Km + 2Km \sum_{i=1}^{m} a^{\,i} - 2K \sum_{i=1}^{m} i \, a^{\,i} \qquad \text{(F-14)}$$

Using the formulae for sums of geometric series gives in the limit as m approaches infinity

$$\sigma^2_{(m)} \approx Km + \frac{2Km}{1 - a} \approx \frac{2K}{1 - a} \, m \qquad \text{(F-15)}$$

For a we use (F-9), with the first order Taylor series approximation for $\exp(-\omega_n T_o)$

$$a \approx 1 - \omega_n T_o \qquad \text{(F-16)}$$

in (F-15) to obtain

$$\sigma^2_{(m)} \approx \frac{2K}{\omega_n T_o}\, m \qquad \text{(F-17)}$$

Which gives the result in (3-29) using the value for K from (F-8).

G. Exponential waveform coupling

This appendix considers the effect on delay in an exponential delay stage of jitter in other stages. Figure G.1 shows an idealized exponential delay stage waveform with delay δ; the waveform voltage v(t) is normalized to the peak amplitude $I_{EE}R_C$. This is part of an N stage ring; the delay of the other (N-1) stages are lumped into one ideal delay D. We will find the change in the stage delay δ caused by a change in the delay D of the other stages; for small changes in D this is approximately the derivative:

$$\frac{\Delta\delta}{\Delta D} \approx \frac{d\delta}{dD} \qquad \text{(G-1)}$$

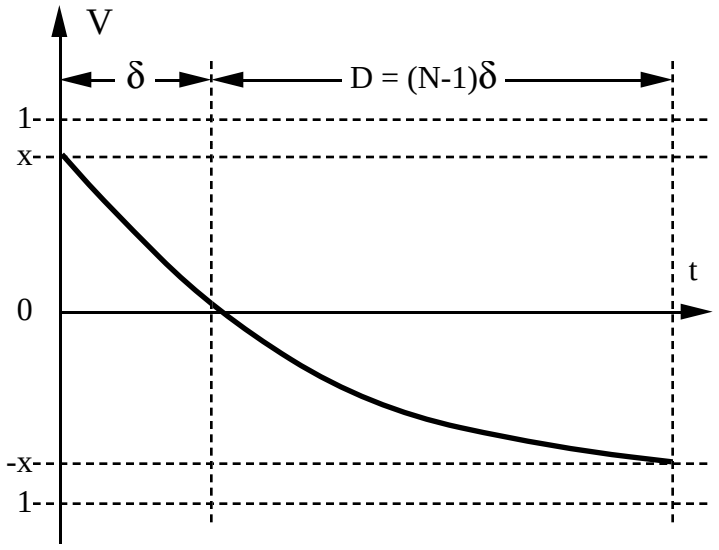


Fig. G.1.
Normalized exponential delay waveform.

N	x	$\frac{d\delta}{dD}$ $\frac{(1-x)}{(1+x)}$
3	0.618	0.236
4	0.840	0.087
5	0.927	0.038

Table G.2.
Delay coupling as a function of N.

In equilibrium, both δ and D are related to the peak excursion x. For an ideal exponential, the waveform after a transition at time t=0 is given by

$$v(t) = (1 + x)\exp(-t/\tau) - 1 \qquad 0 < t < D + \delta \qquad \text{(G-2)}$$

where $\tau = R_C C_C$. Then it is straightforward to show that

$$\delta = \tau \ln(1+x) \qquad \text{(G-3)}$$

$$D = -\tau \ln(1-x) \qquad \text{(G-4)}$$

Taking derivatives of (G-3) and (G-4) with respect to x give

$$\frac{d\delta}{dx} = \frac{\tau}{1+x} \qquad \text{(G-5)}$$

$$\frac{dD}{dx} = \frac{\tau}{1-x} \qquad \text{(G-6)}$$

Applying the chain rule to (G-1) gives

$$\frac{d\delta}{dD} = \frac{d\delta}{dx}\frac{dx}{dD} \qquad \text{(G-7)}$$

Substituting (G-5) and (G-6) into (G-7) gives

$$\frac{d\delta}{dD} = \frac{1-x}{1+x} \qquad \text{(G-8)}$$

From (G-8) we see that dδ/dD is positive: *an error in D causes an error of the same sign in δ.* Hence this coupling mechanism increases jitter over what would be expected if delay errors were completely independent.

The relationship between x and the number of stages in the ring N is transcendental; there is no convenient closed form expression for dδ/dD as a function of N. Table G.2 shows calculated values of x and dδ/dD for some values of N. The coupling becomes less significant quite rapidly as N increases.

H. Differential pair switching delay

The purpose of this appendix is twofold: first, to validate the assumptions in Section 4.1 by determining the approximate magnitudes of the components of switching time, and second, to illustrate the sources of switching time temperature dependence. Figure H.1 shows the current-mode differential pair for which switching speed is analyzed in [101]. The analysis assumes no capacitive loading on the collector node. This represents the minimum switching time that can be achieved. We will see that this minimum time is much less than the RC time constant of the collector load used in the AD806, validating the assumption made in Section 4.1.

Figure H.1. Differential pair for switching time calculations.
(After [101] Figure 8-1-2. © Motorola 1969)

The 10%-to-90% rise time is given in [101] as

$$t_r = \frac{0.8\ (\ 1/\omega_\tau + R_L\ C_{ob})\ I_C}{E_1/(R_S + 2r'_B)} \qquad \text{(H-1)}$$

where $\omega_\tau = 2\pi f_T$ is the cutoff frequency expressed in rad/s, C_{ob} is the base-to-collector capacitance also known as C_{jc}, I_C is the DC collector current, E_1 is the magnitude of the differential waveform, R_S is the source resistance of the circuit driving the differential pair, and r'_B is the bulk resistance from the base contact to the base-emitter junction [31].

We now make the following modifications and simplifying assumptions:

1) Since we are looking for the 0% to 50% time to the threshold crossing of the differential waveform, replace 0.8 with 0.5.
2) The magnitude of the differential waveform is given by

$$E_1 = I_C R_L \qquad \text{(H-2)}$$

3) Assume $R_S << 2r'_B$. In the case of the AD806, R_S is the incremental output resistance r_e of an emitter follower, and is approximately 250Ω. For the minimum geometry transistor in the XFCB process, r'_B is of order 1kΩ.
4) Assume f_T is determined by base transit time, so that

$$\frac{1}{\omega_\tau} = \tau_T \qquad \text{(H-3)}$$

Substituting into (H-1) and simplifying gives

$$t_{sw} = \frac{r'_B}{R_L}\,\tau_T + r'_B\,C_{jc} \qquad \text{(H-4)}$$

Equation (H-4) shows how the switching time is influenced by temperature: r'_B is a silicon resistor with temperature coefficient of order +1000 ppm/°C [106]. Transit time τ_T and capacitance C_{jc} are also temperature dependent, although not as strongly.

Substituting typical values for the XFCB process of r'_B = 1kΩ, τ_T = 30ps, C_{jc} = 20fF [106], and the nominal R_L = 3kΩ, gives

$$t_{sw} = 30 \text{ ps} \qquad \text{(H-5)}$$

which is an order of magnitude less than the RC time constant of the collector load. For the AD806, the total load capacitance (including wiring strays) was approximately 200 fF. The switching delay due to the nominal RC time constant is

$$t_{nom} = \ln(2)R_L C_L = (0.693)(3k\Omega)(200fF) = 415 \text{ ps} \qquad \text{(H-6)}$$

In practice, even without such a large explicit load capacitance, substrate capacitance and wiring strays on the collector node may be the limiting factor on speed, rather than the minimum switching time of (H-4). So the assumption that most of the switching delay is due to an $R_L C_L$ time constant is quite reasonable.

To get a rough estimate of the total switching time, we can simply add (H-4) and (H-6). This is similar to the "zero-value time constant" technique used in [31] for small signal analysis. The result is

$$t_{sw} = \frac{r'_B}{R_L}\,\tau_T + r'_B\,C_{jc} + \ln(2)R_L C_L \qquad \text{(H-7)}$$

Note that this appendix seeks only to determine the approximate magnitudes of the components of switching time. By no means is this an exact solution. (H-7) predicts a delay of 445 ps, whereas the actual delay is approximately 640 ps. The difference is due to the delay of the emitter followers as well as the longer delay in the interpolator due to larger stray capacitances. Nevertheless, (H-7) is valuable for comparing the relative contributions to total switching time of the differential pair.

One shortcoming of the analysis in [101] is that it assumes an input step that is much faster than the eventual switching time. In a ring oscillator, this is not a valid approach since the input is just the output of a previous, identical stage. In [72], Simmons approaches this problem for MOS elements by solving for a "self-consistent" waveform. Presumably this approach could be applied to bipolar delay elements as well, which would give a more accurate estimate of switching time than (H-1).

I. Time-domain (transient) noise source simulation

This appendix first describes the use of random pulse waveforms to simulate white noise in the simulations of Section 4.2.1. Then the use of pulse waveforms as an analysis tool in Section 4.1.3 is described.

Transient noise simulation

The simulations were run on ADICE [94], which is a proprietary extension of SPICE [95] developed by Analog Devices, Inc. Transient noise simulation is necessary since small signal noise analysis (for example, the .NOISE analysis in SPICE) does not accurately model the effects of noise on the large signal switching waveforms encountered in the ring oscillator. For transient noise simulation, noise sources are modeled by random voltage (or current) sources with time domain behavior appropriate to the noise being simulated. The response of the circuit is accurately modelled since the transient analysis numerically solves the (nonlinear) differential equations that describe the circuit's large signal behavior. The statistics of the circuit's noise response can be determined by repeating the simulation in Monte Carlo fashion.

Figure I.1 shows an example of a "pulsed sample-and-hold" (PSH) source waveform [94] which can be used to approximate a white Gaussian noise source. The waveform consists of pulses of duration T. The amplitudes of the pulses are independent, identically distributed Gaussian with standard deviation σ_v. The following analysis is for a PSH voltage source; the analysis for a current source is similar.

By properly specifying T and σ_v, it is possible to approximate a white noise source with density e_n (in $V/\sqrt{Hz}$). This is most easily done by considering the autocorrelation of the waveform, its p.s.d., and comparing that to the p.s.d. of ideal white noise.

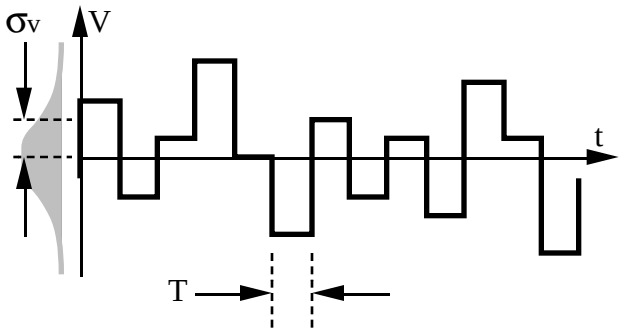


Fig. I.1. Pulsed sample-and-hold waveform for transient noise simulation

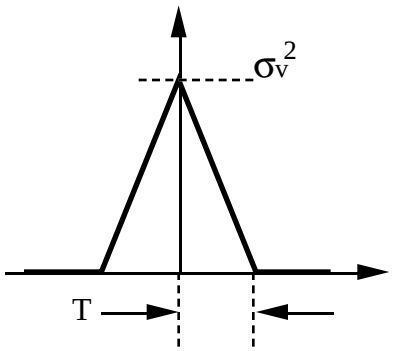


Fig. I.2. Autocorrelation of pulsed sample-and-hold waveform.

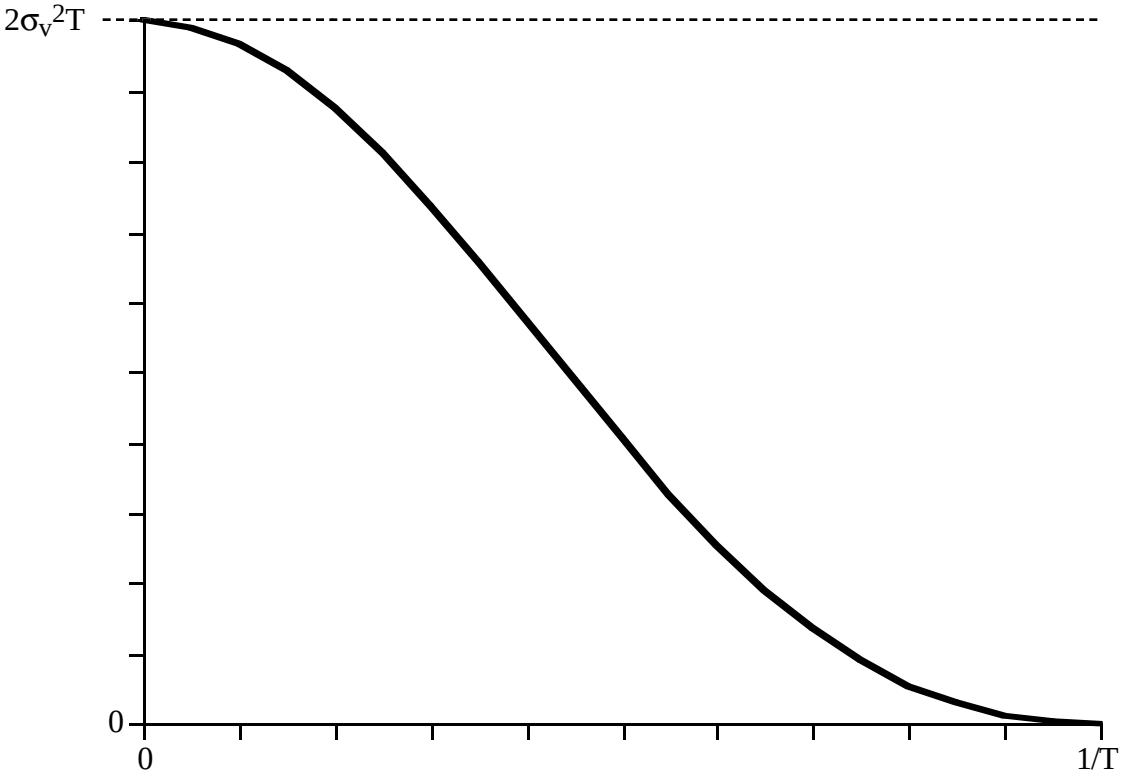


Fig. I.3. Single-sided p.s.d. of pulsed sample-and-hold waveform.

The autocorrelation $R_{xx}(t)$ of the waveform in Figure I.1 is shown in Figure I.2. A Fourier transform gives the p.s.d., which in this case is the familiar sinc^2 function:

$$S_{xx}(f) = (\sigma_v^2 T)\,\frac{\sin^2 \pi fT}{(\pi fT)^2} = (\sigma_v^2 T)\,\text{sinc}^2(\pi fT) \qquad \text{(I-1)}$$

Equation (I-1) is expressed in the two-sided frequency domain, whereas in circuit design noise densities are usually specified in the single-sided frequency domain. The single-sided p.s.d. is

$$S_{xx}(f)_{[SS]} = (2\sigma_v^2 T)\,\text{sinc}^2(\pi fT) \qquad \text{(I-2)}$$

Figure I.3 is a plot of (I-2) for frequencies between 0 and 1/T. From the plot, it is seen that for frequencies << 1/T, the pulsed waveform has a nearly constant spectral density of $2\sigma_v^2 T$. As long as the circuit bandwidth is small compared to 1/T, the pulsed source will have nearly the same effect as an ideal white noise source with power density e_n^2 as shown in the figure. Equating $2\sigma_v^2 T$ with e_n^2 and solving for σ_v in terms of the desired voltage noise density e_n gives

$$e_n^2 = 2\sigma_v^2 T \qquad \text{(I-3)}$$

$$\sigma_v = \frac{e_n}{\sqrt{2T}} \qquad \text{(I-4)}$$

To specify the PSH source, first the pulse width T is chosen such that 1/T is much greater than the highest frequency of interest in the circuit being simulated. Then (I-4) is applied with the desired density e_n to give the necessary standard deviation σ_v.

For current noise, a similar analysis gives the standard deviation

$$\sigma_i = \frac{i_n}{\sqrt{2T}} \qquad \text{(I-5)}$$

Section 4.2.1 simulations

For the simulations in Section 4.2.1, T was chosen to be a factor of 100 smaller than the RC time constant of the circuit. For each case, the simulation was repeated 100 times.

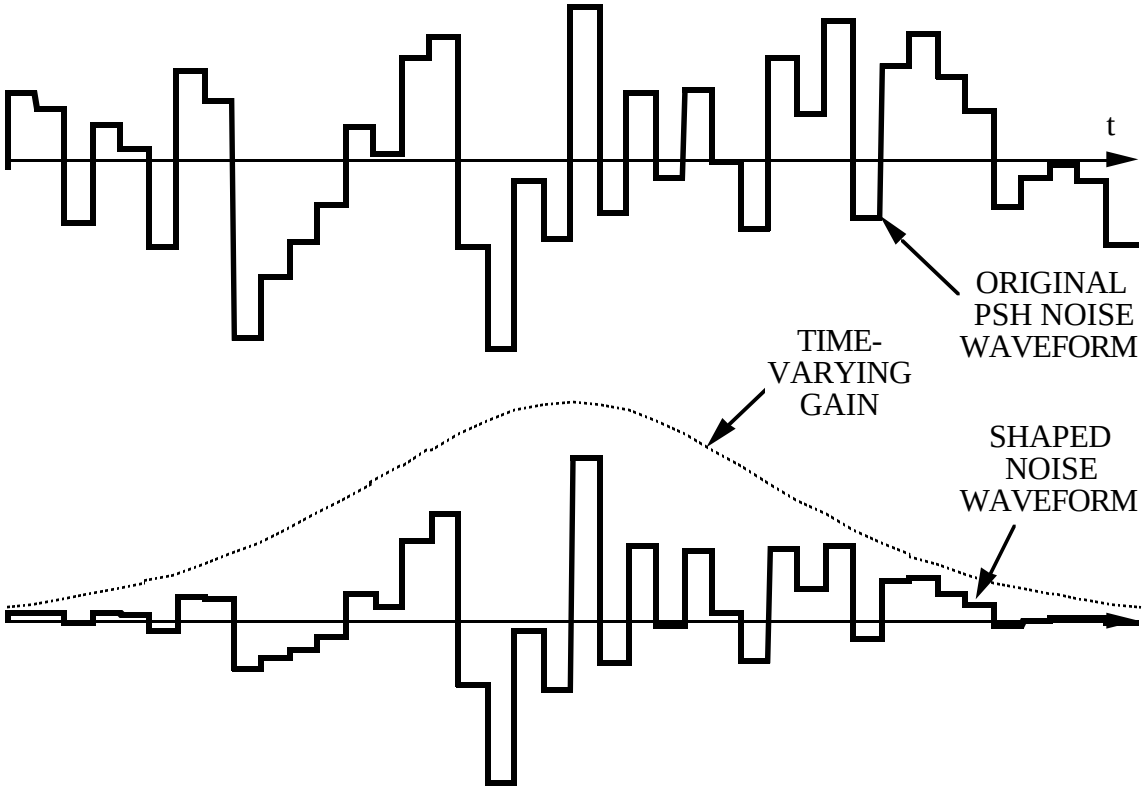


Figure I.4. PSH noise waveform shaped by time-varying gain

Analysis using pulse waveforms

The analysis of Section 4.1.3 represents white noise as a sequence of random pulses of duration dt. Each pulse is scaled by the time-varying gain of the differential amplifier, as shown in Figure I.4. Passing to the limit of infinitesimal dt in analysis is equivalent to setting T = 0 in the p.s.d. of I-1. Using the definition of σ_v in (I-4), we see that (I-1) is a constant $e_n/2$, which is ideal white noise suitable for analysis.

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Vita

John McNeill was born in Syracuse, New York, in 1961. At Dartmouth College, he started on an educational path of physics and computer science, but became interested in analog electronics after taking Engineering Sciences 64 from Prof. W. D. Stratton. Upon graduation in 1983, he went to work for Analogic Corp. in Wakefield, Massachusetts. There he designed high speed, high resolution A/D converters and data acquisition systems. In 1986, he joined Adaptive Optics Associates in Cambridge, Massachusetts. There he designed low noise interface electronics for charge coupled device (CCD) cameras used in high speed, wide dynamic range imaging systems.

In 1990, he began graduate studies in the Ph.D. program at the University of Rochester in Rochester, New York. After becoming engaged to a Boston-area resident, he completed the M.S.E.E. degree in 1991, moved back to the Boston area, and entered the Boston University Ph.D. program as a Presidential University Graduate Fellow. While completing the work in this thesis, he has also taught the graduate-level bipolar and MOS analog circuit design courses, as well as consulted in the area of CCD camera design.

In the future, he intends to pursue an academic career combining teaching and research in analog integrated circuit design.