On-Chip Transformer Design and Application to RF and mm-Wave Front-Ends

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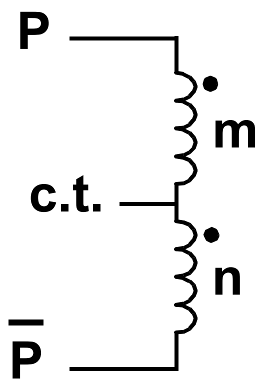
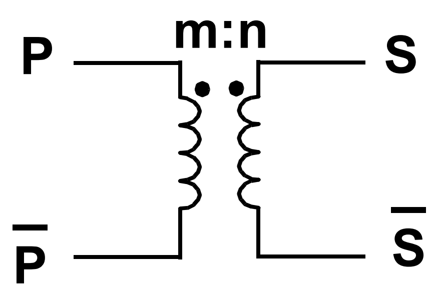
Outline

- Introduction
- On-chip transformer types and circuit models
- Specifications
- Design for RF and mm-Wave circuit applications (LNA, PA, VCO)
- Summary

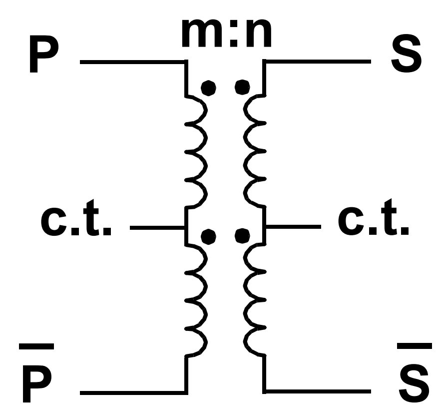
Transformer Types



autotransformer



step-up/step-down



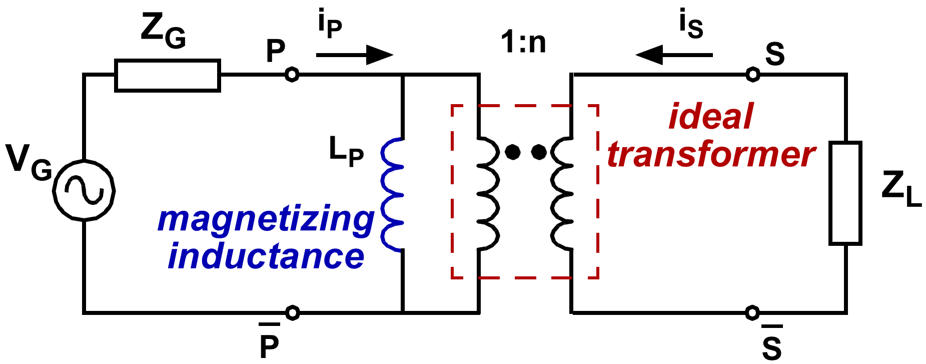
balun

- Autotransformer: primary and secondary are *not* DC-isolated. Conductor losses and leakage inductance may be lower than a multi-winding transformer (optimal when m=n). Primary application is LC-oscillator tanks.

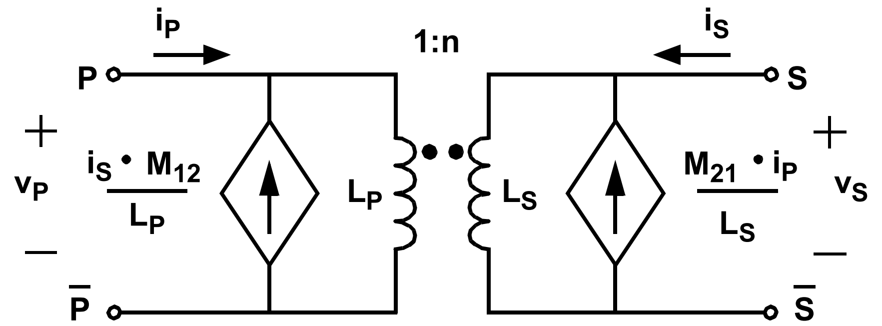
- Step-up/step-down transformer: Bias isolation between primary and secondary. Applied to impedance matching, interstage (AC) coupling, feedback networks, filtering, etc. Can consist of more than two windings.

- Balun: center-tapped (c.t.) transformer used as a phase splitter/combiner. Applications include: on- and off-chip interfacing, and interstage (AC) coupling.

The “Perfect” Transformer



circuit function



circuit model

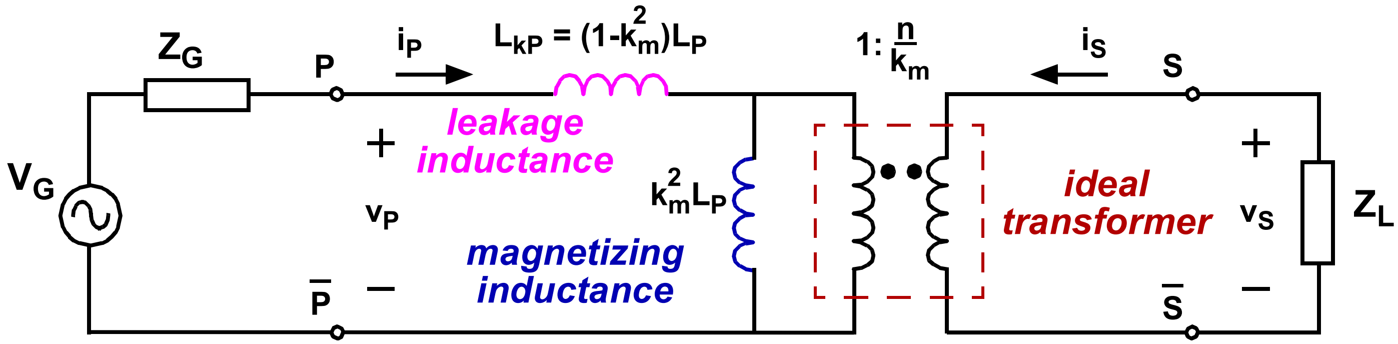
- When reactance of the magnetizing inductance (L_P) is much larger than the source impedance (Z_G) and the reflected load impedance (Z_L/n^2):

$$v_S = n \cdot v_P,\ i_S = i_P / n, \text{ and } Z_S = n^2 \cdot Z_P .$$

$$\text{Turns ratio, } n = \frac{v_S}{v_P} = \frac{i_P}{i_S} = \sqrt{\frac{L_S}{L_P}} .$$

- For “perfect” (i.e., 100%) magnetic coupling: $M_{21} = M_{12} = \sqrt{L_P L_S}$.

Transformer with Magnetic Leakage



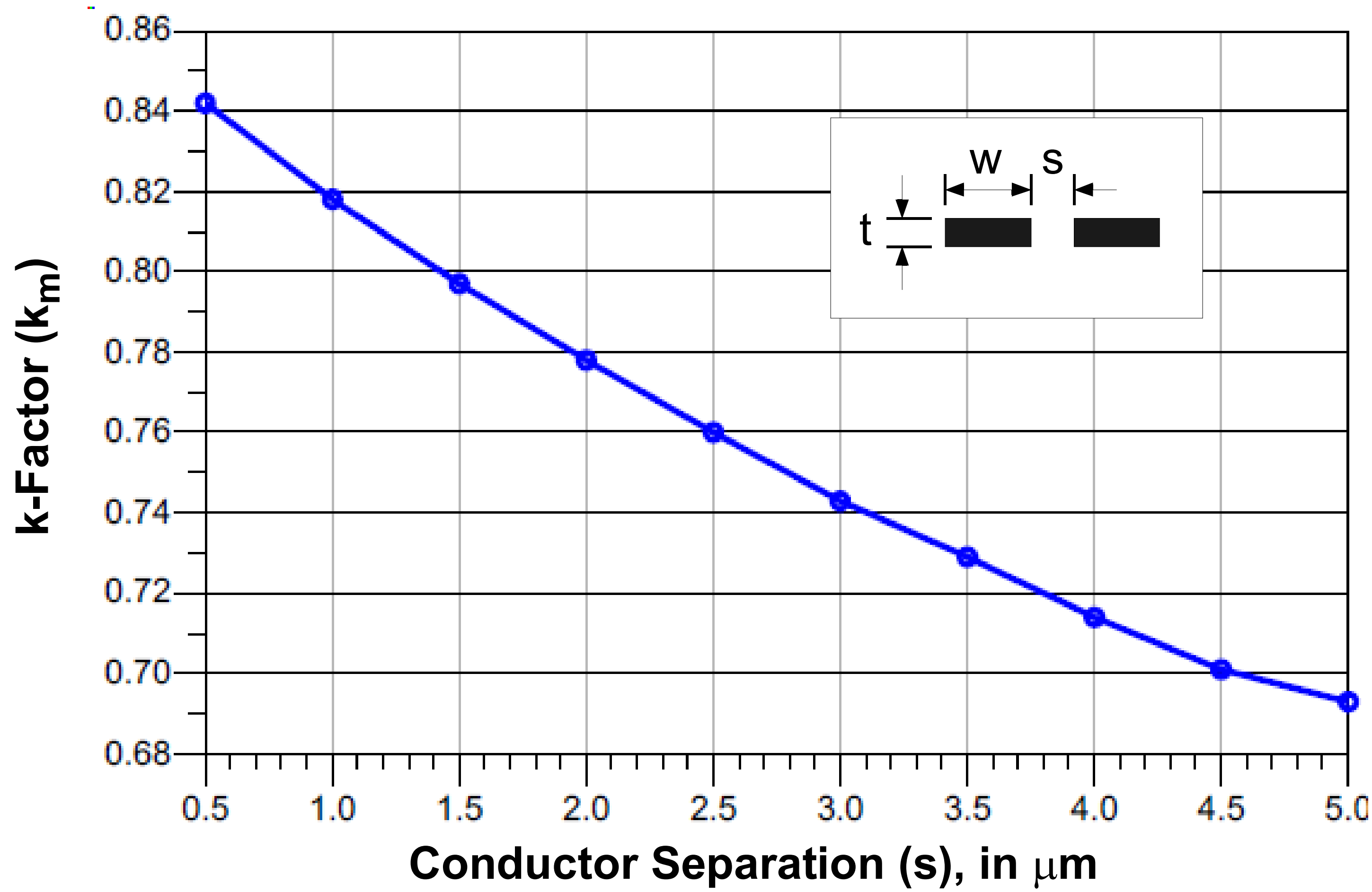
model for magnetic path including leakage

- Imperfect magnetic coupling between primary and secondary windings is called *leakage*, which is characterized by the coefficient of magnetic coupling, k_m

$$k_m = \frac{M}{\sqrt{L_P L_S}}, \text{ and } 0 < k_m < 1.$$

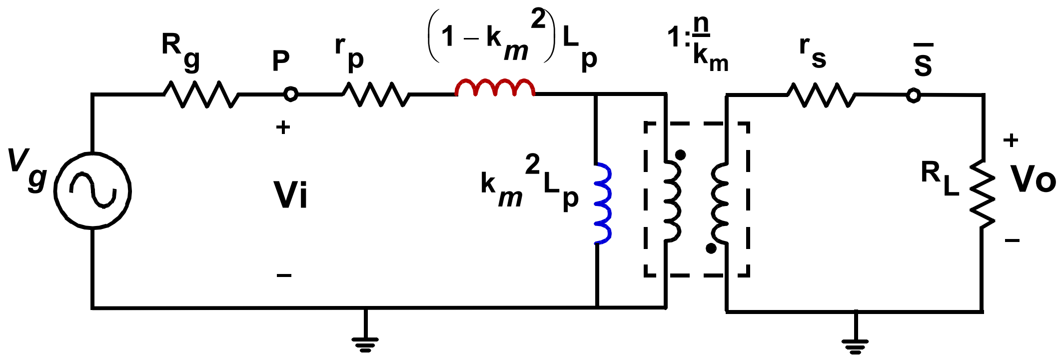
- Leakage prevents signal at the primary input from reaching the secondary output as the frequency increases. Leakage is reduced by shrinking the gap between turns on the windings of an on-chip transformer.

Transformer k-Factor



- k-factor approaches 0.9 for minimum spacing (s) between conductors. Ratio of conductor length and separation diminishes when scaling transformers to mm-wave frequency, which further reduces k-factor.

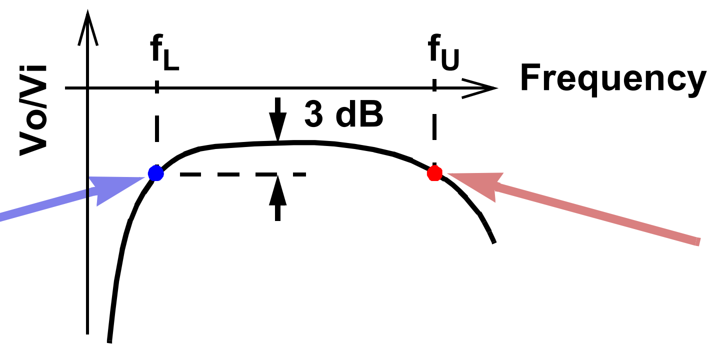
Transformer L.F. Response



Low-frequency equivalent circuit with leakage k_m

$$\frac{f_U}{f_L} = \frac{(1 + k_m)}{(1 - k_m)} \qquad f_U/f_L = 2,\ \text{for km} = 0.33 \qquad f_U/f_L = 9,\ \text{for km} = 0.8$$

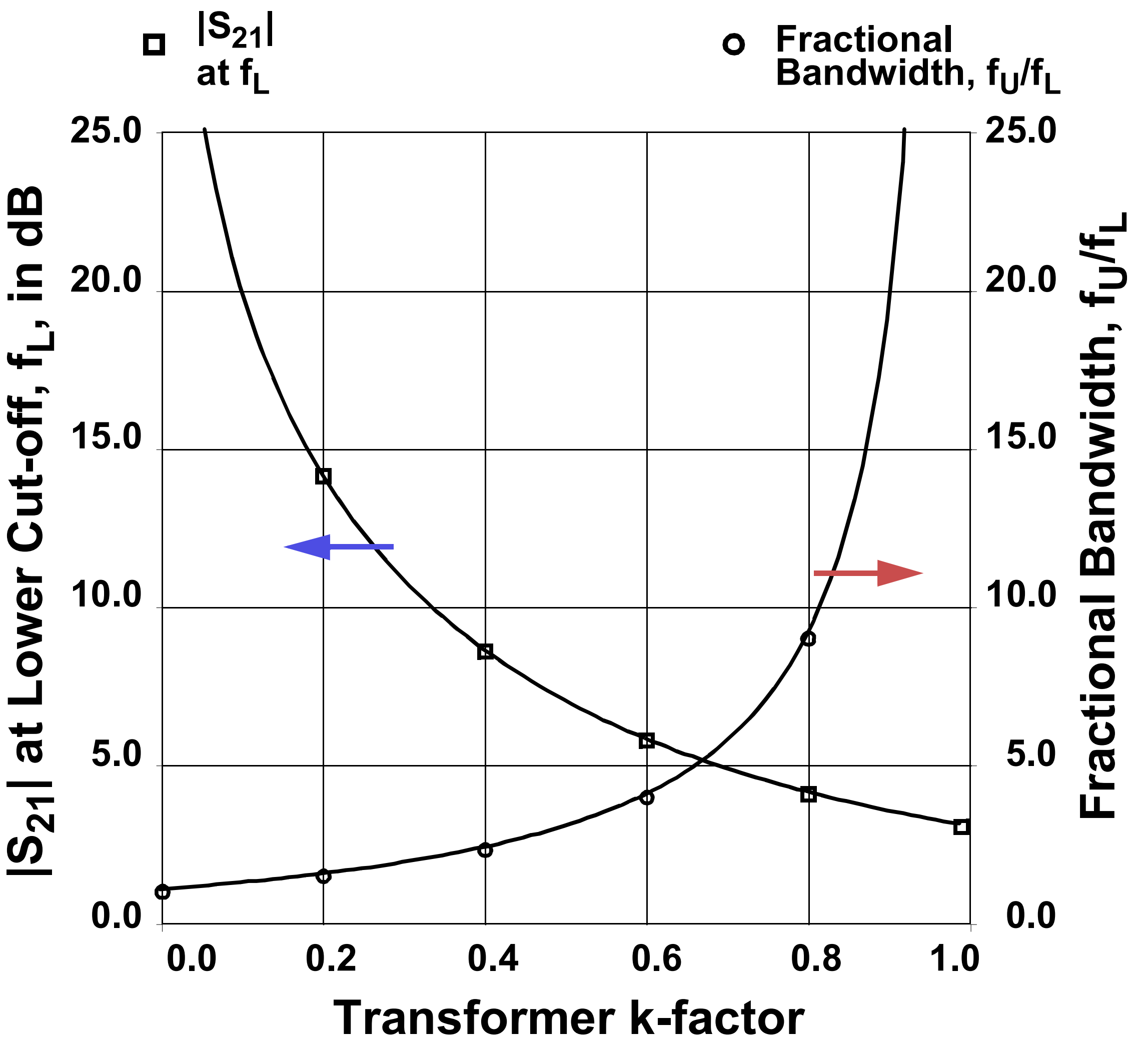
$$f_L \approx \frac{1}{2\pi}\frac{(R_g + r_p) \parallel R_r}{k_m^2 L_p}$$



$$f_U \approx \frac{1}{2\pi}\frac{(R_g + r_p) + R_r}{(1 - k_m^2) L_p}$$

Rr = resistance reflected from secondary back to primary

Transformer M.F. Response



Assuming capacitive parasitics are negligible and $R = R_G + r_P = R_L + r_S$

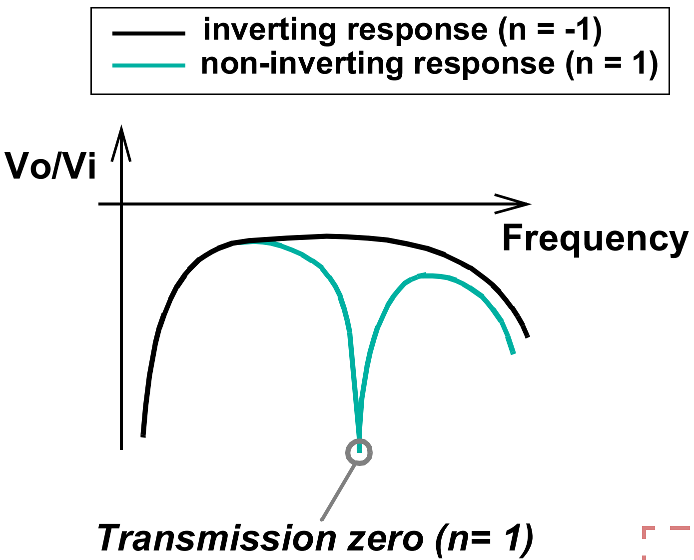
Max. signal transmission in the passband is:

$$|S_{21}| = \frac{2v_o}{v_G} = \frac{k_m(R_L)}{R}$$

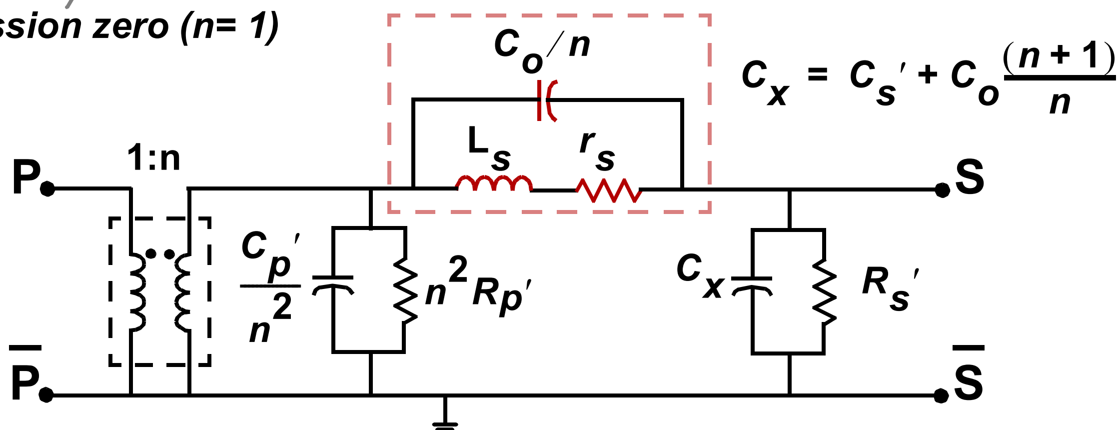
at

$$f_{pk} = \frac{R}{2\pi L_P\sqrt{1-k_m^2}}.$$

Transformer H.F. Response

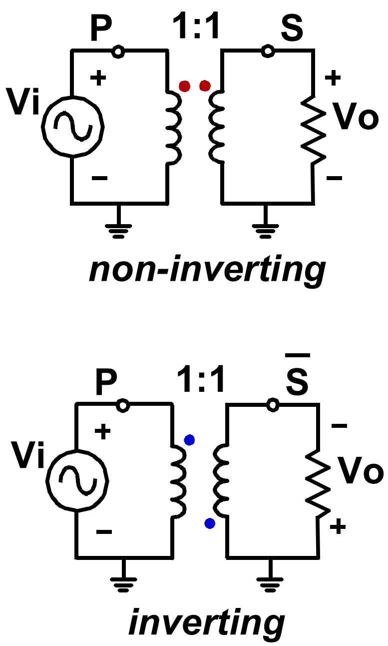


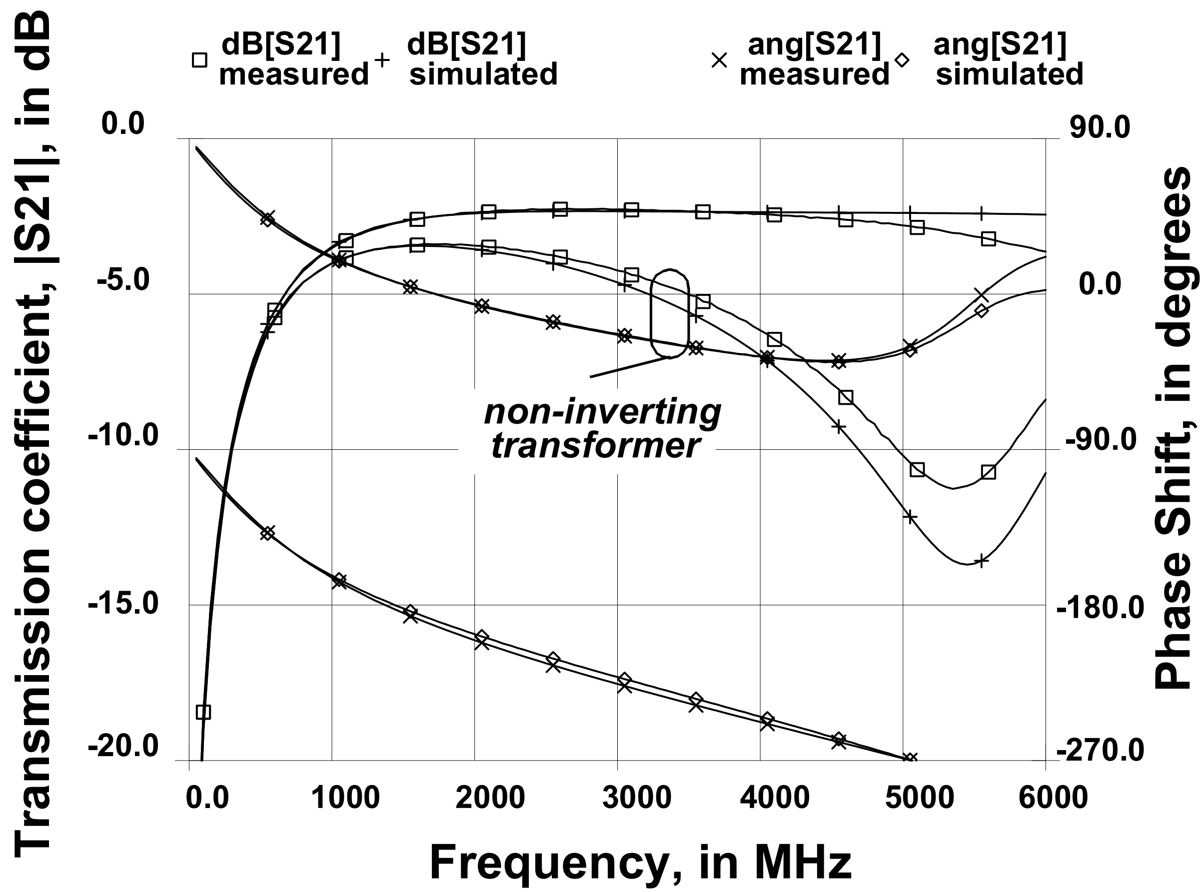
- For n > 0, (Co/n), L_s and r_s introduce a transmission zero.
- For n < 0, (Co/n) is an inductive reactance that decreases in magnitude with increasing frequency. No notch in response.



High-frequency equivalent circuit with leakage shifted to secondary

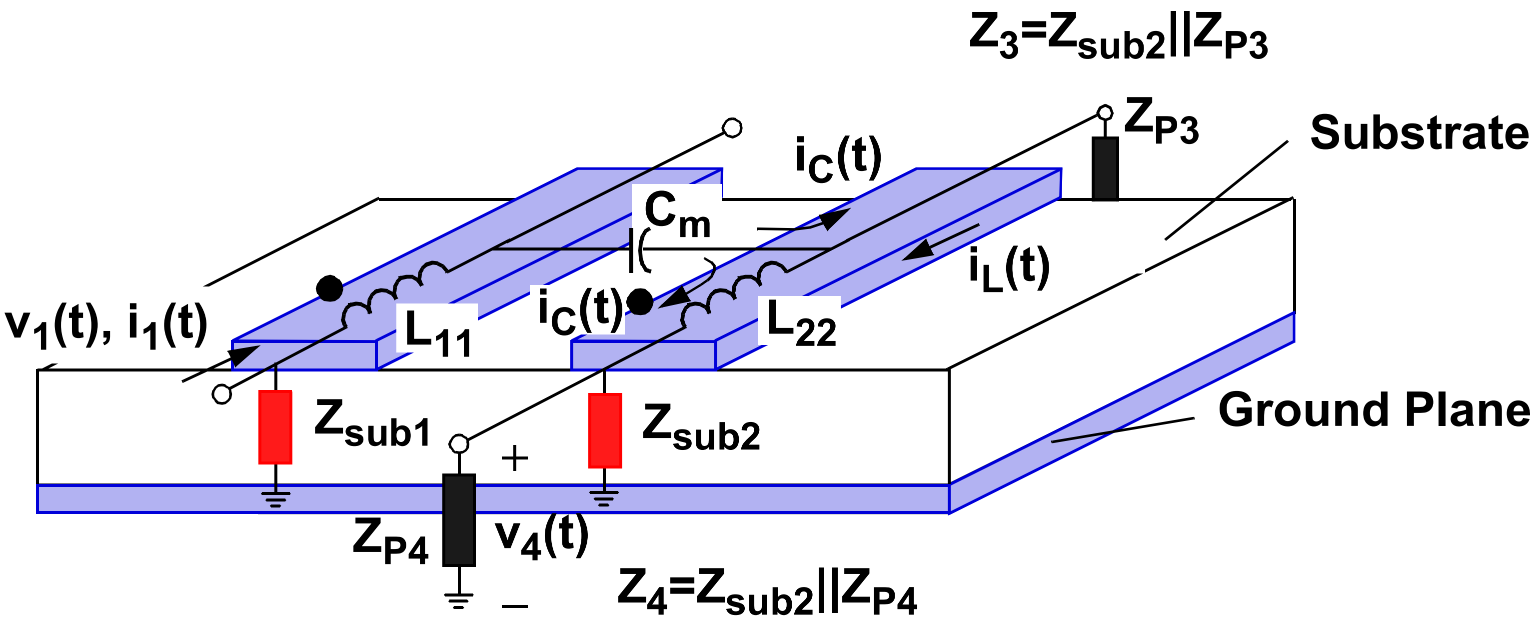
Inverting vs. Non-Inverting





- Frequency response in the inverting configuration (single-ended) is less constrained by effects of interwinding capacitance.

A 2-Wire Planar Transformer

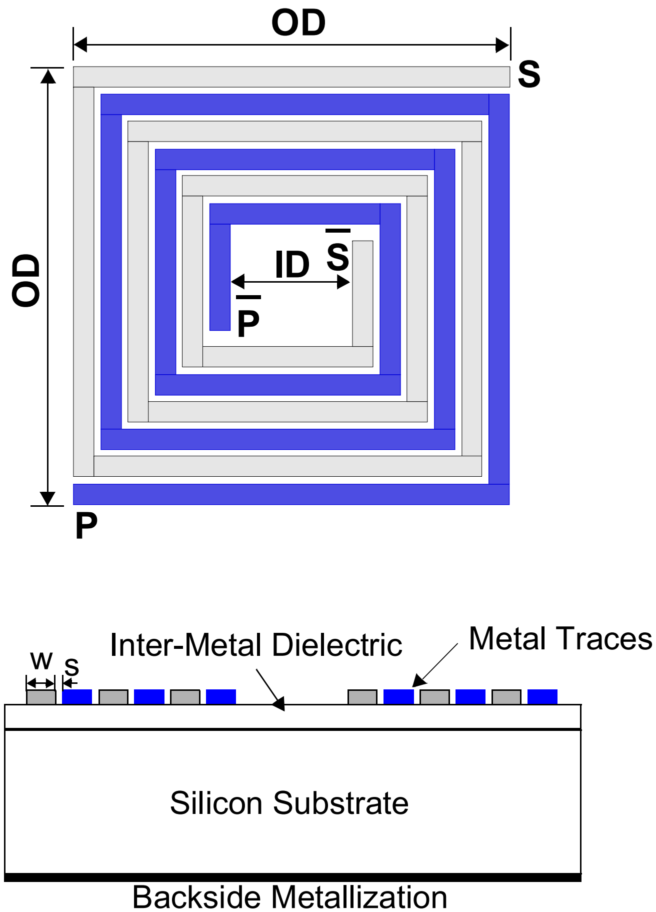


- Parasitic capacitance and substrate dissipation cannot be neglected at RF and mm-wave frequencies. Considering both capacitive and inductive couplings

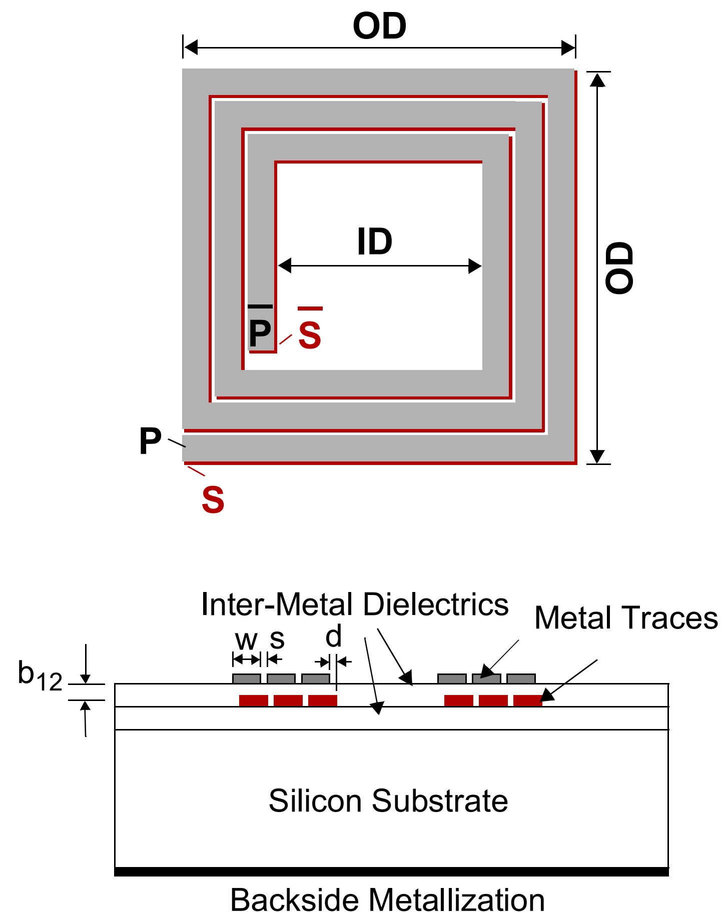
$$v_4 = \frac{Z_4}{Z_3 + Z_4}\left(Z_3 C_m \frac{dv_1}{dt} + L_m \frac{di_1}{dt}\right), \text{ and}$$

$$v_4 = L_m \frac{di_1}{dt} \text{ for } Z_3 = 0 \text{ (i.e., magnetic coupling dominant).}$$

Monolithic Transformer Layouts



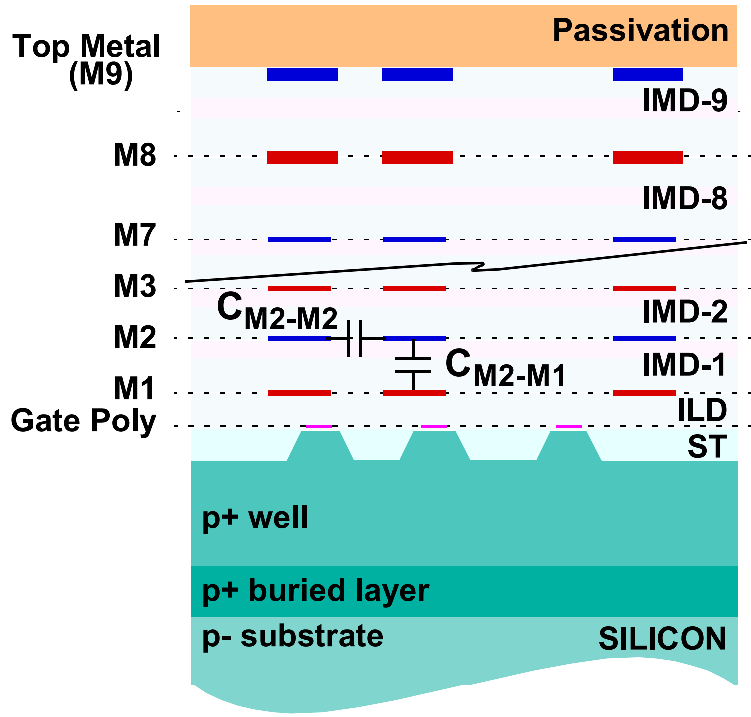
Interleaved (Frlan) winding



Stacked (Finlay) winding

Example Submicron CMOS Backend

Layer	Thickness, in μm
M9	0.9
M8	0.9
M7	0.3
M6	0.3
M5	0.3
M4	0.3
M3	0.3
M2	0.3
M1	0.2



Layer	Thickness, in μm	Effective Permittivity
Passivation	1.8	5.75
IMD-9	1.6	4.3
IMD-8	1.6	4.3
IMD-2 to 7	0.6	3.0
IMD-1	0.25	3.3
ILD	0.45	4.2
ST	0.35	3.9
Silicon	350	11.7

- Example layers for a typical backend metal interconnect stack in deep submicron CMOS technology.

Cross-Coupled (Differential) LC-VCO

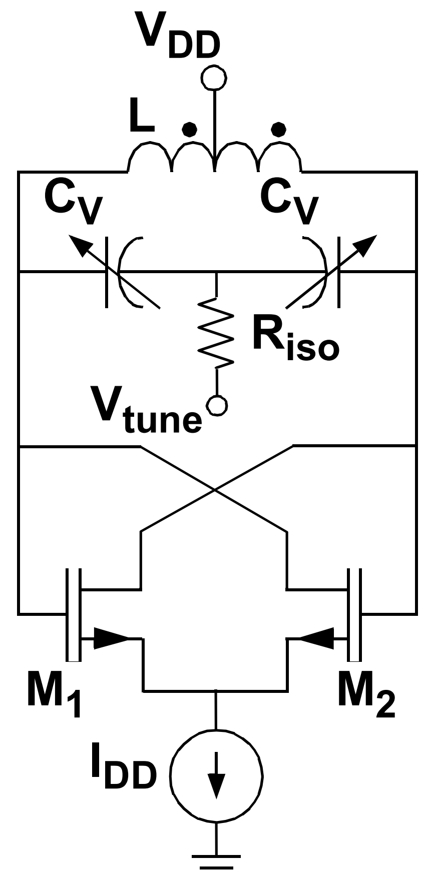
- Assuming a square-wave current driving the tank, phase noise in the $1/f^2$ regime can be written as [13]

$$L_{DP}(\omega_d) = 10\log\left[\frac{kT(1+\gamma_n)}{R_T[(4/\pi)I_{DD}Q_T(\omega_d/\omega_o)]^2}\right],$$

where:

Q_T = tank Q
R_T = tank resistance at resonance, ω_o
γ_n = NMOS excess noise parameter
I_{DD} = bias current

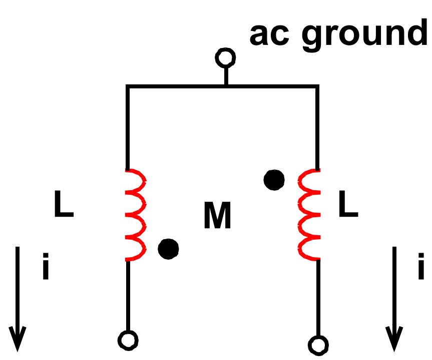
Amplitude of square-wave tank current is $A_s \approx (2/\pi)R_T I_{DD}$. Increasing Q_T reduces phase noise, but output swing also depends upon tank resistance at ω_o and bias current.



- Assuming: f_o=2GHz, Q_T=15 (L=5nH), γ_n=2, L_{DP}(20MHz)=-165dBc/Hz, I_{DD}=6.8mA is required. Need to add margin for current source (i.e., noise, r_{out}), PVT, etc.

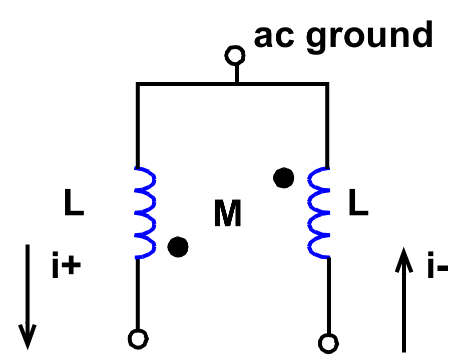
k-Factor and Common-Mode Rejection

$L_{to\ ground} = L(1 - k_m)$



Common-Mode Drive

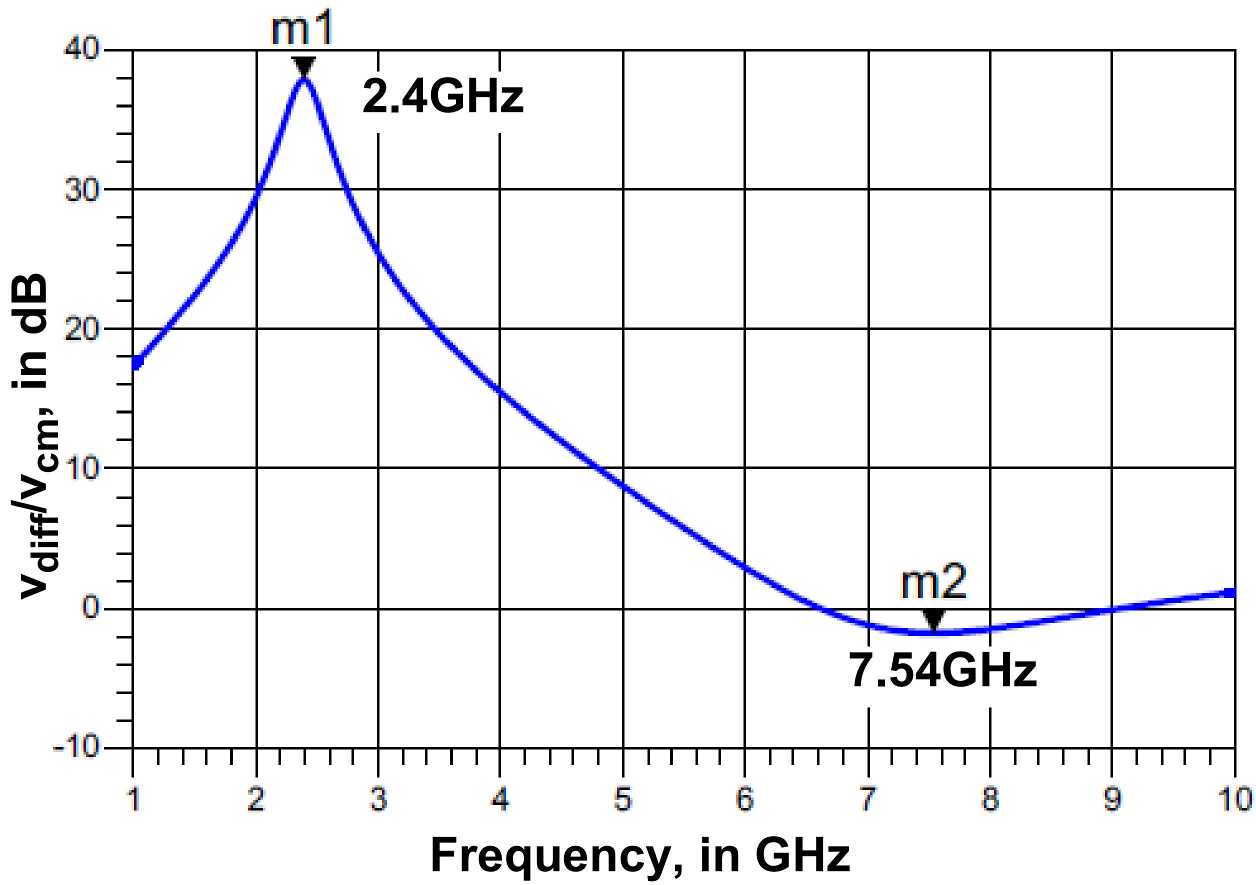
$L_{diff} = 2L(1 + k_m)$

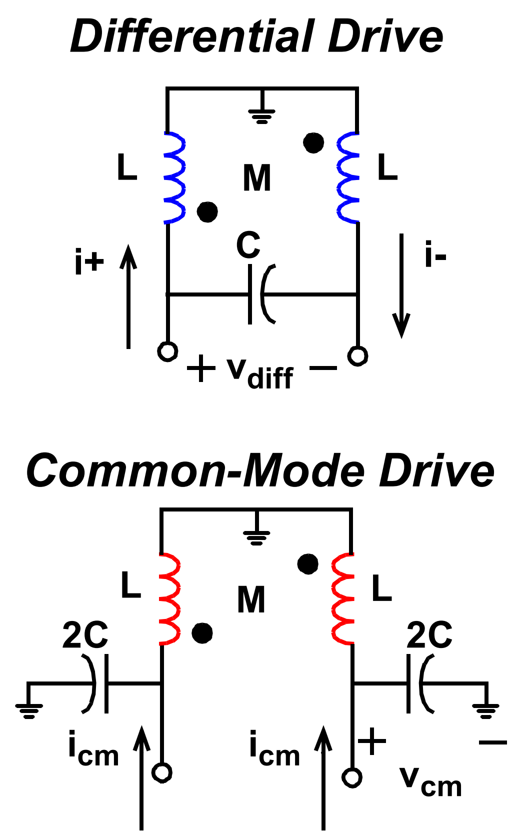


Differential Drive

- Total inductance between terminals is 2x larger when driven differentially (i.e., 4L for k_m=1) and smallest for a common-mode signal (i.e., 0 for k_m=1).
- Common-mode rejection improves when tuned to resonate in differential mode, as common-mode components are “off-resonance” and shorted to ac ground.
- Substrate coupling to and from a symmetric inductor is reduced compared to 2 asymmetric inductor loads due to net cancellation at a distance from the coil.

Common-Mode Rejection of an LC Tank



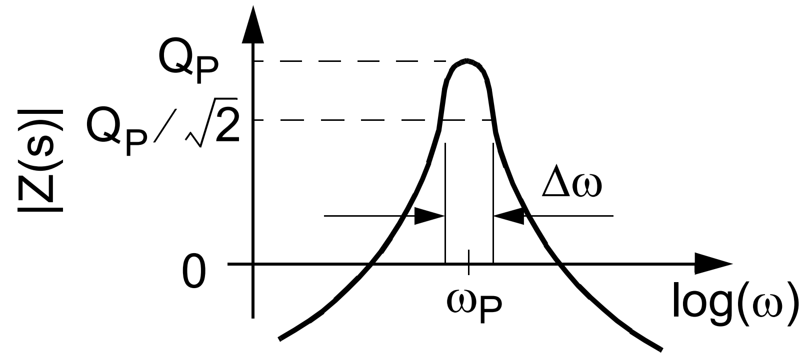


- In this example, a L=2nH inductor (k_m=0.8) resonant in the differential mode has a CMRR of 38dB at 2.4GHz. The common-mode resonant peak is pushed out to 7.54GHz as lower inductance is seen for common-mode drive.

Quality Factor

- For the normalized quadratic bandpass function, Z(s)

$$Z(s) = \frac{\omega_P s}{s^2 + \frac{\omega_P s}{Q_P} + \omega_P^2}$$



- Q_P relates bandwidth and peak frequency:

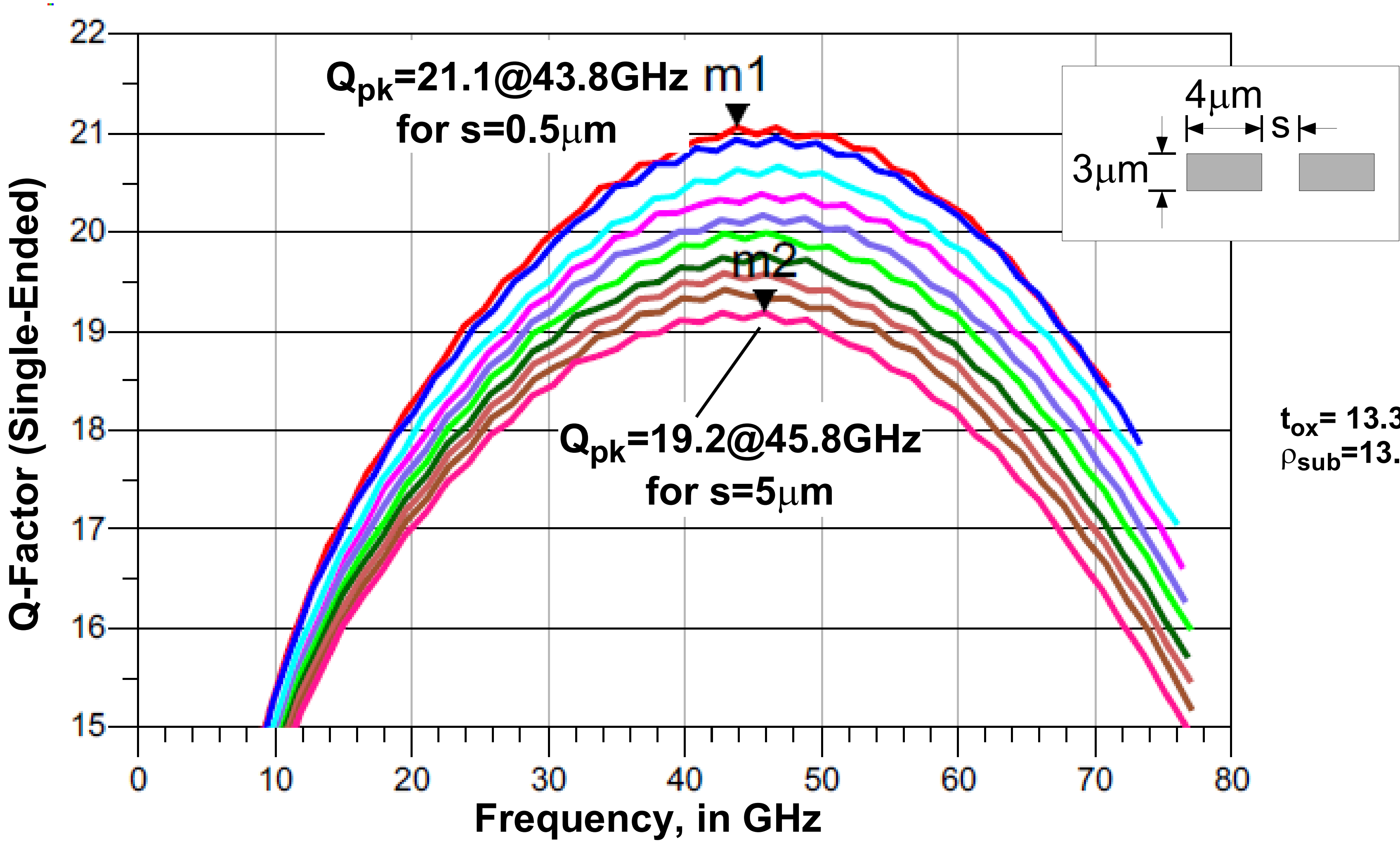
$$Q_P = \frac{\omega_P}{\Delta\omega} = \left.\frac{-\omega_P}{2}\frac{\partial\phi}{\partial\omega}\right|_{\omega = \omega_P}.$$

- Another interpretation: [energy stored/energy dissipated] per cycle in the steady-state for sinusoidal excitation.

- Energy is dissipated as heat in the conductors and dielectric and is also radiated. For a resonator:

$$\frac{1}{Q_{Total}} = \frac{1}{Q_{Conductor}} + \frac{1}{Q_{Dielectric}} + \frac{1}{Q_{Radiation}} \approx \frac{r}{\omega l} + \frac{g}{\omega c}.$$

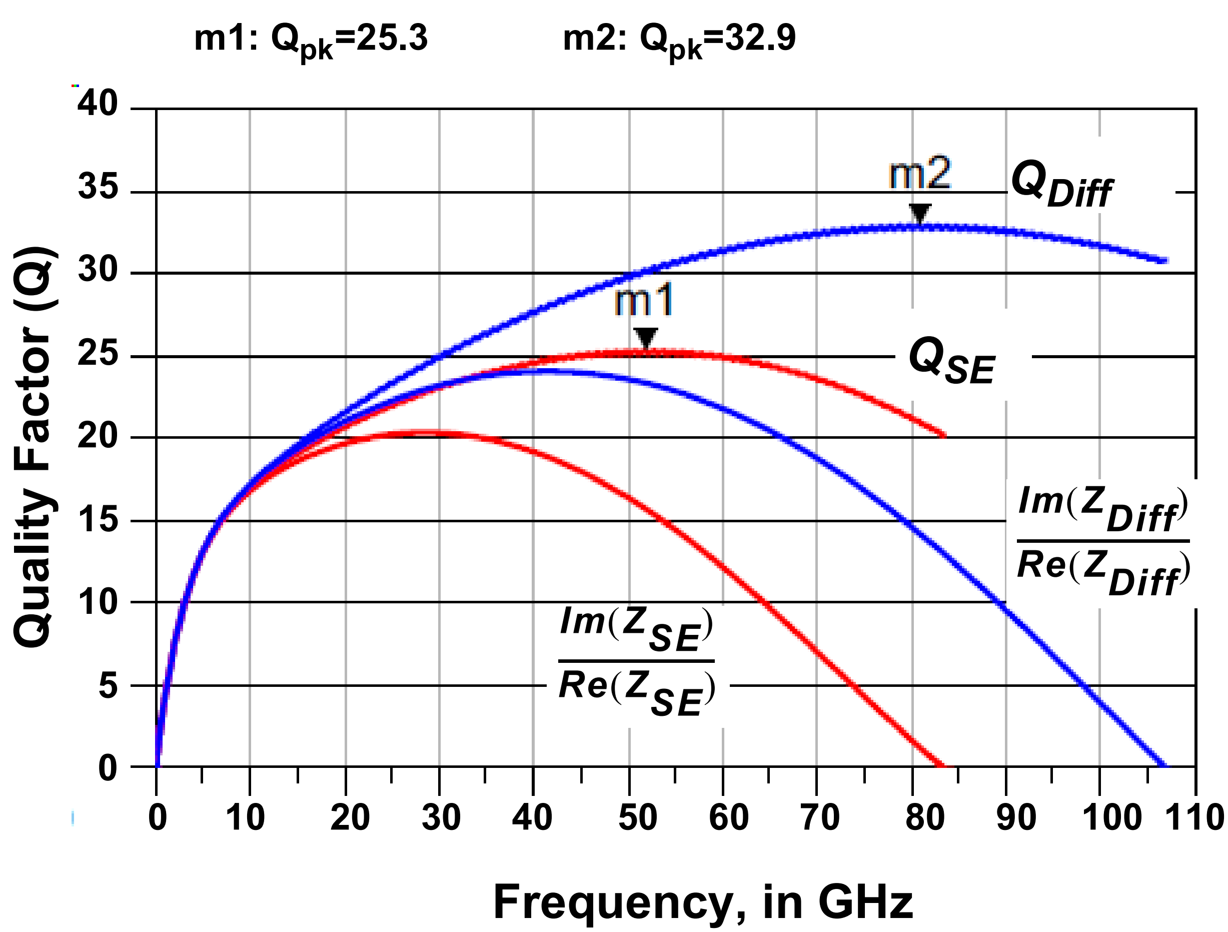
Q-Factor vs. Conductor Spacing

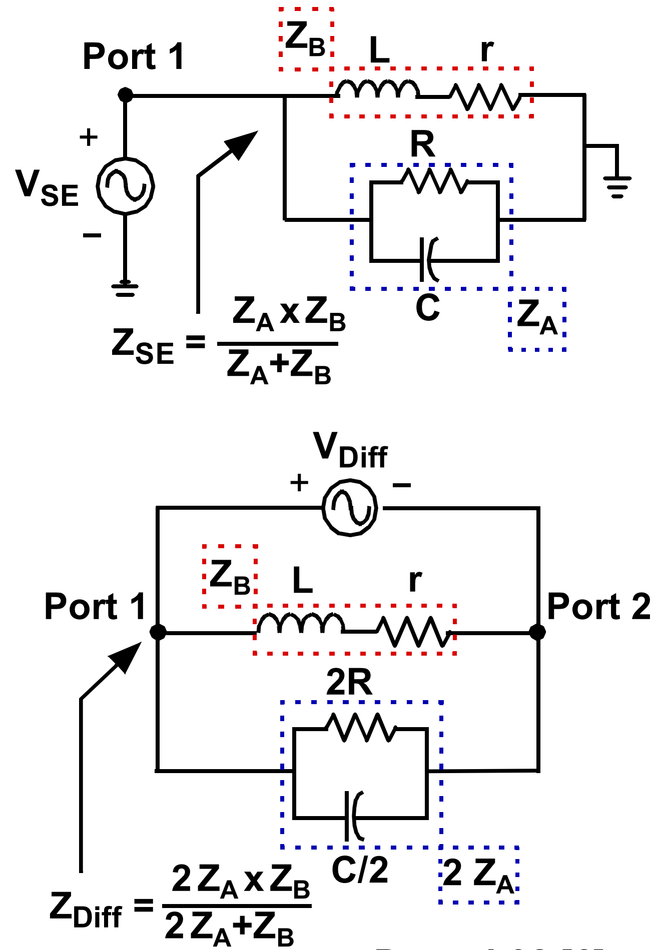


t_{ox}= 13.3μm
ρ_{sub}=13.5Ω-cm

- Single-ended Q for a 2-turn inductor with conductor spacing 0.5μm < s < 5.0μm.

Q-Factor for Differential Drive

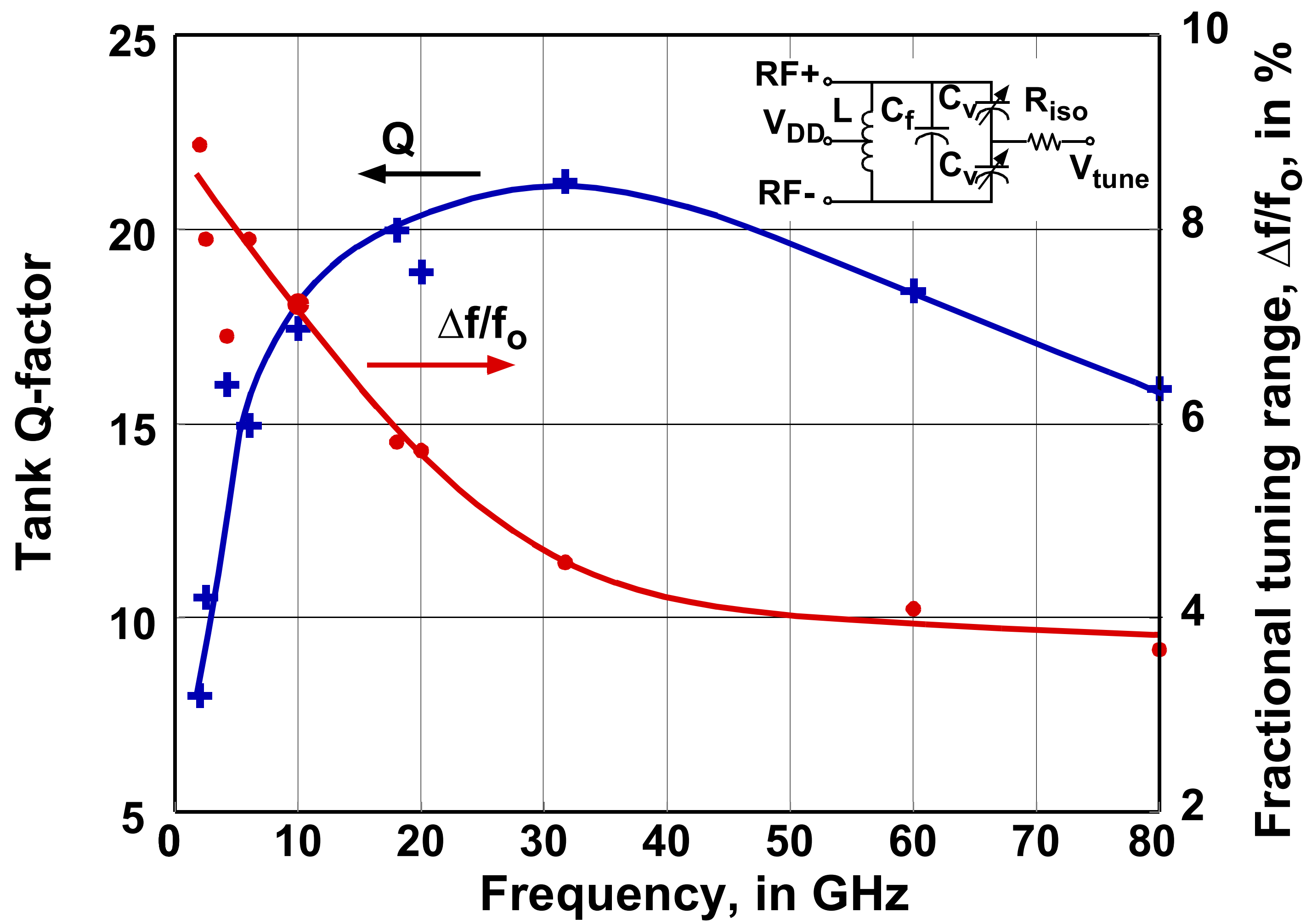




Danesh02 [6]

- Differential excitation gives higher Q-factor and a broader band across which the Q-factor is close to its peak.

Optimizing Tank Q-factor

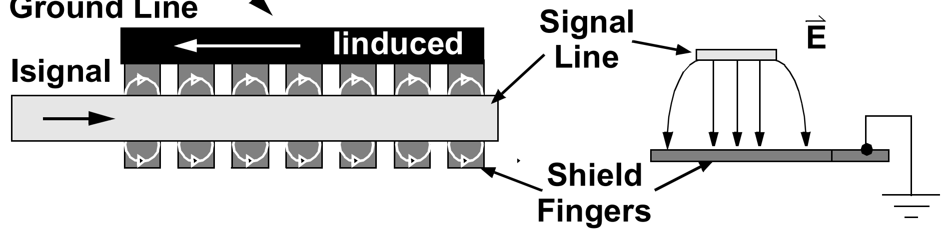


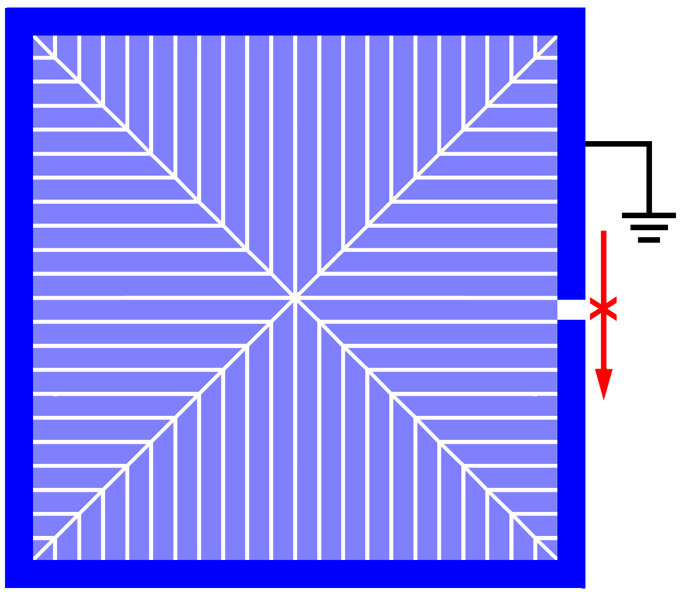
Long12 [10]

- Q-factor and fractional tuning range for monolithic resonators in 65nm CMOS from simulation (C_{fixed}=20fF).

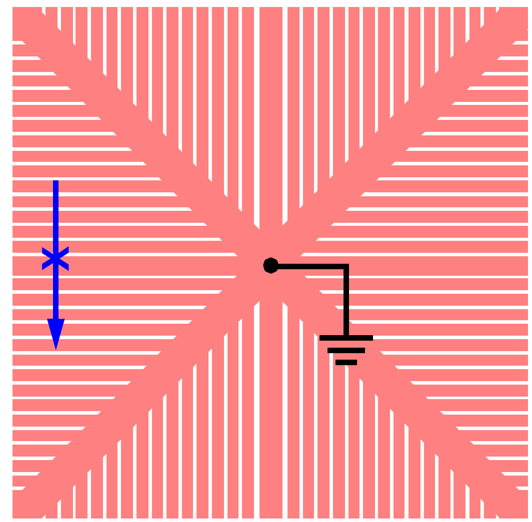
Patterned Ground Shields

Induced current in ground connection reduces inductance and Q-factor



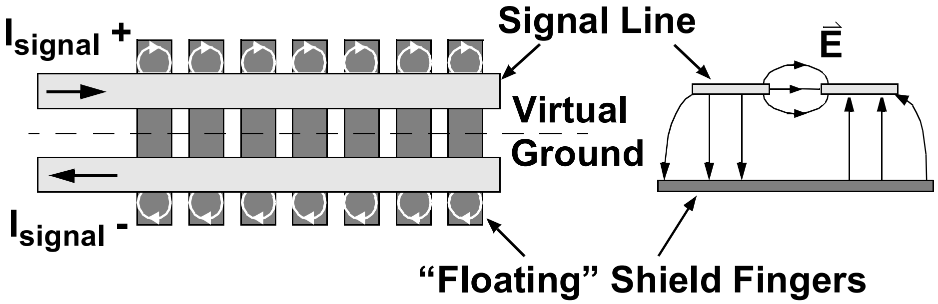


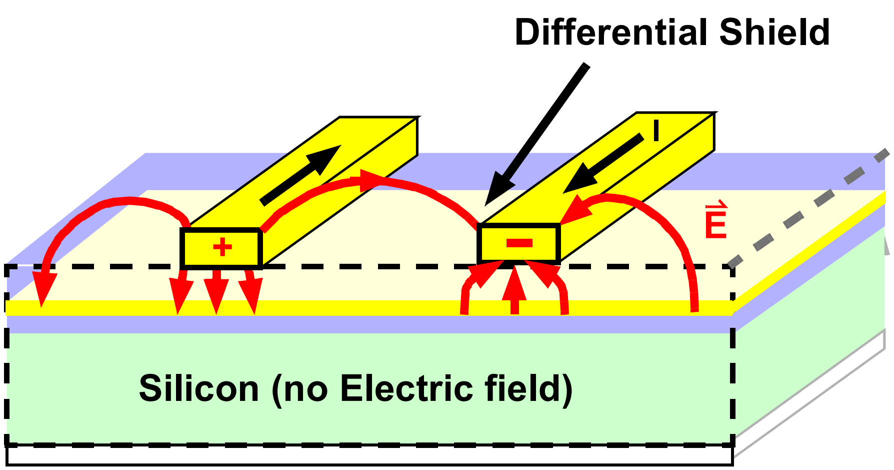
Ring Pattern Yue98 [7]



Star Pattern

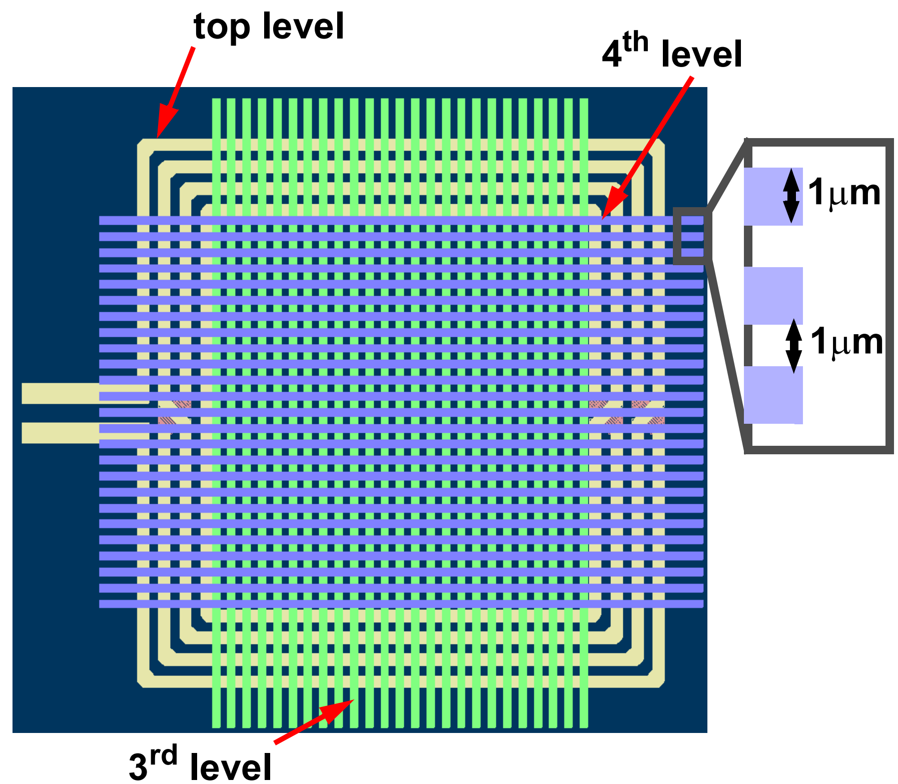
Differential Shielding





Shielded Balanced Tx Line

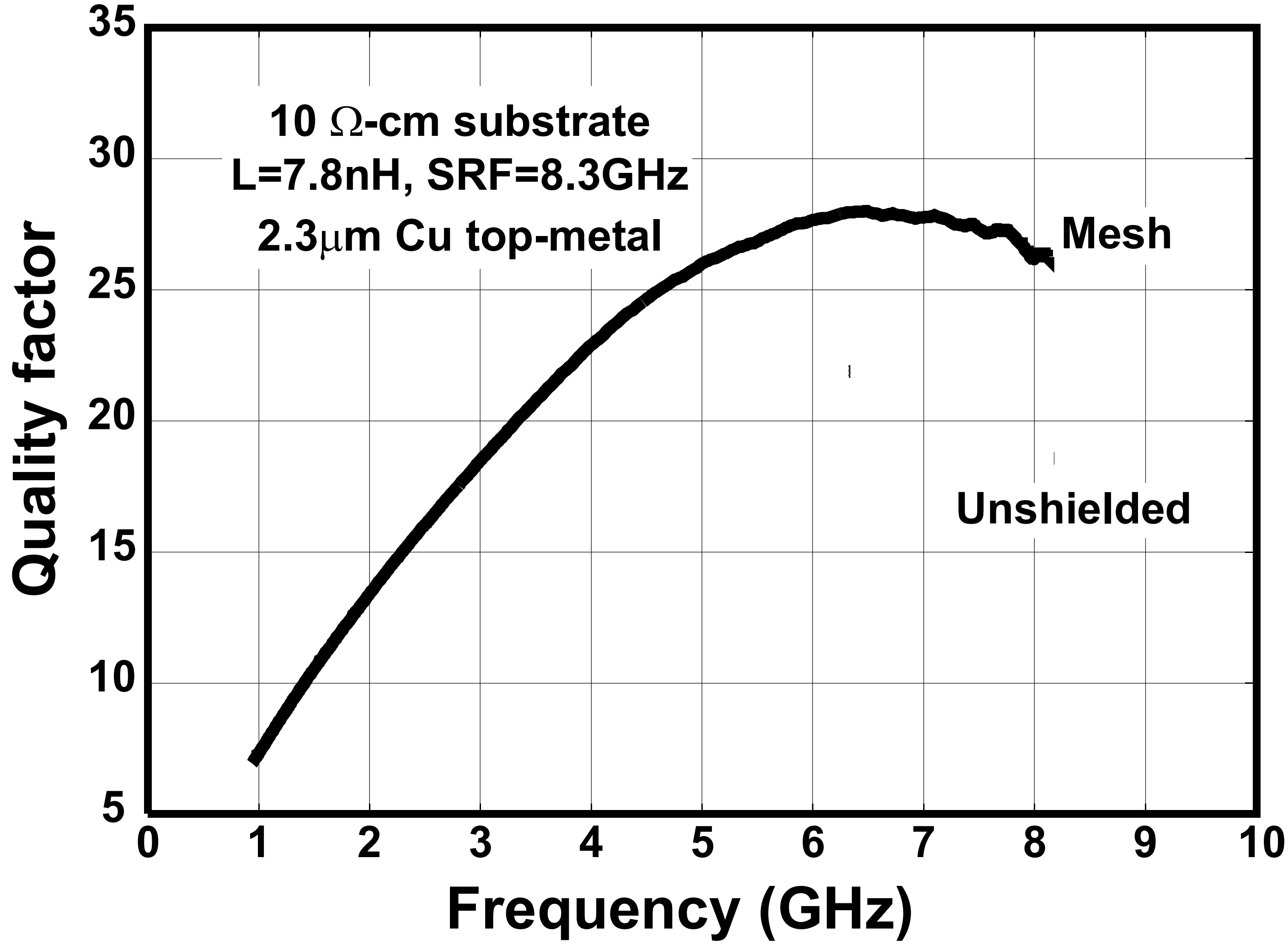
Cheung03 [8]



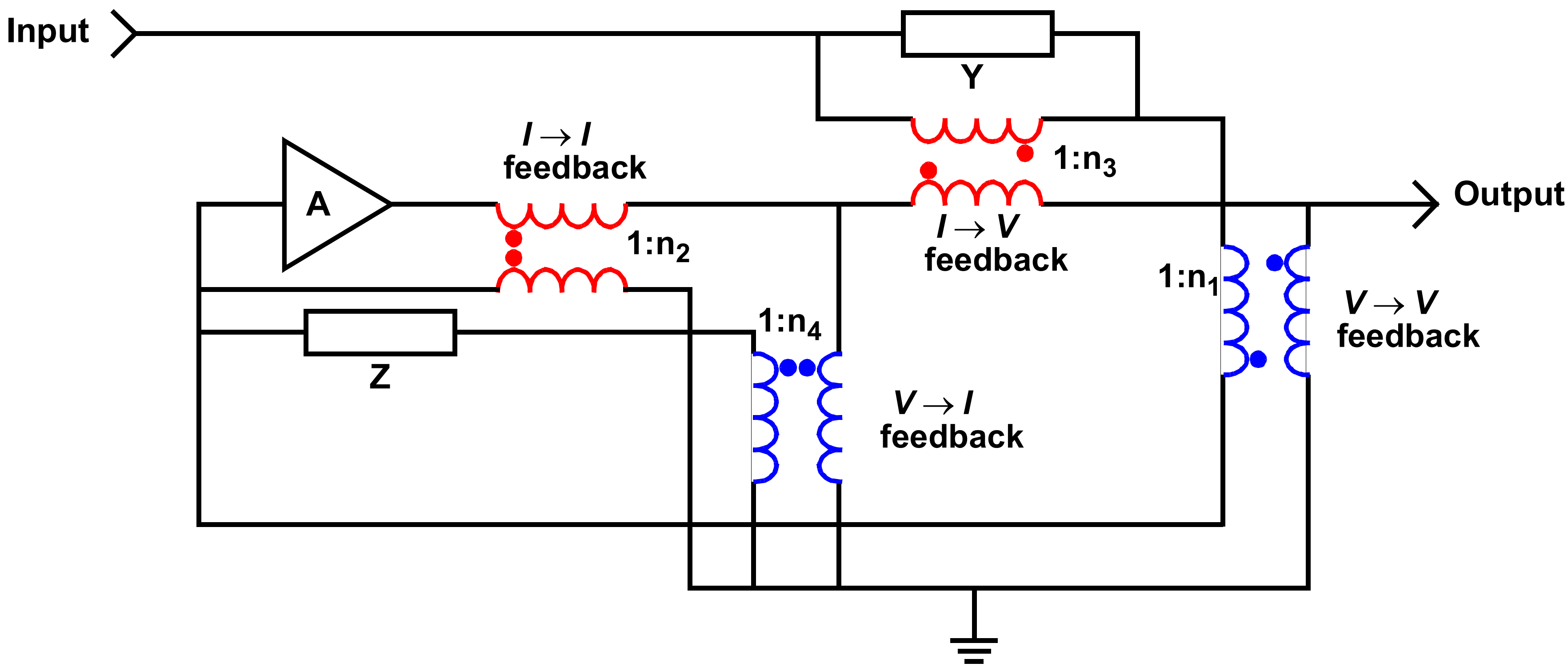
Shielded Symmetric Inductor

Cheung06 [9]

Differentially-Shielded Inductor



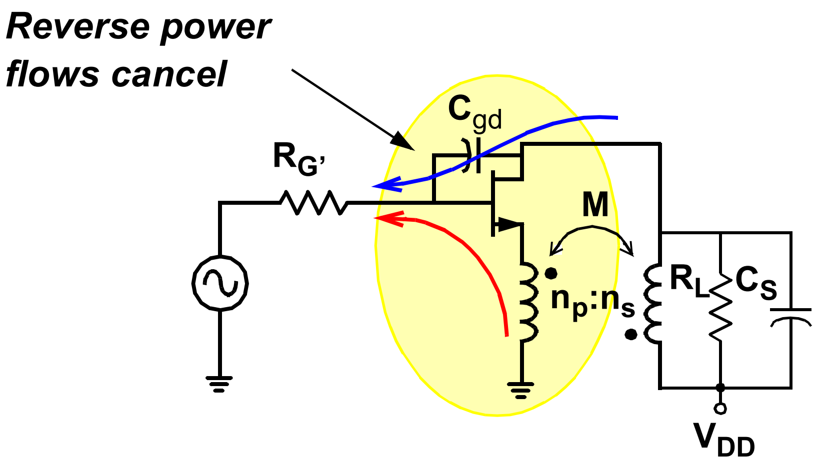
Transformers and RF Amplifiers



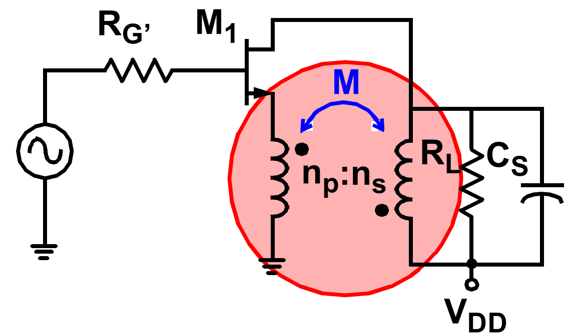
Dual-loop amplifier with 4 feedback loops

- Bandwidth of transformers with floating terminals (i.e., one terminal not at AC ground) is compromised by parasitics. V-V feedback is least affected by substrate parasitics (one terminal on each winding is grounded).

Transformer Neutralization



- greater isolation simplifies matching and increases gain



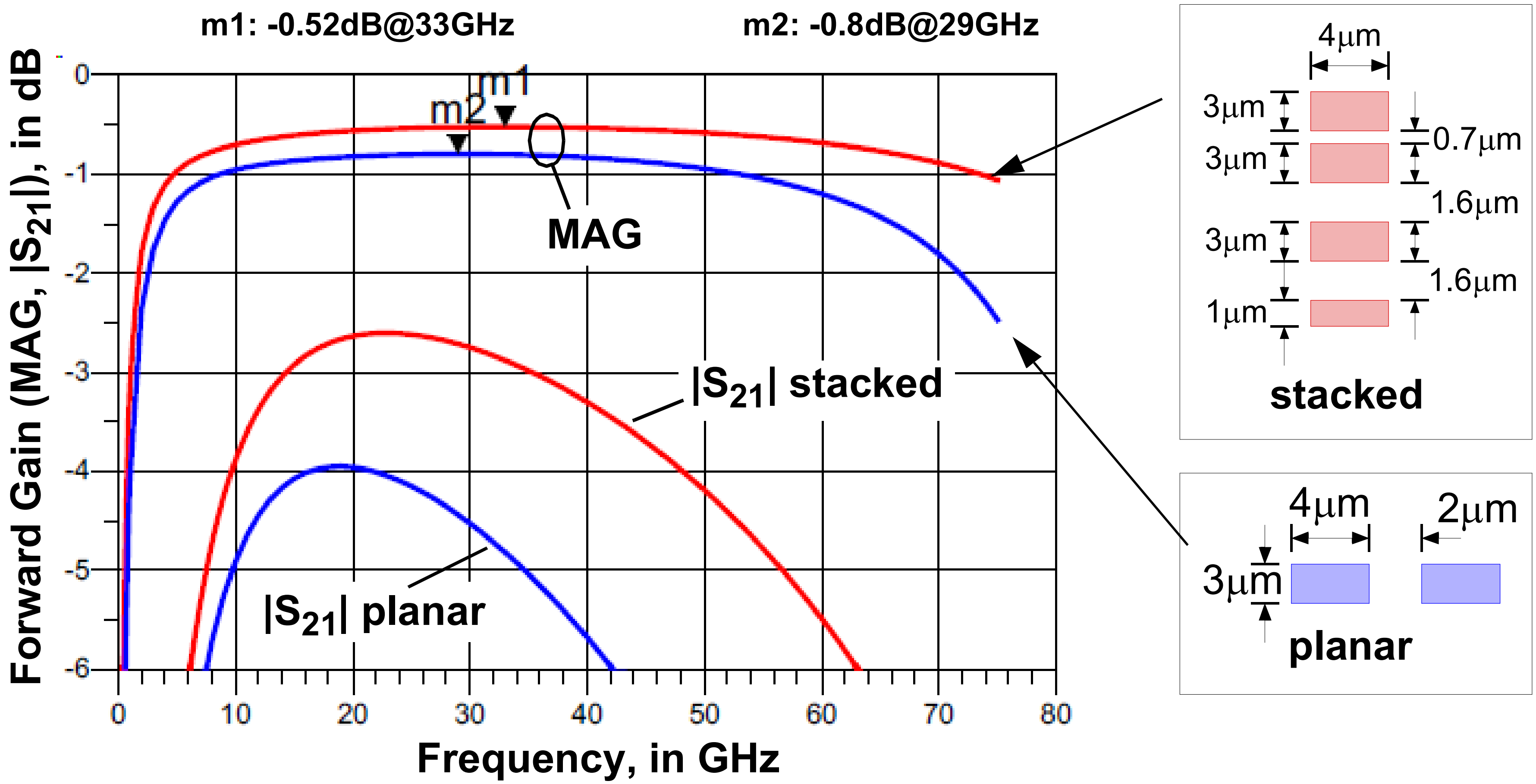
- noiseless feedback stabilizes gain, reduces output impedance

- Neutralizing feedback increases gain and reverse isolation, promotes stability, and raises input and output impedances.

- Neutralization via a step-down transformer cancels signal flow through C_{gd},

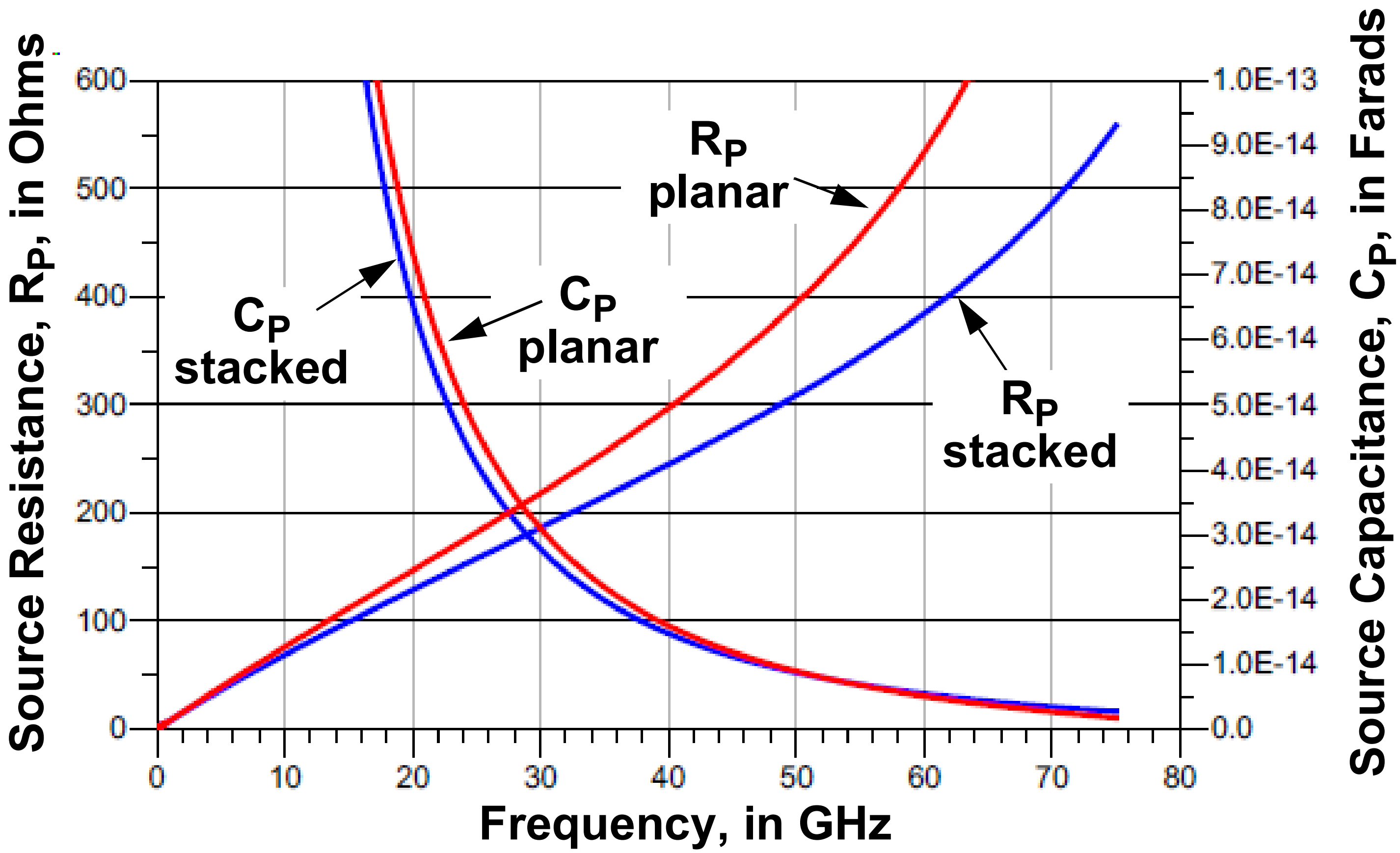
$$\frac{C_{gs}}{C_{gd}} \approx \frac{n}{k} \Rightarrow \text{Neutralization condition .}$$

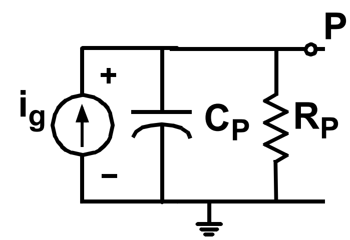
1:1 Transformer MAG



- Maximum available gain (MAG) is realized for conjugate match at source and load ports at each frequency. Untuned (i.e., S_{21}) gain for 50Ω source/load is 2-3 dB lower than MAG. Note that tuning further reduces bandwidth.

1:1 Tuning Impedances for MAG

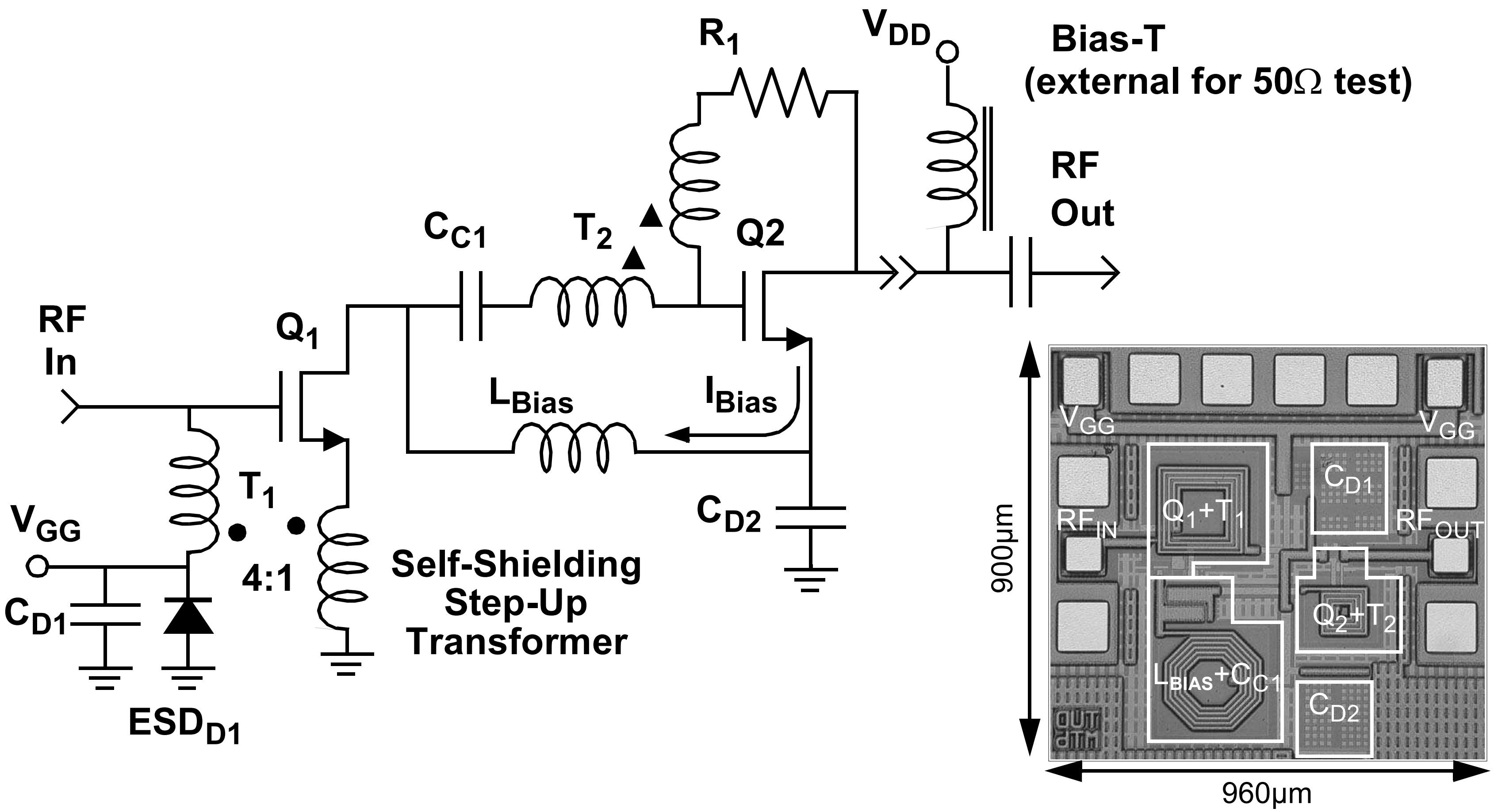




generator model

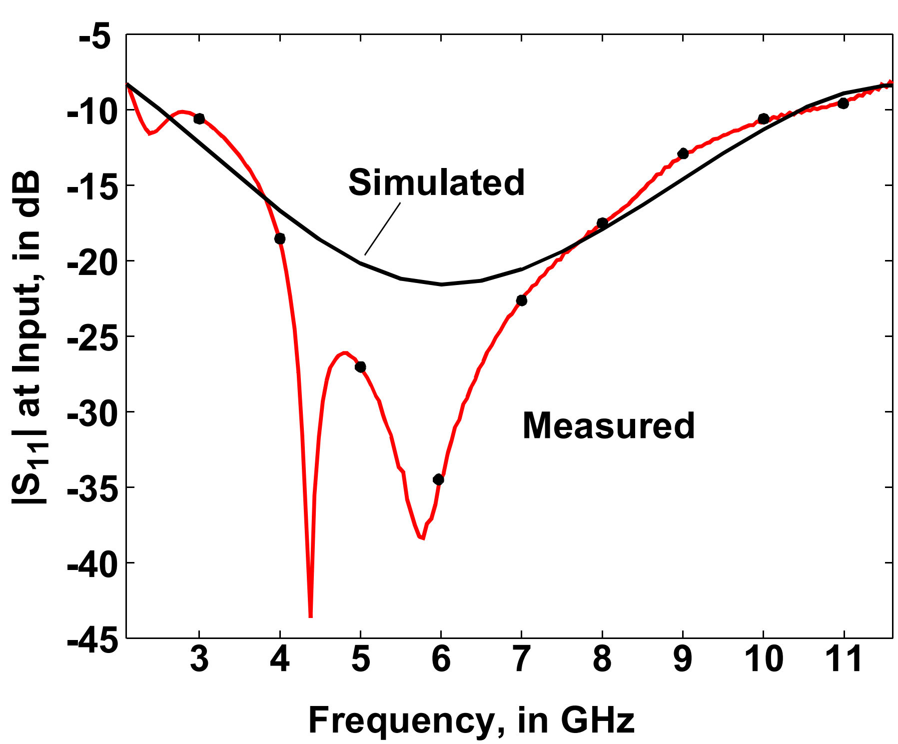
- Source impedances (parallel R-C equivalent, R_P/C_P) required to realize MAG vs. frequency are plotted above (load and source impedances are identical for a 1:1). Circuit loading at terminals must be included in R_P and C_P.

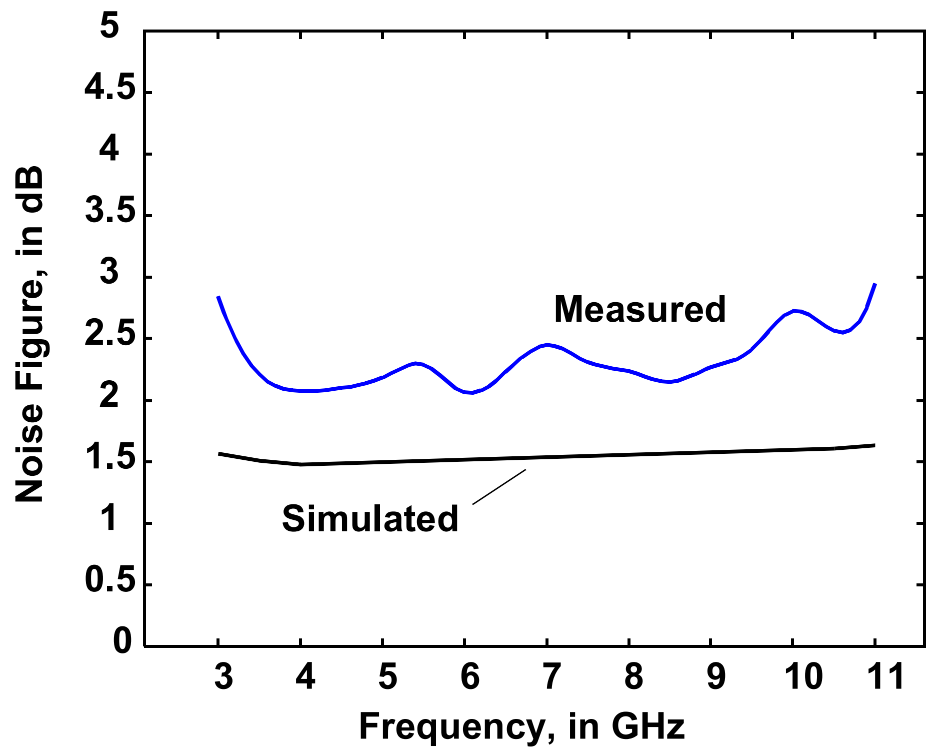
Wideband Feedback Amplifier



- 2-stages: series/shunt feedback via self-shielding transformer sets input impedance; transimpedance second stage lowers output impedance.

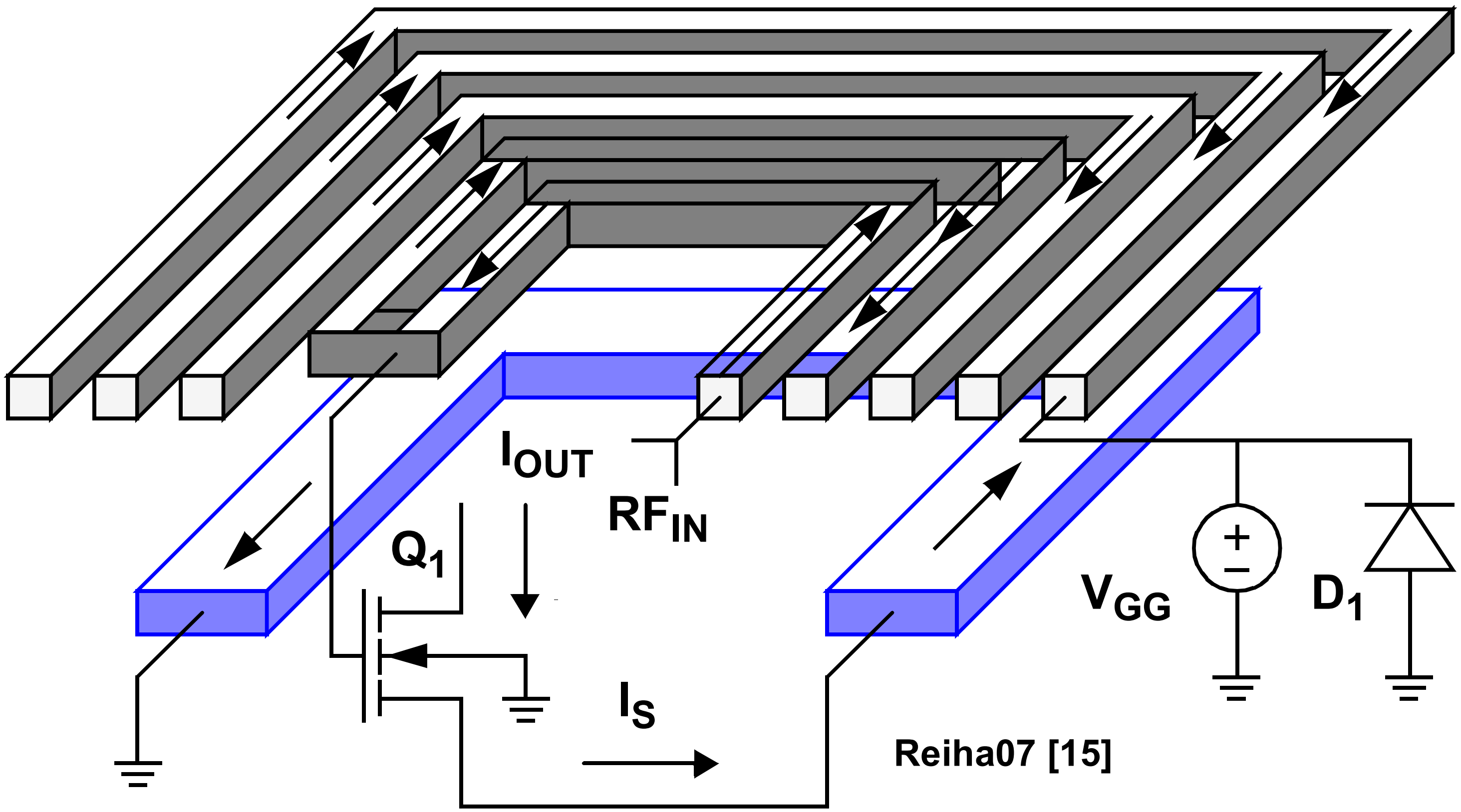
WB-LNA Input Impedance and NF





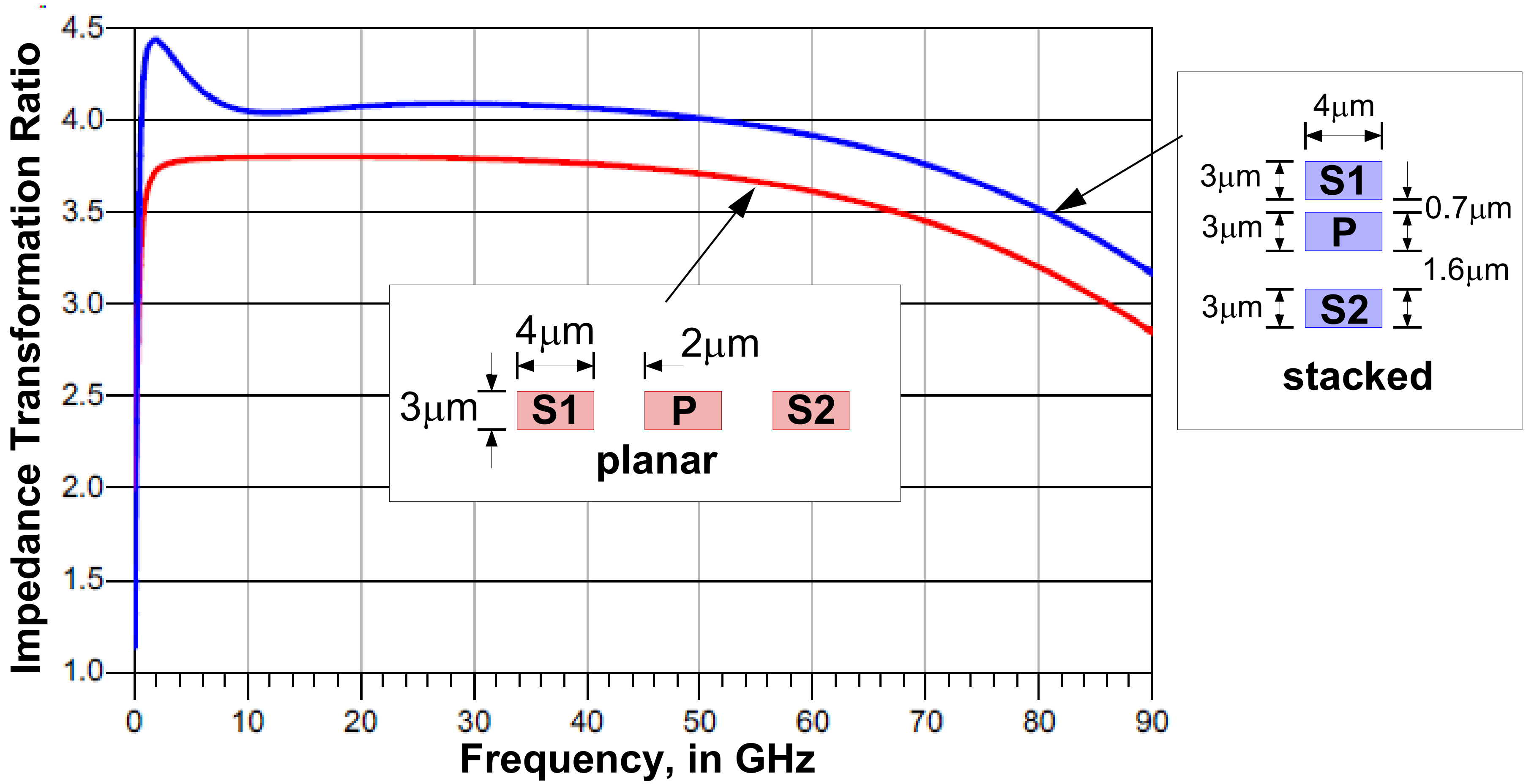
- Broadband gain of approx 15dB while drawing 7.5mA from 1.2V (0.13um CMOS). Noise figure < 2.5dB and relatively flat across > 7GHz. Excellent input match across band (S_{11} < -15dB).

Step-Up Transformer Cutaway



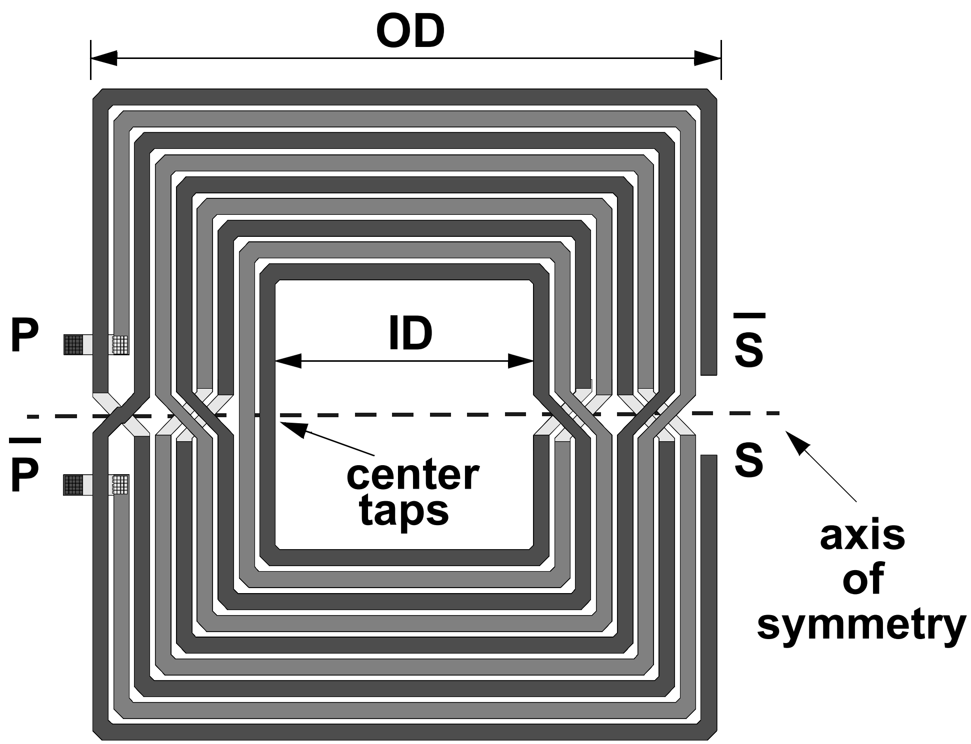
- Turns ratio is determined by the number of turns on each winding and k-factor.
- Stacked layout using separate wiring planes for primary and secondary simplifies implementation and saves chip area.

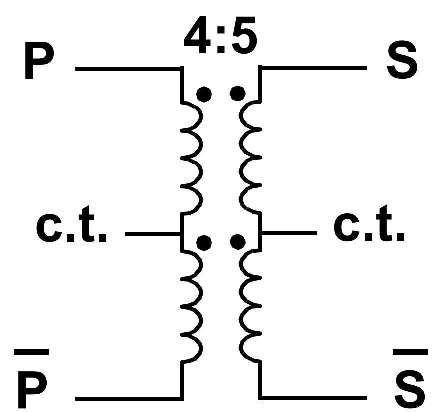
1:2 Step-Up Transformer



- Impedance transformation ratio is 4x for a 1:2 transformer (ideally). Weaker coupling (lower k_m) for the planar transformer results in an error (n^2=3.75 vs. 4). Tighter coupling and lower substrate parasitics are advantages of the stacked layout.

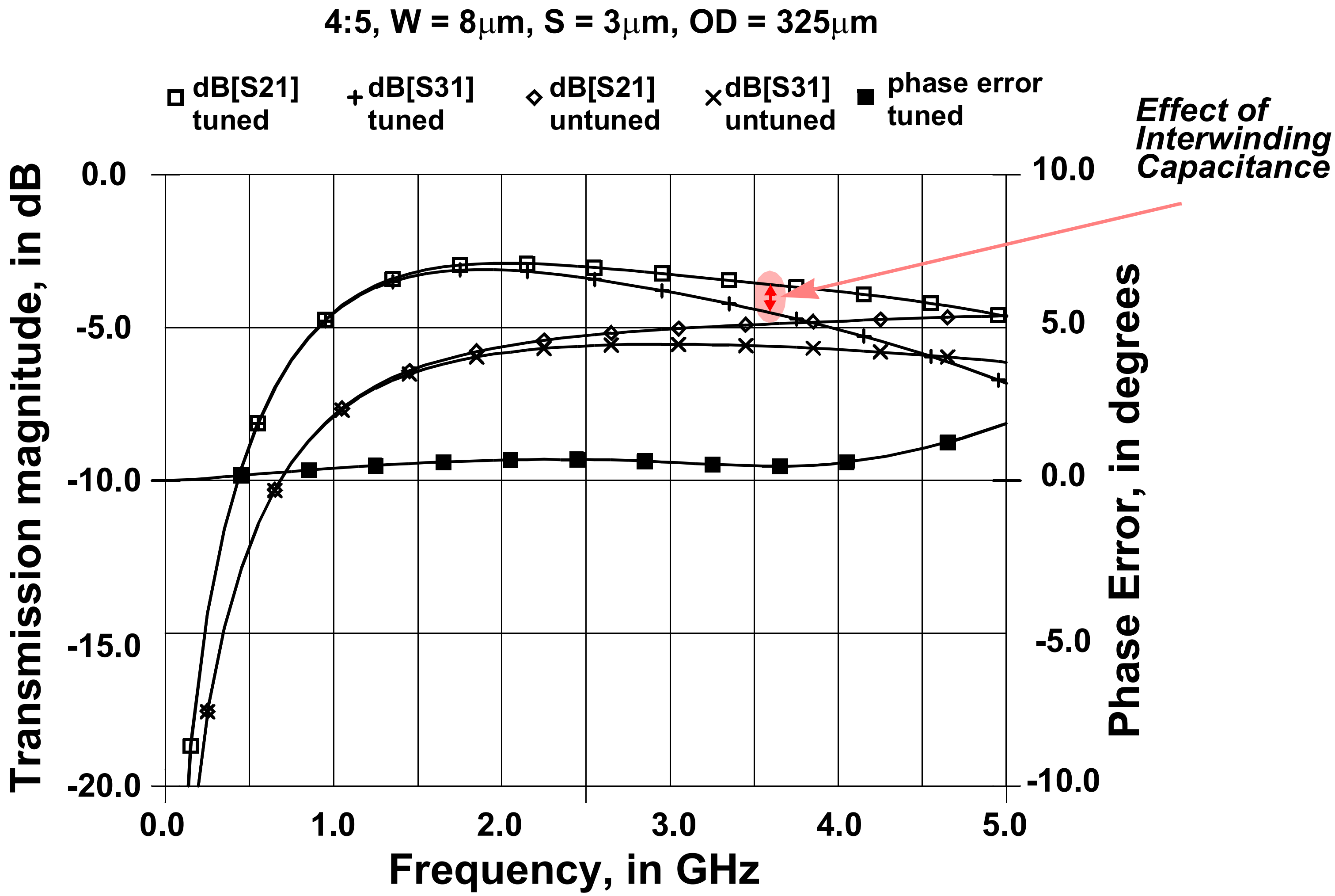
Transformer Balun





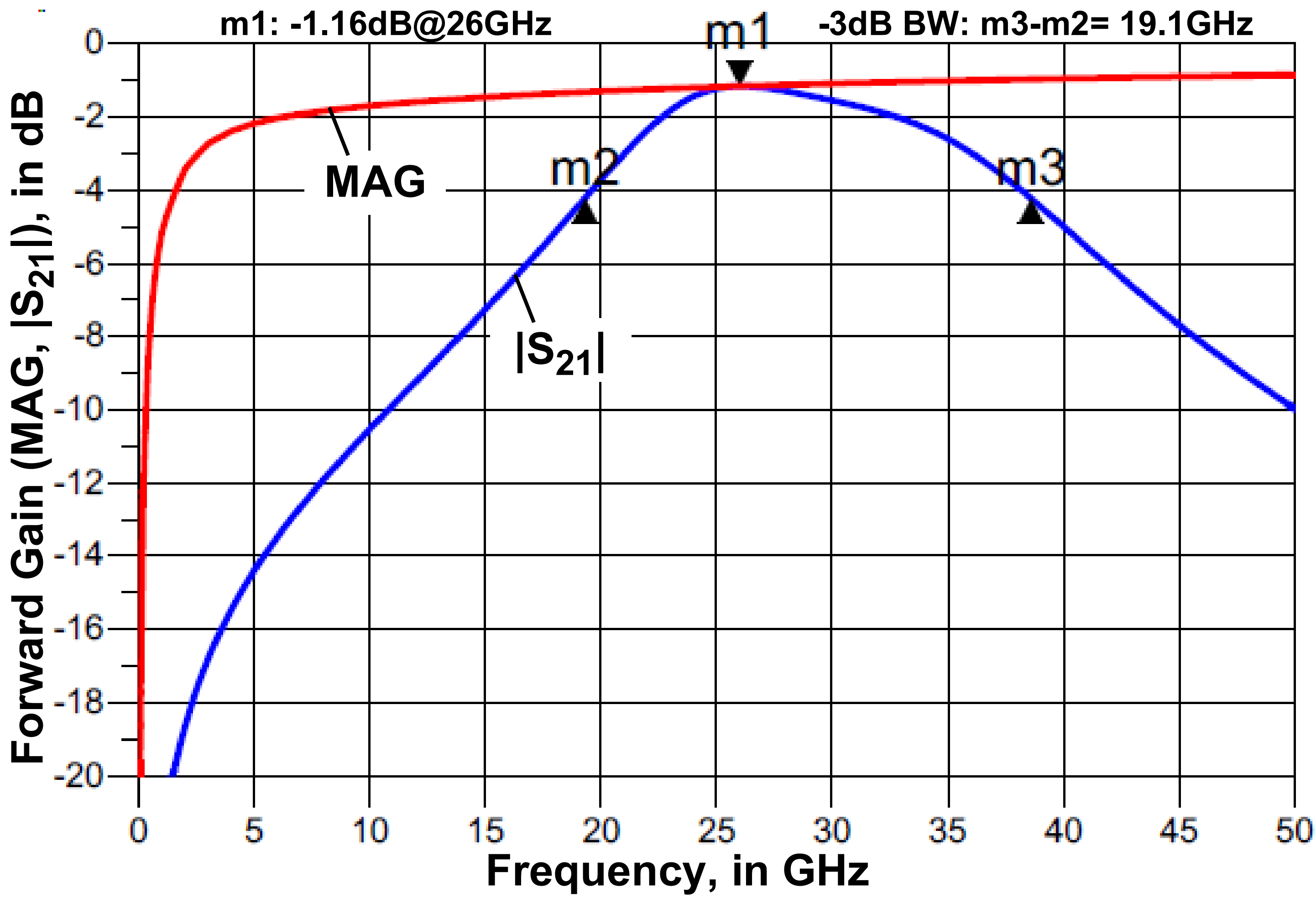
Square symmetric 4:5 (Rabjohn) transformer

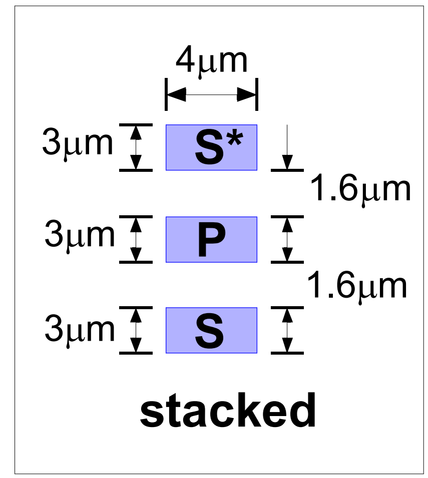
Balun Response



- Output magnitude and phase errors disappear when driven differentially.

mm-Wave Balun

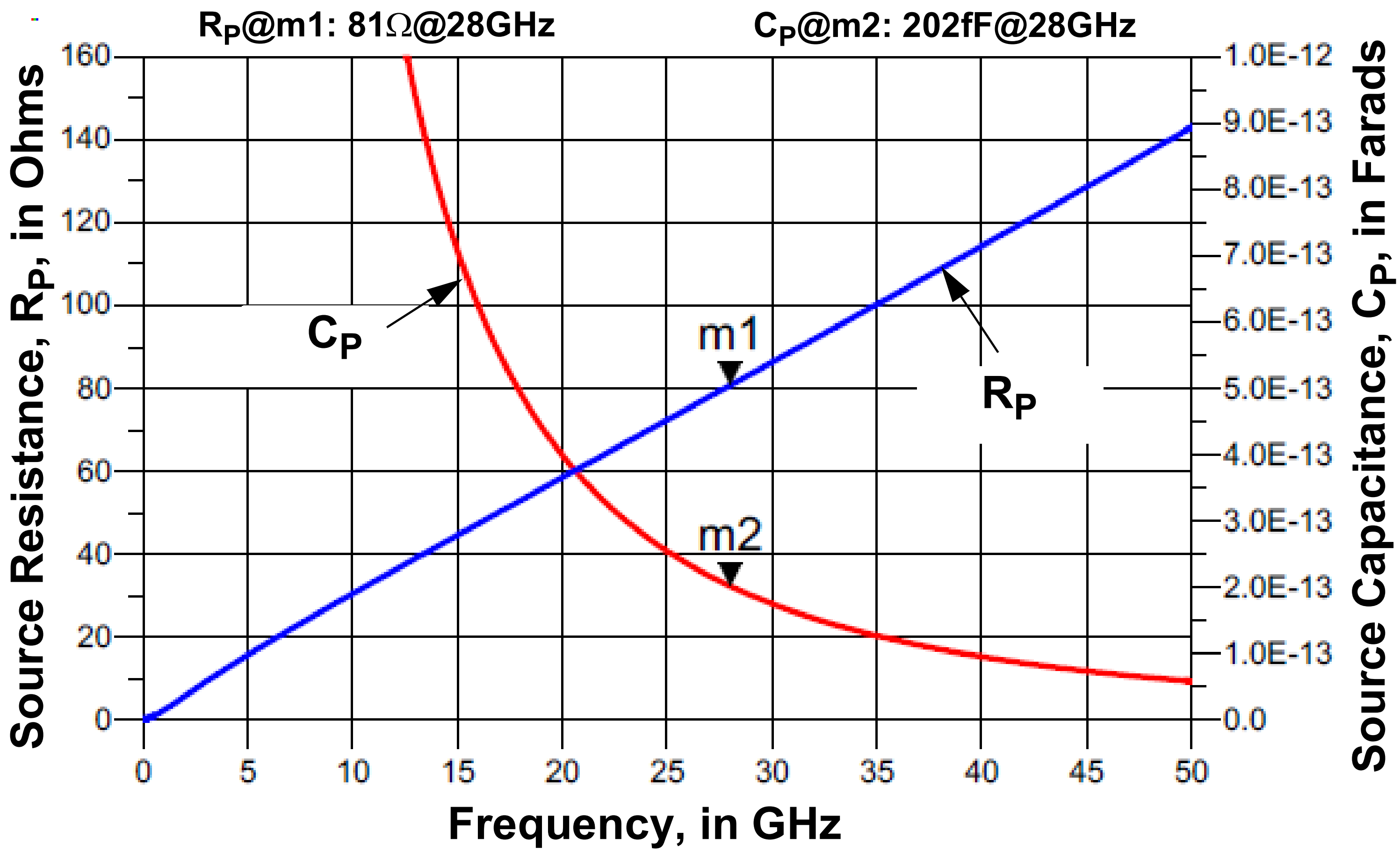


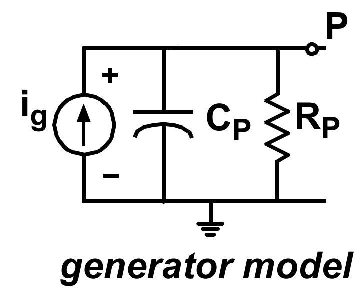


ρ_{sub}=13.5Ω-cm
Lp=0.2nH

- MAG and $|S_{21}|$ for a 3-conductor balun after conjugate match (i.e., $v_{o\text{-}diff}/v_{in}$). A fully-planar layout has ~0.5dB more attenuation in-band, and 2.4GHz less bandwidth.

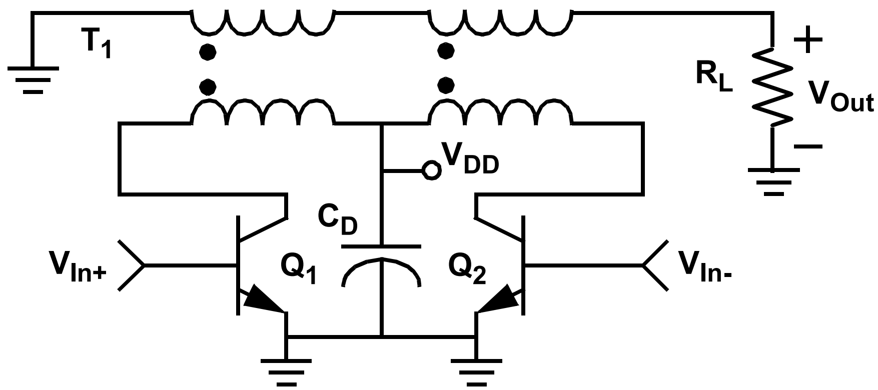
Optimal Source Impedance



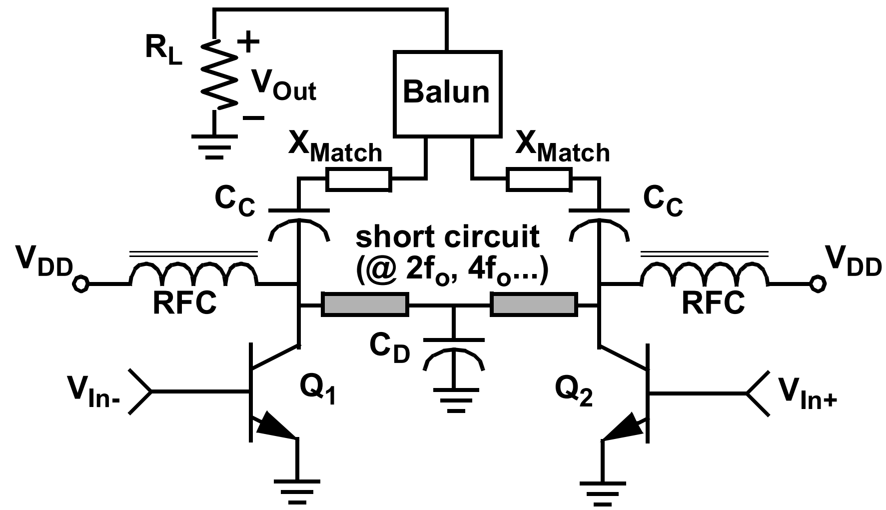


- Optimal source impedance decreases with decreasing frequency and magnetizing inductance. Tuning cap must be large enough to absorb circuit parasitics; can tune on primary, or secondary side (or both).

Push-Pull Amplifier



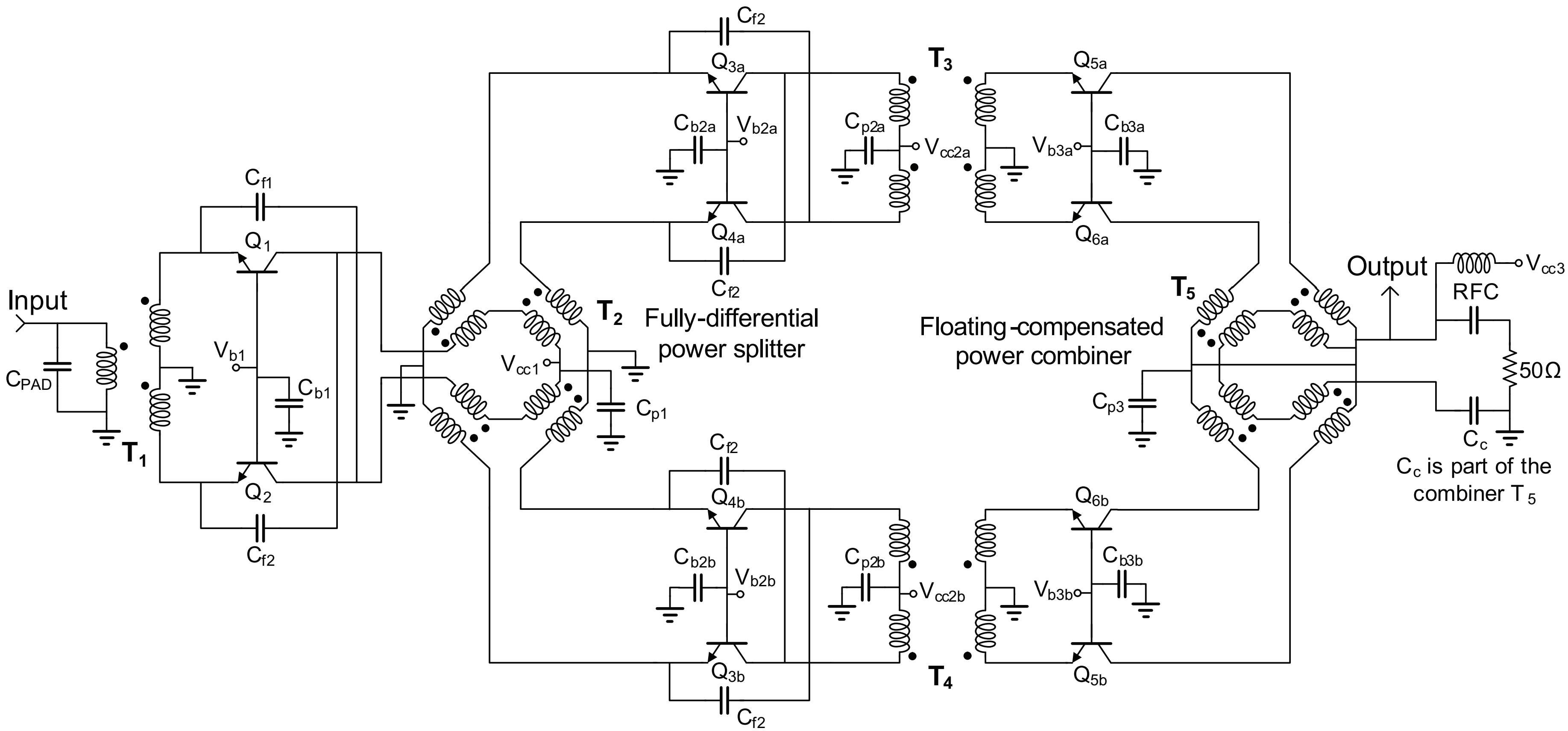
Wideband



2 Single-Ended Stages

- Push-pull topology shorts even harmonics via symmetry using a transformer balun. Drain sees resistive load at fundamental and all odd-order harmonics.
- Coupling 2 single-ended amplifiers requires harmonic terminations (e.g., short-circuit at $2f_o$, $4f_o$, etc.) at each output and separate bias paths.
- Parasitics such as supply and ground path inductances have less effect on performance for push-pull and balanced amplifiers.

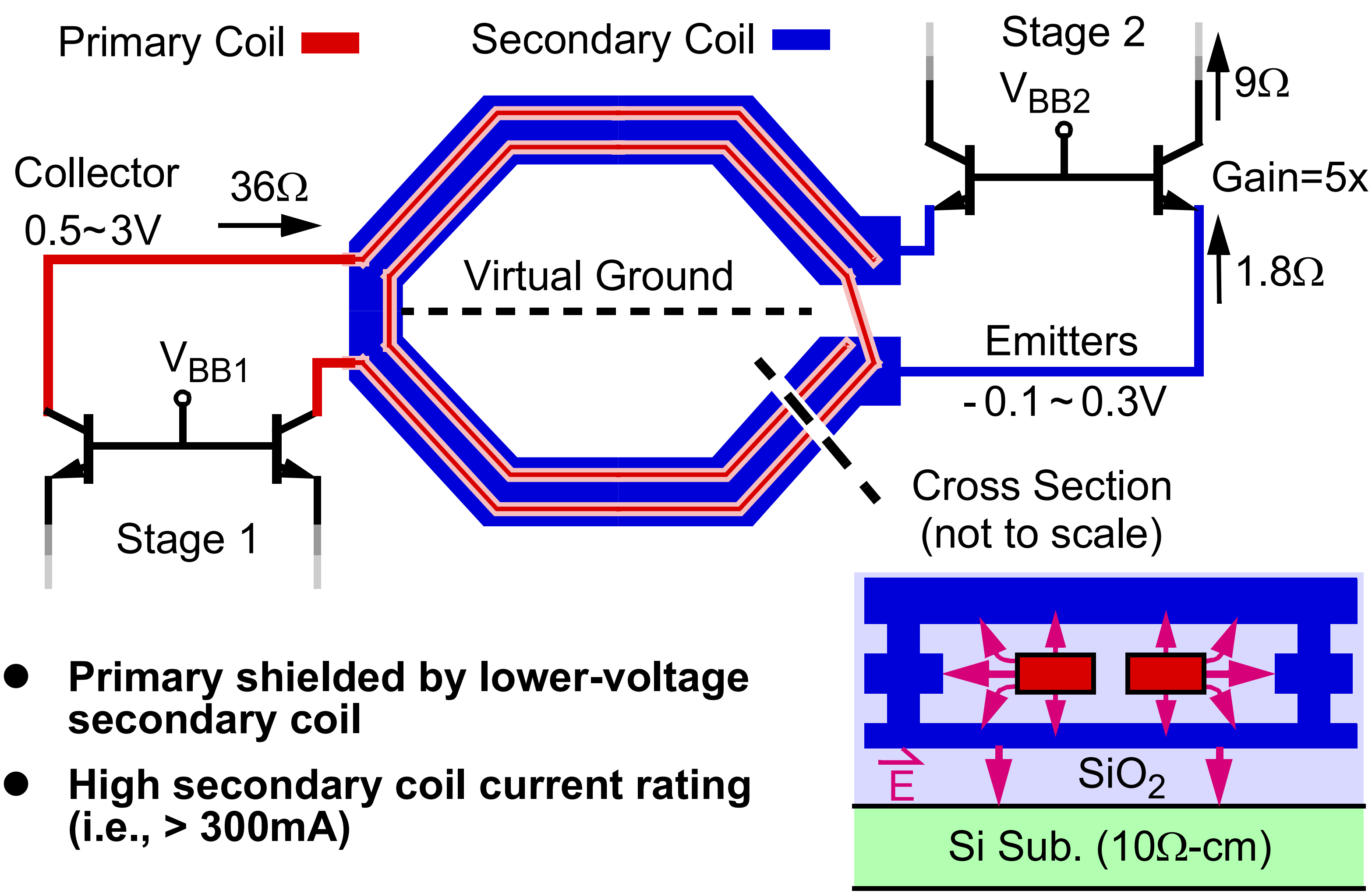
Multi-Path mm-Wave Power Amplifier



- Multi-path amplifier increases power output using passive power splitting (into 2 paths) and power combining of multiple PA stages.

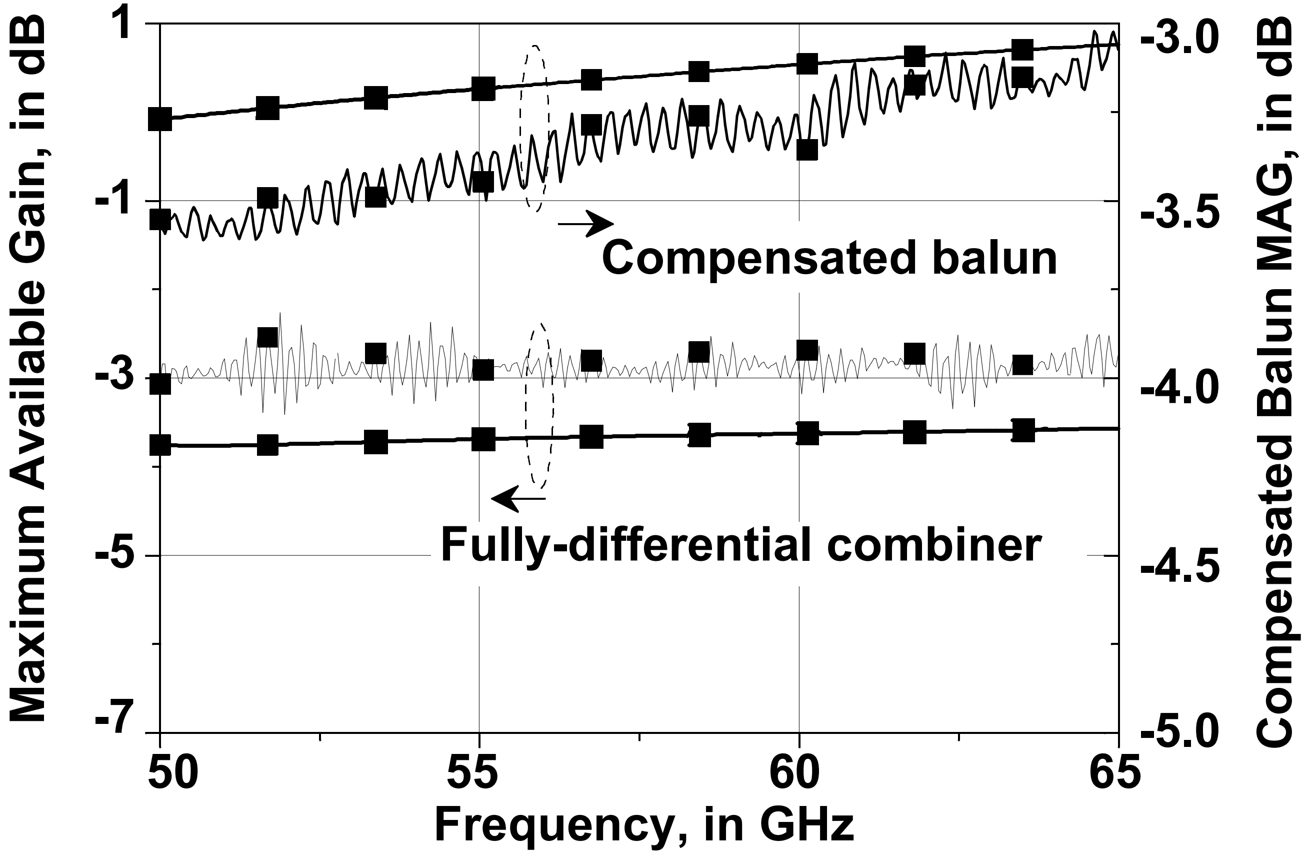
- Interstage gain realized using current-mode step-up transformers and impedance mismatch between active stages.

Self-Shielding Transformers



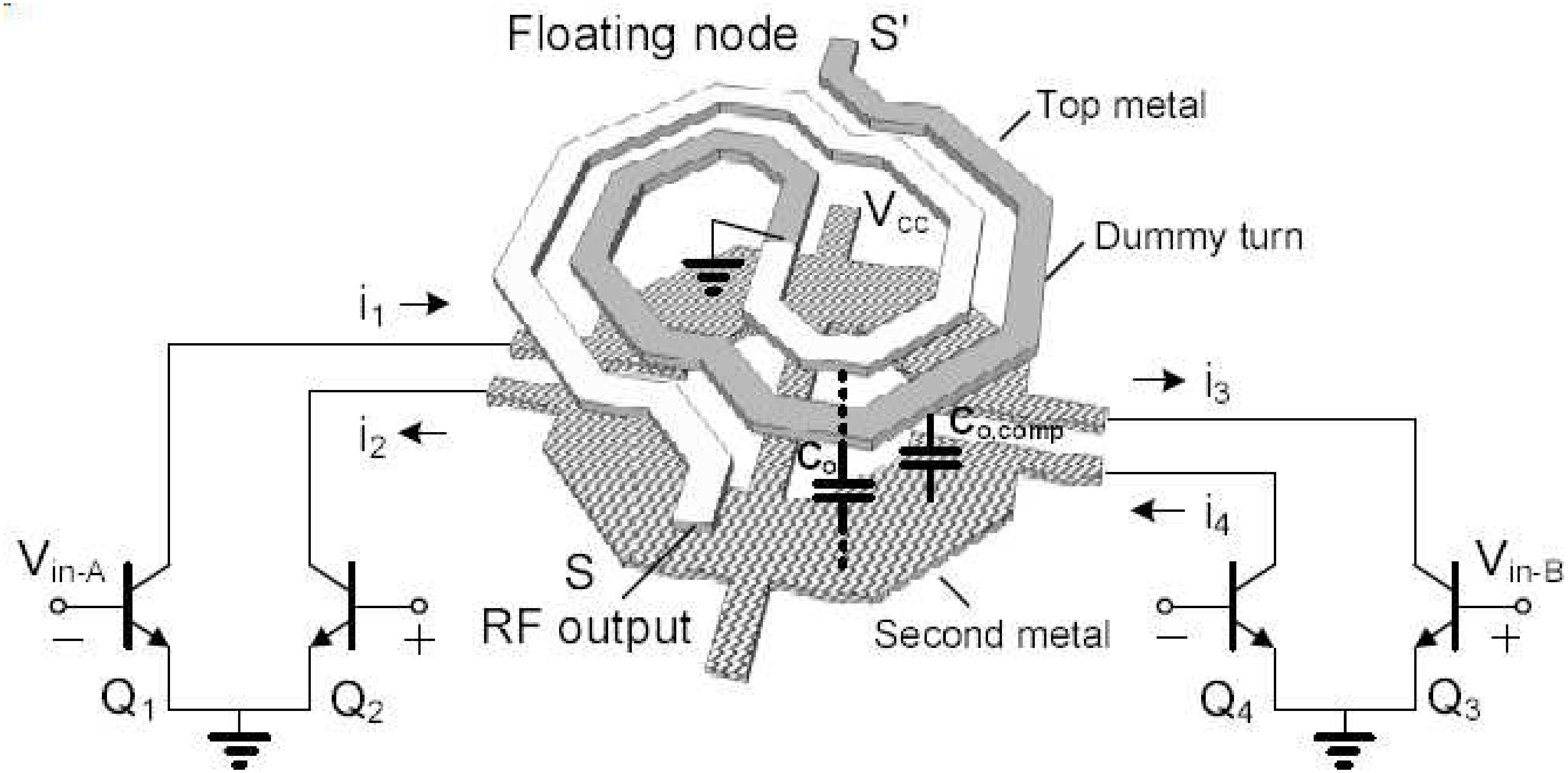
- **Primary shielded by lower-voltage secondary coil**
- **High secondary coil current rating (i.e., > 300mA)**

PA Power Combiner and Balun



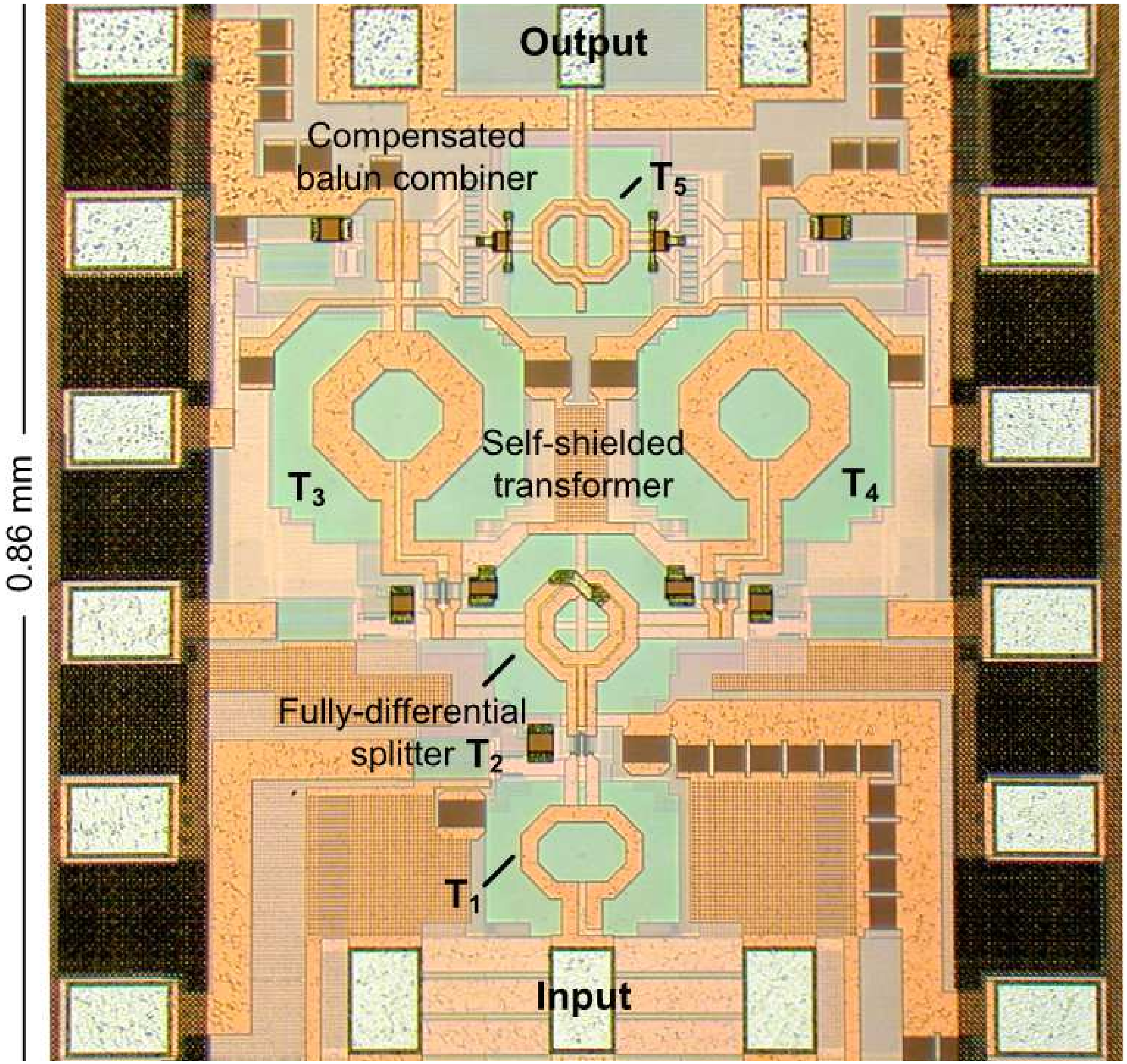
- Back-to-back measurement of self-shielded power combiner and balun. Balun MAG is 1.6dB, << 6dB increase in power from 4-way combining.

Compensated Power Combiner



- Interwinding capacitance compensation mitigates amplitude and phase imbalances and maximizes efficiency when combining power from 4 transistors. Insertion loss at 60GHz is <1dB and chip area is <0.015mm^2. Uniformity of impedances reflected from the load to the transistor outputs is better than 3%.

Dual-Path Power-Combining Amplifier



3-stage 60GHz PA with integrated I/O baluns in 130-nm BiCMOS
RF P_{out}=200mW @ 1.8V

Maximum output power > 20dBm and peak-PAE above 20% at 61.5GHz

Small-signal gain > 20dB
-3dB bandwidth > 10GHz

Reverse isolation > 51dB from 50-65GHz

0.25mm^2 active area
353mW quiescent @ 1.8V

Summary

- Monolithic transformers are synthesized from transmission lines; they are not "lumped elements" but do behave that way over a limited frequency range. Component parasitics must be captured to optimize RF circuit performance.

- Stacked metal windings offer wider bandwidth and higher k_m than planar windings in some technologies. Metal thickness, intermetal dielectric thickness and metal height above substrate affects the performance of stacked vs. planar transformers.

- Interconnect performance at RF is not well-understood, modeled or captured in conventional CAD tools.

- Passive devices in Si-technology are not readily scalable, and further improvements in process technology and IC-CAD models of passive devices are needed for analog RF/MMIC applications.

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