The Design of Sigma-Delta Modulation Analog-to-Digital Converters

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Abstract — **Oversampled analog-to-digital (A/D) converter architectures offer a means of exchanging resolution in time for that in amplitude so as to avoid the difficulty of implementing complex precision analog circuits. These architectures thus represent an attractive approach to implementing precision A/D converters in scaled digital VLSI technologies. This paper examines the practical design criteria for implementing oversampled converters based on second-order sigma-delta ($\Sigma\Delta$) modulation. Behavioral models that include representation of various circuit impairments are established for each of the functional building blocks comprising a second-order $\Sigma\Delta$ modulator. Extensive simulations based on these models are then used to establish the major design criteria for each of the building blocks. As an example, these criteria are applied to the design of a modulator that has been integrated in a 3-μm CMOS technology. This experimental prototype operates from a single 5-V supply, dissipates 12 mW, occupies an area of 0.77 mm^2, and achieved a measured dynamic range of 89 dB.**

I. INTRODUCTION

THE emergence of powerful digital signal processors implemented in CMOS VLSI technology creates the need for high-resolution analog-to-digital (A/D) converters that can be integrated in fabrication technologies optimized for digital circuits and systems. However, the same scaling of VLSI technology that makes possible the continuing dramatic improvements in digital signal processor performance also severely constrains the dynamic range available for implementing the interfaces between the digital and analog representation of signals. A/D converters based on sigma-delta ($\Sigma\Delta$) modulation combine sampling at rates well above the Nyquist rate with negative feedback and digital filtering in order to exchange resolution in time for that in amplitude. Furthermore, these converters are especially insensitive to circuit imperfections and component mismatch since they employ only a simple two-level quantizer, and that quantizer is embedded within a feedback loop. $\Sigma\Delta$ modulators thus provide a means of exploiting the enhanced density and speed of scaled digital VLSI circuits so as to avoid the difficulty of implementing complex analog circuit functions within a limited analog dynamic range.

A $\Sigma\Delta$ modulator consists of an analog filter and a coarse quantizer enclosed in a feedback loop [1]. Together with the filter, the feedback loop acts to attenuate the quantization noise at low frequencies while emphasizing the high-frequency noise. Since the signal is sampled at a frequency which is much greater than the Nyquist rate, high-frequency quantization noise can be removed without affecting the signal band by means of a digital low-pass filter operating on the output of the $\Sigma\Delta$ modulator.

The simplest $\Sigma\Delta$ modulator is a first-order loop wherein the filter consists of a single integrator [2], [3]. However, the quantization noise from first-order modulators is highly correlated [2]–[6], and the oversampling ratio needed to achieve resolution greater than 12 bits is prohibitively large. Higher order $\Sigma\Delta$ modulators, containing more than one integrator in the forward path, offer the potential of increased resolution. However, modulators with more than two integrators suffer from potential instability owing to the accumulation of large signals in the integrators [7], [8]. An architecture whereby several first-order modulators are cascaded in order to achieve performance that is comparable to that of higher order modulators has been suggested as a means of overcoming the stability problem [9]–[11]. These architectures, however, call for precise gain matching between the individual first-order sections, a requirement that conflicts with the goal of designing A/D converters that are especially insensitive to parameter tolerances and component mismatch. Second-order $\Sigma\Delta$ modulators are thus particularly attractive for high-resolution A/D conversion. The effectiveness of second-order $\Sigma\Delta$ modulator architectures has already been illustrated in a variety of applications. Digital speech processing systems and voice-band telecommunications codecs with A/D converters based on second-order $\Sigma\Delta$ modulation have been reported [12]–[15], and the extension of the performance achievable with such architectures to the levels required for digital audio [16] and higher [17] signal bandwidths has been demonstrated.

In this paper, the considerations faced in the design of second-order $\Sigma\Delta$ modulators are examined. First, analysis and simulation techniques for such modulators are introduced. Issues concerning the design and implementation of

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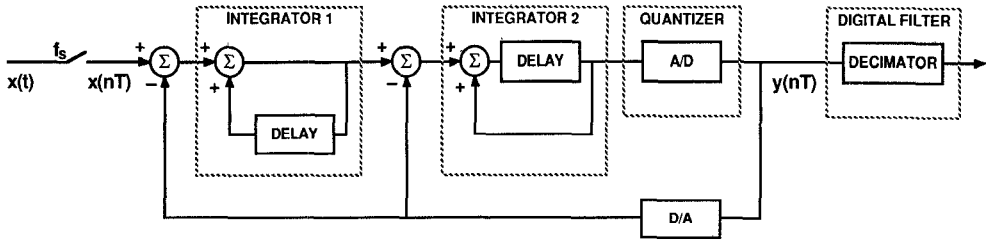


Fig. 1. Block diagram of second-order ΣΔ modulator with decimator.

the building blocks comprising a ΣΔ modulator, as well as the interactions between these blocks, are then examined, leading to a set of functional design criteria for each of the blocks. In Section IV, the design criteria are applied to an example implementation. Measurement results for this experimental prototype are presented in Section V.

II. System Design Considerations

A. Second-Order ΣΔ Modulator

Fig. 1 shows the block diagram of a second-order ΣΔ modulator. The analog input signal $x(t)$ is sampled at the sampling frequency $f_s = 1/T$. A quantizer with only two levels at $\pm \Delta/2$ is employed so as to avoid the harmonic distortion generated by step-size mismatch in multibit quantizers. Out-of-band quantization noise in the modulator output is eliminated with a digital decimation filter that also resamples the signal at the Nyquist rate, $2B$. The power S_N of the noise at the output of the filter is the sum of the in-band quantization noise S_B together with in-band noise arising from other error sources, such as thermal noise or errors caused by jitter in the sampling time. An approximate expression for the quantization noise when the quantizer is modeled by an additive white-noise source [7] is

$$S_B = \frac{\pi^4}{5}\frac{1}{M^5}\frac{\Delta^2}{12}, \qquad M \gg 1. \tag{1}$$

The coefficient M is the oversampling ratio, defined as the ratio of the sampling frequency f_s to the Nyquist rate $2B$. For every octave of oversampling, the in-band quantization noise is reduced by 15 dB.

The performance of A/D converters for signal processing and communications applications is usually characterized in terms of the *signal-to-noise ratio*. Two definitions for this ratio will be used here. The TSNR is the ratio of the signal power to the total in-band noise, whereas the SNR accounts only for uncorrelated noise and not harmonic distortion. The useful signal range, or *dynamic range* (DR), of the A/D converter for sinusoidal inputs is defined as the ratio of the output power at the frequency of the input sinusoid for a full-scale input to the output signal power for a small input for which the TSNR is unity (0 dB). The dynamic range of an ideal Nyquist rate uniform PCM converter with b bits is $DR = 3 \cdot 2^{2b-1}$. This definition of the dynamic range provides a simple means of comparing the resolution of oversampled and Nyquist rate converters. For example, a 16-bit Nyquist rate A/D converter corresponds to an oversampled A/D with 98-dB dynamic range.

For the successful design and integration of a second-order ΣΔ modulator, it is important to establish the sensitivity of the system's performance to various circuit nonidealities. Functional simulation techniques must be used to examine the design trade-offs because the application of conventional circuit and system analysis methods to the study of higher order ΣΔ modulators has, to date, proven to be intractable. Circuit simulations alone are not an effective design approach, since they do not explicitly illustrate the fundamental trade-offs necessary in the design process. The approach taken here is based on the use of a custom simulation program that embodies quantitative models for the functional elements comprising a ΣΔ modulator that reflect nonidealities in the behavior of those elements. Descriptions of these elements are held in a generic form so that they can be mapped to a large variety of possible circuit implementations.

Because of the oversampling process and the long-term memory of second-order ΣΔ modulators, long data traces are necessary to accurately estimate the performance of such converters. MIDAS, a general-purpose simulator for mixed analog and digital sampled-data systems, has been used to generate these traces. MIDAS accepts a system description in the form of a net list and is thus flexible enough to accommodate a wide variety of architectural configurations. Estimates of dynamic range and signal-to-noise ratio, as well as distortion, are generated in MIDAS using the *sinusoidal minimal error method*, a computationally efficient algorithm suitable for both simulation and experimental measurement purposes [18].

Several types of nonidealities that are characteristic of analog circuit implementations of ΣΔ modulators have been studied. Signal range, electronic noise, and timing jitter are discussed below. The sensitivity of the modulator performance of the characteristics of the integrators and the comparator is then considered in Section III.

B. Signal Range

For the conventional second-order ΣΔ modulator architecture shown in Fig. 1, simulations reveal that the signal range required at the outputs of the two integrators is several times the full-scale analog input range, $\pm \Delta/2$. This requirement represents a severe problem in circuit technologies, such as CMOS VLSI, where the dynamic

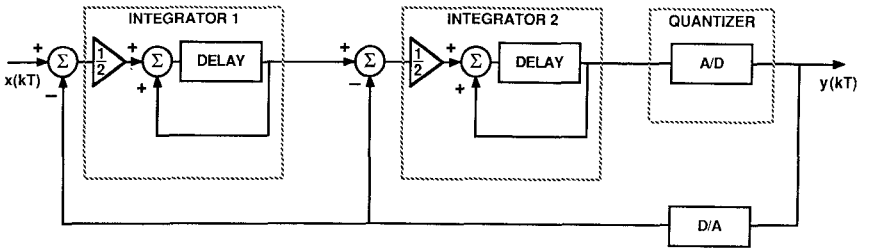


Fig. 2. Modified architecture of second-order ΣΔ modulator.

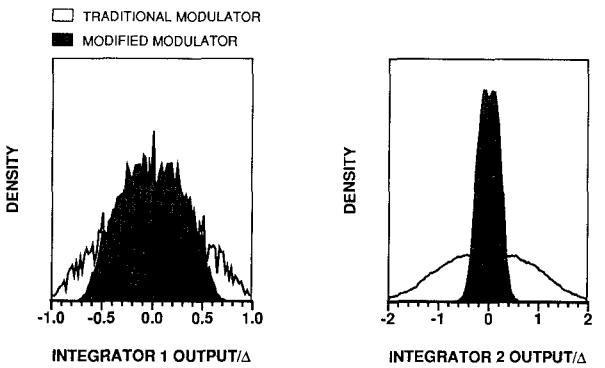


Fig. 3. Comparison of integrator output probability densities for traditional and modified architectures with sinusoidal input 3 dB below overload.

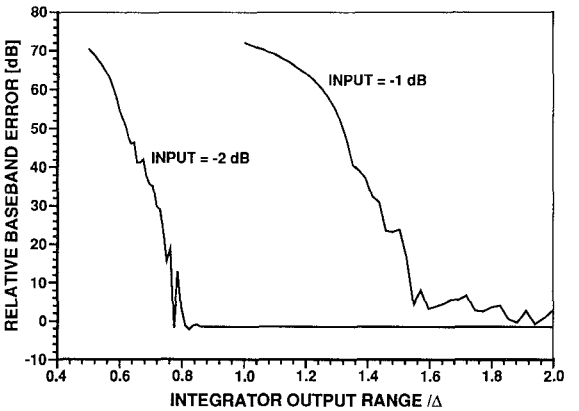


Fig. 4. Simulated influence of integrator output range on baseband quantization noise for input sinusoids 1 and 2 dB below overload.

range is restricted. The modified modulator architecture shown in Fig. 2 calls for considerably smaller signal ranges within the integrators. This architecture differs from the traditional configuration in two respects: a forward path delay is included in both integrators, thus simplifying the implementation of the modulator with straightforward sampled-data analog circuits, and each integrator is preceded by an attenuation of 0.5. An extraction of the modified architecture from the conventional structure results in a configuration with an attenuation of 0.5 preceding the first integrator and a gain of 2 at the input of the second integrator. However, since the second integrator is followed immediately by a single-threshold quantizer, its gain can be adjusted arbitrarily without impairing the performance of the modulator [19].

Fig. 3 shows the probability densities of the outputs of the two integrators for both the traditional (Fig. 1) and the modified (Fig. 2) ΣΔ modulator architectures. Whereas the signals at the outputs of both integrators extend only slightly beyond the full-scale input for the modified modulator design, the signal ranges are considerably larger for the traditional architecture. The modified modulator architecture therefore requires a signal range in the integrators which is only slightly larger than the full-scale input range of the A/D converter. Fig. 4 shows the relative increase in baseband noise that results from clipping the integrator outputs for input signals 1 and 2 dB below overload. From these results it is apparent that for signals as large as 1 dB below overload, the performance penalty is negligible when the signal in both integrators is clipped to a range that is about 70 percent larger than the full-scale input range.

C. Electronic Noise

In analog implementations of ΣΔ modulators, the signal is corrupted not only by quantization error, but also by electronic noise generated in the constituent circuits. Noise injected at the modulator input is the dominant contributor. Input-referred noise from the comparator undergoes the same second-order differentiation as the quantization noise, and noise injected at the input of the second integrator is subjected to a first-order difference function. Out-of-band noise is eliminated by the decimation filter, but high-frequency noise at multiples of the sampling frequency will be aliased into the baseband. The total input-referred noise power within the baseband does contribute to S_N and thus ultimately limits the resolution of the A/D converter.

Offset is only a minor concern in many signal acquisition systems, as long as the quantization is uniform. The offset at the input to the first integrator is the only significant contributor because offsets in the second integrator and the comparator are suppressed by the large low-frequency gain of the integrators. In practice, excessive offsets should be avoided because of the consequent reduction in the effective signal range in the integrators.

D. Sampling Jitter

The sampling theorem states that a sampled signal can be perfectly reconstructed provided that the sampling frequency is at least twice the signal bandwidth and that the sampling occurs at uniformly distributed instances in time. An anti-aliasing filter preceding the sampler ensures that

the first of these requirements is fulfilled. Oversampled A/D converters put considerably less stringent requirements on this filter than Nyquist rate converters since the signal is sampled at a frequency which far exceeds its bandwidth. Sampling clock jitter results in nonuniform sampling and increases the total error power in the quantizer output. The magnitude of this error increase is a function of both the statistical properties of the sampling jitter and the input to the A/D converter. An estimate for this error is derived below.

The error resulting from sampling a sinusoidal signal with amplitude A and frequency f_x at an instant which is in error by an amount δ is

$$x(t+\delta)-x(t) \approx 2\pi f_x \delta A \cos 2\pi f_x t. \tag{2}$$

Under the assumption that the sampling uncertainty δ is an uncorrelated Gaussian random process with standard deviation Δt, the power of this error signal is

$$S_\delta = \frac{A^2}{2}(2\pi f_x \Delta t)^2 \tag{3}$$

with a spectrum that is a scaled and modulated (by the sinusoidal input signal) version of the timing jitter δ. In an oversampled A/D converter, the decimation filter removes the content of this signal at frequencies above the baseband. Since the clock jitter is assumed to be white, the total power of the error is reduced by the oversampling ratio M in the decimator process. The in-band error power $S_{\Delta t}$ is therefore

$$S_{\Delta t} \leq \frac{\Delta^2}{8}\frac{(2\pi B \Delta t)^2}{M}. \tag{4}$$

In this expression, the worst-case amplitude ($\pm \Delta/2$) and signal frequency (B) have been used in order to establish an upper bound on the error power.

The error caused by clock jitter is inversely proportional to the oversampling ratio M and adds directly to the total error power S_N at the output of the A/D converter. Since the in-band quantization noise S_B is inversely proportional to the fifth power of M, the amount of clock jitter that can be tolerated decreases for an increase in oversampling ratio.

III. Integrator and Comparator Design

The two integrators in the forward path of a second-order $\Sigma\Delta$ modulator serve to accumulate the large quantization errors that result from the use of a two-level quantizer and force their average to zero. Ideally, for an integrator of the form used in the modulator architecture of Fig. 2 the output, $v(kT)$, is the sum of the previous output, $v(kT-T)$, and the previous input, $u(kT-T)$:

$$v(kT) = g_0 u(kT-T) + v(kT-T). \tag{5}$$

The constant g_0 represents the gain preceding the input to the integrator, which is 0.5 for each of the integrators in Fig. 2. The above equation corresponds to the following transfer function for an ideal integrator:

$$H(z) = \frac{g_0 z^{-1}}{1-z^{-1}}. \tag{6}$$

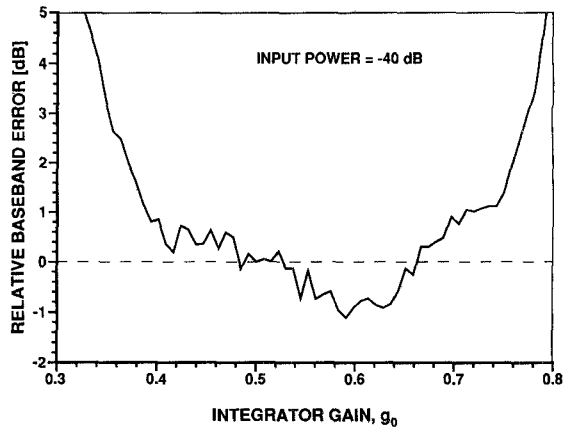


Fig. 5. Simulated influence of variations in integrator gain on baseband quantization noise.

Analog circuit implementations of the integrators deviate from this ideal in several ways. Errors which result from finite gain and bandwidth, as well as those due to nonlinearities, are considered below.

A. Gain Variations

It was pointed out previously that a scalar preceding the second integrator in the $\Sigma\Delta$ modulator of Fig. 2 has no effect on the behavior of an ideal modulator because it is absorbed by the two-level quantizer. However, deviations in g_0 from its nominal value in the first integrator alter the noise shaping function of the $\Sigma\Delta$ modulator and consequently change the performance of the A/D converter.

Fig. 5 shows the change of the in-band quantization noise as a function of g_0. Gain variations of as much as 20 percent from the nominal value have only a minor impact on the performance of the A/D converter, confirming the general insensitivity of the $\Sigma\Delta$ modulator architecture to component variations. Larger g_0 means higher gain in the forward path of the modulator and consequently greater attenuation of the quantization noise. However, for gains larger than about 0.6, the signal amplitudes at the integrator outputs increase rapidly and the system becomes unstable.

B. Leak

The dc gain of the ideal integrator described by (6) is infinite. In practice, the gain is limited by circuit constraints. The consequence of this "integrator leak" is that only a fraction of P_0 of the previous output of the integrator is added to each new input sample. The integrator transfer function in this case becomes

$$H(z) = \frac{g_0 z^{-1}}{1-P_0 z^{-1}} \tag{7}$$

and the dc gain is $H_0 = g_0/(1-P_0)$. The limited gain at low frequency reduces the attenuation of the quantization noise in the baseband and consequently, for the $\Sigma\Delta$ modulator of Fig. 2, results in an increase of the in-band

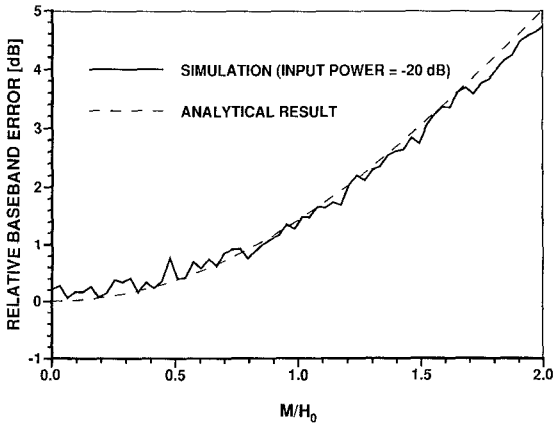


Fig. 6. Influence of integrator leak on baseband quantization noise.

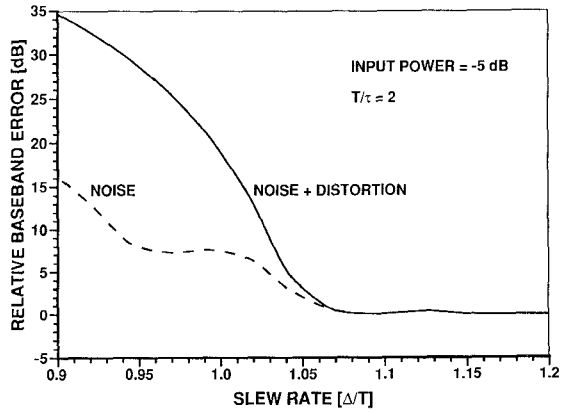


Fig. 7. Simulated influence of integrator output slew rate on baseband quantization noise.

quantization noise S_B that is given by

$$\frac{\Delta S_B}{S_B} = \frac{5}{\pi^4}\left(\frac{M}{H_0}\right)^4 + \frac{10}{3\pi^2}\left(\frac{M}{H_0}\right)^2. \tag{8}$$

This relationship is plotted in Fig. 6, along with data obtained from simulations, for an input 20 dB below full scale. The performance penalty incurred is on the order of 1 dB when the integrator dc gain is comparable to the oversampling ratio.

C. Bandwidth

In typical sampled-data analog filters, the unity-gain bandwidth of the operational amplifiers must often be at least an order of magnitude greater than the sampling rate. However, simulations indicate that integrator implementations using operational amplifiers with bandwidths considerably lower than this, and with correspondingly inaccurate settling, will not impair the $\Sigma\Delta$ modulator performance, provided that the settling process is linear.

For integrators with an exponential impulse response—as is observed for implementations which are based on an amplifier with a single dominant pole—the time constant of the response, τ, can be nearly as large as the sampling period T. This constraint is considerably less stringent than requiring the integrator to settle to within the accuracy of the A/D converter. Simulation results indicate that for values of τ larger than the sampling period, the modulator becomes unstable. In Section V it will be argued that in practice τ must actually be kept somewhat smaller than T.

D. Slew Rate

In the preceding subsection it was pointed out that a large time constant for the settling of the integrator output is acceptable, provided that the settling process is linear. In particular, the settling must not be slew-rate limited. The simulation results presented in Fig. 7 indicate a sharp increase in both quantization noise and harmonic distortion of the converter when the slew rate is less than $1.1\Delta/T$. These simulations are based on the assumption that if the integrator response is not slew-rate limited, the impulse response is exponential with time constant τ:

$$v(kT+t) = \frac{g_0}{1-e^{-T/\tau}}u(kT)[1-e^{t/\tau}] + v(kT). \tag{9}$$

The term $1-e^{-T/\tau}$ has been included to separate the effects of finite slew rate from those due to variations in the equivalent gain. The peak rate of change in the impulse response occurs at $t=0$ and is given by

$$\frac{dv(kT+t)}{dt} = \frac{g_0}{1-e^{-T/\tau}}\frac{u(kT)}{\tau}. \tag{10}$$

Slewing distortion occurs when this rate exceeds the maximum slew rate the integrator can support.

E. Nonlinearity

The imperfections in analog circuit realizations of the integrators that have been considered above are either linear deviations from the ideal frequency response due to gain and bandwidth limitations, or large-scale nonlinearities, such as clipping and slewing. In this subsection the influence of differential nonlinearities on the modulator performance is examined. Such nonlinearities occur, for example, when the integrator implementation is based on capacitors that exhibit a voltage dependence, or on an amplifier with input-dependent gain. From simulations it has been observed that the consequence of these nonlinearities is harmonic distortion that limits the peak SNR achievable at large signal levels.

The following quantitative analysis of effects of integrator nonlinearity is based on representing the integrator by

$$\begin{aligned} v(kT)&\left[1+\beta_1 v(kT)+\beta_2 v^2(kT)+\cdots\right] \\ &= g_0 u(kT-T)\left[1+\alpha_1 u(kT-T)\right. \\ &\quad \left.+\alpha_2 u^2(kT-T)+\cdots\right] \\ &\quad + v(kT-T)\left[1+\beta_1 v(kT-T)\right. \\ &\quad \left.+\beta_2 v^2(kT-T)+\cdots\right]. \end{aligned} \tag{11}$$

This model has been found to be typical of a variety of possible integrator implementations. The parameters α_i and β_i are the coefficients of Taylor series expansions of the integrator input and output and are associated with nonlinearities in the input and the storage elements, re-

spectively. In switched-capacitor integrators, for example, these correspond to the voltage coefficients of the capacitors [20].

Fig. 8 shows simulation and analytical results obtained for evaluating the influence of integrator nonlinearities on the TSNR of the A/D converter, assuming a sinusoidal input. The performance degradation is proportional to the amplitude of the input for the first-order nonlinearity, and proportional to the square of the modulator input for second-order nonlinearity. The degradation is a consequence of harmonic distortion, rather than an increase in quantization noise; thus, it is possible to evaluate the harmonic distortion without taking the quantizer into consideration.

Only distortion introduced by the first integrator in a second-order ΣΔ architecture such as that of Fig. 2 need be considered, since errors introduced by the second integrator are attenuated by the feedback loop. The input to the first integrator is the difference between the modulator input, $x(kT)$, and the modulator output, which consists of the sum of the input delayed by two sampling periods and the quantization noise. The latter can be neglected in the distortion analysis, as has been pointed out above. For a sinusoidal modulator input with amplitude A and frequency f_x, the input to the first integrator is approximately

$$x(kT)-x(kT-2T)\approx 4\pi f_x TA\cos 2\pi f_x T, \qquad f_x T \ll 1. \tag{12}$$

The input-referred harmonics of the integrator for this signal can be determined either by distortion analysis with a circuit simulation program such as SPICE [21] or SWAP [22], or analytically, in a manner similar to the analysis presented in [20]. When the assumption is made that $\alpha_i = \beta_i$, the amplitudes of the first and second harmonics are

$$h_1 = \frac{\alpha_1}{2}A_1^2 \tag{13}$$

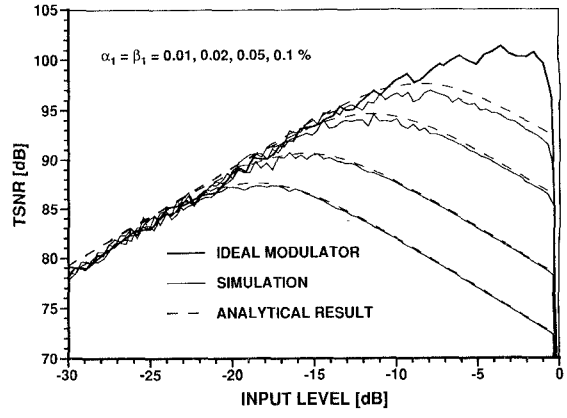
and

$$h_2 = \frac{\alpha^2}{2}A_1^3 \tag{14}$$

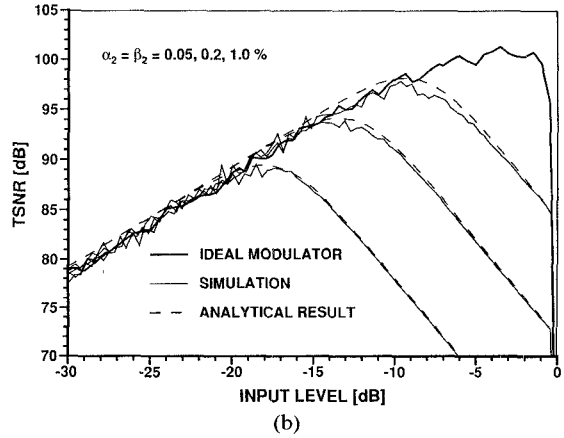
respectively. The power of the harmonic distortion in the output of the A/D converter due to integrator nonlinearity is then approximately $h_1^2/2 + h_2^2/2$, provided that the contribution of higher order harmonics is negligible. Harmonics at frequencies above the bandwidth of the converter are, of course, suppressed by the decimation filter. This result is in excellent agreement with simulations that do not include any simplifications.

F. Comparator Hysteresis

The 1-bit quantizer in the forward path of a ΣΔ modulator can be realized with a comparator. The principle design parameters of this comparator are speed, which must be adequate to achieve the desired sampling rate,



(a)



(b)

Fig. 8. Influence of integrator nonlinearity on A/D converter performance: (a) first-order nonlinearity, and (b) second-order nonlinearity.

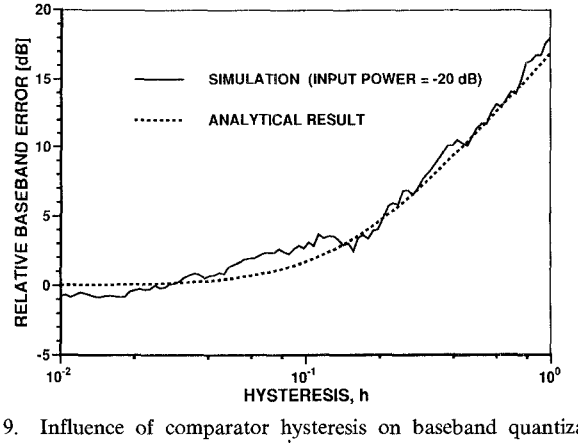


Fig. 9. Influence of comparator hysteresis on baseband quantization noise.

input offset, input-referred noise, and hysteresis. It has been pointed out already that offset and noise at the comparator input are suppressed by the feedback loop of modulator. Fig. 9 shows the performance of the A/D converter as a function of comparator hysteresis, defined as the minimum overdrive required to change the output. The power of the in-band noise, S_N, is virtually unchanged for hysteresis as large as 10 percent of the full-scale converter input, Δ, and rises at 20 dB per decade above this point.

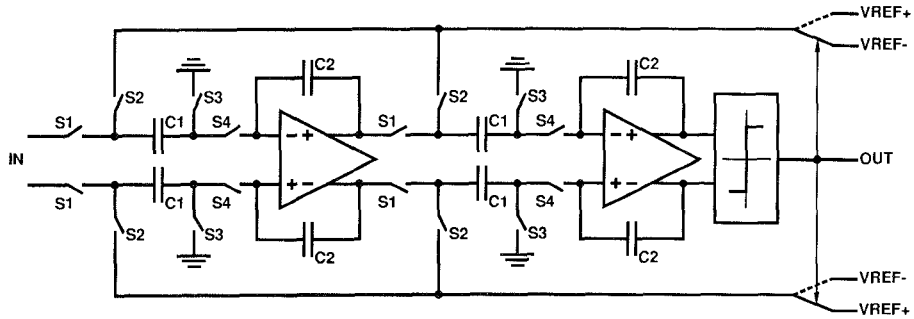


Fig. 10. Second-order ΣΔ modulator implementation.

The sensitivity of the A/D converter performance to comparator hysteresis is modeled quite accurately by an additive white noise with power $(h\cdot\Delta/2)^2$, where h is the magnitude of the comparator hysteresis relative to Δ. The noise undergoes the same spectral shaping as the quantization noise. The sum of the quantization noise, S_B, and the hysteresis is therefore

$$S_N = \frac{\pi^{2L}}{2L+1}\frac{\Delta^2}{M^{2L+1}}\left[\frac{1}{12}+4h^2\right], \qquad M \gg 1. \quad (15)$$

The factor 4 reflects the adjustment of the scalar preceding the second integrator from 2 to 0.5.

The sensitivity of ΣΔ modulators to comparator hysteresis is several orders of magnitude smaller than that of Nyquist rate converters. It is apparent from the model that this is attributable to the presence of negative feedback with high loop gain in a ΣΔ modulator.

IV. Implementation

The considerations addressed above have been applied to the design of a second-order ΣΔ modulator that has been integrated in a 3-μm CMOS technology. The performance objective for this design was a dynamic range of 16 bits at as high a Nyquist rate as could be achieved within the constraints of the technology in which the circuit was integrated. The resolution of 16 bits corresponds to a dynamic range of 98 dB, which can be achieved with an oversampling ratio of $M=153$ if the performance is limited only by the quantization noise. To allow for increased baseband noise due to circuit nonidealities, as well as to maintain an oversampling ratio that is a power of 2 so as to simplify the subsequent decimation to the Nyquist sampling rate, a sampling ratio of $M=256$ was chosen. The modulator has been designed to operate from a single 5-V power supply.

A. Circuit Topology

Since ΣΔ modulators are sampled-data systems, they are readily implemented in MOS technology with switched-capacitor (SC) circuits. Fig. 10 shows a possible topology. A fully differential configuration has been adopted in order to ensure high power supply rejection, reduced clock feedthrough and switch charge injection

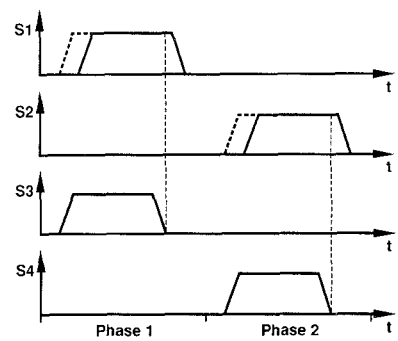


Fig. 11. Clock diagram for second-order ΣΔ modulator.

errors, improved linearity, and increased dynamic range. The two identical integrators in Fig. 10 each consist of an amplifier, two sampling capacitors C_1, and two integrating capacitors C_2. The ratio of C_1 to C_2 is chosen so as to realize the gain of 0.5 that precedes each integrator in the architecture of Fig. 2.

Operation of the modulator is controlled by a nonoverlapping two-phase clock. During phase 1 all of the switches labeled S_1 and S_3 are open, while those labeled S_2 and S_4 are closed, and the input to each integrator is sampled onto the capacitors C_1. In phase 2, switches S_1 and S_3 open, while S_2 and S_4 close, and charge stored on C_1 is transferred to C_2. During this phase, the closing of switches S_2 has the effect of subtracting the output of the two-level D/A network from the input to each integrator. The comparison of the outputs from the second integrator is performed during phase 1, and the comparator reset during phase 2. With this clocking arrangement, the time available for the integration and the time for the comparison are both one-half a clock cycle.

To first order, the charge injected by the MOS switches in the circuit of Fig. 1 is a common-mode signal that is canceled by the differential implementation of the modulator. Signal-dependent charge injection is further suppressed by opening switches S_3 and S_4 slightly before S_1 and S_2, respectively [23]. Since S_3 and S_4 are connected to either a ground or virtual ground node, they do not exhibit signal-dependent charge injection. Once S_3 or S_4 has opened, and before the other has closed, C_1 is floating; thus, the subsequent opening of S_1 or S_3 during the interval when both S_3 and S_4 are open will, to first order, not inject charge onto C_1.

A timing diagram for all of the switches in the modulator is given in Fig. 11. The switches are closed when the controlling clocks are high. The clocks must be nonoverlapping in order to prevent charge sharing. The clocks for switches S_1 and S_2 are generated by delaying the clocks for S_3 and S_4. An upper limit for the tolerable clock jitter follows from (4):

$$\Delta t \leq \frac{1}{2\pi B \cdot 2^b}\sqrt{\frac{2M}{3}}. \tag{16}$$

If the baseband error power induced by clock jitter is to be no larger than the quantization noise resulting from an ideal modulator, then it is necessary that $\Delta t \leq 630$ ps for $B = 20$ kHz.

The choice of the full-scale analog input range of the converter, which is equal to the quantizer step size Δ, involves trade-offs among a number of design constraints. A large signal range is desirable due to the presence of electronic noise in the analog circuits. However, a large signal range results in increased harmonic distortion due to integrator nonlinearity. In addition, increasing the signal range calls for operational amplifiers with a higher slew rate. A differential full-scale input range of $\Delta = 4$ V has been chosen so as to limit the performance impairment due to electronic noise. The simulation results presented in Fig. 4 indicate that the signal range at the output of both integrators should be at least 50 percent larger than the full-scale analog input in order to avoid significant performance degradation. The output swing of the operational amplifiers should therefore be at least 6 V. This requirement is accommodated within a single 5-V supply through the use of the fully differential topology.

B. Integrator Design

The design of the differential operational amplifier is key to the successful realization of the integrators. The specifications for this amplifier follow from the integrator performance requirements described in the previous section. A consideration of integrator leak mandates that the amplifier open-loop gain be at least equal to the oversampling ratio, $M = 256$. However, the gain must generally be somewhat larger than this in order to adequately suppress harmonic distortion.

An operational amplifier that is not slew-rate limited is essential in order to avoid slewing distortion. A class *AB* configuration with a single gain stage similar to that described in [24] has been chosen to meet this constraint. The slew-rate requirement is more stringent for this implementation than was derived from Fig. 7 for two reasons. First, the integration is accomplished only during phase 2 and thus must be completed within one-half the clock cycle. Second, the signal swing at the integrator output in response to a step input is somewhat larger than anticipated in Fig. 7 owing to feedforward through the integrating capacitors C_2. Therefore, in the implementation of Fig. 10 the slew rate must be at least $3\Delta/T \approx 150$ V/μs.

For an amplifier with a single dominant pole and unity-gain frequency f_u, the impulse response of the integrator output during phase 2 will be exponential with a time constant [25], [26]

$$\tau = \frac{1 + C_1/C_2}{2\pi f_u}. \tag{17}$$

The simulation results presented in the previous section indicate that the condition $\tau \leq T$ must be met in order to guarantee stability of the modulator. This requirement corresponds to a lower limit for f_u of

$$f_u \geq \frac{1 + C_1/C_2}{\pi T}. \tag{18}$$

The fact that only one-half of the clock period T is available for the integration has been accounted for in this equation. From (18) it is apparent that the bandwidth f_u must be greater than approximately one-half the sampling rate, provided that the step response is purely exponential. In practice, this latter requirement is not met precisely because of secondary effects such as nondominant poles and the dependence of the pole locations on the amplifier operating point, which in this design changes during transients.

Constraints on the dynamic range mandate that the sum of input-referred baseband noise of the first integrator and baseband noise in the output of the two-level D/A network be 104 dB below the power of a full-scale sinusoidal input to the converter if this noise is not to exceed the quantization noise. Sampling capacitors of 1 pF have been employed to reduce the level of thermal noise in the circuit, and large input transistors in the amplifier limit flicker noise.

Harmonic distortion limits the TSNR of the converter for large inputs. The main contributor to this distortion is nonlinearity in the first integrator, which is a consequence of the voltage dependence of the capacitors and the gain nonlinearity of the operational amplifier. In the previous section it was shown that it is possible to predict the impact of these nonlinearities through an analysis of the integrator alone. In these circumstances, the magnitude of the harmonics can be determined using a circuit simulator that includes distortion analysis.

An estimate of the tolerable voltage dependence of the capacitors can be extracted from the results presented in Fig. 8. For capacitors with a voltage dependence given by $C(v) = C_0(1 + \gamma_1 v + \gamma_2 v^2)$, it follows from charge conservation and comparison with (11) that $\alpha_1 = \beta_1 = \gamma_1\Delta$ and $\alpha_2 = \beta_2 = \gamma_2\Delta^2$. The first harmonic, h_1, will be smaller than predicted by (13) because of the differential configuration of the modulator. The peak TSNR will be reduced by about 6 dB for $\gamma_1 = 50$ ppm/V in a single-ended configuration; in the differential design the capacitor voltage coefficient can be several times larger for the same performance. Second-order harmonic distortion reduces the peak TSNR by 6 dB for $\gamma_2 = 30$ ppm/V^2 in a single-ended configuration.

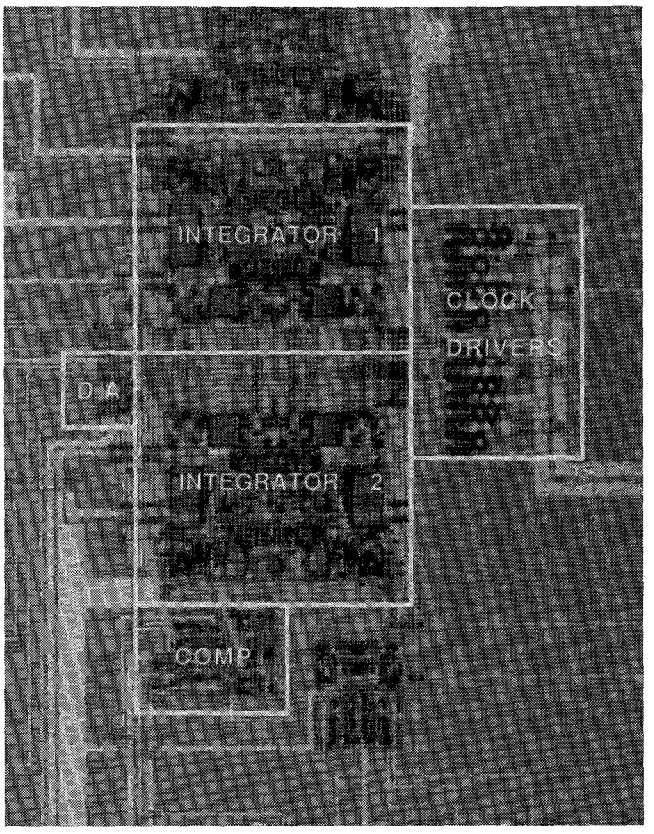


Fig. 12. Die photo of second-order ΣΔ modulator.

C. Comparator Design

Neither sensitivity nor offset considerations present stringent design constraints for the comparator in a second-order ΣΔ modulator. The two integrators provide preamplification of the signal, and due to the feedback the comparator offset is stored in the second integrator. The data in Fig. 9 imply that comparator hysteresis as large as 5 percent of the full-scale input range Δ has a negligible impact on the performance of the A/D converter. A simple regenerative latch without preamplification or offset cancellation, such as that presented in [27], fulfills the comparator requirements.

V. Experimental Results

The second-order ΣΔ modulator implementation of Fig. 10 has been integrated in a 3-μm CMOS technology. A photograph of the chip is shown in Fig. 12. Most of the 0.77-mm^2 die area is occupied by the two integrators, which have been laid out symmetrically in order to reduce component mismatch. The circuit dissipates 12 mW when operating from a single 5-V power supply.

For testing, the experimental ΣΔ modulator was connected to a high-quality sinusoidal signal source, and the initial stages of decimation were implemented with an off-chip digital filter. The output of this filter was then transmitted to a host computer for further filtering and an analysis of the performance. Amplitudes of both the output signal and its harmonics, the quantization noise power and spectral density, and the signal frequency were estimated by the host using the same algorithms employed for performing the simulations [18]. The advantage of this approach over techniques that are based on the use of a high-precision D/A converter and analog test instruments is its insensitivity to the performance of analog test equipment. The only analog—and therefore potentially limiting—component in the measurement setup is the sinusoidal source.

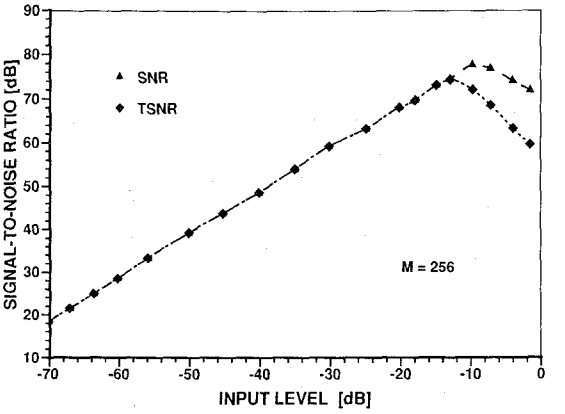


Fig. 13. Measured SNR for a sampling frequency of 4 MHz and a signal frequency of 1.02 kHz.

Fig. 13 shows the SNR and TSNR measured for the experimental A/D converter. For this data the modulator was operated at its maximum clock rate of $f_s = 4$ MHz, and the oversampling ratio was $M = 256$. The corresponding Nyquist rate is 16 kHz. The frequency of the sinusoidal input signal was 1.02 kHz. From the data of Fig. 13, the measured dynamic range of the converter is found to be 89 dB, which corresponds to a resolution of 14.5 bits. Additional tests show that the modulator performance drops by less than 3 dB for signal frequencies up to half the Nyquist rate. The measured gain tracking is better than ±0.5 dB and is limited largely by the decimation filter design used.

For large input signals, the precision of the converter is limited by harmonic distortion rather than quantization noise, as is apparent from the divergence of the TSNR from the SNR in Fig. 13. In this design, the amplifier is the dominant source of distortion, a consequence of the large signal range in the integrators in comparison with the supply voltage. The capacitors in the experimental modulator were realized with double polysilicon layers, and their contribution to the total distortion is negligible.

The dynamic range of the ΣΔ modulator is plotted as a function of the sampling rate in Fig. 14. For sampling rates below 4 MHz, the dynamic range is independent of the clock rate; it then drops rapidly at higher operating frequencies. The pronounced decrease of the performance above 4 MHz has also been observed in simulation results and has been identified as resulting from instability. The unity-gain bandwidth of the operational amplifiers was measured to be 8 MHz with a phase margin of 80°. Thus, the modulator can be operated at speeds up to half the amplifier bandwidth without performance degradation. In

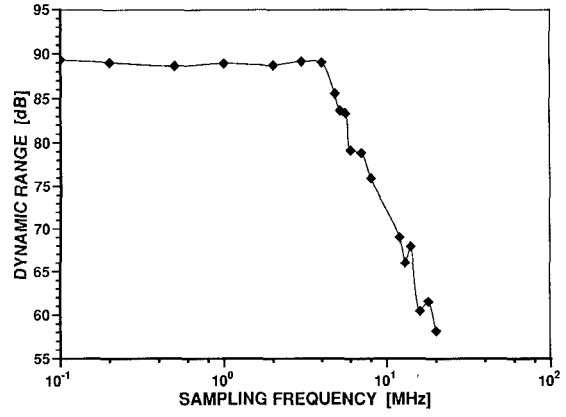


Fig. 14. Maximum operating frequency.

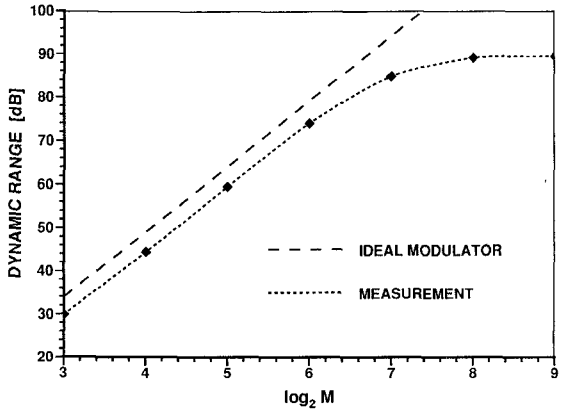


Fig. 15. Dynamic range as a function of the oversampling ratio for a sampling frequency of 4 MHz.

contrast, an order of magnitude higher bandwidth would be required if it were necessary for the amplifier outputs to settle to within the resolution of the overall converter.

Second-order effects are responsible for limiting the useful sampling frequency to a value which is smaller than that predicted by simulation of the modulator assuming integrators with a perfectly exponential impulse response. These effects include deviations in the impulse response from an exponential waveform because of the drastic change in bias currents that occur in the class *AB* operational amplifier during large-signal transients. In addition, the time constants of the amplifier response during phase 1 and phase 2 differ as a result of changes in the equivalent load capacitance. The slew rate of the amplifier is greater than 200 $V/\mu s$, sufficient to prevent slewing distortion in all operating conditions of the integrators.

In Fig. 15 the dynamic range of the converter is plotted as a function of the oversampling ratio. The performance increases by 15 dB for every doubling of the oversampling ratio up to $M \approx 64$, as is expected for an ideal $\Sigma\Delta$ modulator. In this regime, the dynamic range of the modulator is within 4 dB of that of an ideal modulator with perfect components and no error sources other than quantization noise. At higher oversampling ratios, the performance improvement obtained by increasing the oversampling ratio is reduced. Flicker noise in the input transistors of the first integrator has been found to be the primary limitation when the signal is oversampled by a factor greater than 64. The dynamic range of 89 dB corresponds to fabrication of the modulator in a technology wherein the $1/f$ noise is characterized by a flicker-noise coefficient $K_1 = 5 \cdot 10^{-24}$ $V^2 \cdot F$ [28], a value consistent with typical CMOS technologies [29]. This flicker-noise limitation can be overcome by increasing the size of the input transistors, or through the use of a chopper-stabilized amplifier [30]. The size of the input devices was kept relatively small in this design because of concern for the amplifier frequency response.

VI. Conclusion

Second-order $\Sigma\Delta$ modulators constitute an efficient architecture for implementing high-resolution A/D converters in scaled high-performance integrated circuit technologies. Both simulations and analytic results have been used to establish design criteria for the analog circuit blocks comprising such a modulator. Specifically, it has been found that integrator linearity has a crucial influence on the performance of these converters, whereas $\Sigma\Delta$ modulators impose only modest demands on integrator bandwidth and are relatively insensitive to offset and hysteresis in the comparator. The analysis presented here has also been used to identify mechanisms other than quantization noise that may limit the performance of $\Sigma\Delta$ modulators regardless of the oversampling ratio.

The limitations on both the speed and dynamic range of the experimental A/D converter reported herein can be readily overcome through the use of a higher performance technology. Scaled digital VLSI technologies are especially suitable for these types of converters because they provide the density and speed necessary to include the decimation filter, as well as other signal processing functions, on the same chip as the modulator. Conversely, oversampling architectures provide a means of exploiting the enhanced speed of scaled digital technologies so as to overcome constraints on the available dynamic range and the need for precision circuits and components. In a sampled-data CMOS implementation of a $\Sigma\Delta$ modulator, the only requirement imposed on the fabrication technology is the availability of capacitors. The accuracy of the capacitor ratios is not critical since the performance of $\Sigma\Delta$ modulators is not sensitive to the gain g_0 preceding the integrators. In comparison with Nyquist rate converters, relatively large capacitor voltage coefficients can be tolerated because the modulator feedback loop serves to reduce the resulting distortion.

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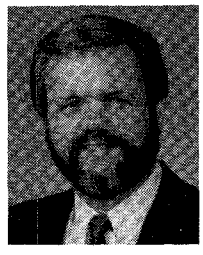

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