A 55-mW, 10-bit, 40-Msample/s Nyquist-Rate CMOS ADC

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***Abstract*—A low-power 10-bit converter that can sample input frequencies above 100 MHz is presented. The converter consumes 55 mW when sampling at $f_s = 40$ MHz from a 3-V supply, which also includes a bandgap and a reference circuit (70 mW if including digital drivers with a 10-pF load). It exhibits higher than 9.5 effective number of bits for an input frequency at Nyquist ($f_{\rm in} = f_s/2 = 20$ MHz). The differential and integral nonlinearity of the converter are within $\pm$0.3 and $\pm$0.75 LSB, respectively, when sampling at 40 MHz, and improve to a 12-bit accuracy level for lower sampling rates. The overall performance is achieved using a pipelined architecture without a dedicated sample/hold amplifier circuit at the input. The converter is implemented in double-poly, triple-metal 0.35-μm CMOS technology and occupies an area of 2.6 mm^2.**

***Index Terms*—Analog-to-digital (A/D) converter, Nyquist rate converter, pipeline converter, switched-capacitor design.**

I. Introduction

MANY applications ranging from wireless receivers and ultrasound systems to wireline interfaces and camera/camcorder front ends make use of 10-bit analog-to-digital converters (ADC's) sampling at around 40 MHz [12], [24], [27]. Most of them require low power consumption as well as low noise, and many of them require high dynamic performance for Nyquist input frequencies or higher. Modern CMOS technology provides the opportunity for implementing medium-resolution (8–12 bit) ADC's that are able to fulfill the requirements of the applications mentioned above. However, achieving good dynamic performance for high input frequencies has proved to be a difficult task [5], [7], [14], [16], [32]. Nyquist-rate ADC's that operate at high frequencies with reasonable power consumption have mainly been implemented using BiCMOS technology [12], and are only recently becoming accessible in CMOS [3], [21].

This paper presents a 10-bit pipeline ADC that features low power consumption (55 mW is the lowest reported figure for a Nyquist-rate 10-bit ADC sampling at 40 MHz) combined with good dynamic performance (ENOB = 9.55 at $f_{\rm in} = f_s/2 = 20$ MHz, which takes into account both noise and distortion) including spurious free dynamic range (SFDR > 72 dB) and total harmonic distortion (THD < –70 dB). This performance is achieved without using a dedicated input sample/hold amplifier (SHA) by distributing the sampling operation inside the first pipeline stage. Section II discusses design requirements and challenges then relates those to architectural choices and trade-offs. Circuit implementation details are presented in Section III, followed by measured results in Section IV. This paper concludes with Section V.

Manuscript received July 16, 1999; revised October 8, 1999.

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Publisher Item Identifier S 0018-9200(00)00542-4.

II. ADC Architecture

The list of design requirements is topped by a low-power CMOS Nyquist-rate (and above) implementation. Also, there is a need to preserve good linearity and low noise such that the converter exhibits true 10-bit performance (more that 9 ENOB) for input frequencies well beyond Nyquist when sampling at 40 Msample/s. Another constraint that results from the need for higher levels of integration is to build a converter in a small geometry and low area. The challenge in meeting the aforementioned requirements lies in the fact that many are conflicting (low noise versus small area, low power versus high-speed operation).

There are quite a few architectures that could be used to implement a 10-bit ADC. However, straight flash topologies are impractical from a power and area perspective. Also, successive approximation (or cyclic) topologies are not practical for high-speed Nyquist-rate operation. Consequently, two major candidates can be identified as architectural choices for this implementation. First, folding and/or interpolating (averaging) topologies have been successfully used as reported in [5] and [12]. They exhibit low power due mostly to interpolation, and low latency (delay from input to the output). However, they do not excel regarding dynamic performance, and based on the latest published results, bipolar technology is more appropriate for their implementation [31]. The second choice is the pipelined architecture [18], [30], known to be more power efficient at the expense of conversion latency. This parameter was not a major constraint, and reducing the latency usually means increased power consumption by using fewer stages or a two-step architecture at the extreme [26]. In pipeline converters, power consumption can be optimized by an appropriate selection of bits/stage [17], [20] and capacitor scaling down the pipeline [8]. Also, pipeline architectures are successfully implemented in CMOS using switched-capacitor design, which makes them easy to integrate. Speed can be improved through the use of various parallel blocks through the pipeline [4], [15], [23], although usually at the expense of higher power consumption and less impressive dynamic performance for high input frequencies. For parallel-type pipeline converters, the degradation in performance due to mismatches between channels can be reduced by calibration [9]. Also, since the dynamic performance of any converter is dependent on its linearity, it is worth considering some form of calibration [13], [25] for this reason as well. Nevertheless, this

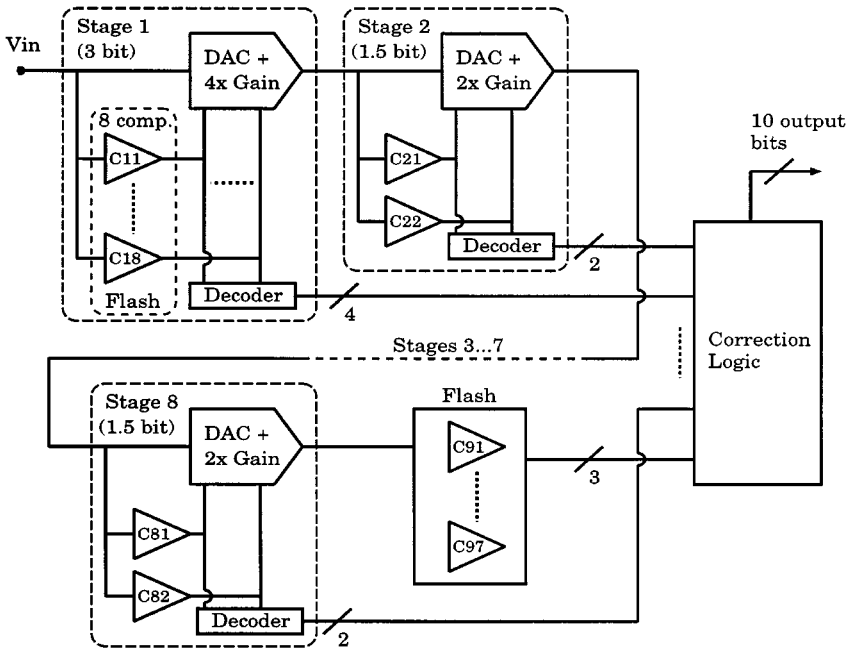

Fig. 1. A 10-bit ADC pipeline architecture including 3-bit first stage followed by 1.5-bit stages and a 3-bit flash in the back end.

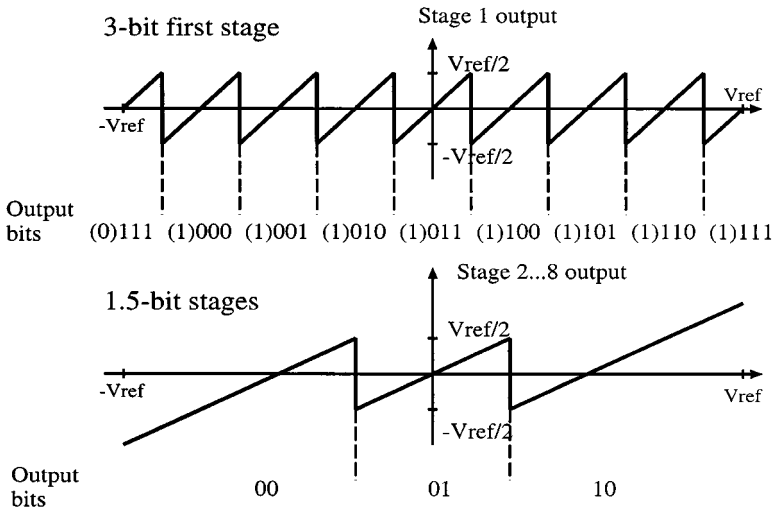

Fig. 2. Residue transfer functions for Stage 1 and Stages 2–8 from Fig. 1.

usually adds to the power consumption and the operation at high input frequencies is still very difficult to improve. Another example is [10], where dither was used to improve dc linearity; however, its effectiveness for a large range of input frequencies is disputable. The present design does not use calibration since good linearity can be achieved at the 10-bit level using double-poly capacitors [11], [28]. However, this implementation is prone to coupling particularly for higher integration systems. Consequently, a fully differential topology is used for the converter presented here, and a single-ended to differential conversion is performed in the front-end sampling network [29] since both type of inputs need to be accommodated.

Fig. 1 presents the architecture of the converter. The first stage samples the input and generates the residue for the next stage. Note the absence of an input SHA. Typically, the dynamic performance of pipeline converters is limited at the front end by the distortion and noise performance of the SHA. This implies significant power consumption in this block in order to achieve the requirements for high input frequencies. The absence of this block saves power; however, since a sampling operation is still needed, the sampling operation is distributed inside the first stage. The gain/digital-to-analog converter (MDAC) block and the comparators in the flash ADC inside the first stage all sample directly the input voltage. Then the MDAC generates and holds the residue for the next stage [1], [4], [7], [8], [10], [30]. Although this would contribute to aperture errors, particularly in the presence of high-frequency signals at the input, it is possible to obtain good dynamic performance by matching the sampling networks for the MDAC and the comparators in terms of topology and time constants. The price paid for not having a dedicated SHA is more power spent in the op-amp and comparators inside the first stage. These need to be faster, as discussed in the next section; however, the overall power consumption is significantly reduced. All pipeline stages are 1.5 bit (one bit

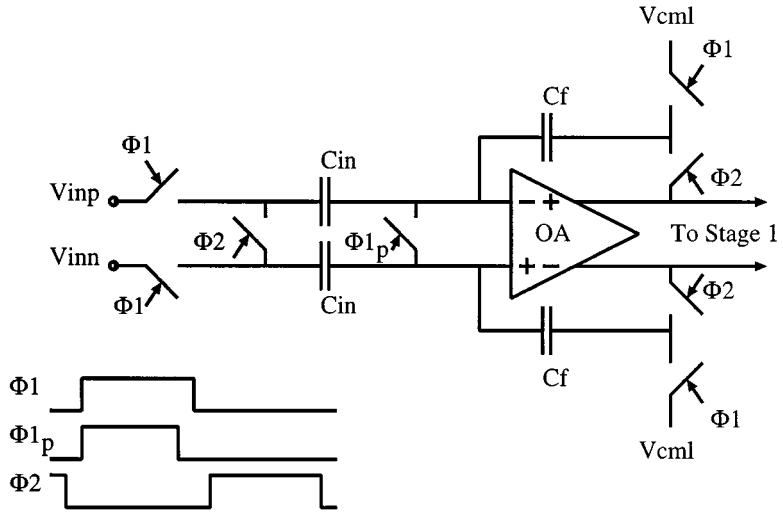

Fig. 3. Conventional SHA architecture.

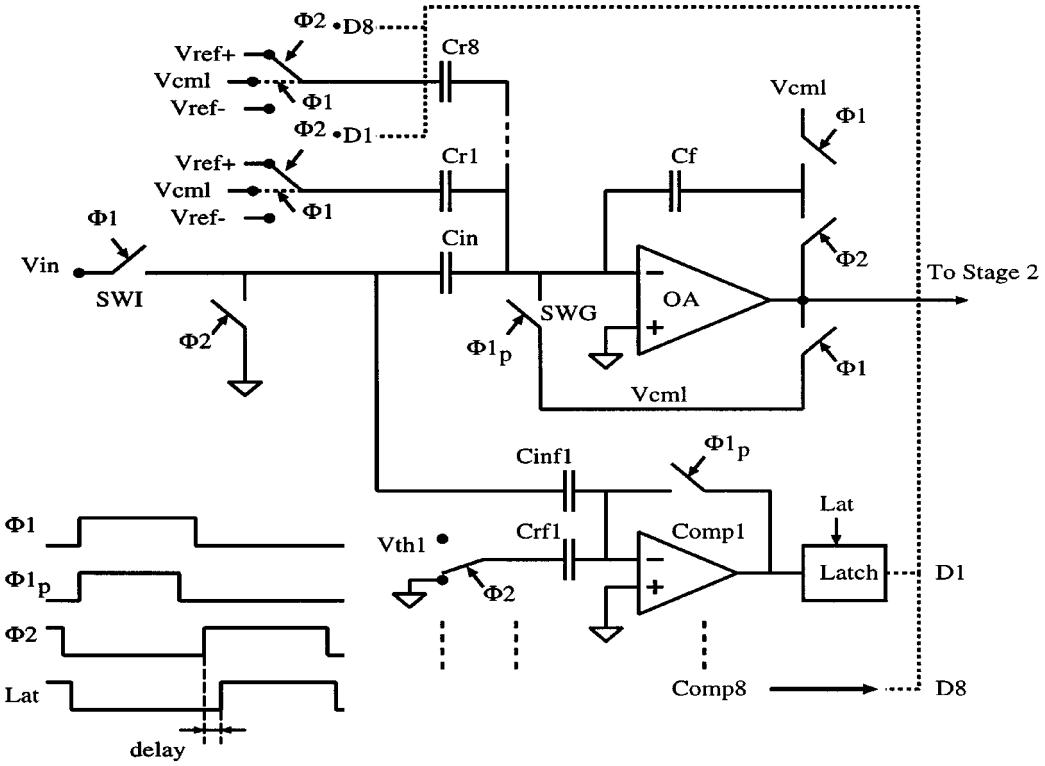

Fig. 4. Input sampling networks for the MDAC block and the flash comparator inside the first stage.

resolved) except for the first, which is 3 bit (two bits resolved), and the last, which is a 3-bit flash. This topology provided the best power consumption tradeoff taking into account the minimum capacitance value to achieve the desired noise floor (capacitors were scaled down the pipeline) and the power consumption of the comparators and the op-amps [17], [20]. The use of 1.5 bit for all stages of the pipeline has become increasingly popular [1], [8], [10], [19] mainly from a power perspective; however, this usually assumes a certain relation between the power consumption in the MDAC op-amps and in the comparators. Since in this design the comparators use a small amount of power, the first stage resolution was increased, thus reducing the accuracy requirements on subsequent stages. Consequently, bias currents and op-amp device sizes were also scaled down the pipeline, which results in significant power saving. The transfer functions for the first and the following stages are shown in Fig. 2. Also shown are the stage output bits sent to the digital alignment and correction logic. The first stage generates an extra bit based on an extra comparator in order to signal the overrange case. As mentioned before, the last stage of the converter is a 3-bit flash, and its most significant bit corresponds to the least significant bit of the 10-bit converter. The two least significant bits of the flash are used only to test the input-referred noise of the ADC (they improve grounded input noise measurement resolution). A 10-bit output code is finally generated with a five-clock cycle latency. Although not shown in Fig. 1, there

is also a bandgap-based generator, which provides the required reference voltages for the MDAC's and threshold voltages for the comparators.

Last, it is worth mentioning that reducing the power supply in a given CMOS technology does not necessarily reduce power consumption [2] in a predominantly analog IC, based on slewing currents inside the op-amps. However, going to a finer geometry CMOS technology (like 0.35 μm) might help for a particular input voltage range, since a significant portion of the op-amp settling can be linear. In this case, time constants $\tau = C/g_m$ dictate the power consumption. These τ's become smaller using a smaller CMOS technology, as presented in the Appendix.

III. Circuit Description

In order to capture high-frequency input signals, most converters, including pipeline ADC's, make use of a front-end SHA. Fig. 3 presents such a circuit [27]. The input voltage is sampled on capacitors $C_{\rm in}$ at the end of the track phase Φ_{1p}. During the hold phase Φ_2, the charge from $C_{\rm in}$ is transferred to feedback capacitors C_f such that the output is $V_{\rm out} = \frac{C_{\rm in}}{C_f} V_{\rm in}$. It can be noted that this circuit can accommodate single-ended inputs or, in general, a large input common-mode range, as opposed to the "flip-around" type of SHA [30]. Also, this circuit can provide voltage gain. Then, it can be reasoned that this sampling/gain operation can be moved inside the MDAC by adding appropriate "reference" capacitors that would help perform the DAC function. Consequently, the sampling operation at the input of the converter takes place in the MDAC and the flash comparators inside the first stage, as shown in Fig. 4. For simplicity, only a single-ended version is represented, although the implementation is fully differential. The MDAC op-amp and switching network is shown on top of one out of the eight flash comparators. During the track phase Φ_{1p}, both capacitors $C_{\rm in}$ and $C_{{\rm in}f1...8}$ are charged and track the input voltage. The sampling operation in the MDAC occurs when switch *SWG* opens on the falling edge of Φ_{1p}. The sample is taken relative to a common-mode voltage $V_{\rm cml}$ rather than around the op-amp. This does not cancel op-amp offsets, but it also does not require the op-amp to be stable in unity-gain feedback. Offsets at the input of this converter are not a problem for the majority of applications. The sampling operation inside the flash comparators occurs on the same falling edge of Φ_{1p}. At this time the comparator preamplifiers are also auto-zeroed, as shown in the figure. Separate reference capacitors ($C_{r1...8}$ in the MDAC and $C_{rf1...8}$ in the flash) are required to accommodate the input common-mode range. The reference voltages for the comparators are sampled on the falling edge of Φ_{1p} as well. At this moment, the input voltage $V_{\rm in}$ is sampled and available on $C_{{\rm in}f1...8}$, while corresponding reference voltages $V_{\rm th1...8}$ are sampled and available on $C_{rf1...8}$. After the rising edge of Φ_2, the difference $V_{\rm in} - V_{\rm th1...8}$ is sensed at the summing junction of the comparators. Meanwhile, the MDAC transitions to the amplify phase Φ_2 although the decision from the flash is not available yet. After a short delay (shown in Fig. 4 as *delay*) from the rising edge of Φ_2, which is necessary to allow the difference between the input and the references to be amplified inside the comparators, the latching signal *Lat* occurs and the decisions $D_{1...8}$ become available to the MDAC (after the latch regenerates). It can be inferred that this mode of operation requires both the comparator and the MDAC op-amp to be faster due to the absence of a dedicated SHA. The comparator needs to be faster in order to make its decision available without taking too much time away from the amplify phase of the MDAC. The MDAC op-amp needs to be faster due to the delayed flash decisions' reducing the amplify phase of the MDAC. All this means more power consumed in the first stage. However, the power saving due to the absence of the dedicated SHA more than compensates for this increase. Another drawback due to the distributed sampling operation is the need for separate reference capacitors $C_{r1...8}$, which contribute noise. They also contribute to the reduction of the feedback factor for the MDAC op-amp during the amplify phase.

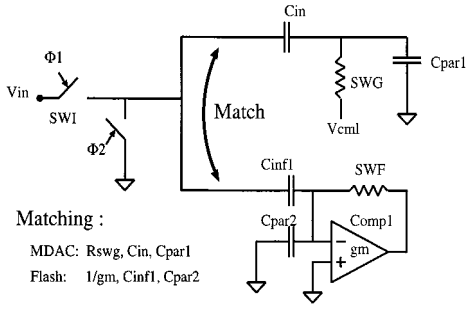

Fig. 5. Matching input networks for the MDAC and the flash comparators.

To avoid aperture errors, the sampling networks for the op-amp *OA* and for the flash comparators need to provide the same time constants relative to the input. This is shown in Fig. 5. The condition to be fulfilled is

$$\frac{C_{\rm in}}{C_{{\rm in}f}} = \frac{C_{\rm par1}}{C_{\rm par2}} = \frac{1/g_m}{R_{\rm SWG}} \tag{1}$$

where $C_{\rm in}$ and $C_{\rm inf}$ are the input capacitors for the MDAC and flash comparator, respectively. $C_{\rm par1}$ and $C_{\rm par2}$ are parasitic capacitors connected to the summing junctions. $R_{\rm SWG}$ is the on-resistance of the sampling switch in the MDAC, and g_m is the transconductance of the comparator preamplifier. Since $R_{\rm SWG} \approx \frac{L_{\rm sw}}{\mu_n C_{\rm ox} W_{\rm sw}(V_{\rm gs,sw} - V_{\rm th,sw})}$ and $g_m \approx \frac{\mu_n C_{\rm ox} W (V_{\rm gs} - V_{\rm th})}{L}$ are based on similar NMOS devices, it is possible to roughly match the sampling network (accurate matching is difficult due to $V_{\rm gs}$ difference and second-order effects like short channel and device output impedance). Assuming a full-scale sinewave at the input $V_{\rm in} = V \cdot \sin(2\pi f_{\rm in} t)$, the maximum slope is at the origin $\text{slope} = V \cdot 2\pi f_{\rm in}$. A mismatch in the time constant $\Delta\tau = \epsilon\tau$ results in a voltage error

$$V_{\rm error} = V \cdot 2\pi f_{\rm in} \tau \epsilon. \tag{2}$$

This error needs to be smaller than the correction range of the first pipeline stage, that is, $V_{\rm error} < V/8$ since the first stage flash contains eight comparators (the correction range can be also observed on the transfer function from Fig. 2). Since the timing signals used to control the sampling are generated inside a unique block, global timing jitter affects the overall converter noise floor but not $V_{\rm error}$ from (2). The input sampling networks are designed such that for the maximum input frequency $f_{\rm in} \cdot \tau <$

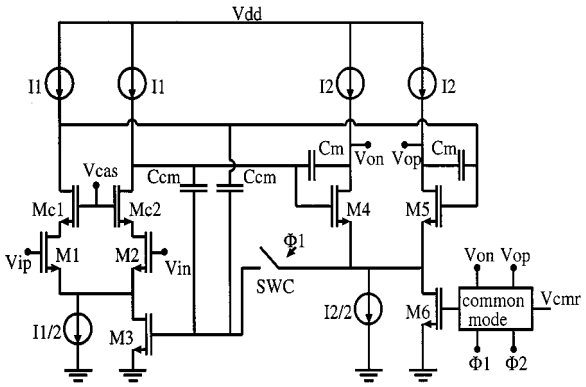

Fig. 6. The op-amp used to implement the switched capacitor DAC/gain block inside Stage 1.

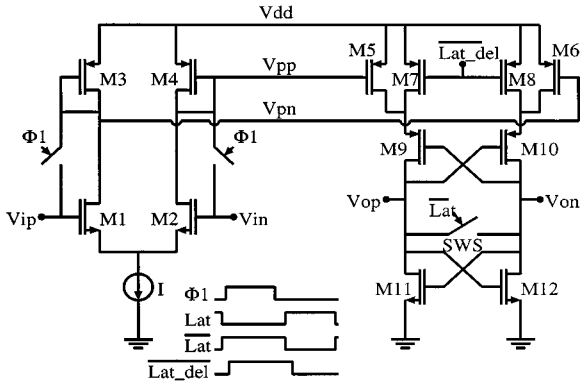

Fig. 7. Flash comparator circuit diagram.

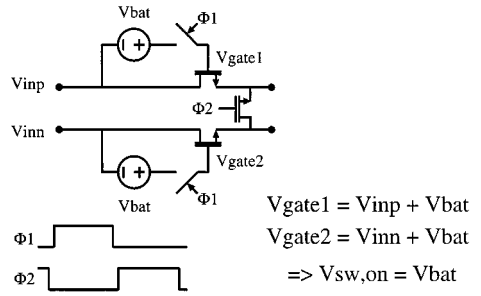

Fig. 8. Boosted input switches.

0.1. All this translates into a condition for the time constant error of

$$\epsilon < \frac{1}{2\pi \cdot 0.1 \cdot 8} \cong 0.2. \tag{3}$$

Even for a mismatch of 20% in the time constant, the converter would still generate correct data. Simulations showed that the aperture error is small enough to allow operation for input frequencies well above 100 MHz.

A simplified schematic of the MDAC op-amp is presented in Fig. 6. The signal path includes two NMOS differential pairs and Miller compensation capacitors C_m. The first cascoded (M_{c1}-M_{c2}) differential pair M_1-M_2 is presented with a PMOS current source (also cascoded) as a load and also drives the input gates of the second differential pair M_4-M_5. The tail current is provided to some extent by a fixed current source $I_1/2$ and the rest by the common-mode feedback ($3I_1/2$ flows through device M_3). During track mode when Φ_1 is high, switch *SWC* is closed and the common-mode feedback is closed around M_1-M_2 through M_4-M_5 and M_3. Thus, capacitors $C_{\rm cm}$ are charged to the appropriate value. During amplify mode, *SWC* is opened and the common-mode feedback loop is closed around M_1-M_2 through capacitors $C_{\rm cm}$, which looks like a typical switched capacitor common-mode feedback loop. A similar mechanism sets the common mode at the output of the op-amp $V_{\rm op}$ and $V_{\rm on}$ using device M_6. The unity-gain bandwidth of the op-amp in closed loop is designed for about 1 GHz worst case. The reason for using a two-stage topology is mainly the low power supply (min. 2.7 V) and the desire to preserve a large voltage swing at the output. Since the output stage can not be cascoded due to headroom constraints, a high-gain first stage is needed to provide for the overall accuracy requirement. The open-loop gain was about 90 dB from simulated results. The closed-loop bandwidth of the overall MDAC in amplify mode can be expressed as

$$\begin{aligned} \mathrm{BW}_{\rm closedloop} &= \mathrm{BW}_{\rm OA,unitygain} \cdot \beta \\ &= \frac{g_{m,M_{1,2}}}{C_m} \cdot \frac{C_f}{C_f + C_{\rm par} + C_{\rm in} + \sum_{i=1}^{8} C_{r_i}} \end{aligned} \tag{4}$$

where $g_{m,M_{1,2}}$ is the transconductance of devices $M1/M2$, C_m is the Miller capacitor in Fig. 6, C_f is the feedback capacitor, $C_{\rm in}$ is the input capacitor, $C_{r1...8}$ are reference capacitors from Fig. 4, and $C_{\rm par}$ is the parasitic capacitor in the summing junction of the MDAC including the op-amp input capacitance.

The first-stage flash comparators include a preamplifier followed by a latch, as presented in Fig. 7. The preamplifier consists of an NMOS differential pair driving a PMOS diode connected load, and the auto-zero function is performed around this circuit. The impedance of this preamplifier in closed loop is taken into account when matching the sampling network of the comparator to the one for the MDAC, as discussed earlier. Its output is applied to the latch (similar to the one described in [22]), which ultimately generates CMOS levels and drives the switches inside the MDAC block as shown in Fig. 4.

In Fig. 4, the input is presented to the DAC/gain block through a series switch *SWI*. This switch is of NMOS type having the gate driven by a boosted voltage, which is a result of the input's being summed with $V_{\rm dd}$ (power supply), as shown in Fig. 8. The circuit that provides the boosted gate voltage is similar to the one described in [1]. When high-frequency input signals are applied, the dynamic performance of the converter is improved by reducing the on-resistance and the nonlinear capacitance associated with *SWI*, and this is achieved using the boosted gate drive referenced above.

Next, a single-ended version of the 1.5-bit stage of the pipeline is shown in Fig. 9. According to the timing diagram in the figure, when Φ_2 is high and Stage 1 is in amplify mode, Stage 2 is in track mode and its input $V_{\rm in}$ is sampled on both capacitors C_2. Also $V_{\rm in}$ is presented to the comparators, which were auto-zeroed the previous half-cycle. The sampling of $V_{\rm in}$ occurs on the falling edge of Φ_{2p} relative to the common-mode level (switch *SWS* on the figure). When Φ_1 becomes high, one of the capacitors C_2 is flipped around the op-amp, and the amplified residue is presented to the next stage. Since the

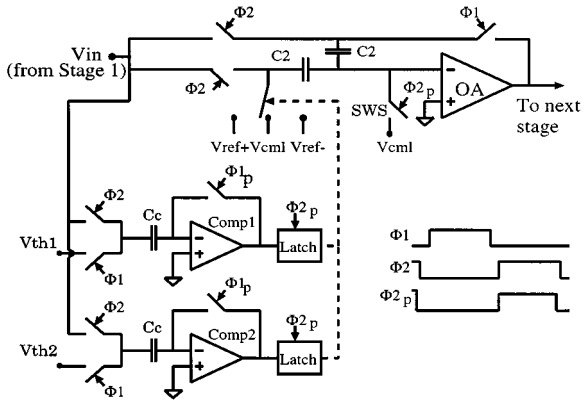

Fig. 9. The second stage (following stages are scaled versions) of the pipeline is a 1.5-bit stage.

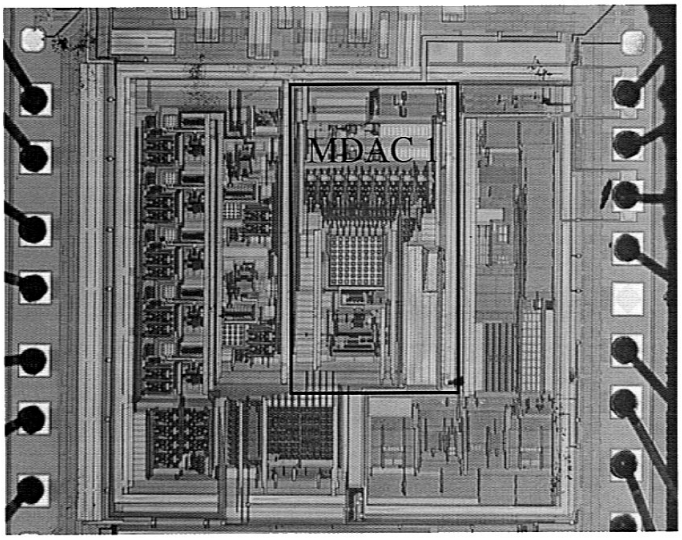

Fig. 10. Photomicrograph of the overall chip.

signal at the input of this stage is already held by Stage 1, no additional speed constraints on the op-amp or comparator are required. All subsequent stages have the same topology except the last stage, which is a 3-bit flash. Also, the stages are scaled down for power reasons going toward the back end of the pipeline.

IV. Layout and Measured Results

Fig. 10 presents the layout of the chip, which was implemented in a double-poly, triple-metal (DPTM) 0.35-μm CMOS technology and occupies an area of about 2.6 mm^2. The most critical component is the first pipeline stage, which is shown in the figure. On the right side lies the bandgap-based reference circuit, while on the left are the remaining pipeline stages and the correction logic. Dummy poly stripes were placed in the vicinity of the first-stage flash comparators to reduce offsets [6].

The power consumption of the converter is 55 mW, including the bandgap-based voltage reference, but not including the digital drivers. It increases to 70 mW overall with a 10-pF load on the digital outputs when sampling at 40 Msample/s and a 19-MHz input signal (basically Nyquist-rate operation). Power measurements were taken for a power supply of $V_{\rm dd} = 3$ V. The

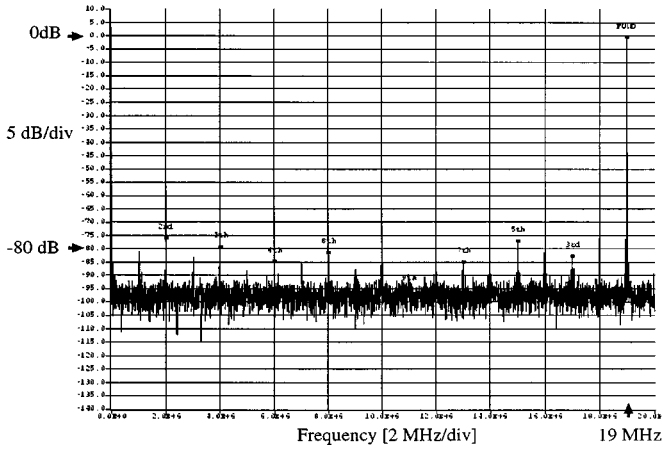

Fig. 11. A fast Fourier transform (FFT) plot of the output for a sampling rate $f_s = 40$ MHz and input $f_{\rm in} = 19$ MHz.

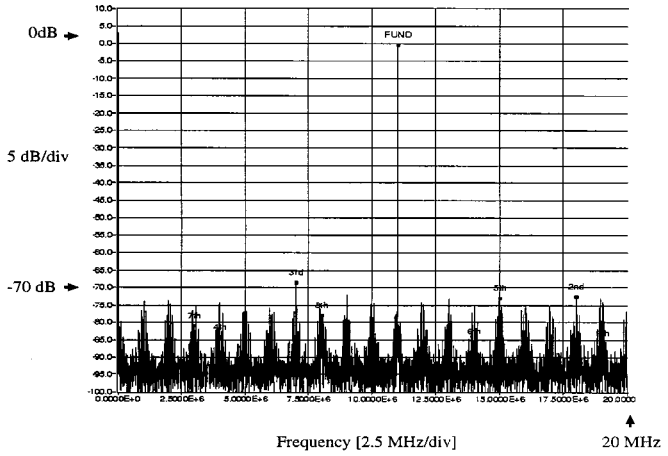

Fig. 12. An FFT plot of the output for a sampling rate $f_s = 40$ MHz and input $f_{\rm in} = 109$ MHz.

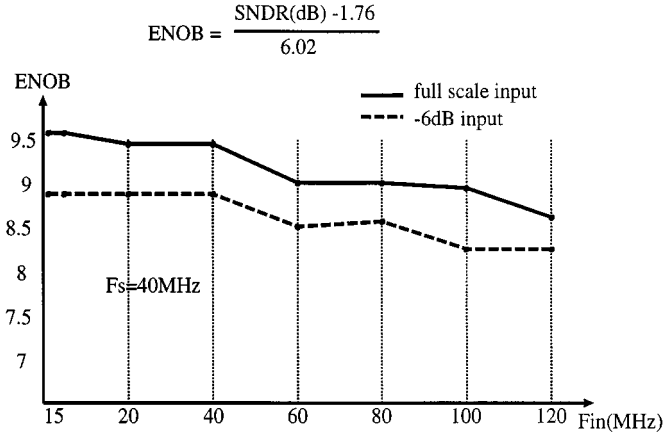

Fig. 13. ENOB plotted versus input frequency when sampling at $f_s = 40$ MHz.

input range of the converter is 2 Vpp (peak-to-peak) differential or single ended. All following ac measurements were done using differential inputs, whereas the low-frequency performance was obtained using a single ended input setup. The dynamic performance of the converter is presented in Fig. 11, where a full-scale input sinewave at $f_{\rm in} = 19$ MHz is sampled with frequency

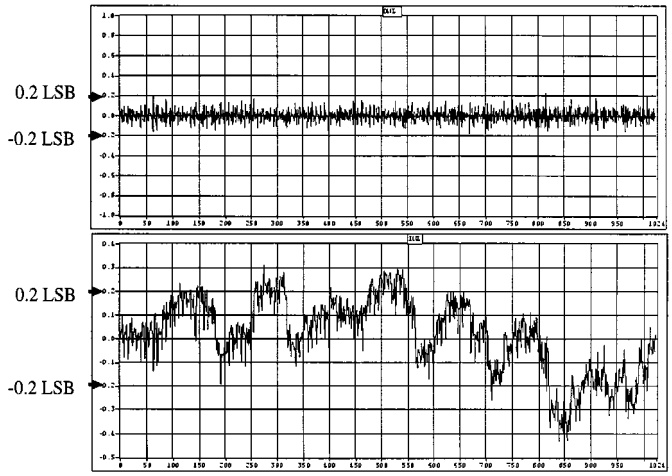

Fig. 14. DNL and INL plots obtained using a ramp at the input sampled at $f_s = 40$ MHz.

TABLE I
SUMMARY OF EXPERIMENTAL RESULTS

Resolution	10 bits
Input voltage range	2V peak-to-peak
ENOB ($f_{in} = f_s/2 = 20MHz$)	9.5
SNDR ($f_{in} = f_s/2 = 20MHz$)	59dB
SFDR ($f_{in} = f_s/2 = 20MHz$)	72dB
THD ($f_{in} = f_s/2 = 20MHz$)	-70dB
SNR ($f_{in} = f_s/2 = 20MHz$)	59.5dB
Input referred noise (2V full scale)	220μV
$\|DNL\|$ ($f_s = 40MHz$)	<0.3LSB
$\|INL\|$ ($f_s = 40MHz$)	<0.75LSB
Power cons. (core)	55mW (V_{dd}=3V)
Power cons. (10pF load)	70mW (V_{dd}=3V)
Technology	DPTM 0.35μm CMOS
Area	2.6 mm^2

$f_s = 40$ MHz. Other measurements corresponding to this plot are THD $= -70$ dB, signal-to-noise ratio (SNR) $= 59.5$ dB, and signal-to-noise-and-distortion ratio (SINAD) $= -59.2$ dB, which results in ENOB $= 9.55$. The converter can sample input frequencies beyond 100 MHz, as demonstrated by the plot from Fig. 12. Here, an input signal $f_{\text{in}} = 109$ MHz was applied to the converter sampling at the same 40 Msample/s. The other measurements corresponding to this plot are THD $= -65$ dB, SNR $= 56.5$ dB, SFDR $= -66$ dB, and SINAD $= 55.9$ dB, which results in ENOB $= 9$. The overall ac performance is summarized in Fig. 13 corresponding to typical conditions. For a fixed sampling rate $f_s = 40$ MHz, the input frequency is swept from 1 to 120 MHz for two cases. The ENOB corresponding to both a full-scale input represented by the solid line and a –6-dB input degrades gradually to 120 MHz. The performance degrades rapidly above 120 MHz. This overall performance indicates that the absence of a dedicated input SHA can be well compensated by matching input sampling networks for the MDAC and the flash comparator inside the first stage of the pipeline. Fig. 14 presents the low-frequency performance of the converter still clocked at 40 MHz. The differential (DNL) and integral nonlinearity (INL) improve even further ($|\text{DNL}| < 0.2\text{LSB}$ and $|\text{INL}| < 0.4\text{LSB}$) if the converter is clocked at a slower rate, which suggests a 12-bit level matching between the capacitors in Stage 1. Table I summarizes the performance of the converter. The input-referred noise was measured using the regular output of the converter plus the two additional bits from the last flash in order to improve histogram resolution.

V. CONCLUSION

We have implemented a 10-bit ADC in a 0.35-μm DPTM CMOS process, sampling at $f_s = 40$ MHz and showing ENOB > 9 up to $2f_s$. The design exhibits the lowest power figure reported to date for the given performance, particularly for high-frequency input signals. No dedicated input SHA is required since the converter performs well even in undersampled mode. Last, a 12-bit static matching was measured, which suggests that a low-power CMOS 12-bit pipeline ADC sampling at 40 MHz without calibration might be possible.

APPENDIX I

The closed-loop bandwidth of a CMOS op-amp used inside a SHA or an MDAC having a gain of C_{in}/C_f (as drawn in Fig. 3) can be related to the physical size of input devices of the op-amp. Assuming W/L for these devices, then

$$\text{BW} \sim \frac{g_m}{C_{\text{ox}}WL + C_l} = f_{(W)} \tag{5}$$

where $C_l = C_f + C_{\text{in}}$, g_m is the transconductance of the same input devices, and C_{ox} is the oxide capacitance. Using the fact that $g_m = \sqrt{2\mu C_{\text{ox}} I \frac{W}{L}}$, where μ is the mobility, the expression above can be maximized with respect to W. This maximum is attained when

$$W_{\text{opt}} = \frac{C_l}{C_{\text{ox}}L}. \tag{6}$$

Consequently, the maximum closed-loop bandwidth is achieved when $f_{(W)}$ is at a maximum, that is

$$\text{BW}_{\max} \sim f_{(W_{\text{opt}})} = \frac{\sqrt{2\mu C_{\text{ox}} I \frac{W_{\text{opt}}}{L}}}{C_{\text{ox}}W_{\text{opt}}L + C_l} = \frac{1}{L}\sqrt{\frac{\mu I}{2C_l}}. \tag{7}$$

From this expression, it can be seen that a lower L, which is equivalent to a smaller CMOS process, can yield a higher closed-loop bandwidth, providing that the mobility does not decrease too much. The current is assumed to remain the same (for slewing reasons).

ACKNOWLEDGMENT

The authors thank S. Ho for contribution to the design, K. Longo and J. Dispirito for contribution to layout, and M. Hughes and B. Odom for test end evaluation.

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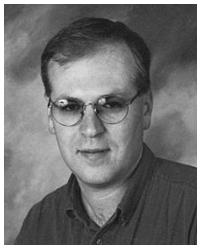

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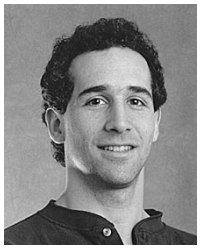

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