A High Bandwidth Constant g_m and Slew-Rate Rail-to-Rail CMOS Input Circuit and its Application to Analog Cells for Low Voltage VLSI Systems

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***Abstract*—A new rail-to-rail CMOS input architecture is presented that delivers behavior nearly independent of the common-mode level in terms of both transconductance and slewing characteristics. Feedforward is used to achieve high common-mode bandwidth, and operation does not rely on analytic square law characteristics, making the technique applicable to deep submicron technologies.**

From the basis of a transconductor design, an asynchronous comparator and a video bandwidth op-amp are also developed, providing a family of general purpose analog circuit functions which may be used in high (and low) bandwidth mixed-signal systems. Benefits for the system designer are that the need for rigorous control of common-mode levels is avoided and input signal swings right across the power supply range can be easily handled. A further benefit is that having very consistent performance, the circuits can be easily described in VHDL (or other behavioral language) to allow simulation of large mixed-signal systems.

The circuits presented may be easily adapted for a range of requirements. Results are presented for representative transconductor, op-amp, and comparator designs fabricated in a 0.5-μm 3.3-V digital CMOS process.

***Index Terms*—CMOS analog integrated circuits, comparators, operational amplifiers.**

I. Introduction

THE business of analog design in CMOS is becoming increasingly concerned with issues of signal headroom; power supply voltages for very large scale integration (VLSI) technologies are being driven down by the constraints of transistor breakdown limits, but threshold voltages are not scaling in proportion. Further, nonthermal noise levels due to large areas of associated digital circuitry are growing, and so signal swings must be maintained. Consequently, analog blocks with rail-to-rail inputs are becoming more important for mixed-signal audio and video systems designed in submicron CMOS. Large signal swings can, of course, be handled at amplifier inputs with virtual earth architectures, but the problem cannot always be sidestepped in this way. Voltage follower or noninverting amplifier configurations may be unavoidable, or comparator references may vary widely in operation; true rail-to-rail input range is then essential. Note that it is not sufficient to have good virtual earth performance available over a slowly varying range of common-mode values; it is also important that the common-mode response is available over the full required bandwidth.

For large scale mixed-signal IC's, there is also the issue of system-level design and simulation. VHDL or other behavioral languages are now widely used for the digital description and as a basis for synthesis, and thus where a system has both analog and digital functions entangled in a complex way, it is highly desirable to be able to simulate the entire system and verify functionality. Having achieved this, the logic part of the VHDL may be separated from the analog and synthesized, with a high confidence that the entire system will operate as intended. For this approach to work, it is clearly necessary to have accurate behavioral models of the analog cells; most conventional circuits present a quite complex performance envelope, and even a simple single-sided op-amp is not so easy to describe comprehensively for all common-mode input ranges.

Against this background, the work here describes the development of a family of basic analog cells which attempts to solve these problems. We require amplifiers and comparators whose basic behavior closely resemble the ideal "textbook" descriptions, and which can maintain this behavior for any terminal voltages within the power supply range. Thus, the system-level designer can assemble quite complex signal flows without having to constrain analog references and signal ranges and can confidently and quickly model the whole system in a behavioral simulation. Particularly where time-to-market is a high priority, the small penalty in a marginal increase in area and power consumption may be easily justified.

II. Circuit-Level Requirements for a Rail-to-Rail Architecture

In order to address the need for a set of general purpose circuit cells, one should consider the central requirements and what are the common problems (Fig. 1). For an op-amp with general rail-to-rail capability, the output stage is not a great obstacle. Simple class-A or class-AB designs can drive loads close to (if not right up to) power supply rails. The key problems lie at the input stage, and the classic two-stage architecture therefore demands a rail-to-rail transconductor function. Further, this transconductor should ideally have both constant g_m and limiting current so that unity gain bandwidth

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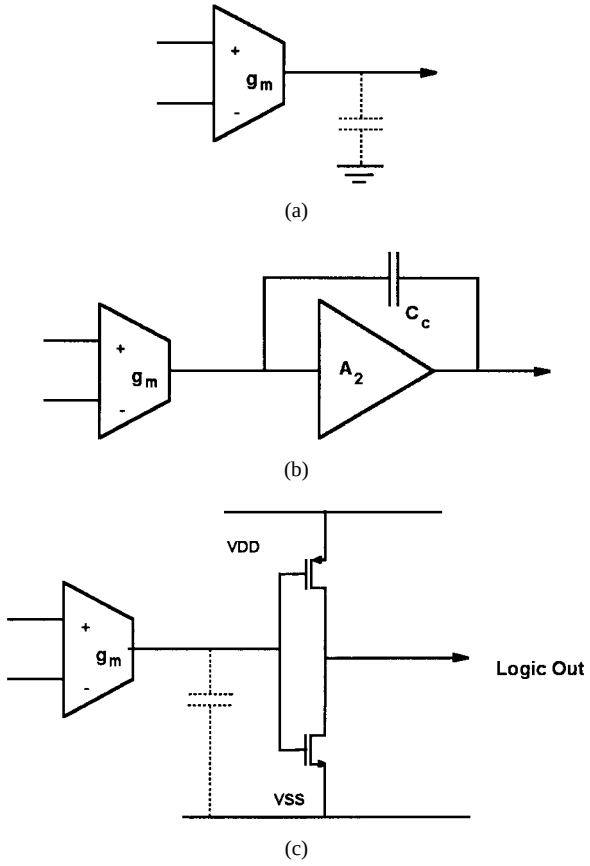


Fig. 1. Circuit configurations based on transconductor core.

and slew-rate are both maintained over the full common-mode input range.

An asynchronous comparator is also easily constructed using a transconductor as its core. A simple logic inverter is usually placed at the output of the stage. The output current is integrated on the parasitic input capacitance of the inverter, and when sufficient voltage change occurs at this internal node, the logic output changes. Clearly, both the large and small signal behavior of the transconductor affect the response time of the complete comparator, and consistency with common-mode variation is desirable.

Lastly, a transconductor is useful in its own right, as a feedback element in control loops (such as dc-level clamps) or as a filter element. Again, both the small signal g_m value and the limiting current should be consistent over the input range for maximum flexibility and ease of system design.

Hence, effort should be focused on the design of a transconductor with rail-to-rail input capability and near constant large and small signal behavior. Note that with technology scaling, the familiar square law MOS model [1] is increasingly limited in its applicability; to be useful in modern submicron CMOS, the circuit should not rely on precise square law device characteristics.

III. Existing Rail-to-Rail Architectures and Their Limitations

A simple rail-to-rail input can be easily constructed as a composite of p and n-channel differential pairs [2] (Fig. 2),

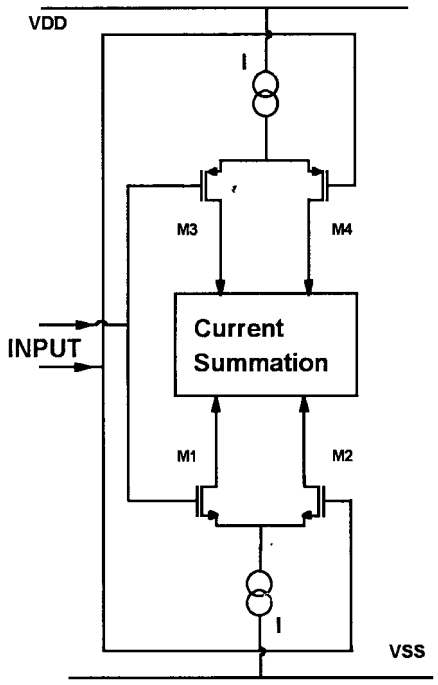


Fig. 2. Simple rail-to-rail architecture with p and n-channel differential pairs.

but this suffers from two drawbacks. First, at the extreme input ranges, only one input pair is active, and so the effective transconductance is halved. Second, the large signal output current is also halved. When used in a conventional two-stage amplifier, this means that both the unity-gain bandwidth and slew-rate will be a function of common-mode input.

Stabilization of the total g_m over the common-mode range can be tackled by varying the effective tail current in the active differential pair, so that its g_m doubles when the other is inactive. A simple way of achieving this is to increase the tail current bias on each side by a factor of four, and to add additional devices inside each differential pair which have a width three times that of the active devices [3] (Fig. 3). Thus, in normal operation, 75% of the tail current is diverted through the center path, leaving the active devices with the nominal tail current of I. This implies a four-fold current increase in the effective tail current, and so if square law operation is valid, g_m will double, making good the deficit caused by the inactive pair. However, this extra tail current also adds to the large signal limiting value, and hence the slewing value doubles from $2I$ to $4I$.

An alternative technique is to sense that one of the pairs has lost sufficient gate bias to operate and to divert the unused tail current through a bypass transistor, biased at a minimum active level [4] (Fig. 4). When current flows through this path, it activates a current mirror of the opposite polarity which has a ratio of $1:3$. Hence, an additional current of $3I$ is added to the active pair's tail, raising the operating current to $4I$. Again, with square law operation, this doubles the g_m in the active pair, restoring the active g_m to its mid-range value. Also in common with the first scheme, there is a doubling of the maximum slewing current from $2I$ to $4I$. The use of such feedback loops for this current control is unsuitable for

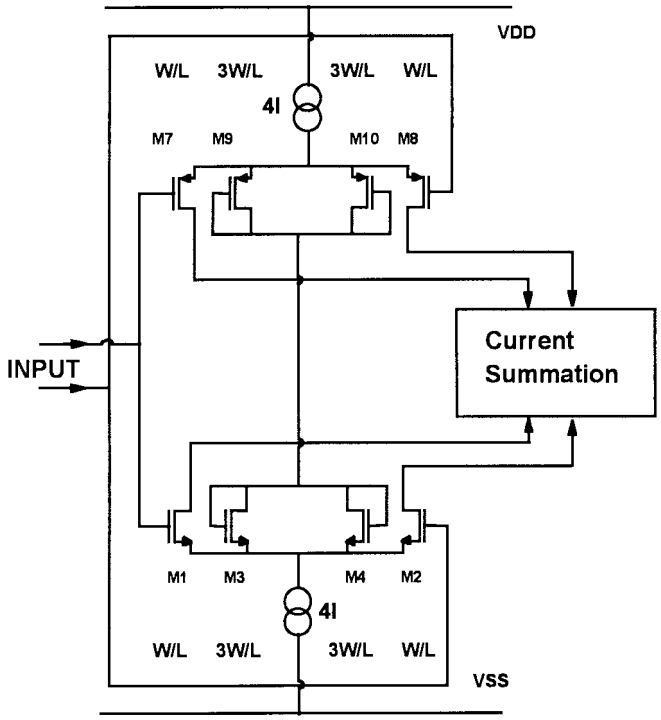


Fig. 3. Rail-to-rail architecture with tail current diversion giving near constant g_m.

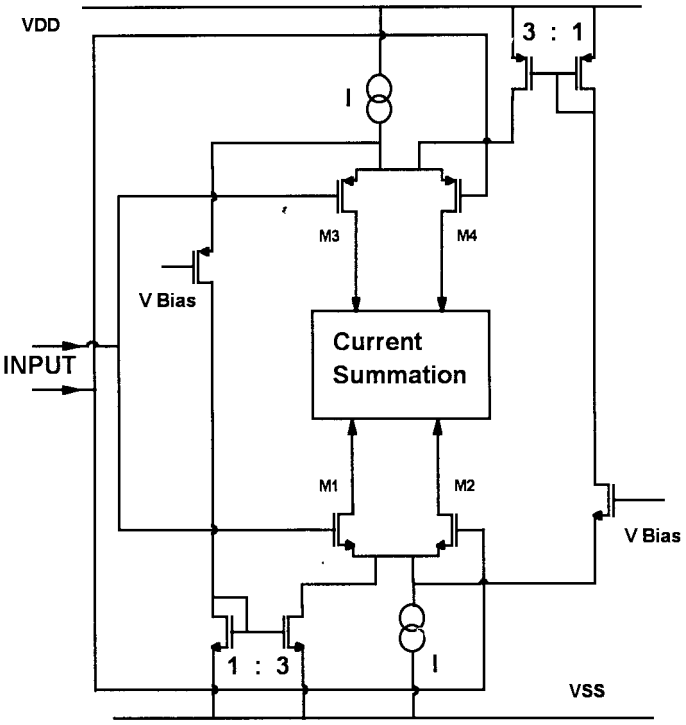


Fig. 4. Rail-to-rail architecture with tail current multiplication by 1:3 mirrors giving near constant g_m.

high frequency applications due to the loop bandwidth limits (due to the nonunity current mirrors etc.), and also gives rise to rather sharp steps in g_m. Other approaches include: controlling the sum total V_{GS}-V_T in the two pairs by current steering, and hence regulating the total g_m [5]; the use of bias loops to maintain the sum of the square-roots of the tail currents constant [6]; and controlling the sum of the roots of the tail currents scaled by the prevailing on-chip n and p-channel transconductances [7]. As well as relying on a long-channel square law device model, these all still result in slewing current variations.

IV. New Rail-to-Rail Input Structure

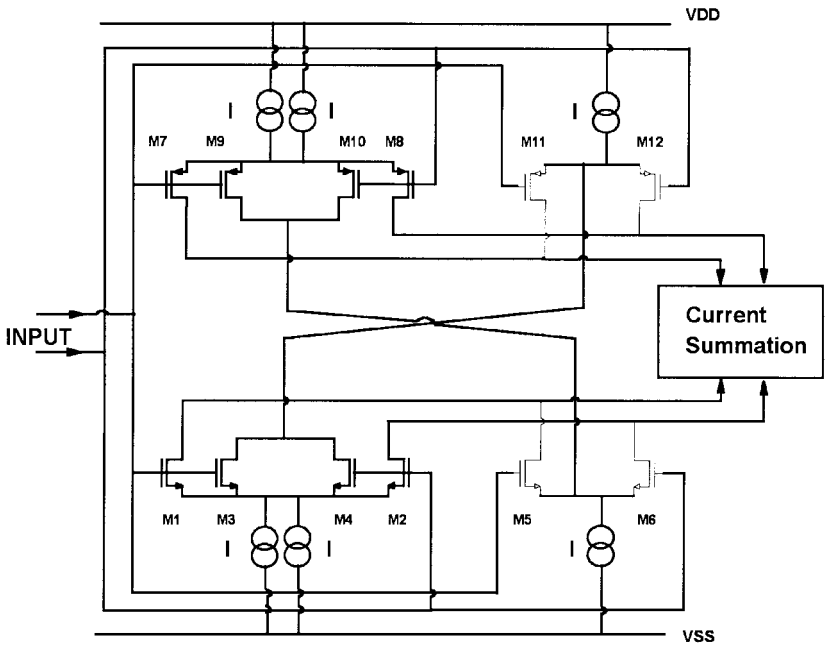
A new input structure has been developed which attempts to meet the objections to the abovementioned techniques. Certain guiding principles underlie the design approach.

First, to achieve rail-to-rail input range, in common with almost all previous designs, a combination of n and p-channel differential pairs is used with geometries scaled so that the nominal g_m values are the same. This arrangement brings with it certain limitations. Clearly, the matching of the two g_m values will be subject to process and temperature tolerances; in the process used, these can be expected to vary by less than $\pm 5\%$. Further, the offset voltage for each part of the input will vary depending on which components are active. Hence, a periodic signal, whose precise form will vary from device to device, will appear in series with any applied input signal, leading to harmonic distortion. This effect is unavoidable in absolute terms, but can be kept manageable by selecting device gate areas to keep the random offset due to each pair small [8]. This clearly places some restriction on the applicability of the circuit for ultra-low distortion systems, e.g., hi-fi audio.

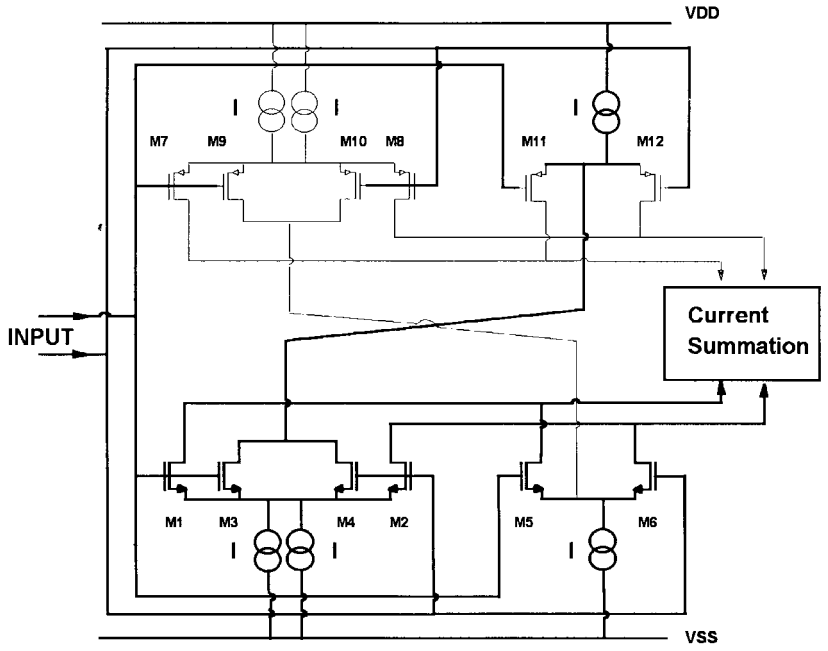
Second, to achieve a constant transconductance over the whole input range without relying upon the MOS devices' g_m/I_D characteristics, the condition must hold that the sum of the device current densities contributing to the output are maintained constant. Third, to achieve a constant limiting current, the sum of the contributing large signal currents must also be constant. Finally, since it is vital that the time response to common-mode level changes is not a restriction, feedforward techniques are preferred to feedback to achieve the required characteristics.

The function of the circuit can be explained easily with reference to Fig. 5(a)–(c). A total of three differential pairs of each polarity are used in different configurations: all the p-channel differential pairs are of identical width and length; similarly, all the n-channel differential pair transistors are identical. The p and n-channel geometries are in the ratio of the nominal unit transconductance parameters, as outlined above. The current sources on each side of the structure are all of unit value, and can be simple single transistor designs.

Fig. 5(a) shows the circuit with the common-mode input at a midrange level. Both the n and the p-channel devices have sufficient gate bias to operate. In the n-channel circuitry, both $M1$ and $M2$ contribute signal current, with a transconductance set by half the total tail current available, i.e., I. The other half of the tail current, I, is diverted by $M3$ and $M4$, since they are of equal size, and have the same mean gate-source voltage. This diverted current in turn draws the tail current I away from the p-channel pair $M11$ and $M12$,



(a)

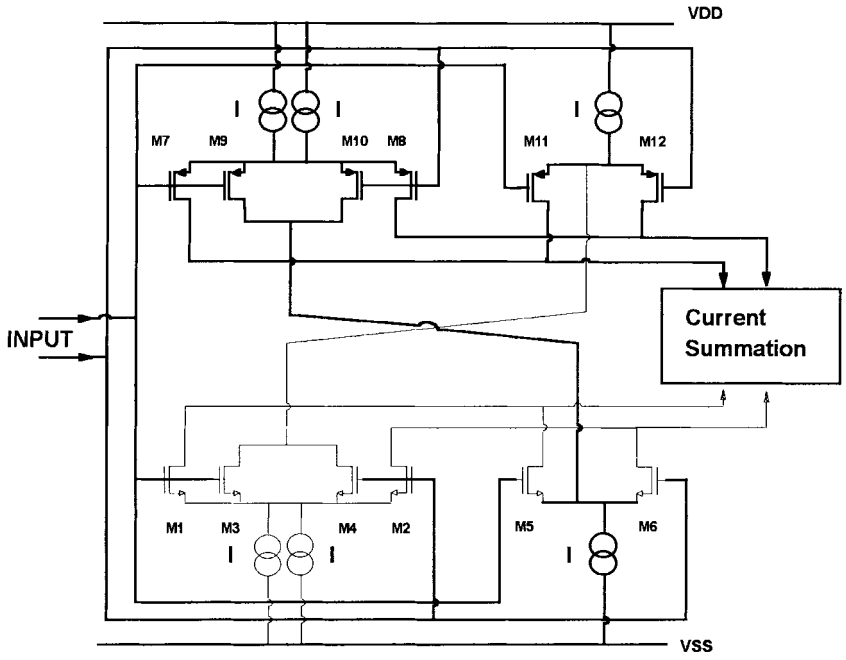


(b)

Fig. 5. New rail-to-rail architecture. All p-channel W/L are identical, and all n-channel W/L identical, with W/L(n): W/L(p) = uCox(p): uCox(n). Highlighted parts show active signal paths. (a) Signal paths with midrange common-mode values; n and p differential pairs active. (b) Signal paths with high common-mode values; only n differential pairs active.

switching them off. On the p-channel side, Both $M7$ and $M8$ contribute signal current, again with an operating current of I. The other half of the current available, also I, is diverted by $M9$ and $M10$, since they have the same geometry and share the same gate-source voltage as $M7$ and $M8$. This current is sunk by the source attached to $M5$ and $M6$, so that the latter n-channel devices are held off. Hence, only four devices $M1, M2, M7$, and $M8$ are contributing signal current, each with a nominal unit g_m value. There is also a total of $2I$ available at the current summer for the limiting current.

Fig. 5(b) shows the situation with a high common-mode level. In this case, none of the p-channel transistors have sufficient gate-source voltage to remain active. With no other path, the current sources supplying $M7-10$ collapse and turn off. Now, the tail current source attached to $M5$ and $M6$ is not supplied from elsewhere, and these transistors become active and contribute signal current to the output. The current



(c)

Fig. 5. (*Continued.*) New rail-to-rail architecture. All p-channel W/L are identical, and all n-channel W/L identical, with W/L(n): W/L(p) = uCox(p): uCox(n). Highlighted parts show active signal paths. (c) Signal paths with low common-mode values; only p differential pairs active.

diverted by $M3$ and $M4$ is still of value I, and this is still supplied by the source attached to $M11$ and $M12$. $M1$ and $M2$ remain active and contribute signal as before, still with a tail current of I. Hence, the total output is again supplied by four transistors, $M1, M2, M5$, and $M6$, all operating with a nominal unit transconductance, and the total current available in the limiting case is still $2I$.

Finally consider Fig. 5(c). The input is now at a low level, and all of the n transistors are off due to lack of gate bias. Consequently, the current sources supplying $M1$–$M4$ collapse, and so the current source attached to $M11$ and $M12$ no longer flows past these devices. Hence, they become active and contribute signal current. $M9$ and $M10$ remain on, and send half the total tail current, I, to the source attached to $M5$ and $M6$, which itself can remain active. Thus, $M7$ and $M8$ still contribute signal with nominal g_m and have available I in the limiting case. Hence, there are still four transistors contributing with nominal unit g_m values and there is still just $2I$ available in the limiting case.

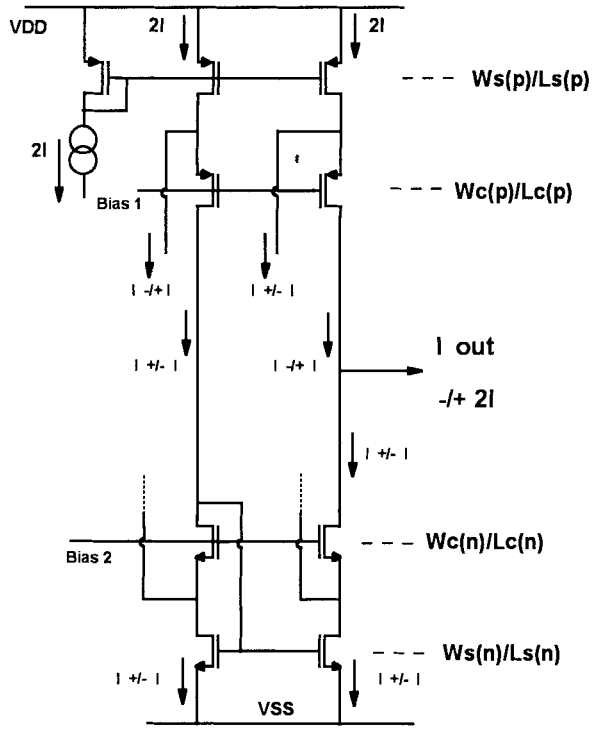
From the above discussion it can be seen that there is no requirement for any precise analytic relationship between drain current and transconductance, and the circuit is thus applicable to a variety of device characteristics. This is particularly important as it makes the circuit useful for deep submicron CMOS technologies, where the region of bias between weak inversion and velocity saturation is very limited, and ideal square law characteristics are not realistic [9]. The influence of a particular relationship between g_m and I_D will only be evident in the narrow transition regions where one set of devices is turning off and another turning on. Hence, with some deterioration in the ratio between g_m and I_D in a device affected by velocity saturation, there will be a slightly more noticeable ripple in the transconductance versus common-mode voltage, but no adverse effects in the center or the extreme ranges.

V. Complete Transconductor Design

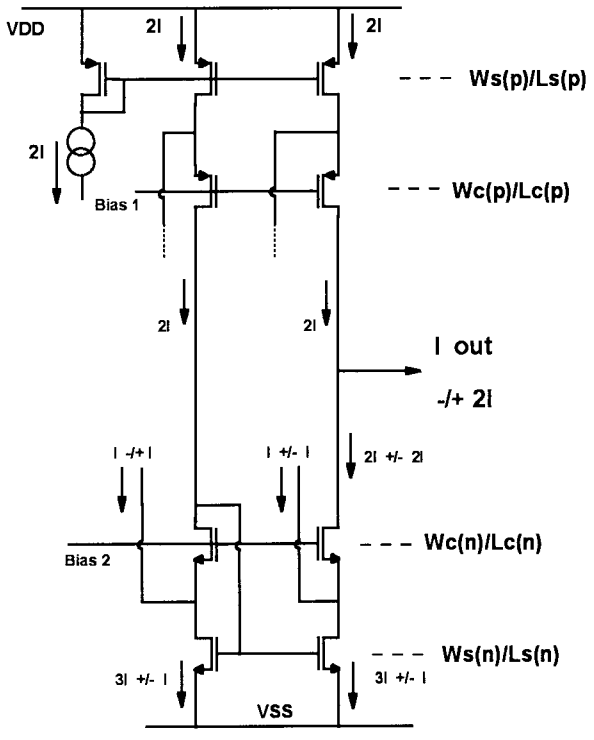
A. Input Stage

The dimensioning of the input stage itself is very straightforward. Input transistor sizes are chosen in the normal way to give the required transconductance with the specified nominal tail current, taking into account the compromise between offset, total input capacitance, noise, etc. The n and p dimensions are ratioed to give the same nominal transconductance in each polarity. As mentioned earlier, the ripple in the transconductance as a function of the common-mode input will be a weak function of the devices' gate bias, and operation with very strong velocity saturation will give increased error.

Tail currents can be single devices or cascodes. It should be noted that in the transition regions, the common source nodes of $M5$ and $M6$, and $M11$ and $M12$ can experience some significant voltage excursion, due to any mismatch between the n and p channel current sources presented at these points during high impedance conditions. This can be cured by making the current source resistances more modest, or by dimensioning the sources supplying $M5$ and $M6$ and $M11$ and $M12$ to be slightly greater than the nominal value used for the other pairs. In many applications, small fluctuations of total output current due to the limited output conductance of simple sources are quite acceptable.



(a)



(b)

Fig. 6. Current summation circuit—extremes of operating conditions: (a) high-range condition: only n-channel pairs active and (b) low-range condition: only p-channel pairs active.

B. Current Summer

The current summation must be performed with a few basic restrictions. First, it should not impose any headroom constraints on the input structure, in the way of forcing input transistors into triode region. Second, it should be high bandwidth, so as not to degrade significantly the common-mode and differential-mode bandwidth (and avoid undesirable parasitic poles when used in an op-amp configuration). Finally, the output range should be as large as possible to approach the ideal overall transconductor function. The circuit adopted in this work is a composite current mirror and current source arrangement [4]. Where speed is of the essence, the circuit should be configured with the current mirror on the n-channel side. However, the compliance degrades most on the current mirror side; for the target application in question, consistent performance was needed close to V_{SS}, and so the circuit was reversed to place the mirror on the p-channel side.

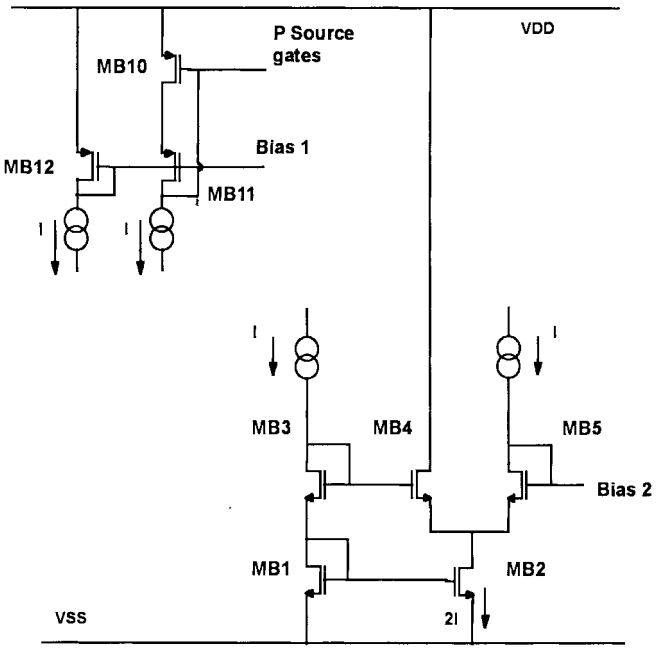


Fig. 7. Bias circuitry for current summer—n-channel mirror version. (For current summer with p-channel mirror, reverse all device polarities.)

One of the most critical parts of the whole design is the biasing of the cascodes in the current summer, particularly on the mirror side [10]. The cascode must operate with a value of V_{Dsat} which is less than the operating value of V_T, otherwise saturation is not maintained. The gate bias of the mirror cascode must also be set so as to accommodate large variations in large signal current. The restrictions are shown diagrammatically in Fig. 6(a) and (b), which show the most stringent limitations under extreme input conditions.

In Fig. 6(a), the input common mode is high, and the p-channel inputs are taken to be off. Now, there is no current injected directly into the n-channel mirror, and the current applied at the p folding cascodes is $\pm I$ (where I is again the unit tail current). Hence, the cascode devices must be biased so that with a maximum current of $2I$ flowing, saturation conditions are maintained. Setting ***Bias1*** too low reduces headroom for the input. Any of several classical bias schemes is quite adequate for the folding cascodes section, noting that the cascodes will probably be of shorter-channel length than the sources [i.e., Lc(p) $<$ Ls(p)] for good bandwidth. Fig. 7 shows the circuit used.

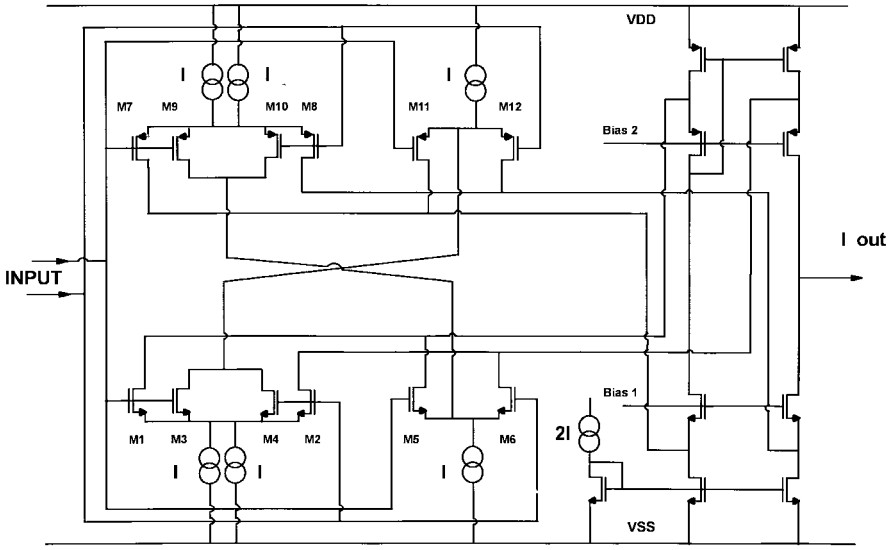


Fig. 8. Complete transconductor (without bias).

Turning to the mirror cascodes, one can see that the current level which passes through the mirror under these conditions can be in the range 0–$2I$. To maintain saturation as the currents fall close to zero, ***Bias2*** must lie in the range

$$V_{T0} < Bias2 < V_{T0} + V_{T2} \tag{1}$$

where V_{T2} is the effective threshold for the cascode's source potential. The other extreme is shown in Fig. 6(b), where the input common-mode level is low. Now, the only the p-channel inputs are active, and the current in the mirror transistors can vary in the range $2I$–$4I$. At the maximum current, the value of ***Bias2*** must now be in the range

$$V_{T2} + \sqrt{2}(V_{Dsat(c(n))} + V_{Dsat(s(n))}) < Bias2 < V_{T0} + V_{T2} + \sqrt{2}(V_{Dsat(c(n))} + V_{Dsat(s(n))}) \tag{2}$$

where the subscripts $c(n)$ and $s(n)$ refer to the n-channel cascodes and sources, respectively. Note that one can use square law approximations here, since as will be seen, bias levels are necessarily quite low. From (1) and (2) one can see that to satisfy all operating extremes the following conditions must hold:

$$\sqrt{2}(V_{Dsat(c(n))} + V_{Dsat(s(n))}) < V_{T0} \tag{3}$$

and thus

$$V_{T2} + \sqrt{2}(V_{Dsat(c(n))} + V_{Dsat(n))}) < Bias2 \leq V_{T0} + V_{T2}. \tag{4}$$

In practice, the range allowed by (4) is quite small if devices are to be kept in strong inversion, and the value of ***Bias2*** should be set quite close to the upper bound.

Fig. 7 also shows the mirror bias in n-channel form; the circuit is related to a well-known high compliance cascode bias network [11]. In this version, we match the length and current densities in MB1 and MB2 to the mirror source devices, and the length and current density in MB5 to that in the cascodes. Hence, to be able to set

$$V_{Bias2} \approx V_{T0} + V_{T2} \tag{5}$$

TABLE I
BIAS NETWORK DIMENSIONS (FIG. 7)

Bias Device	Relative Width	Relative Length
MB1	Ws(n)/2	Ls(n)
MB2	Ws(n)	Ls(n)
MB3	Wc(n)/2	Lc(n)
MB4	∼Wc(n)/18	Lc(n)
MB5	Wc(n)/2	Lc(n)
MB10	Ws(p)/2	Ls(p)
MB11	Wc(p)/2	Lc(p)
MB12	∼Wc(p)/12	Lc(p)

we require that at the drain of MB2 the voltage is

$$V_{D(MB2)} \approx V_{T0} - V_{Dsat(c(n))}. \tag{6}$$

This is achieved by matching MB3 to the cascodes (as MB5) so that

$$V_{MB3} = V_{T0} + V_{Dsat(s(n))} + V_{T2} + V_{Dsat(c(n))} \tag{7}$$

and then dimensioning the width of MB4 so that its ***ON*** voltage is equal to $2V_{Dsat(c(n))} + V_{Dsat(s(n))}$. With saturation voltages similar in the sources and the cascodes, this implies a current density around nine times that in MB3. The bias network transistor dimensions are summarized in Table I. These calculations are obviously approximate, but small errors can be easily removed in simulation with minor width adjustments to MB3 and MB4. Power can also be saved by judicious scaling of the currents in proportion to the nominal tail current $\boldsymbol{I}$.

The complete transconductor cell is shown without bias in Fig. 8.

VI. COMPARATOR DESIGN

As outlined in Section II, a transconductor cell may be used as the basis of an asynchronous comparator. The basic architecture given in Fig. 1 is not, however, ideal. The response time of this basic configuration appears to be a function of the transconductor part's g_m (for small inputs) and the

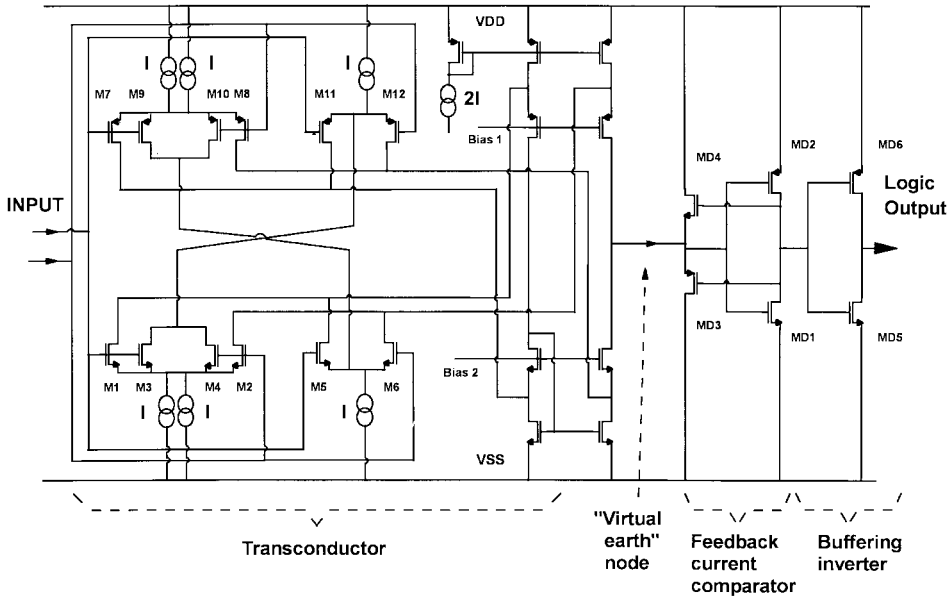


Fig. 9. Complete asynchronous comparator circuit (excluding bias).

slewing current (for large inputs), together with the parasitic capacitance seen at the input to the inverter (which is used as a current integrating comparator). Since the inverter capacitance can be very small, the response time would appear to be fast, even for small inputs. The problem lies not with the response starting from a balanced equilibrium condition, but rather with the consequences of a previous decision.

When an input is applied for any length of time, a decision will be made, but the inverter input node will continue to move to the point that the cascode transistors on one side will fall out of saturation, and eventually, so will the current summer sources. Now, even with a large input signal reversal, the gate and source body capacitances in the current summer cascodes can only be recharged with a current of $2I$ at most. If the reversal is modest, then a much smaller current will be available. Until these capacitances have been restored to the active operating state, there can be no valid current output to the inverter. Consequently, the decision will be greatly delayed.

To avoid these problems, the inverter is replaced with a feedback current comparator network [12], as shown in the context of the complete comparator schematic, Fig. 9. In addition to the basic inverter MD1 and MD2, two source followers MD3 and MD4 provide a feedback path to the input node. In this application, it is this feedback which makes the circuit particularly useful.

When the current comparator output is somewhere between logic levels, there is not enough gate bias to turn on either of the source followers, and the circuit has a high impedance input. Any input current is thus integrated as with a normal inverter. However, once there has been some excursion from the inverter's balance point, its gain produces a larger inverted output excursion, which quickly becomes large enough to turn on either MD3 or MD4. Current is thus fed back to the transconductor output so as to balance that being delivered. Consequently, the action of MD3 and MD4 is to provide an automatic clamp for the transconductor, maintaining the current summer devices in their normal active conditions, and hence there is no significant recovery delay present for a decision of either polarity.

At the output of MD1 and MD2, the voltage excursion will be $+V_{TN}/-V_{TP}$. Although not a rail-to-rail logic swing, this is more than enough to drive a subsequent inverter, MD5 and MD6. Dimensioning of the complete design is relatively straightforward. The response time of the complete comparator will clearly depend on the g_m value and limiting current of the transconductor section, since this controls the charging time of the capacitances. Devices MD1, MD2, MD5, and MD6 can be minimum logic inverter sizes (i.e., with scaling for p and n-channel gain). The feedback transistors MD3 and MD4 should be minimum length but wide enough to pass the transconductor's limiting output current for a relatively small gate drive (less than say 0.5 V) under all conditions. Note that both MD3 and MD4 experience significant body effect, and hence can set the lowest supply voltage at which the circuit can maintain performance if not chosen with a little care.

VII. Operational Amplifier Design

In Section II it was also noted that the transconductor core can be used as the basis for a conventional two-stage op-amp. The simplest approach is to add standard class-A output stage, which can achieve close to rail-to-rail drive if biased judiciously and will not add significant distortion at high frequencies, albeit at the expense of power consumption. For the target application, video bandwidth buffers were needed with the capability to operate as a voltage follower with near rail-to-rail signal range, while driving resistive loads in the kΩ range. Fig. 10 shows the complete scheme (without bias circuits).

Generally, the design procedure follows the normal pattern. In this application, noise and offset demands were not very stringent, but these can be addressed in the usual way with

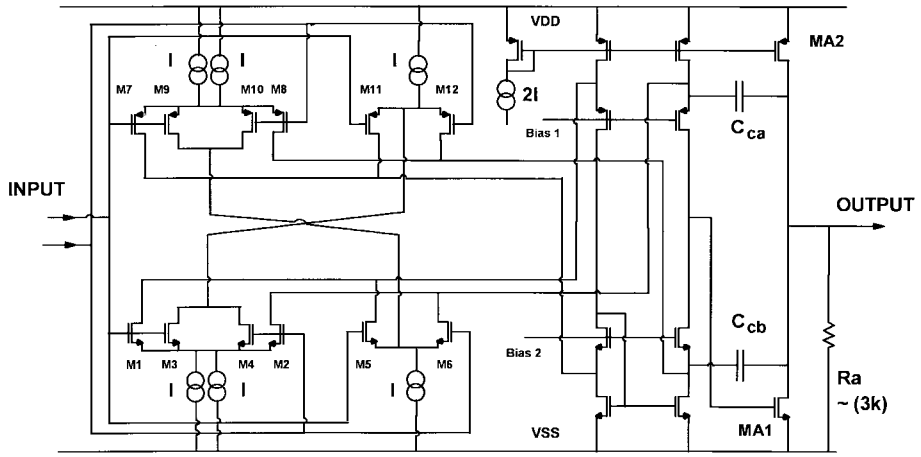


Fig. 10. Video bandwidth op-amp circuit (excluding bias).

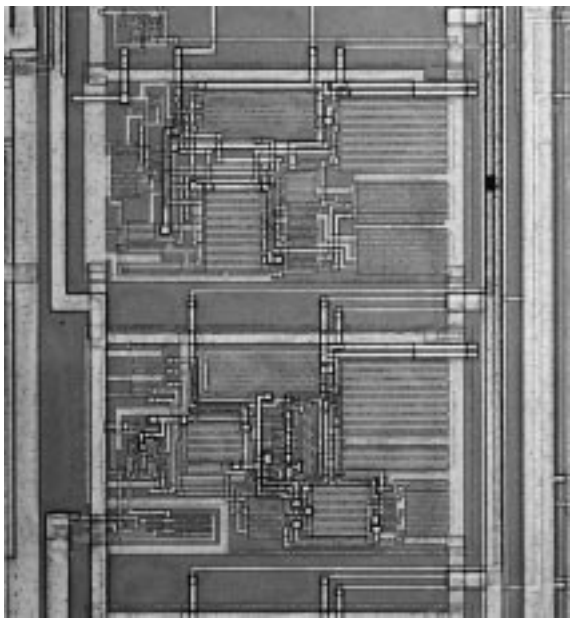


Fig. 11. Microphotograph of transconductor and comparator cells, embedded in video processor IC.

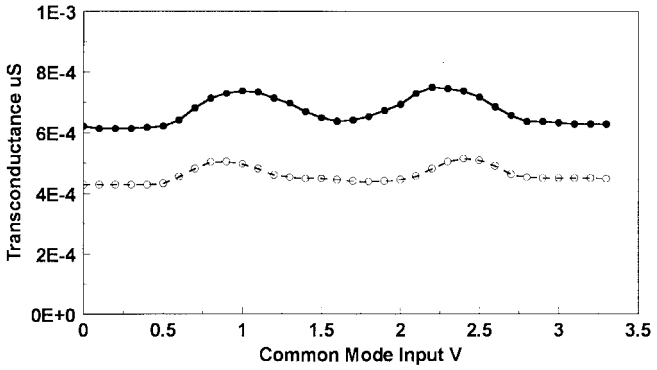


Fig. 12. Measured transconductor g_m versus input common-mode level ($V_{DD} = 3.3$ V; output level $= V_{DD}/2$).

device area. An n-channel output driver is used with a p-channel current source, mainly to optimize the signal swing for regions close to V_{SS}, and to keep the area limited. The output stage runs at about 1.5 mA to get a low enough resistance and adequate slewing into the load envisaged. The resistor in parallel with the output provides some stabilization of the output pole position under large signal conditions and also helps slightly with pull-down close to V_{SS}. Another feature which helps the large signal behavior is the splitting of the compensation capacitor in two and feeding back via the current summer cascodes [13] (for right-half-plane zero cancellation). This means that during slewing conditions, when one or other cascode paths may be cut off, there is always some compensation preventing transient instability.

VIII. Experimental Results

Fig. 11 is a microphotograph of the comparator and transconductor cells embedded in a video processing chip. The area of each cell is approximately 0.04 mm^2 in the 0.5-μm three-metal CMOS process. The comparator cell is the lower of the two, with the small current comparator section at the bottom left.

A. Transconductor Results

The circuit fabricated was virtually identical to that shown in Fig. 8, except that the current summer and its associated bias were of the opposite polarity for better performance close to V_{SS}. The design was set to have a nominal transconductance of 500 μS (at 85°C) and a limiting current of 160 μA. Fig. 12 shows the measured value of g_m versus common-mode level. There is a noticeable double humped shape to the curves, due to transistors entering the moderate inversion region at the transitions between having either both n and p on, and just one polarity on. Under these conditions, there is more total transconductance per unit tail current compared with the strong inversion case. Nonetheless, the variation measured is less than $\pm$10%, and there are no sharp discontinuities in the characteristic.

Note that reducing the bias current by 50% brings the input devices closer to moderate inversion in the ***ON*** state, and hence the variation in g_m as a function of total tail current is reduced.

Fig. 13 shows the variation from the normalized value of limiting current. A deviation of the order of 2% is evident; this

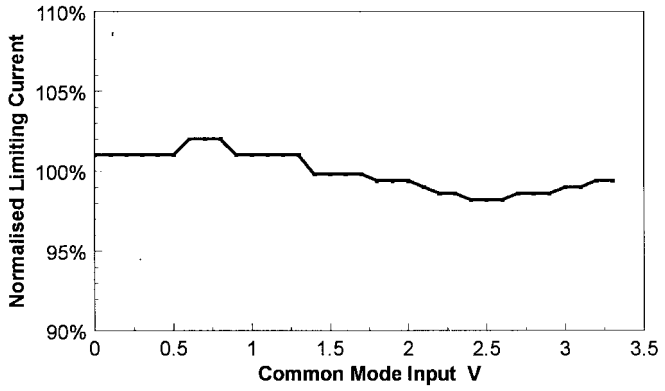


Fig. 13. Measured maximum limiting output current of transconductor versus input common-mode level ($V_{DD} = 3.3$ V; output level $= V_{DD}/2$).

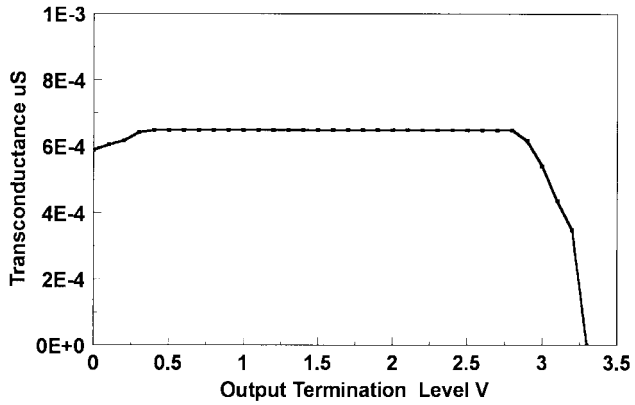


Fig. 14. Measured transconductor g_m versus output common-mode level ($V_{DD} = 3.3$ V; input level $= V_{DD}/2$).

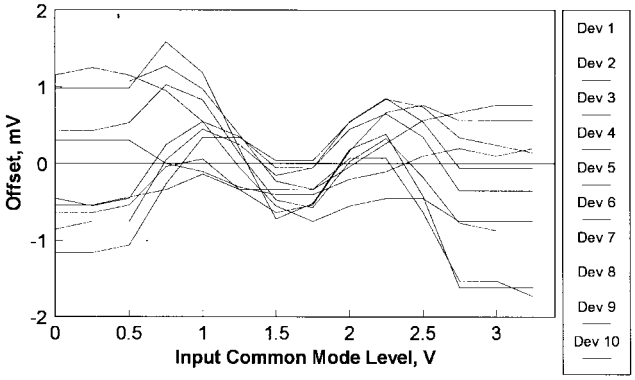


Fig. 15. Measured transconductor normalized input offset variation versus input level voltage ($V_{DD} = 3.3$ V; output fixed at $V_{DD}/2$).

can be accounted for by the modest performance of the single transistor current sources used for the tail currents. Finally, the performance of the current summer was examined by varying the output termination level of the transconductor, while keeping the input common-mode constant near midsupply. Fig. 14 shows that the value of g_m holds up well almost right down to V_{SS}, and falls away within about 0.4 V of V_{DD} as expected (due to the collapse of the p-channel mirror circuit).

Fig. 15 shows how the input offset varies with the applied common-mode level. Variations of around ± 1.5 mV are observed; this result is of most significance in the context of the op-amp measurements, discussed later.

The basic functionality was also checked with reduced power supply voltage, without adjusting the I_{ref} supplied to the cell; failure was observed with V_{DD} at around 2.2 V.

B. Comparator Results

In the target application, the key parameter was the response time to both large and small input overdrive levels, and the associated recovery time after a previous opposite decision before a valid result can be obtained. An arbitrary waveform generator was used to produce a test signal which would show this behavior, and using capacitive coupling, the signal was added to a common-mode dc level at the input pin. Fig. 16 shows results for an input comprising a 400 mV step, followed by a reversal of polarity by 40 mV. These levels were used to ensure that random offsets did not affect responses significantly, while still driving the comparator to a new decision in small-signal mode. The common-mode reference voltages chosen, 0.5 V, 1.65 V, and 2.8 V, illustrate behavior in the three main regimes without the excitation signal activating the input protection structures on the die. It can be seen that the recovery time is very close to 22 ns (including driving the pad via a buffer), regardless of the common-mode input level.

C. Op-Amp Results

Fig. 17 shows the op-amp test-chip. The cell occupies 0.12 mm^2 in the 0.5 μm process. Evaluation has focused on its use in voltage follower (and other noninverting) applications. An external load of 5 kΩ was capacitively coupled to the output, which together with scope lead and board capacitances, represented the moderate application load. Input signals were capacitively coupled to the noninverting input, with the dc level being set by a simple high resistance potential divider (inset in Fig. 18). Oscilloscope observations were supplemented with spectral analyses of the outputs. Sine wave signals were applied at 100 kHz from a low distortion oscillator, and at higher frequencies using a synthesizer and passive 50 Ω impedance filters. With a 2.5 $V_{p\text{-}p}$ 100 kHz sine wave applied on a pedestal of $V_{DD}/2$, the circuit performs very well as a follower. Raising the frequency to 2.5 MHz brings little deterioration; Fig. 18(a) shows the input and output with a 2.5 MHz, 2.5 $V_{p\text{-}p}$ input. Examining the output spectrum shows that the harmonics are below -55 dB [Fig. 18(b)], which is more than adequate for video applications. The circuit yields similar results with a 1.4 $V_{p\text{-}p}$ 5 MHz input, but slew-rate limiting in the rather modest output stage distorts larger signals.

Offset voltage in follower configuration was also measured (i.e., just the dc error between input and output) over the full input range. These are very similar to the transconductor alone, albeit with a small additional contribution due to the loading of an amplifier with limited gain and output drive range. As mentioned earlier, this offset fluctuation appears as a periodic signal in series with the applied input. Hence, offset related signals of ± 2 mV are consistent with the ~ -55 dB distortion

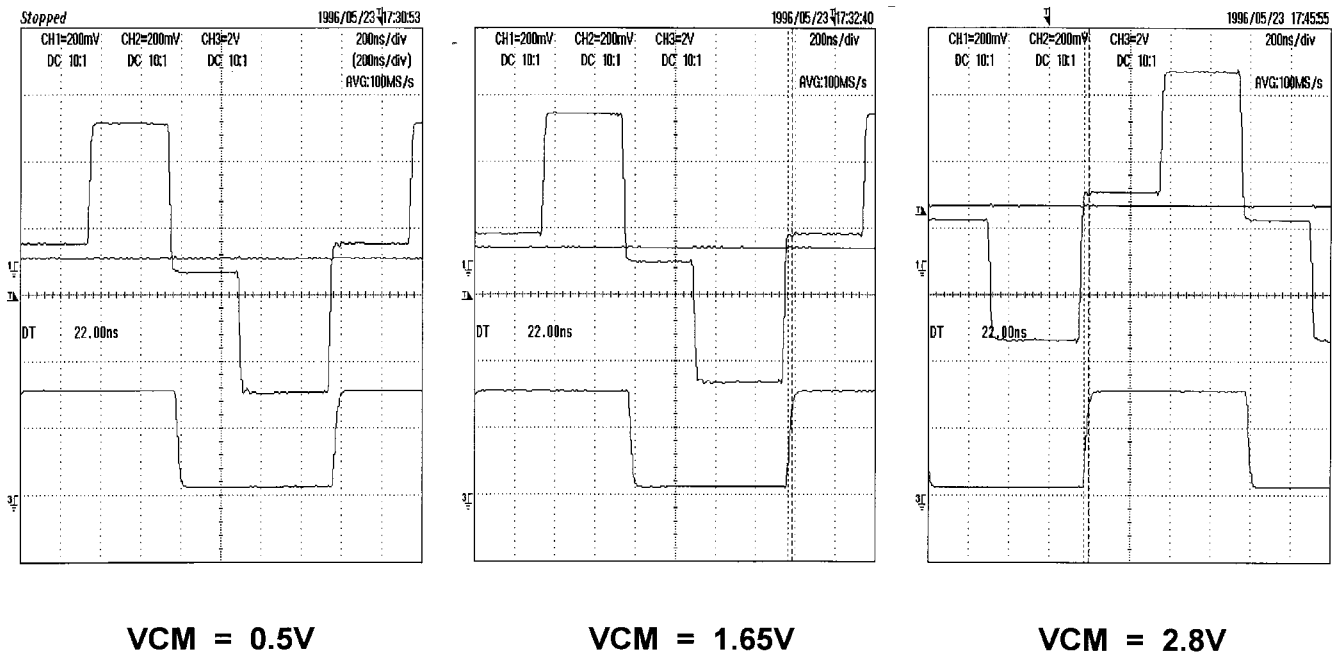


Fig. 16. Comparator recovery performance: Recovery from 400 mV differential input overdrive, followed by 40 mV reversal of input, with common-mode reference levels in each of main operating regimes (0.5 V, 1.65 V, and 2.8 V). ($V_{DD} = 3.3$ V).

TABLE II
SUMMARY OF MEASURED RESULTS

	Transconductor	Comparator	Op-Amp
G_m variation versus common-mode i/p	$< \pm$ 10%	"	"
Slewing current variation versus common-mode i/p	$< \pm$ 2%		
Midsuply input stage offset (10 samples)	-4 mV $\pm$ 5 mV	-4 mV $\pm$ 5 mV	
Input stage offset variation versus common-mode input	$< \pm$ 1.5 mV (0–3 V)	As Transconductor	
Offset in follower configuration $R_L = 5\text{k}\Omega$			$< \pm$ 5 mV (0.5 V–3.0 V)
Comparator recovery time variation versus common-mode input		22 ns $\pm$ <1 ns	
LF gain			77 dB
Unity gain bandwidth			40 MHz
Power consumption ($V_{DD} = 3.3$ V)	2.3 mW	2.3 mW	9 mW
Miminum supply	2.2 V	—	—
Process	0.5-μm CMOS	0.5-μm CMOS	0.5-μm CMOS
Area	0.04 mm^2	0.04 mm^2	0.12 mm^2

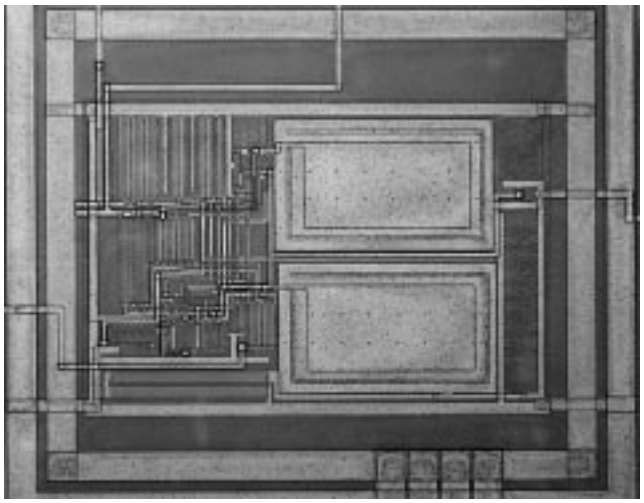


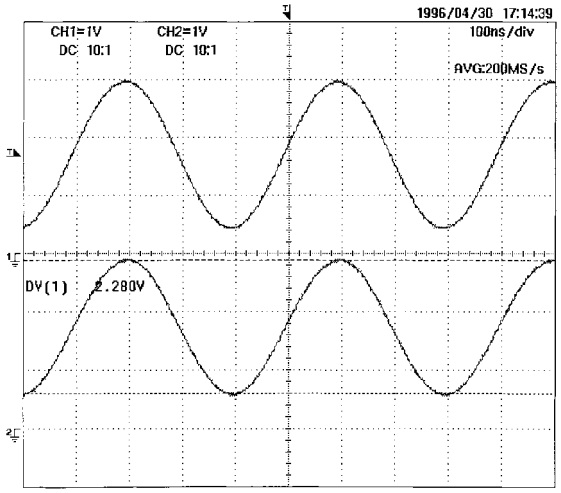
Fig. 17. Op-amp cell microphotograph.

levels seen. Input offset may be controlled in the design phase by means of gate areas in the usual way. Note that there is a secondary but nonetheless significant contribution to input offset from the current summer, particularly if short channel transistors are use to maximize bandwidth.

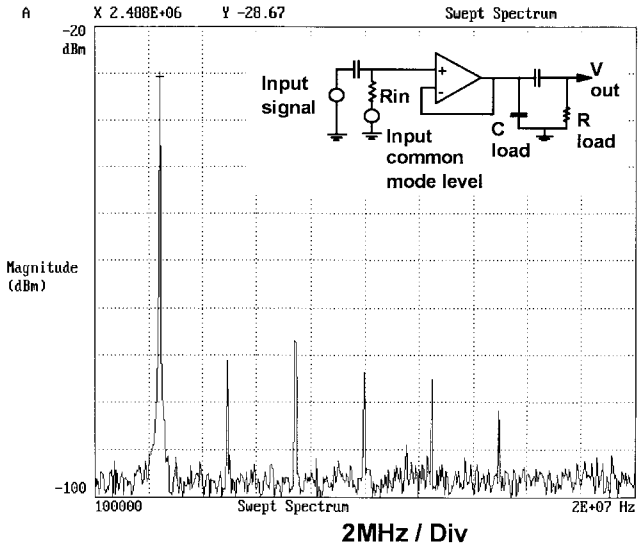
Finally, the low frequency gain and bandwidth were checked; these were measured at 77 dB, with no external load, and the gain bandwidth was 40 MHz. The results are summarized in Table II. These figures (and all other results) agree very closely with MOS9 [14] simulations.

IX. CONCLUSIONS

A new rail-to-rail input circuit has been described which achieves high bandwidth and near constant large and small signal behavior. The circuit places no reliance on analytic square law device characteristics, and is therefore applicable in deep submicron CMOS. Feedforward is used in preference to feedback to generate the desired characteristic, thereby maximizing bandwidth. Simple design procedures and a robust biasing scheme for the current summation network have been described.



(a)



(b)

Fig. 18. Measured op-amp voltage follower with ac coupled 5 kΩ load. 2.5 $V_{p\text{-}p}$, 2.5 MHz, common-mode voltage pedestal = 1.65 V. ($V_{DD} = 3.3$ V). (a) Time domain response: upper trace, input; lower trace, output. (b) Signal spectrum at op-amp output.

Using this circuit, a family of basic low voltage analog functions has been developed which demonstrate good dynamic common-mode performance across the entire power supply range, as well as being usable in virtual earth mode. Starting with a transconductor core, a fast recovery asynchronous comparator and a two-stage op-amp have been designed. These cells have been shown to be more than adequate for video signal conditioning and processing. The performance of each is close to being independent of operating common-mode levels, allowing very simple behavioral models to be used for complex mixed-signal system simulation.

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REFERENCES

[1] Y P Tsividis, *Operation and Modeling of the MOS Transistor*. New York: McGraw-Hill, 1987.
[2] J N Babnezhad, "A rail-to-rail CMOS op-amp," *IEEE J. Solid-State Circuits*, vol. 23, pp. 1414–1417, Dec. 1988.
[3] M. Ryat, "Rail-to-rail operational transconductance amplifier," U.S. patent 5 208 552, May 1993.
[4] R. Hogervorst *et al.*, "Compact power efficient 3V CMOS rail-to-rail input/output op-amp for VLSI cell libraries," *IEEE J. Solid-State Circuits*, vol. 29, pp. 1505–1513, Dec. 1994.
[5] S. Akurai and M. Ismail, "Robust design of rail-to-rail CMOS operational amplifiers for a low power supply voltage," *IEEE J. Solid-State Circuits*, vol. 31, pp. 146–156, Feb. 1996.
[6] K. Nagaraj, "Constant transconductance CMOS amplifier input stage with rail-to-rail input common mode voltage," *IEEE Trans. Circuits Syst. II*, vol. 42, pp. 366–368, May 1995.
[7] R. Hogervorst *et al.*, "Compact CMOS constant-gm rail-to-rail input stages with g_m controlled by an electronic Zener diode," *IEEE J. Solid-State Circuits*, vol. 31, pp. 1035–1040, July 1996.
[8] M. J. M. Pelgrom *et al.*, "Matching properties of MOS transistors," *IEEE J. Solid-State Circuits*, vol. 24, pp. 1433–1439, Oct. 1989.
[9] W. Sansen, "Analog circuit design in scaled CMOS technology," in *Proc. 1996 Symp. VLSI Circuits*, Hawaii, June 1996, pp. 8–11.
[10] J. N. Babanezhad and R. Gregorian, "A programmable gain/loss circuit," *IEEE J. Solid-State Circuits*, vol. SC-22, pp. 1082–1090, Dec. 1987.
[11] P. Gray and R. Meyer, *Analysis and Design of Analog Integrated Circuits*, 3rd ed. New York: Wiley.
[12] H. Traff *et al.*, "Novel approach to high speed CMOS current comparators," *Electron. Lett.*, vol. 28, no. 3, pp. 310–312, Jan. 1992.
[13] D. B. Ribner and M. A. Copeland, "Design techniques for cascoded CMOS op-amps with improved PSRR and common mode input range," *IEEE J. Solid-State Circuits*, vol. SC-19, pp. 919–925, Dec. 1984.
[14] R. Velghe *et al.*, "MOS 9 model," Philips unclassified report NL-UR003/94, Philips Research, Eindhoven, June 1995.

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