A 15-bit Linear 20-MS/s Pipelined ADC Digitally Calibrated With Signal-Dependent Dithering

Yun-Shiang Shu, *Student Member, IEEE*, and Bang-Sup Song, *Fellow, IEEE*

***Abstract*—Pseudo-random dithers have been used to measure capacitor mismatch and opamp gain errors of the pipelined analog-to-digital converter (ADC) in background and to calibrate them digitally. However, this error measurement suffers from signal range reduction and long signal decorrelation time. A signal-dependent dithering scheme allows the injection of a large dither without sacrificing the signal range and shortens the signal decorrelation time. A 1.5-bit multiplying digital-to-analog converter (MDAC) stage is modified for signal-dependent dithering with two additional comparators, and its capacitor mismatch and gain errors are measured and calibrated as one error. When sampled at 20 MS/s, a 15-bit prototype ADC achieves a spurious-free dynamic range of 98 dB with 14.5-MHz input and a peak signal-to-noise plus distortion ratio of 73 dB with 1-MHz input. Integral nonlinearity is improved from 25 to 1.3 least significant bits (LSBs) after calibrating the first six stages. The chip is fabricated in 0.18-μm CMOS process, occupies an active area of 2.3 $\times$ 1.7 mm^2, and consumes 285 mW at 1.8 V.**

***Index Terms*—Background calibration, capacitor mismatch and gain calibration, digital calibration, pipelined analog-to-digital converter, signal-dependent dithering.**

I. Introduction

THE resolution of the pipelined ADC is limited by the inter-stage gain error resulting from capacitor mismatch and finite opamp gain in the MDAC. As fine-line lithography advances, even 14-bit level performance has been achieved without calibration by carefully matching capacitors in the multibit first-stage MDAC but still using high-gain opamps [1], [2]. A recent trend is to digitally calibrate both capacitor mismatch and opamp finite gain errors simultaneously in background [3]–[14]. The digital background calibration is preferred to other high-resolution techniques because it can track long-term process variations, and the digital power and area overhead diminishes as CMOS technology is scaled down. For any background calibration to be useful, it is necessary that its impact on analog circuits be minimized, and the calibration cycle be made short.

The pseudo-random noise (PN) pulse sequence has been used in background calibration for error randomization and detection [7]–[19]. PN-modulated errors or dithers can be measured by correlating them digitally with the same PN sequences. In the digital domain, the measurement process is simply the digital sign change by the PN followed by the accumulation for averaging (low-pass filtering). In most cases, capacitor mismatch errors can be PN-modulated by switching circuit configurations [15]–[17]. However, to measure the total gain error contributed by both capacitor mismatch and finite opamp gain, a PN-modulated dither needs to be injected into the same gain path for gain measurement, but it can be subtracted later digitally [7]–[12], [18]. The background calibration by PN-modulation or dithering has two constraints. One is the measurement time constraint. With a large uncorrelated signal present, it is difficult to detect a small PN-modulated error. In particular, a prohibitively large number of samples should be accumulated when the number of bits resolved per stage is low [9]. The other is the dither magnitude constraint. The signal magnitude needs to be reduced so that the signal plus dither may not exceed the full-scale range of the MDAC [7]–[10], [18].

A signal-dependent dithering scheme is proposed to overcome these measurement time and dither magnitude constraints present in the previous fixed-magnitude PN dithering. In the signal-dependent dithering [20], dithers of different magnitudes are selectively used depending on the signal level so that the signal-to-dither ratio can be minimized, and thereby both constraints are significantly relieved. When applied to a 1.5-bit/stage pipelined ADC, the inter-stage gain error of the standard tri-level MDAC is measured with 15-bit accuracy within a practical number of measurement cycles of 2^{26}. Dither is injected by adding two comparators and splitting the unit capacitor into two in each pipeline stage. The proposed digital background calibration method calibrates all gain errors resulting from capacitor mismatch, finite opamp gain, and other sources in one step with no strict requirements imposed on analog components and without using digital multipliers or dividers [5]–[8].

After reviewing the nonlinearity error of the 1.5-bit/stage pipelined ADC and its digital calibration concept in Section II, the background inter-stage gain measurement by PN dithering and its constraints are discussed in Section III. In Section IV, a digital background calibration scheme based on signal-dependent dithering is proposed. Section V covers the circuit implementation, and experimental results are summarized in Section VI.

II. Nonlinearity Error and Digital Calibration

A. Nonlinearity Error of the 1.5-bit/Stage Pipelined ADC

A pipelined ADC consists of several low-resolution stages as shown in Fig. 1. In each stage, after the input is sampled and quantized by the sub-ADC, the residue is amplified to fit into the next stage's full range using a switched-capacitor MDAC [21]. Since the comparator offsets in the sub-ADC can be digitally

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The authos are with the Department of Electrical and Computer Engineering, University of California at San Diego, La Jolla, CA 92093 USA (e-mail: song@ece.ucsd.edu).

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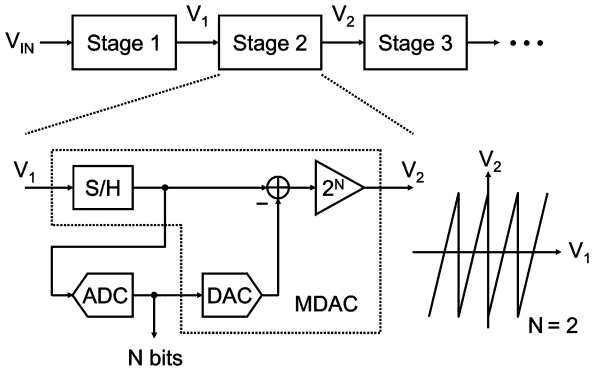


Fig. 1. Pipelined ADC block diagram.

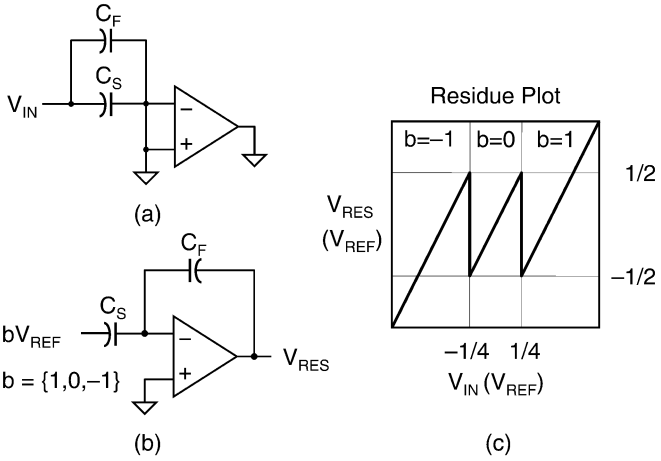


Fig. 2. Tri-level MDAC. (a) Sampling phase. (b) Amplification phase. (c) Residue plot.

corrected using a redundant bit [22], the ADC performance relies only on the accuracy of the amplified residue. Fig. 2 shows a tri-level MDAC in two phases, where "b" is the sub-ADC output bit. During the amplification phase, the sampled input is multiplied by a gain of 2, and $\mathrm{bV_{REF}}$ is subtracted as shown in the residue plot of Fig. 2(c), where the comparator thresholds of the sub-ADC are set to $\pm 1/4\ V_{\mathrm{REF}}$.

The amplified residue is affected by two major nonideal factors, α and δ, which result from capacitor mismatch and finite opamp gain, respectively, and becomes

$$V_{\mathrm{RES}} = (1+\delta)[(2+\alpha)V_{\mathrm{IN}} - (1+\alpha)\mathrm{bV_{REF}}]. \qquad (1)$$

Using (1), the MDAC stage can be modeled as shown in Fig. 3. The residue, V_{RES}, is further digitized by the later ADC stages. The digital output, $\mathrm{D_{OUT}}$, is obtained by adding the digital V_{REF}, $\mathrm{bD}(V_{\mathrm{REF}})$, to the digitized residue, $\mathrm{D}(V_{\mathrm{RES}})$, and then divided by 2 so that what is subtracted in the MDAC can be restored digitally. However, the analog $\mathrm{bV_{REF}}$ subtracted in (1) is affected by both α and δ, and therefore, it does not match with the ideal digital V_{REF}, $\mathrm{bD}(V_{\mathrm{REF}})$. Fig. 4(a) shows how this mismatch affects the pipelined ADC's linearity. In this example, $(1+\alpha)(1+\delta)V_{\mathrm{REF}}$ is subtracted in the analog domain, but the ideal $\mathrm{D}(V_{\mathrm{REF}})$ is added in the digital domain when the sub-ADC output bit is 1. As a result, a mismatch error occurs at

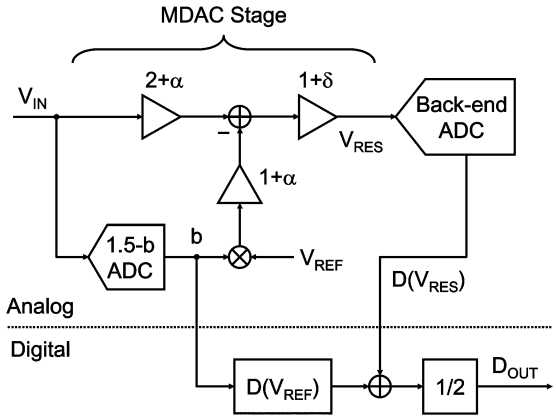


Fig. 3. Model of a pipelined ADC with nonideal factors.

the comparator threshold point, and is translated into the nonlinearity of the ADC.

B. Digital Calibration Concept

The mismatch between the analog V_{REF} and the digital $\mathrm{D}(V_{\mathrm{REF}})$ can be eliminated by either reducing the nonideal factors in the analog domain or adjusting $\mathrm{D}(V_{\mathrm{REF}})$ in the digital domain. The analog implementation usually requires capacitor trimming [23], capacitor error-averaging [24]–[26], or capacitor shuffling [16], [27] to reduce the capacitor mismatch error α and uses high-gain opamps to get rid of the low-gain effect δ. Such analog methods increase the circuit complexity, especially in the opamp design at low supply voltages. However, in the digital implementation, only the digital $\mathrm{D}(V_{\mathrm{REF}})$ needs to be adjusted to match the nonideal analog V_{REF} [28], [29]. For this, the analog V_{REF} should be measured accurately with the back-end ADC. The digital calibration concept is explained in Fig. 4(b). While $(1+\alpha)(1+\delta)V_{\mathrm{REF}}$ is subtracted in the MDAC, the digital value of $\mathrm{D}[(1+\alpha)(1+\delta)V_{\mathrm{REF}}]$ is added back instead of the ideal $\mathrm{D}(V_{\mathrm{REF}})$ to eliminate the mismatch error. Even after this calibration, the overall gain slope error remains, but the gain slope correction is not necessary since the ADC transfer function is linear. Digital calibration may increase the complexity of the digital circuitry, but the overhead is minimal in deep submicron CMOS chips.

III. Background Gain Measurement

A. Gain Measurement With PN Dithering

Fig. 5 explains the gain measurement scheme by PN dithering, where the gain errors of $(1+\alpha)$ and $(1+\delta)$ are combined as $(1+\epsilon)$. To measure this gain of the V_{REF}, a well-defined PN-modulated calibration signal, V_{CAL}, which is a usually a fraction of V_{REF}, is added to the input, V_{IN}. The PN is a zero-mean sequence of 1 and -1. After multiplied by the same PN and $V_{\mathrm{REF}}/V_{\mathrm{CAL}}$, the digital output becomes

$$\left(\frac{V_{\mathrm{IN}}}{V_{\mathrm{CAL}}}\right)\mathrm{PN}(1+\varepsilon)V_{\mathrm{REF}} + \mathrm{PN}^2(1+\varepsilon)V_{\mathrm{REF}}. \qquad (2)$$

Note that the input signal V_{IN} is modulated by PN and translated into a noise, but the PN-modulated calibration signal is correlated by the same PN sequence and becomes a DC value

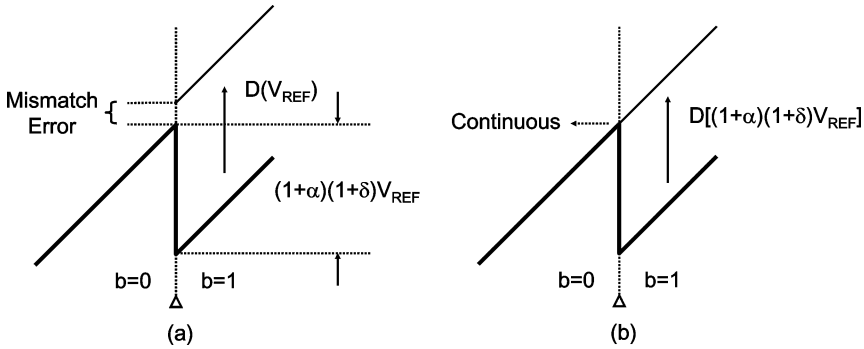


Fig. 4. Nonlinearity error in pipelined ADC. (a) Before calibration. (b) After calibration.

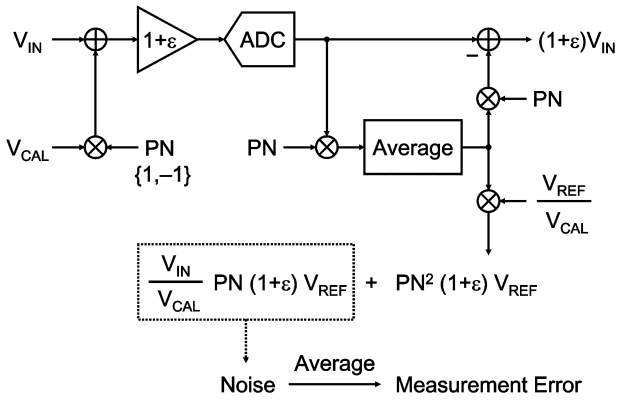


Fig. 5. Principle of background gain measurement with PN dithering.

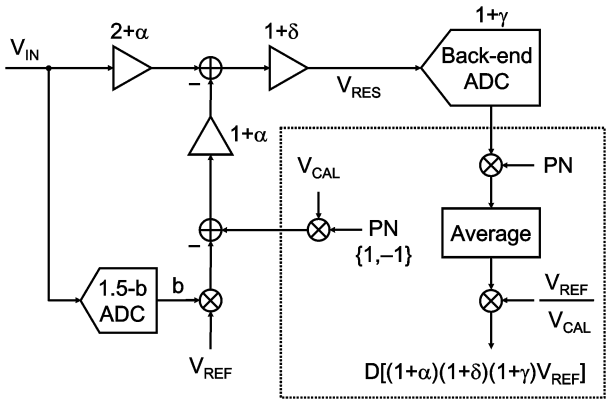


Fig. 6. Background gain measurement of an MDAC stage.

of $(1+\varepsilon)V_{\rm REF}$ since $\rm PN^2 = 1$. Therefore, the gain of $V_{\rm REF}$ is obtained by low-pass filtering the output given by (2). However, since the bandwidth of the low-pass filter is limited, the noise-like PN-modulated $V_{\rm IN}$ remains as a measurement error after low-pass filtering. The simplest digital low-pass filter is an accumulator that averages a large number of samples. Ideally, the measurement error approaches zero if infinitely many samples are averaged. However, as the number of samples is limited in practice, $V_{\rm IN}/V_{\rm CAL}$, which is the signal-to-dither ratio, should be kept as small as possible in order to minimize this residual measurement error.

Fig. 6 shows how the gain measurement is performed in one 1.5-bit stage in the pipelined ADC, where the measurement function is enclosed inside the dotted rectangle. The subtracted $\rm bV_{REF}$ is multiplied by the gains of $(1+\alpha)$, $(1+\delta)$, and quantized by a nonideal back-end ADC with a gain of $(1+\gamma)$. The PN-modulated $V_{\rm CAL}$ is injected to measure the gain of the $V_{\rm REF}$. After the PN correlation, accumulation for averaging, and multiplication by $V_{\rm REF}/V_{\rm CAL}$, the digital value of $\rm D[(1+\alpha)(1+\delta)(1+\gamma)V_{REF}]$ is obtained. Therefore, all errors resulting from capacitor mismatch, finite opamp gain, and the nonideal back-end ADC can be grouped and calibrated as one gain error. Once calibrated, the ADC performance will be only limited by the nonlinearity of the opamp and nonlinear signal-dependent charge injection in sampling.

B. Constraints of PN Dithering

The measurement time constraint originates from the tradeoff between the measurement accuracy and the averaging time. Fig. 7(a) shows the measurement error given by (2) after averaging 2^{20} samples, where both $V_{\rm IN}/V_{\rm CAL}$ and $V_{\rm REF}$ are set to 1. The simulation is repeated 1000 times with a 2-$V_{\rm PP}$ sinusoidal input. In the output histogram, 99% of the measurement errors are smaller than 2^{-10}, which is a 10-bit accuracy. Fig. 7(b) demonstrates the relation between the measurement accuracy and the numbers of samples averaged. Note that four times more samples should be averaged to get one more bit of measurement accuracy. This is true if the PN-modulated $V_{\rm IN}/V_{\rm CAL}$ in (2) is treated as a white noise since the standard deviation of a white noise is reduced by the square root of 2 as the number of averaging samples is doubled. The result in Fig. 7(b) implies that 2^{30} samples should be averaged for 15-bit accuracy, and it takes almost one minute to complete one measurement if the ADC works at 20 MS/s.

The dither magnitude constraint results from the tradeoff between the dither magnitude and the signal range. Fig. 8(a) explains the dither magnitude constraint with a large PN-modulated dither, where the full scale is normalized from -1 to 1. The signal range is reduced accordingly to keep the total signal plus dither within the full-scale range. This leads to the reduction of the effective number of bit (ENOB). The signal range reduction is not desirable in a system where the signal-noise ratio (SNR) is dominated by the thermal noise. For example, switched-capacitor circuits will need capacitors of twice the size to suppress the kT/C noise by 3 dB, thus resulting in a significant area and power penalty. Although a smaller dither, as shown in Fig. 8(b), makes the signal range larger, it takes much longer to

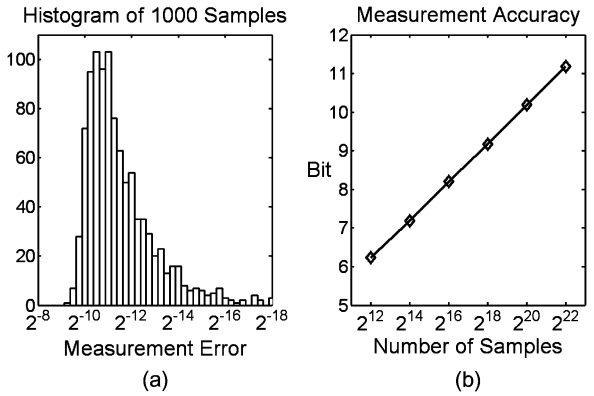


Fig. 7. (a) Histogram of measurement error after averaging 2^{20} samples. (b) Measurement accuracy versus number of samples averaged.

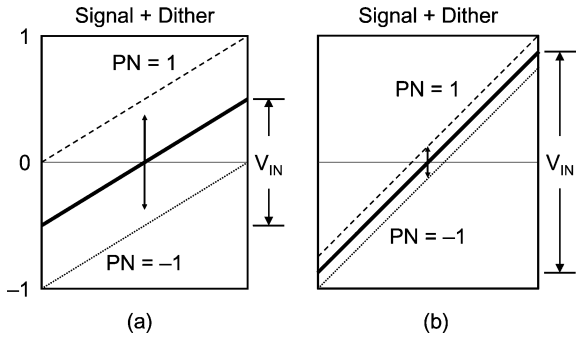


Fig. 8. Fixed-magnitude PN dithering. (a) Large dither. (b) Small dither.

achieve the same accuracy since the ratio of $V_{\rm IN}/V_{\rm CAL}$ in (2) is large. This relation between the signal range and the measurement time makes it even more difficult to find a solution that satisfies both constraints.

IV. Calibration With Signal-Dependant PN Dithering

A. PN Dithering

A signal-dependent dithering scheme is proposed to relieve both the measurement time and dither magnitude constraints. The dither magnitude is adjusted depending on the signal level. For example, the signal is divided into three sub-ranges as shown in Fig. 9(a). A dither of 2/3 is injected depending on the PN value in the middle range. When the signal is higher than $+1/3$, no dither is injected if $\rm PN = 1$, but a dither of $-4/3$ is injected if $\rm PN = -1$. When it is lower than $-1/3$, dithers of $+4/3$ and 0 are injected if $\rm PN = 1$ and -1, respectively. As a result, the signal plus dither is equivalent to a smaller signal, which is between $\pm 1/3$, with a large fixed-magnitude dither of 2/3 as shown in Fig. 9(b). This implies that the ratio of $V_{\rm IN}/V_{\rm CAL}$ in (2) is smaller and the measurement accuracy is higher. That is, the signal-dependent dithering scheme shortens the measurement time and achieves the same level of measurement accuracy while permitting a large dither to be injected with a full-scale signal. Note that the signal-to-dither ratio $V_{\rm IN}/V_{\rm CAL}$ can be further reduced if the signal range is divided into more sub-ranges. In the signal-dependent dithering, the PN-correlated component stays constant although additional

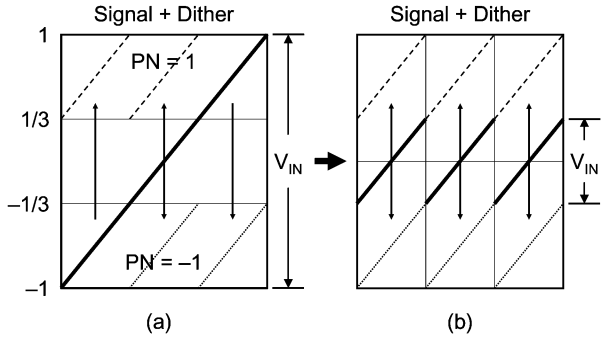


Fig. 9. Signal-dependent dithering. (a) Three sub-ranges. (b) Equivalent fixed-magnitude PN dithering.

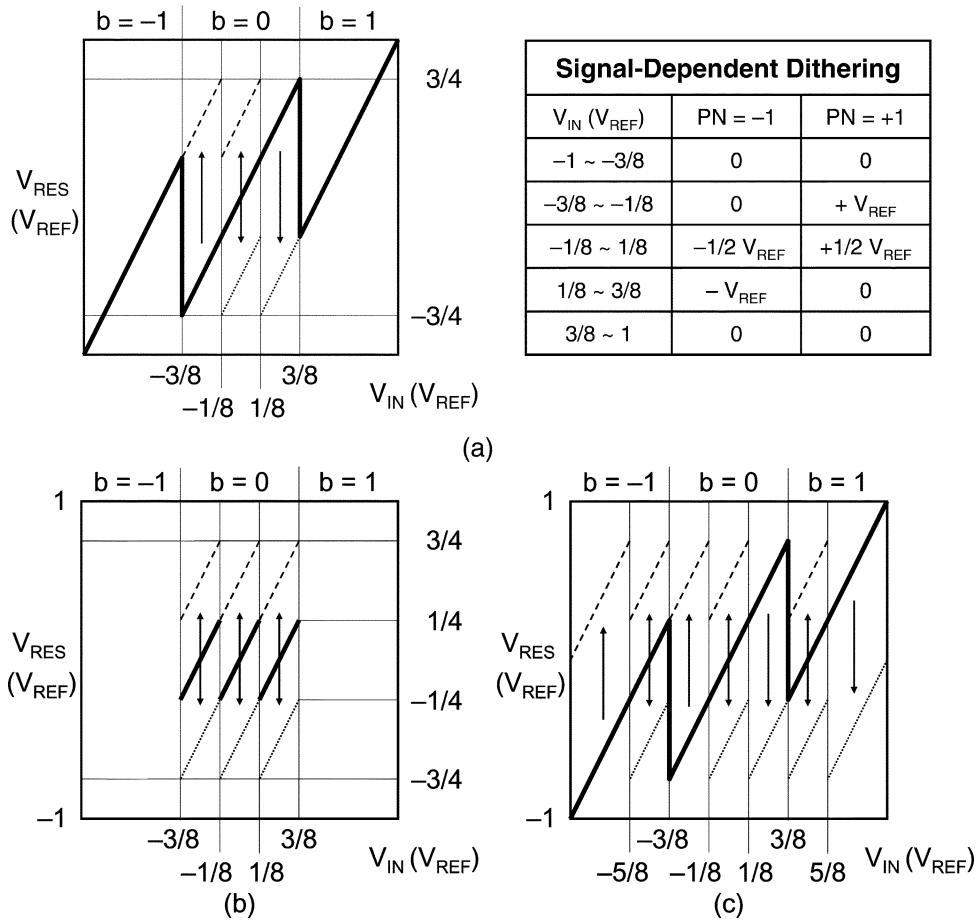
dither depending on the input is added. In practice, the difference of the outputs for two cases of $\rm PN = 1$ and -1 should be generated by the same hardware in order to emulate the fixed-magnitude PN dithering. The comparator thresholds and the dither magnitudes are set so that the signal can stay within the full-scale range regardless of the comparator offsets.

The benefits of the signal-dependent dithering are apparent if the fixed-magnitude dithering case with a dither of 1/4, which is a compromise between Fig. 8(a) and (b), is compared to the signal-dependent dithering case shown in Fig. 9(a). First, since the dither of 1/4 reduces the signal range to 3/4, the ENOB with Fig. 9(a) is about 0.5-bit better. Second, the ratio of $V_{\rm IN}/V_{\rm CAL}$ decreases from 3 to 1/2 in the signal-dependent dithering. This improves the measurement accuracy further by 2.5 bits. Therefore, the dithering scheme in Fig. 9(a) gives 3 more bits of accuracy and can shorten the measurement time by 1/4 [3]. That is, one measurement cycle that would otherwise take one minute to complete can now be completed in one second.

The dithering scheme used in [13] and [14] is very similar to the proposed signal-dependent dithering. The sub-ADC and sub-DAC resolve one more bit to produce two different residues. Both designs use a multibit first stage to achieve a 12-bit calibrated resolution. In [13], the inter-stage gain and nonlinearity errors are calibrated by detecting the difference between the two residues. In [14], digital outputs are averaged so that the estimated gain and nonlinearity parameters can converge after a certain number of steps. The proposed signal-dependent dithering lowers the signal-to-dither ratio further by dividing the input range into more sub-ranges, and the inter-stage gain error is measured together. This low signal-to-dither ratio is an important feature when calibrating a high-resolution ADC with a low-resolution first stage. For example, calibrating a 1.5-bit first stage requires more accuracy than calibrating a multibit first stage. Therefore, a large number of output samples were averaged [9]. Although using a multibit first stage can somewhat relax the calibration accuracy requirement, calibrating both multibit DAC mismatch and residue amplifier gain error increases the complexity of the calibration algorithm [8], [12].

B. Signal-Dependent Dithering for Tri-Level MDAC

Fig. 10(a) shows the modified residue plot of a tri-level MDAC for dithering. The comparator thresholds in the sub-ADC are shifted from $\pm 1/4\ V_{\rm REF}$ to $\pm 3/8\ V_{\rm REF}$.



Signal-Dependent Dithering		
V_{IN} (V_{REF})	PN = –1	PN = +1
–1 ~ –3/8	0	0
–3/8 ~ –1/8	0	+ V_{REF}
–1/8 ~ 1/8	–1/2 V_{REF}	+1/2 V_{REF}
1/8 ~ 3/8	– V_{REF}	0
3/8 ~ 1	0	0

Fig. 10. Modified residue of an MDAC stage. (a) Signal-dependent dithering. (b) Equivalent fixed-magnitude PN dithering. (c) Restored to full signal range dithering.

Signal-dependent dithers are injected between $\pm 3/8\ V_{\rm REF}$, and two more comparators are added with thresholds at $\pm 1/8\ V_{\rm REF}$. No dither is injected when signal is high for simplicity. This does not delay the calibration time significantly as will be explained later. A dither magnitude of $-V_{\rm REF}$, $-1/2\ V_{\rm REF}$, 0, $+1/2\ V_{\rm REF}$ or $+V_{\rm REF}$ is chosen depending on the PN values and the signal level as shown in Fig. 10(a). The comparator thresholds and dither magnitudes are set to have room for comparator offsets. As a result, the signal plus dither between $\pm 3/8\ V_{\rm REF}$ is in effect a large fixed-magnitude dither of $1/2\ V_{\rm REF}$ with a small signal within the range of $\pm 1/4\ V_{\rm REF}$ as shown in Fig. 10(b). The signal-to-dither ratio of $V_{\rm IN}/V_{\rm CAL}$ is reduced to 1/2. By averaging the output samples while the input stays within $\pm 3/8\ V_{\rm REF}$, 99% of the measurement errors are smaller than 2^{-14} when 2^{26} samples are averaged. If referred to the input after divided by the residue gain of 2, it corresponds to a 15-bit accuracy.

The standard tri-level MDAC modified for signal-dependent dithering by adding two more comparators and splitting a capacitor into two is shown in Fig. 11. Dithers are injected by controlling the switches according to the comparator outputs and PN values. Both C1 and C2 are switched between $-V_{\rm REF}$ and 0 for the signal range from $-3/8$ to $-1/8\ V_{\rm REF}$, and between 0 and $+V_{\rm REF}$ for the signal range from $+1/8$ to $+3/8\ V_{\rm REF}$ if PN is 1 and -1, respectively. When the signal lies in the middle

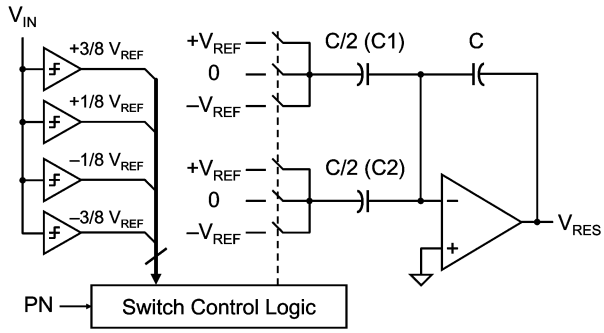


Fig. 11. MDAC residue amplifier for signal-dependent dithering.

range, C1 and C2 are alternately switched to $-V_{\rm REF}$ if $\rm PN = 1$ and $+V_{\rm REF}$ if $\rm PN = -1$ to inject a dither of 1/2 $V_{\rm REF}$ equally through two capacitors. The mismatch between the two split capacitors contributes to noise after randomized and spread over the Nyquist band. However, it is below the noise level of the system and is not subtracted digitally in this design.

The proposed tri-level MDAC shown in Fig. 11 has the following features. 1) Large dithers are used without sacrificing the signal range. 2) The signal decorrelation time is greatly shortened due to the low signal-to-dither ratio, $V_{\rm IN}/V_{\rm CAL}$. 3) No additional capacitor is used for dithering, and the analog perfor-

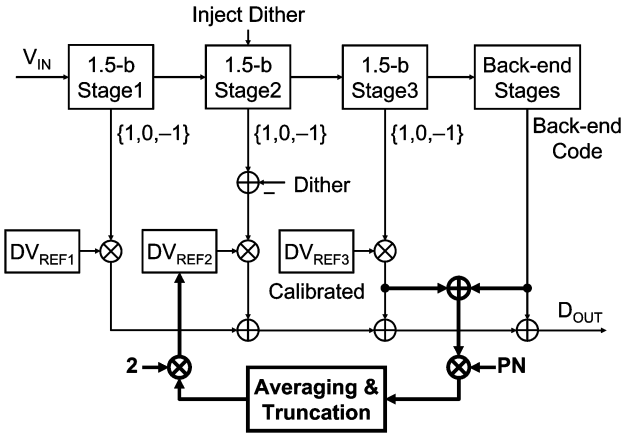


Fig. 12. 1.5-bit/stage pipelined ADC calibrated with dithering.

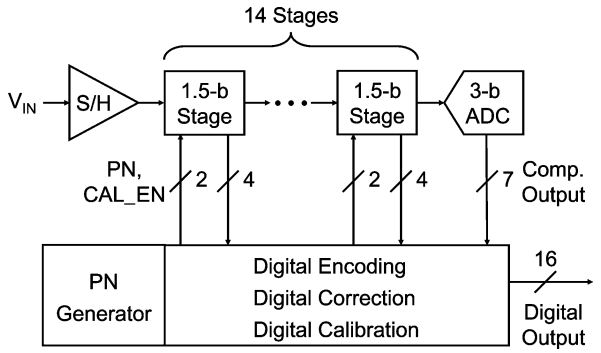


Fig. 13. ADC block diagram with digital calibration.

mance is not affected. 4) Switch control logic does not delay opamp settling. 5) Two more comparators are added in each pipeline stage.

One major concern regarding the proposed signal-dependent dithering scheme in Fig. 10(a) is that the calibration time varies with the signal condition since no dither is injected when the signal is high. Dithering for the full-range signal is possible as shown in Fig. 10(c) with additional comparators added. For example, if the signal is larger than $+5/8\ V_{\rm REF}$ and $\rm PN = -1$, the residue can be $2\ V_{\rm IN} - 2\ V_{\rm REF}$ although an additional capacitor or a reference voltage of $2V_{\rm REF}$ should be used for that. However, numerical analysis of the calibration time based on the proposed scheme shown in Fig. 10(b) indicates that only the dithering of the first stage is sensitive to the input condition while the later stages are not because the inputs of the later stages are randomized by the previous stages. The proposed signal-dependent dithering still offers a substantial saving in the measurement time with low circuit complexity unless the signal stays at a high level all the time. It is noted that the residue plot shown in Fig. 10(a) is similar to the residue plot used in [11] except for the range between $\pm 1/8\ V_{\rm REF}$. However, in [11], dither is injected before the sub-ADC by randomizing the comparator thresholds, and all output samples are averaged. A two-channel ADC architecture is used to cancel the PN uncorrelated input signal, and therefore, it introduces the mismatch problem between the two channels.

C. Digital Background Calibration

The pipelined ADC with the proposed calibration scheme is illustrated in Fig. 12. The $\rm DV_{REF}$'s are adjusted to match the analog $V_{\rm REF}$'s added/subtracted in the MDAC stages. In this example, the dither is injected into the stage2 and subtracted digitally from the signal path. The digitized residue of the stage2 is PN-correlated and then multiplied by $V_{\rm REF}/V_{\rm CAL}$ to measure and update the $\rm DV_{REF2}$ as drawn with the thick lines. The calibration proceeds from the rear stages to the front repeatedly in order to measure errors with the calibrated back-end ADC. All multipliers in Fig. 12 are implemented with adders and shifters. The digital circuitry for the PN correlation is shared by all stages.

Since the nonideal effects in the back-end stages are less critical, the calibration accuracy in the later stages can be lowered gradually to shorten the calibration time. The uncalibrated back-end ADC can be modeled as a linear ADC with a gain error. Offset has no effect on the error measurement since the offset becomes a white noise after it is spread by the PN sequence. In system simulations including all circuit nonidealities such as capacitor mismatch, finite opamp gain, and comparator and opamp offsets, the calibration achieves an SNDR of 96 dB and an SFDR of 114 dB by averaging 2^{26} samples per stage.

V. CMOS Implementation

The proposed ADC has one S/H, 14 1.5-bit stages, and a 3-bit flash as shown in Fig. 13. The digital output is 16 bits with a redundant bit to reduce the digital truncation error. The comparator outputs in each stage are connected to the digital logic. The digital encoding, digital correction, digital calibration, and also the PN sequence generator are all integrated in the digital logic. It provides each pipeline stage with the PN value and the calibration enable signal.

Since all gain errors in the signal path can be simultaneously calibrated with the proposed calibration method, the circuit implementation should ensure that all components are linear enough to achieve high SFDR. Fig. 14 shows the opamp used in both the S/H and MDAC. A two-stage Miller-compensated opamp is chosen for a large output swing. The opamp gain is designed to be high enough to neglect its nonlinearity but not to slow down its speed since the finite opamp gain error can be calibrated. The length of NMOS transistors in the signal path is minimized to meet the high-speed requirement. Simple boosting amplifiers are added to compensate for the gain reduction due to the short channel effect. The length of PMOS transistors is chosen to be longer than the minimum length for high output resistance. Simulation results show that the gain of this opamp is 95 dB. The flip-around S/H is used in this design, and the tri-level MDAC is modified for dithering as shown in Fig. 11. The S/H and MDAC have simulated loop gains of 94 dB and 87 dB, respectively, and achieve16-bit linearity with a $2\text{-}V_{\rm PP}$ input signal. The simulated closed-loop bandwidths of the S/H and MDAC are 360 and 300 MHz, respectively. They are designed high enough to settle with 16-bit accuracy at 50 MS/s. Note that the MDAC settling error is also calibrated

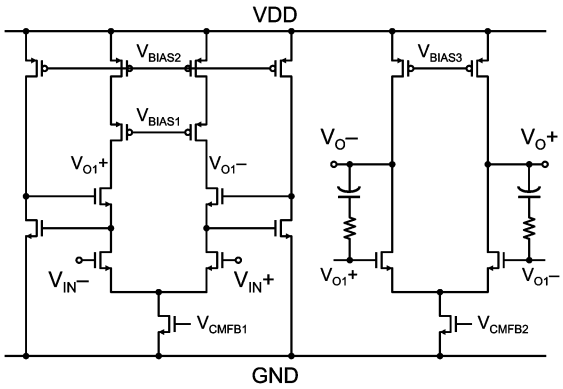


Fig. 14. Operational amplifier for S/H and residue amplifier.

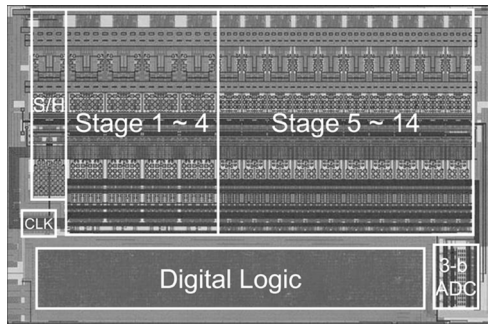


Fig. 15. Die photograph.

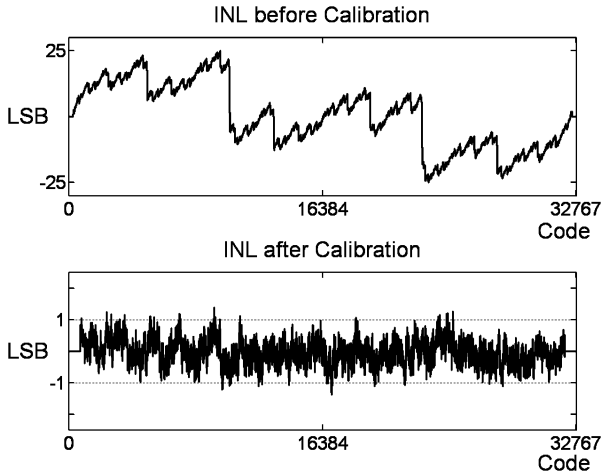


Fig. 16. Measured INL at 15-bit level.

if it is linear, and fast settling is not necessary if the settling behavior is purely exponential with a fixed time constant without any slew limit.

Bootstrapped switches [30] are used in the signal path. In high-speed circuits, as switch gets larger, the amount of charge injection increases. The bootstrapped switch provides a lower and more linear on-resistance, and contributes to a smaller and more linear signal-dependent charge injection, which can be also calibrated along with the gain error. Its parasitic capacitance is mainly the junction capacitance since its boosted gate voltage follows the drain and source voltages. The drawback is that it needs a large capacitor to boost its gate to a high voltage. Therefore, only the switches in the S/H stage in this design use a large boosting capacitor to achieve high linearity while the switches in the MDAC are boosted with smaller capacitors.

In the digital circuits, 2^{26} samples are averaged to guarantee a calibration accuracy of a 15-bit level as discussed. No measurement accuracy is scaled for later stages in this design for simplicity. The word length of the $\mathrm{DV_{REF}}$'s is 21 bits so that the accumulated truncation error can be smaller than the measurement error.

VI. Experimental Results

The prototype chip is fabricated in a 0.18-μm CMOS process. The die photograph shown in Fig. 15 occupies an active area of 2.3×1.7 mm^2. The digital calibration algorithm is fully implemented on the prototype chip. The digital logic occupies 0.6 mm^2. The area only for calibration is smaller than that since the digital area also includes the digital encoding and digital correction functions. The sampling capacitors in the S/H and stages 1–4 are set to 2 pF, and the kT/C noise limits the SNR of the ADC to be $-$ 76 dB. Stages 5–14 are scaled down by half to save chip power and area. The highly-linear differential sinusoidal input is obtained by using a synthesized signal generator followed by a bandpass filter and a single-ended-to-differential converter. The clock signal is generated by a low-jitter pulse generator.

Fig. 16 shows the measured INL at a 15-bit level before and after calibration measured at 20 MS/s. The INL error jumps significantly at the comparator threshold points before calibration. The largest INL jump is from the first stage. After the first six stages are calibrated, the INL errors are greatly reduced and improved from 25 LSB to 1.3 LSB. Fig. 17 shows the FFT spectrum of a 14.5-MHz input sampled at 20 MHz. The SFDR, total harmonic distortion (THD), and SNR, before calibration, are 69, $-$67, and 61 dB, respectively. The ENOB is about 10 bits. After calibration, the SFDR, THD, and SNR are improved to 98 dB, $-$92, and 71 dB, respectively. The ADC linearity is improved to 15 bits while the SNDR is mainly limited by the kT/C noise. Experimental results imply the clock jitter is less than 2 ps.

It takes 45 s to calibrate the first six stages while averaging 2^{26} samples per stage with a full-scale sinusoidal input at 20 MS/s. The calibration time is reduced to 38 s if the input is uniformly distributed over the full signal range since the sinusoidal signal gives less number of samples at low signal levels. If the calibration is performed without input, it takes 20 s to average 6×2^{26} samples at 20 MS/s. Note that this calibration time difference is not significant, considering the fact that the number of samples required to average grows exponentially if the signal-to-dither ratio is higher. In the previous work of a 1.5-bit/stage pipelined ADC [9], which loses 25% of the signal range and averages 2^{31} samples per stage, it took 8.95 minutes to calibrate five stages at 20 MS/s while achieving less calibration accuracy than this work. The proposed signal-dependent dithering exhibits a clear advantage in both calibration accuracy and time. The calibration time can be further saved by gradually scaling down the measurement accuracy. For example, by scaling 0.5-bit accuracy per

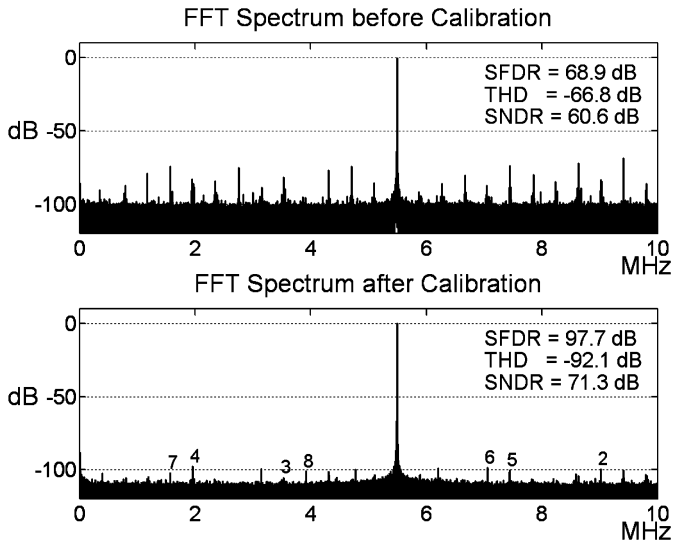


Fig. 17. Measured FFT spectrum with 14.5-MHz input @ 20 MS/s.

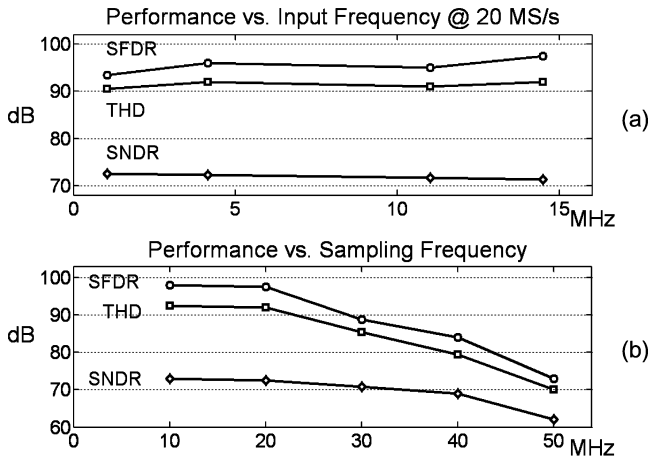


Fig. 18. (a) Measured performance versus input frequency sampled @ 20 MS/s. (b) Measured performance versus sampling frequency.

two stages, it can be reduced to 24 s with a random input. Higher sampling rate is also effective in shortening the calibration time.

Fig. 18(a) shows the ADC performance at 20 MS/s with varying input frequencies up to 14.5 MHz. The SFDR and THD stay constant at about 95 and −90 dB, respectively. The peak SNDR reaches 73 dB with 1-MHz input. Fig. 18(b) shows the ADC performance with varying sampling frequencies up to 50 MS/s. The SFDR stays higher than 95 dB up to 20 MS/s and starts to degrade slightly beyond 30 MS/s. The conversion rate in the measurement is mainly limited by the kick-back and charge-injection when switching the input sampling capacitor because the bonding wire inductance of the test package is larger than expected. As a result, measurements at a higher sampling rate of 50 MS/s are limited to 12 bits. The measured performance at 20 MS/s is summarized in Table I. The digital logic consumes 5 mW. Assuming that the digital power consumption is proportional to the sampling frequency and supply voltage, the digital power for calibration of this prototype is lower than that of [8] and [9], which also calibrates digitally in background to 15-bit linearity using on-chip digital logic.

TABLE I
SUMMARY OF MEASURED PERFORMANCE

Technology	0.18-μm CMOS
DNL / INL	0.4 / 1.3 LSB @ 15 b
Conversion Rate	20 MS/s
SFDR	98 dB
THD	–92 dB
Peak SNDR	73 dB
Signal Range	2 V_{PP}
Active Area (Digital)	2.3 x 1.7 (2.1 x 0.3) mm^2
Total Power	285 mW @1.8 V
Analog/Digital/Output Drivers	275/5/5 mW

VII. CONCLUSION

A digital background calibration scheme with signal-dependent dithering is applied to a 1.5-bit/stage pipelined ADC based on the standard tri-level MDAC pipeline stage. This technique allows the injection of a large dither without reducing the signal range while keeping the signal-to-dither ratio low. The proposed method calibrates all gain errors resulting from capacitor mismatch, finite opamp gain, and other sources in one step with no strict requirements imposed on analog components. It overcomes both the measurement time and dither magnitude constraints found in the fixed-magnitude PN dithering schemes. Highly accurate calibration up to above 15-bit resolution is demonstrated to be feasible within a practical time without paying significant penalty in the circuit complexity and die area.

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Yun-Shiang Shu (S'05) received the B.S. and M.S. degrees in electrical engineering from National Taiwan University, Taipei, Taiwan, R.O.C., in 1997 and 1999, respectively. Since 2003, he has been working toward the Ph.D. degree in electrical and computer engineering at the University of California, San Diego.

From 2000 to 2002, he was a Design Engineer at ALi Corp., Taipei, where he worked on delta-sigma data converters for audio applications. In Summer 2004 and Summer 2006, he was with Conexant Inc., Palm Bay, FL, designing pipelined and delta-sigma A/D converters for wireless communications. His current research interests include high-resolution, high-speed data converters and techniques used to improve analog-circuit performance with digital aid.

Bang-Sup Song (S'79–M'83–SM'88–F'99) received the B.S. degree from Seoul National University, Seoul, Korea, in 1973, the M.S. degree from Korea Advanced Institute of Science, Daejon, Korea, in 1975, and the Ph.D. from University of California, Berkeley, in 1983.

From 1975 to 1978, he was a Member of Research Staff at Agency for Defense Development, Korea. From 1983 to 1986, he was a Member of Technical Staff at AT&T Bell Laboratories, Murray Hill, NJ, and was also a visiting faculty member in the Department of Electrical Engineering, Rutgers University, New Brunswick, NJ. From 1986 to 1999, he was a Professor in the Department of Electrical and Computer Engineering and the Coordinated Science Laboratory, University of Illinois at Urbana. In 1999, he joined the faculty of the Department of Electrical and Computer Engineering, University of California, San Diego, where he is endowed with the Charles Lee Powell Chair Professor in Wireless Communication. He was a founder and CEO of Wireless Interface Technologies Inc., San Diego, which was later merged with Chrontel Inc., San Jose, CA, in 2003.

Dr. Song received a Distinguished Technical Staff Award from AT&T Bell Laboratories in 1986, a Career Development Professor Award from Analog Devices in 1987, and a Xerox Senior Faculty Research Award from the University of Illinois in 1995. His IEEE activities have been in the capacities of an Associate Editor and a Program Committee Member for IEEE JOURNAL OF SOLID-STATE CIRCUITS, IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS, IEEE International Solid-State Circuits Conference (ISSCC), and International Symposium on Circuits and Systems (ISCAS).