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11.2 3D Ultrasonic Fingerprint Sensor-on-a-Chip

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The increasing popularity of mobile devices such as smart phones in applications including smart payments and personal health sets a pressing need for improved security without compromised ease of use. Fingerprint recognition has emerged as a particularly attractive option. Unfortunately, present capacitive solutions suffer from poor accuracy in the presence of contamination such as perspiration, and in addition are easily compromised, e.g., with fingerprints recovered from the device surface.

The ultrasonic recognizer described in this paper avoids these shortcomings. Figure 11.2.1 shows a block diagram of the device comprising a MEMS wafer with AlN transducers and standard 0.18µm HV CMOS circuits bonded at the wafer level [1]. Each die consists of an array of 110×56 rectangular piezoelectric micromachined ultrasonic transducers (PMUTs) with 14MHz resonance, Q~4, 51.7% fill-factor and 43 and 58µm pitch, corresponding to 582 and 431 dpi resolution, respectively, and covered by a protective PDMS layer. An FPGA controller, ADC, and high-voltage generation are off-chip.

Imaging is based on acoustic time-of-flight and can therefore record both the epidermis and the dermis fingerprints at the surface of the finger and below the skin, respectively. Valleys produce a strong echo at the sensor surface due to the impedance mismatch between air (430Rayl) and PDMS (1.5MRayl). Conversely, the impedance of finger ridges is closely matched to PDMS, resulting in only a weak echo from the sensor surface. Instead, the wave penetrates into finger and is partially reflected at dermis layer beneath the skin.

Readout is column-sequential and begins with a reset phase during which the charge on the S&H capacitor is cleared and the digital circuits are initialized. Imaging starts by first recording a background image. Subsequently, all 56 transducers in the selected column are excited with three 24V pulses at 14MHz, producing an ultrasonic pulse. To increase power and focus, four adjacent columns are excited also with delays adjusted to focus the beam to the desired imaging depth. The returning echoes flex the PMUTs, resulting in a charge on the PMUT electrodes. The charge signals are demodulated with an envelope detector, subtracted from the background and stored on per-row S&H capacitors at the chip output. After a 4µs delay that ensures spurious echoes decay below the noise floor, the readout sequence is repeated a total of three times to improve the SNR. The final 5µs of the column readout are allocated to A/D conversion. Readout takes 24µs per column and 2.64ms for the entire array, translating into a maximum output rate of 380fps. The high operating speed enables continuous verification for high-security applications for example by incorporating fingerprint recognizers into the keys of a keyboard.

Figure 11.2.2 shows an overview and detail of the pixel readout circuits for one of 56 identical rows. To reduce crosstalk, a differential architecture is adopted that pairs the selected PMUT pixel with a replica at the edge of the array. The replicas exhibit the same parasitics, but are not mechanically released and hence are insensitive to acoustic inputs. To reduce capacitive loading, the array is divided into 10 groups with 11 columns each. Switches S_{1a} select the pixel, S_{1b} the replica at the edge of the array that is closest to the selected pixel, and S_{2b} the group. S_{2a} is used to balance the load on either side of the differential pair, consisting of 10 S_{2b} and 2 S_{1b} on the left side of the differential pair and 11 S_{1a} and 1 S_{2a} on the right, respectively. The current source loads, common-mode feedback circuit, and a 2.5× buffer are shared by all pixels in a group.

In transmit mode, the bottom electrode of all pixels is grounded through S_{TX}. A per-column high-voltage level shifter and latch applies pulses to the top electrodes of the selected columns. During readout, the level shifter is programmed to ground the top plates of all pixels and S_{TX} is opened. This switching scheme isolates the bottom plate readout electrode from the parasitics of the high-voltage devices used to implement the level shifter and latch, avoiding signal attenuation. Since S_{TX} sees only low voltages, it can be realized with a low-voltage switch with low parasitic capacitance.

The size of the feedback capacitor C_f is approximately equal to the capacitance of the transducer (35fF) resulting in approximately unity gain. Readout occurs in two steps. First, the reset switch S_{res} is closed and the offset of the readout circuits stored on interstage coupling capacitors that are part of the 2.5× and 20× amplifiers. In the second step, S_{res} is opened and the received waveform amplified for processing by the demodulator.

Figure 11.2.3 shows the circuit diagram of the demodulator, which rectifies the received signal V_{dem} from pixel readout circuit. The S&H is used for CDS and for averaging three images to improve the SNR. Adjusting the precise sampling point t_{sig} of the rectified envelope signal selects the imaging depth, facilitating the acquisition of separate images for the epidermis and dermis. The built-in demodulator greatly reduces the ADC sampling rate, enabling fast readout with low power consumption. The chip consumes 280µJ to record an entire fingerprint at one depth setting or 280µW at 1fps continuous operation. This reduces to 2.5µJ per measurement or 25µW at 10 fps in wakeup mode, where data is acquired from only one column to detect the presence of a finger, at which point a full image is recorded.

Figure 11.2.4 shows recorded fingerprint images under clean conditions, and with perspiration and oil. Contamination results in only marginal degradation of image quality. Also shown are optical images of the sensor after the finger has been removed. Although the fingerprint is clearly visible, the reader unambiguously distinguishes it from an actual finger and corresponding echoes. This feature guarantees robustness against spoofing attacks and ensures high security. The measurements also confirm that images are not affected by previously taken recordings.

The ability to record features inside the finger further adds to the ability of the sensor to operate under adverse conditions and guards against spoofing attacks. Figure 11.2.5 shows images with delay set in the demodulator to 750 and 870ns, to record the epidermis and dermis at the sensor surface and 90m depth, respectively. While the surface pattern can still be seen, additional features from the dermis are clearly visible for the real finger but absent in the image from a silicone phantom that does not model the dermis. The bottom row shows the image from a phantom with diagonal lines at the surface and a logo inside. The logo is partially obscured by surface features and has lower resolution due to beam spreading. The ability to record both epidermis and dermis fingerprints improves the reliability of the device in situations where the epidermis image if faint due to genetics or physical damage and enhances security by rejecting spoofing attacks with mockups that lack the full 3D characteristics and acoustic properties of real fingers.

Figure 11.2.6 compares this work to other solutions. The sensor in [2] images a larger area but being capacitive does not offer the insensitivity to contamination and added security of 3D acoustic imaging. Reference [3] describes an ultrasonic fingerprint recognizer with only a single column and that is not integrated. A complete image is recorded by swiping the finger across the sensor. The result in [4] uses a bulk piezo transducer with lower resolution and is capable only of 2D recording. Lack of integration translates into a considerably larger size.

Figure 11.2.7 shows a die photograph of the CMOS readout circuits before wafer bonding and an SEM of a cross-section of the bonded device, partially contaminated by the epoxy filling used to prepare the cross-section. The eutectic bond doubles as mechanical support and electrical interconnect.

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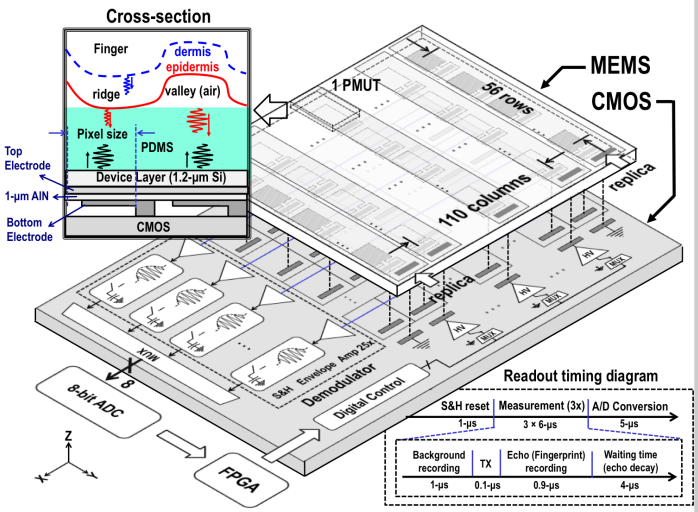

Figure 11.2.1: Block diagram and cross-section of the ultrasonic fingerprint sensor comprising MEMS and CMOS bonded at the wafer level.

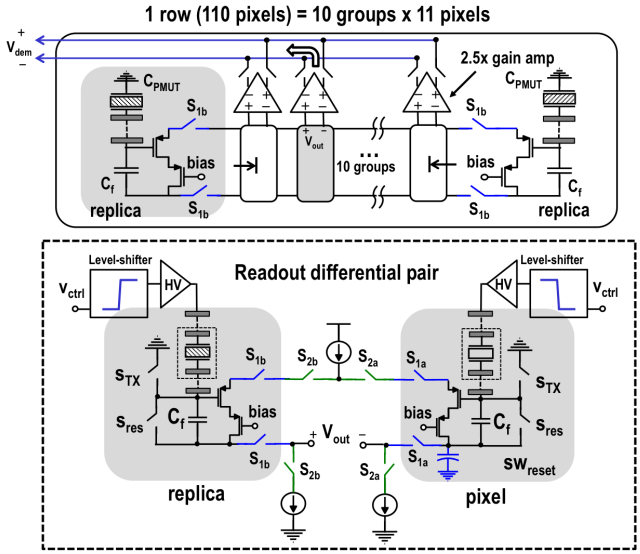

Figure 11.2.2: Readout circuits.

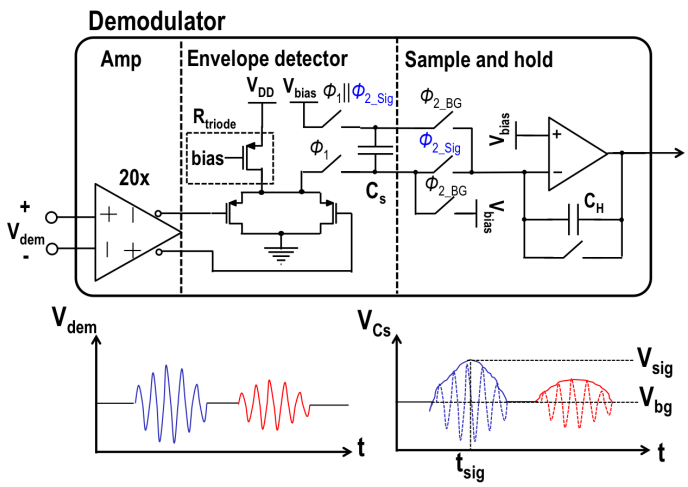

Figure 11.2.3: Circuit diagram and waveforms of the demodulator.

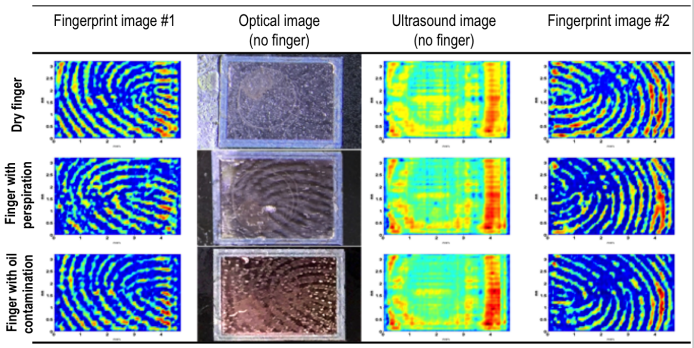

Figure 11.2.4: Recorded fingerprint images with clean and contaminated finger.

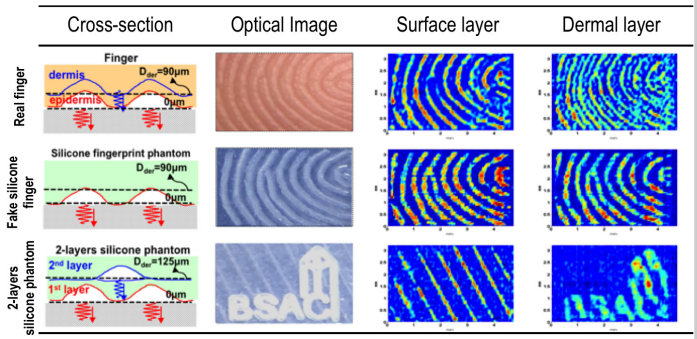

Figure 11.2.5: 3D images.

	This work	ISSCC'08 [2]	Jsensor'10 [3]	IUS' 04 [4]
Method	Ultrasonic (Pulse-Echo)	Capacitive	Ultrasonic (Pulse-Echo)	Ultrasonic (Impediography)
Process	0.18um CMOS + MEMS, wafer-bonded	0.5um CMOS	Discrete electronics + MEMS	Discrete electronics + MEMS
Imaging capability	3D image	2D image	3D image	2D image
Transducer	PMUT	Capacitor	CMUT	Bulk Piezo
Array size	110 x 56 pixels 4.73 x 3.25 mm^2	224 x 256 pixels 11.2 x 12.8 mm^2	1 x 192 pixels 0.11 x 21.5mm^2	64 x 64 pixels 8.06 x 8.06 mm^2
Pixel size	43 x 58 μm^2 (591 x 438 dpi)	50 x 50 μm^2 (508 x 508 dpi)	112 x 112 μm^2 (227 x 227 dpi)	126 x 126 μm^2 (250 x 250 dpi)
Image contrast	5.53:1	2.43:1	N/A	5:1
Frame rate	380 frame/sec	N/A	N/A	50 frame/sec
Energy per measurement	280uJ	25mW÷ frame rate	N/A	N/A

Figure 11.2.6: Comparison table.

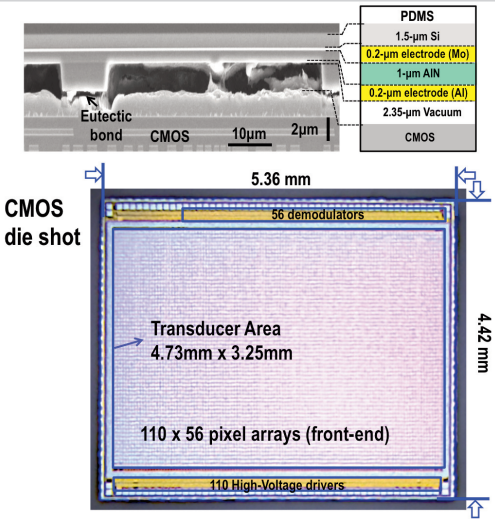

Figure 11.2.7: Die photo of CMOS before wafer bonding and cross section of the fingerprint sensor.

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