Low-Power Single-Ended SAR ADC Using Symmetrical DAC Switching for Image Sensors With Passive CDS and PGA Technique

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***Abstract*— An integrated, power-saving SAR analog-to-digital converter suitable for image sensor applications is presented in this paper. In comparison with previous works, the proposed, build-in passive correlated double sampling (CDS) and programmable gain amplifying (PGA) technique is superior in power, as it achieves correlated noise cancellation and signal amplification without additional OTAs. Furthermore, inspite of a single-ended signal from the image sensor array, single-ended-to-differential sampling is used to enable symmetrical DAC switching. The adopted LSB-first algorithm, utilizing the strong correlation between neighboring pixels, significantly reduces the energy and number of bitcycles per conversion. Additionally, a comparator with four inputs is adopted to keep the DAC array unchanged, avoiding power consumption from the operation of the initial guess for next quantization. Fabricated using a 65-nm process, the 10-bit ADC occupies a die area of 0.19 mm^2. The measured DNL and INL are less than +0.68/−0.45 LSB and +1.07/−1.15 LSB, respectively. Operating at 40 MS/s, the ADC provides an SNDR of 55.7 dB and SFDR of 70.9 dB for signal bandwidths of 17.2876 MHz and consumes 415.2 μW from a 1.2-V power supply, resulting in a figure of merit of 21.7 fJ/conversion-step. Additionally, the CDS and PGA functionality are verified to be effective in removing reset level influence and providing gains of −6 dB, 0 dB, and 6 dB.**

***Index Terms*— Image sensor, analog-to-digital converter (ADC), single-ended-to-differential sampling, correlated double sampling, programmable gain amplifying, successive approximation (SA), image-dependent power savings.**

I. Introduction

THE market demand for electronic image sensors, such as charge-coupled devices, CMOS image sensors, and recently, pinned photodiodes, is continuously increasing [1]–[3]. In many applications including but not limited to remote imaging, mobile devices, wearable devices, and biomedical devices, low-power image sensors and readout schemes are greatly expected. Power consumption is one of the main design constraints [4]. Studies have shown that most of the energy is consumed by readout schemes [5], which include key blocks such as a correlated double sampling (CDS) circuit, a programmable gain amplifier (PGA) and column-parallel analog-to-digital converters (ADCs) [6], [7]. Owing to the limitation resulting from noise, a CDS readout scheme is essential. It is used to extract the voltage difference between the reference level and the data level of each pixel to remove any low frequency noise, which appears as a constant or is correlated to both signals [2]. Further, PGAs are also necessary to maximize the dynamic range of the ADCs in weak-light conditions. However, these two blocks consume substantial amount of power. The individual CDS chip and PGA chip dissipate approximately half of the total power of an AFE [8]. Although a combination of CDS and PGA [9] [10] achieves conciseness and efficiency, the power consumption of an active amplifier is not negligible. The digital CDS that performs a subtraction between signal data and reset data in the digital domain is introduced for better noise cancellation and power saving [2], [11]. However, a PGA is still required to modulate the signal from the image sensor. To reduce the total power consumption, one can make efforts to reduce power in the CDS and PGA blocks or modify the ADC structures and operations to achieve functionality of the CDS and PGA with or without a system level power saving.

On the other hand, low-power column-parallel ADC designs for image sensors are extensively available in literature. Single-slope ADCs have been widely used owing to their simplicity, small area, and high linearity [7], [12], however, the conversion time exponentially grows as the resolution increases. For example, an N-bit conversion requires $2N$ clock cycles, limiting the frame rate of image sensors. Recently, various single-slope-based two-step ADCs [13]–[15] and hybrid ADCs [16], [17] have been developed to solve the problem of conversation speed. However, it consumes more power owing to multiple-ramp generators [14]. The SS/SAR ADC in [16] and SAR/SS ADCs in [17] convert the pixel output into the upper bit using the SS ADC and the SAR ADC, respectively. However, some problems exist: many accurate reference voltages are required for the SAR ADC to achieve high resolution [16]; ADC is vulnerable to the error in the step size of the ramp signal and the gain error of the capacitor DAC [17]. As alternative solutions, Δ-$\sum$ ADCs and cyclic ADCs exhibit superior noise performance and faster conversion speed, respectively [18], [19]; however, both of them require high power-consuming operational amplifiers, even if self-biasing and OTA sharing technology for lower power are

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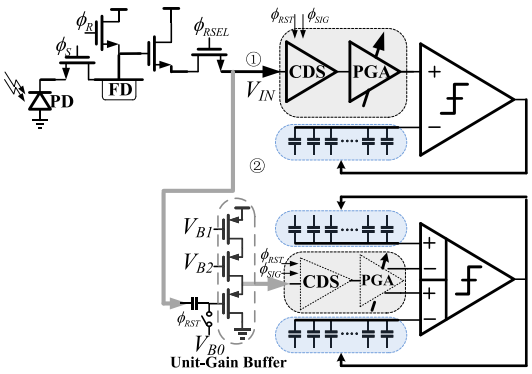

Fig. 1. Block diagram of the proposed SAR ADC and conventional one with image sensor arrays.

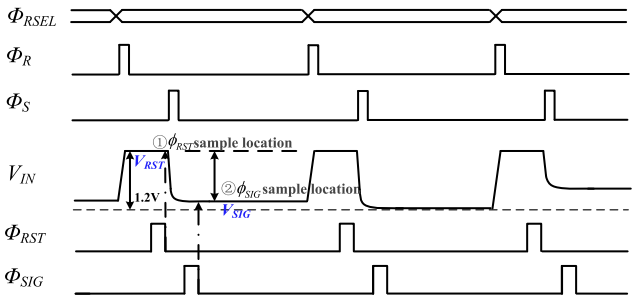

Fig. 2. Operational timing diagram of the SAR ADC.

used [20]. All the above approaches are proposed to follow the traditional ADC operation and optimization for achieving good performance in quantizing pixel data. However, two general characteristics of pixel signals should be considered for further power saving and better performance.

First, the neighboring pixels are strongly correlated with each other, and Δ_{pixel} of two adjacent pixels shows relatively small values compared to the absolute gray values [4], [5]. Therefore, power-efficient delta-readout algorithms that reduce the operation cycle and cyclic power should be used. Second, image sensor generates a single-end signal. This results in a power supply and signal handling capability limitation in the ADC, which is implemented in a single-ended configuration to handle a large single ended voltage signal. Reducing the power supply voltage for lower power is not acceptable owing to the requirement of a high dynamic range. In addition, a single-ended ADC structure has inferior supply and substrate rejection in comparison with a differential structure.

Inspired by previous works and features of pixel signals, this paper presents a new SAR ADC for image sensor that is superior to other ADCs in power consumption. The proposed SAR ADC takes in a single ended pixel signal and converts it into a fully differential signal for quantization. As the difference between two adjacent pixels is small, the ADC can utilize the quantized result of the previous pixel as an initial guess for the sampled value of the following pixel. Here, the designed ADC quantizes the pixel data using the LSB-first algorithm to reduce the operating cycle and power consumption. In addition, CDS and PGA for input signals are performed utilizing passive capacitance, which does not involve any extra power consumption. The paper is organized as follows. Section II describes and analyzes the key technology for the proposed ADC. Implementation details of ADC and key block circuits are described in Section III. The experimental results measured from the prototype are presented in Section IV. Section V presents the conclusions.

II. Proposed Key Technology

A. Proposed SAR ADC Topology

The image sensor signals are generally single-ended signals, which consist of the reset level and signal level, and two parts have the same noise component. A SAR ADC for image sensor application can be implemented in either a fully-differential [1] or single-ended [4] topology. Although a single-ended SAR ADC is always favored in area and power constrained circuit systems, it is inferior in common-mode noise rejection, distortion performance, and voltage swing. A conventional N-bit single-ended SAR ADC, together with the additional CDS and PGA for image sensors is illustrated in the upper part of Fig. 1 and receives the signal through route ①. The input signals are sampled and amplified by CDS and PGA, respectively. The comparator compares the polarity of the reference and input signal, where the reference voltage is generated via the capacitor array. The proposed SAR ADC is shown in the lower part of Fig. 1, and the key idea of this architecture is to achieve SDS, CDS and PGA functionality through passive capacitance. A board-level unit-gain buffer (source follower) is adopted in front of the ADC to drive the sampling capacitance of ADC. Its static current is 10 mA in the supply voltage of 2.5 V. A symmetrical DAC switching technique is adopted here. The ADC receives the single-end image sensor signal through routed ② and converts it into a differential signal through a SDS operation for better common mode rejection during the quantization process; then the four-input comparator outputs the digital code and controls the DAC arrays to approximate the input signal successively. Owing to the passive CDS and PGA, the ΔV_{IN} of the input signal is obtained and amplified to allow relaxed comparator noise and faster settling speeds of the comparator. More importantly, no more extra power except for board-level source follower is consumed in comparison with the conventional ADCs using active amplifier. Fig. 2 shows the corresponding operational timing diagram of the ADC for image sensor application. The pixel enabled in phase Φ_{RSEL} generates the reset value V_{RST} after Φ_R, so that CDS block could sample it by Φ_{RST}. Then the pixel signal value V_{SIG} appearing on V_{IN} after Φ_S is sampled by Φ_{SIG}, making ΔV_{IN} is obtained as a result of CDS operation.

B. Proposed Passive Capacitance Technology

This part describes the key concept of the proposed built-in passive CDS, PGA and SDS technology for SAR ADC. Based on the characteristics of the image sensor signals, the proposed SAR ADC achieves passive SDS, CDS and PGA as shown in Fig. 3. In the phase Φ_{RST} of sampling phase, the reset

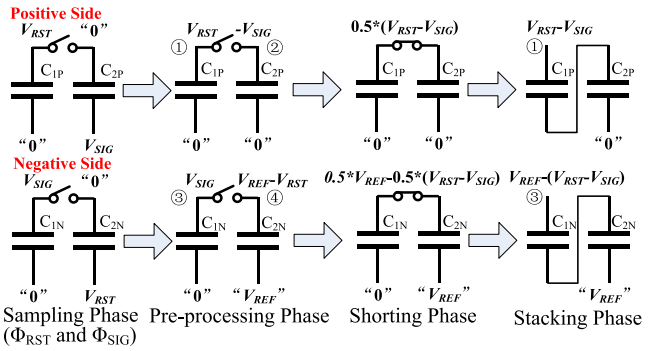

Fig. 3. Proposed passive capacitance technology.

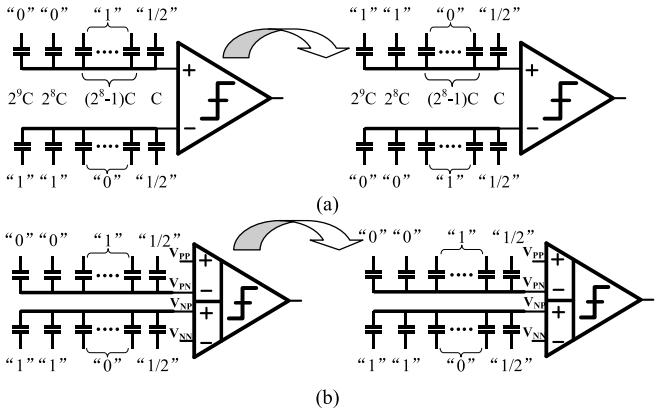

Fig. 4. The switching procedure for the initial guess of the next V_{IN}. (a) The conventional switching procedure and structure. (b) The proposed switching procedure and structure.

signal V_{RST} is sampled on the top plate and bottom plate of capacitances C_{1P} and C_{2N} on the positive and negative sides, respectively. While in the phase Φ_{SIG} of sampling phase, the data signal V_{SIG} is sampled on the bottom plate and top plate of capacitances C_{2P} and C_{1N}, respectively. Then in the pre-processing phase, the bottom plates of C_{2P} and C_{2N} are connected to *GND* and V_{REF}, respectively. Therefore, after the pre-processing phase, the voltages of point ① and ② on the positive side are equal to V_{RST} and $-V_{SIG}$, while the voltages of points ③ and ④ on the negative side are equal to V_{SIG} and $V_{REF} - V_{SIG}$. In the shorting phase, the points ①, ② and ③,④ are connected together and voltages turn into $0.5 \times V_{RST} - V_{SIG}$) and $0.5 \times V_{REF} - 0.5 \times V_{RST} - V_{SIG}$). Finally, after the capacitor stacking operation in stacking phase, the output voltages of points ① and ③ are twice of that in the shorting phase, which equal $(V_{RST} - V_{SIG})$ and $V_{REF} - (V_{RST} - V_{SIG})$, respectively. After the sampling capacitance is settled completely, the comparator compares the differential voltage and quantizes it by successive approximation. Here, it is worth nothing that: firstly, $\Delta V_{IN} = V_{RST} - V_{SIG}$ is obtained. As the noise components of V_{RST} and V_{SIG} are the same, the CDS functionality reduces noise influence to improve the precision; secondly, the sampled single end input ($V_{RST} V_{SIG}$) and its complementary signal $V_{REF} - (V_{RST} - V_{SIG})$ are obtained after the stacking phase; thirdly, after capacitor stacking, the voltage is twice the previous value. Therefore, the SDS, CDS and PGA functionality are obtained without the additional amplifier.

C. Proposed Power-Efficient DAC Method

Recently, considering the strongly correlated characteristics between two continuous samplings of input signals, many SAR ADCs have been designed taking advantage of the previous digital output code [21], [22]. A significant amount of power is saved if the input signal has low activity. However, the power consumed by the operation of initial guess could not be ignored. As an example shown in Fig. 4 (a), the bottom plates of V_P in the DAC array of conventional SAR ADC should be transferred from "0011…" to "1100…" for the initial guess. It is observed that the power consumed by this operation is 766 CV^2, where C is the unit capacitance. The proposed SAR ADC shown in Fig. 4 (b), which adopts the comparator with four inputs to separate the input terminals from the DAC arrays, achieves power saving by keeping the DAC array unchanged. The quantization for the next sampling of input signals begins directly without the operation of the initial guess. The details of the switching procedure are described in Section III.

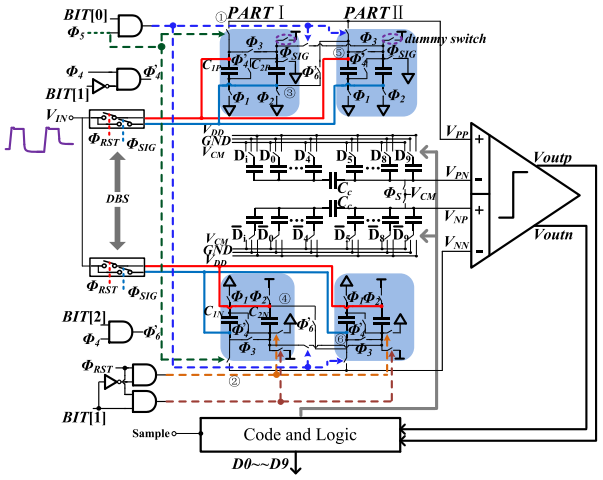

Fig. 5. The block diagram of the proposed SAR ADC.

III. Proposed SAR ADC Implementation

The input signal from the image sensor is sampled by a bootstrapped switch. The sampling capacitor with embedded CDS, PGA, and SDS functionality and a DAC capacitance array are followed by a two-stage comparator, which also generates quantization code and provides a data-ready signal needed for the asynchronous SAR operation. In the following subsections, we will elaborate on the implementation and practical design considerations of the key building blocks for the proposed SAR ADC.

A. Proposed SAR ADC Structure

As shown in Fig. 5, the proposed SAR ADC samples the image sensor signal V_{IN} through the bootstrap switch, which has Φ_{RST} and Φ_{SIG} as sampling clocks to make a correlated

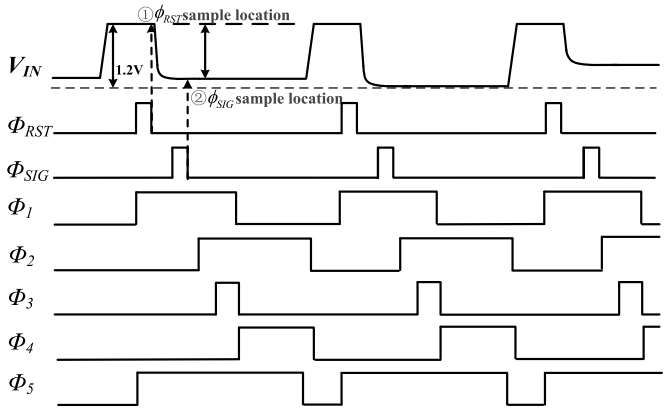

Fig. 6. Timing diagram of the proposed SAR ADC.

TABLE I
DIGITAL CONTROL WORD FOR GAIN CONTROL

BIT[0]	BIT[1]	BIT[2]	GAIN
1	1	0	-6 dB
1	0	0	0 dB
0	0	1	6 dB

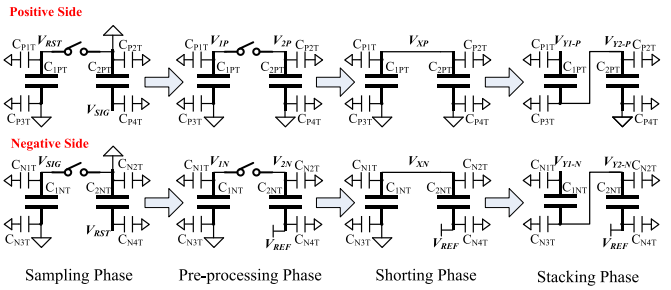

Fig. 7. Parasitic capacitors in the proposed sampling network.

double sampling for ΔV_{IN} and removing the fixed noise component. Two sampling positions are located in the reset level and data level, respectively, as shown in Fig. 6. The sampling capacitor is divided into two identical parts *PART I* and *PART II*, and each part contains the capacitor C_{1X} and C_{2X} (X = P, N). In the sampling phase, the input signals are sampled by the capacitances in *PART I* and *PART II*, respectively. A sampled voltage error $V_{\rm err} = (2\pi\ f_{\rm IN} V_{\rm FS}/2)*\Delta t_{\rm skew}$ owing to the different sampling paths via *PART I* and *PART II* is observed; here, $\Delta t_{\rm skew}$ is the aperture delay difference between the two paths [23]. To ensure that the aperture delay difference is less than half LSB of the ADC, the complexity in circuit design and layout is apparent. However, the input image signal of the proposed ADC remains constant during the sampling phase; thus, the specific attentions are not required here. The 3-bit digital control word *BIT[0:2]* is used to set the programmable gain varied from −6 dB to 6 dB in 6-dB step, as listed in Table I. Taking 0 dB as an instance, when Φ_{RST} is high, the voltage V_{RST} of the input signal V_{IN} is sampled on the top plate of capacitor C_{1P}. The bottom plate of capacitor C_{1P} is connected to *GND*. Meanwhile, the bottom plate of capacitor C_{2N} connects to V_{RST}. The top plate of capacitor C_{2N}, which is controlled by digital *BIT[1]*, connects to *GND* in the situation involving 0 dB (where *BIT[1] = 0*). Then the signal level V_{SIG} of the input signal V_{IN} are sampled by the bottom plate of capacitor C_{2P} and top plate of capacitor C_{1N} during sampling phase Φ_{SIG}, respectively. When Φ_2 is high, the bottom plates of C_{2P} and C_{2N} connect to *GND* and V_{REF}, respectively. Thus, the top plates of C_{2P} and C_{2N} turned into $-V_{SIG}$ and $V_{REF} - V_{RST}$, respectively. During the phase Φ_3, the top plates of the capacitance in each part are connected together. Thus, the voltage V_{PP} becomes $1/2 * \Delta V_{IN}$ during phase Φ_3, where $\Delta V_{IN} = V_{RST} - V_{SIG}$. Similarly, V_{NN} becomes $1/2*V_{REF} - \Delta V_{IN}$). In phase of Φ_4, the passive amplification is enabled by stacking the capacitors C_1 and C_2. The voltage V_{PP} transforms from $1/2*\Delta V_{IN}$ into ΔV_{IN}. On the other side of the comparator, the voltage V_{NN} equaling $V_{REF} - \Delta V$ is obtained. Then the comparator makes a comparison between $V_{PP} - V_{PN}$ and $V_{NP} - V_{NN}$; the output digital code controls the binary DAC capacitor array to generate the corresponding reference voltage, which finally has a distinction less than 1 LSB with the input. The DAC capacitor array is switched according to the LSB-first timing algorithm, and its top plates are connected into V_{CM} at the beginning of the quantization process. The proposed SAR ADC provides three gain settings for input signals with different dynamic ranges. When a ΔV_{IN} exceeding the range of V_{REF} is applied to the ADC, the digital control word *BIT[0:2] = 110* and the programmable gain is −6 dB. The voltage of V_{PP} and V_{NN} equal $1/2*\Delta V_{IN}$ and $V_{REF} - 1/2 * \Delta V_{IN}$, respectively. When ΔV_{IN} with small amplitude is applied, it is necessary to provide amplification through *BIT[2]*. The sampling capacitor arrays, *PART I* and *PART II*, are connected together through Φ_6' to achieve a 6 dB gain, and the voltage of $V_③$ changes from 0 to ΔV_{IN}. According to the charge conservation principle, $V_①$ would increase from ΔV_{IN} to $2 * \Delta V_{IN}$. Meanwhile, the voltage of $V_②$ changes from $V_{REF} - \Delta V_{IN}$ to $V_{REF} - 2\Delta V_{IN}$.

According to the above content, the passive capacitance technology looks quite nice for ideal capacitor. However, the difference of the parasitic capacitance in top-plate and bottom-plate of the sampling capacitance has a non-negligible influence in practice. Next, we will examine the gain error due to parasitic capacitors in the proposed sampling network. We redraw Fig. 3 with parasitic capacitance in Fig. 7, where C_{PXT} and C_{NXT} stand for the total parasitic capacitance in its corresponding node. In the positive side of Fig. 7, the top-plates of C_{1PT} and C_{2PT} (which consist of C_{1P} and C_{2P} in *PART I* and *PART II*, respectively.) are connected together after sampling phase, pre-processing phase and shorting phase. The voltage V_{XP} can be obtained as

$$V_{XP} = \frac{V_{RST}\ (C_{1PT} + C_{P1T}) - V_{SIG} C_{2PT}}{C_{1PT} + C_{P1T} + C_{2PT} + C_{P2T}} \tag{1}$$

The sampling capacitance C_{1PT} and C_{2PT} are stacked subsequently in stacking phase. And the node voltage V_{Y1-P} is

$$V_{Y1-P} = V_{XP}\ [\frac{C_{1PT}\ (C_{2PT} + C_{P2T})}{(C_{1PT} + C_{P1T})(C_{2PT} + C_{P2T} + C_{P3T})} + 1] \tag{2}$$

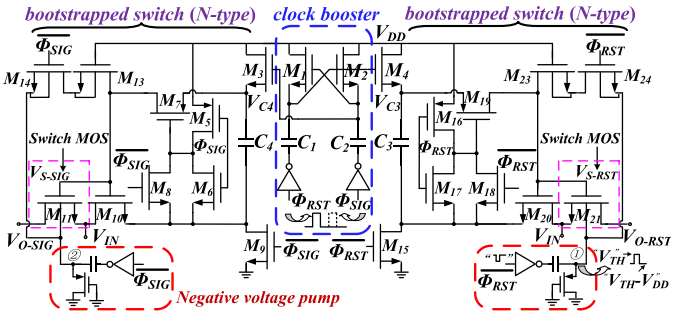

Fig. 8. The bootstrap switch for double sampling.

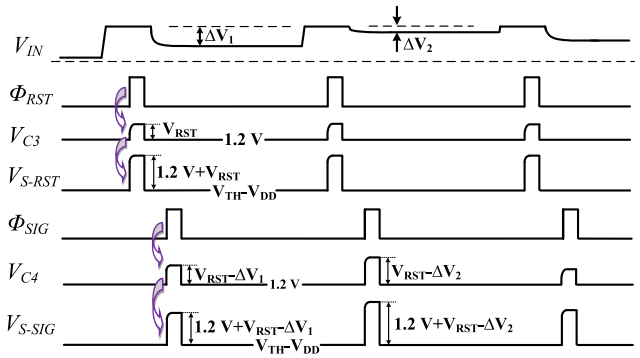

Fig. 9. The timing diagram of the bootstrap switch.

Similarly, in the negative side of Fig. 7, the node voltage V_{Y1-N} can be obtained as

$$V_{Y1-N} = V_{XN}\ [\frac{C_{1NT}\ (C_{2NT}+C_{N2T})}{(C_{1NT}+C_{N1T})(C_{2NT}+C_{N2T}+C_{N3T})}+1] \quad (3)$$

where

$$V_{XN} = \frac{V_{SIG}\ (C_{1NT}+C_{N1T})+(V_{REF}-V_{RST})C_{2NT}}{C_{1NT}+C_{N1T}+C_{2NT}+C_{N2T}} \quad (4)$$

According to Fig. 5, the sampling capacitance and switches are designed symmetrically with the same sizes, and a dummy switch with the same size as the extra switch for V_{REF} in the top-plate of C_{2NT} is adopted in top-plate of C_{2PT} for keeping the same parasitic capacitance value of C_{P2T} and C_{N2T}. As $C_{P2T} = C_{N2T}$, and $C_{1NT} = C_{1PT} = C_{2NT} = C_{2PT}$, $C_{P1T} = C_{N1T}$, $C_{P2T} = C_{N2T}$, $C_{P3T} = C_{N3T}$, the sampled input differential voltage $V_{diff} = V_{PP} - V_{NN} = V_{Y1-P} - V_{Y1-N}$ can be calculated as after the stacking phase.

$$V_{diff} = V_{PP} - V_{NN} = k[(2+\frac{C_{P1T}}{C_{1PT}})V_{IN} - V_{REF}] \quad (5)$$

where $V_{IN} = V_{RST} - V_{SIG}$, and k can be calculated as

$$k = \frac{C_{1PT}}{C_{1PT}+C_{P1T}+C_{2PT}+C_{P2T}} \times [\frac{C_{1PT}\ (C_{2PT}+C_{P2T})}{(C_{1PT}+C_{P1T})(C_{2PT}+C_{P2T}+C_{P3T})}+1] \quad (6)$$

Combining Equation (5) (6), therefore, a gain error exists inevitably due to the parasitic capacitance in practice. It can be regarded as a fixed gain error and does not affect the dynamic performance obviously. Additionally, the finger typed metal-oxide-metal (MOM) capacitor is used as the sampling capacitances instead of MIM cap for same parasitic capacitance in two plates. Every metal layer of the symmetrical MOM capacitor consists of both top- and bottom-plate, hence, both plates observe the same parasitic capacitance with respect to ground. On the other hand, the designed shielding structure, which consists of bottom poly shield and side-wall metal shield, is incorporated into the sampling capacitor, reducing the undesired parasitic capacitance for substrate and routing lines. Meanwhile the designed MOM capacitance has a density of 3fF/μm^2, superior to the 1-2fF/μm^{2}of MIM cap, reducing the capacitance area.

B. Bootstrap Switch for Double Sampling

The adopted bootstrap switch is shown in Fig. 8, and the timing diagram is shown in Fig. 9. The bootstrap switch consists of a common clock booster and two N-type bootstrapped switches, avoiding the use of two independent bootstrapped switches, which would increase the required chip area and power consumption. The operating procedure is described as follows. When $\Phi_{RST}$is high, M_4 and M_{15} is off, and the capacitor C_3 is connected between the gate and source of the sampling-switch transistor M_{21} to provide a constant V_{GS}, which equals V_{DD}. The output voltage V_{O-RST} tracks with the input voltage V_{IN}(equaling to V_{RST}). When Φ_{RST} is low, the capacitor C_3 is recharged through transistors M_4 and M_{15}. Similarly, in the data sampling phase, $\Phi_{SIG}$is high, M_3 and M_9 is off, the capacitor C_4 is connected between the gate and source of the switch M_{11}. The gate voltage V_{S-SIG} of M_{11} equals $V_{SIG}+1.2$, where $V_{SIG} = V_{RST} - \Delta V$. Thus the input voltage V_{IN} (equaling to V_{SIG}) is tracked and sampled. When Φ_{SIG} is low, the capacitor C_4 is recharged through transistors M_3 and M_9.

The influence of low V_{TH} is obvious, which results in a substantial increase in the sub-threshold leakage current. In order to reduce the leakage current [18], V_{GS} or V_{DS} may be reduced or V_{TH} may be increased [18]. Instead of a connection to *GND*, a negative substrate bias is generated by a negative voltage generator to reduce the sub-threshold leakage current [24]. The negative voltage pump uses a PMOS to generate negative voltage approximating to $V_{TH} - V_{DD}$. In the data sampling phase, for example, when Φ_{SIG} is high and Φ_{RST} is low, the voltages in ① and ② are $V_{TH} - V_{DD}$ and V_{TH}, respectively. For reducing the leakage current of M_{21}, the bulk connects to negative voltage. Meanwhile, the gate of switch transistor M_{21} is connected to the point ① through M_{23} and M_{24}. Fig. 10 shows a summary of drain leakage currents for a normal switch transistor with gate and bulk connecting to *GND*, a switch transistor with only negative bulk voltage and the proposed one with negative gate and bulk voltage. It is apparent that the drain leakage currents increase with the value of V_{ds}, and the leakage current reduces greatly when the negative voltage is applied on the gate and bulk synchronously. It is very meaningful that in the image sensor application, the reset level and signal level are sampled in the Φ_{RST} and Φ_{SIG} phases, respectively. And the difference

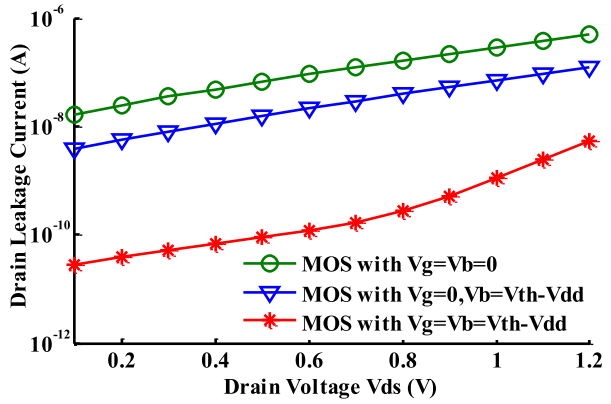

Fig. 10. Comparison of leakage current in switch MOS with size of 35um/60nm.

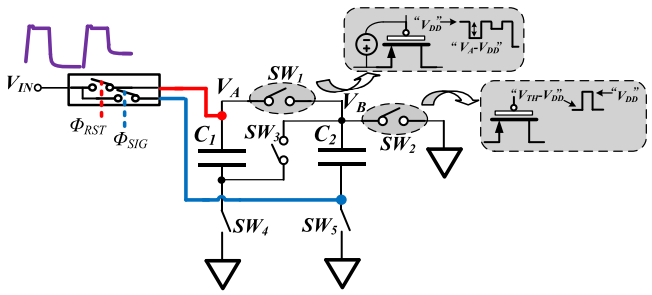

Fig. 11. Specific switch for sampling capacitance in the proposed SAR ADC.

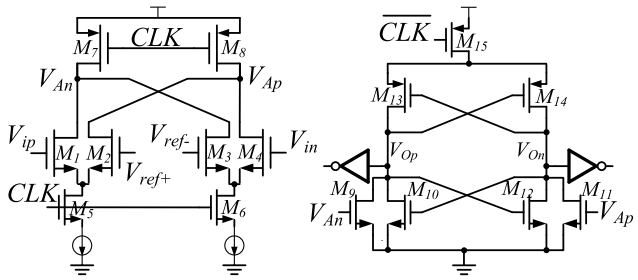

Fig. 12. The adopted four-input comparator.

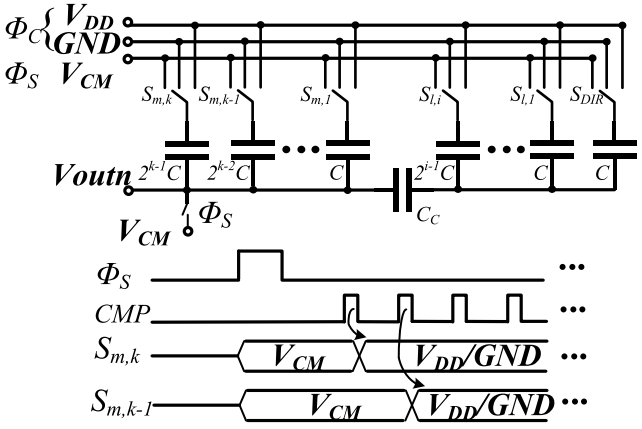

Fig. 13. Single-ended split capacitive DAC arrays and its switching timing diagrams for first quantization process using the V_{CM}-based switching method.

value ΔV ($\Delta V = V_{RST} - V_{SIG}$) varies from 0 to 1.2 V. Therefore, the V_{ds} of a switch transistor (which is in the "off" situation) might be very large, resulting in an error caused by the leakage current. In order to minimize the errors introduced by the leakage current, the switch MOS transistors M_{11} and M_{21} must exhibit a good performance in the "off" state. The bootstrap switch connects bulk and gate of the switch MOS to the negative voltage so as have an obvious degradation in drain leakage current.

In addition, some switches of the proposed SAR ADC are designed carefully to guarantee their stability during the sampling phase. As shown in Fig. 11, the switch SW_5 is on and SW_2 is off after the sampling phase Φ_{SIG}. The voltage V_B changes from 0 to $-V_{IN}$, which would cause improper operation of the switch SW_2. In such a case, an NMOS switch transistor would start to conduct current when it should be off. To ensure proper operation, a PMOS transistor with a thick oxide layer is used as SW_2 to prevent the incorrect conduction. Additionally, a negative voltage $V_{TH} - V_{DD}$ is used to conduct switch during Φ_{SIG}. Similarly, a PMOS transistor with bootstrapping functionality is used as SW_1, which keeps a constant $V_{GS} = -V_{DD}$ to conduct the voltage V_A and V_B sufficiently when SW_1 is "on".

C. Comparator

Fig. 12 shows the double-tail latch type comparator that is adopted for the proposed SAR ADC. The comparator consists of a pre-amplifier and a latch. The pre-amplifier with four input terminals is used, rather than two single-ended inputs in the conventional op-amp. When the clock signal *CLK* is low, the input stage and latch are reset, with V_{An} and V_{Ap} being high and V_{On} and V_{Op} being low. When *CLK* is high, the input stage compares the $V_{ip} - V_{ref+}$ and $V_{in} - V_{ref-}$. Then, the latch with positive feedback forces one output to high and the other to low according to the comparison result.

D. DAC Array Implementation and Switch Procedure

The single-ended structure of the proposed capacitive DAC array is depicted in Fig. 13, which provides the reference voltage. The DAC is implemented as the 5-bit MSB and the 5-bit LSB arrays with fewer unit capacitors and a smaller silicon area compared to a regular capacitor array. In this design, the unit capacitance is designed to be 50 fF. The maximum equivalent capacitance observed between the top and the bottom plates of the capacitor array is 32C. Ideally, the value of capacitor C_C is 32/31 unit capacitor. This compresses the entire range of the sub-DAC into one main-DAC LSB, thus allowing the sub-DAC to provide a 5-bit interpolation between the main-DAC LSBs. In reality, C_C is increased by an enlarging factor of 1.1 times to compensate for the impact of the parasitic capacitance at the top plate of the sub-DAC [26], [25]. Through post-simulation, the C_C is obtained as 56.8 fF. In addition, for improving the matching accuracy and reducing the process variation, the DAC is implemented using MOM capacitor array. In this prototype, we use a multi-finger capacitor structure, and the number of fingers is chosen judiciously such that the fractional C_C can be achieved

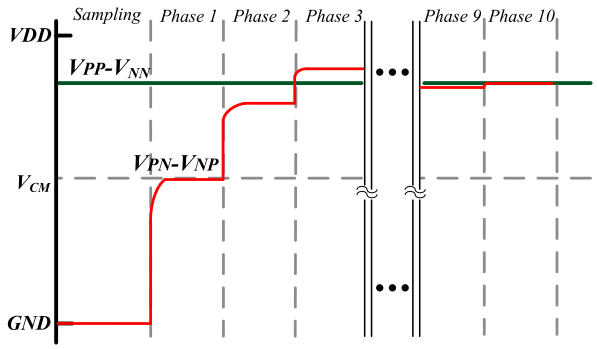

Fig. 14. Waveform of the DAC output in the quantization process for the first pixel data.

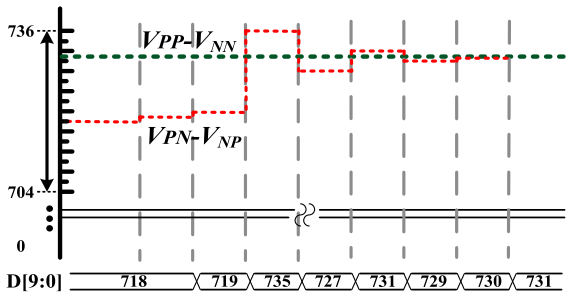

Fig. 15. Example 10 bit conversions for the neighboring pixels data using the LSB-first SA algorithm.

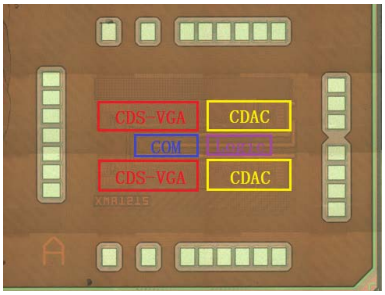

Fig. 16. Die microphotograph of the fabricated SAR ADC.

with identical finger lengths but a different number of finger segments.

The characteristic of Δ_{pixel} is strongly correlated between the neighboring pixels [4]. The ADC presented here adopts the LSB-first algorithm to quantify the pixel data, which starts with an initial guess of the current sample's value and bitcycles LSBs first instead of MSBs as in the conventional SA. Fig. 14 depicts the DAC voltage V_{DAC} during 10-bit conversion for the first quantization process of the pixel data, and the V_{CM}-based switching method is used [27]. As shown in Fig. 13, the DAC array varies as follows: in the Φ_S phase, the top plates of the MSB capacitor array and the bottom plates of the DAC capacitor array are connected to V_{CM}. The switches $S_{m,k}$, $S_{m,k-1}$,... is connected to V_{CM}. Then in the converting phase Φ_C, the comparator makes a comparison when CMP is high, and the comparator output decides the switch logic of DAC array, which translate the bottom plate of the capacitor from V_{CM} to V_{DD}/*GND*. The DAC output can be calculated (7), as shown at the bottom of this page, where C_M and C_L are the sum of the capacitance in the 5-bit LSB and the 5-bit MSB arrays, respectively. The DAC digital input $X = [S_{l,n},...S_{m,n}]$, with S_x equals to 1 or -1 represents the DAC connecting V_{DD} or GND. And S_{DIR} equals to 0, meaning that DIR capacitance connects V_{CM} in the first quantization process. After ten quantization phases of the first pixel, the DAC output voltage $V_{PN} - V_{NP}$ approaches the input voltage $V_{PP} - V_{NN}$ step-by-step and finally the error between them becomes less than 1 LSB. To reduce power consumption and the number of cycles, the proposed ADC takes advantage of the correlation between neighboring pixels, according the LSB-first algorithm [2]. When the ADC samples the next neighboring pixel data, the reference voltage of DAC arrays remains the value for the previous pixel data (which is used as an initial guess); it is not necessary to reset the reference voltage value to V_{CM}, and there is no need for an additional initializing process as the classic LSB-first algorithm. The initializing process of DAC arrays would increase costs in delay time and power. Therefore, the proposed ADC is superior to the ones proposed in previous works. The ADC operates as follows: In the quantization process, S_{DIR} connects V_{CM}. V_{DAC} is then compared against the sampled V_{IN}. If the comparator output is 1, meaning V_{DAC} is greater than V_{IN}, the initial guess was too high and S_{DIR} translates from V_{CM} to *GND*, which denotes the need to decrease the guess. Inversely, if the comparator output is 0, then S_{DIR} connects V_{DD}. In this case, the initial guess is either too low or exactly correct. When the initial guess is exactly correct, the conversion ends after only two bitcycles. Otherwise, the algorithm moves the digital output from LSB to MSB until it converges to the final output code. The example conversion in Fig. 15 has an initial guess $D_{PREV} = 718$ and a final $D_{OUT} = 731$. As each bitcycle involves a DAC transition, an analog comparison, and logic transitions, it is observed that LSB-first SA saves energy in all components of the ADC by performing fewer bitcycles than the conventional ones when the signal activity decreases.

IV. Experiment Results and Analysis

Fig. 16 shows the die microphotograph of the proposed ADC. It has been fabricated using 65-nm standard CMOS technology, and the active area occupies 0.19 mm^2. To reduce the mismatch between the unit capacitors, the capacitor array

$$V_{out}\ (X) = V_{CM} + \frac{C_C\ (\sum_{n=1}^{i} 2^{n-1} CS_{l,n} + CS_{DIR} + \sum_{n=1}^{k} 2^{n-1} CS_{m,n}) + C_L \sum_{n=1}^{k} 2^{n-1} CS_{m,n}}{C_C\ (C_L + C_M) + C_L C_M} \bullet \frac{1}{2} VDD \tag{7}$$

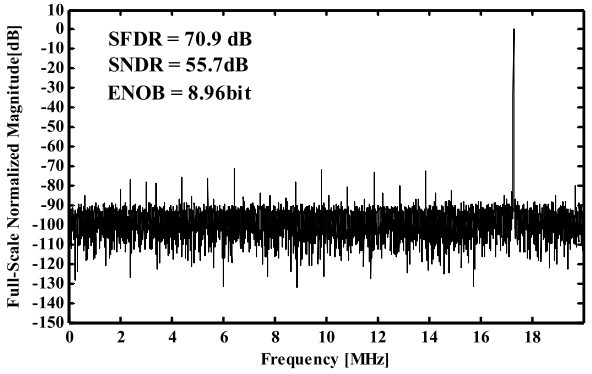

Fig. 17. Measured ADC output spectra at $f_S = 40$ MS/s.

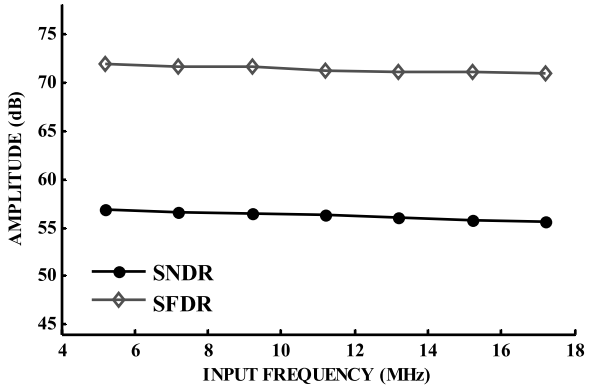

Fig. 18. Measured dynamic performance versus the input frequency.

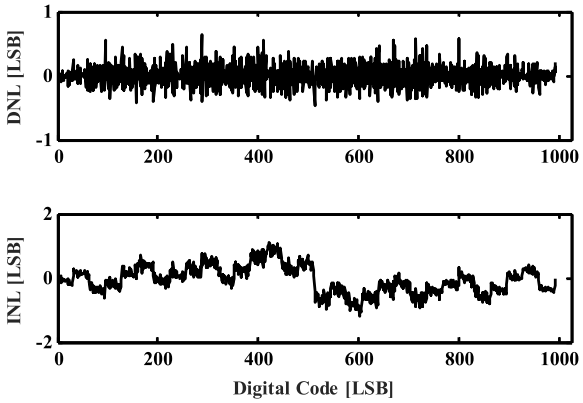

Fig. 19. Measured DNL and INL.

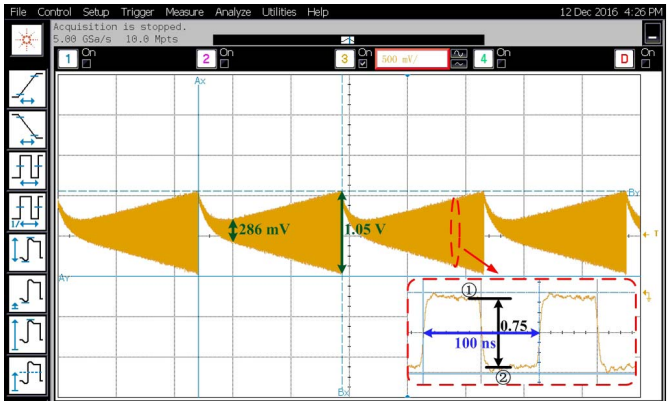

Fig. 20. Input signal V_{IN} for measurement of CDS functionality.

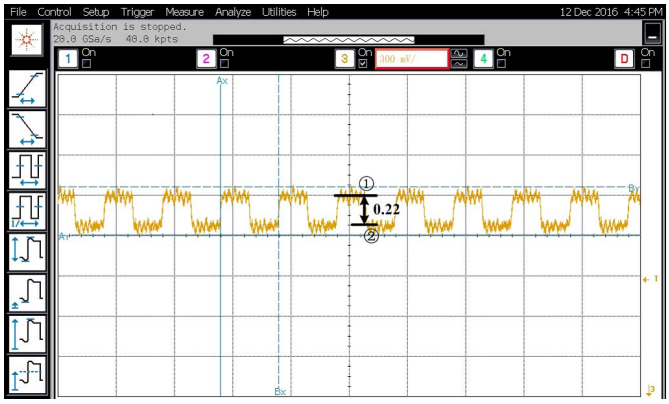

Fig. 21. Input signal V_{IN} for measurement of PGA functionality.

follows the partial common-centroid configuration and is surrounded by dummy capacitors. To conveniently and fairly evaluate and compare the dynamic performance and linearity with other works, the proposed ADC is measured using single-tone testing (the CDS and PGA functionality are not used). Thus, the sine input signal is sampled onto the capacitance. The voltages V_{PP} and V_{NN} of the comparator are equal to V_{SIG} and $V_{REF} - V_{SIG}$. Fig. 17 shows the fast fourier transform of the ADC with a near-Nyquist frequency input signal at 17.2876 MHz. The SNDR and SFDR are 55.7 dB and 70.9 dB, respectively. Fig. 18 summarizes the measured SNDR and SFDR with respect to the input frequency. The SNDR and SFDR are greater than 55.7 dB and 70.9 dB respectively, when the input signal varies from 5 MHz to 17.2876 MHz at a sampling rate of 40 MS/s. The linearity of the ADC in terms of DNL and INL is measured and illustrated in Fig. 19. The DNL/INL measurement result for one test chip uses 1.2-V supply voltage, and the DNL is bounded at $+0.68/-0.45$ LSB and the INL at $+1.07/-1.15$ LSB.

The CDS and PGA are achieved in the proposed ADC using passive technology, which are measured and verified in Fig. 20 and Fig. 21, respectively. As shown in Fig. 20, a stair-step signal is used as V_{IN}, which is generated by a 14-bit DAC. The magnitude of ΔV_{IN} ranges in 0–1.05 V and varies linearly in 0.286–1.05 V with each step of $1.2/2^{10}$ V. The V_{IN} with small voltage magnitude increases non-linearly due to evaluation board for measurement, as shown in Fig. 20. Therefore, we choose a linear part of V_{IN} from 0.286 V to 1.05 V for verifying the functionality of CDS. A micro-photo in Fig. 20 shows the correlated double sampling locations ① and ②. The measurement results indicate that output digital codes (corresponding to ΔV_{IN} from 0.286 to 1.05 V) increase linearly with the same tendency of the input signal V_{IN}. Thus the CDS functionality is effective in obtaining the difference of voltages in two adjacent sampling phases.

The proposed ADC provides programmable gains of -6 dB, 0 dB, and 6 dB according to the setting of *BIT [0:2]*. The input signal V_{IN} with a constant value of $\Delta V_{IN} = 0.22$ V is applied

TABLE III

PERFORMANCE SUMMARY AND COMPARISON

Reference	[4]	[5]	[15]	[16]	[17]	[19]	[20]	[29]	[30]	[31]	[32]	[33]	[34]	This work
ADC Architecture	SAR	SAR	SS	SS/SAR	SAR/SS	Cyclic	ΔΣ	SAR	SAR/SS	SAR	SAR	SAR	SAR	SAR
Technology(nm)	180	350	130	180	180	180	180	180	90	180	180	180	130	65
Supply voltage (V)	1.8	3.3	2.8	3.3	3.3	1.8	1.8	3.3	2.8	3.3	3.3	3.3	2.8	1.2
CDS Functionality	W/O	W/O	W/O	W/O	W/O	W/O	W/O	W/O	W/O	W/O	W/O	W	W/O	W/
PGA Functionality	W/O	W/O	W/O	W/O	W/O	W/O	W/O	W/O	W/O	W/O	W/O	W/O	W/O	W/
Sampling rate(MS/s)	2.5	1.79	N/A	0.083	0.3	0.5	20	0.56	N/A	0.4	0.77	0.03	0.06	40
Resolution (bit)	10	10	12	11	9	12	10	8	12	12	10	9	14	10
DNL (LSB)	0.94	-0.6/+0.73	-0.49/+1.34	-1.45/+1.65	-1.0/+9.9	+/-0.5	-0.2/+0.22	-1.5/+1.7	-0.45/+0.84	0.83	0.55	1.2	-0.9/+0.99	+0.68/-0.45
INL(LSB)	1.39	-2.43/+2.60	-2.5/+2.4	N/A	-9.8/+4.7	-2/+3.2	-0.89/+0.71	-1.3/+0.6	-1.5/+0.74	1.62	0.77	4	-3.9/+12	+1.07/-1.15
Active area (mm^2)	0.035	N/A	0.0066	N/A	0.009	0.0075	0.00186	0.0024	0.002	0.012	0.01	0.0036	0.11	0.19
FoM(fJ/conv.-step)	15	844	178	206	37.8	241.6	151	1410	36.9	92.8	74	140	--	21.7

TABLE II

PERFORMANCE SUMMARY

Active die area	0.19 mm^2
Sampling rate	40 MHz
Resolution mode	10-bit
CDS	with
PGA	-6 dB, 0 dB, 6 dB
SFDR(dB)@Nyquist	70.9 dB
SNDR(dB)@Nyquist	55.7 dB
Power Consumption	415.2 μW
DNL (LSB)	+0.68/-0.45
INL (LSB)	+1.07/-1.15
FoM((fJ/conv.-step))	21.7

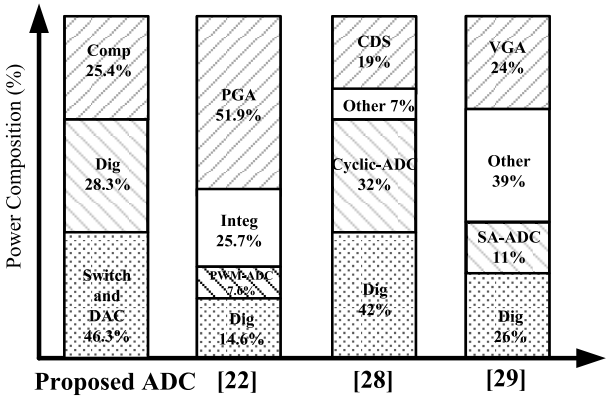

Fig. 22. Power breakdown summary of proposed SAR ADC and others.

into the ADC, as shown in Fig. 21. In the measurement, the obtained digital output code is 155 at the gain of 0 dB, while the digital output code is 355 (corresponding to $\Delta V_{IN} = 0.433$ V) at the gain of 6 dB, which is less than the ideal value of 361(corresponding to $\Delta V_{IN} = 0.44$ V). It is observed that the proposed ADC has a gain of less than 6 dB partially due to the effect of parasitic capacitance in the sampling capacitance.

A power constitution summary of the proposed ADC and other works for image sensor is shown in Fig. 22. It is apparent that the CDS and PGA occupy a major component of the total power consumption [22] [28] [29]. In contrast

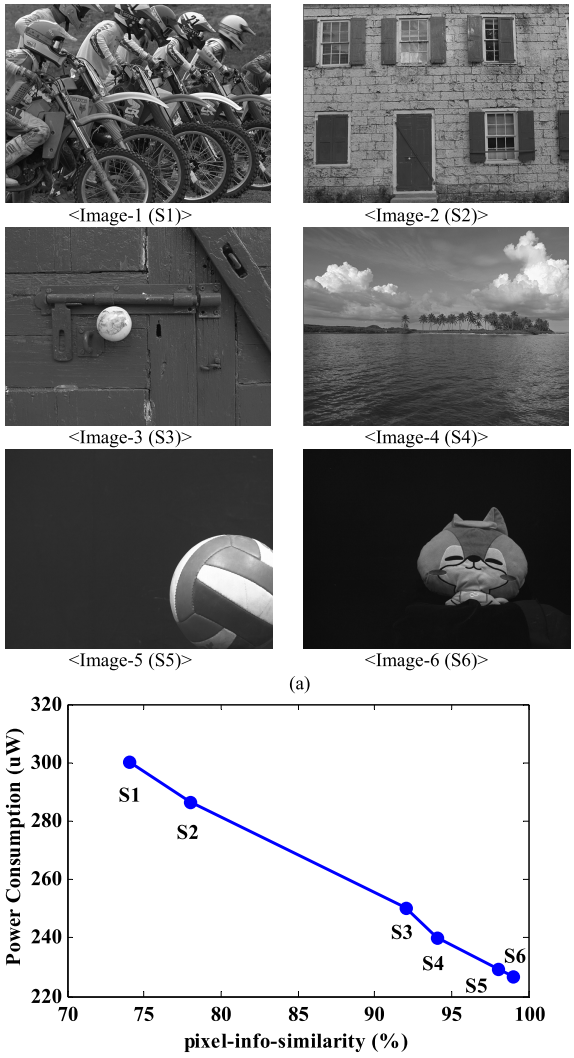

Fig. 23. Measurement of image inputs. (a) Six different image inputs for measurement. (b) Power consumption versus pixel-info-similarity @ S1-S6.

to previous works, the proposed ADC provides the CDS and PGA functionality with low power consumption by the comparator, logic, and DAC. The measured performance of

the fabricated chip is summarized in Table II. Here, the figure-of-merit (FOM) adopts the definition from [33] [35].

To demonstrate the power consumption of proposed ADC using delta-readout concept and LSB-first algorithm, six image inputs with different pixel-info-similarity are used to measure the power consumption of the proposed ADC, as shown in Fig. 23 (a). The pixel-info-similarity is defined as the percentages of delta values between neighboring pixels are smaller than 15 LSB. The pixel-info-similarity is inversed to the image signal activity. Targeting these image input signals with pixel-info-similarity from 74% to 99%, the power consumed by the ADC is from 300 μW to 226 μW, as shown in Fig. 23 (b). It is indicated that lower power consumed by ADC for image input with higher pixel-info-similarity through using the LSB-first algorithm.

Table III summarizes the basic performance of the proposed chip and previously reported ADCs utilized for the image sensor application. Among the ADCs in Table III, the work described here is the only one that integrated the CDS and PGA functionality effectively without additional power consumption. And the proposed ADC exhibits a good performance in terms of linearity, area, and energy-efficiency.

V. Conclusion

A 10-bit, 40-MS/s power-saving SAR with passive SDS, CDS and PGA technology for image sensor applications is presented in this paper. The CDS achieved by the sampling capacitance removes the noise component of the data signal, and the SDS prevents the occurrence of even error during the quantization process. The PGA controlled by digital word provides gains of -6 dB, 0 dB, and 6 dB. Based on the characteristic of the adjacent pixels, the LSB-first algorithm is adopted in the ADC to effectively reduce the power consumption by varying the LSB array according to the initial guess. The measurement results show that the proposed ADC has a better SNDR (55.7 dB) and SFDR (70.9 dB) at a 40 MS/s sampling rate, resulting in a FOM of 21.7 fJ/conversion-step. And the lower power is consumed for image input with higher pixel-info-similarity through using the LSB-first algorithm.

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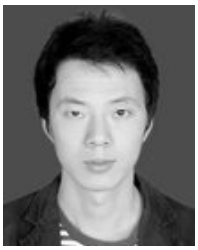

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