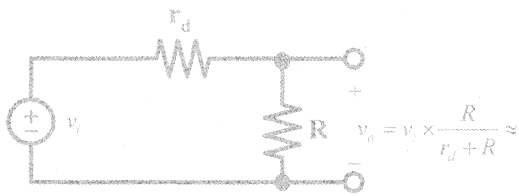
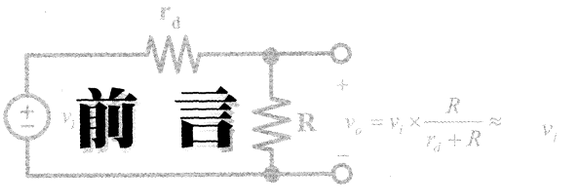


陳龍英的電子學

第一冊 VOLUME 1



前言

從研究所畢業後，我就留在母校任教，至今已經超過三十年。「電子學」是我從剛開始教書到現在仍然在講授的學科，它好像是陪了我走過三十多年青春歲月的老朋友，已經融入我的生命，成為不可或缺的一部分。

交大是以電子研究起家，「電子學」是電子系必修的基礎科目，被安排在第二學年全年及第三學年上學期的課程，每週四節課。該科目所包含的內容相當繁雜，初學者常不易理出頭緒及抓住重點，因此很需要藉助一位有多年教學經驗的老師，利用在課堂上「深入淺出」的講解，幫助學生釐清許多基本概念。

為了幫助學生學習，交大教務處看重本人在這方面的豐富教學經驗，因而從民國90年9月起，就有計畫地拍攝我在課堂上講授「電子學」的實況，製作成影片，上傳到學校網站，提供學生上網學習及複習。雖然反應熱烈，但是因為當時教室的聲光設備並不考究，又缺乏講義輔助，使教學效果打了折扣，是美中不足的地方。

93年初，我們換了一間設備較好、較大的教室（可容納150人）上課，並且重新錄影製作。此外，我請班上幾位優秀同學整理隨堂筆記，以便搭配實況影片，讓學生可以邊看邊學，獲得更好的學習效果。在使用這套教學光碟時，我也建議同學們採用Sedra/Smith所著的Microelectronic Circuits為自修教科書。

在電子學(一)，我們將「Diodes」排在第一章，特別是將基本半導體觀念及pn接面放在最前面。在二極體之後，接著是「Bipolar Junction Transistors」(第二章)，然後才是「MOS Field-Effect Transistors」(第三章)。這樣的排序，我認為在學習效果上會比較好;此外，顧及學生在上電子學(一)時，還沒有建立交流電路的觀念，因此有關電晶體的高頻模式及頻率響應，都先予以略去，留待電子學(二)用第六章專章來說明。學生在上過二極體及電晶體等基本電子元件之後，邁入第四章「Operational Amplifiers」。

電子學(二)包括第五章「Differential Amplifiers 」、第六章「Frequency Response」、第七章「Feedback」以及第八章「Output Stages and Power Amplifiers」。在差動

放大器中有關頻率響應的部份，則擺在第六章加以說明。我們考量將輸出級與功率放大器安排在電子學(二)中說明，乃是我覺得這樣安排，對於後面在電子學(三)中討論運算放大器電路(741 op-amp電路)會有較大幫助。「Single-Stage Integrated-Circuit Amplifiers」則打散放至相關各章節中。

電子學(三)則包括第九章「Operational-Amplifiers and Data-Converter Circuits」、第十章「Signal Generators and Waveform-Shaping Circuits」以及第十一章「Digital Logic Circuits 」等內容。其中數位邏輯電路會談到CMOS邏輯電路及射極耦合邏輯（ECL），其他較少被用到的雙極性（Bipolar）數位電路，則予以簡略。

總之，我希望培養學生電子學的基本觀念、理論，使學生能融會貫通，奠定基礎科學的能力，而後才能與實務接軌，結合其他領域向上提昇。

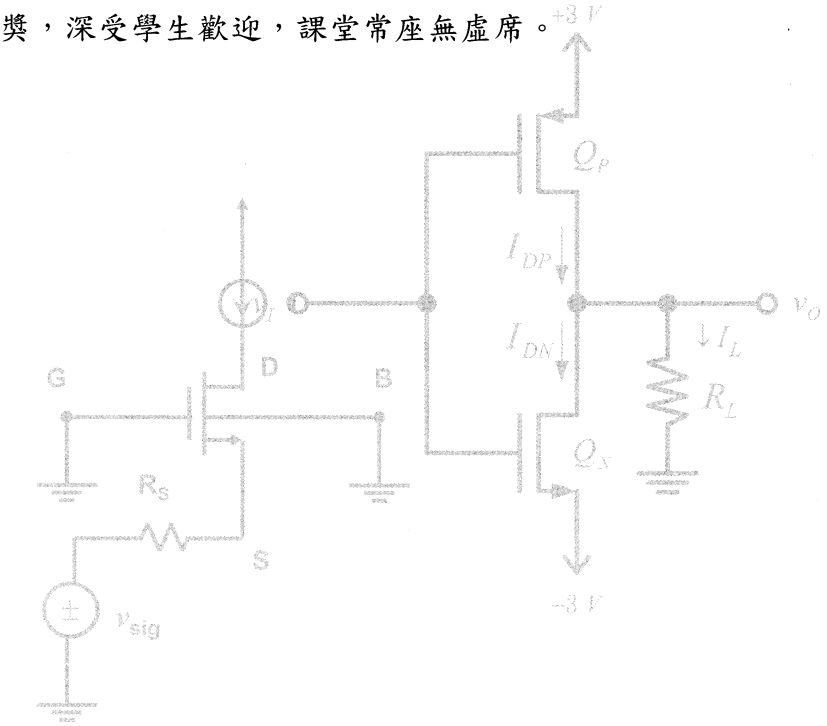
本出版品的完成，我要感謝下列同學在整理隨堂筆記及打字、繪圖所花費的心力，包括：交大電子所博士生鄧至剛(第一章)、王文傑（第二章)、陳旻珓(第三、四章）、交大電子研究所碩士班吳承佑（電子學二、三）、交大電子工程系學生陳怡潔、程士恆（整理電子學二、三之筆記）、李佳叡、許書餘、趙芳翌（校正再版講義暨光碟）；此外，交大教務處數位內容製作中心及交大出版社的同仁也出力甚多，在此一併感謝。

國立交通大學電子工程系教授

陳龍英

作者簡介

陳龍英先生，西元1941年生，國立台灣大學電機工程系畢業，國立交通大學電子研究所碩士及博士，現為交大電子工程系教授。他曾在國際知名的美國貝爾實驗室擔任研究員，並先後擔任過交大電子工程系系主任、交大教務長、副校長、教育部高等教育司司長及國立空中大學校長。其學術專長包括積體電路與系統、電子電路設計及電子構裝等領域，為人謙虛，熱愛教學，在交大教授「電子學」科目超過三十年，多次榮獲教育部及交大傑出教學獎，深受學生歡迎，課堂常座無虛席。



電子學(一)

電子學(二)

電子學(三)

學目錄 Contents

Chapter 1: Diodes

1.1 Physical Operation of Diodes

1.1.1 Basic Semiconductor Concepts

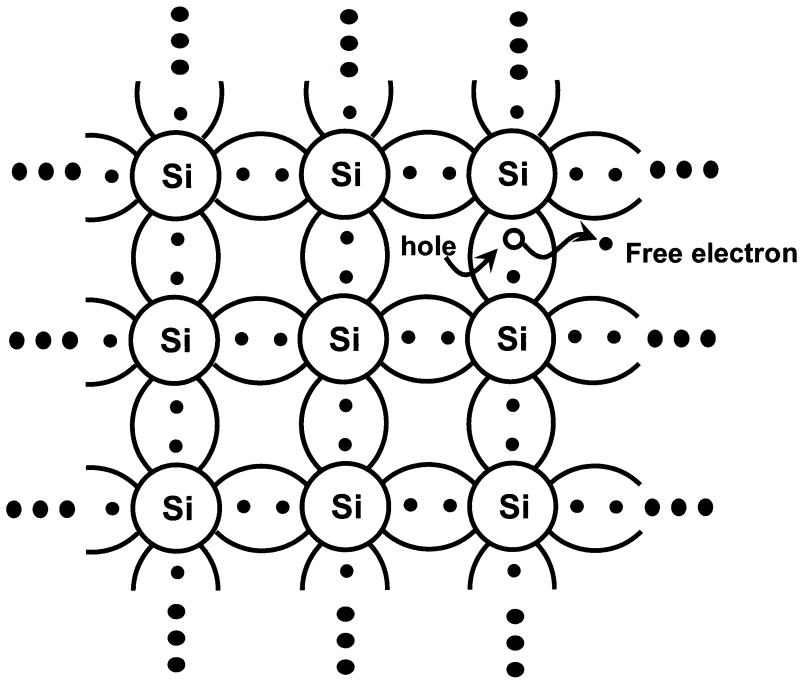
Basic Semiconductor Concepts：

Conductor ←→ Insulator

Conductivity of semiconductor is between conductor and insulator

半導體多為四價，例如: Si

Si 之間以共價鍵相結合，成正四面體狀



半導體可分為：

(1) Intrinsic semiconductor (本質半導體)

(2) Extrinsic semiconductor (異質半導體，帶雜質)

在半導體當中，載子(carrier)有兩種，分別為：

(1)自由電子(electron)、電洞(hole)

(2)自由電子與電洞兩者電量相同，電性相反

Intrinsic semiconductor：

$n = p = n_i(\mathrm{T})$ （其中：n 為電子濃度，p 為電洞濃度，單位 個/cm^3）

$n_i^2(\mathrm{T}) = BT^3 \times \exp(-E_G/kT)$ ，$T\uparrow$➔ $n=p=n_i\uparrow$

其中 B: material dependent parameter; k: Boltzman constant

E_G: 1.12eV energy gap; B for silicon = 5.4×10^{31}

Thermal equilibrium：

Generation rate　　G: 單位時間、體積當中，產生的電子電洞對

Recombination rate　R: 單位時間、體積當中，消失的電子電洞對

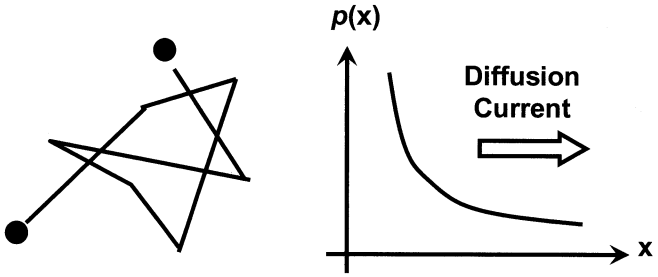
在某溫度下，$G = R$ (熱平衡) and　$T\uparrow$➔ $G(T)\uparrow$➔ $n\uparrow$ $p\uparrow$➔ $G > R$

$G(\mathrm{T}) = f_1(\mathrm{T})$ and $R(\mathrm{T}) = n \times p \times f_2(\mathrm{T})$

由 Hall effect 實驗的結論:可將電洞視為一個帶正基本電荷的粒子

Two mechanisms carriers move：

Diffusion: 濃度的梯度產生擴散



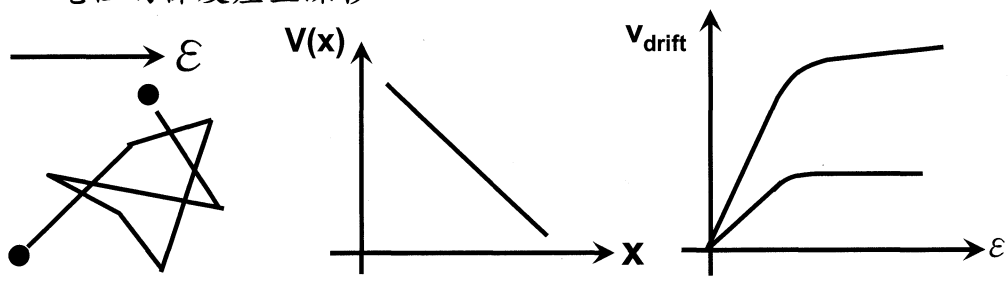
$J = I/A$ (A/cm^2)

$J_p = -qD_p \dfrac{dp}{dx}$　　D_p: Diffusion constant of holes (cm^2/s)

$J_n = qD_n \dfrac{dn}{dx}$　　D_n: Diffusion constant of electrons (cm^2/s)

$$J = J_p + J_n = -qD_p \frac{dp}{dx} + qD_n \frac{dn}{dx}$$

Drift:電位的梯度產生漂移



$$\mathcal{E} = -\frac{dV}{dx} \quad (\textit{Electric field} = \textit{negative Potential gradients})$$

$J_p = qp\mu_p\mathcal{E}$　　其中：μ_p 為 mobility of holes ($cm^2/V \bullet s$)

$J_n = qn\mu_n\mathcal{E}$　　其中：μ_n 為 mobility of holes ($cm^2/V \bullet s$)

$J_{drift} = J_p + J_n = q(p\mu_p + n\mu_n)\mathcal{E}$　　其中：$v_{drift} = \mu\mathcal{E}$

$$J_{diff} = J_{p-diff} + J_{n-diff} = -qD_p\frac{dp}{dx} + qD_n\frac{dn}{dx}$$

室溫下　$D_n = 34\ cm^2/s$　and　$\mu_n = 1350\ cm^2/V{\cdot}s$

　　$D_p = 12\ cm^2/s$　and　$\mu_p = 480\ cm^2/V{\cdot}s$

Review

For intrinsic semiconductor：

$n = p = n_i(T)$　(其中：n 為電子濃度，p 為電洞濃度，單位 個/cm^3)

$$J_{diff} = J_{p-diff} + J_{n-diff} = -qD_p\frac{dp}{dx} + qD_n\frac{dn}{dx}$$

$$I = \frac{V}{R} = \frac{VA}{\rho l}\quad 其中：R = \rho\cdot\frac{l}{A};\ J = \frac{\mathcal{E}}{\rho} = \sigma\mathcal{E};\ \rho = \frac{1}{\sigma} = \frac{1}{qn_i(\mu_n + \mu_p)}$$

for Si：$\rho = 2.3\times10^5\ \Omega{\cdot}cm$

Thermal voltage：

Einstein relationship：$\frac{D_n}{\mu_n} = \frac{D_p}{\mu_p} = V_T \equiv \frac{kT}{q} = 25.9\text{mV}$ at T = 300K

25mV at T = 292K

Doped (Extrinsic) Semiconductor：

Extrinsic Si：Small carefully controlled impurity content

三價 B ➔ p-type 五價 P, As ➔ n-type

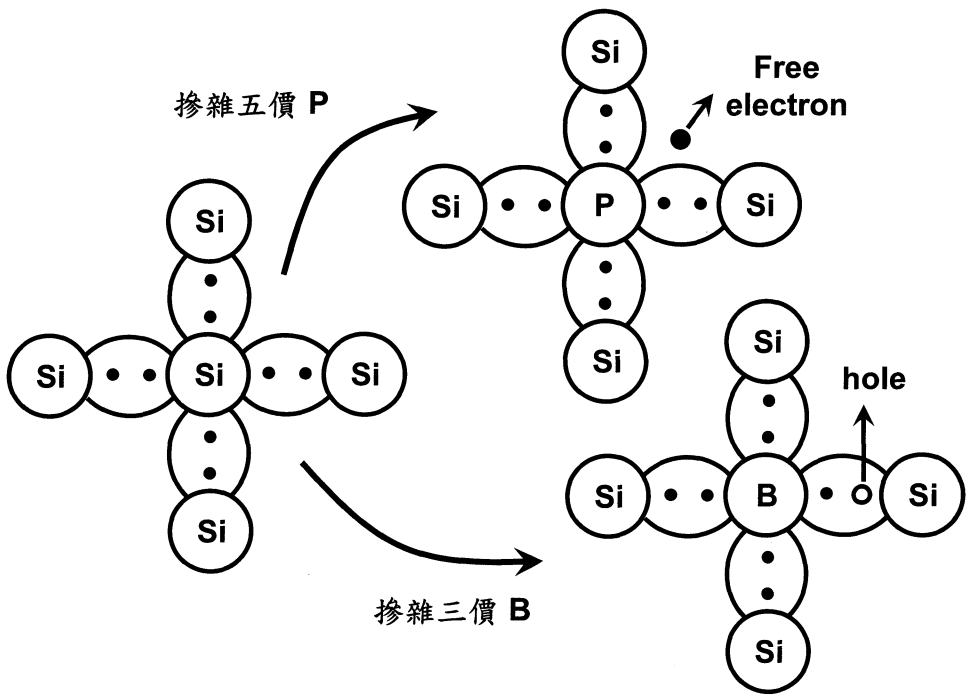
Si $\approx 10^{22}$ /cm^3; Impurity $\approx 10^{16}$ /cm^3

沒有雜質下 $n_i \approx 10^{10}$ /cm^3

加入五價的雜質之後，電子濃度大大提升 $n \approx 10^{16}$ /cm^3 >> n_i >> p

五價雜質為施子雜質(Donor impurity)

N_D 表示施子雜質的濃度



綜合以上，我們可得知在 n-type 的半導體裡面

$n >> n_i >> p$ and $n_{no} >> p_{no}$

n_{no}：In thermal equilibrium the concentration of free electron in the n-type silicon

(在此為 majority carrier 是電子)

p_{no}：In thermal equilibrium the concentration of hole in the n-type silicon

(在此為 minority carrier 是電洞)

Thermal equilibrium：

$G(T) = R(T)$ $f_1(T) = n \times p \times f_2(T)$ ➔ $n \times p = f_1(T)/f_2(T) = f_3(T)$

Intrinsic：

$n = p = n_i$ ➔ $f_3(T) = n_i^2$

In n-type (加上五價雜質)：

$n \cong N_D$

$n \times p = n_i^2(T)$ (mass-active law)

$$p_{n0} = \frac{n_i^2}{n_{n0}} = \frac{n_i^2}{N_D}$$

when T↑ ➔ n = N_D and $n_i(T)$ ↑ ➔ p↑

In p-type (加上三價雜質)

for Si：Si ≈ $10^{22}/cm^3$ Impurity ≈ $10^{16}/cm^3$

$N_A \approx 10^{16}/cm^3$ (N_A 為 acceptor 受子)

$p_{p0} \cong N_A$

$n \times p = n_i^2(T)$ (mass-active law)

$$n_{n0} = \frac{n_i^2}{p_{p0}} = \frac{n_i^2}{N_A}$$

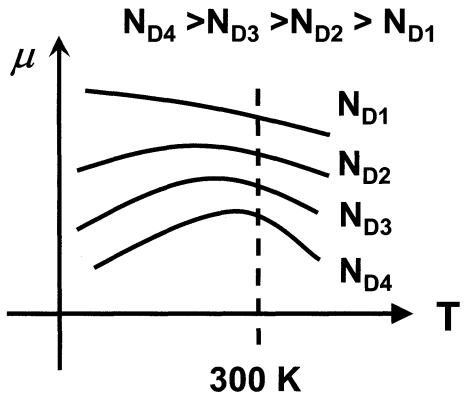
Conductivity：

$\sigma = q \times p \times \mu_p + q \times n \times \mu_n = q \times (p \times \mu_p + n \times \mu_n)$ (通式)

For intrinsic：$\sigma = q \times n_i \times (\mu_p + \mu_n)$

For n-type：$\sigma = q \times N_D \times \mu_n$

For p-type：$\sigma = q \times N_A \times \mu_p$

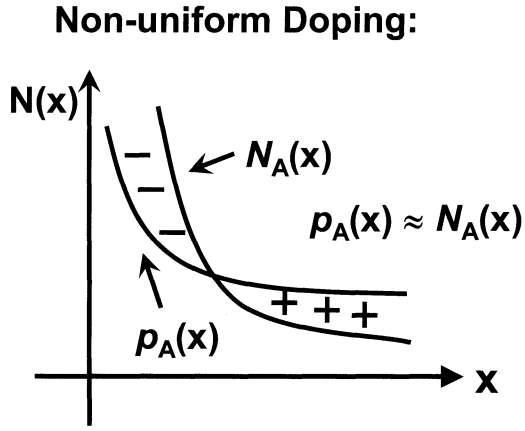


低溫以 impurity scattering 為主
高溫以 lattice scattering 為主

重要觀念：

不論 n-type 或是 p-type 當中，都是電中性的。或許有人認為 n-type 或 p-type 當中分別有很多的電子或電洞，因此不是電中性的；但是別忘了裡面還有帶著相反電性的雜質所構成的離子，因此整體而言還是電中性的。

Graded (Non-uniform) Semiconductor：



Build-in Potential：V_{12}

Diffusion current： $J_{p-diff} = -q \times D_p \times \frac{dp}{dx}$

Build-in field： $\mathcal{E} = -\frac{dV}{dx}$

其中 $p(x) \approx N_A(x)$ ➔ $\frac{dp}{dx} \approx \frac{dN_A}{dx}$

在熱平衡下： $J_p = J_{p-drift} + J_{p-diff} = 0$

因此 $J_p = q \times p \times \mu_p \times \mathcal{E} + (-q \times D_p \times \frac{dp}{dx}) = 0$

➔ $\mathcal{E} = \frac{D_p}{\mu_p} \times \frac{dp}{p} \times \frac{1}{dx} = V_T \times \frac{dp}{p \cdot dx}$ ➔ $\mathcal{E}dx = V_T \frac{dp}{p}$

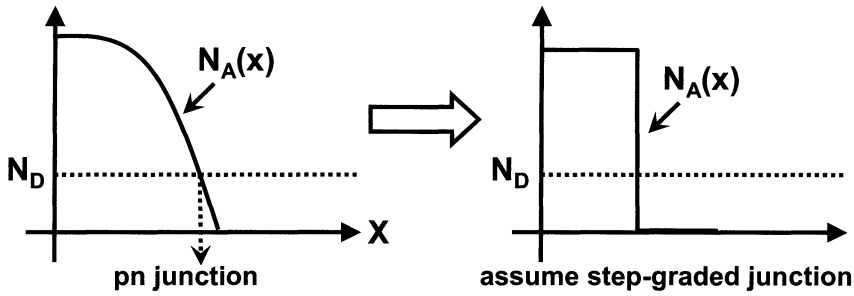
又 $\mathcal{E} = -\frac{dV}{dx}$ ➔ $dV = -\mathcal{E}dx = \frac{-V_T dp}{p}$

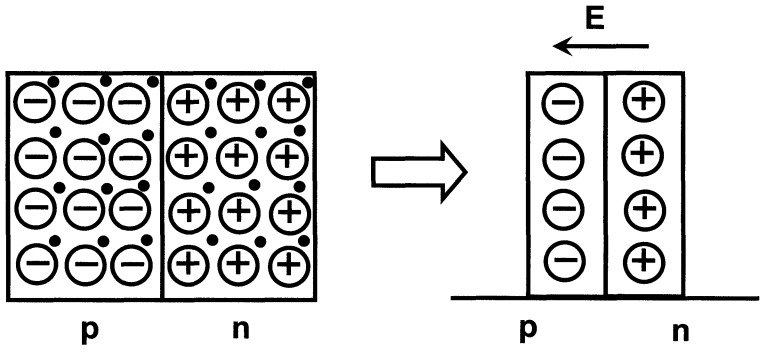
因此 $V_{21} = V_2 - V_1 = \int_{V_1}^{V_2} dV = -V_T \times \int_{p_1}^{p_2} \frac{dp}{p} = -V_T \times \ln\frac{p_2}{p_1} = V_T \times \ln\frac{p_1}{p_2}$

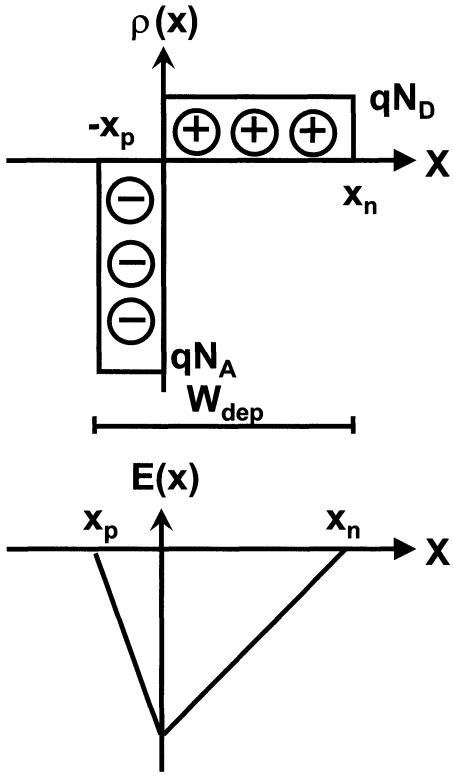
$$V_{21} = V_2 - V_1 = V_T \times \ln\frac{p_1}{p_2}$$

由 $n_1 \times p_1 = n_2 \times p_2$ ➔ $V_{21} = V_T \times \ln\frac{p_1}{p_2} = V_T \times \ln\frac{n_2}{n_1}$

1.1.2 Open-Circuit pn Junction







ρ(x): charge density

$$\frac{N_A}{N_D} = \frac{x_n}{x_P}$$

$$W_{dep} = x_n + x_p = \sqrt{\frac{2\varepsilon_{Si}}{q}\left(\frac{1}{N_A} + \frac{1}{N_D}\right)V_O}$$

$W_{dep} \approx 0.1 \sim 1\mu m$

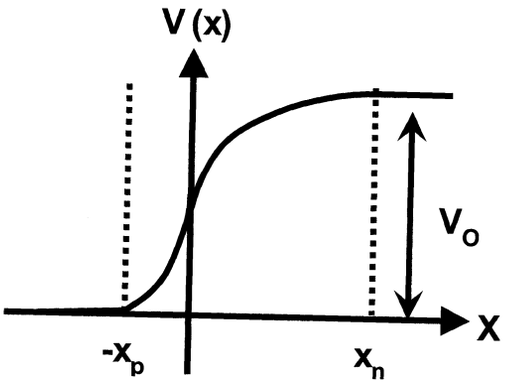
For $N_A >> N_D$,

$$W_{dep} \approx x_n = \sqrt{\frac{2\varepsilon_{Si}V_O}{qN_D}} \propto \frac{1}{\sqrt{N_D}}$$

$$E = \frac{1}{\varepsilon_{Si}}\int \rho(x)dx$$

$\varepsilon_{Si} = 11.7\varepsilon_0 = 1.04 \times 10^{-12}$ F/cm

ε_{Si} : permittivity of Si



$$dV(x) = -E\,dx$$

$$V_O = V_T \ln\frac{p_1}{p_2} = V_T \ln\frac{N_A N_D}{n_i^2}$$

V_O大約為 0.6~0.8V

V_O: junction built-in voltage

P.S.：(1) 會由雜質濃度低的側邊，來決定 W_{dep} 的寬度

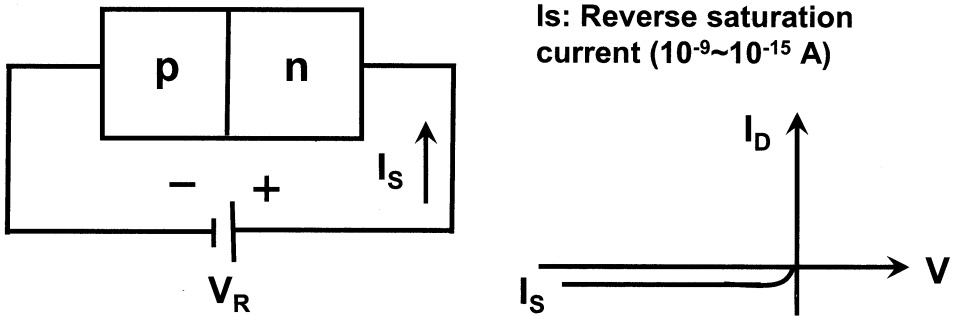
(2) 若為 linear graded junction 則方程式將會不一樣

1.1.3 Reverse-Bias pn Junction

將 open-circuit pn junction 兩端加上電壓(如下圖)

推論: p 型區電洞濃度高，與電源負極相吸；n 型區電子濃度高。與電源正極相吸。因此會造成大電流。

實際上，約只有 10^{-15} A (極小)因為 p 型區電子濃度低，n 型區電洞濃度低，來不及補充。



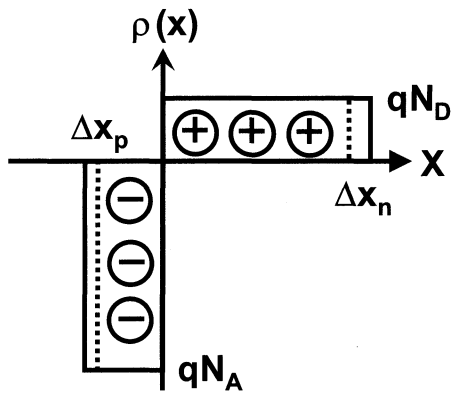
I_S 與逆向偏壓大小無關(已飽和)。但有少數載子導電，其值≠0，但極小。

當 N_A、N_D 濃度越高，多數載子數量增加，然而少數載子數量卻減少

➔ I_S 下降。(I_S 由少數載子數量控制)

當溫度越高 (T↑) ➔ n_i↑ ➔ 少數載子數量變多 ➔ I_S 上升。

Junction area 面積上升 ➔ I_S 上升($I_S \propto A$) ，又稱 scale current。

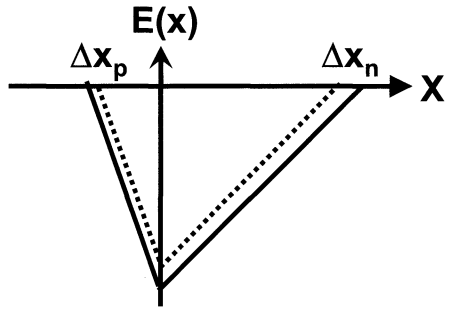


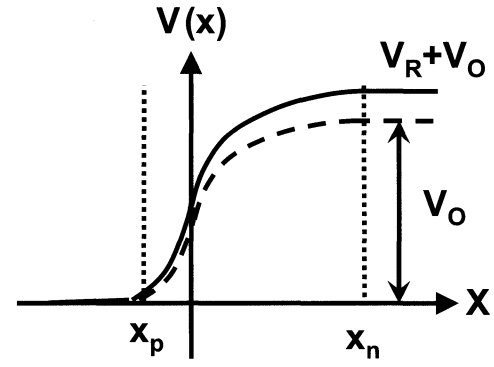
在Reverse-Biased Circuit中

W_{dep} 要修正為:

$$W_{dep} = \sqrt{\frac{2\varepsilon_{Si}}{q}\left(\frac{1}{N_A}+\frac{1}{N_D}\right)(V_O + V_R)}$$

其中V_R 為外加逆向偏壓





Depletion (Junction) Capacitance：

電容量: 改變一單位電位差所需電量。

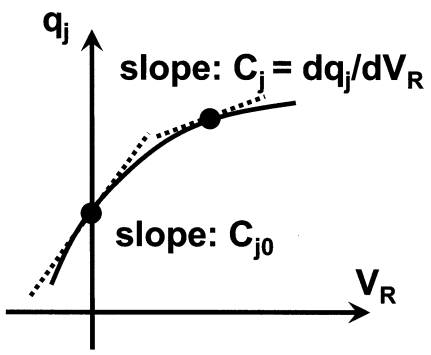
$C = \dfrac{dq_J}{dV_R}$ (junction capacitance of pn junction) 接面會有電容存在

$q_j = qN_D x_n A$

$x_n = W_{dep} \times \dfrac{N_A}{N_D + N_A}$

$$C_j \equiv \frac{dq_J}{dV_R} = \frac{A\sqrt{\dfrac{\varepsilon_{Si}\cdot q}{2}\left(\dfrac{N_A \cdot N_D}{N_A + N_D}\right)\dfrac{1}{V_O}}}{\sqrt{1+\dfrac{V_R}{V_0}}} = \frac{C_{j0}}{\sqrt{1+\dfrac{V_R}{V_0}}}$$

其中 $C_{jo} = A\sqrt{\dfrac{\varepsilon_{Si}\cdot q}{2}\left(\dfrac{N_A \cdot N_D}{N_A + N_D}\right)\dfrac{1}{V_O}}$ for zero applied voltage C_j



廣義C_j：$$C_j = \frac{C_{j0}}{(1+V_R/V_O)^m}$$

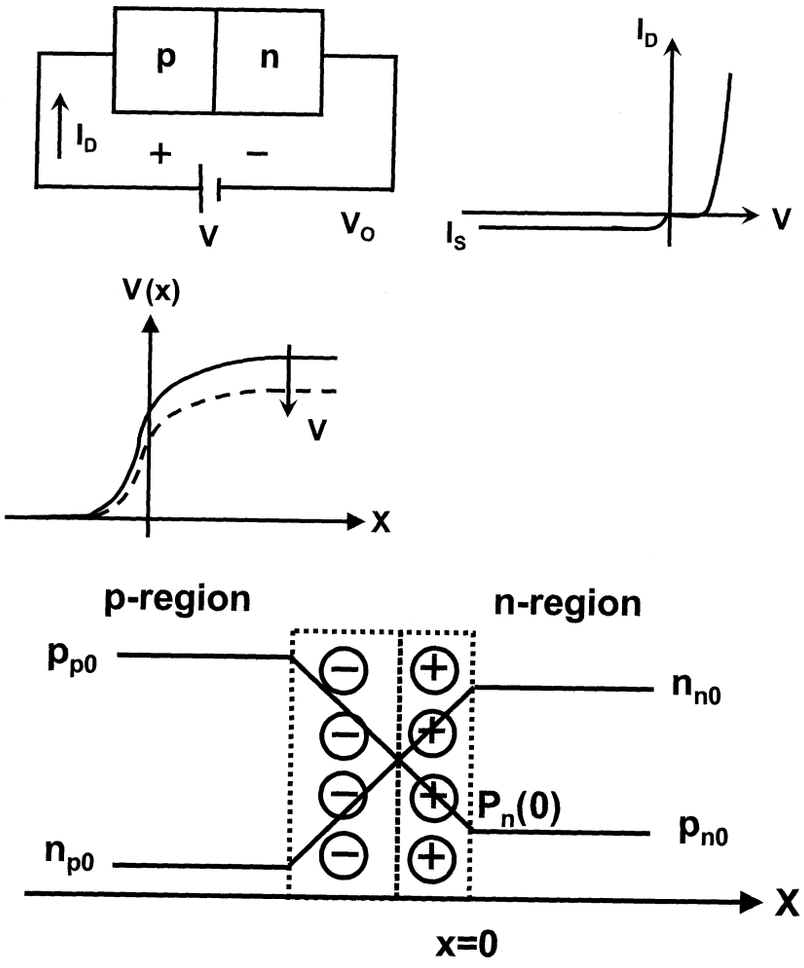
For step-graded junction: m=1/2

For linear junction: m=1/3

亦可以用W_{dep}表示C_j：

$$C_j = A \times \frac{\varepsilon_{Si}}{W_{dep}}$$ 此式可適用於任何之雜質分佈

1.1.4 Forward-Bias pn Junction



在外加偏壓的條件下，已破壞熱平衡： $p \cdot n > n_i^2$

$p_n(0) = p_{n0} \times e^{V/V_T}$ (law of the junction)

$p_n'(x) \equiv p_n(x) - p_{n0} \Rightarrow p_n'(0) = p_n(0) - p_{n0}$

$p_n'(x) = p_n'(0) \times e^{-x/L_p}$ (其中 L_p 為 diffusion length of holes)

$p_n'(x) = p_{n0}(e^{V/V_T} - 1) \times e^{-x/L_p} \Rightarrow p_n'(0) = p_{n0}(e^{V/V_T} - 1)$

$$\frac{dp_n'(x)}{dx} = -\frac{p_n'(0)}{L_p} \times e^{-x/L_p}$$

$J_{p-diff} = f(x)$ (電洞的擴散電流可以是 x 的函數)

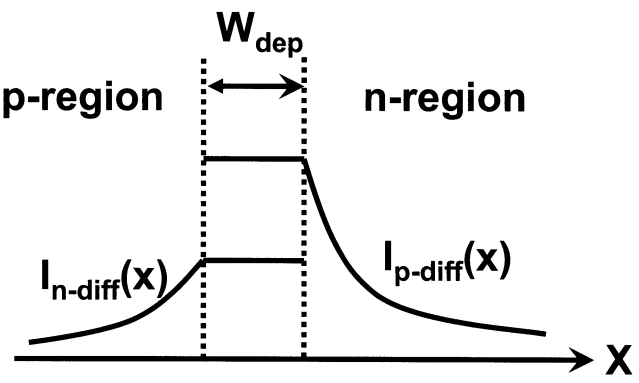
$$J_{p-diff} = -qD_p \frac{dp}{dx} = -qD_p \frac{dp_n'(x)}{dx} = q\frac{D_p}{L_p} p_{n0}(e^{V/V_T} - 1) \times e^{-x/L_p}$$

(1) 以上公式同時適用於順偏及逆偏。逆偏時候，$V < 0$ 時，由於是指數的負次方，可得知 $p_n(0)$ 會變的很小

(2) 總電流應該不為一隨位置變化的變數，總電流應為一常數。否則在此 pn-junction 上會出現電荷累積的情形。因此想要定出一點，找出確切的電流，即得知整個 pn-junction 的電流，因此我們選擇以 Depletion region 來討論電流。

以 Depletion region 找電流的好處：

若 $W_{dep} << L_P$，$W_{dep} << L_n$，如此可以略去 recombination 所造成的影響，且 n、p 小，因此可略去 I_{drift}



N 型區的電洞電流=電洞的總電流 $I_{p-total} \cong I_{p-diff} = A \times q \times D_p \times \frac{p_n'(0)}{L_p} e^{-x/L_p}$

P 型區的電子電流 $I_n = A \times q \times D_n \times \frac{n_p'(0)}{L_n} e^{-x/L_n}$

$$I = A \times q \times D_p \times \frac{p_n'(0)}{L_p} + A \times q \times D_n \times \frac{n_p'(0)}{L_n}$$

$$= A \times q \left[D_p \times \frac{p_{n0}}{L_p} + D_n \times \frac{n_{p0}}{L_n} \right] \times (e^{v/V_T} - 1)$$

$$= A \times q \times (D_p \times \frac{1}{L_p \times N_D} + D_n \times \frac{1}{L_n \times N_A}) \times n_i^2 (e^{v/V_T} - 1) = I_S (e^{v/V_T} - 1)$$

由上式可看出，I 主要是由濃度低的一方雜質決定(N_A 和 N_D 在分母)

以上式子化簡用到了以下公式：

$$p_n(0) = p_{n0} \times e^{v/V_T} \quad \text{and} \quad p_n'(0) = p_n(0) - p_{n0} = p_{n0} \times (e^{v/V_T} - 1)$$

$$p_{n0} = \frac{n_i^2}{N_D} \quad \text{and} \quad n_{p0} = \frac{n_i^2}{N_A} \text{。}$$

逆向飽和電流：$I_S \approx 10^{-15}$ A

(by brand new technology，we may get $I_S \approx 10^{-18}$~10^{-19} A)

Discrete diode ↔ intergraded diode：

$$I = I_S \times (e^{V/\eta V_T} - 1) \quad \text{其中} \ \eta = 1\text{~}2$$

$\eta = 1$　(Using standard IC fabrication process)

$\eta = 2$　(Discrete component)

Diffusion Capacitance：

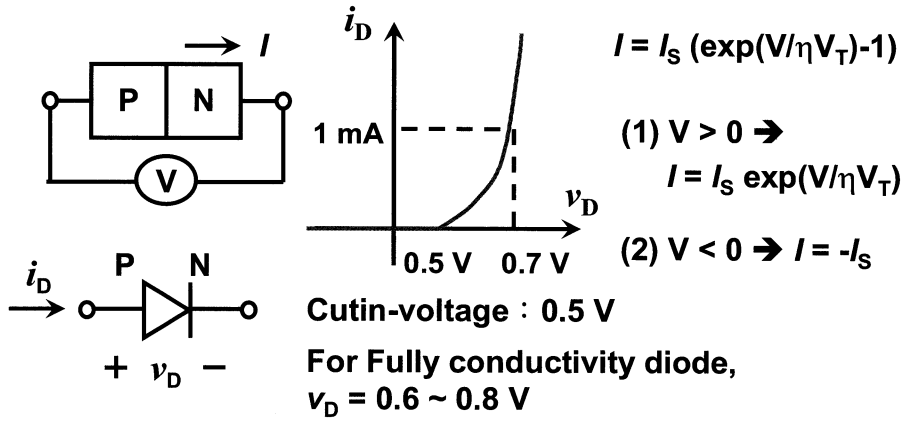
$$C_d \equiv \frac{dQ}{dV} = \frac{\tau_T}{V_T} I \propto I \qquad (\tau_T : \text{Transit time})$$

Q 為接面兩側的 excess minority-carrier stored charge

Forward bias：$C = C_j + C_d \cong C_d$

Reverse bias：$C = C_j + C_d \cong C_j$

1.2 Terminal Characteristics of Junction Diodes



$$i_D = I_s(e^{v_D/\eta V_T} - 1)$$

Forward bias: $i_D \approx I_s e^{v_D/\eta V_T}$ and $v_D = \eta V_T \ln(i_D/I_s)$

Reverse bias: $i_D = -I_S$

If $V_1 = \eta V_T \ln(I_1/I_s)$ and $V_2 = \eta V_T \ln(I_2/I_s)$

➔ $V_2 - V_1 = \eta V_T \ln I_2/I_1$ ➔ $V_2 = V_1 + \eta V_T \ln I_2/I_1$

P. S.：由上式可知，若要得知一 Diode 在某電壓（或電流）時，相對應的電流（或電壓），則必須先得知：I_S，η，或者是 V_1，I_1。得知其中一項才能求得以上需求。

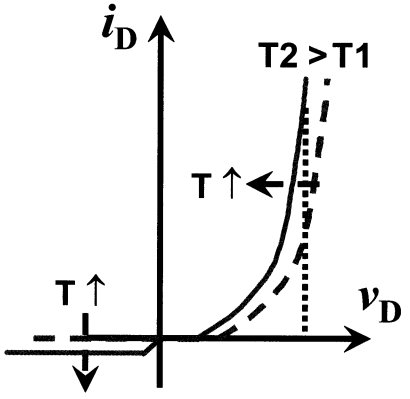
Temperature dependence：

由實驗歸納出：

I_S 在每上升 1°C，即增加 7 %。

因 $(1.07)^{10} \sim 2$，$I_S(T) = I_S(T1) \times 2^{(T-T1)/10}$

同一個 i_D 下，v_D 會呈現 -2mV/°C。

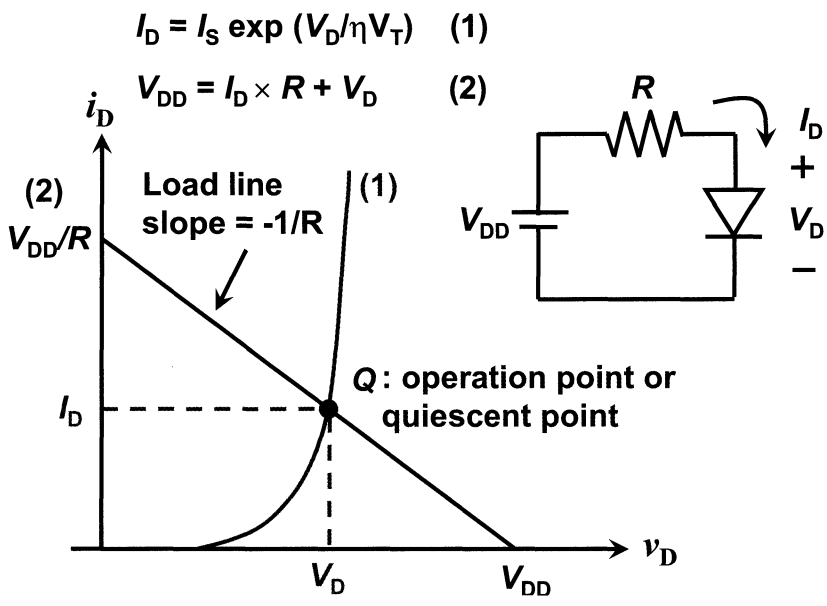


1.3 Modeling the Diode Forward Characteristics

1.3.1 Exponential Model：most accurate and most difficult

(a) Graphical analysis (圖解法)：

Q：Quiescent point or Operation point (I_D, V_D)



(b) Iterative analysis (疊代分析)：

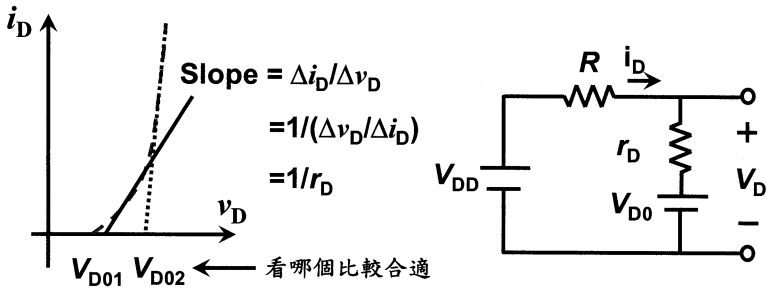
先設 $V_D = 0.7$ V ➔ $I_D = (V_{DD} - V_D)/R = (V_{DD} - 0.7)/R$

以上式求得 I_D，再帶回式子 $V_2 = V_1 + \eta \times V_T \times \ln(I_2/I_1)$

其中假設已知(I_1, V_1)，EX：$V_1 = 0.7$ V at $I_1 = 1$mA

可求出 V_2，再帶回 $I_D = (V_{DD} - V_2)/R$ 得 I_D

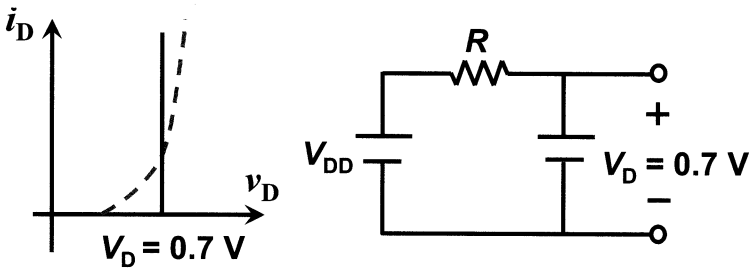
1.3.2 Piecewise-Linear Model：(Battery-plus-resistance model)



當 $v_D < V_{D0}$ ➔ $i_D = 0$

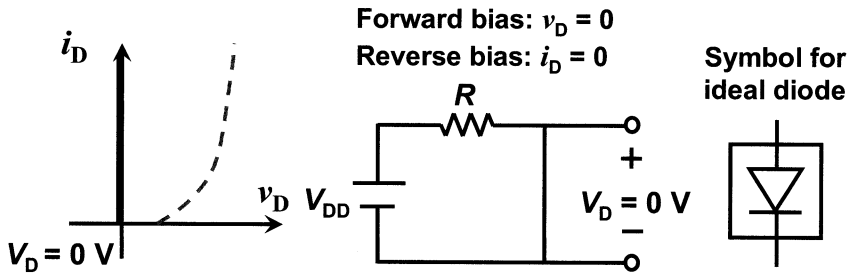
當 $v_D > V_{D0}$ ➔ $i_D = \dfrac{v_{DD} - V_{D0}}{r_D + R}$ and $v_D = V_{D0} + i_D \times r_D$

1.3.3 Constant-Voltage-Drop Model：



當 $r_D << R$ ➔ 則視 $r_D = 0$，$V_D = 0.7$ V ➔ $i_D = (V_{DD} - 0.7\text{ V})/R$

1.3.4 Ideal-Diode Model：



(1)-(4) model：DC-model、Large-signal model

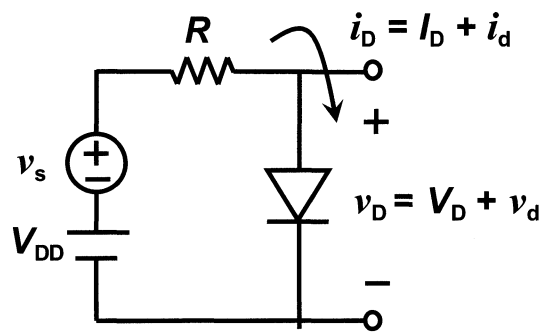
(2)-(4) model：Piecewise linear model

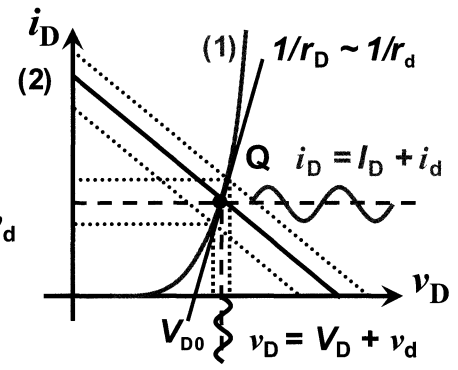
1.3.5 Small-Signal Model：

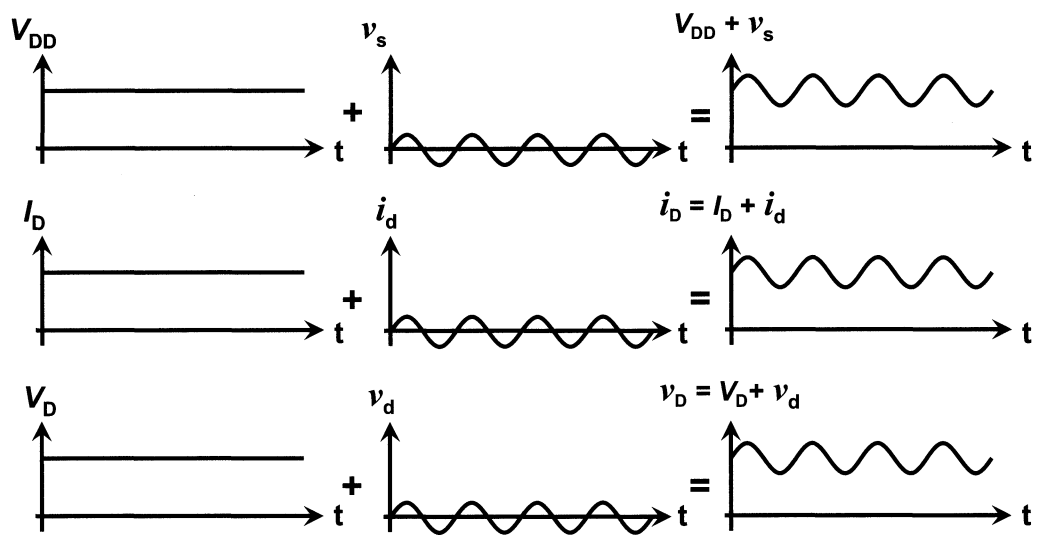
$i_D = I_S \exp(v_D/\eta V_T)$ (1)

$V_{DD} + v_s = i_D \times R + v_D$ (2)

Small signal ➔ linear approx.







$$I_D + i_d = I_s e^{(V_D+v_d)/\eta V_T} = I_s \times e^{V_D/\eta V_T} \times e^{v_d/\eta V_T}$$

$$\approx I_D\left(1+\frac{v_d}{\eta V_T}\right) = I_D + \frac{I_D}{\eta V_T} \times v_d$$

$e^x = (1 + x + \ldots)$

$x << 1, \quad e^x \cong 1 + x$

若 $v_d/\eta V_T << 1$ ($v_d << \eta V_T = 50\text{mV}$ or $v_d < 10\text{mV}$)

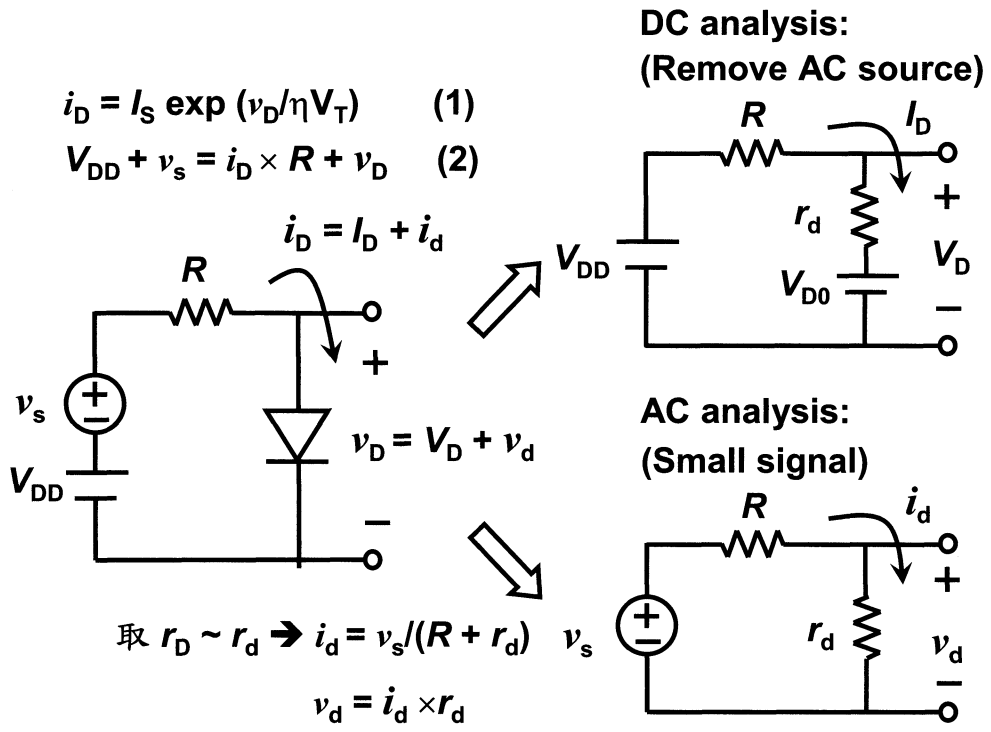
➔ small signal approx.)

$$\therefore \; i_d = \frac{I_D}{\eta V_T} \times v_d \;\rightarrow\; \frac{\Delta v_D}{\Delta i_D} = \frac{v_d}{i_d} = \frac{\eta V_T}{I_D} \equiv r_d$$

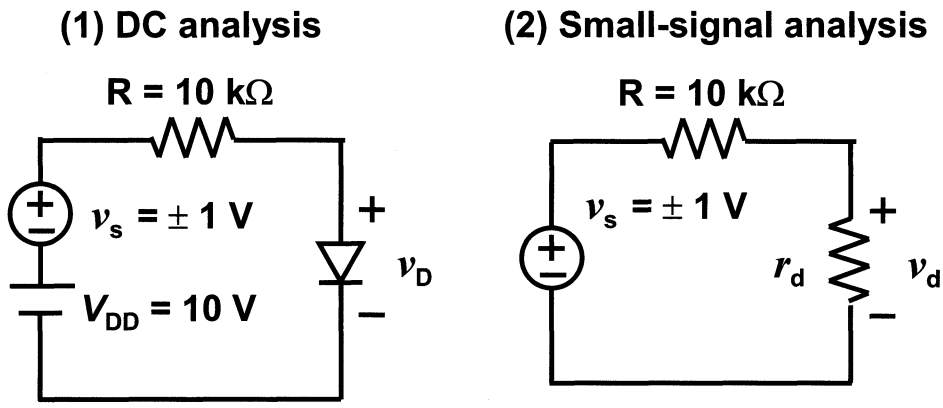
r_D：diode DC equivalent resistance

r_d：diode increment resistance or diode dynamic resistance

直接微分：$r_d \equiv \dfrac{\Delta v_D}{\Delta i_D} = \dfrac{v_d}{i_d} = \dfrac{1}{\left(\dfrac{\Delta i_D}{\Delta v_D}\right)} = \left[\dfrac{I_S e^{V_D/\eta V_T}}{\eta V_T}\right]^{-1} = \dfrac{\eta V_T}{I_D}$



EXAMPLE1：If η = 2; I_1 = 2 mA, V_1 = 0.7 V



(1) DC analysis：

$\Rightarrow$設 $V_D = 0.7$ V $\quad \begin{cases} I_D = \left(10 - 0.7\right) \Big/ 10k\Omega = 0.93mA (\cong 1mA) \\ V_D \cong 0.7V \end{cases}$

(2) Small-signal analysis：

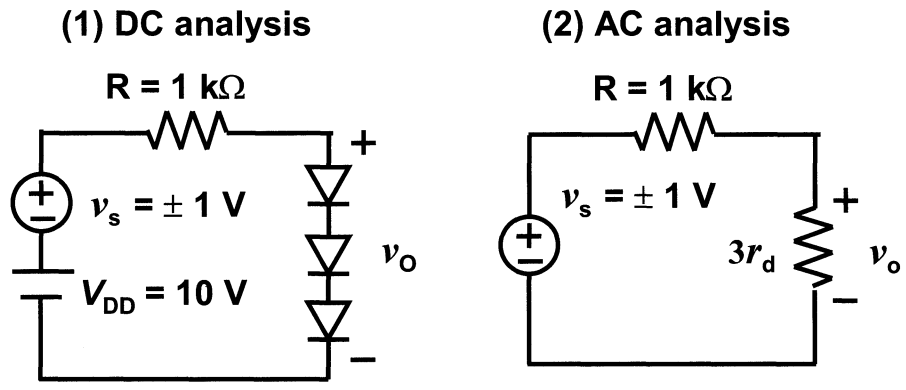
$$r_d = \frac{\eta V_T}{I_D} = \frac{2 \times 25mV}{0.93mA} = \frac{50}{0.93} = 53.8\Omega$$

$$v_{d(peak)} = \pm 1V \times \frac{0.0538}{10 + 0.0538} = 5.35mV (< 10mV)$$

$$v_D = V_D + v_d = 0.7V \pm 5.35mV \cong 0.7V$$

$$\frac{1V}{10V} = 10\% \quad \text{and} \quad \frac{5.35mV}{0.7V} = 0.8\%$$

EXAMPLE2：If $\eta = 2$; $I_1 = 2$ mA, $V_1 = 0.7$ V



(1) DC analysis：

設 $V_D = 0.7$ V ➔ $V_O = 3 \times 0.7$ V $= 2.1$ V, $I_D = (10 - 2.1)/1k = 7.9$ mA

設 $V_D = 0.7 + \eta V_T \times \ln(7.9mA/1mA) = 0.8$ V

➔ $I_D = \frac{10 - 0.8 \times 3}{1} = 7.6mA$

(2) AC analysis：

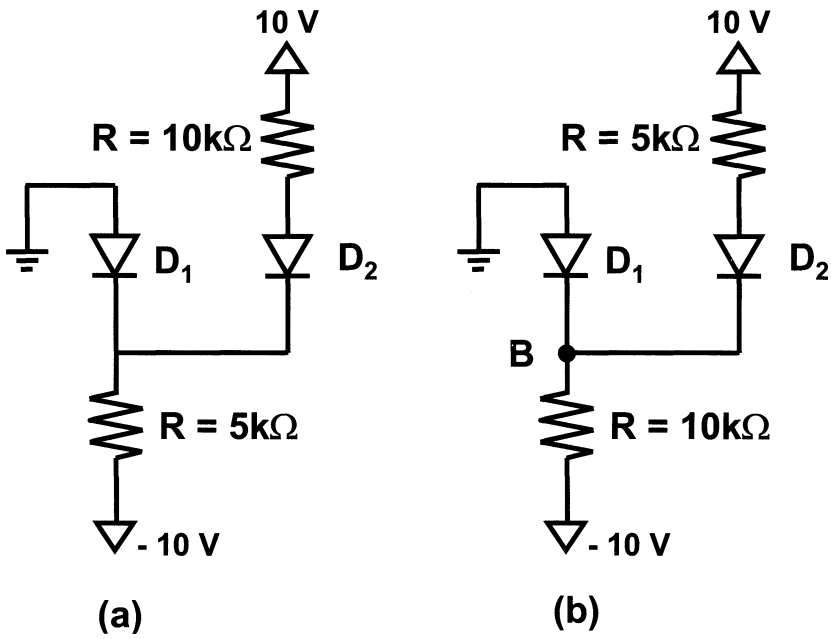
$$3r_d = 3 \times \frac{\eta \times V_T}{I_D} = \frac{3 \times 2 \times 25}{7.6} = 3 \times 6.6\Omega = 19.8\Omega$$

$$v_0 = \pm 1V \times \frac{3 \times 6.6}{1k + 3 \times 6.6} = \pm 19.4mV$$

$v_o / V_o = 0.8$ %

$$\frac{\Delta v_0}{\Delta v} = \frac{\pm 19.4mA}{\pm 1V} = 19.4\,mV/V$$ Line regulation

EXAMPLE3：設 D1，D2 為理想二極體。



(a) 設 D1：ON (conduct) and D2：ON (conduct)

$$I_{D2}=\frac{10-0}{10k}=1\ mA;\quad I_{D1}+I_{D2}=\frac{0-(-10)}{5k}=2\ mA$$

$$I_{D1}=2-1=1\ mA$$

(b) 假如電阻對換，同樣設 D1：ON (conduct) and D2：ON (conduct)

$$I_{D2}=\frac{10-0}{5k}=2\ mA;\quad I_{D1}+I_{D2}=\frac{0-(-10)}{10k}=1\ mA$$

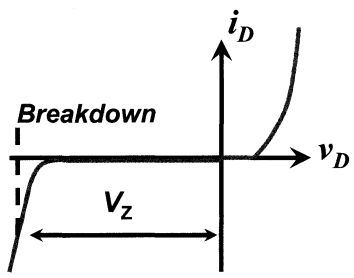
$$I_{D1}=1-2=-1\ mA \quad \text{(不合理)}$$

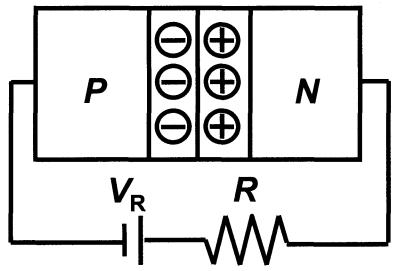
重新假設，設 D1：OFF and D2：ON (conduct)

$$I_{D2}=\frac{10-(-10)}{5k+10k}=1.33\ mA$$

$V_B = -10 + 1.33 \times 10 = 3.3\ V > 0\ V$，D1 確實為 OFF。

1.4 Zener Diodes



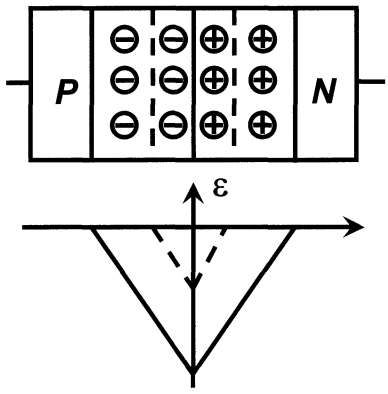


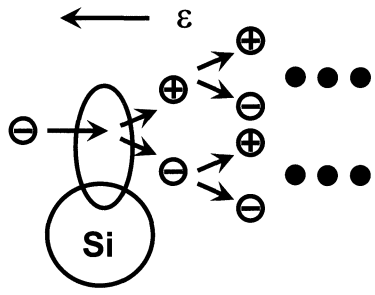
Two breakdown mechanisms：

(1) Avalanche multiplication：

V_R↑ ➔ ε↑ ➔ q ε↑ ➔ a↑ ➔ ν↑ ➔ $mv^2/2$↑

N_D 和 N_A↓ ➔ ε↓ ➔ Vz↑

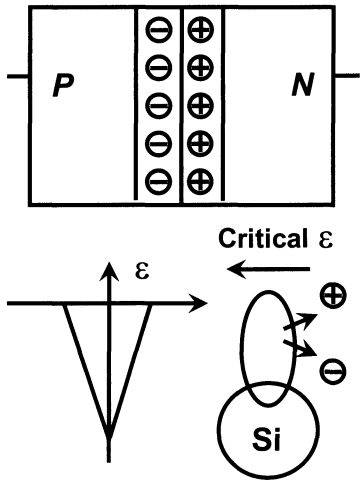


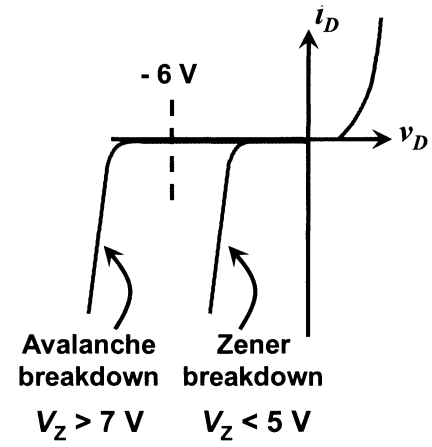


(2) Zener breakdown：

V_R↑ ➔ ε↑ (2×10^7 V/cm) ➔ q ε↑

N_D 和 N_A↑ ➔ Vz↓





Temperature effect：

(1) For avalanche multiplication：

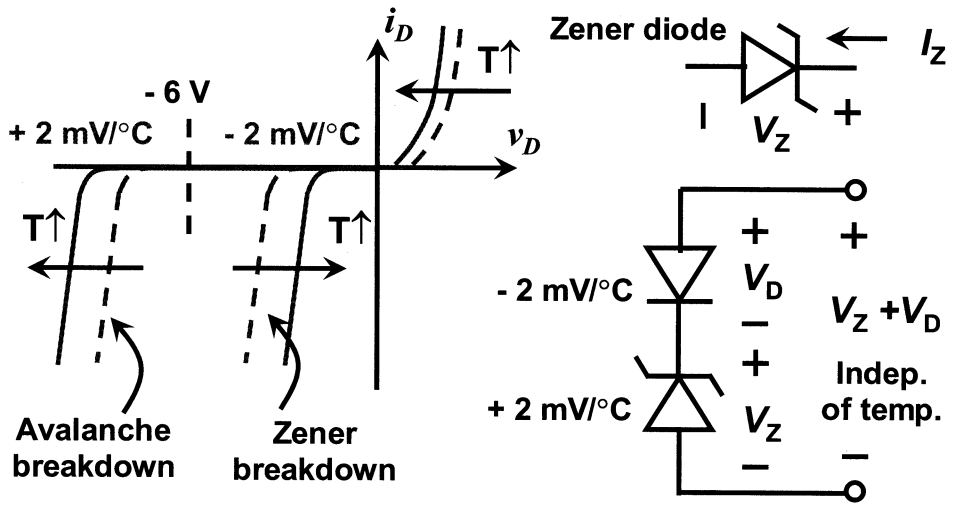
T↑ ➔ free path ↓ ➔載子越難被加速➔V_Z↑ (positive temp. coeff.)

(2) For Zener breakdown：

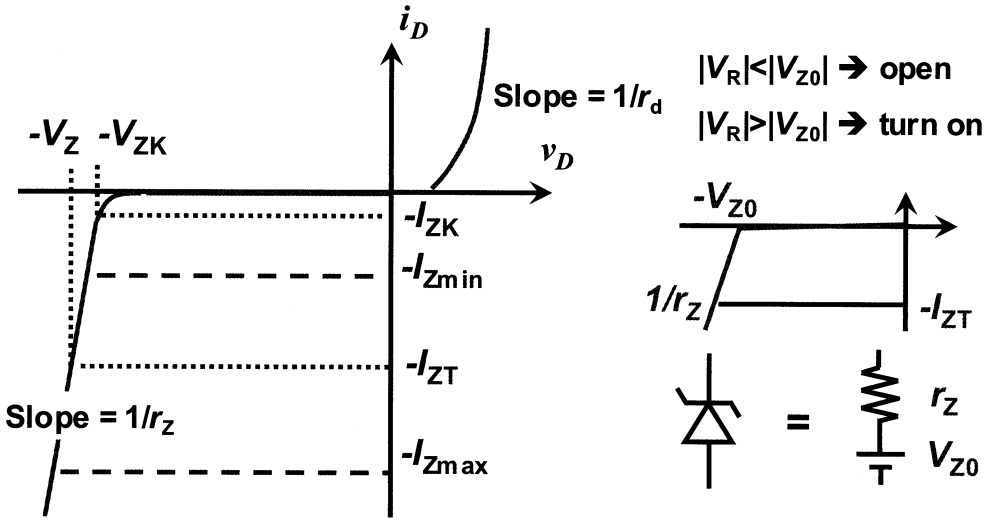
T↑ ➔ Si 鍵能越弱➔越容易拉出價電子

➔V_Z↓ (negative temp. coeff.)

Temp. Coeff.約為 ±2mV/°C or $\pm \frac{\frac{\Delta V_Z}{V_Z}(\%)}{^oC} = \pm 0.1\ \%/°C$



Zener diode 參數標示：



EX：Given: V_Z = 6.8 V at I_{ZT} = 5 mA ; r_Z = 20 Ω ; Vs = 10 V; R = 0.5 kΩ

6.8 V = V_{Z0} + 5 mA × 20 Ω ; V_{Z0} = 6.8 - 5×10^{-3} × 20 = 6.7 V

DC analysis： $I_Z = \dfrac{10 - V_{Z_0}}{R + r_Z} = \dfrac{10 - 6.7}{0.5 + 0.02} = 6.35mA$

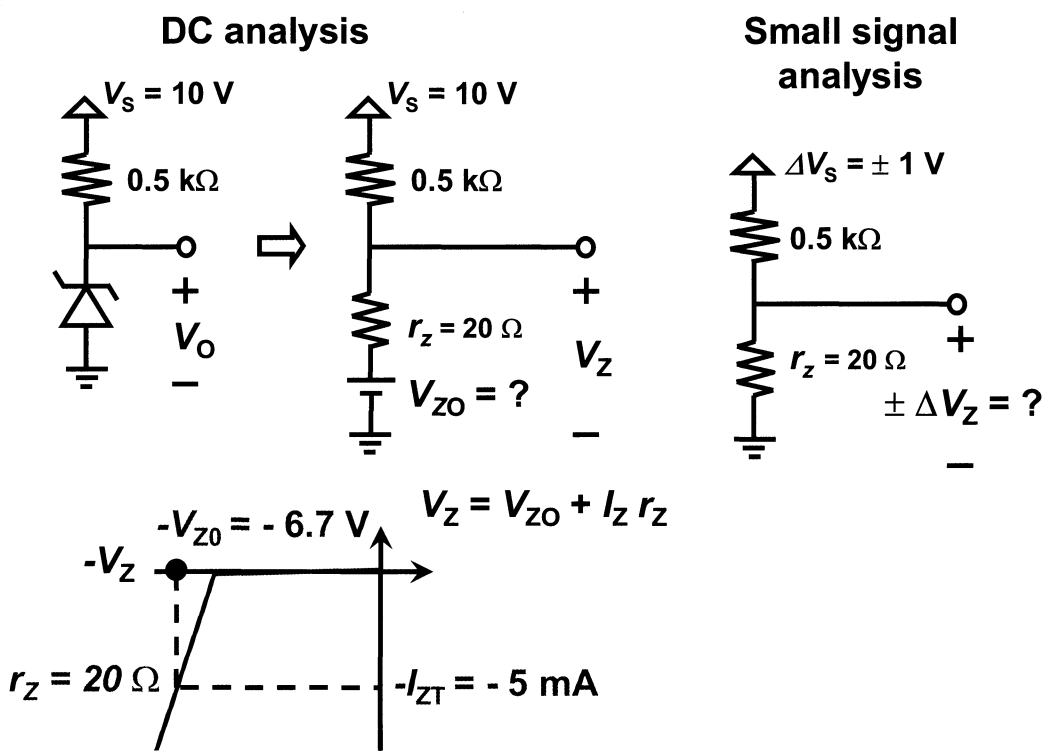
$V_Z = 6.7 + I_Z \times 0.02 = 6.7 + 6.35 \times 0.02 = 6.872$ V

Small signal analysis： $\pm\Delta V_Z == \pm 1V \times \dfrac{r_Z}{R + r_Z} = \pm 1V \times \dfrac{20}{500 + 20} = \pm 38.5mV$

$\pm \Delta V_Z / V_Z = \pm 38.5mV / 6.827V = \pm 0.6\%$

Line regulation： $\Delta V_Z / \Delta V_S = 38.5mV / 1V = 38.5 mV / V$

P.S.：現在已經用 IC 電路做的 voltage regulator 來取代單純由 Zener diode 做的 voltage regulator。

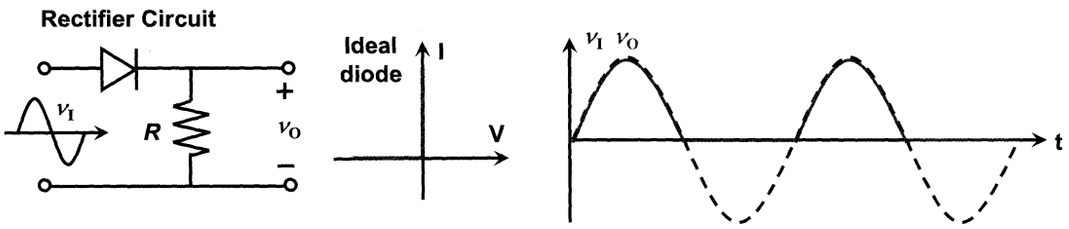


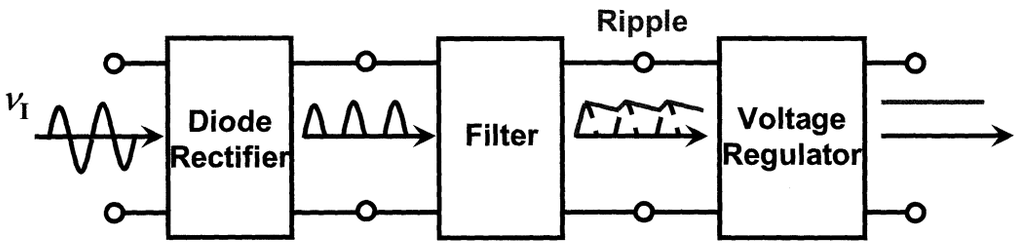
1.5 Rectifier Circuits

設為 ideal diode

(a)當 $v_I > 0$ V ➔ Diode ON ➔ $v_O = v_I$

(b)當 $v_I < 0$ V ➔ Diode OFF ➔ $v_O = 0$ V

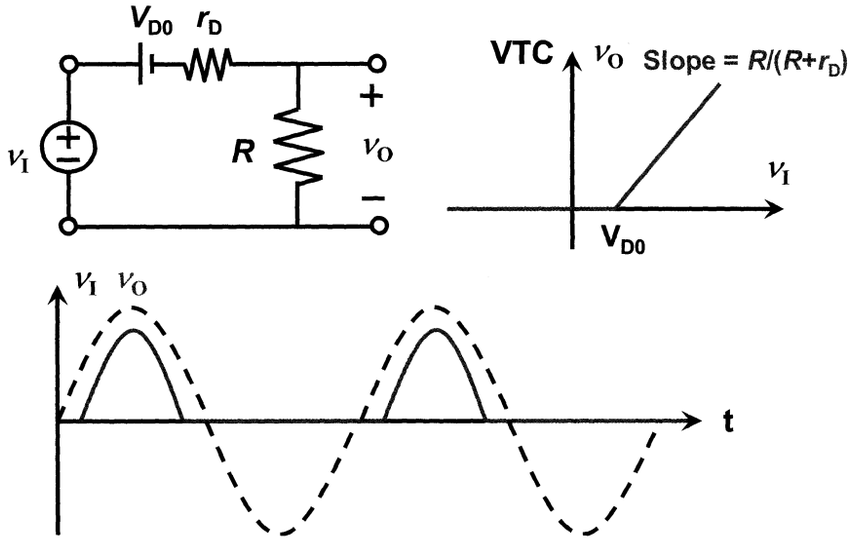




設為 battery-plus-resistor

(a)當 $v_I > V_{D0}$ ➔ Diode ON ➔ $v_O = (v_I - V_{D0}) \times \dfrac{R}{R + r_D}$

(b)當 $v_I < V_{D0}$ ➔ Diode OFF ➔ $v_O = 0$ V

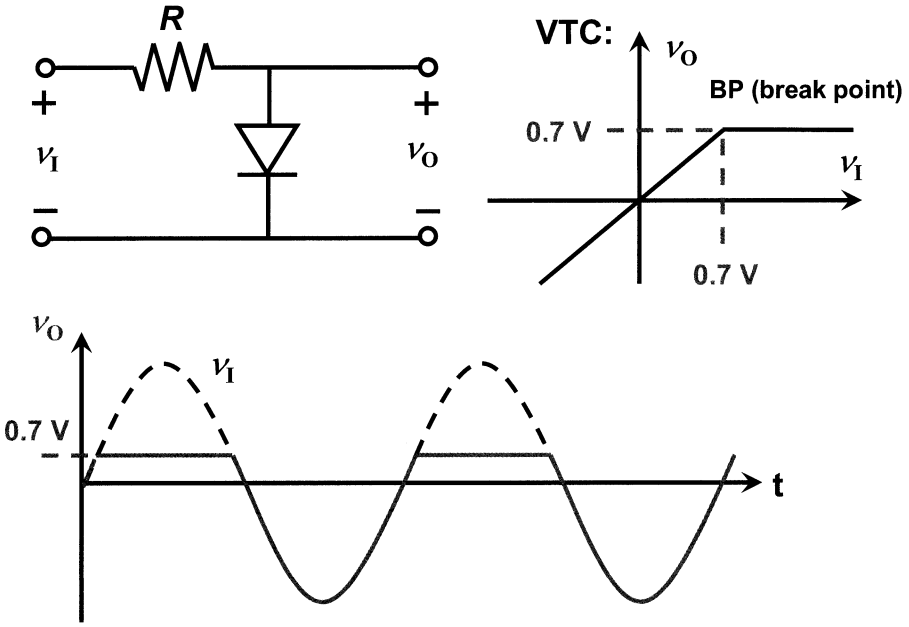


1.6 Limiting Circuits (Clipping Circuits)

設 D：Constant voltage drop (0.7 V)

(1) $v_I < 0.7$ V ➔ Diode OFF➔ $v_O = v_I$

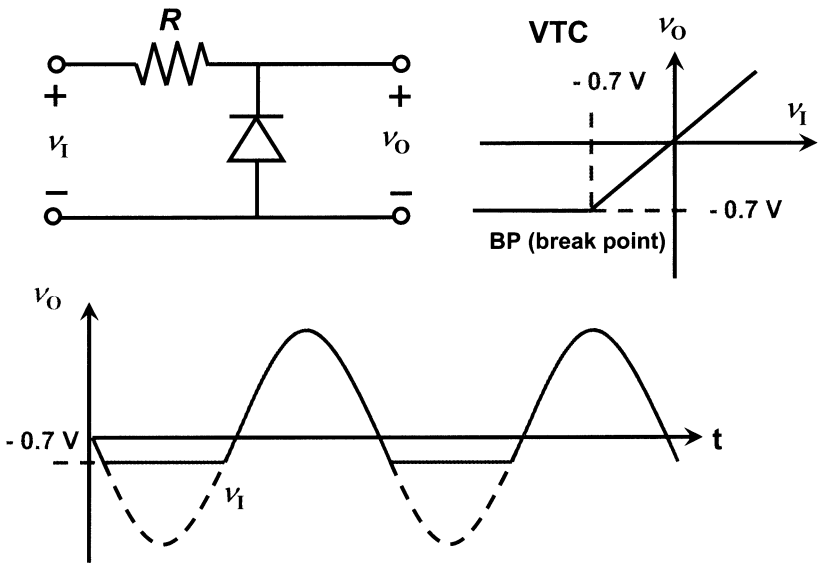
(2) $v_I > 0.7$ V ➔ Diode ON ➔ $v_O = 0.7$ V



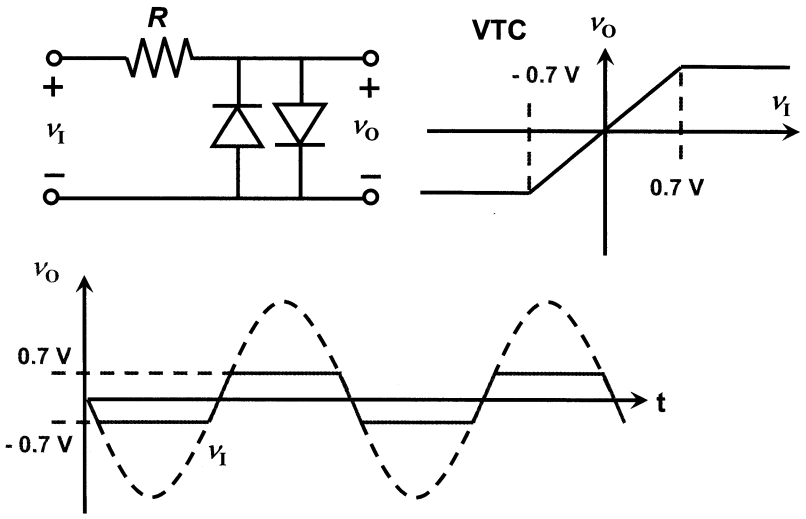
設 D：Constant voltage drop (0.7 V)

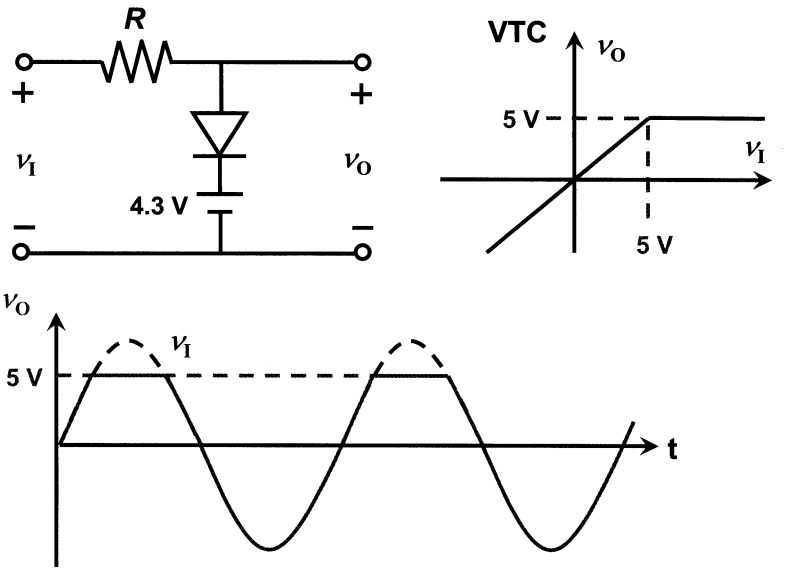
(1) $v_I < 0.7$ V ➔ Diode ON ➔ $v_O = 0.7$ V

(2) $v_I > 0.7$ V ➔ Diode OFF ➔ $v_O = v_I$

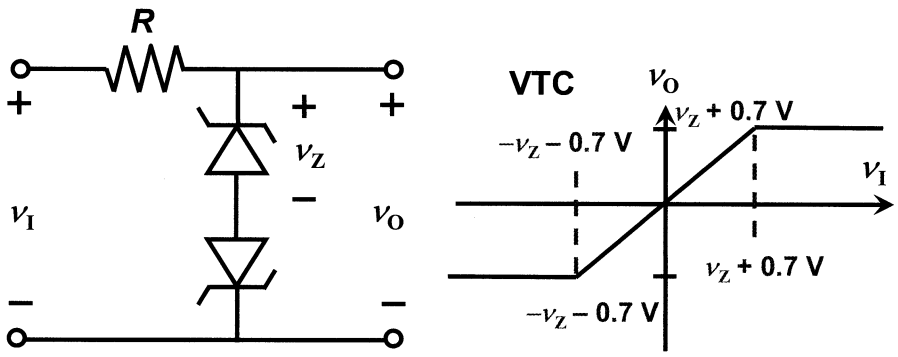


Double limiter：

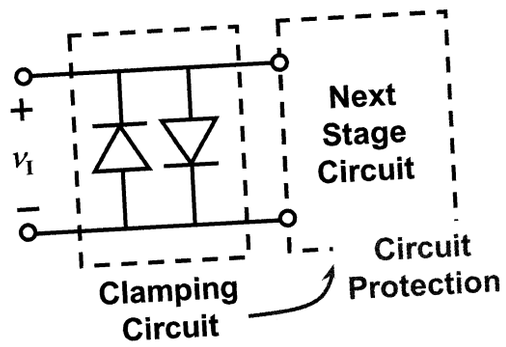




Zener diode (齊納二極體)：



Limiting circuit 功能：保護下一級電路。



Chapter 2: Bipolar Junction Transistors (BJTs)

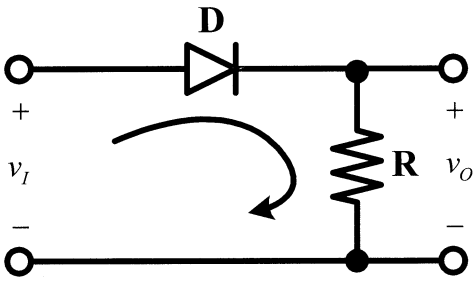
2.1 Device Structure and Physical Operation

Review of P-N junction diode:

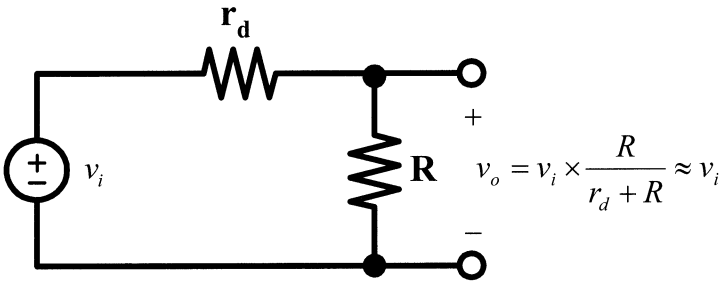
2 – Terminal Device

二極體最大的缺憾：沒有放大的功用。因此用途有限。

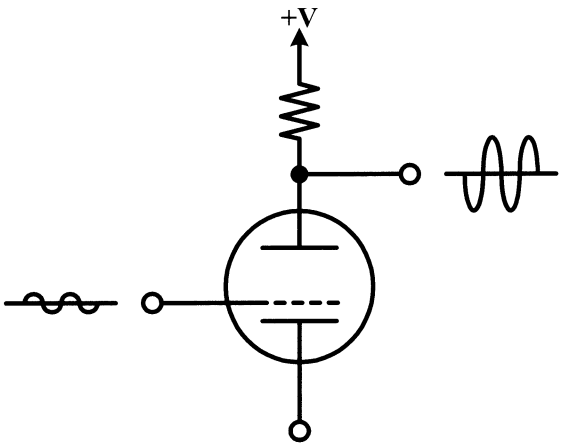
Large Signal:



Small Signal:

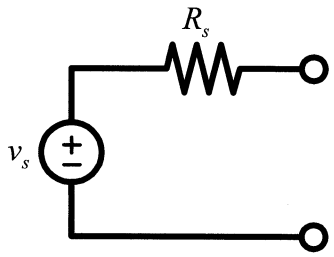


真空管 (三極管): voltage controlled

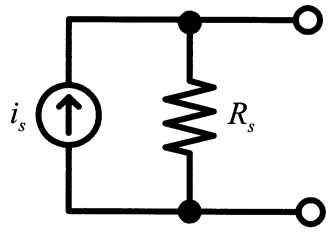


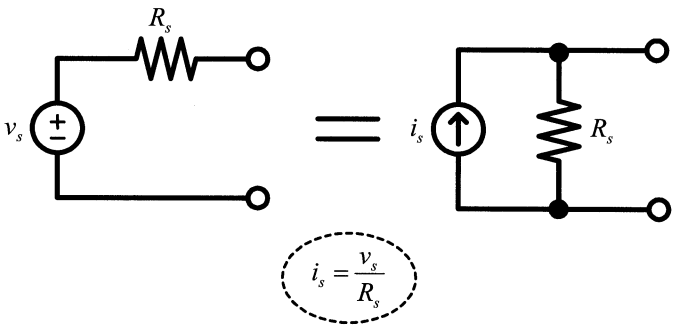
Signal source representations: **(small-signal, ac signal)**

(1) voltage type (Thevenin's)

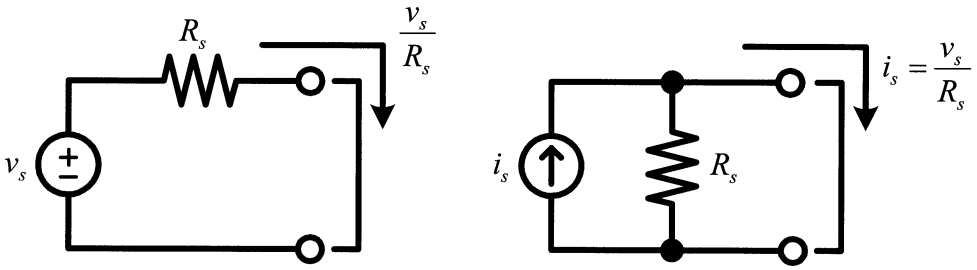


(2) current type (Norton's)

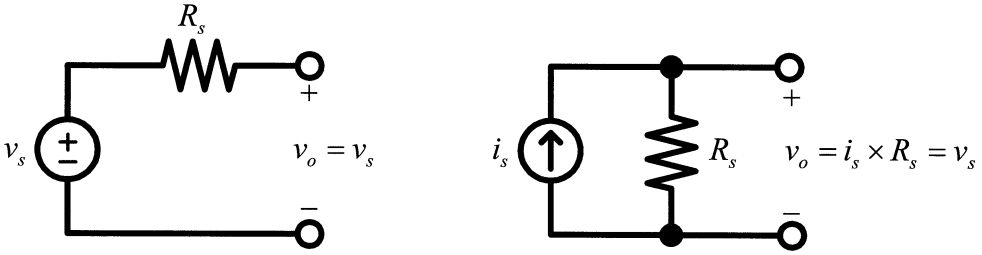




a. output "short"

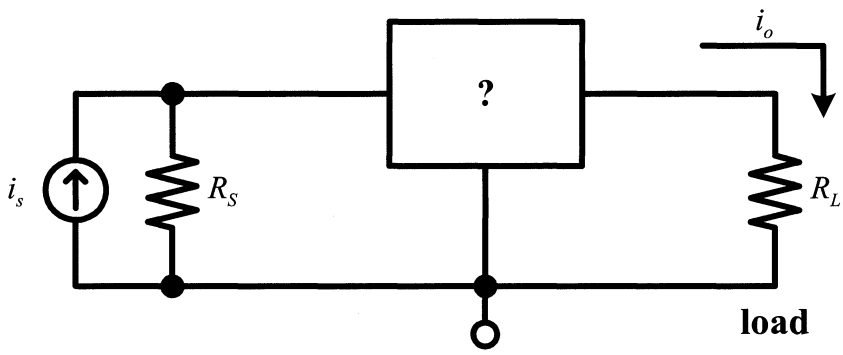


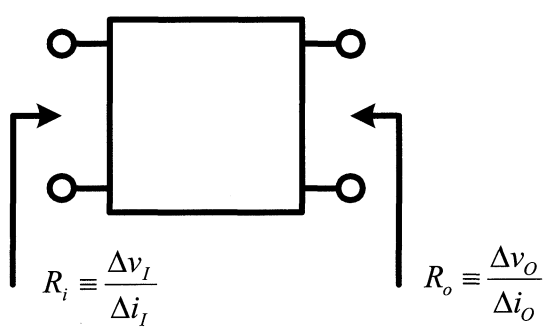
b. output "open"



如何製作一個 current controlled, current amplifier 的元件？

3 端元件





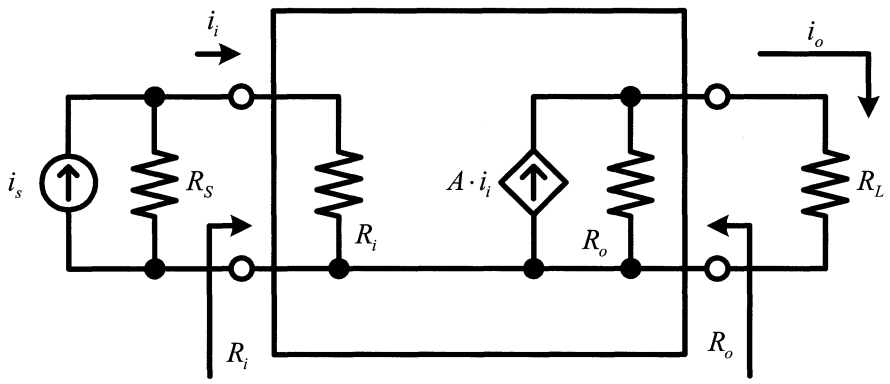
符號標示：

Independent current source

Dependent current source

Independent voltage source

Dependent voltage source

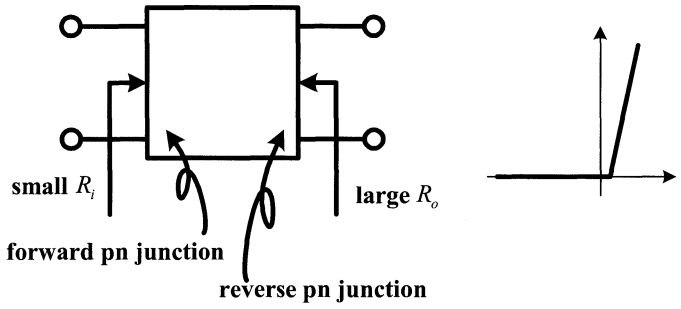


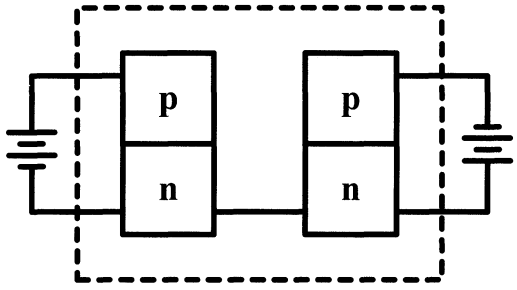
Requirements:

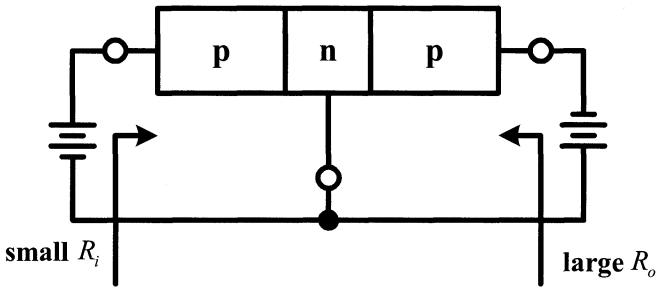
(1) A：大

(2) $i_i = i_s \cdot \dfrac{R_S}{R_S + R_i} \rightarrow i_s$ ➔ $R_i << R_S$

(3) $i_o = A \cdot i_i \times \dfrac{R_o}{R_o + R_L} \rightarrow A \cdot i_i$ ➔ $R_o >> R_L$



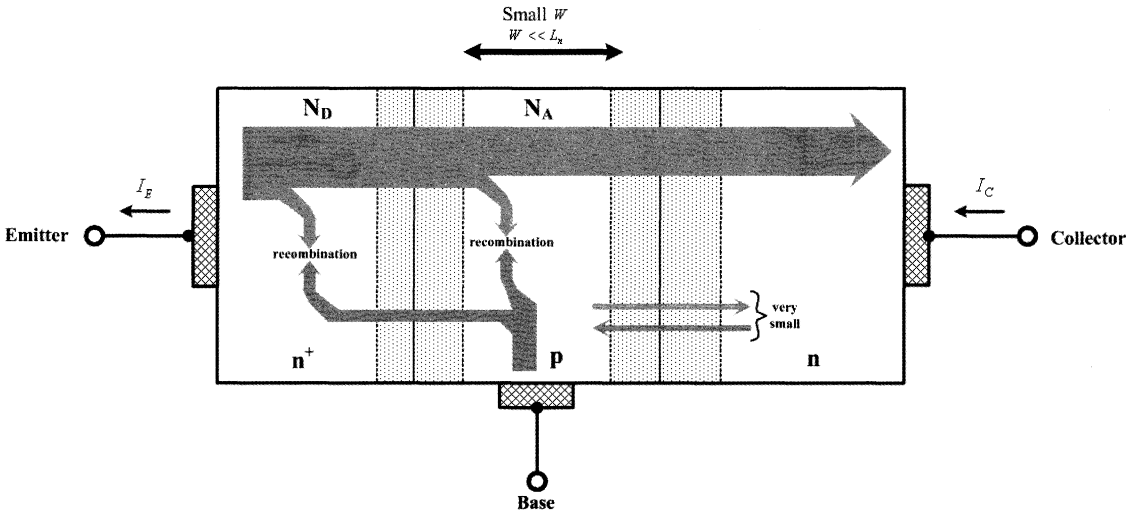




小 R_i ➔ 大 R_o

Transfer Res**istor** ➔ **Transistor**

電晶體發明人：Bardeen, Schottky, Brattain, in Bell Lab, 獲諾貝爾物理獎。

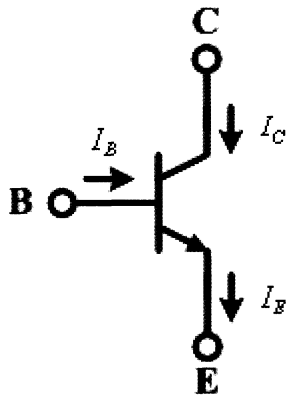


$N_E >> N_B$
$W_B << L_n$
} Large A

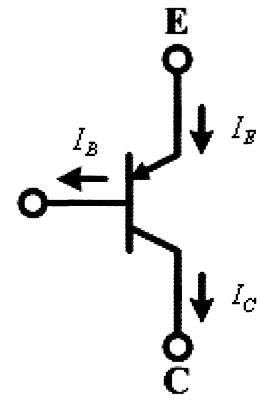
Circuit Symbols and Conventions

p ⟶ **n**

npn:

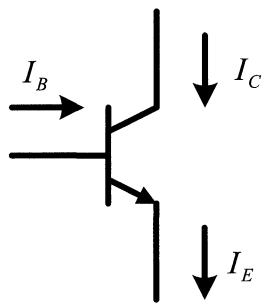


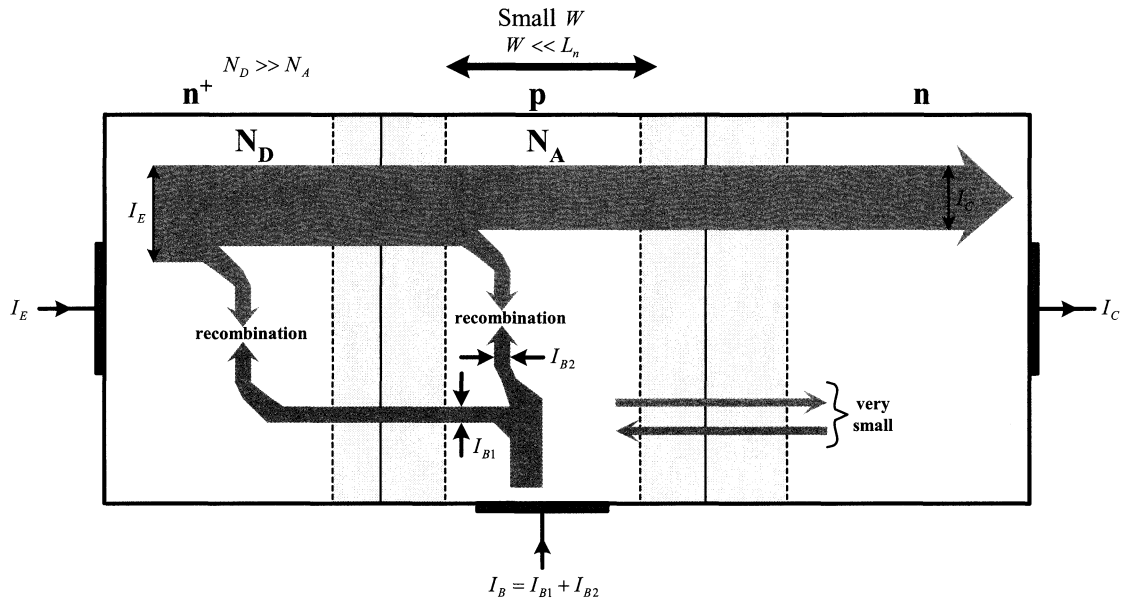
pnp:



EBJ	ECJ	Mode	Note
Forward	Reverse	(Forward) Active	$I_E \geq I_C >> I_B$
Reverse	Reverse	Cutoff	$I_B = 0$, $I_C = 0$, $I_E = 0$
Forward	Forward	Saturation	
Reverse	Forward	Reverse Active (or Inverted)	

Operation in the Active Mode





$I_C + I_B = I_E$

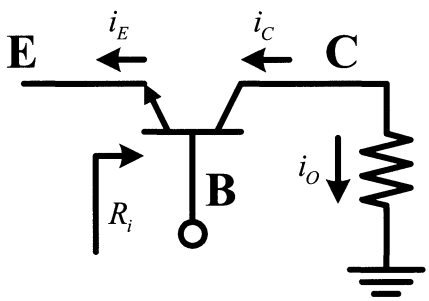
$W << L_n$ ➔ 擴散電流幾乎維持常數，沒有衰減，幾乎沒有在 Base 區和電洞發生 recombination。

擴散電流和梯度成正比。

擴散電流維持常數 ➔ 梯度幾乎維持直線

Current Gain～1, Voltage Gain=?? 是否有 amplifier 的功能？

common base configuration:



電壓訊號 = 電流訊號 × 電阻

輸入電壓訊號 = 輸入電流訊號 × 輸入電阻

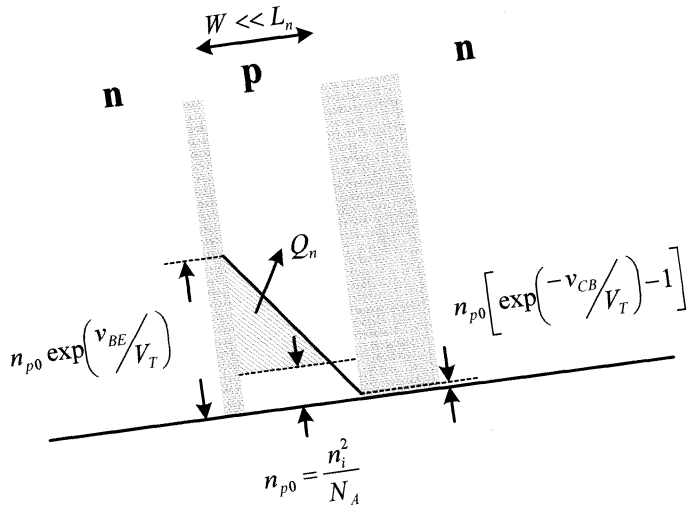
輸出電壓訊號 = 輸出電流訊號 × 輸出電阻

輸入電流訊號 ～ 輸出電流訊號

但是，輸出電阻 >> 輸入電阻 ($R_L >> R_i$)

➔ 有電壓的增益

➔ $|A_I| \leq 1$ ； $|A_V| >> 1$



In Base Region：

斜率：$\dfrac{n_{p0}\exp\left(v_{BE}/V_T\right)}{W_B}$

$$J_{n(diff)} = qD_n \frac{n_{p0}\exp\left(v_{BE}/V_T\right)}{W_B}$$

$$I_{n(diff)} = A_E \times J_{n(diff)} = A_E qD_n \frac{n_{p0}\exp\left(v_{BE}/V_T\right)}{W_B}$$ (Base Region 中少數載子的擴散電流)

$I_S \equiv \dfrac{A_E qD_n n_{p0}}{W_B}$ BJT Saturation Current or BJT Scale Current

➔ $I_{n(diff)} = I_S \exp\left(v_{BE}/V_T\right)$

➔ $i_C \approx I_{n(diff)} = I_S \exp\left(v_{BE}/V_T\right)$

i_C 和 Collector-Base 間的電壓(v_{CB})無關，和 Base-Emitter 間的電壓(v_{BE})有關。此外，和 Collector Junction 的面積(A_C)無關係，而主要和 Emitter Junction 的面積(A_E)

有關！(在現今的製程中，$A_C >> A_E$)。
而實際上，A_C的大小，主要是考量到電晶體散熱的問題。
電晶體在運作時，主要的熱能產生在 collector junction 處。所以製作上需要靠大的 collector junction 幫助散熱。

比較 Diode 與 BJT 的 Scale Current

Diode: $I_S = Aq\left(\frac{D_n n_{p0}}{L_n} + \frac{D_p p_{n0}}{L_p}\right) = Aqn_i^2 \times \left(\frac{D_n}{L_n N_A} + \frac{D_p}{L_p N_D}\right)$

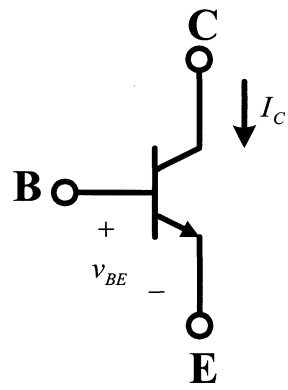
BJT: $I_S = A_E q \frac{D_n n_{p0}}{W_B}$

真正有用的輸出電流，是靠：
➔ Base region 中的 minority current 的 diffusion current。

$$i_C = I_S \exp\left(v_{BE}/V_T\right)$$

當 emitter 端 **OPEN** ➔ $I_E = 0$
➔ $I_C = 0$ **??**
當 collector 接 "+"，base 接 "-"，Base-Collector Junction 逆向偏壓的電流考慮之。
➔ I_{CBO}

完整的i_C電流公式應為：
$i_C = I_S \exp\left(v_{BE}/V_T\right) + I_{CBO}$，$I_{CBO}$可忽略。



$$i_C = I_S \exp\left(v_{BE}/V_T\right) \quad \text{Where} \quad I_S = A_E q \frac{D_n n_{p0}}{W_B}$$

$$i_E = i_C + i_B$$

$$i_B = i_{B1} + i_{B2}$$

$$i_{B1} = \left(A_E q \frac{D_p p_{n0}}{L_p}\right) \cdot \exp\left(v_{BE}/V_T\right) = I_S \left(\frac{D_p}{D_n} \cdot \frac{N_A}{N_D} \cdot \frac{W_B}{L_p}\right) \cdot \exp\left(v_{BE}/V_T\right)$$

$L_p >> W_B$; $N_D >> N_A$ ➔ i_{B1} is very small! (越小越好)

$$i_{B2} = \frac{Q_n}{\tau_b}$$

τ_b : minority carrier (mean) lifetime (before recombination)

$$Q_n = \frac{1}{2} \cdot q \cdot W_B \cdot n_p(0) \cdot A_E \qquad n_p(0) = n_{p0} \exp\left(v_{BE}/V_T\right)$$

➔ $$i_{B2} = \frac{q W_B A_E n_{p0} \exp\left(v_{BE}/V_T\right)}{2\tau_b} = I_S \cdot \left(\frac{W_B^2}{2\tau_b D_n}\right) \cdot \exp\left(v_{BE}/V_T\right)$$

$$\therefore \quad i_B = \left(\frac{D_p}{D_n} \cdot \frac{N_A}{N_D} \cdot \frac{W_B}{L_p} + \frac{W_B^2}{2D_n\tau_b}\right) \times i_C$$

➔ $$\beta \equiv \frac{1}{\left(\frac{D_p}{D_n} \cdot \frac{N_A}{N_D} \cdot \frac{W_B}{L_p} + \frac{W_B^2}{2D_n\tau_b}\right)}$$

➔ $i_B = \frac{i_C}{\beta}$ ➔ $\beta = \frac{i_C}{i_B}$ (current gain of CE configuration)

$$i_E = i_C + i_B = i_C + \frac{i_C}{\beta} = \left(\frac{\beta+1}{\beta}\right)\cdot i_C = \frac{i_C}{\alpha} \qquad \alpha = \frac{\beta}{\beta+1}$$

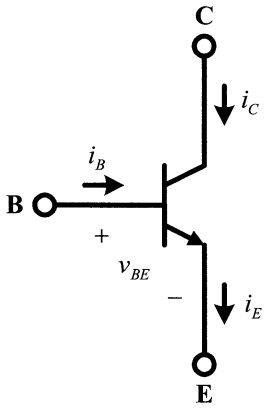
$$\beta = \frac{i_C}{i_B}$$

$$\alpha = \frac{i_C}{i_E}$$

$$\alpha = \frac{\beta}{\beta+1} \Leftrightarrow \beta = \frac{\alpha}{1-\alpha}$$

注意！！以上的電流表示式，並沒有將漏電流(I_{CBO})考慮進。

2.2 Current-Voltage Characteristics



Active Region

$$i_C = I_S \exp\left(v_{BE}/V_T\right) \text{ where } V_T \approx 25mV$$

$$i_B = \frac{i_C}{\beta} = \frac{I_S}{\beta}\exp\left(v_{BE}/V_T\right)$$

$$i_E = i_B + i_C = \frac{\beta+1}{\beta} I_C = \frac{\beta+1}{\beta} I_S \exp\left(v_{BE}/V_T\right)$$

$$i_C = I_C + i_c \qquad i_B = I_B + i_b$$

$$\beta \approx \frac{\Delta i_C}{\Delta i_B} \approx \frac{i_C}{i_B} \approx \frac{I_C}{I_B} \approx \frac{i_c}{i_b}$$

$\beta = \dfrac{i_C}{i_B}$ ➔ **Common Emitter (CE) current gain**

$$\alpha = \frac{\beta}{\beta+1} \approx \frac{\Delta i_C}{\Delta i_E} \approx \frac{i_C}{i_E} \approx \frac{I_C}{I_E} \approx \frac{i_c}{i_e}$$

$$\beta = \frac{\alpha}{1-\alpha}$$

若 $\Delta\alpha : 0.99 \rightarrow 0.995$

$$\alpha = 0.99 \quad \rightarrow \quad \beta = \frac{0.99}{1-0.99} = 99$$

$$\alpha = 0.995 \quad \rightarrow \quad \beta = \frac{0.995}{1-0.995} = 199$$

$\Delta\alpha$ 的變化造成很大的 $\Delta\beta$ 的變化

➔意即為何電晶體的 β 的變化很廣，即使同一型號的電晶體其 β 亦有大差異。

2.3 Large-Signal Model

Equation Model:

(1) $i_C = I_S \exp\left(v_{BE}/V_T\right)$

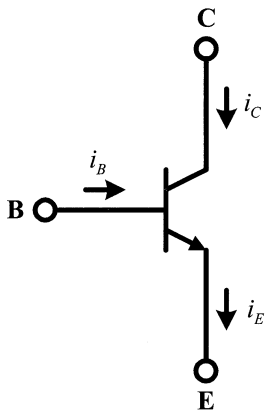
(2) $i_B = \frac{i_C}{\beta} = \frac{I_S}{\beta}\exp\left(v_{BE}/V_T\right)$

(3) $i_E = i_C + i_B$

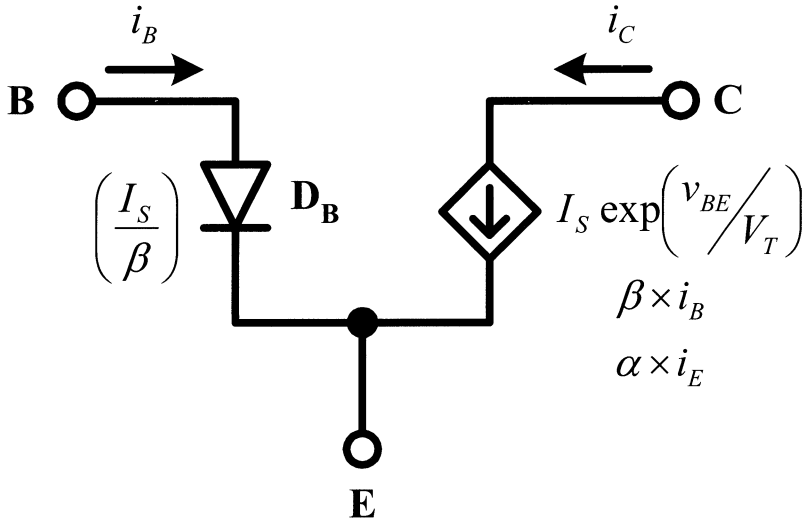
Circuit Model:

NPN Type:

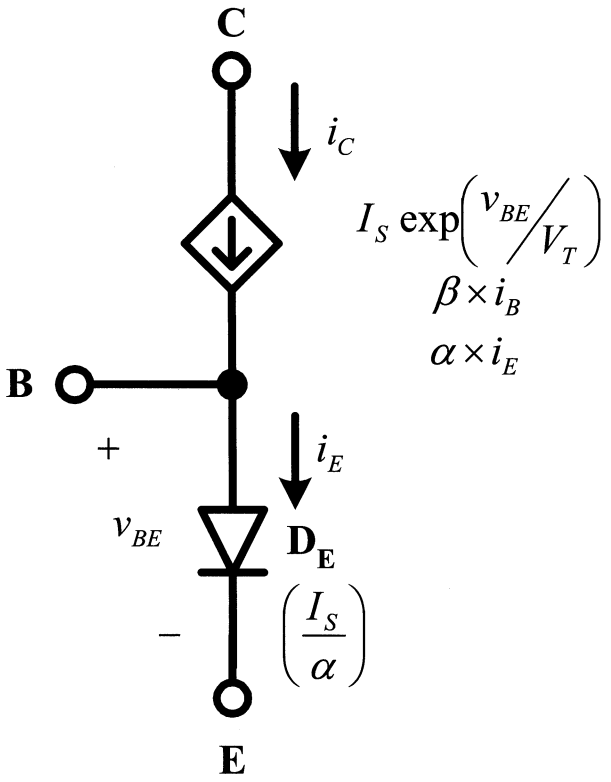
Circuit Model:



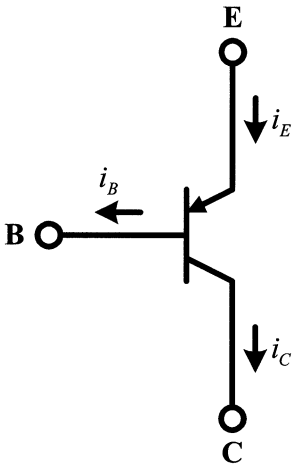
(1) π-model (將輸入端，PN 接面的電流，通通計算在 **Base** 端)



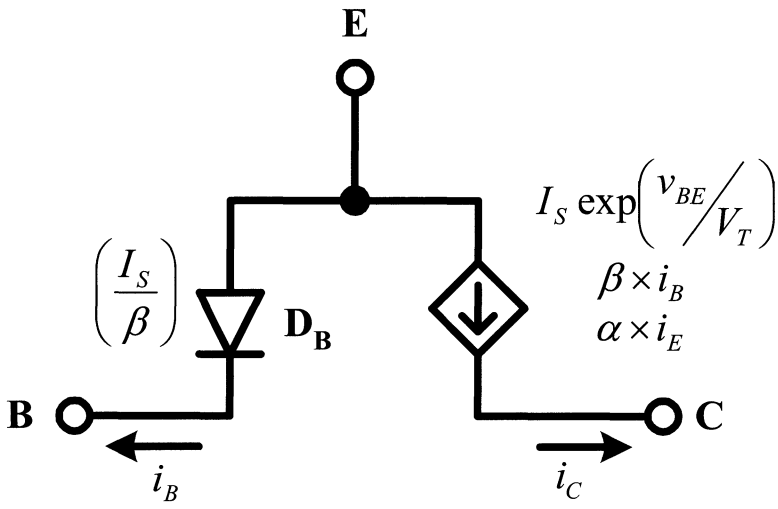
(2) T-model (將輸入端，PN 接面的電流，通通計算在 **Emitter** 端)



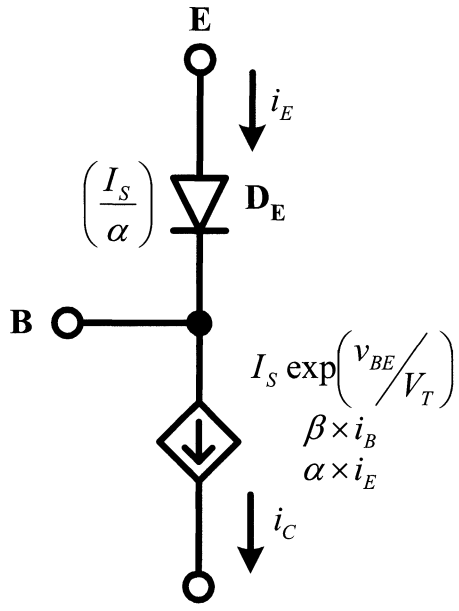
PNP Type



(1) π-model (將輸入端，PN 接面的電流，通通計算在 **Base** 端)



(2) T-model (將輸入端，PN 介面的電流，通通計算在 **Emitter** 端)



$\mu_n > \mu_p$; $D_n > D_p$

因此，npn type 比 pnp type 常被使用。但是，pnp 仍是需要，主要作為互補的作用。

注意:

電晶體將小訊號放大(不管是電壓或是電流訊號)，是不是表示能量增加？

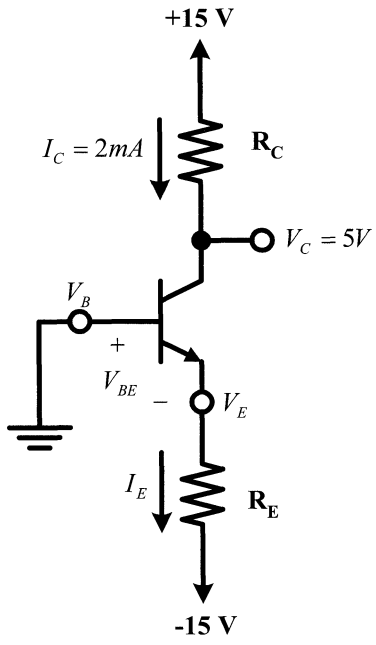
➔不是！

➔注意！電晶體本身不是能源，不儲存任何能量。但是，小訊號變成大訊號時，能量增加！

➔那麼，能量從哪來呢？

➔所有的能量由直流電源或電池提供。改變能量的型態。

Example:



Given $\begin{cases} v_{BE} = 0.7V \text{ at } i_C = 1mA \\ \beta = 100 \\ (I_{CBO} \text{ 忽略}) \end{cases}$

Design the circuit，

使 $I_C = 2mA$ 以及 $V_C = 5V$ ，求 R_C 以及 R_E 的值。

(精確算計算)

(➔使用 exponential model)

Sol:

$$R_C = \frac{15V - 5V}{2mA} = 5k\Omega$$

$$I_E = \frac{\beta + 1}{\beta} \times I_C = 1.01 \times 2mA = 2.02mA$$

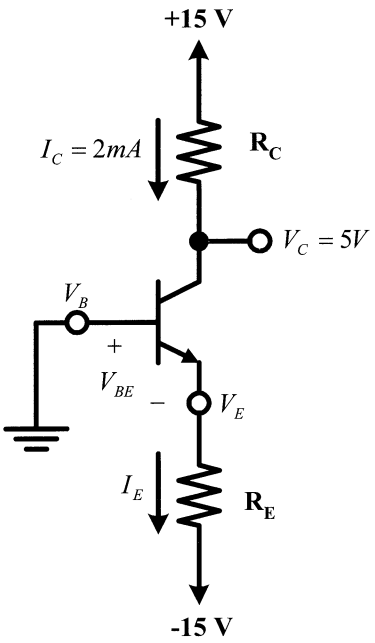
$$V_{BE} = 0.7 + V_T \times \ln\left(\frac{2mA}{1mA}\right) = 0.7V + 25mV \times \ln 2 \approx 0.717V$$

Therefore, $V_E = 0 - 0.717 = -0.717V$

$$R_E = \frac{(-0.717V) - (-15V)}{2.02mA} = 7.07k\Omega$$

大訊號等效電路 model 本身是備而不用，並不是每次分析都會用到。

Example:



Design the circuit，

使 $I_C = 2mA$ 以及 $V_C = 5V$ ，求 R_C 以及 R_E 的值。

(簡單計算)

(➔取 $V_{BE} = 0.7V$ ， $I_C = I_E$)

Sol:

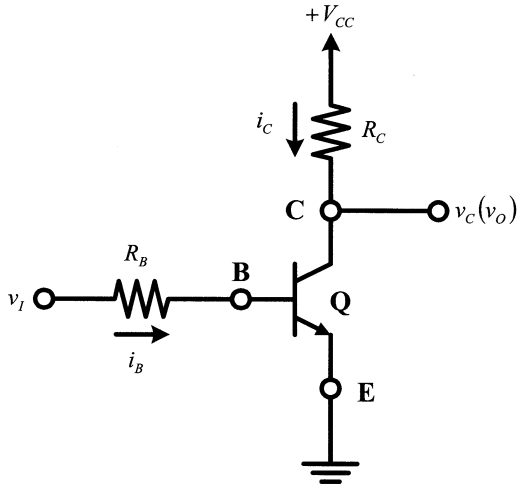
$$R_C = \frac{15V - 5V}{2mA} = 5k\Omega$$

$$R_E = \frac{(-0.7V) - (-15V)}{2mA} = 7.15k\Omega \qquad (\text{上一個例題，} R_E = 7.07k\Omega)$$

在 discrete 的電路設計，可以不用非常精確的計算，因為 discrete 電阻的值並不是連續的，並且有誤差。

若是在 IC 電路的設計情況下，電阻可以製作的較為連續，此情況下進行精確的計算才有意義。

2.4 Operation as a Switch



假設：

EBJ: constant voltage drop 0.7V

CBJ: constant voltage drop **0.5V** (Generally, because of $I_{SC} >> I_{SE}$)

Emitter 的濃度遠大於 collector 的濃度 ➔ $N_C << N_E$

Collector junction 的面積大於 Emitter junction 的面積 ➔ $A_C >> A_E$

➔ Collector junction 的 scale current 遠大於 Emitter junction 的 scale current。

➔ $I_{SC} >> I_{SE}$

(1) $v_I < 0.5V(0.7V)$

➔ EBJ: 逆偏 & CBJ: 逆偏

➔ 電晶體(Q)工作在 cutoff region

➔ $i_B = 0$, $i_C = 0$

➔ $V_C = V_{CC} - i_C \times R_C = +V_{CC}$

(2) $v_I > 0.7V$, $v_C > V_{CE,sat} = 0.2V$

➔ EBJ: 順偏 & CBJ: 逆偏

➔ Q 工作在 active region

➔ $i_B = \dfrac{v_I - 0.7V}{R_B}$

➔ $i_C = \beta \cdot i_B$ (斜率為 i_B 的 β 倍)

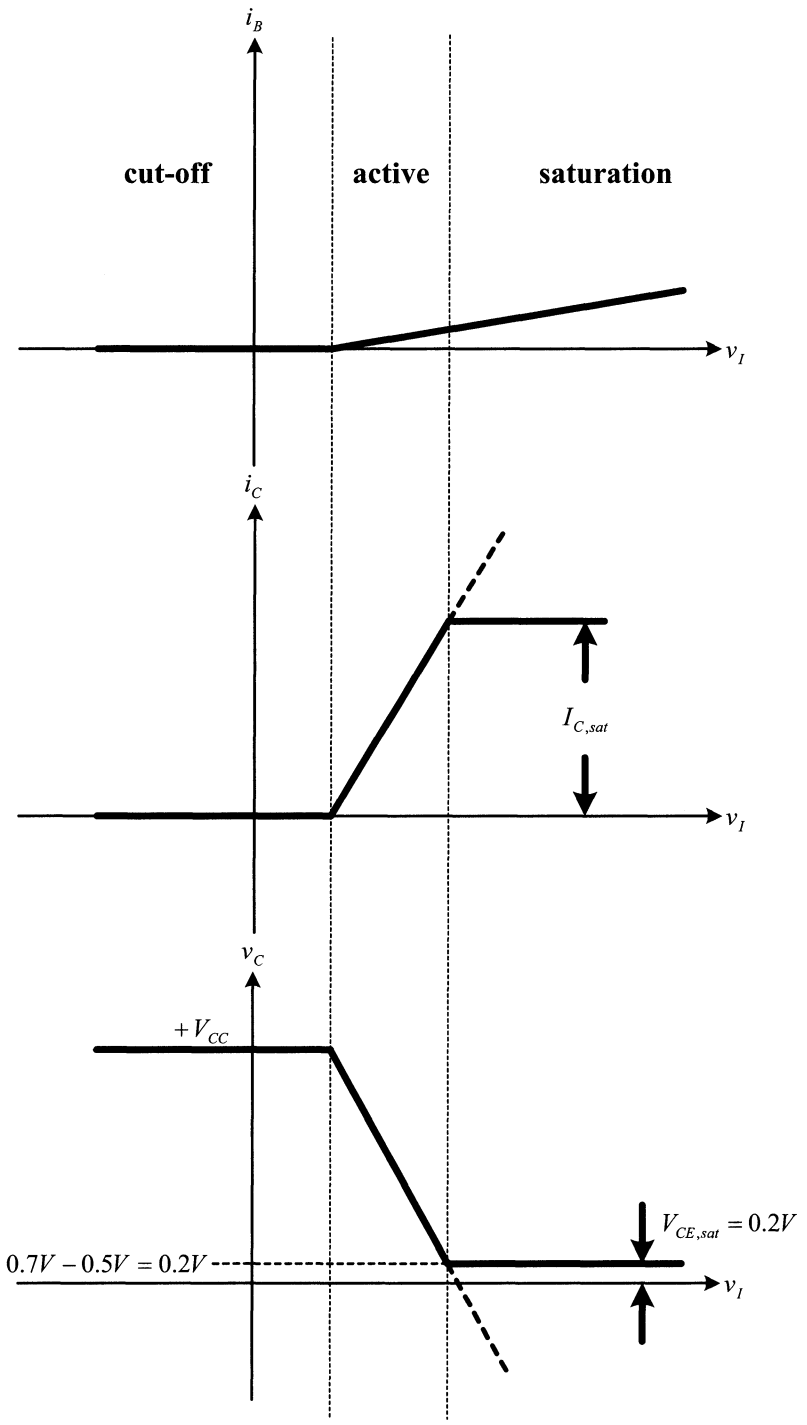
➔ $v_C = V_{CC} - i_C \times R_C$

(3) $v_I \uparrow\uparrow$

➔ Q 進入 saturation region

➔ $v_C = V_{CE,sat} = 0.2V \quad (0.7V - 0.5V)$

➔ $i_C = \dfrac{V_{CC} - V_{CE,sat}}{R_C} \equiv I_{C,sat}$



$\beta = \frac{i_C}{i_B}$ (in active region)

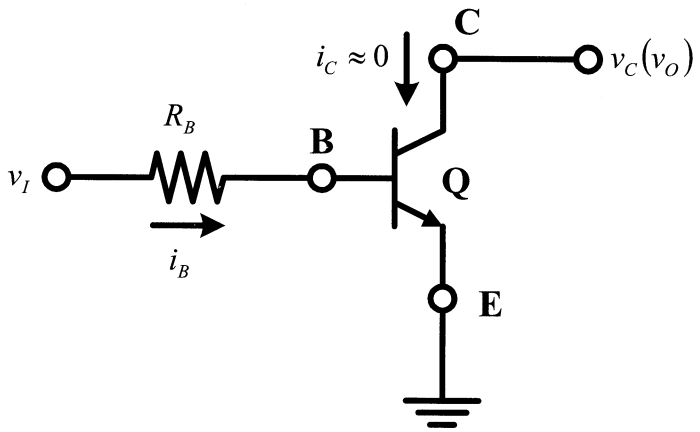
若電晶體工作在 saturation region:

$i_C < \beta \cdot i_B$

$\frac{i_C}{i_B} = \frac{I_{C,sat}}{i_B} \equiv \beta_{forced} \leq \beta$

β_{forced}：電晶體工作在飽和區時，飽和電流($I_{C,sat}$)和 Base 電流(I_B)的比。

觀念問題：



若 $R_C \to \infty$ (Open)，v_I 接正電壓，電晶體工作在何區域？

Cutoff Region	Incorrect
Active Region	Incorrect
Reverse Active Region	Incorrect
Saturation Region	**Correct**

Discussions:

(1) Cutoff Region?

兩個 junction (EBJ, CBJ)皆是 reverse bias 才是工作在 cut-off region

但是 EBJ 是 forward bias ➔ Not cutoff region

(2) Active Region?

若為 active region，則 $i_C = \beta \cdot i_B$ 要成立

已知 $i_C = 0$。但是 $i_B \neq 0$ ！！ ➔ Not Active region

(3) Saturation Region?

原本的討論是 I_C 電流增加到最後飽和後，隨即進入 saturation region。

亦即 $i_C = I_{C,sat}$

但是此 case，$i_C = 0$，算進入飽和區嗎？

“ 觀念釐清 “

何謂進入飽和區？

➔ 只要 $i_C < \beta \cdot i_B$ ➔ 即進入飽和區。

➔ $i_C = 0 \le \beta \cdot i_B \neq 0$ 不等式成立

因此，此電晶體工作在 saturation region

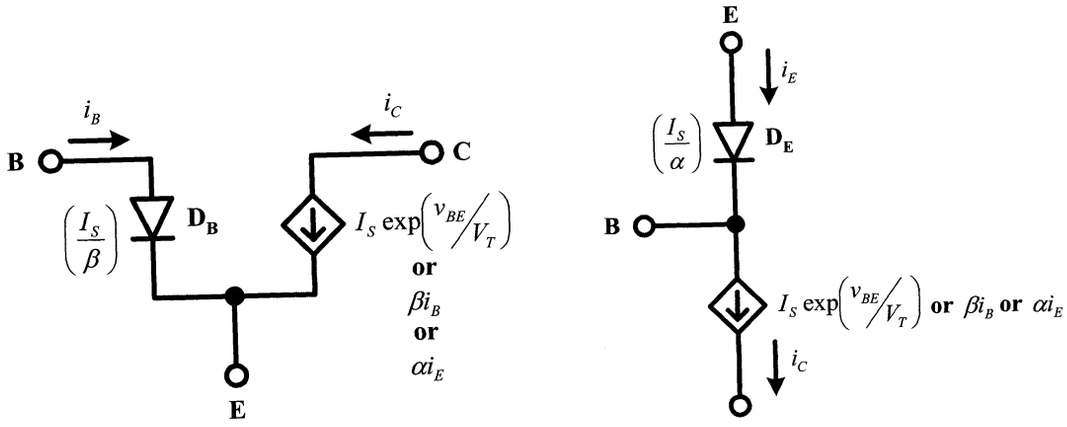
(飽和電流為 0 之飽和，因為 $i_C = 0 \le \beta \cdot i_B \neq 0$)

而兩個 junction (EBJ, CBJ)也必然順偏。

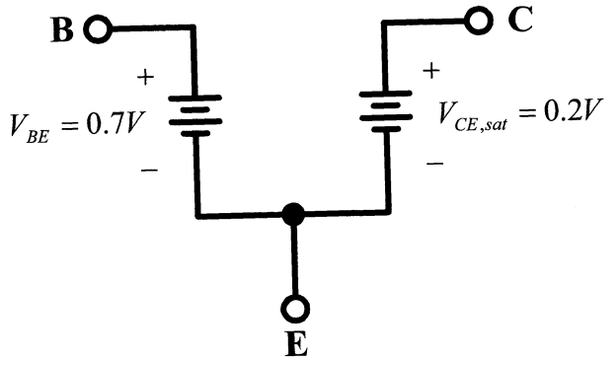
$$i_C = \left.\frac{V_{CC} - V_{CE,sat}}{R_C}\right|_{R_C \to \infty} = I_{C,sat} \to 0$$

當 Q 工作在 **saturation region** 時，其大訊號的等效模型為何？

Review of the Large-Signal Model of transistor, Q, operating in active region:



Large-Signal Model of Q operating in "**saturation region**"



電晶體工作在飽和區時，沒有放大訊號的作用。

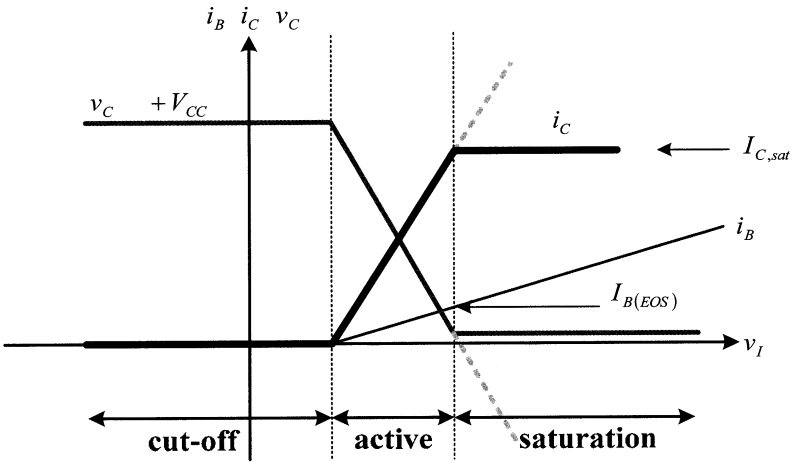
(放大訊號，為電晶體工作在 active region 時的應用。)

飽和區的應用 ➔ 電子開關(switch)運用。➔ 數位電路的應用

當開關時，(要避開 active region)

➔ 低電壓輸入時，v_I 要夠低，使電晶體進入 cutoff ➔ v_C 為高電位 V_{CC}

➔ 高電壓輸入時，v_I 要夠高，使電晶體進入飽和區 ➔ $v_C = V_{CE,sat} \approx 0.2V$



$I_{B(EOS)}$ 在 **E**dge **o**f **S**aturation 處的 i_B 電流。

唯一的一工作點，其 $I_{B(EOS)} \times \beta = I_{B(EOS)} \times \beta_{forced} = I_{C,sat}$

➔ $I_{B(EOS)} = \dfrac{I_{C,sat}}{\beta} = \dfrac{I_{C,sat}}{\beta_{forced}}$

$\dfrac{I_B}{I_{B(EOS)}} \equiv$ overdrive factor

一般來說，要使電晶體操作在飽和區時，overdrive factor 大約取 2~10 倍，

2.5 Graphical Representations of Transistor Characteristics

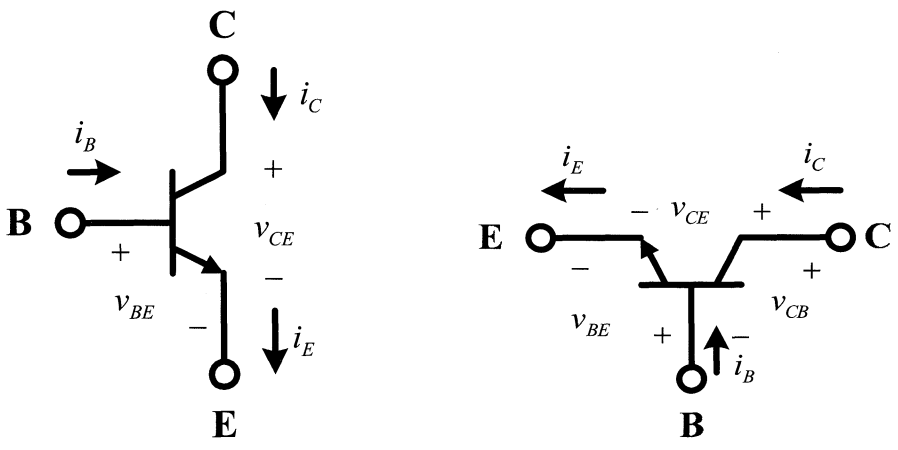
Review:

(1) Equation Model

(2) Circuit Model

(3) … to be discussed in this chapter

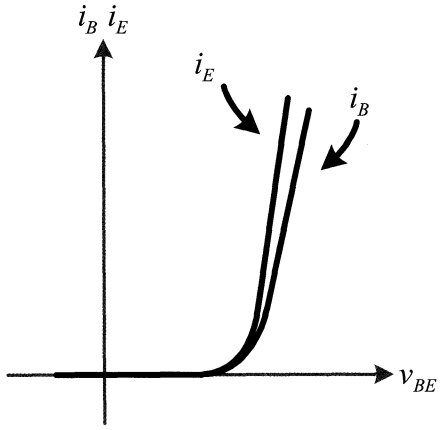
圖解法



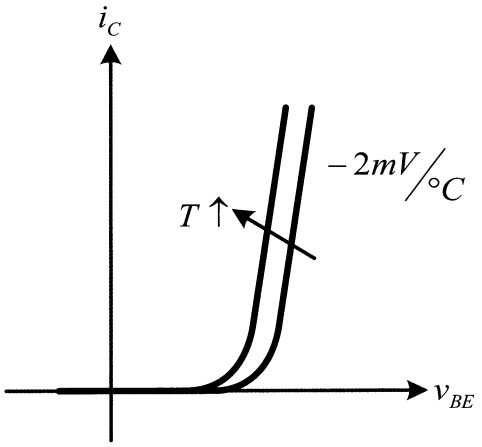
Input characteristics – i_E or i_B V.S. v_{BE}

From equation,

$$\begin{cases} i_B = \dfrac{I_S}{\beta}\exp\left(v_{BE}/V_T\right) \\ i_E = \dfrac{I_S}{\alpha}\exp\left(v_{BE}/V_T\right) \end{cases}$$



Transfer characteristics – i_C V.S. v_{BE}



Output characteristics – i_C V.S. v_{CE}

From equation:

$i_C = I_S \exp\left(v_{BE}/V_T\right)$ independent of v_{CE}

分成兩種情況討論

– common base type (i_C V.S. v_{CB})

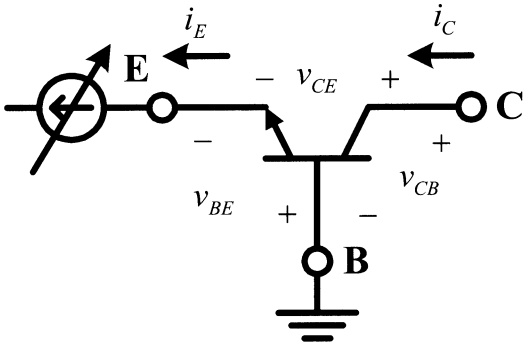
– common emitter type (i_C V.S. v_{CE})

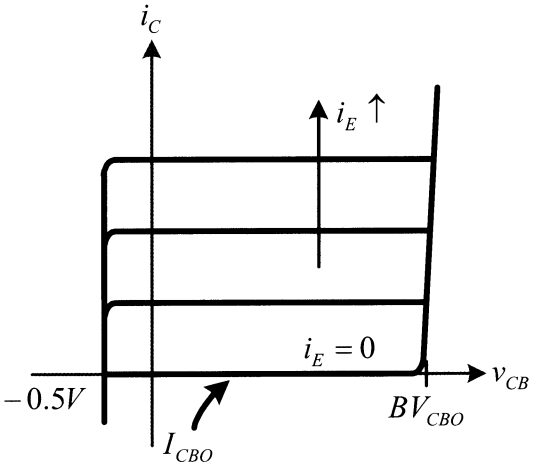
Common Base Type:

(1) 當 emitter open ($i_E = 0$) ➔ $i_C = I_{CBO}$

(2) $i_E > 0$, in active region, $i_C = \alpha \cdot i_E$

作圖： i_C V.S. v_{CB}，以 i_E 為參數



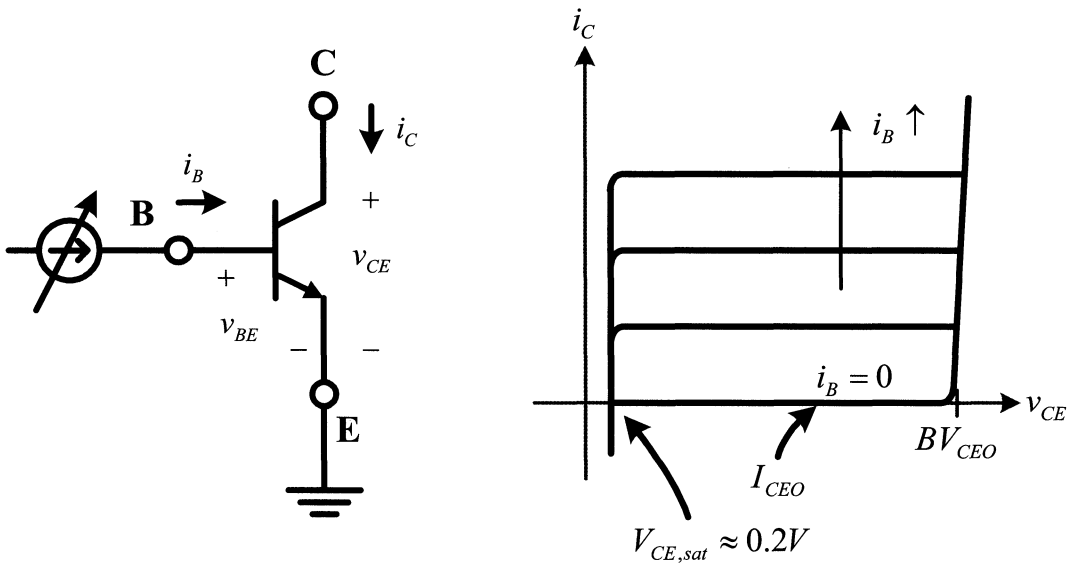


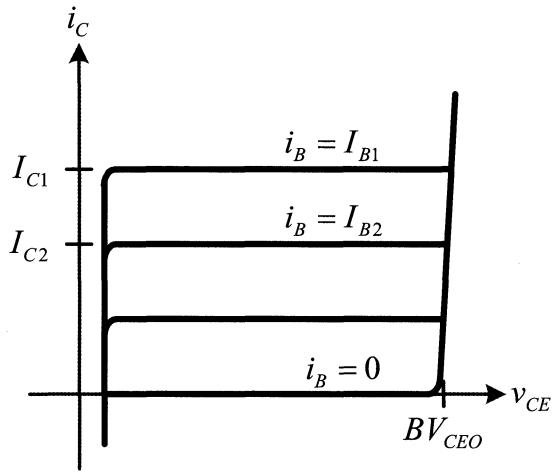
Common Emitter Type:

(1) 當 Base open ($i_B = 0$) ➔ $i_C = I_{CEO}$ (usually, $I_{CEO} > I_{CBO}$)

(2) $i_B > 0$, in active region, $i_C = \beta \cdot i_B$

作圖： i_C V.S. v_{CE}，以 i_B 為參數



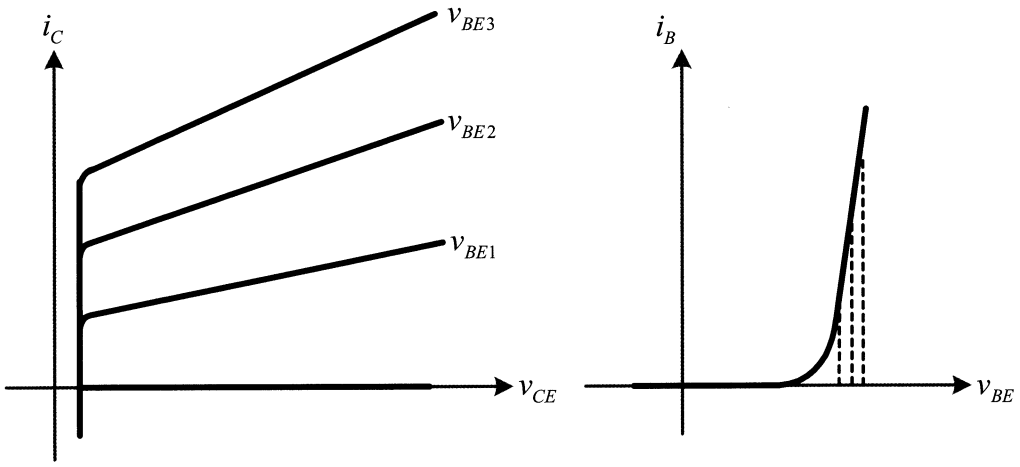


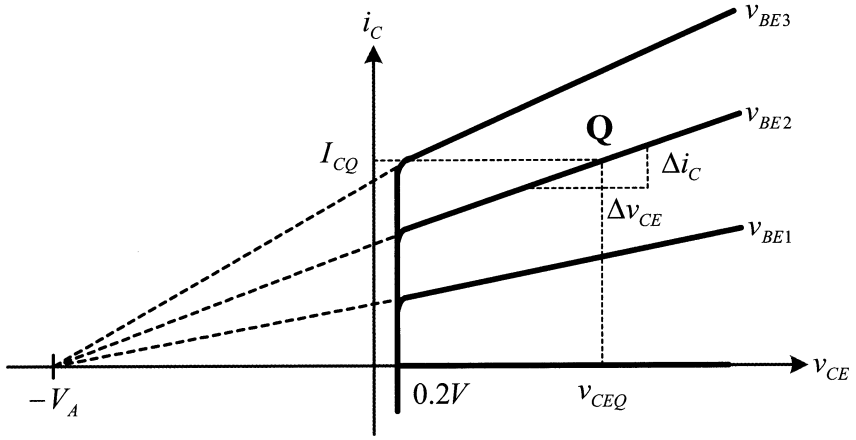
$$\beta \equiv \frac{\Delta i_C}{\Delta i_B} = \frac{I_{C1} - I_{C2}}{I_{B1} - I_{B2}}$$ 稱為 incremental β 或是 β_{ac}

$$\beta_{dc} \equiv \frac{i_C}{i_B}$$

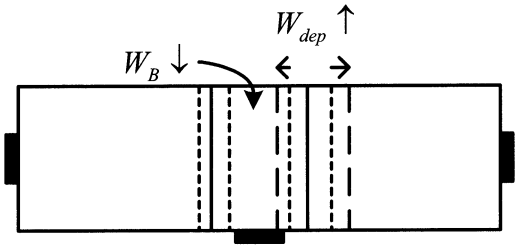
$$\beta_{ac} \approx \beta_{dc}$$

Early Effect





V_A : **Early Voltage**



為何電流在 active region 處，不是維持 constant，而會隨著 v_{CE} 增加而增加？

➔ 當 collector junction 逆向偏壓增加時，其 depletion region 變更寬，等效的 base width 會變窄，使得基極區的少數載子的分佈斜率變大

➔ 擴散電流變大 (因為擴散電流和少數載子的分佈斜率成正比)

$v_{CE}\uparrow$ ➔ $W_B\downarrow$ ➔ $I_S\uparrow$ ➔ $i_C\uparrow$ $\quad (I_S \propto 1/W_B)$

因此，電流關係式需做小修正，

$$i_C = I_S \exp\left(v_{BE}/V_T\right)\left(1+\frac{v_{CE}}{V_A}\right)$$

電晶體需工作在 active region 才成立 ($v_{CE} > 0.2V$)

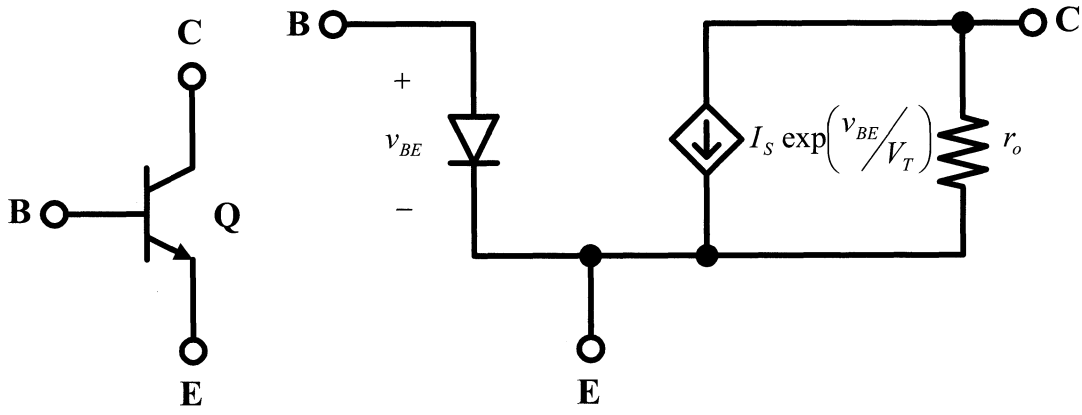
$$\frac{\Delta i_C}{\Delta v_{CE}} = \frac{1}{\left(\Delta v_{CE}/\Delta i_C\right)}$$

Output resistance $r_o \equiv \left.\frac{\partial v_{CE}}{\partial i_C}\right|_{V_{BE}} = \frac{V_A + V_{CEQ}}{I_{CQ}} \approx \frac{V_A}{I_{CQ}} \qquad (V_A >> V_{CEQ})$

V_A (Early Voltage)主要和 Base 的寬窄有關。

➔ Base 寬，Early Effect 較不明顯，V_A 較大；反之，Base 窄，V_A 變小。

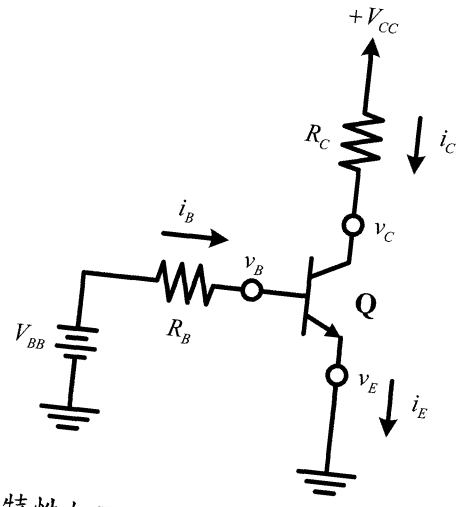
當考慮 Early Effect，則原電晶體的大訊號模型需作些許修正，如下：



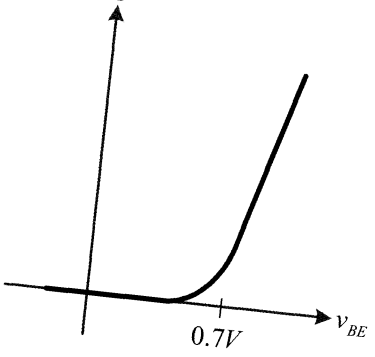
2.6 Graphical Analysis

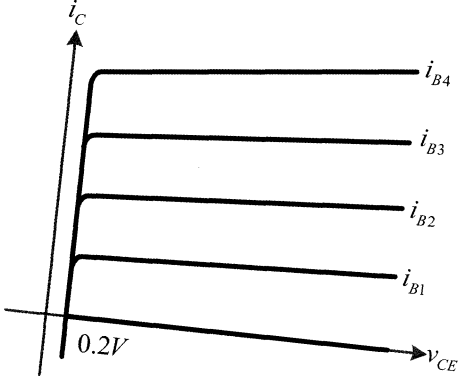
使用 graphical analysis，目的在獲得"精確"的解。

Example：(DC analysis)



已知電晶體的輸入、輸出特性如下：

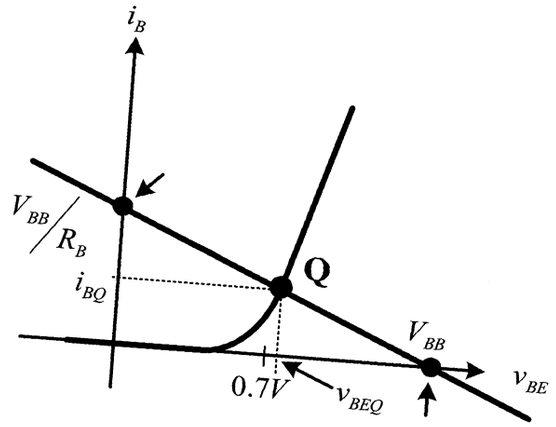




Sol:

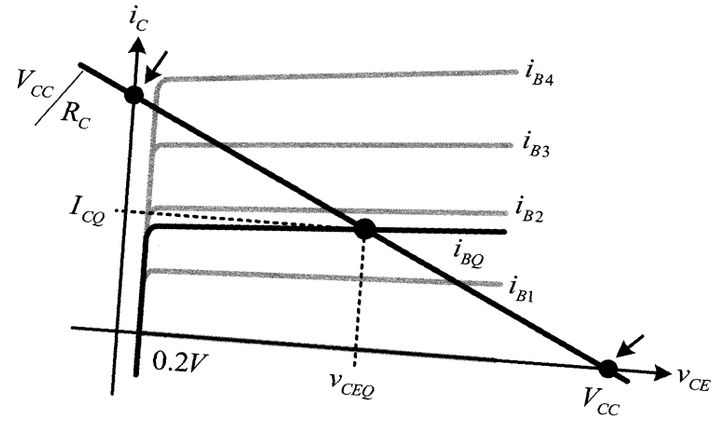
(1) i_B v.s. v_{BE}

(2) $V_{BB} = i_B R_B + v_{BE}$



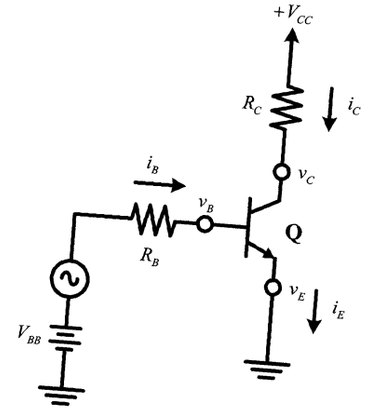
(3) i_C v.s. v_{CE}

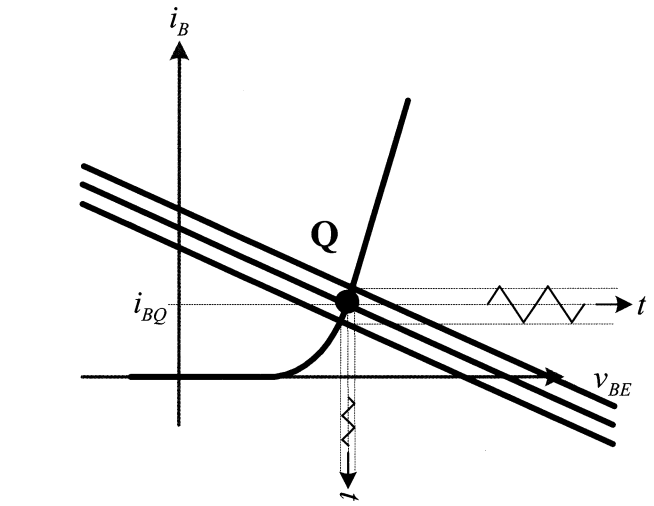
(4) $V_{CC} = i_C R_C + v_{CE}$ (Load Line)

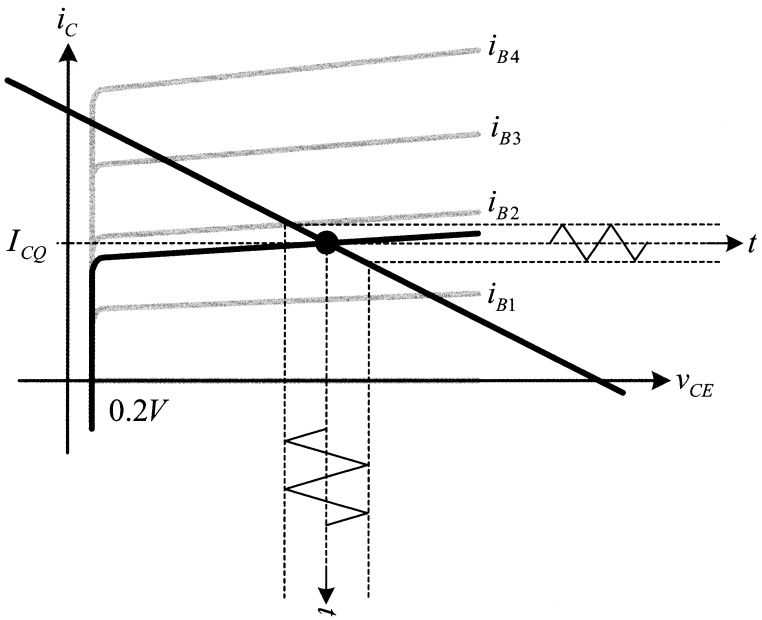


Example：(AC analysis)

當有訊號輸入時，使用圖解法解之。電晶體特性如同前 example。







$$\Delta i_C = \beta \cdot \Delta i_B$$

Q 點位置要適中，避免有訊號時，進入 saturation region 或 cut-off region！
藉由適當的偏壓電路，使 Q 點選擇在 active region 中間的區域最好。

2.7 BJT Circuits at DC

在此 section，會使用簡化的計算方法，不使用圖解的精確解法。
不需要畫大訊號等效模型。
假設：

(1) $V_{BE(on)} = 0.7V$ ，constant voltage drop model。

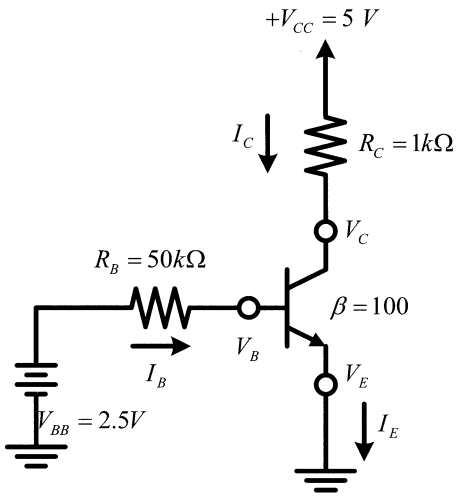
(2) $V_{CE,sat} = 0.2V$

(3) β 知

(4) 其他：$r_o \to \infty$ $(V_A \to \infty)$ ➔ $I_C = \beta \cdot I_B$

(5) $I_{CBO} = 0$ ； $I_{CEO} = 0$

Example 1 :



求出此電路在 DC 時的特性：I_B，I_C，I_E，V_B，V_C，V_E。

(note: R_B 通常很大，使 I_B 不至於太大，而致電晶體進入飽和區)

➔想辦法設計適當偏壓電路，使 I_{CEQ} 以及 V_{CEQ} 落在適當的偏壓點！

Sol:

(1) $V_E = 0V$

(2) $V_B = 0 + 0.7V = 0.7V$

(3) $I_B = \dfrac{2.5V - 0.7V}{50k\Omega} = 0.036mA$

設電晶體 active region

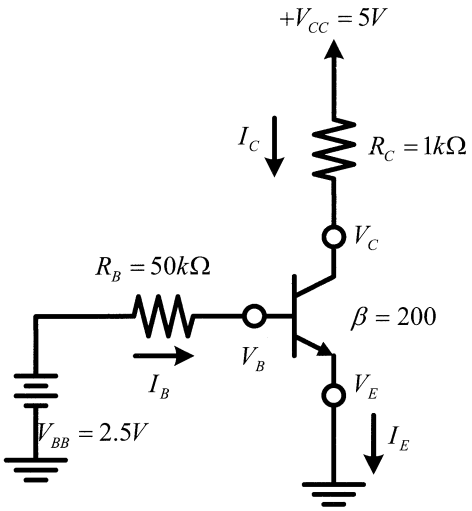
(4) $I_C = \beta \cdot I_B = 100 \times 0.036mA = 3.6mA$

(5) $V_C = 5 - 3.6mA \times 1k\Omega = 1.4V$

$(> V_B = 0.7V$ ➔ reverse biasing ➔ 假設成立)

(6) $I_E = I_B + I_C = 3.636mA$

Example 2 :



若上述例子之β由 100 改變為 200，
求出此電路在 DC 時的特性：I_B，I_C，I_E，
V_B，V_C，V_E。

Sol:

(1) $V_E = 0V$

(2) $V_B = 0 + 0.7V = 0.7V$

(3) $I_B = \dfrac{2.5V - 0.7V}{50k\Omega} = 0.036mA$

設電晶體 active region

(4-a) $I_C = \beta \cdot I_B = 200 \times 0.036mA = 7.2mA$

(5-a) $V_C = 5 - 7.2mA \times 1k\Omega = -2.2V$ (不合理)

($< V_B = 0.7V$ ➔ forward biasing ➔ 假設不成立)

故知電晶體工作在 saturation region

(4-b) $V_C = V_E + V_{CE,sat} = 0V + 0.2V = 0.2V$

(5-b) $I_C = \dfrac{5V - 0.2V}{1k\Omega} = 4.8mA$

(6) $I_E = I_B + I_C = 0.036mA + 4.8mA = 4.836mA$

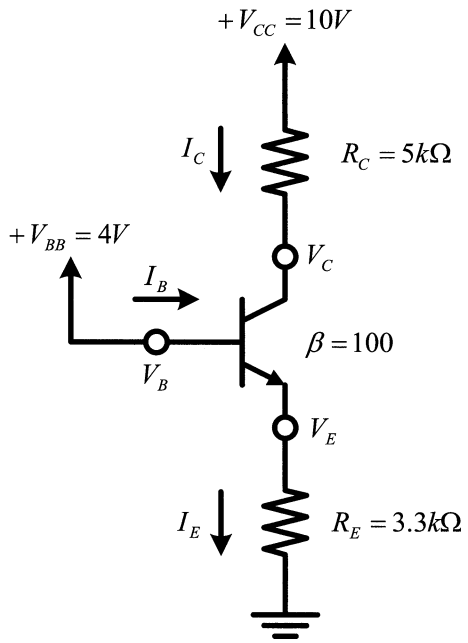
Discussion:

從偏壓電路設計的角度來看：

此種偏壓電路，工作點(Q)隨β值的變化很不穩定，為一 Bad biasing design。但是，voltage gain 應該不錯。(小小的變化，輸出端有大幅度的變化)。

此電路可適用於數位電路。

Example 3 :



求出此電路在 DC 時的特性：I_B，I_C，I_E，V_B，V_C，V_E。

$I_C \uparrow \Rightarrow V_E \uparrow \Rightarrow V_{BE} \downarrow \Rightarrow I_C \downarrow$

Re：emitter degeneration resistance

Sol:

(1) $V_B = 4V$

(2) $V_E = 4V - 0.7V = 3.3V$

(3) $I_E = \dfrac{3.3V}{3.3k\Omega} = 1mA$

假設此電晶體工作在 active region。

$$\alpha = \frac{\beta}{\beta+1} = \frac{100}{101} = 0.99$$

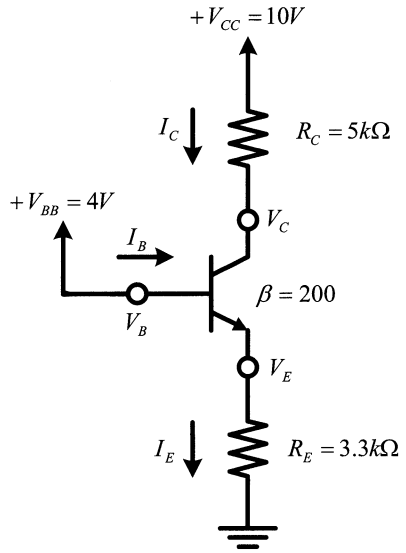
(4) $I_C = \alpha I_E = \dfrac{100}{101} \times 1mA = 0.99mA$

(5) $I_B = 1mA - 0.99mA = 0.01mA$

(6) $V_C = V_{CC} - I_C R_C = 10V - 0.99mA \times 5k\Omega = 5.V$

$V_C = 5V > V_B = 4V$ ➔ CBJ 為 reverse bias ➔ OK!

Example 4 :



若 β 由 100 增為 200，求出此電路在 DC 時的特性：I_B，I_C，I_E，V_B，V_C，V_E。

Sol:

(1) $V_B = 4V$

(2) $V_E = 4V - 0.7V = 3.3V$

(3) $I_E = \dfrac{3.3V}{3.3k\Omega} = 1mA$

假設此電晶體工作在 active region。

$$\alpha = \frac{\beta}{\beta+1} = \frac{200}{201} = 0.995$$

(4) $I_C = \alpha I_E = \dfrac{200}{201} \times 1mA = 0.995mA$

(5) $I_B = 1mA - 0.995mA = 0.005mA$

(6) $V_C = V_{CC} - I_C R_C = 10V - 0.995mA \times 5k\Omega = 5V$

$V_C = 5V > V_B = 4V$ ➔ CBJ 為 reverse bias ➔ OK!

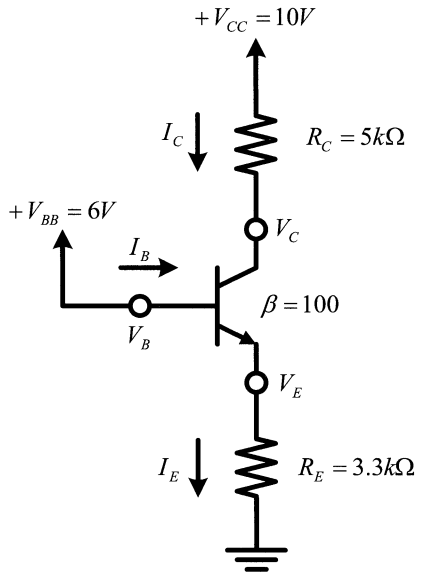
Discussion:

β 加倍了，但是偏壓點並沒有改變太大，除了 I_B 變化的百分比稍大，因此，這樣具有 R_E 電阻的電路其 Q 點非常的穩定。

➔ 對偏壓電路來說，這是一個 good bias design!

➔ 但是，不大能指望有好的 voltage gain (A_V)，voltage gain 被 R_E 給壓抑。

Example 5 :



若 V_{BB} 由 $4V$ 增為 $6V$ ，求出此電路在 DC 時的特性：I_B，I_C，I_E，V_B，V_C，V_E 。

Sol:

(1) $V_B=6V$

(2) $V_E=6V-0.7V=5.3V$

(3) $I_E=\dfrac{5.3V}{3.3k\Omega}=1.6mA$

假設此電晶體工作在 active region：

$$\alpha=\frac{\beta}{\beta+1}=\frac{100}{101}=0.99$$

(4) $I_C=\alpha I_E=\dfrac{100}{101}\times 1.6mA=1.59mA$

(5) $I_B=1.6mA-1.59mA=0.01mA$

(6) $V_C=V_{CC}-I_CR_C=10V-1.59mA\times 5k\Omega\approx 2V$

$V_C=2V<V_B=6V$ ➔ CBJ 為 forward bias ➔ 假設錯誤！

假設此電晶體工作在 saturation region，V_{BE} 仍設為 $0.7V$ ：

(1) $V_B=6V$

(2) $V_E=6V-0.7V=5.3V$ (同前)

(3) $I_E=\dfrac{5.3V}{3.3k\Omega}=1.6mA$ (同前)

(4) $V_C=V_E+V_{CE,sat}=5.3V+0.2V=5.5V$ $(>2\ V)$

(5) $I_C=\dfrac{10V-5.5V}{5k\Omega}=0.9mA$ $(<1.59mA)$

(6) $I_B=1.6mA-0.9mA=0.7mA$ $(>0.01mA)$

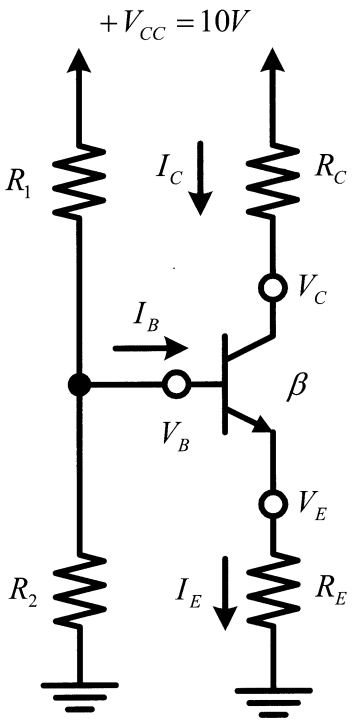
2.8 Biasing in BJT Amplifier Circuits

透過偏壓電路的適當設計，建立電晶體的 Biasing Point (Q)，使其偏壓位置適中，並且穩定。

如此電晶體操作時，不會進入 cut-off region 以及 saturation region，而能夠維持在 active region。

(在 cut-off region 以及 saturation region 中，電晶體沒有放大的功用)

Example:



求出此電路在 DC 時的特性：I_B，I_C，I_E，V_B，V_C，V_E。

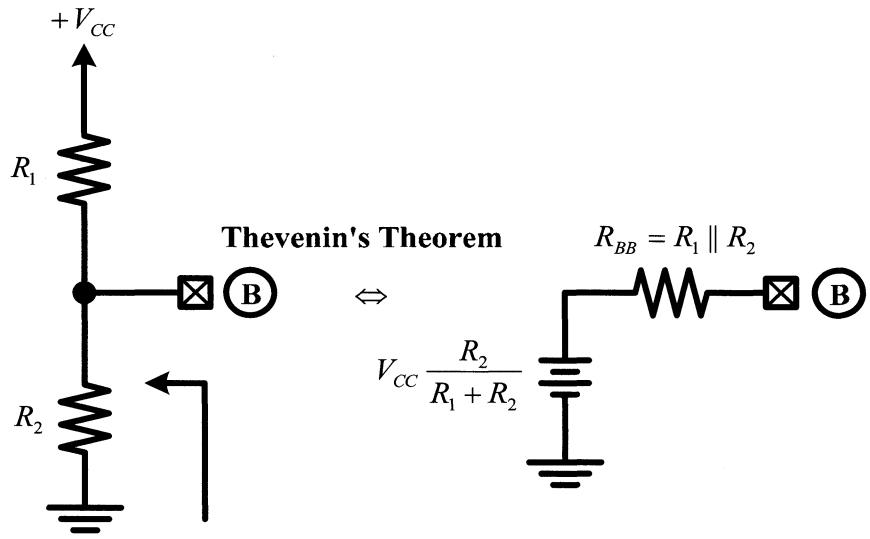
(note: 此為典型的應用在 discrete BJT 的偏壓電路)

$I_C \uparrow (I_E \uparrow) \rightarrow V_E \uparrow \rightarrow (V_B - V_E) = V_{BE} \downarrow \rightarrow I_C \downarrow (I_E \downarrow) \rightarrow \ldots$

➔ 工作點(Q)穩定！(due to R_E)

(有些電路，有可能發生以下的情況：$I_C \uparrow \rightarrow T \uparrow \rightarrow I_C \uparrow \rightarrow$ thermal runaway)

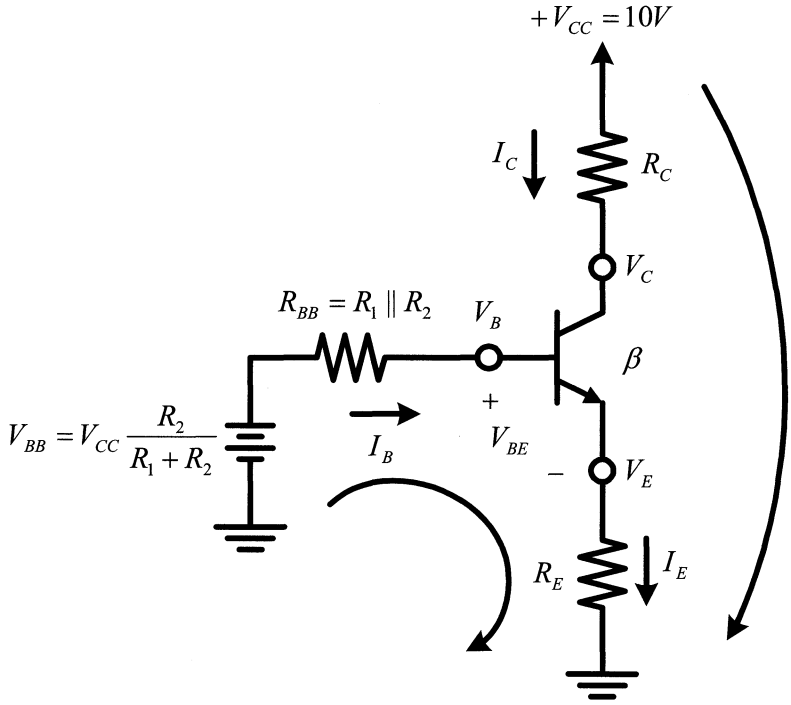
Sol:



(任意網路的化簡：求出 Open circuit voltage (V_{open}), short circuit current (I_{short})

➔ 等效的電阻為 V_{open}/I_{short})

➔ 將原電路，利用 Thevenin's Theorem 化簡：



假設電晶體 Q 工作在 **active region**：

(1) $V_{BB} = I_B R_B + V_{BE} + I_E R_E \quad (V_{BE} = 0.7V)$

(2) $I_B = \dfrac{I_E}{\beta + 1}$

∴可以解出 I_B 以及 I_E ➔ 然後即可解得剩下的工作點。

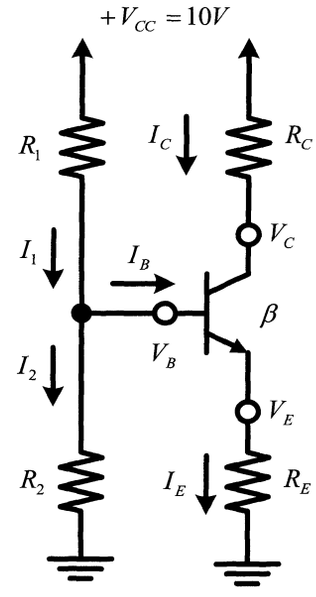
➔ $I_B = \dfrac{V_{BB} - V_{BE}}{R_{BB} + (\beta+1)R_E}$

$I_E = (\beta+1)I_B = \dfrac{V_{BB} - V_{BE}}{R_{BB} + (\beta+1)R_E}(\beta+1) = \dfrac{V_{BB} - V_{BE}}{R_E + \dfrac{R_{BB}}{(\beta+1)}}$

➔ (觀念：從 base 端看，R_E 被放大 $(\beta+1)$ 倍，因為電流 $I_E = (\beta+1)I_B$)
(意即 emitter 端的電阻，反射到 base 端)

➔ (觀念：從 emitter 端看，R_{BB} 被縮小 $(\beta+1)$ 倍，因為電流 $I_B = I_E / (\beta+1)$)
(意即 base 端的電阻，反射到 emitter 端)

➔ (觀念：以上的觀念稱為『電阻反射』的概念，僅使用在 **active region**。)



$I_B = \dfrac{V_{BB} - V_{BE}}{R_{BB} + (\beta+1)R_E}$ $\quad$ $I_E = \dfrac{V_{BB} - V_{BE}}{R_E + \dfrac{R_{BB}}{(\beta+1)}}$

Where $\begin{cases} V_{BB} \equiv V_{CC} \times \dfrac{R_2}{R_1 + R_2} \\ R_{BB} = R_1 \parallel R_2 \end{cases}$

$I_C = \alpha I_E \approx I_E = \dfrac{V_{BB} - V_{BE}}{R_E + \dfrac{R_{BB}}{(\beta+1)}}$

其中，$V_{BE}(T)$ 以及 $\beta(T)$ 是溫度的函數，為了減小溫度變化對工作點的影響

➔ (1) $V_{BB} >> V_{BE}(T)$ ➔ $R_1 << R_2$ ➔ 但：$(I_C R_C + V_{CB})\downarrow$ ➔ $V_{CB}\downarrow$

又 $V_{CB}=V_{CE}-V_{BE}=V_{CE}-0.7V$ ➔ $V_{CE}\downarrow$ ➔表 Q 點很接近飽和區

雖然工作點穩定，但是 Q 點不適合！

➔ 因此，<u>不適合</u>取 $R_1 << R_2$ ！

(2) $\dfrac{R_{BB}}{\beta(T)+1} << R_E$ ➔ $R_{BB}\downarrow$ ➔ $R_1, R_2\downarrow$ 但小的 R_1, R_2 會使 $I_1, I_2\uparrow$

➔ $\begin{cases} P_D\uparrow \\ R_{in}\downarrow \end{cases}$

➔ 一般而言，R_1, R_2 會取大電阻以降低功率的消耗！！

<u>折衷的設計取法：(經驗式子)</u>

$$\Delta V_{R_C}\approx\frac{1}{3}V_{CC},\quad V_{CB}\approx\frac{1}{3}V_{CC},\quad \left(V_{BE}+\Delta V_{R_E}\right)\approx\frac{1}{3}V_{CC}$$

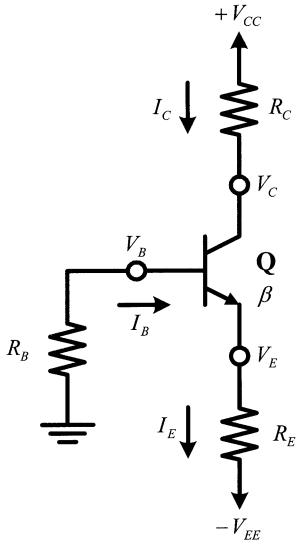
➔ $V_B\approx\dfrac{1}{3}V_{CC},\quad V_{CB}\approx\dfrac{1}{3}V_{CC},\quad I_C R_C\approx\dfrac{1}{3}V_{CC}$

$\Delta V_{R_1}=I_C R_C+V_{CB}\approx\dfrac{2}{3}V_{CC},\quad \Delta V_{R_2}\approx\dfrac{1}{3}V_{CC}$

➔ $\dfrac{R_1}{R_2}\approx\dfrac{2}{1}$ (哪一種數量級？？ Ω？ kΩ？ MΩ？)

➔ 經驗式所取的 R_1, R_2 之數量級，使 $I_1, I_2\approx 0.1I_E\sim I_E$!!

Example:



求出此電路在 DC 時的特性：I_B，I_C，I_E，V_B，V_C，V_E。

(note: 亦為典型的應用在 discrete BJT 的偏壓電路) (兩組 power supply)

Sol:

(直接運用『電阻反射』的概念解此電路)

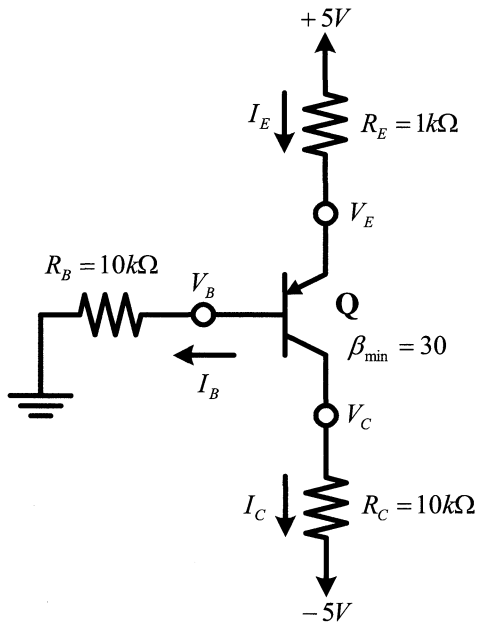
設此電晶體 Q 操作在 active region

$$I_E = \frac{0 - V_{BE} - (-V_{EE})}{\frac{R_B}{(\beta+1)} + R_E}$$

$$I_C \approx I_E = \frac{V_{EE} - V_{BE}}{\frac{R_B}{(\beta+1)} + R_E}$$

Example:

求出此電路在 DC 時的特性：I_B，I_C，I_E，V_B，V_C，V_E。



(note: 亦為典型的應用在 discrete BJT 的偏壓電路) (兩組 power supply)

Sol:

(直接運用『電阻反射』的概念解此電路)

設此 pnp 電晶體 Q 操作在 active region

$V_{EB} = 0.7V$

$$I_E = \frac{5V - 0.7V}{1k\Omega + \frac{10k\Omega}{(30+1)}} = 3.3mA$$

$$I_C = I_E \times \left(\frac{\beta}{\beta+1}\right) \approx 3.3mA$$

➔ $V_C = -5V + 3.3mA \times 10k\Omega = 28V$ ➔ 不合理!! CBJ 順偏!!

(R_B 太小導致 I_B 太大而進入 saturation region)

顯然，此 pnp 電晶體 Q 操作在 saturation region ➔ 電阻反射不能使用!!

$V_{EB} = 0.7V$，$V_{EC,sat} = 0.7V - 0.5V = 0.2V$

$I_E = I_B + I_C$

(1) $\dfrac{5V - V_E}{1k\Omega} = \dfrac{V_B}{10k\Omega} + \dfrac{V_C - (-5)}{10k\Omega}$

(2) $V_E = V_B + 0.7V$

(3) $V_C = V_B + 0.5V$

➔ V_B (可一一解出)

V_E (可一一解出)

V_C (可一一解出)

I_E (可一一解出)

$I_C = 0.86mA$

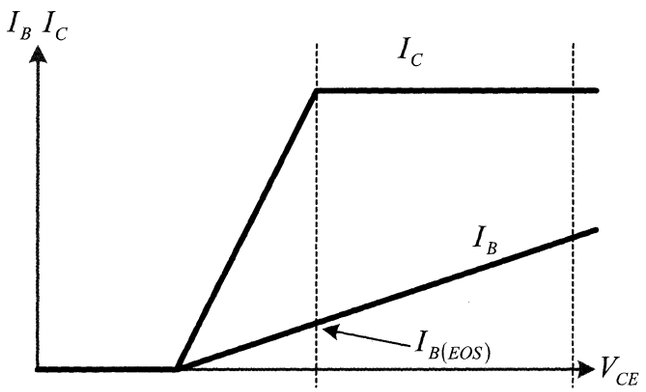
$I_B = 0.31mA$

$\beta_{\min}$ 的用意在求得 overdrive factor $\equiv \dfrac{\beta}{\beta_{forced}}$

$\beta_{force} \equiv \dfrac{I_{C,sat}}{I_B} = \dfrac{0.86mA}{0.31mA} = 2.8 \quad < \beta_{\min} = 30$ (in saturation region)

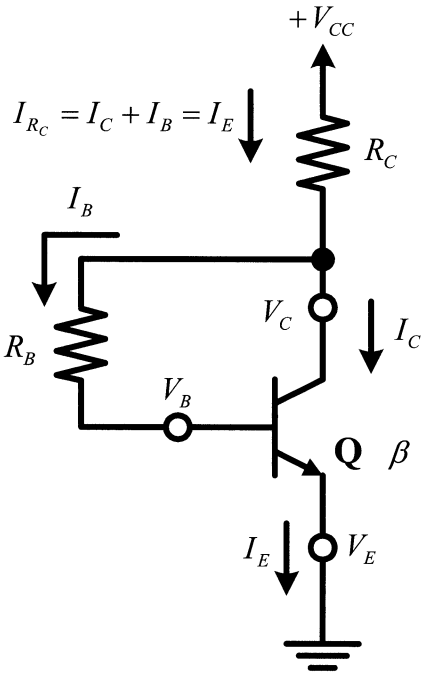
$\dfrac{\beta_{\min}}{\beta_{force}} = \dfrac{30}{2.8} \approx 10$ ➔ 很深的 saturation

(overdrive factor $\equiv \dfrac{\beta}{\beta_{forced}} = \dfrac{I_B}{I_{B(EOS)}}$)



Example:

求出此電路在 DC 時的特性：I_B，I_C，I_E，V_B，V_C，V_E。



(note: 亦為典型的應用在 discrete BJT 的偏壓電路)

Sol:

EBJ ➔ 一定順偏　　CBJ ➔ 一定逆偏

➔ 此電晶體 Q <u>必然操作在 **active region**</u>

若 $I_E\uparrow$ ➔ $V_C\downarrow$ ➔ $I_B=\dfrac{V_C-0.7}{R_B}\downarrow$ ➔ $\begin{cases} I_C=\beta\cdot I_B\Rightarrow\downarrow \\ I_E=(\beta+1)\cdot I_B\Rightarrow\downarrow \end{cases}$ 偏壓穩定

(negative feedback, 負回授)　R_B 用來當作負回授用的電阻。

➔ 可不用 R_E 就可以使偏壓點穩定。

$$V_{CC}=I_{R_C}\cdot R_C+I_B\cdot R_B+V_{BE}=I_E\cdot R_C+I_B\cdot R_B+V_{BE}$$

$$I_E=I_B(\beta+1)$$

➔ $$V_{CC}=I_E R_C+\frac{I_E}{(\beta+1)}R_B+V_{BE}$$

➔ $$I_C\approx I_E=\frac{V_{CC}-V_{BE}}{R_C+\dfrac{R_B}{(\beta+1)}}$$　(其中，$V_{BE}(T)$ 且 $\beta(T)$)

為了使偏壓電流 I_C 不受溫度變化而有大的改變，

➔ (1) $V_{CC}>>V_{BE}(T)$ ➔ 需要折衷考量

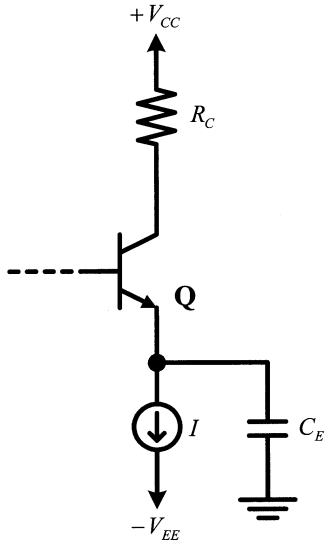
(2) $\dfrac{R_B}{(\beta+1)}<<R_C$ ➔ 需要折衷考量

此種電路在設計偏壓電路時，電壓的經驗取法為：

取 $V_{CB} \approx \frac{1}{2} V_{CC}$

$V_{CB}\uparrow$ ➔ $V_{CE}\uparrow$ ➔ 可使所選的 Q 點較靠 active region 的中間區域。

Example:



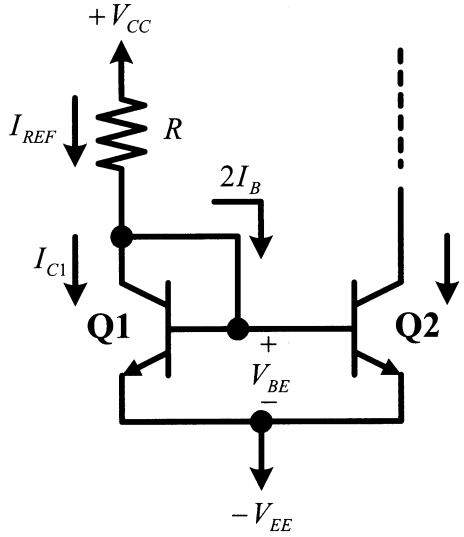
C_E : bypass capacitor

如何讓 I_C 穩定？ ➔ 製作一個等流電源(constant current source)來偏壓！

(note: 亦為應用在 Integrated Circuit 中應用常見的偏壓電路)

Sol:

如何 constant current source (current mirror) ??



(1) $Q1 = Q2$ (matched) ➔ $\begin{cases} \beta_1 = \beta_2 = \beta \\ I_{S1} = I_{S2} = I_S \end{cases}$

(2) $V_{BE1} = V_{BE2} = V_{BE}$

假設: (a) $\beta >> 1$ ➔ $I_B \to 0$

(b) $V_A >> 1$ ➔ r_o high

➔ i_C 和 v_{CE} 無關➔ neglect Early effect

$Q1$ 必為 active; 若 $Q2$ 為 active

在以上的假設下， $I_{C2} = I_{C1} = I_{REF}$

$$I_{C2} = I_{C1} = I_{REF} = \frac{+V_{CC} - (-V_{EE}) - V_{BE}}{R} = \frac{V_{CC} + V_{EE} - V_{BE}}{R}$$

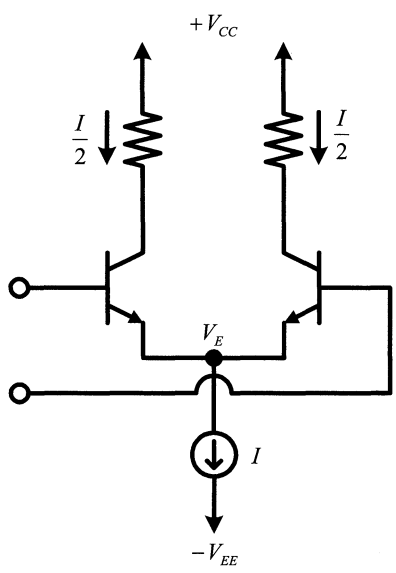
: constant current source 可以實現出來！

為何在 discrete 的 BJT 應用中不用此電路？

➔ 很難挑出兩個一模一樣(matched)的電晶體。

在 IC 當中製作電容 C_E 會很耗面積，別種方法解決？

➔ 使用 differential amplifier。

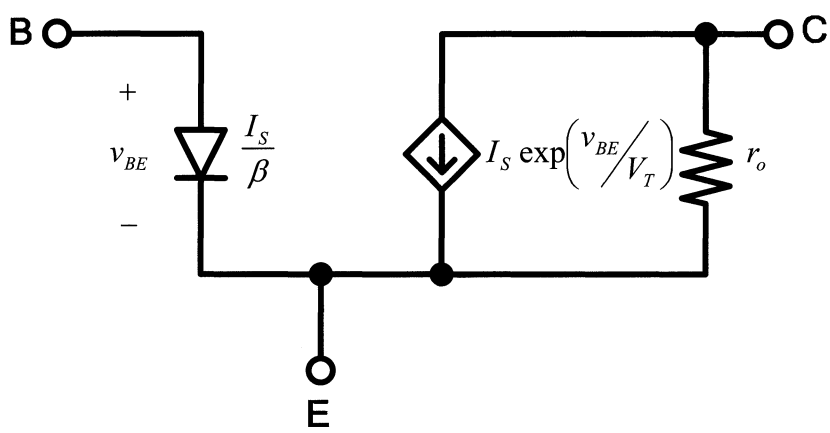


➔在 ac 訊號分析時，V_E 點等效為 ac 接地，而不需使用 C_E ！

2.9 Small-Signal Operation and Models

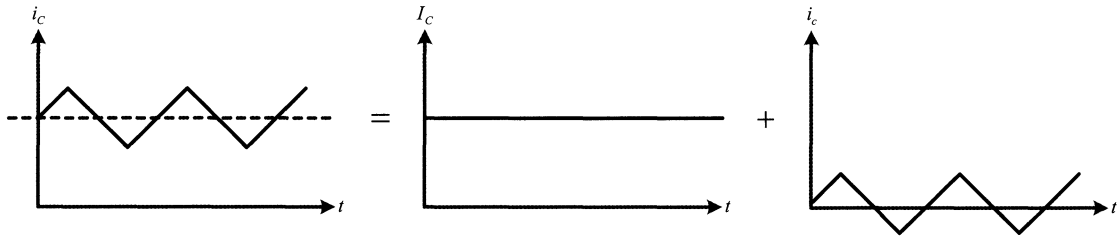
小訊號的 level 要多小，才能夠適用於 BJT 小訊號模型分析？
BJT 小訊號的電路模型為何？

Review:
BJT 的 Large-Signal Models：



每一個電壓或電流訊號，皆包含直流成分＋訊號成分

$$i_B = I_B + i_b \qquad v_{BE} = V_{BE} + v_{be}$$
$$i_C = I_C + i_c \qquad v_{CE} = V_{CE} + v_{ce}$$
$$i_E = I_E + i_e$$



$$i_C = I_S \exp\left(\frac{v_{BE}}{V_T}\right)$$

➔ $$I_C + i_c = I_S \exp\left(\frac{V_{BE} + v_{be}}{V_T}\right) = I_s \exp\left(\frac{V_{BE}}{V_T}\right) \cdot \exp\left(\frac{v_{be}}{V_T}\right)$$

若 $v_{be} << V_T$

➔ $I_C + i_c \approx I_S \exp\left(\frac{V_{BE}}{V_T}\right) \cdot \left(1 + \frac{v_{be}}{V_T}\right)$

➔ $i_c \approx I_C \cdot \left(\frac{v_{be}}{V_T}\right) = g_m v_{be}$

定義：$g_m \equiv \frac{i_c}{v_{be}} = \frac{I_C}{V_T}$ (mutual conductance 或 transconductance)

$$\left(g_m \equiv \left.\frac{\partial i_C}{\partial v_{BE}}\right|_{V_{BE}} = \left.\frac{\partial}{\partial v_{BE}}\left[I_S \exp\left(\frac{v_{BE}}{V_T}\right)\right]\right|_{V_{BE}} = \frac{I_C}{V_T}\right)$$

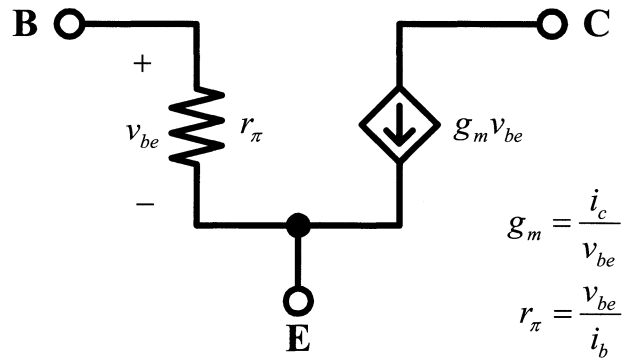
即當為小訊號$(v_{be} << V_T)$時，i_c 訊號與 v_{be} 訊號具有線性關係：$i_c = g_m v_{be}$

又由：$i_B = \frac{I_S}{\beta} \exp\left(\frac{v_{BE}}{V_T}\right)$

定義：Base resistance (基極輸入端電壓訊號與基極輸入電流訊號的比值)：

$$r_\pi \equiv \frac{\Delta v_{BE}}{\Delta i_B} = \frac{V_T}{I_B}$$

π-model (Hybrid-π model):



$$g_m = \frac{i_c}{v_{be}} = \frac{I_C}{V_T}$$

$$r_\pi = \frac{v_{be}}{i_b} = \frac{V_T}{I_B}$$

$$g_m \cdot r_\pi = \frac{I_C}{I_B} = \beta$$

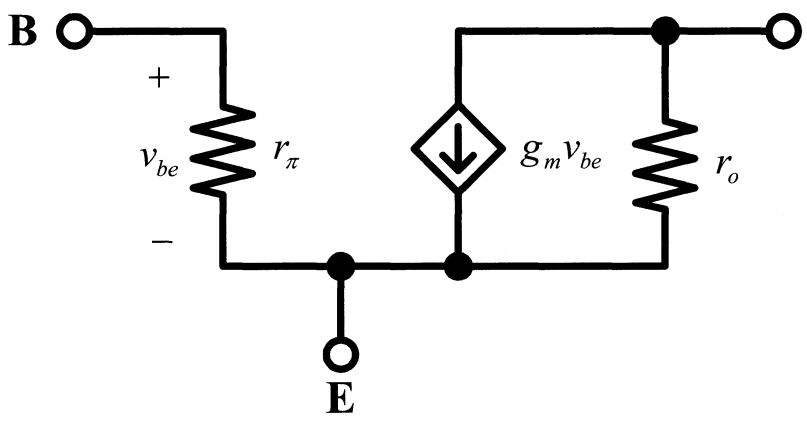
$$\begin{cases} g_m = \frac{i_c}{v_{be}} = \frac{I_C}{V_T} \\ r_\pi = \frac{v_{be}}{i_b} = \frac{V_T}{I_B} \\ g_m \cdot r_\pi = \frac{I_C}{I_B} = \beta \end{cases}$$

Analysis Procedure:

DC analysis ➔ I_C ➔ g_m ➔ $r_\pi\left(=\frac{\beta}{g_m}\right)$ ➔ ac analysis

考慮 **Early Effect**：

小訊號的 r_o 和大訊號的 r_o 同。因為 i_C 和 v_{CE} 特性為一條直線。



$$g_m = \frac{i_c}{v_{be}} = \frac{I_C}{V_T}$$

$$r_\pi = \frac{v_{be}}{i_b} = \frac{V_T}{I_B}$$

$$r_o = \frac{V_A}{I_C}$$

在 π-model 中，v_{be} 常表為 v_π。

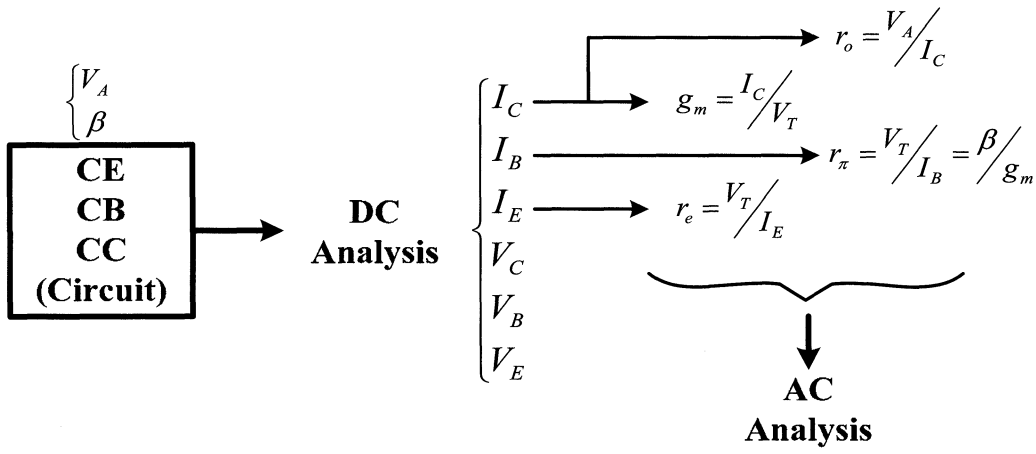
2.10 Single-Stage BJT Amplifiers

3 basic configurations:

CE (Common Emitter Configuration)

CB (Common Base Configuration)

CC (Common Collector Configuration) (Emitter Follower)



假設：

電晶體操作在 active region，且 Q 點位置恰當。

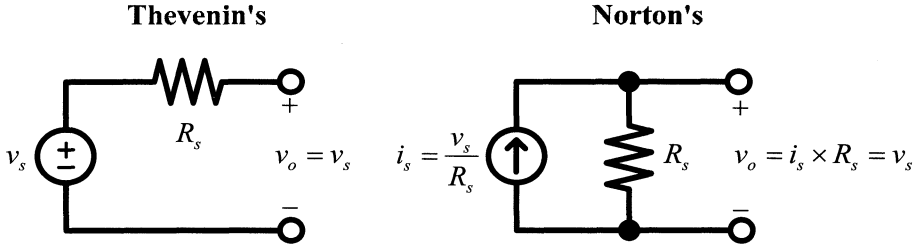
可以正確的當作放大器。

$v_{be} << V_T$ ➔ small-signal approximation

對此三種型態電路(CE、CB、CC)有興趣的基本參數特性： (考慮中低頻)

R_i, R_o, A_i, A_v (輸入阻抗、輸出阻抗、電流增益、電壓增益)

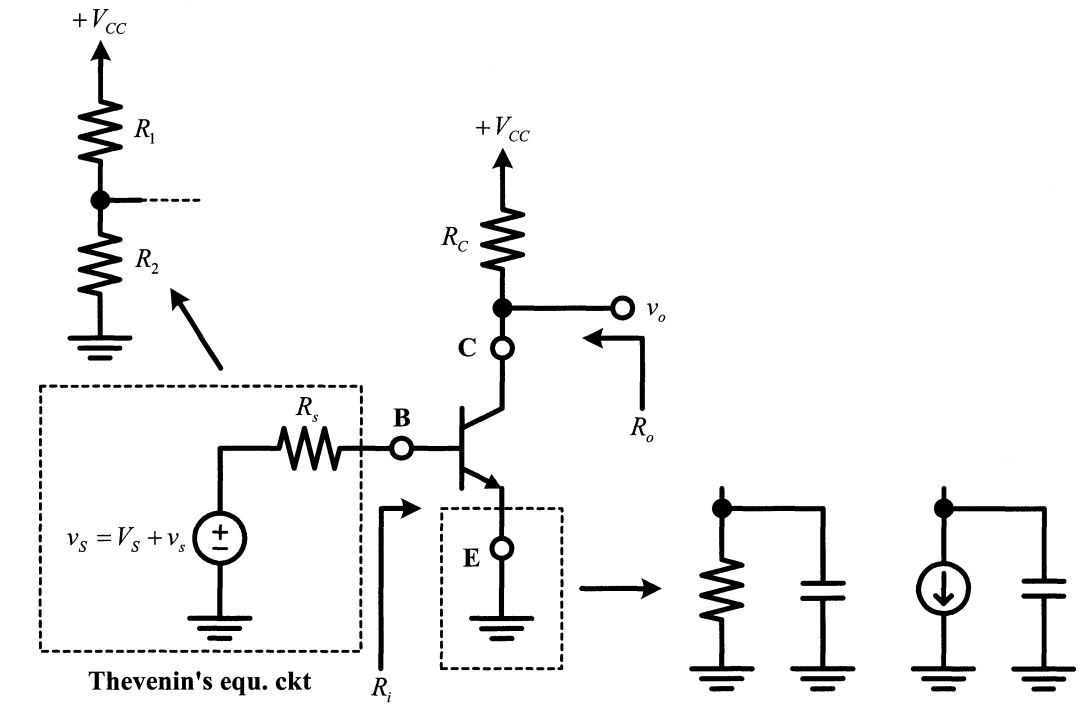
輸入訊號源的表示種類：



此兩種表示等效對應。

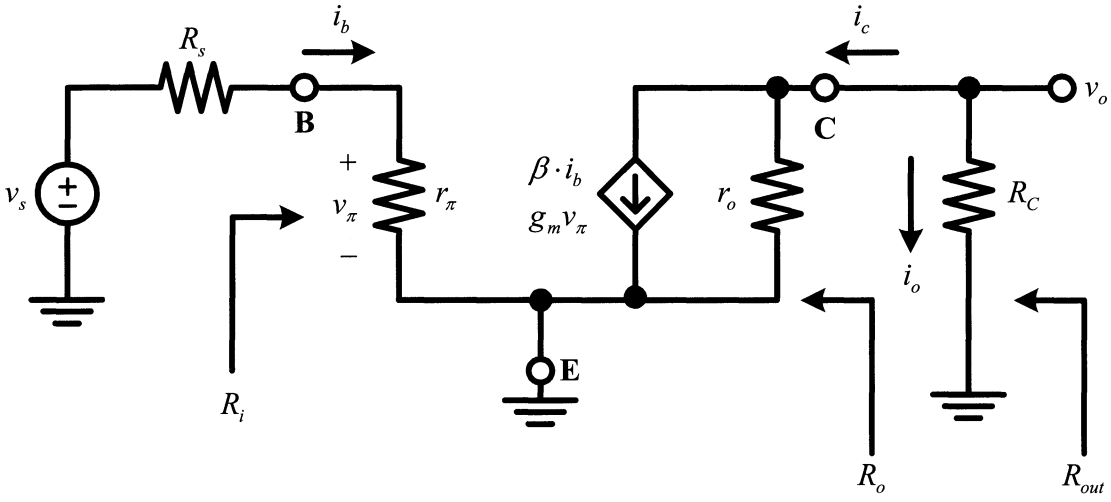
Common Emitter (CE) Amplifier :

假設 DC Analysis 已經完成，僅考慮訊號的部分。



計算：R_i，R_o，A_i，A_v

使用π-model 分析此電路：



(1) $R_i \equiv \dfrac{v_i}{i_i} = \dfrac{v_\pi}{i_b} = r_\pi$

(2) $A_i \equiv \dfrac{i_o}{i_i} = \dfrac{-i_c}{i_b} = -\dfrac{(\beta \cdot i_b) \times \dfrac{r_o}{r_o + R_C}}{i_b} = -\dfrac{\beta \cdot r_o}{r_o + R_C}$

Note: $r_o \to \infty$, $R_C \to 0$ ➔ $A_i \to \beta$

因此，正確的來說，在考慮 Early effect 之後(V_A, r_o)

β 更正確的說法，應為：common emitter **short circuit** current gain

(3) $A_v \equiv \dfrac{v_o}{v_s} = \dfrac{v_\pi}{v_s} \times \dfrac{v_o}{v_\pi} = \dfrac{r_\pi}{R_s + r_\pi} \times \dfrac{(-g_m v_\pi) \times (r_o \parallel R_C)}{v_\pi} = -g_m \cdot (r_o \parallel R_C) \cdot \dfrac{r_\pi}{R_s + r_\pi}$

$v_\pi = v_s \times \dfrac{r_\pi}{R_s + r_\pi}$

Note: 若 $r_o >> R_C$, $R_s << r_\pi$ ➔ $A_v \to (-g_m R_C)$

要 $A_v \uparrow$ ➔ $g_m \uparrow$ ➔ $I_C \uparrow$ ➔ 消耗功率

➔ $R_C \uparrow$ ➔ $V_{CC} \uparrow$ ➔ 消耗功率　　trade-off needed!

若 R_C 改用 active load，可增進 A_v，可大電流，但不需高 V_{CC}

$$\begin{cases} g_m r_\pi = \beta \\ g_m r_e = \alpha \end{cases}$$

$$\frac{v_c}{v_b} = -g_m (r_o \parallel R_C) = -\alpha \frac{(r_o \parallel R_C)}{r_e}$$

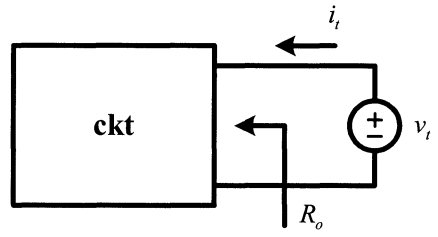
Note: $r_o \parallel R_C$: total resistance in collector terminal

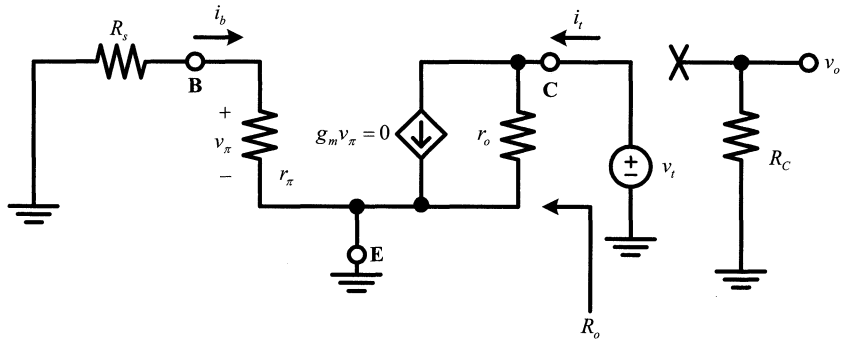
r_e : total resistance in emitter terminal

Voltage gain between base and collector $= -\alpha \times \dfrac{\text{total resistance in C}}{\text{total resistance in E}}$

(4) R_o ?

Set $v_S = 0$ and $i_S = 0$ (將獨立訊號源設為 0)





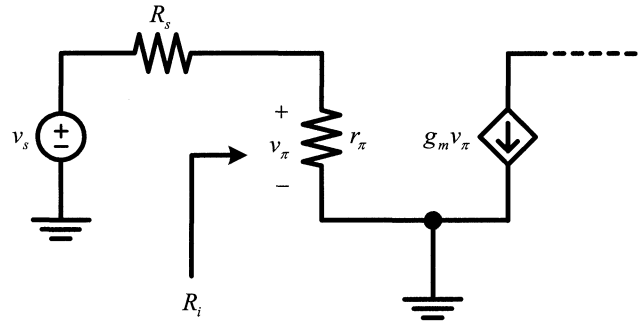
➔ $R_o = r_o$

➔ $R_{out} = (R_C \parallel R_o) = (r_o \parallel R_C)$

Discussions R_i:

考慮放大<u>電壓訊號</u> ➔ 使用 Thevenin's equivalent circuit

Target: $g_m v_\pi$



$$v_\pi = v_s \times \frac{r_\pi}{R_s + r_\pi}$$

$$R_i = r_\pi$$

$$v_\pi = v_s \times \frac{R_i}{R_s + R_i}$$

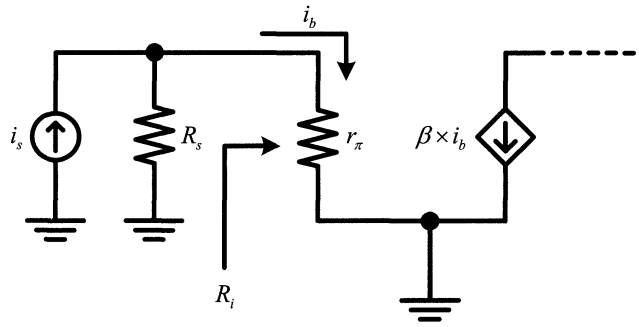
因此，若要將電壓訊號放大，則我們希望輸入電壓訊號的損耗越小越好!

➔ $R_s << R_i$

➔ R_i 越大越佳！

考慮放大<u>電流訊號</u> ➔ 使用 Norton's equivalent circuit

Target: $\beta \times i_b$



$$i_b = i_s \times \frac{R_s}{r_\pi + R_s}$$

$$R_i = r_\pi$$

$$i_b = i_s \times \frac{R_s}{R_s + R_i}$$

因此，若要將電流訊號放大，則我們希望輸入電流訊號的損耗越小越好!

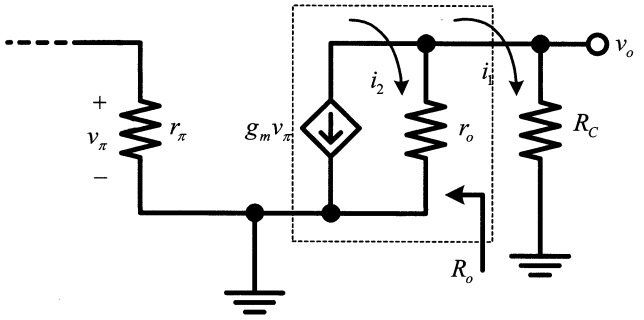
➔ $R_s >> R_i$

➔ R_i 越小越佳！

Discussions R_o :

考慮輸出為<u>電流</u>訊號 ➔ 使用 Norton's equivalent circuit

Target: i_1



$$i_1 = -g_m v_\pi \times \frac{r_o}{r_o + R_C}$$

$$R_o = r_o$$

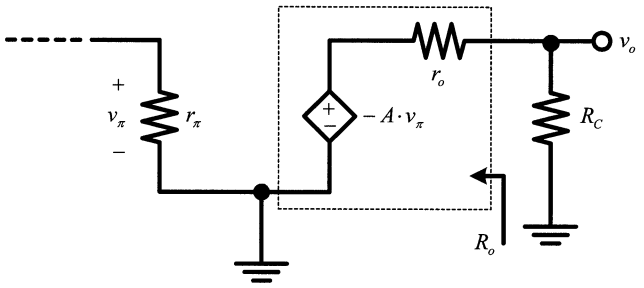
$$i_1 = -g_m v_\pi \times \frac{R_o}{R_o + R_C}$$

因此，若要將電流訊號放大，則希望輸出電流訊號的損耗越小越好! ➔ $R_o >> R_C$

➔ R_o 越大越佳！

考慮輸出為<u>電壓</u>訊號 ➔ 使用 Thevenin's equivalent circuit

Target: v_o



$$v_o = (-A \cdot v_\pi) \times \frac{R_C}{r_o + R_C}$$

$$R_o = r_o$$

$$v_o = (-A \cdot v_\pi) \times \frac{R_C}{R_o + R_C}$$

因此，若要將電壓訊號放大，則我們希望輸出電壓訊號的損耗越小越好!

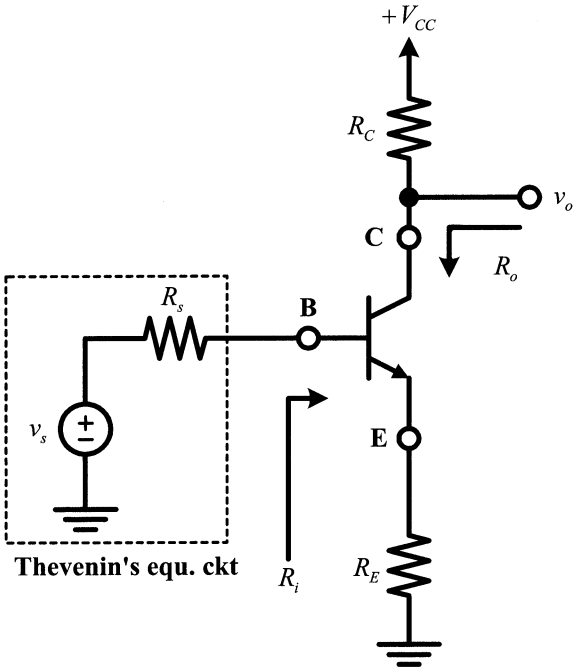
➔ $R_o << R_C$

➔ R_o 越小越佳！

➔ R_i 以及 R_o 之值所要設計的大小，和電路處理電流或電壓訊號的放大有關。

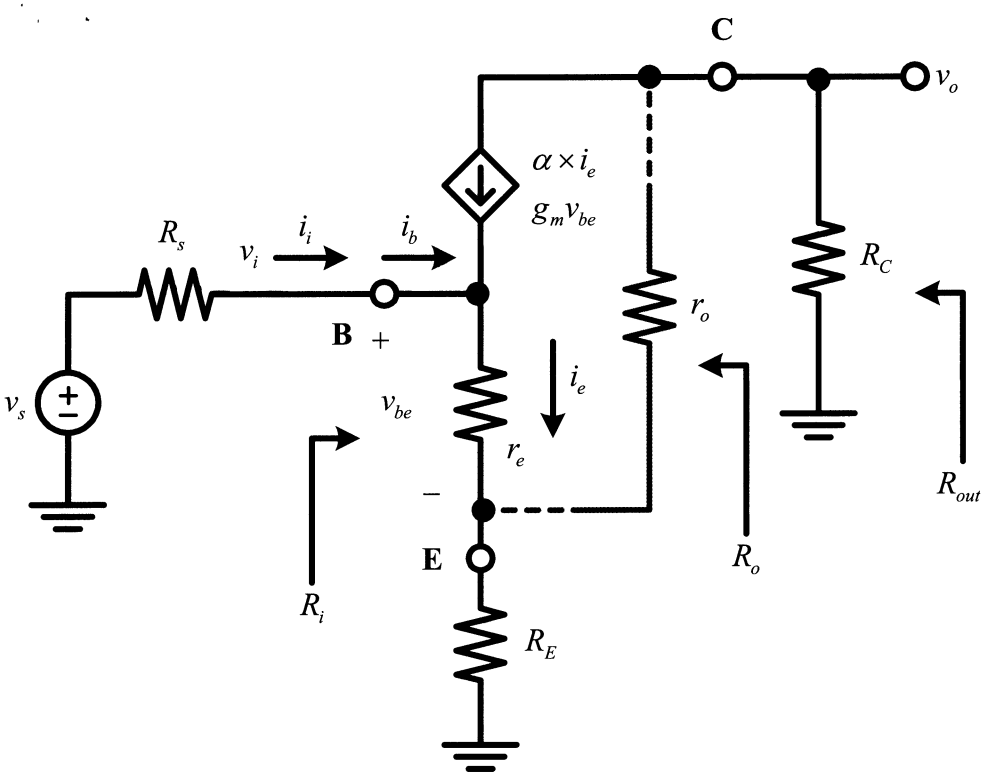
Common Emitter (CE) Amplifier with R_E :

假設 DC Analysis 已經完成，下面僅考慮訊號的部分。



求此放大器型態之: R_i, R_o, A_i, A_v

使用T-model 分析此電路：



假設: 略去 r_o 。($r_o \to \infty$ ，忽略 Early effect)

(合理的假設以簡化問題，但是會有誤差存在)

(1) 使用『電阻反射』的概念

$R_i = (\beta+1)\cdot(r_e + R_E)$

推導並證明此電阻反射的概念：

$$R_i \equiv \frac{v_i}{i_i} = \frac{i_e(r_e+R_E)}{i_b} = (\beta+1)\cdot(r_e+R_E)$$

Emitter 端加入 R_E 可大大提高輸入電阻！

(2) $$A_i \equiv \frac{i_o}{i_i} = \frac{-\beta \times i_b}{i_b} = -\beta$$

(3) $$A_v \equiv \frac{v_o}{v_s} = \frac{v_o}{v_i}\cdot\frac{v_i}{v_s} = \left(\frac{v_c}{v_b}\right)\times\left(\frac{v_i}{v_s}\right) = \left(-\alpha \times \frac{R_C}{r_e+R_E}\right)\times\left(\frac{R_i}{R_s+R_i}\right)$$

Review: Voltage gain between base and collector $= -\alpha \times \dfrac{\text{total resistance in C}}{\text{total resistance in E}}$

➔ $$A_v = \left[-\alpha \times \left(\frac{R_C}{r_e+R_E}\right)\right]\times\left[\frac{(\beta+1)\cdot(r_e+R_E)}{R_s+(\beta+1)\cdot(r_e+R_E)}\right]$$

➔ $$A_v = -\alpha\frac{(\beta+1)\cdot R_C}{R_s+(\beta+1)\cdot(r_e+R_E)}$$

Note: 加 R_E 使 voltage gain 壓低，

但是也使 β 的敏感度降低！ ← $(\beta+1)\cdot(r_e+R_E) >> R_s$

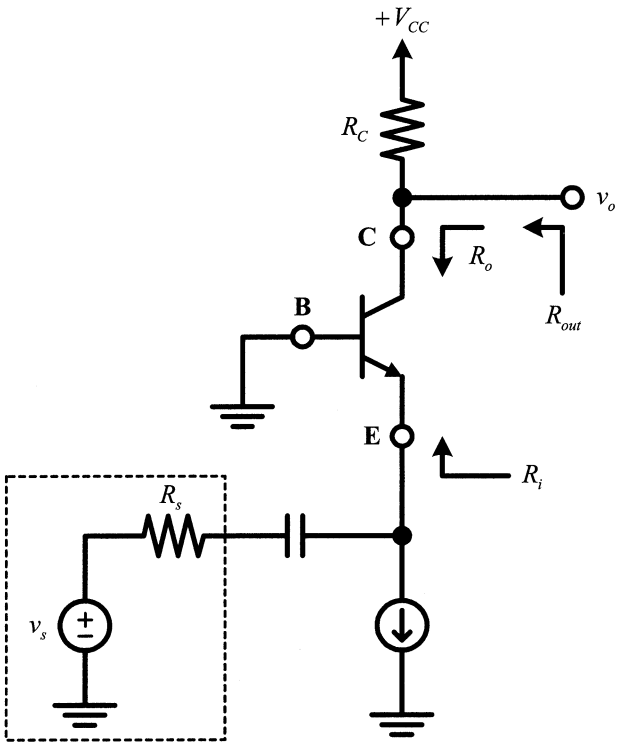
(4) $R_o = ??$

$R_o \to \infty$ （略去 r_o）

$R_{out} = (R_o \,||\, R_C) = R_C$

Common Base (CB) Amplifier:

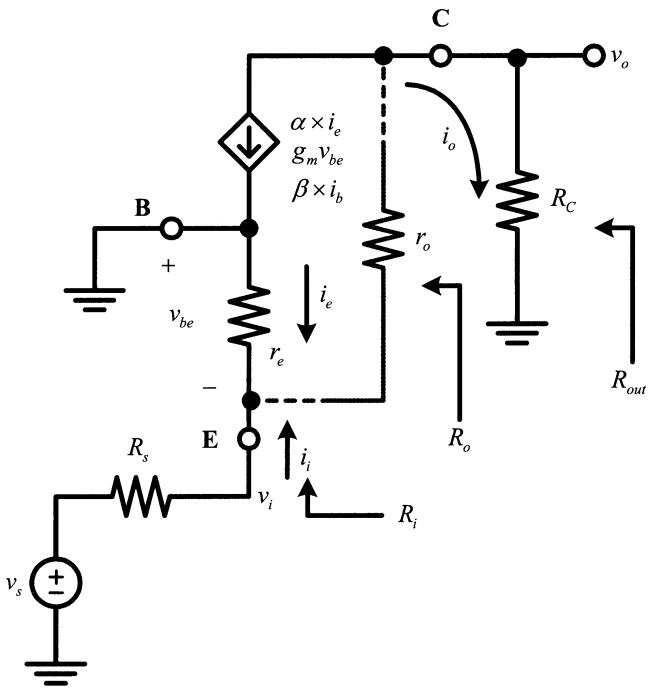
假設 DC Analysis 已經完成，僅考慮訊號的部分。



Thevenin's equ. ckt

求此放大器型態之: R_i, R_o, A_i, A_v

使用T-model 分析此電路：



假設: 略去 r_o。($r_o \to \infty$，忽略 Early effect)

(合理的假設以簡化問題，但是會有誤差存在)

(1) $R_i = r_e$ (很小)

(2) $A_i \equiv \frac{i_o}{i_i} = \frac{-\alpha \cdot i_e}{-i_e} = +\alpha \leq 1$

(3) $A_v \equiv \frac{v_o}{v_s} = \frac{(-\alpha \times i_e) \times R_C}{-i_e \times (r_e + R_s)} = \frac{\alpha \times R_C}{(r_e + R_s)}$

電壓增益仍大，

電壓增益對 β 變化的影響小，但是 **voltage gain "critically" depends on** R_s **!!**

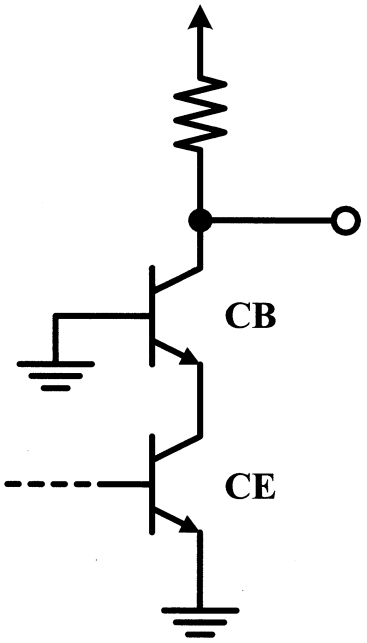
(4) $R_o \to \infty$

$R_{out} = (R_o \parallel R_C) = R_C$

Common Base 雖然有上述的缺點，但是 CB 的<u>高頻響應</u>是上述幾種放大器中最好的架構！

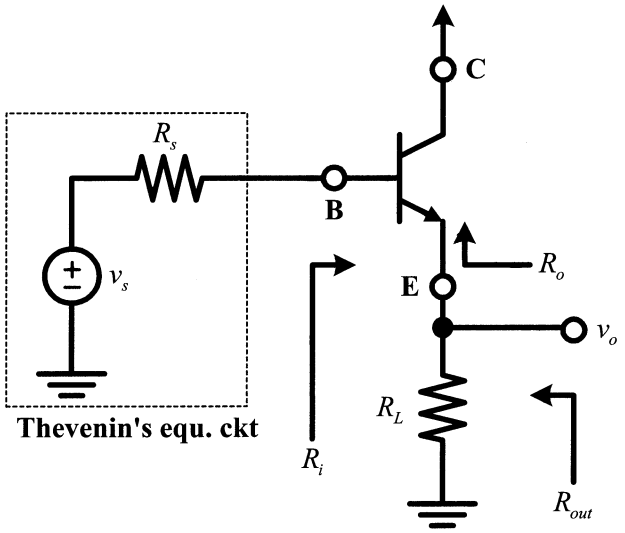
通常，Common Base 為和 Common Emitter 一起運用。如左圖 **<u>Cascode Amplifier</u>** 架構。

提高 amplifier 的頻寬！！



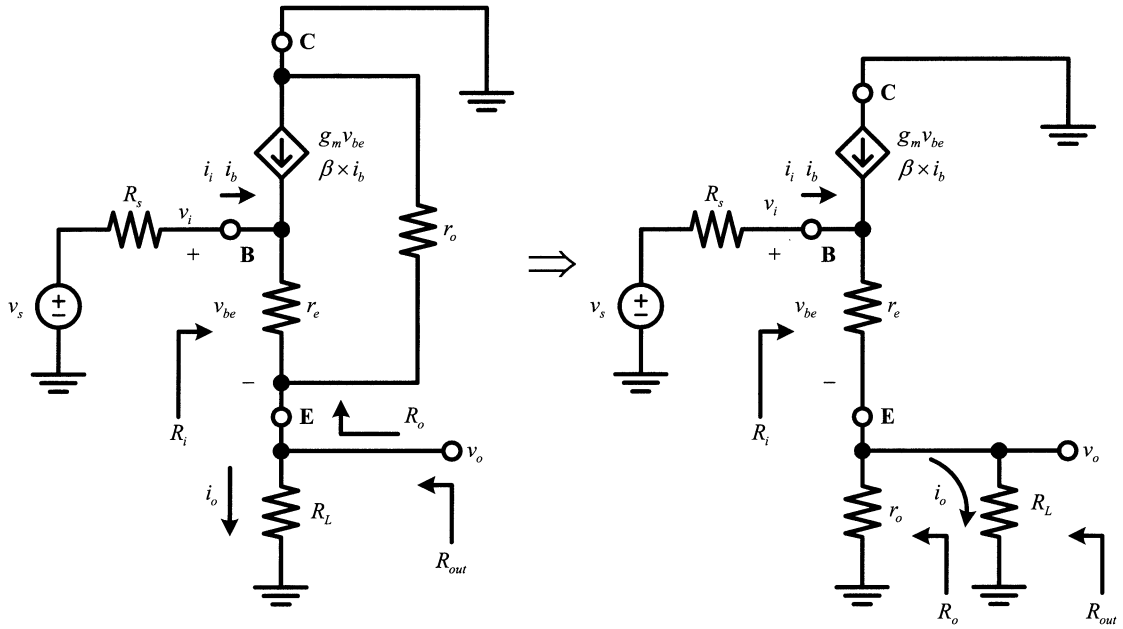
Common Collector (CC) Amplifier: (Emitter Follower)

假設 DC Analysis 已經完成，僅考慮訊號的部分。



求此放大器型態之: R_i, R_o, A_i, A_v

使用T-model 分析此電路：



(1) 利用『電阻反射』的概念

$$R_i = (\beta+1)\cdot(r_e + r_o \,\|\, R_L) \approx (\beta+1)\cdot R_L \quad (大) \qquad (r_o >> R_L >> r_e)$$

(2) $$A_i \equiv \frac{i_o}{i_i} = \frac{(\beta+1)\times i_b \times \dfrac{r_o}{r_o + R_L}}{i_b} = (\beta+1)\frac{r_o}{r_o + R_L} \approx (\beta+1) \quad (大)$$

(3) $$A_v \equiv \frac{v_o}{v_s} = \left(\frac{v_i}{v_s}\right) \times \left(\frac{v_o}{v_i}\right) = \left[\frac{v_s \times \left(\frac{R_i}{R_i + R_s}\right)}{v_s}\right] \times \left[\frac{v_i \times \left(\frac{r_o \parallel R_L}{r_e + r_o \parallel R_L}\right)}{v_i}\right]$$

➔ $$A_v = \frac{R_i}{R_i + R_s} \times \frac{r_o \parallel R_L}{r_e + r_o \parallel R_L} \approx \frac{(\beta+1)R_L}{R_s + (\beta+1)R_L} \times \frac{r_o \parallel R_L}{r_e + r_o \parallel R_L} \quad (<1)\cdot(<1) \Rightarrow <1$$

➔ $$A_v = \frac{(\beta+1) \times (r_o \parallel R_L)}{R_s + (\beta+1) \times [r_e + (r_o \parallel R_L)]} \quad <1 \quad (小)$$

➔or $$A_v = \frac{(r_o \parallel R_L)}{\frac{R_s}{(\beta+1)} + [r_e + (r_o \parallel R_L)]}$$

Discussions:

電壓增益雖然小於 1，但是

電壓增益對 β 變化的影響小。

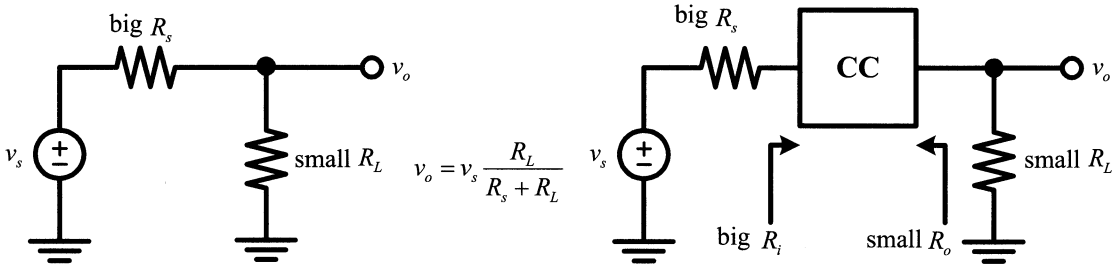
電壓增益對 R_s 變化的影響小。

(R_s 可視為前一級 amplifier 的輸出阻抗)

(4) 利用『電阻反射』的概念

$$R_o = \left[\frac{R_s}{(\beta+1)} + r_e\right] \parallel r_o \approx \left[\frac{R_s}{(\beta+1)} + r_e\right] \quad (小) \qquad r_o >> \left[\frac{R_s}{(\beta+1)} + r_e\right]$$

$$R_{out} = \left[\frac{R_s}{(\beta+1)} + r_e\right] \parallel r_o \parallel R_L \approx \left[\frac{R_s}{(\beta+1)} + r_e\right] \parallel R_L \qquad r_o >> \left[\frac{R_s}{(\beta+1)} + r_e\right]$$



若 R_S 大，R_L 小，

上圖左這種接法，R_S、R_L 不匹配，輸入訊號出不來，或衰減的很嚴重！

因此需要一個<u>緩衝級</u>，此緩衝級的特性需要：輸入電阻大，輸出電阻小!

➔ 使用 Common Collector amplifier 來當作緩衝級(buffer) ➔ 電路接法如上圖右。

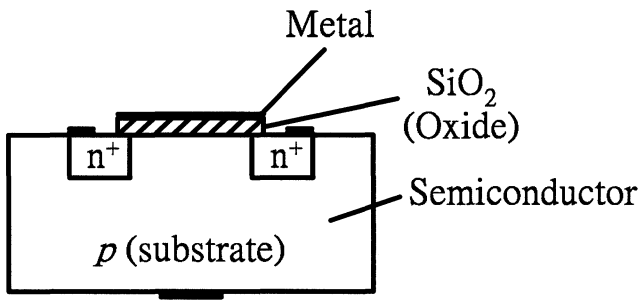
Discussions:

因為 common collector 具有高輸入阻抗，以及低輸出阻抗的特性，因此通常用做輸出級(output stage)，或緩衝器(buffer)使用！

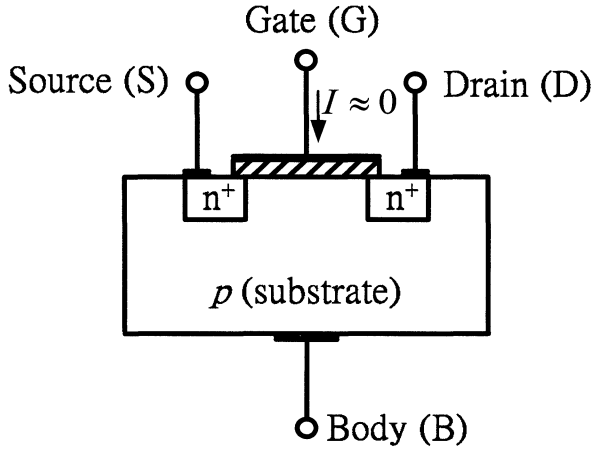
Chapter 3 MOS Field-Effect Transistors (MOSFETs)

3.1 Device Structure and Physical Operation

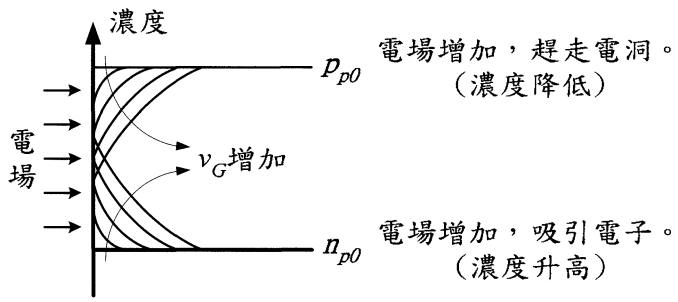
1. MOS (Metal Oxide Semiconductor)



2. Concept:
   a. $I \approx 0$, 利用電壓改變電場，故為 voltage control。(BJT 為 current control)
   b. Body is always connected to V_{SS}. (最負電壓) 故 device 內部的 pn junction 皆為逆偏。
   c. Four terminals device。(BJT is three terminals device)



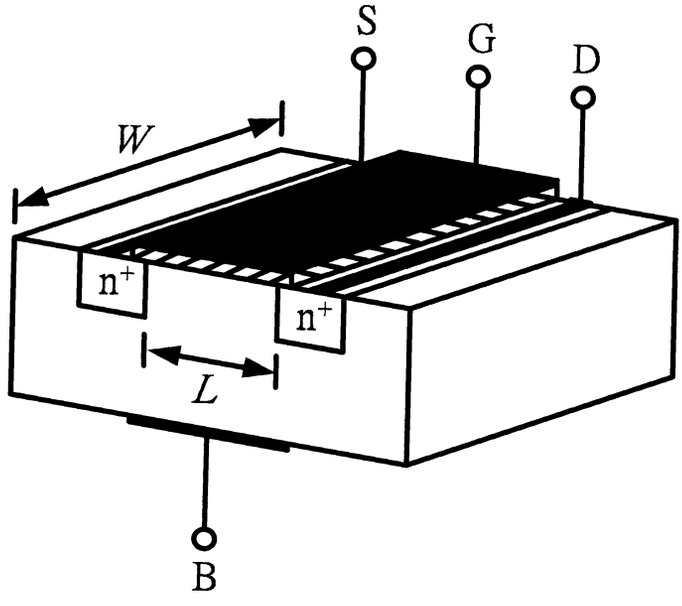
3. 如何利用改變 gate 電壓讓 MOS 工作？
   a. 增加 gate 電壓，增加電場，改變表面的電子與電洞濃度
   b. 當反轉層(inversion layer)產生的時候，定義此時的 $v_{GS} = V_t$ (t: threshold)。
   c. 當 $v_{GS} \geq V_t$ 時，會在表面產生 n 通道。(induce n-channel)
   d. 僅有 drift current，無 diffusion current。(unipolar)



4. Summary
   a. Voltage control (v_{GS})
   b. Unipolar (單一載子工作)
   c. 僅有 drift current，無 diffusion current
   d. $R_i = \infty \Rightarrow i_G = 0$
   e. 對稱元件(symmetry device)，source 和 drain 濃度相同
   f. 熱穩定性高(thermal stability)。$T \uparrow \Rightarrow i_D \downarrow$
   g. 產生 n-channel 的 MOS 稱為 NMOS，反之，產生 p-channel 的為 PMOS
   h. Enhancement type (增強型): MOS 的通道需額外改變 gate 電壓才能產生
      Depletion type (空乏型): MOS 製作時，就已經包含通道

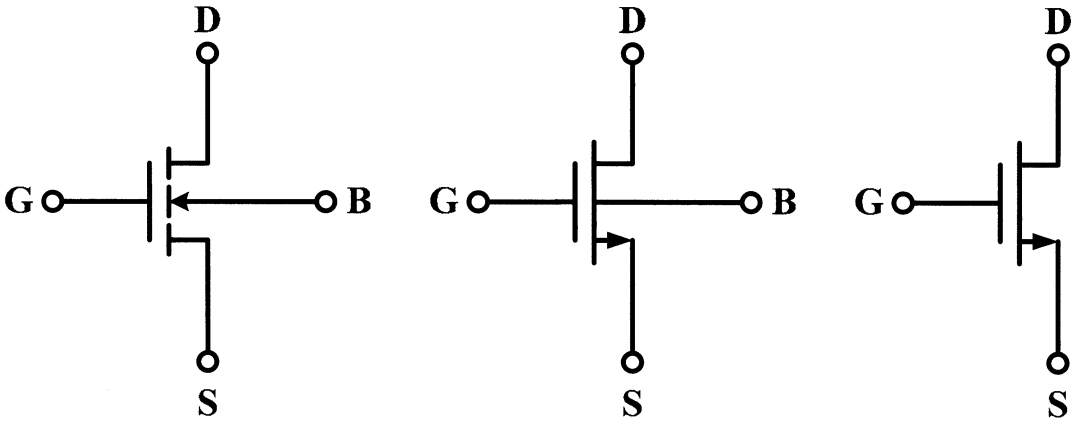
5. 如何降低 V_t (threshold voltage)
   a. 增加 $\varepsilon_{ox} / t_{ox}$
   b. 增加 source 和 drain region 的濃度(N_D)
   c. 降低 substrate 的濃度(N_A)　(改變最明顯)

6. MOS dimension
   a. L: 通道長度 (channel length)
   b. W: 通道寬度 (channel width)

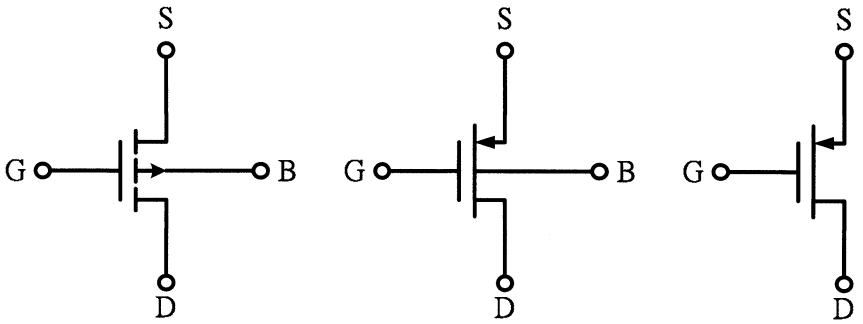


7. Circuit symbol

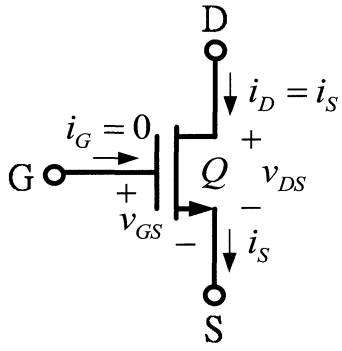
a. Enhancement type NMOS



b. Enhancement type PMOS

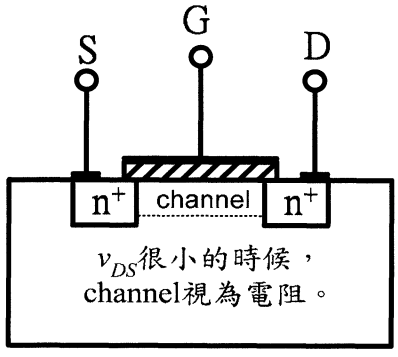


3.2 Current-Voltage Characteristics



1. For $v_{GS} \le V_t$ Q：cutoff

   $i_D = 0$



2. For $v_{GS} > V_t$ and $v_{DS} < v_{GS} - V_t (v_{GD} > V_t)$

   $\Rightarrow$continuous channel Q：triode region

   $$i_D = k_n'\left(\frac{W}{L}\right)\left[(v_{GS} - V_t)v_{DS} - \frac{1}{2}v_{DS}^2\right], k_n' = \mu_n C_{ox}$$

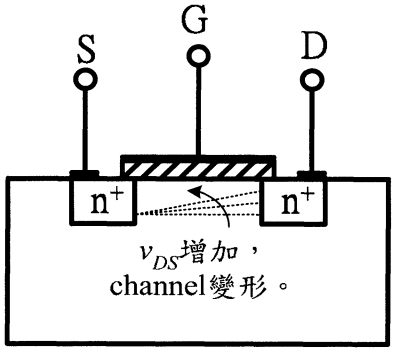
   當v_{DS}很小的時候，上式可忽略$\frac{1}{2}v_{DS}^2$該項，

   則電流可近似為

   $$i_D = k_n'\left(\frac{W}{L}\right)(v_{GS} - V_t)v_{DS}$$

   $\because i_D \propto v_{DS}$ 適用歐姆定律

   $\Rightarrow Q$：ohmic region



3. For $v_{GS} > V_t$ and $v_{DS} > v_{GS} - V_t (v_{GD} < V_t)$

   $\Rightarrow$pinched-off channel Q：saturation region

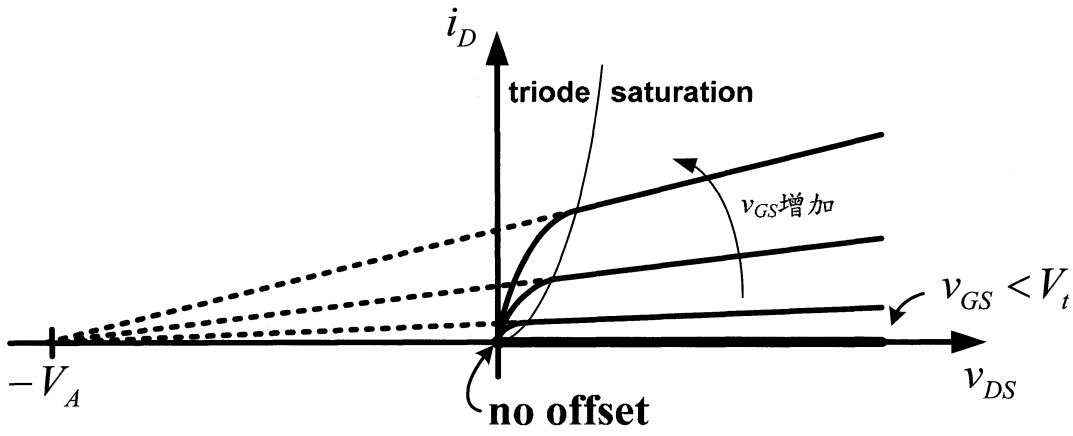
   $$i_D = \frac{1}{2}k_n'\left(\frac{W}{L}\right)(v_{GS} - V_t)^2\left(1 + \frac{v_{DS}}{V_A}\right)$$

4. Channel length modulation

a. 利用 V_A 來等效表示輸出電流和輸出電壓的關係

b. 令 $\lambda = (V_A)^{-1} \Rightarrow i_D = \frac{1}{2} k_n' \left(\frac{W}{L}\right)(v_{GS} - V_t)^2 (1 + \lambda v_{DS})$

c. 電晶體的輸出阻抗 $r_o = \left(\frac{\partial I_D}{\partial v_{DS}}\right)^{-1}\Big|_{v_{GS}=V_{GS}} = \frac{V_{DS} + V_A}{I_D} \approx \frac{V_A}{I_D}$

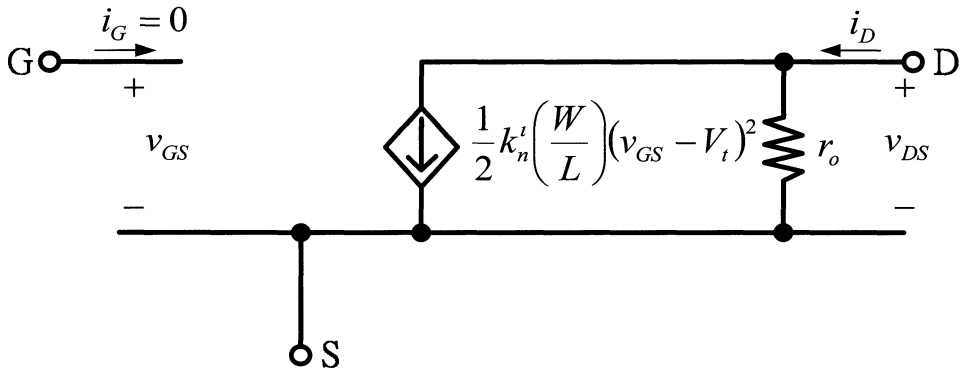


V_A : Early voltage

3.3 Large-Signal Model (In Saturation Region)

1. Large-Signal Model

a. r_o 用來 model channel length modulation



3.4 MOS Circuits at DC

1. BJT and MOS DC analysis

a. BJT

① 已知：$V_{BE}=0.7\ V$ (constant voltage drop)

② 待求：I_B、I_C、I_E、and V_{CE}

b. MOSFET

① 已知：$I_G=0\ mA$ (input impedance is infinite)

② 待求：I_D、V_{GS}、and V_{DS}

Example 1

Design 使得 I_D=0.5 mA 、V_D=1 V

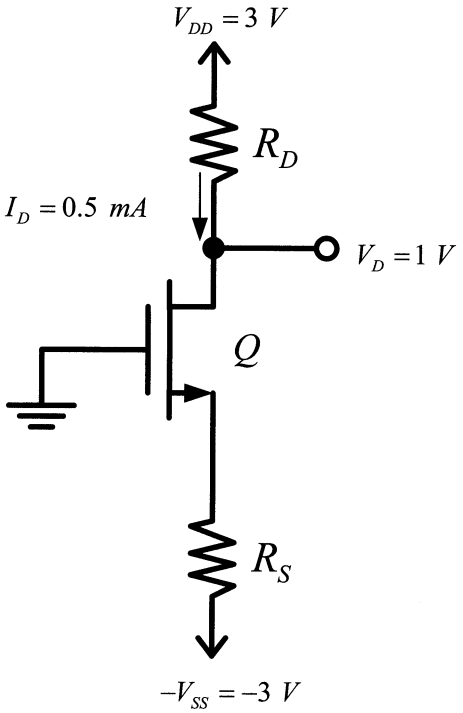
Given $V_t=0.7\ V$、$k_n'\left(\frac{W}{L}\right)=1\ mA/V^2$

$V_A\to\infty\ (\lambda=0)$

問 $R_D=?$、$R_S=?$

Sol:

$$R_D=\frac{V_{DD}-V_D}{I_D}=\frac{3-1}{0.5}=4\ k\Omega$$



$V_G-V_D=0-1=-1\ V<V_t=0.7\ V$

$\therefore$ pinched-off channel

$\Rightarrow$ Q is in saturation region.

$$I_D=\frac{1}{2}k_n'\frac{W}{L}(V_{GS}-V_t)^2$$

$$\Rightarrow 0.5=\frac{1}{2}\times 1(V_{GS}-0.7)^2$$

$\Rightarrow V_{OV}=V_{GS}-0.7=1V$ (-1V 不合)

$V_{GS}=V_t+V_{OV}=0.7+1=1.7\ V$ $\quad\therefore V_S=V_G-V_{GS}=0-1.7=-1.7\ V$

$$R_S=\frac{-1.7-(-3)}{0.5}=2.6\ k\Omega$$

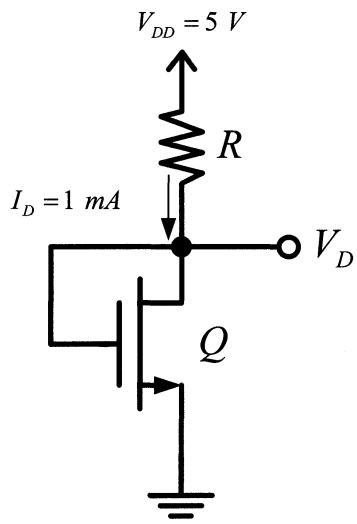
Example 2

Design 使得 $I_D = 1\ mA$

Given $V_t = 1\ V$、$k_n'\left(\frac{W}{L}\right) = 2mA/V^2$、$V_A \to \infty\ (\lambda = 0)$

問 $R = ?$、此時 $V_D = ?$

Sol:



$V_{GD} = 0\ V < V_t = 1\ V$

$\therefore$ Q is in saturation region.

$$I_D = \frac{1}{2}k_n'\frac{W}{L}(V_{GS} - V_t)^2$$

$$\Rightarrow 1 = \frac{1}{2} \times 2(V_{GS} - 1)^2$$

$$\Rightarrow V_{OV} = 1\ V\ (-1V\text{不合理})$$

$$\therefore V_{GS} = V_t + V_{OV} = 1 + 1 = 2\ V = V_D$$

$$R = \frac{V_{DD} - V_D}{I_D} = \frac{5-2}{1} = 3\ k\Omega$$

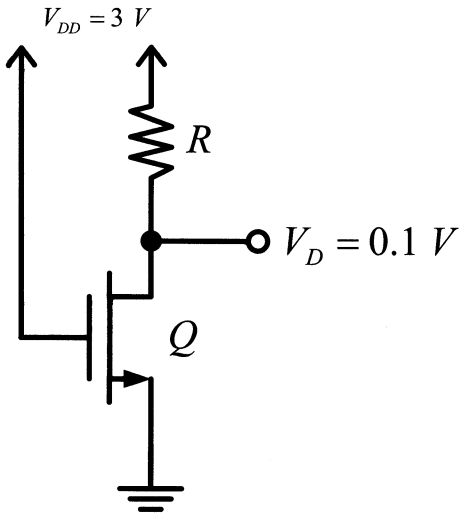
Example 3

Design 使得 $V_D = 0.1\ V$

Given $V_t = 0.5\ V$、$k_n'\left(\frac{W}{L}\right) = 1\text{m}A/V^2$、$V_A \to \infty\ (\lambda = 0)$

問 $R = ?$、此時 $r_{DS} = ?$

Sol:



$$V_{GD} = V_G - V_D = 3 - 0.1 = 2.9\ V > V_t = 0.5\ V$$

$\therefore$ Q is in triode region.

$$I_D = k_n'\left(\frac{W}{L}\right)\left[(V_{GS} - V_t)V_{DS} - \frac{1}{2}V_{DS}^2\right]$$

$$\Rightarrow I_D = 1\times\left[(3-0.5)\times 0.1 - \frac{1}{2}(0.1)^2\right]$$

$$= 0.25 - 0.005 = 0.245\ mA$$

$$R = \frac{V_{DD} - V_D}{I_D} = \frac{3-0.1}{0.245} = 11.8\ k\Omega$$

$$r_{DS} \cong \frac{V_{DS}}{I_D} = \frac{0.1}{0.245} = 408\ \Omega$$

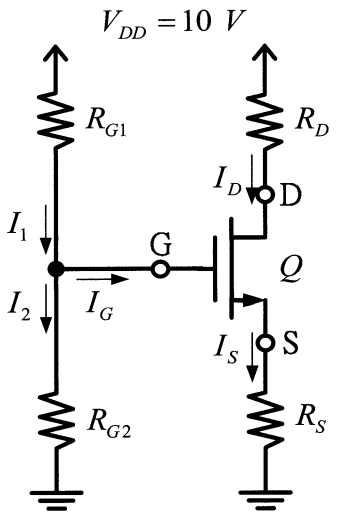
Example 4

Given $V_t = 1\ V$、$k_n'\left(\frac{W}{L}\right) = 0.5\ \text{m}A/V^2$、$\lambda = 0$

$R_{G1} = 5\ M\Omega$、$R_{G2} = 5\ M\Omega$、$R_D = 6\ k\Omega$、$R_S = 6\ k\Omega$

求：各電位（V_G、V_s、V_D）及各電流（I_G、I_s、I_1、I_2）

Sol:



$I_G = 0\ mA$

$I_1 = I_2 = \frac{10}{5+5} = 1\ \mu A$

$V_G = 10 \times \frac{5}{5+5} = 5\ V$

假設 Q is in saturation region

$$\begin{cases} I_D = \frac{1}{2}k_n'\left(\frac{W}{L}\right)(V_{GS} - V_t)^2 \quad \cdots(1) \\ V_{GS} = V_G - V_S = 5 - I_D \times 6 \quad \cdots(2) \end{cases}$$

$\Rightarrow I_D = 1\ mA$ or $I_D = \frac{4}{9}\ mA$

If $I_D = 1\ mA$ $\quad V_S = 1 \times 6 = 6\ V > V_G = 5\ V$ （不合）

$\therefore I_D = \frac{4}{9}\ mA$

$V_S = \frac{4}{9} \times 6 = 2.67V < (V_G - Vt) = 5 - 1 = 4\ V$（合理）

$V_D = 10 - \frac{4}{9} \times 6 = 7.33\ V$

Check

$V_{GD} = V_G - V_D = 5 - 7.33 = -2.33\ V < V_t = 1\ V$

$\therefore$ Q is in saturation region. (原假設是對的)

Example 5

Design 使得 Q_p in saturation region，$I_D = 1\ mA$ 、$V_D = 3\ V$ (即 $V_{DS} = -2\ V$)

Given $V_t = -1\ V$、$k_p'\left(\frac{W}{L}\right) = 2\ mA/V^2$、$\lambda = 0$

問 $R_D = ?$、$R_{G1} = ?$、$R_{G2} = ?$　另求 $R_{DMax} = ?$

Sol:

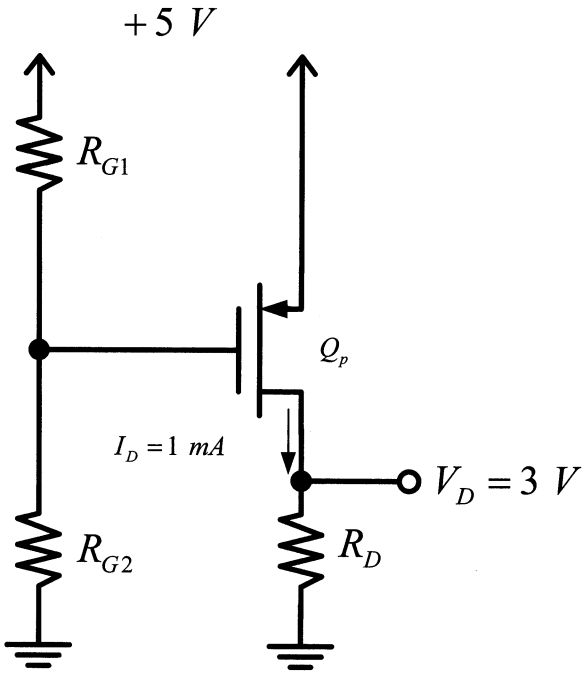
$$R_D = \frac{V_D - 0}{I_D} = \frac{3-0}{1} = 3\ k\Omega$$

$$I_D = \frac{1}{2}k_p'\frac{W}{L}(V_{GS} - V_t)^2$$

$$\Rightarrow 1 = \frac{1}{2}\times 2\times\left[V_{GS} - (-1)\right]^2$$

$$\Rightarrow V_{GS} = -2\ V$$ （另一解不合）

$$V_G = V_S + V_{GS} = 5 - 2 = 3\ V$$



$$\therefore \frac{R_{G1}}{R_{G2}} = \frac{2}{3}$$　Choose $R_{G1} = 2\ M\Omega$ 、$R_{G2} = 3\ M\Omega$

另求 R_{DMax}，而 Q_p 仍工作於飽和區，$I_D = 1\ mA$

The boundary of saturation region and triode region

$$\Rightarrow |V_{DS}| = |V_{GS} - V_t| \text{ or } |V_{GD}| = |V_t|$$

$$\Rightarrow |V_{DS}| = |-2-(-1)| = 1\ V \quad \therefore V_{DMax} = 4\ V \quad \Rightarrow R_{DMax} = \frac{4}{1} = 4\ k\Omega$$

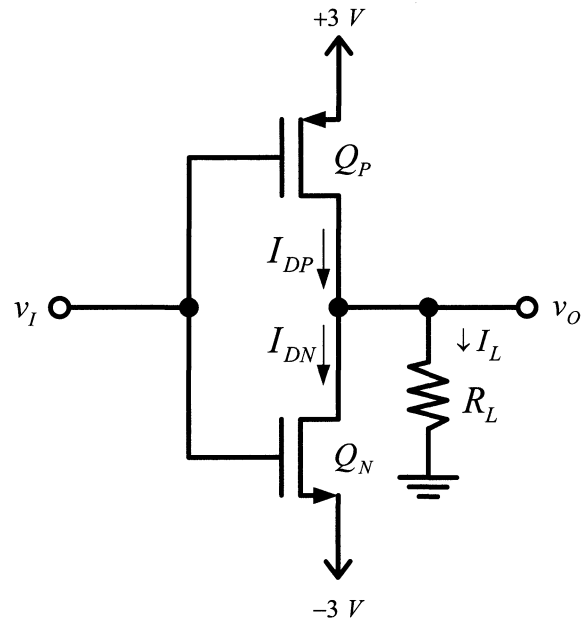
Example 6

Given $Q_N = Q_P$ (match) $V_{tN} = -V_{tP} = 1\ V$ 、 $k_n'\left(\frac{W}{L}\right)_N = k_p'\left(\frac{W}{L}\right)_P = 2\ mA/V^2$ 、

$V_{AN} = |V_{AP}| = \infty$ 、 $R_L = 5\ k\Omega$

問當(a) $v_I = 0\ V$ 、(b) $v_I = 3\ V$ 時，$I_{DN} = ?$、$I_{DP} = ?$、$v_O = ?$

Sol:



(a)當 $v_I = 0\ V$ 時，

$\because Q_N = Q_P$ 由電路具對稱性知 $v_O = 0\ V$

$I_L = 0$

$|V_{GD}| = 0 < |V_t| = 1\ V$

$\therefore Q$ is in saturation region

$I_D = \frac{1}{2}k_n'\left(\frac{W}{L}\right)(V_{GS} - V_t)^2$

$\Rightarrow I_D = \frac{1}{2}\times 2\times(3-1)^2 = 4\ mA \quad I_{DN} = I_{DP} = 4\ mA$

(b)當 $v_I = 3\ V$ 時，

Q_P 之 $V_{GS} = 0V$ ，$\therefore$ Q_P ：cut off，$I_{DP} = 0$

又 $-3 \le V_D \le 0 \quad \therefore V_{GD} \ge 3\ V > V_t = 1\ V$

$\therefore Q_N$ is in triode region. $\Rightarrow I_{DN} = k_n'\left(\frac{W}{L}\right)\left[(V_{GS} - V_t)V_{DS} - \frac{1}{2}V_{DS}^2\right]$

另外 Q_P 的 $V_{SG} = 0 \quad \therefore Q_P$ off.，而 $I_L = -I_{DN}$

假設 $(V_{GS} - V_t)V_{DS} >> \frac{1}{2}V_{DS}^2$ 即忽略 $\frac{1}{2}V_{DS}^2$ 項，

$$\therefore \begin{cases} I_{DN} = 2\times(6-1)\times[v_O - (-3)] & \cdots(1) \\ I_{DN} = \dfrac{0 - v_O}{R_L} = \dfrac{-v_O}{5} & \cdots(2) \end{cases} \Rightarrow \begin{cases} I_{DN} = 0.588\ mA \\ v_O = -2.94\ V \approx -3\ V \end{cases}$$

$I_{DP} = 0\ mA$ 、 $I_{DN} = 0.588\ mA$ 、 $v_O = -2.94\ V$

Check $V_{DS} = v_O - (-3) = -2.94 + 3 = 0.06\ V << V_{GS} - V_t = 5\ V$ (原假設是對的)

3.5 Biasing in MOS Amplifier Circuits

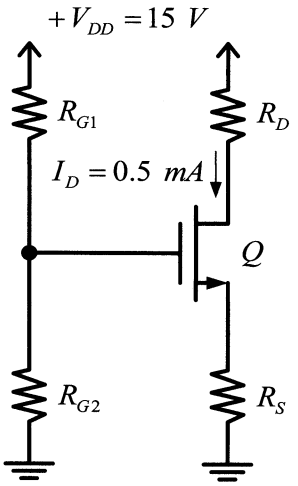
The design of MOS DC bias

Design 使得 $I_D = 0.5\ mA$

Given $V_{tN} = 1\ V$ 、$k_n'\left(\frac{W}{L}\right) = 1\ mA/V^2$ 、$V_A = \infty$

問 $R_{G1} = ?$、$R_{G2} = ?$、$R_D = ?$、$R_S = ?$

Sol:



Choose $V_D = \frac{2}{3}V_{DD} = 10\ V$

$$V_S = \frac{1}{3}V_{DD} = 5\ V$$

$$\Rightarrow R_D = \frac{V_{DD} - V_D}{I_D} = \frac{15-10}{0.5} = 10\ k\Omega$$

$$R_S = \frac{V_S - 0}{I_S} = \frac{5-0}{0.5} = 10\ k\Omega$$

Q is in saturation region

$$I_D = \frac{1}{2}k_n'\left(\frac{W}{L}\right)(V_{GS} - V_t)^2$$

$$\Rightarrow 0.5 = \frac{1}{2}\times 1\times (V_{GS} - 1)^2 \quad \Rightarrow V_{GS} = 2\ V \text{ or } V_{GS} = 0\ V \text{ (不合)}$$

$$\therefore V_G = V_S + V_{GS} = 5 + 2 = 7\ V \quad \text{則} \frac{R_{G1}}{R_{G2}} = \frac{8}{7}$$

Choose $R_{G1} = 8\ M\Omega$ 、$R_{G2} = 7\ M\Omega$

＊Discussion

a. Choose voltage drop across each of R_D 、V_{DS} 、R_S 為 $\frac{1}{3}V_{DD}$

b. $V_D = 10\ V$ ，則輸出訊號大小限制為

① Maximum positive signal swing：

$$V_{D\max} - V_D = V_{DD} - V_D = 15 - 10 = 5\ V$$

② Maximum negative signal swing：

$$V_D - V_{D\min} = V_D - (V_G - V_t) = 10 - (7 - 1) = 4\ V$$

c. 工作點穩定性

假設電晶體的 V_t 改為 1.5 V，則 I_D 變成？

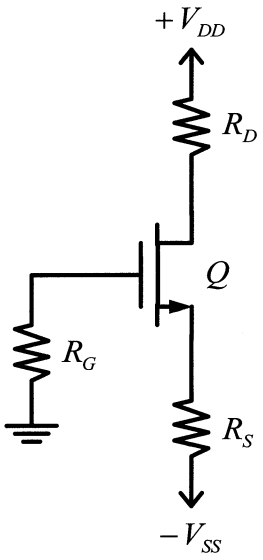
$$V_G = V_{DD} \times \frac{R_{G2}}{R_{G1} + R_{G2}} = 7 \ V \quad \text{(fixed)}$$

$$\begin{cases} I_D = \frac{1}{2} \times 1 \times (V_{GS} - 1.5)^2 & \cdots(1) \\ V_G = 7 = V_{GS} + V_S = V_{GS} + I_D R_D & \cdots(2) \end{cases} \Rightarrow I_D = 0.455 \ mA$$

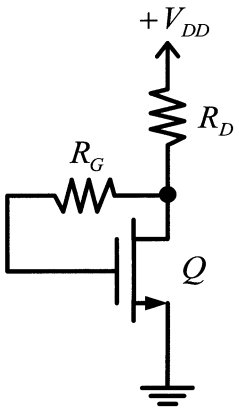
$$\Delta I_D = 0.455 - 0.5 = -0.045 \ mA \quad (9\% \text{的誤差})$$

其他典型 discrete circuit 偏壓電路

a. 兩個 power supply



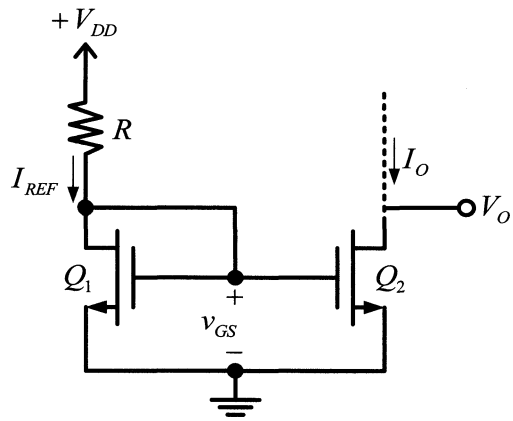
b. Gate-drain self-bias



Current mirror (電流鏡)

a. $Q_1 = Q_2$

$$\Rightarrow \begin{cases} V_{t1} = V_{t2} = V_t \\ k_{n1}' = k_{n2}' = k_n' \\ \vdots \end{cases}$$



b. Q_1 ：saturation $\because V_{GD} = 0$

c. Q_2 ：saturation if $V_{DS2} > V_{GS2} - V_t$

d. $V_{GS1} = V_{DS1} = V_{GS2} = V_{GS}$

and $V_{DS2} = V_O$

e. $$\begin{cases} I_{D1} = I_{REF} = \dfrac{1}{2} k_n' \left(\dfrac{W}{L}\right)_1 (V_{GS} - V_t)^2 \cdots (1) \\ I_{D1} = I_{REF} = \dfrac{V_{DD} - V_{GS}}{R} \qquad \cdots (2) \end{cases}$$

f. $I_O = I_{REF} \dfrac{\left(W/L\right)_2}{\left(W/L\right)_1}$

g. 電流源的輸出電阻 $r_o = \dfrac{\Delta V_O}{\Delta I_O} = \dfrac{V_A + V_{DS}}{I_O} \approx \dfrac{V_A}{I_O}$

h. Current source 由 PMOS 組成；current sink 由 NMOS 組成。

Example

Design 使得 $I_{REF}=100\ \mu A$

Given $V_{DD}=3\ V$、$Q_1=Q_2$、$V_t=0.7\ V$、$V_A'=20\ V/\mu m$、$k_n'=200\ \mu A/V^2$、

$L=1\ \mu m$、$W=10\ \mu m$

問 (a)$R=?$、$r_{o2}=?$； (b)若 $\Delta V_O=1\ V$，則 $\Delta I_O=?$

Sol

(a)

$$I_{D1}=\frac{1}{2}k_n'\left(\frac{W}{L}\right)_1\left(V_{GS}-V_t\right)^2$$

$$\Rightarrow 100=\frac{1}{2}\times 200\times\frac{10}{1}\times\left(V_{Gs}-V_t\right)^2$$

$$\Rightarrow V_{OV}=0.316\ V$$

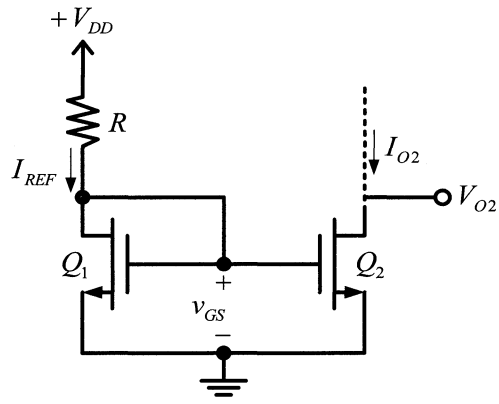
$$\therefore V_{GS}=V_t+V_{OV}$$

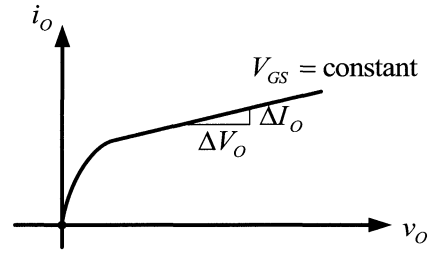
$$=0.7+0.316=1\ V$$

$$\therefore R=\frac{V_{DD}-V_{GS}}{I_{REF}}=\frac{3-1}{0.1}=20\ k\Omega$$

$$r_{o2}=\frac{V_A}{I_{O2}}=\frac{V_A'\times L}{I_{O2}}$$

$$=\frac{20\times 1}{0.1}=200\ k\Omega$$





(b)

$$r_{o2}=\frac{\Delta V_{O2}}{\Delta I_{O2}}=\frac{1}{\Delta I_{O2}}=200\ k\Omega\ \Rightarrow \Delta I_{O2}=5\ \mu A$$

即若 V_O 增加 $1\ V$，則 I_{O2} 由原 $I_{REF}=100\ \mu A$ 增加 $5\ \mu A$

3.6 Small-Signal Operation and Models

1. Concept of MOS small-signal model

a. 令 $i_D \equiv I_D + i_d \quad i_D = \frac{1}{2}k_n'\left(\frac{W}{L}\right)\left[(V_{GS}+v_{gs})-V_t\right]^2$

$$\Rightarrow i_D = \frac{1}{2}k_n'\left(\frac{W}{L}\right)\left[(V_{GS}-V_t)^2 + 2(V_{GS}-V_t)v_{gs} + v_{gs}^2\right]$$

$$i_D \approx \frac{1}{2}k_n'\left(\frac{W}{L}\right)\left[(V_{GS}-V_t)^2 + 2(V_{GS}-V_t)v_{gs}\right] \quad \text{when} \quad v_{gs} << 2(V_{GS}-V_t)$$

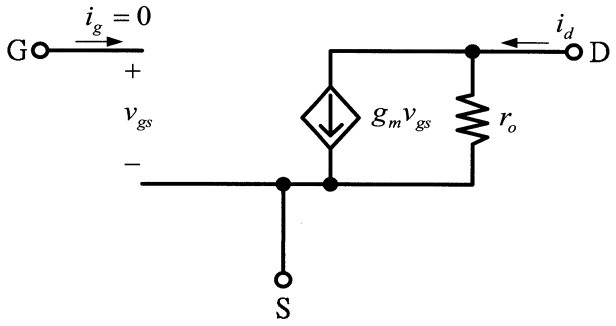
rewrite $i_D = \frac{1}{2}k_n'\left(\frac{W}{L}\right)\left[(V_{GS}-V_t)^2 + 2(V_{GS}-V_t)v_{gs}\right] = I_D + i_d$

$$\therefore i_d = k_n'\left(\frac{W}{L}\right)(V_{GS}-V_t)v_{gs} = g_m v_{gs} \quad \text{where} \quad g_m \equiv k_n'\left(\frac{W}{L}\right)(V_{GS}-V_t)$$

b. 直接微分

$$g_m \equiv \frac{i_d}{v_{gs}} = \frac{\partial i_D}{\partial v_{GS}}\bigg|_{v_{GS}=V_{GS}} = k_n'\left(\frac{W}{L}\right)(V_{GS}-V_t)$$

2. Small-signal model



a. $g_m = k_n'\left(\frac{W}{L}\right)(V_{GS}-V_t)$ and $r_o = \frac{V_A}{I_D}$

b. $g_m = k_n'\left(\frac{W}{L}\right)(V_{GS}-V_t) = \sqrt{2k_n'\left(\frac{W}{L}\right)I_D} = \frac{2I_D}{(V_{GS}-V_t)}$

c. 由 b.可知

① $g_m \propto (V_{GS}-V_t)$

② $g_m \propto \sqrt{I_D}$

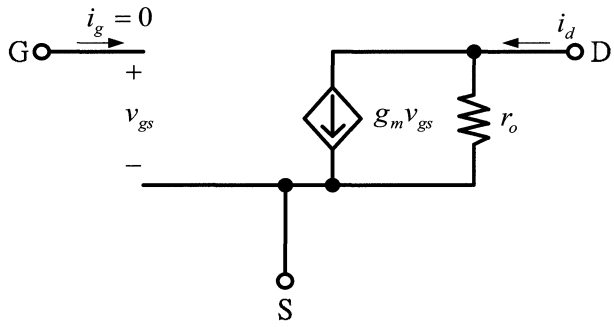
③ $g_m \propto \frac{W}{L}$

3. Comparison with MOS and BJT

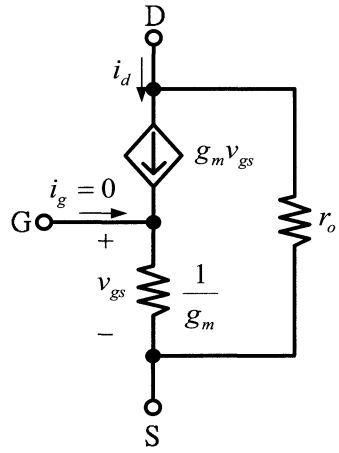
	MOS	BJT
g_m	$g_m = \dfrac{I_D}{(V_{GS} - V_t)/2}$ 較小	$g_m = \dfrac{I_D}{V_T}$ 較大
r_{in}	$r_{in} \to \infty$ 較大	r_{in} 較小
IC 製作	面積小，製程簡單	面積大，製程複雜
熱穩定性	$T\uparrow \Rightarrow \mu_n \downarrow \Rightarrow I_D \downarrow$ $T\uparrow \Rightarrow V_t \downarrow \Rightarrow I_D \uparrow$ total $T\uparrow \Rightarrow I_D \downarrow$	$T\uparrow \Rightarrow I_C \uparrow$

4.

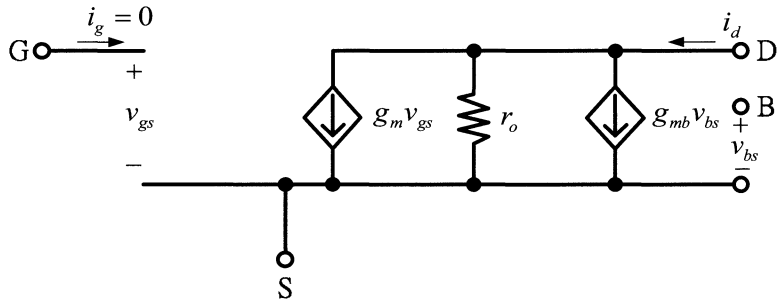
a. Hybrid-π model



b. T model



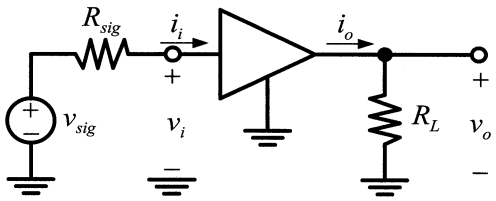
5. Body effect in small-signal model



a. $g_{mb} = \chi g_m$ where $\chi = 0.1 \sim 0.2$

3.7 Single-Stage Discrete-Circuit MOS Amplifiers

1. Definition



a. Input resistance $R_{in} \equiv \dfrac{v_i}{i_i}$

b. Input resistance with no load $R_i \equiv \left.\dfrac{v_i}{i_i}\right|_{R_L=\infty}$

c. Voltage gain $A_v \equiv \dfrac{v_o}{v_i}$

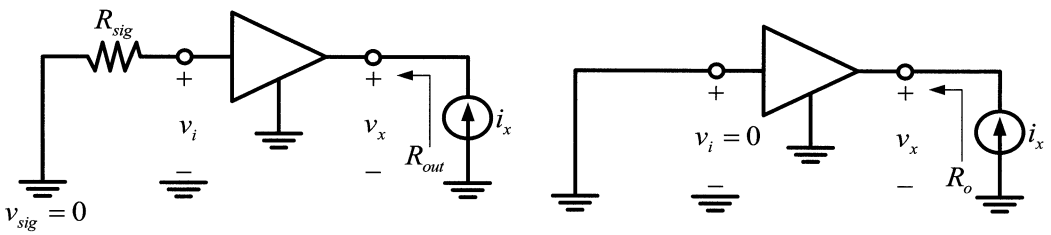
d. Open-circuit voltage gain $A_{vo} \equiv \left.\dfrac{v_o}{v_i}\right|_{R_L=\infty}$

e. Overall voltage gain $G_v \equiv \dfrac{v_o}{v_{sig}}$

f. Overall open-circuit voltage gain $G_{vo} \equiv \left.\dfrac{v_o}{v_{sig}}\right|_{R_L=\infty}$

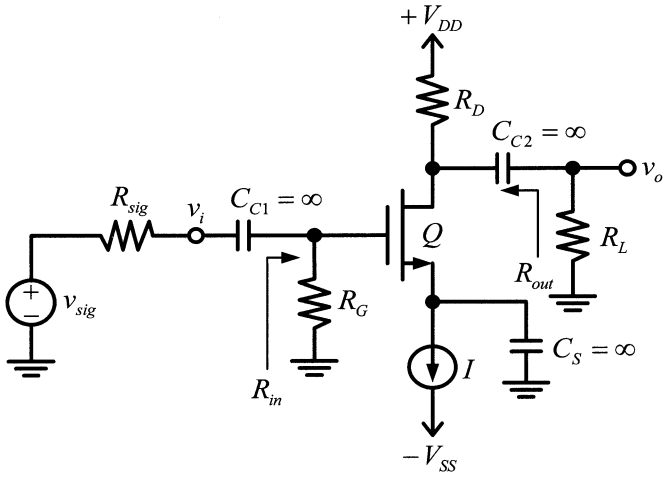
g. Output resistance $R_{out} \equiv \left.\dfrac{v_x}{i_x}\right|_{v_{sig}=0}$

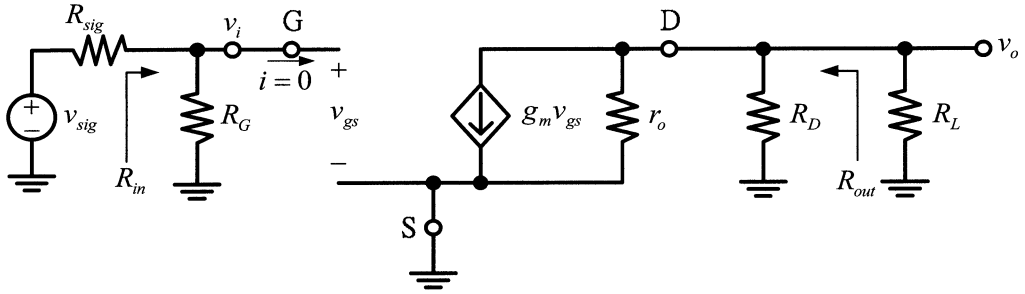
h. Output resistance of amplifier proper $R_o \equiv \left.\dfrac{v_x}{i_x}\right|_{v_i=0} = R_{out}\big|_{R_{sig}=0}$



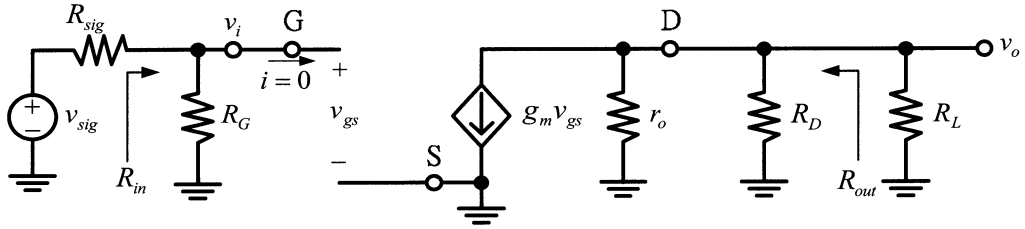
3.7.1 Common-Source (CS) Amplifier

1. Conventional CS amplifier





⇓小訊號電路簡化



a. $R_{in} = R_i = R_G$

b. $A_v = \dfrac{v_o}{v_i} = -g_m\left(r_o \| R_D \| R_L\right) = \dfrac{-\left(r_o \| R_D \| R_L\right)}{1/g_m} = -\dfrac{\text{total resistance in drain}}{\text{total resistance in source}}$

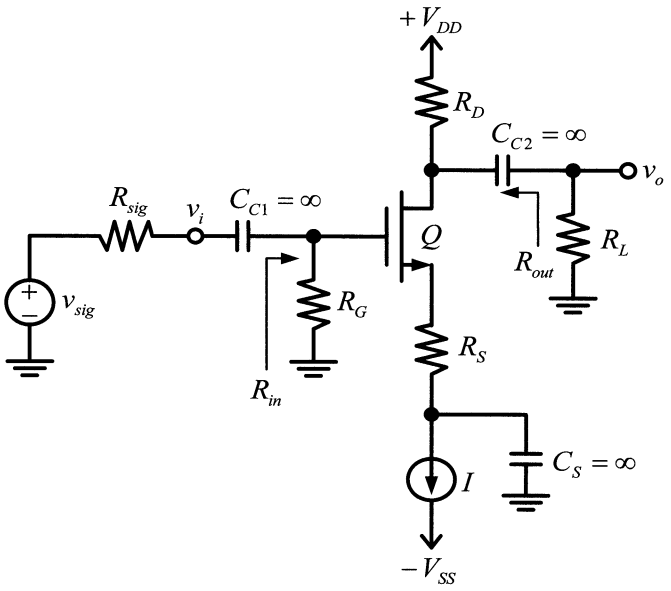
$$A_{vo} = A_v\big|_{R_L=\infty} = -g_m\left(r_o \| R_D\right)$$

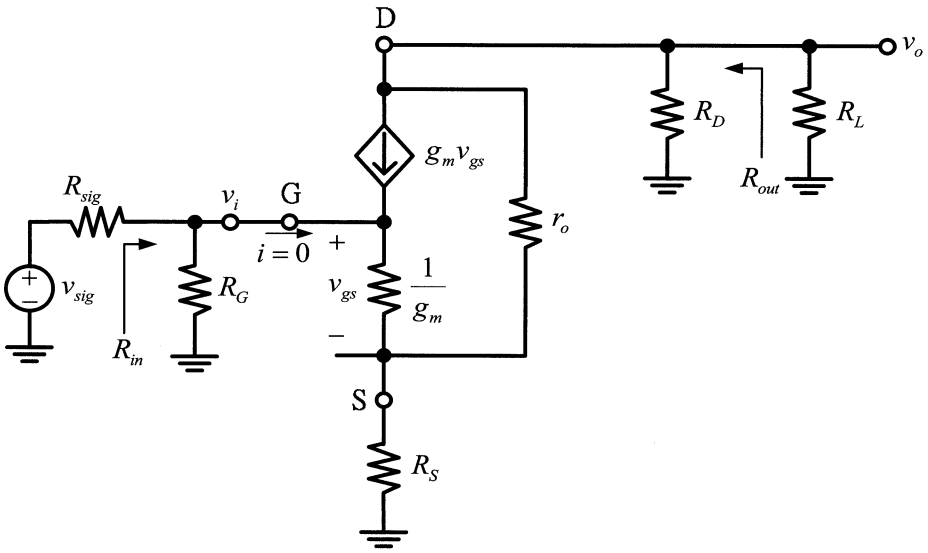
c. $G_v = \dfrac{v_o}{v_{sig}} = \dfrac{v_o}{v_i} \times \dfrac{v_i}{v_{sig}} = -g_m \left(r_o \| R_D \| R_L\right) \dfrac{R_G}{R_{sig} + R_G}$

$G_{vo} = G_v\big|_{R_L=\infty} = -g_m \left(r_o \| R_D\right) \dfrac{R_G}{R_{sig} + R_G}$

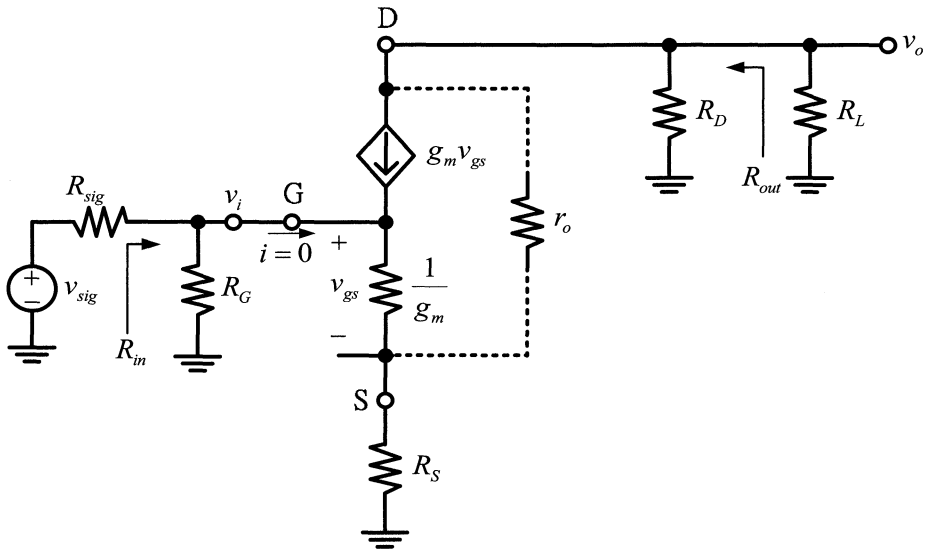
d. $R_{out} = R_o = \left(r_o \| R_D\right)$

2. CS amplifier with source degeneration (R_S)





⇓小訊號電路簡化



a. $R_{in} = R_i = R_G$

b. $A_v = \dfrac{v_o}{v_i} = \dfrac{-g_m v_{gs}\left(R_D \| R_L\right)}{v_i} = -g_m\left(R_D \| R_L\right)\dfrac{1}{1+g_m R_S} = -\dfrac{R_D \| R_L}{1/g_m + R_S}$

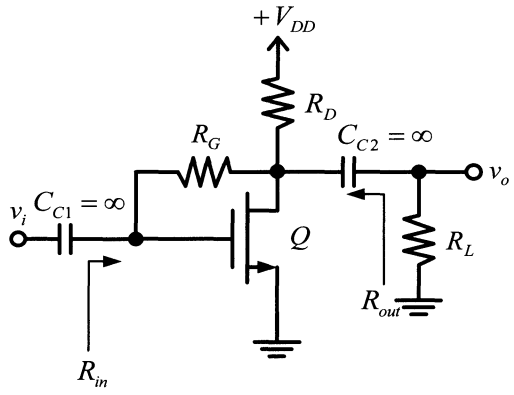
$A_{vo} = A_v\big|_{R_L=\infty} = -g_m R_D \dfrac{1}{1+g_m R_S}$

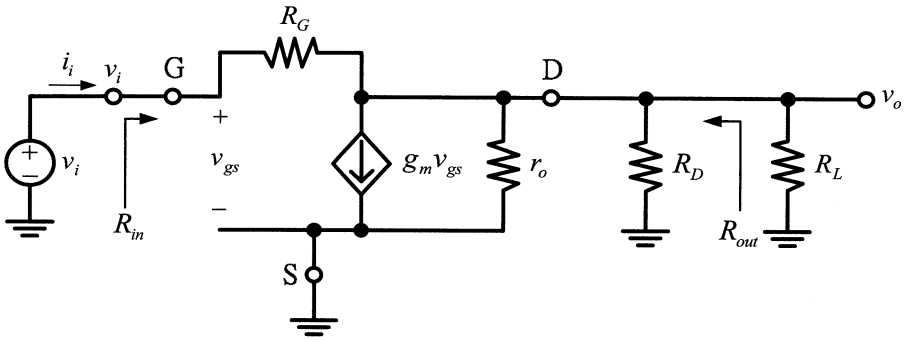
c. $G_v = \dfrac{v_o}{v_{sig}} = \dfrac{v_o}{v_i} \times \dfrac{v_i}{v_{sig}} = -g_m\left(R_D \| R_L\right)\dfrac{1}{1+g_m R_S} \times \dfrac{R_G}{R_{sig}+R_G}$

$G_{vo} = G_v\big|_{R_L=\infty} = -g_m R_D \dfrac{1}{1+g_m R_S} \times \dfrac{R_G}{R_{sig}+R_G}$

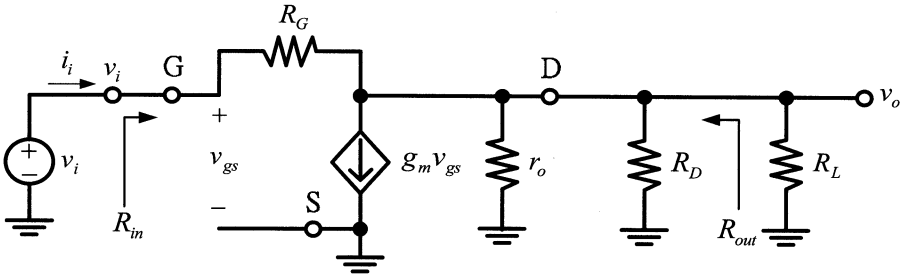
d. 上面的推導，皆假設r_o相對於其他電阻非常大，即忽略其效應

3. CS amplifier with negative feedback (R_G)





⇓小訊號電路簡化



Given $V_t = 1.5\ V$、$k_n'\left(\frac{W}{L}\right) = 0.25\ \ mA/V^2$　$V_A = 50\ \ V\ (\lambda = 0.02\ \ 1/V)$

$$R_D = 10\ \ k\Omega \text{、} R_L = 10\ \ k\Omega \text{、} R_G = 10\ \ M\Omega \text{、} V_{DD} = 15\ \ V$$

問 $R_{in} = ?$、$R_{out} = ?$、$A_v = ?$

Sol

1. DC analysis

$V_{GD} = 0 < V_t$　$\therefore Q$ is in saturation region

$$\Rightarrow \begin{cases} I_D = \frac{1}{2}k_n'\left(\frac{W}{L}\right)(V_{GS} - V_t)^2 \\ V_{GS} = V_{DS} = V_{DD} - I_D R_D \end{cases} \Rightarrow \begin{cases} I_D = \frac{1}{2} \times 0.25 \times (V_{GS} - 1.5)^2 \cdots (1) \\ V_{GS} = 15 - I_D \times 10 \qquad \cdots (2) \end{cases}$$

$$\Rightarrow \begin{cases} I_D = 1.06\ \ mA \\ V_{GS} = 4.4\ \ V \end{cases}$$

2. AC analysis

$$\therefore g_m = k_n'\left(\frac{W}{L}\right)(V_{GS} - V_t) = 0.725\ \ mA/V$$

$$R_{in} = \frac{v_i}{i_i} = \frac{v_i}{(v_i - v_o)/R_G} = \frac{R_G}{1 - v_o/v_i} = \frac{R_G}{1 - A_v} \quad \text{(Miller's theorem)}$$

$$A_v = \frac{v_o}{v_i} \approx \frac{-g_m v_{gs}\left(r_o \| R_D \| R_L\right)}{v_i} = -g_m\left(r_o \| R_D \| R_L\right) = -3.3 \ \ V/V$$

$$\because R_{in} = \frac{R_G}{1 - A_v} = 2.33 \ \ M\Omega$$

$$R_{out} = r_o \| R_D \| R_L = 8.24 \ \ k\Omega$$

3. 在此電路中，$R_i = R_{in}\big|_{R_L=\infty} = \dfrac{R_G}{1 + g_m\left(r_o \| R_D\right)} \neq R_{in}$

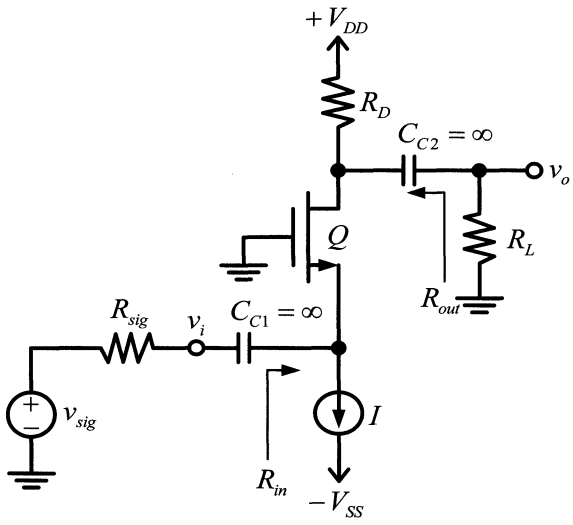
$$R_o = R_{out}\big|_{R_{sig}=0} = R_{out} \quad \because R_{sig} = 0$$

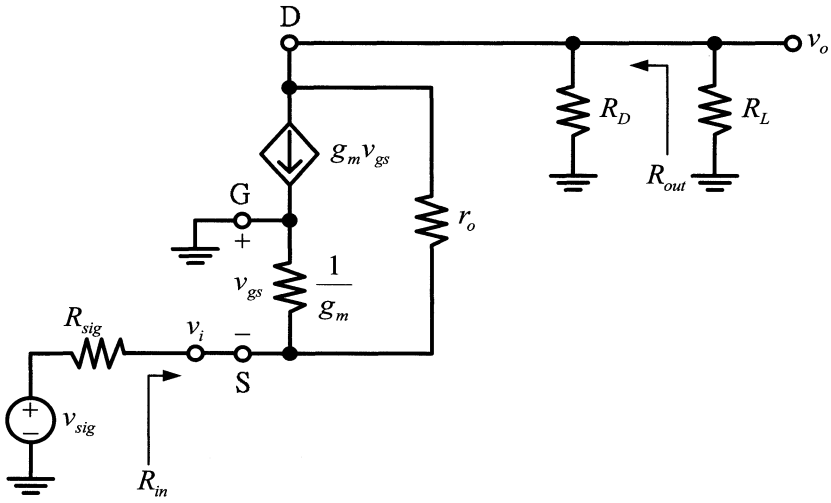
4.

a. Unilateral：輸入端不受輸出端影響

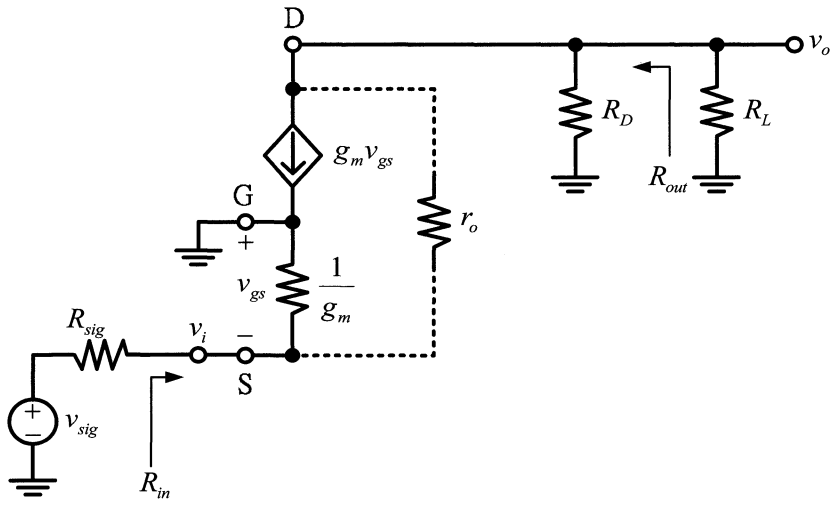
b. Non-unilateral：輸入端受輸出端影響，電路具有 internal feedback

3.7.2 Common-Gate (CG) Amplifier





⇓小訊號電路簡化



a. $R_{in} = R_i = \dfrac{1}{g_m}$

b. $A_v = \dfrac{v_o}{v_i} = \dfrac{-g_m v_{gs}(R_D \| R_L)}{v_i} = g_m(R_D \| R_L) \qquad (v_{gs} = -v_i)$

$A_{vo} = A_v\big|_{R_L=\infty} = g_m R_D$

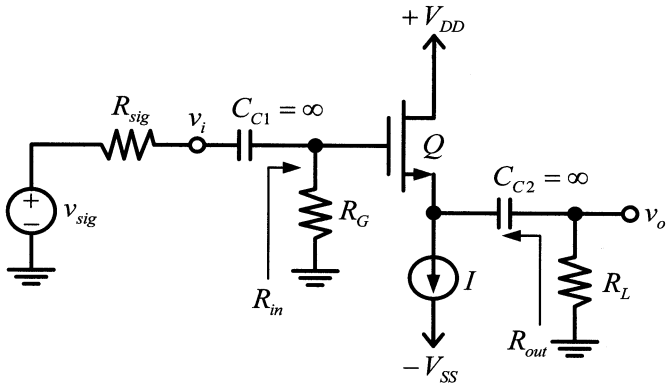
c. $G_v = \dfrac{v_o}{v_{sig}} = \dfrac{v_o}{v_i} \times \dfrac{v_i}{v_{sig}} = g_m(R_D \| R_L)\dfrac{1/g_m}{1/g_m + R_{sig}} = g_m(R_D \| R_L)\dfrac{1}{1+g_m R_{sig}}$

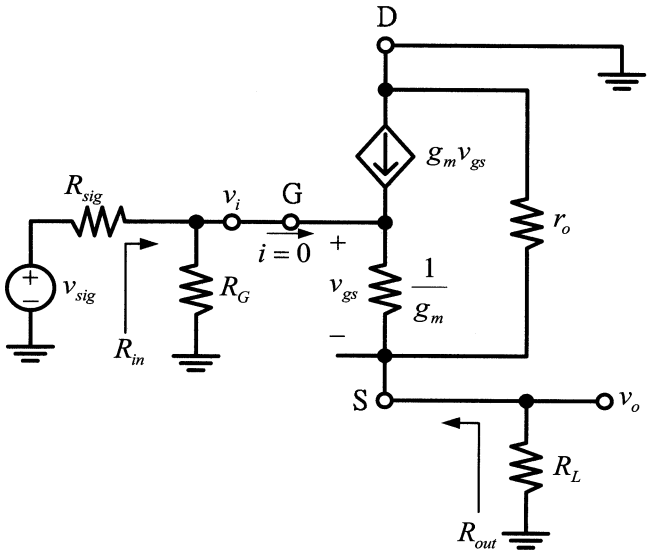
$G_{vo} = G_v\big|_{R_L=\infty} = g_m R_D \dfrac{1}{1+g_m R_{sig}}$

d. $R_{out} = R_o = R_D$

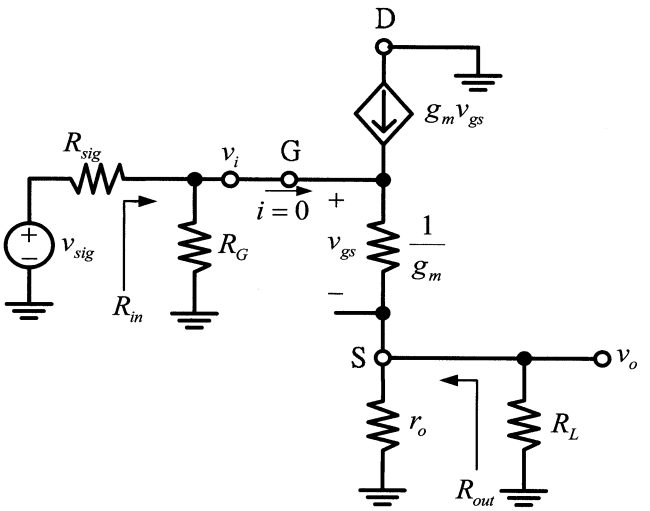
e. 上面的推導，皆假設r_o相對於其他電阻非常大，即忽略其效應

3.7.3 Common-Drain (CD) or Source Follower Amplifier





⇓小訊號電路簡化



a. $R_{in} = R_i = R_G$

b. $A_v = \dfrac{v_o}{v_i} = \dfrac{(r_o \| R_L)}{1/g_m + (r_o \| R_L)}$

$$A_{vo} = A_v\big|_{R_L=\infty} = \frac{r_o}{1/g_m + r_o}$$

c. $G_v = \dfrac{v_o}{v_{sig}} = \dfrac{v_o}{v_i} \times \dfrac{v_i}{v_{sig}} = \dfrac{(r_o \| R_L)}{1/g_m + (r_o \| R_L)} \times \dfrac{R_G}{R_{sig} + R_G}$

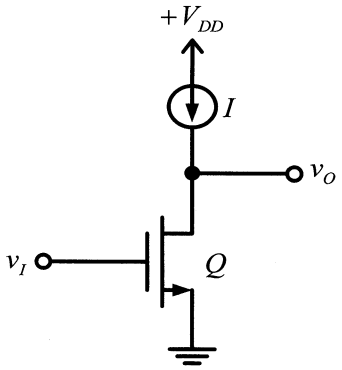
$$G_{vo} = G_v\big|_{R_L=\infty} = \frac{r_o}{1/g_m + r_o} \times \frac{R_G}{R_{sig} + R_G}$$

d. $R_{out} = R_o = \left(r_o \left\| \dfrac{1}{g_m} \right. \right) \approx \dfrac{1}{g_m}$

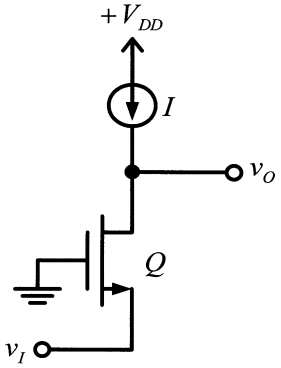
3.8 Single-Stage Integrated-Circuit MOS Amplifiers

1. Property
   a. 考慮 r_o 和 body effect
   b. 使用主動元件當負載。(Active load)

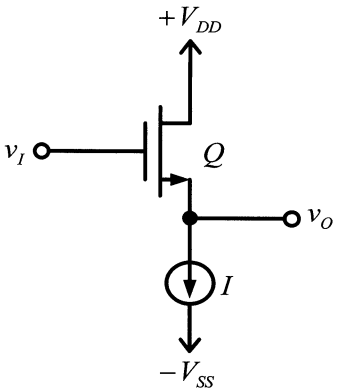
2. Three basic amplifier configuration
   a. Common-source amplifier (CS)



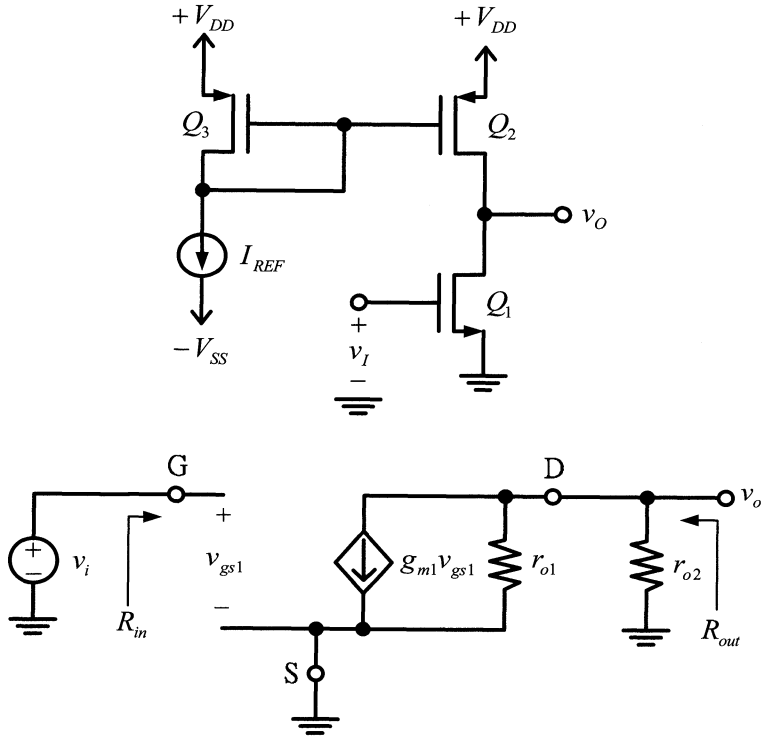
   b. Common-gate amplifier (CG)



   c. Common-drain amplifier (CD) or source follower



3.8.1 CS Amplifier with Active Load



a. $R_{in} = R_i = \infty$

b. $A_v = \dfrac{v_o}{v_i} = -g_{m1}\left(r_{o1} \| r_{o2}\right)$

$A_{vo} = A_v\big|_{R_L=\infty} = -g_{m1} r_{o1}$

c. $G_v = A_v = -g_{m1}\left(r_{o1} \| r_{o2}\right)$

$G_{vo} = G_v\big|_{R_L=\infty} = -g_{m1} r_{o1}$

d. $R_{out} = R_o = \left(r_{o1} \| r_{o2}\right)$

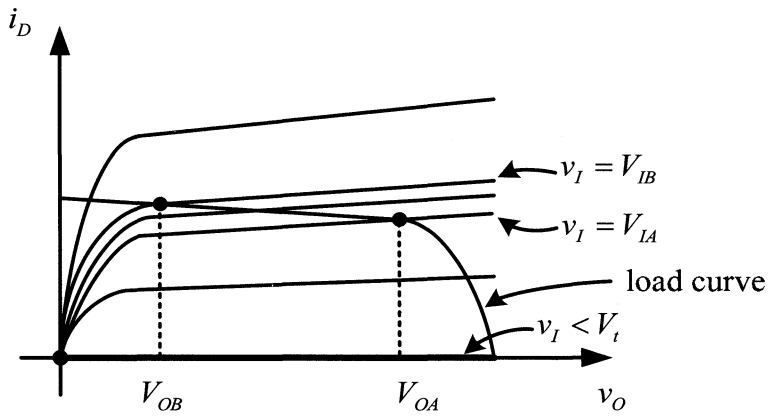
e. $I_{REF} = I_{D1} = I_{D2}$

if $I_{REF} \uparrow$ for discrete circuit $A_v \approx -g_m R_D \uparrow$ $\because g_m \propto \sqrt{I_D}$

for IC $A_v \approx -g_m r_o \downarrow$ $\because g_m \propto \sqrt{I_D}$ 、 $r_o \propto I_D^{-1} \Rightarrow A_v \propto 1/\sqrt{I_D}$

1. Input and output voltage range

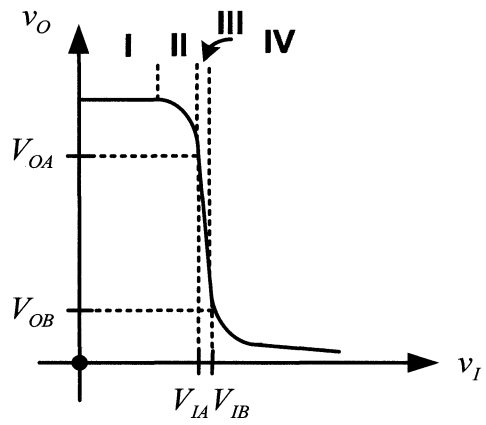
a. Output characteristic curve



① $V_{OA} = v_{O\max} = V_{DD} - \left(v_{SG2} - |V_{tP}|\right)$ if $v_O > v_{O\max}$ $\Rightarrow Q_2$ ：triode

② $V_{OB} = v_{O\min} = v_I - V_{tN}$ if $v_O < v_{O\min}$ $\Rightarrow Q_1$ ：triode

b. Voltage transfer characteristic



	v_I 範圍	MOS 狀態
Region I	$v_I < V_{tN}$	Q_1 ：cutoff Q_2 ：triode
Region II	$V_{tN} < v_I < V_{IA}$	Q_1 ：saturation Q_2 ：triode
Region III	$V_{IA} < v_I < V_{IB}$	Q_1 ：saturation Q_2 ：saturation
Region IV	$V_{IB} < v_I$	Q_1 ：triode Q_2 ：saturation

2. Example 1

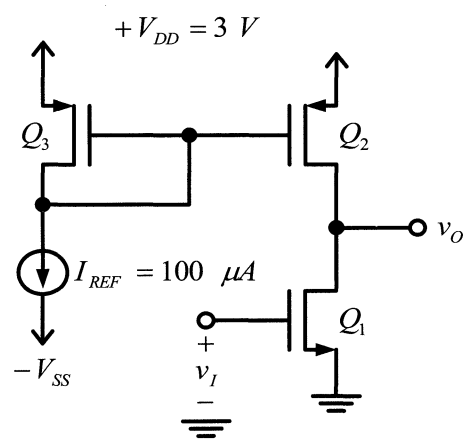
Given $V_{tN}=|V_{tP}|=0.6\ V$、$k_n^{'}=\mu_n C_{ox}=200\ \mu A/V^2$、$k_p^{'}=\mu_p C_{ox}=65\ \mu A/V^2$

Q_N、Q_P：$L=0.4\ \mu m$、$W=4\ \mu m$、$V_{AN}=20\ V$、$|V_{AP}|=10\ V$

問 $A_v=?$、$V_{IA}=?$、$V_{IB}=?$、$V_{OA}=?$、$V_{OB}=?$、

large-signal voltage gain = ?

Sol



假設 Q_1、Q_2 are in saturation region

$$A_v=-g_{m1}\left(r_{o1}\|r_{o2}\right)$$

$$g_{m1}=\sqrt{2k_n^{'}\left(\frac{W}{L}\right)I_{REF}}=0.63\ \ mA/V$$

$$r_{o1}=\frac{V_{AN}}{I_{REF}}=\frac{20}{0.1}=200\ \ k\Omega$$

$$r_{o2}=\frac{V_{AP}}{I_{REF}}=\frac{10}{0.1}=100\ \ k\Omega$$

$$\Rightarrow A_v=-g_{m1}\left(r_{o1}\|r_{o2}\right)=-42\ \ V/V$$

$$V_{OA}=V_{DD}-\left(V_{SG3}-|V_{tP}|\right)=V_{DD}-V_{OV3}$$

$$\Rightarrow I_{REF}=\frac{1}{2}k_p^{'}\left(\frac{W}{L}\right)_3\left(V_{OV3}\right)^2\left(1+\frac{V_{SD3}}{V_{AP}}\right)$$

$$\Rightarrow 0.1=\frac{1}{2}65\left(\frac{4}{0.4}\right)\left(V_{OV3}\right)^2\left(1+\frac{V_{OV3}+0.6}{10}\right)\qquad V_{SD3}=V_{SG3}=V_{OV3}+0.6$$

可得 $V_{OV3}\approx 0.53\ V$

$$\Rightarrow V_{SG3}=V_{OV3}+|V_{tP}|=0.6+0.53=1.13=V_{SG2}$$

$$V_{OA}=V_{DD}-\left(V_{SG}-|V_{tP}|\right)=V_{DD}-V_{OV3}=3-0.53=2.47\ \ V$$

又 $I_{D1}=I_{D2}$　且在 region III 時 Q_1、Q_2 are in saturation region

$$\Rightarrow \frac{1}{2}k_n^{'}\left(\frac{W}{L}\right)_1\left(v_I-V_{tN}\right)^2\left(1+\frac{V_{DS1}}{V_{AN}}\right)=\frac{1}{2}k_p^{'}\left(\frac{W}{L}\right)_2\left(V_{SG2}-|V_{tP}|\right)^2\left(1+\frac{V_{SD2}}{|V_{AP}|}\right)$$

$$\Rightarrow \frac{1}{2}100\left(\frac{4}{0.4}\right)(v_I-0.6)^2\left(1+\frac{v_O}{20}\right)=\frac{1}{2}65\left(\frac{4}{0.4}\right)(1.13-0.6)^2\left(1+\frac{3-v_O}{10}\right)$$

$$\Rightarrow 8.55\times(v_I-0.6)^2=\frac{1-0.08\times v_O}{1+0.05\times v_O}$$

$$\Rightarrow 8.55\times(v_I-0.6)^2=1-0.13\times v_O \quad \because \frac{1-0.08\times v_O}{1+0.05\times v_O}\approx 1-0.13\times v_O$$

$$\Rightarrow v_O=7.69-65.77\times(v_I-0.6)^2$$

在 A 點的時候　$v_O=V_{OA}=2.47\ V$

$$\Rightarrow V_{IA}=0.88\ V$$

在 B 點的時候　$V_{OB}=V_{IB}-V_{tN}=V_{IB}-0.6$

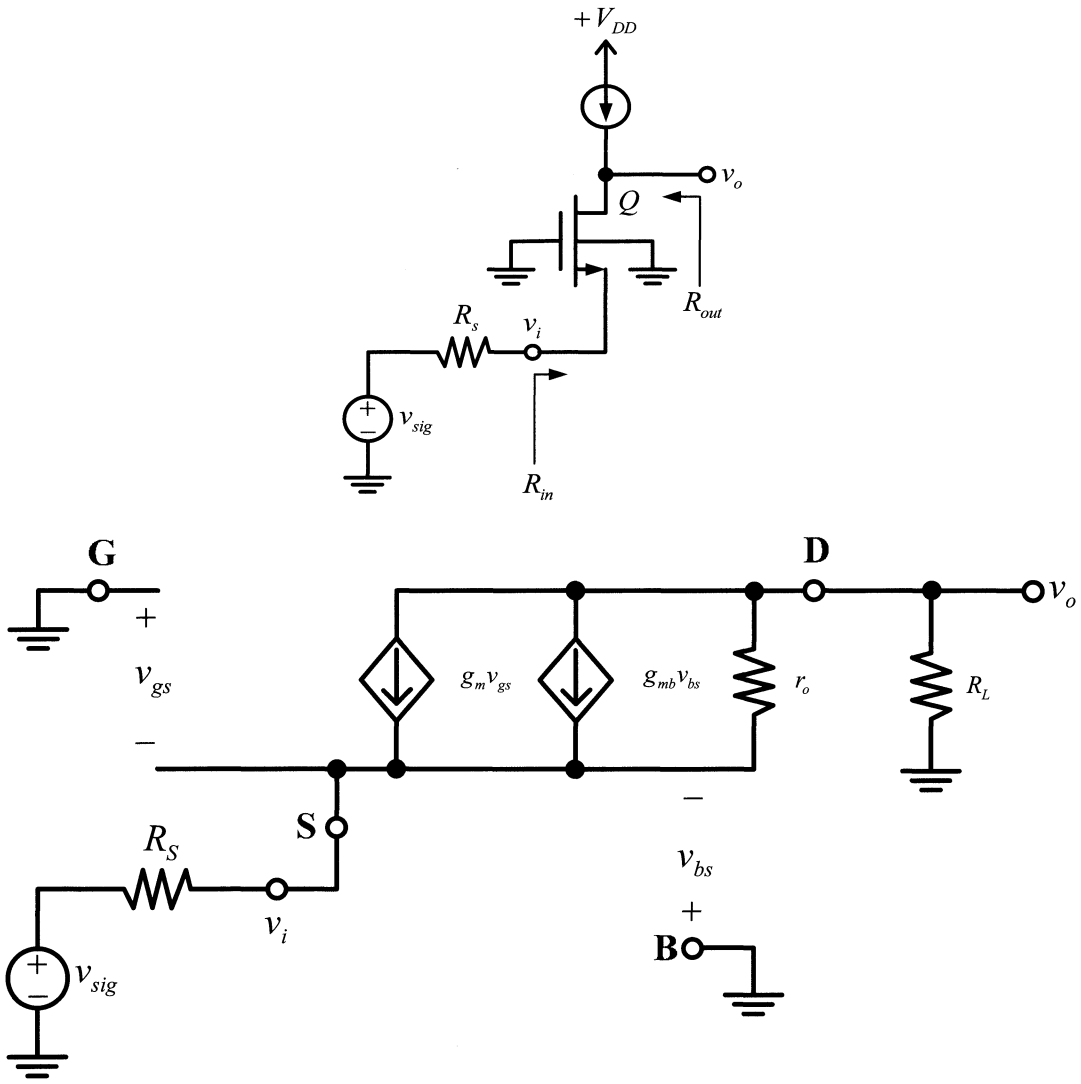
$$\Rightarrow V_{IB}=0.93\ V \ 、\ V_{OB}=0.33\ V$$

Large-signal voltage gain

$$\frac{\Delta v_o}{\Delta v_i}=\frac{0.33-2.47}{0.93-0.88}=-42.8\ V/V$$

⇒大訊號的增益和小訊號的增益大約相等。

3.8.2 CG Amplifier with Active Load



a. $R_{in} = \dfrac{r_o + R_L}{1 + (g_m + g_{mb})r_o}$

$R_i = R_{in}\big|_{R_L=\infty} = \infty$

b. $A_v = \dfrac{v_o}{v_i} = \dfrac{R_L}{R_{in}} = R_L \times \dfrac{[(g_m + g_{mb})r_o + 1]}{r_o + R_L} = A_{vo} \times \dfrac{R_L}{r_o + R_L}$

$A_{vo} = (g_m + g_{mb})r_o + 1$

c. $G_v = \dfrac{v_o}{v_{sig}} = \dfrac{R_L}{R_S + R_{in}} = A_{vo}\dfrac{R_L}{R_L + r_o + A_{vo}R_S}$

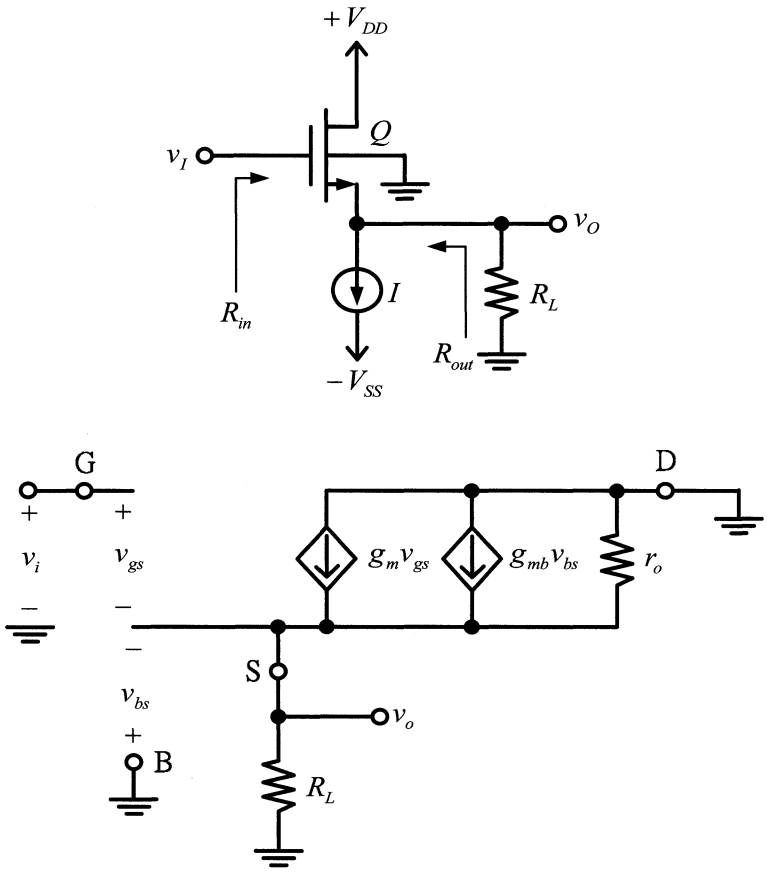
$G_{vo} = G_v\big|_{R_L=\infty} = A_{vo}$

d. $R_{out} = R_S + r_o + (g_m + g_{mb})R_S r_o = r_o + [1 + (g_m + g_{mb})r_o]R_S = r_o + A_v R_S$

$R_o = r_o$

e. 特性 R_i 小 R_o 大 $\Rightarrow$ 可做 current buffer

3.8.3 IC Source Follower



a. $R_{in} = R_i = \infty$

b. $A_v = \dfrac{v_o}{v_i} = \dfrac{g_m R_L^{'}}{1 + g_m R_L^{'}} = \dfrac{R_L^{'}}{1/g_m + R_L^{'}} < 1$ where $R_L^{'} = R_L \| r_o \| \dfrac{1}{g_{mb}}$

$$A_{vo} = A_v\big|_{R_L=\infty} = \frac{g_m r_o}{1 + (g_m + g_{mb}) r_o} \approx \frac{g_m}{g_m + g_{mb}} = \frac{1}{1+\chi} \approx 0.8 \sim 0.9$$

c. $G_v = A_v = \dfrac{g_m R_L^{'}}{1 + g_m R_L^{'}}$

$$G_{vo} = A_{vo} \approx \frac{g_m}{g_m + g_{mb}} = \frac{1}{1+\chi}$$

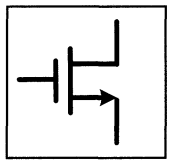
d. $R_{out} = R_o = \left(\dfrac{1}{g_m + g_{mb}} \right) \Big\| r_o \approx \dfrac{1}{g_m + g_{mb}} = \dfrac{1}{g_m (1+\chi)}$

e. 特性 R_i 大 R_o 小 $\Rightarrow$ 可做 voltage buffer

3.9 Depletion –Type MOSFET

此處以 NMOS 為例

◎ enhancemant type 原先無通道 $V_t > 0$



$V_{GS} \le V_t$, *cuttoff* , $i_D = i_S = 0$

$V_{GS} > V_t$, *Q conducting*

(a) *triode*: $V_{DS} < V_{GS} - V_t \; (V_{GD} > V_t)$

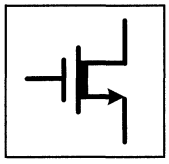
$$i_D = k_n' \left(\frac{w}{L}\right)\left[(V_{GS} - V_t)V_{DS} - \frac{1}{2}(V_{GS} - V_t)^2\right]$$

(b) *saturation*: $V_{DS} \ge V_{GS} - V_t \; (V_{GD} \le V_t)$

$$i_D = \frac{1}{2} k_n' \left(\frac{w}{L}\right)(V_{GS} - V_t)^2$$

◎ depletion type 原先有通道 $V_t < 0$

設 $V_t = -4V$



$V_{GS} \le V_t$, *cuttoff* , $i_D = i_S = 0$

$V_{GS} > V_t$, *Q conducting*

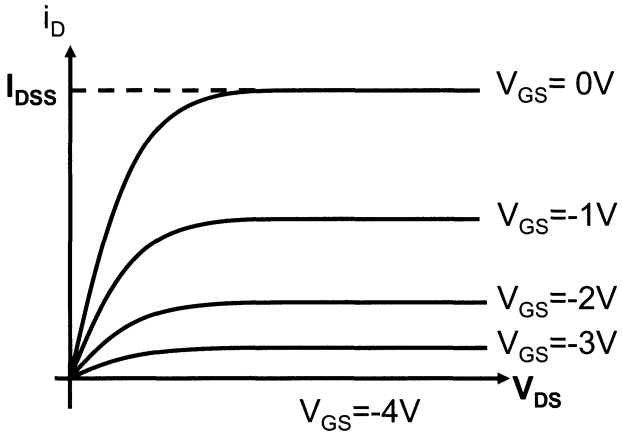
(a) *triode*: $V_{DS} < V_{GS} - V_t = V_{GS} + |V_t|$

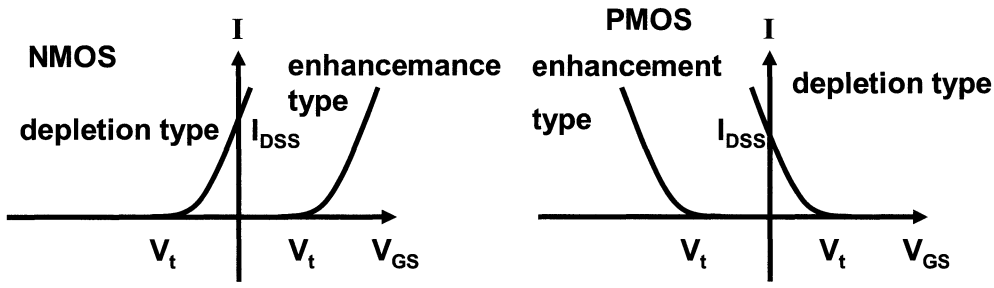
$$i_D = k_n' \left(\frac{w}{L}\right)\left[(V_{GS} - V_t)V_{DS} - \frac{1}{2}(V_{GS} - V_t)^2\right]$$

(b) *saturation*: $V_{DS} \ge V_{GS} - V_t$

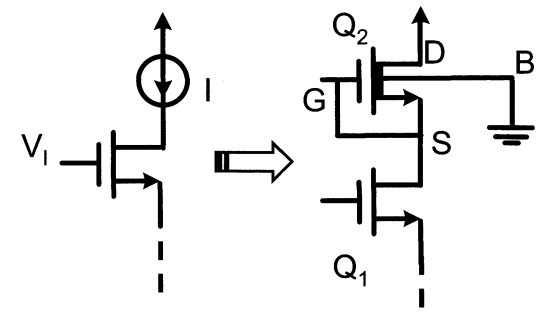
$$i_D = \frac{1}{2} k_n' \left(\frac{w}{L}\right)(V_{GS} - V_t)^2$$

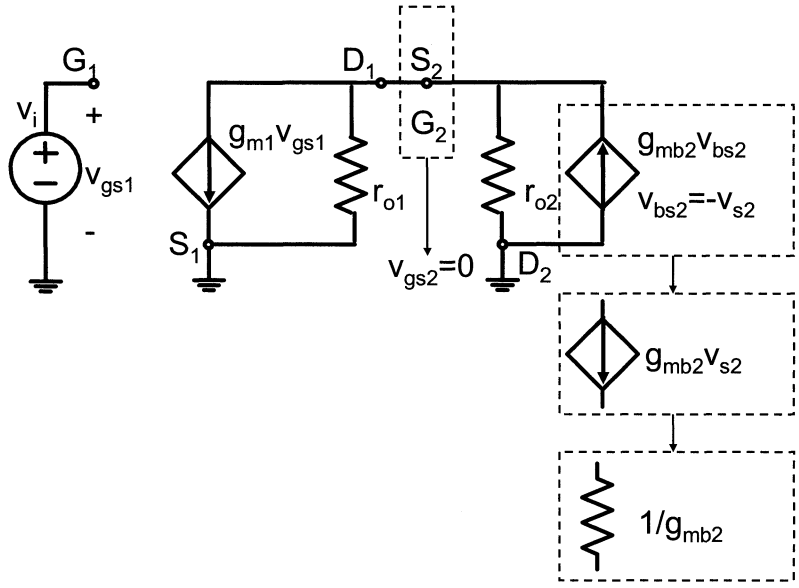
同 enhancemant type 公式，但要注意 $V_t < 0$





◎ 可否取代電流鏡 ？



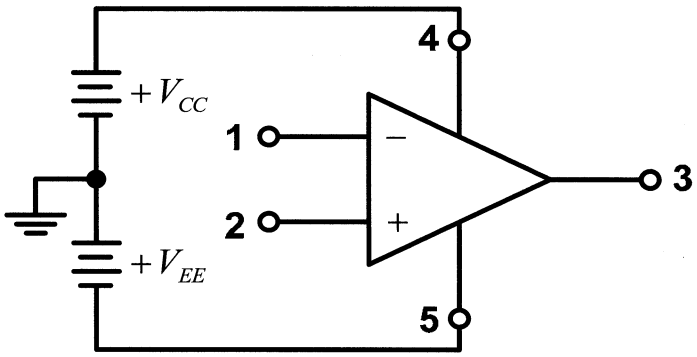


$$A_v = \frac{V_O}{V_I} = -gm_1\left(r_{O1} \,\|\, r_{O2} \,\|\, \frac{1}{gmb_2}\right) \simeq -\frac{gm_1}{gmb_2}$$

Chapter 4 Operational Amplifiers (Op-Amps)

4.1 The Ideal Op-Amp

1. Circuit symbol and terminals



a. Terminal 1: inverting input terminal
b. Terminal 2: noninverting input terminal
c. Terminal 3: output terminal
d. Terminal 4(5): positive (negative) power supply terminal

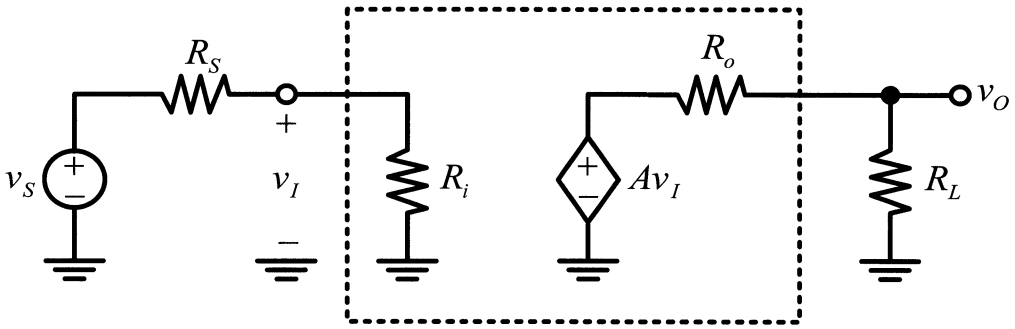
2. Differential signal and common-mode signal:

a. $v_{id} \equiv v_2 - v_1$ differential input signal

b. $v_{icm} \equiv \frac{1}{2}(v_1 + v_2)$ common-mode input signal

c. $\begin{cases} v_{id} = v_2 - v_1 \\ v_{icm} = \frac{1}{2}(v_2 + v_1) \end{cases} \Rightarrow \begin{cases} v_1 = v_{icm} - \frac{v_{id}}{2} \\ v_2 = v_{icm} + \frac{v_{id}}{2} \end{cases}$

3. Ideal op-amp



$\frac{v_O}{v_S} = A \times \frac{R_i}{R_S + R_i} \times \frac{R_L}{R_o + R_L}$ 電壓增益被 R_i 和 R_o 影響。 Non-ideal

Ideal op-amp:

a. Input impedance = ∞ $\Rightarrow R_i = \infty$

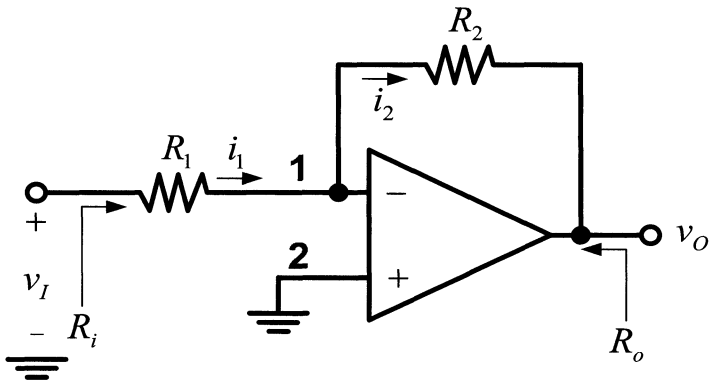
b. Output impedance = 0 $\Rightarrow R_o = 0$

c. Open loop gain = ∞ $\Rightarrow A_d = \infty$

d. Common-mode gain = 0 $\Rightarrow A_{cm} = 0$ (infinite common-mode rejection)

e. Bandwidth = ∞

4.2 The Inverting Configuration



1. Ideal op-amp

a. voltage gain $G \equiv \dfrac{v_O}{v_I} = -\dfrac{R_2}{R_1}$

$v_2 - v_1 = \dfrac{v_O}{A_d} = 0 \quad (\because A_d = \infty) \quad \Rightarrow v_2 = v_1$ (虛擬短路)

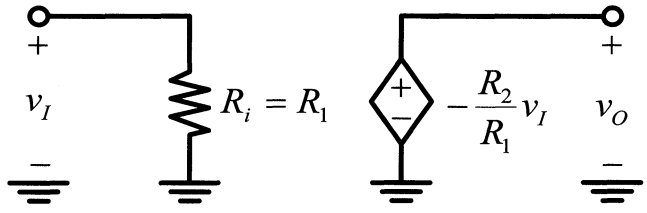
$i_1 = \dfrac{v_I}{R_1} = i_2$

$v_O = -i_2 R_2 = -\dfrac{v_I}{R_1} R_2 \quad \Rightarrow \dfrac{v_O}{v_I} = -\dfrac{R_2}{R_1}$ (inverting)

b. $R_i = R_1$

c. $R_o = 0$

d.



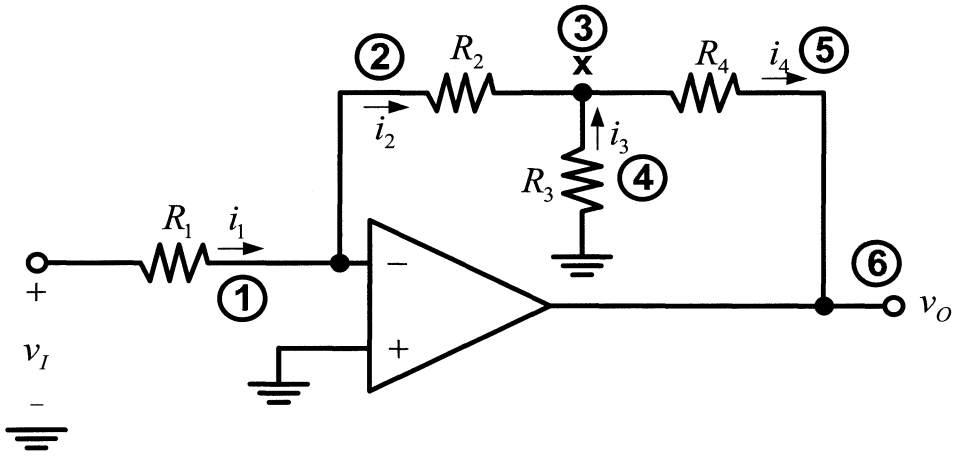
2. Finite A_d

a. voltage gain $G \equiv \dfrac{v_O}{v_I} = -\dfrac{R_2 / R_1}{1 + \left(1 + R_2 / R_1\right) / A_d}$

$$\begin{cases} v_O = -i_2 R_2 + v_1 \cdots (1) \\ v_I = i_1 R_1 + v_1 \quad \cdots (2) \\ i_1 = i_2 \quad \cdots (3) \\ v_1 = \dfrac{-v_O}{A_d} \quad \cdots (4) \end{cases} \Rightarrow \frac{v_O}{v_I} = -\frac{R_2 / R_1}{1 + \left(1 + R_2 / R_1\right) / A_d}$$

b. $R_i = R_1 + \dfrac{R_2}{A_d + 1}$

3. T-network



a. voltage gain $G \equiv \dfrac{v_O}{v_I} = -\dfrac{R_2}{R_1}\left(1 + \dfrac{R_4}{R_2} + \dfrac{R_4}{R_3}\right)$

① $i_1 = \dfrac{v_I}{R_1}$

② $i_2 = i_1 = \dfrac{v_I}{R_1}$

③ $v_x = 0 - i_2 R_2 = -\dfrac{R_2}{R_1} v_I$

④ $i_3 = \dfrac{0 - v_x}{R_3} = \dfrac{R_2}{R_1 R_3} v_I$

⑤ $i_4 = i_2 + i_3 = \dfrac{v_I}{R_1} + \dfrac{R_2}{R_1 R_3} v_I$

⑥ $v_O = v_x - i_4 R_4$

$\Rightarrow \dfrac{v_O}{v_I} = -\dfrac{R_2}{R_1}\left(1 + \dfrac{R_4}{R_2} + \dfrac{R_4}{R_3}\right)$

b.

Design 使得 $R_i = 1\ M\Omega$，$G = -100$

Given 各 $R \le 1\ M\Omega$

Sol:

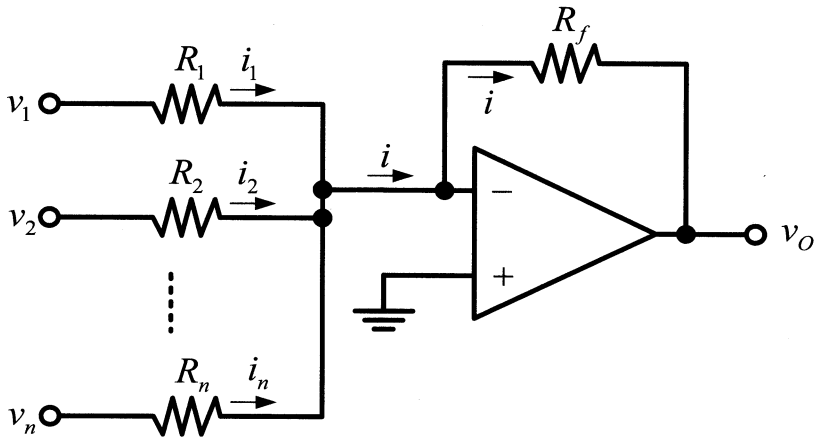
$R_i = R_1 = 1\ M\Omega$

Let $R_2 = R_4 = 1\ M\Omega$

则 $G = -100 = -\frac{1}{1}\left(1 + \frac{1}{1} + \frac{1}{R_3}\right) \Rightarrow R_3 = 10.2\ k\Omega$

4. Application

a. Weighted summer



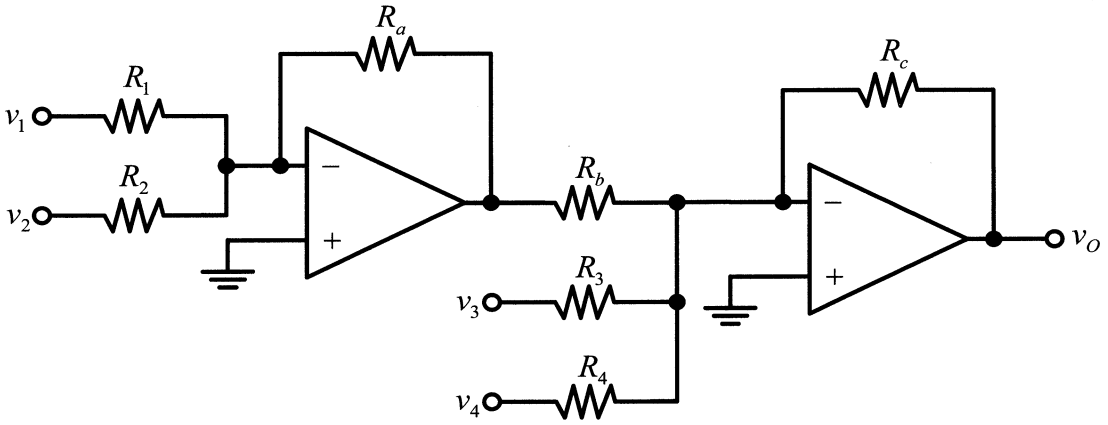
$$i = i_1 + i_2 + \cdots + i_n = \frac{v_1}{R_1} + \frac{v_2}{R_2} + \ldots\ldots + \frac{v_n}{R_n}$$

$$\Rightarrow v_O = -i \times R_f = -\left(\frac{R_f}{R_1}v_1 + \frac{R_f}{R_2}v_2 + \cdots + \frac{R_f}{R_n}v_n\right)$$

If $R_1 = R_2 = \cdots = R_n$

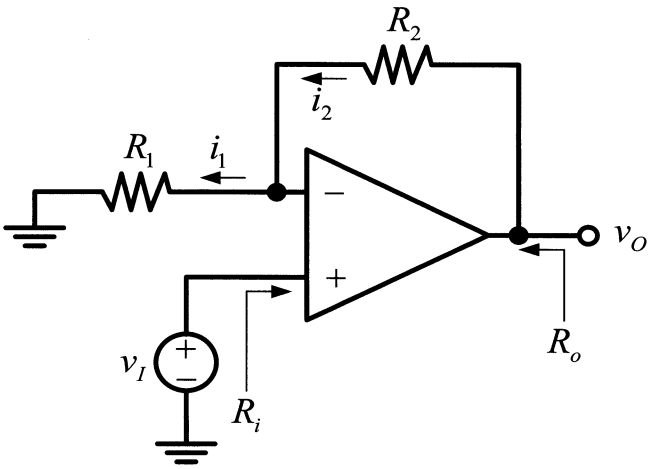
$$\Rightarrow v_O = -\frac{R_f}{R_1}\left(v_1 + v_2 + \cdots + v_n\right)$$

b. Weighted summer with weighting factors of both signs



$$v_O = v_1\left(\frac{R_a}{R_1}\right)\left(\frac{R_c}{R_b}\right) + v_2\left(\frac{R_a}{R_2}\right)\left(\frac{R_c}{R_b}\right) - v_3\left(\frac{R_c}{R_3}\right) - v_4\left(\frac{R_c}{R_4}\right)$$

4.3 The Noninverting Configuration



1. Ideal op-amp

a. voltage gain $G \equiv \dfrac{v_O}{v_I} = 1 + \dfrac{R_2}{R_1}$

$$v^+ - v^- = \frac{v_O}{A_d} = 0 \quad (\because A_d = \infty) \quad \Rightarrow v^+ = v^- = v_I \quad (\text{虚擬短路})$$

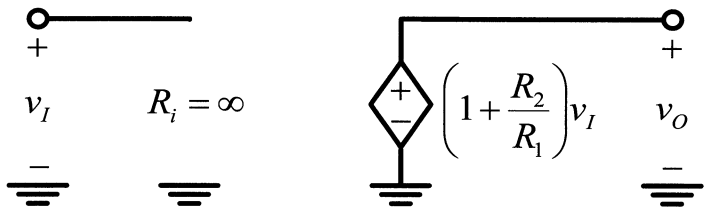
$$i_1 = \frac{v_I}{R_1} = i_2$$

$$v_O = v_I + i_2 R_2 = v_I + \frac{R_2}{R_1} v_I \quad \Rightarrow \frac{v_O}{v_I} = 1 + \frac{R_2}{R_1} \quad (\text{noninverting})$$

b. $R_i = \infty$

c. $R_o = 0$

d.

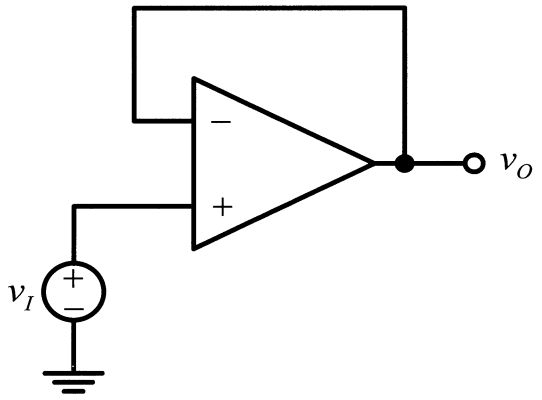


2. Finite A_d

a. voltage gain $G \equiv \dfrac{v_O}{v_I} = -\dfrac{1 + R_2 / R_1}{1 + \left(1 + R_2 / R_1\right) / A_d}$

b. $R_i = \infty$

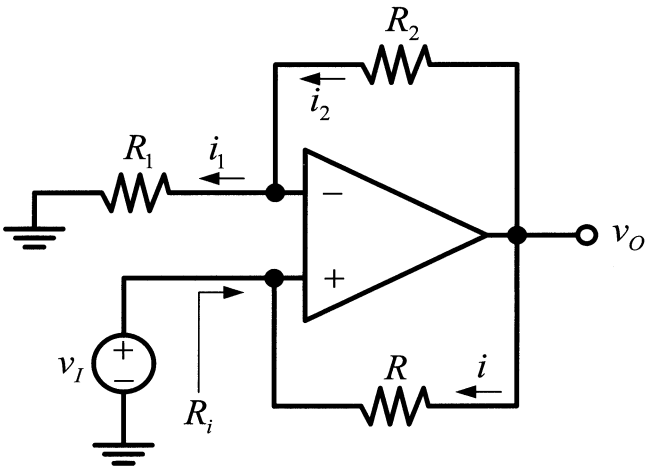
3. Unit gain buffer



a. $A_d = \infty \quad \Rightarrow v_O = v_I$

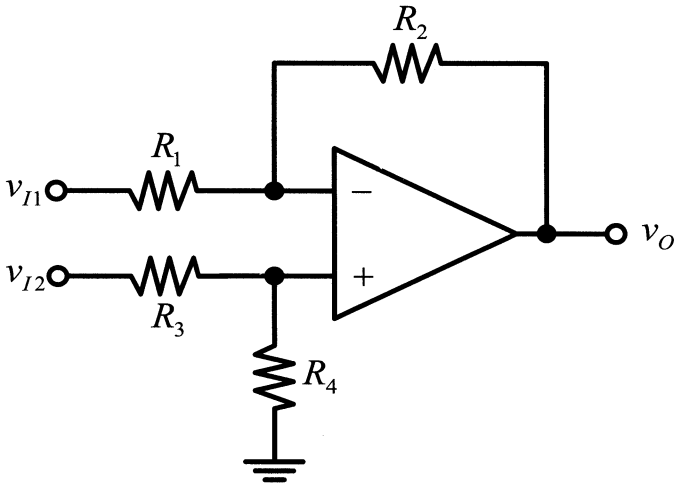
b. Finite $A_d \quad \Rightarrow v_O = \dfrac{A_d}{A_d + 1} v_I$ 或 $\dfrac{v_O}{v_I} = \dfrac{1}{1 + 1/A_d}$

4. Negative impedance converter



$R_i = -\dfrac{R_1}{R_2} \cdot R$ （負電阻）

4.4 Difference Amplifiers



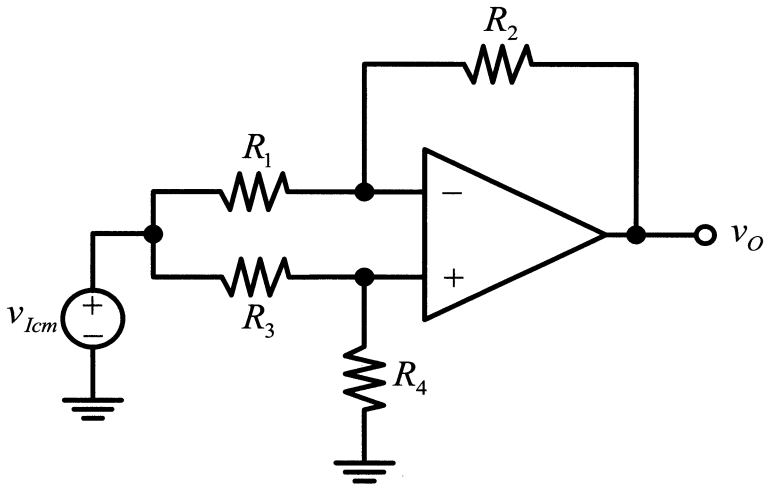
1. Use superposition

a. Differential voltage gain

$$v_O = -\frac{R_2}{R_1}v_{I1} + \left(\frac{R_4}{R_3+R_4}\right)\left(\frac{R_1+R_2}{R_1}\right)v_{I2}$$

Let $\frac{R_2}{R_1} = \left(\frac{R_4}{R_3+R_4}\right)\left(\frac{R_1+R_2}{R_1}\right) \Rightarrow \frac{R_1}{R_2} = \frac{R_3}{R_4}$ 或 $R_1 = R_3$, $R_2 = R_4$

then $v_O = \frac{R_2}{R_1}(v_{I2} - v_{I1})$



b. Common-mode gain

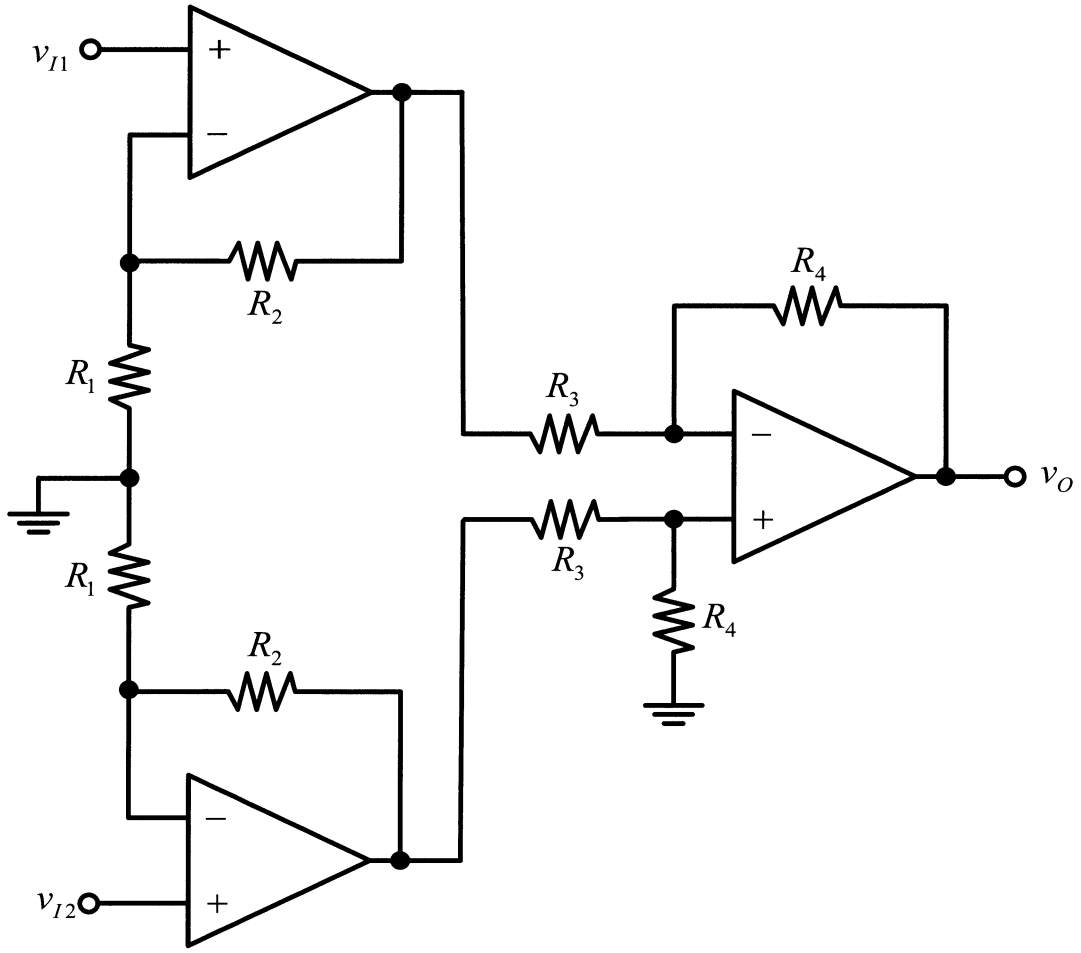
$$v_O = \frac{R_4}{R_3 + R_4}\left(1 - \frac{R_2}{R_1}\frac{R_3}{R_4}\right)v_{Icm}$$

Let $\frac{R_1}{R_2} = \frac{R_3}{R_4} \quad \Rightarrow \frac{v_O}{v_{Icm}} = 0 \quad \Rightarrow A_{cm} = 0$

c. $R_{i1} = R_1 \neq R_{i2} = R_3 + R_4$ （輸入阻抗不一樣）

d. $R_{id} = 2R_1$ （$R_1 = R_3$）

2. Instrumentation amplifier

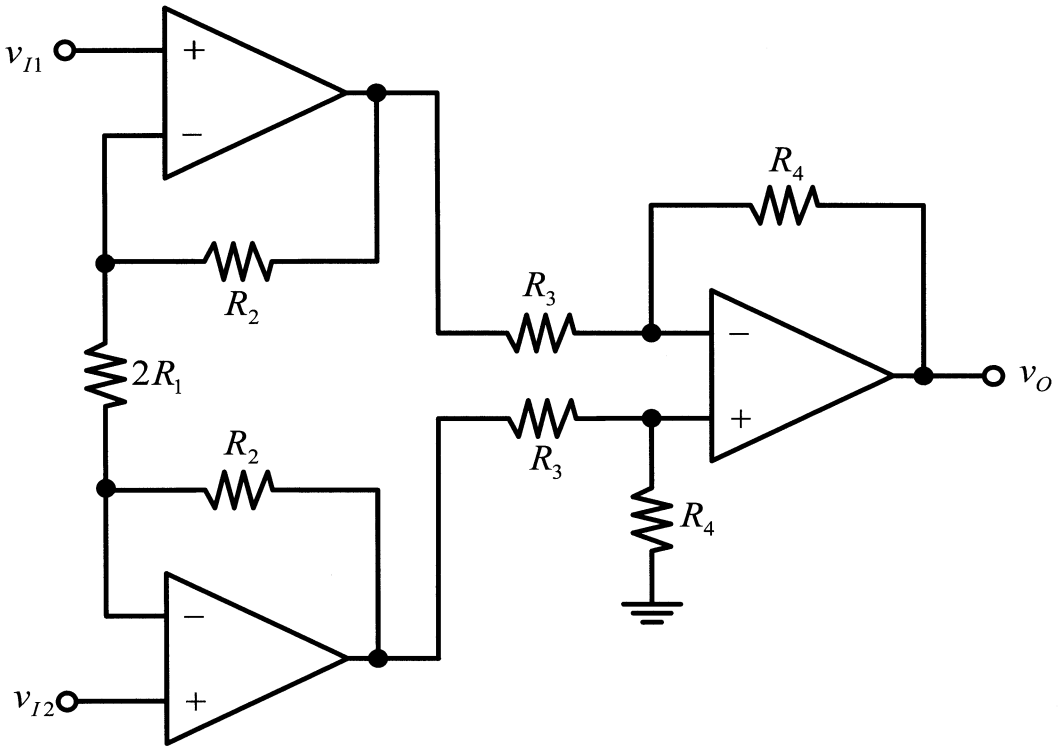


a. $A_d \equiv \frac{v_O}{v_{Id}} = \frac{R_4}{R_3}\left(1 + \frac{R_2}{R_1}\right)$

b. $R_i = \infty$

c. 第一級會將 v_{Icm} 放大 $\left(1 + \frac{R_2}{R_1}\right)$ 倍，容易導致電路飽和。 $\Rightarrow CMRR \downarrow$

3. Improved instrumentation amplifier design



a. $A_d \equiv \dfrac{v_O}{v_{Id}} = \dfrac{R_4}{R_3}\left(1+\dfrac{R_2}{R_1}\right)$

b. $R_i = \infty$

c. 當 $v_{I1} = v_{I2} = v_{Icm}$，將沒有電流流過 $2R_1$，第一級將不放大 v_{Icm}，使得 $v_O = 0$
$\Rightarrow CMRR \to \infty$

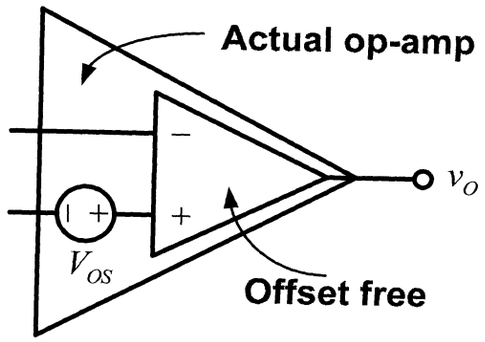
d. 可利用改變 R_1，改變電路差動增益

4.5 DC Imperfection

1. Definition

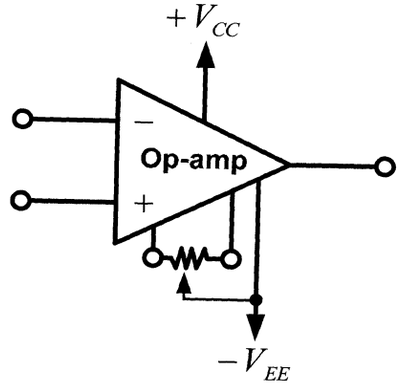
a. Output offset voltage: 當輸入端皆接地時，在輸出端的電壓。

b. Input offset voltage (V_{OS}): 使得輸出電壓為 0 的時候，輸入端電壓的差異值，但正負相反。



c. Input offset voltage drift $= \dfrac{\Delta V_{OS}}{\Delta T}$

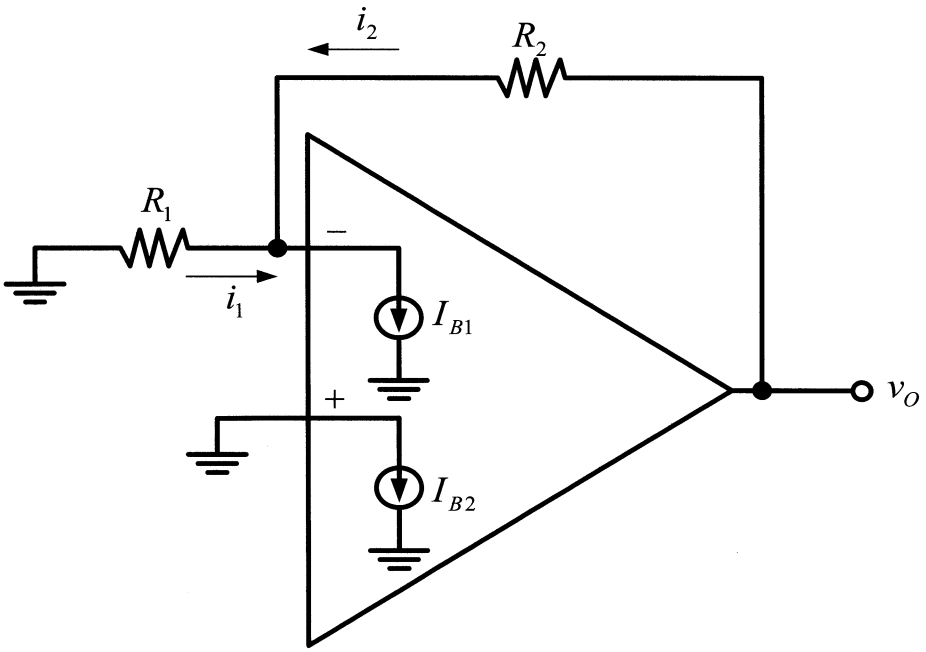
d. Offset-nulling terminal:



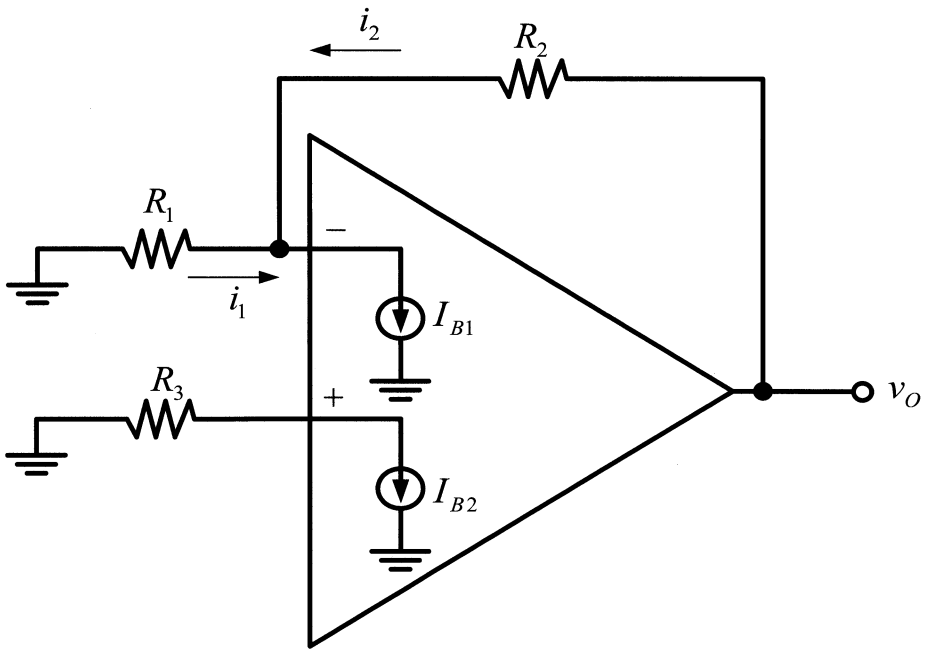
e. Input offset current (I_{OS}): $I_{OS} \equiv I_{B1} - I_{B2}\big|_{v_O=0}$

f. Input offset current drift $= \dfrac{\Delta I_{OS}}{\Delta T}$

2. Input offset current 的影響



a. $i_1 = 0 \quad \Rightarrow v_O = I_{B1} \cdot R_2 \neq 0$



b. $v_O = \left(I_{B1} - \dfrac{I_{B2} R_3}{R_1} \right) R_2 - I_{B2} R_3$

If $I_{OS} = 0 \quad \Rightarrow \quad I_{B1} = I_{B2} = I_B \quad \Rightarrow v_O = I_B \left[R_2 - R_3 \left(1 + \dfrac{R_2}{R_1} \right) \right]$

When $R_3 = R_1 \| R_2 \quad \Rightarrow v_O = 0$

c. If $I_{OS} \neq 0$

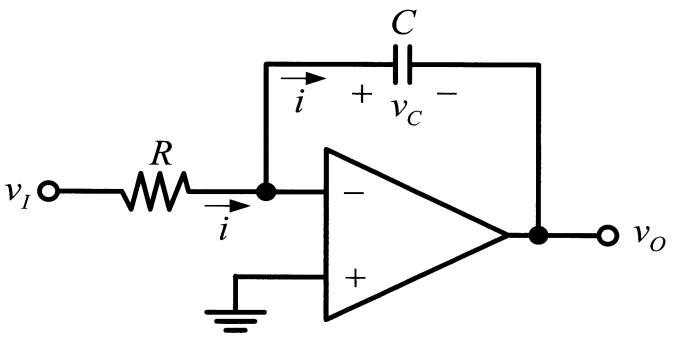
Let $I_B = \frac{1}{2}(I_{B1} + I_{B2})$

$\Rightarrow I_{B1} = I_B + \frac{I_{OS}}{2}$, $I_{B2} = I_B - \frac{I_{OS}}{2}$

則 $v_O = I_{OS} \cdot R_2 \neq 0$ （由 $v_O = I_{B1} \cdot R_2$ 降為 $v_O = I_{OS} \cdot R_2$）

4.6 Integrators and Differentiators

1. Integrators



a. $v_O(t) = -V_C - \frac{1}{RC}\int_0^t v_I(t)\,dt$

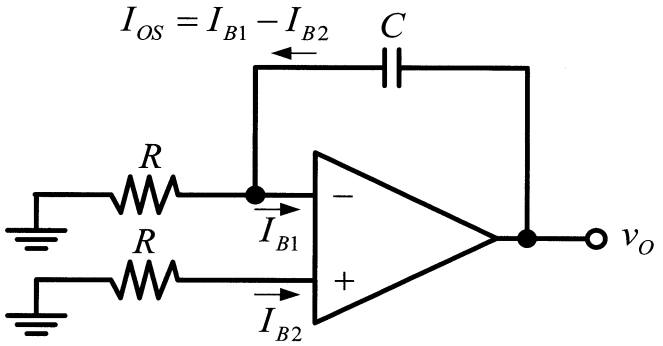
b. RC = integrator time constant

c. Input offset effect

① Input offset voltage

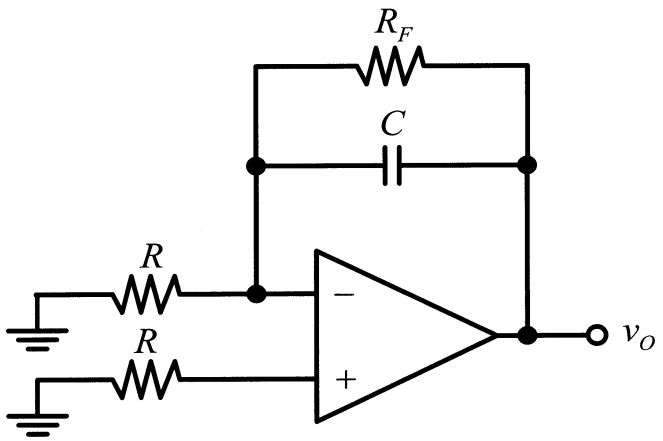
$$A = -\frac{Z_2}{Z_1} = -\frac{\infty}{R} = -\infty \quad (v_O \text{趨向飽和})$$

② Input offset current



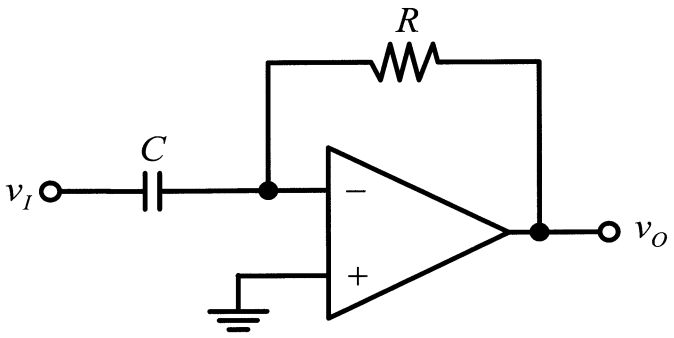
$$v_O(t) = -I_{B2}R + \frac{I_{OS}}{C}t$$

d. Solution



$$\Rightarrow v_O = V_{OS}\left(1+\frac{R_F}{R}\right)+I_{OS}\cdot R_F \quad \text{(非理想的積分器)}$$

2. Differentiators

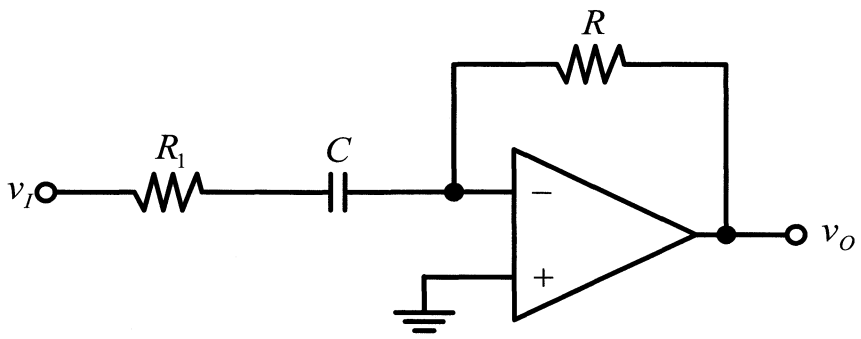


a. $v_O = -RC\cdot\dfrac{dv_I}{dt}$

b. 頻率 $f\uparrow \Rightarrow A_v = \dfrac{-R}{0} \rightarrow -\infty$

將會放大高頻的 noise，導致電路飽和。 (noise magnifier)

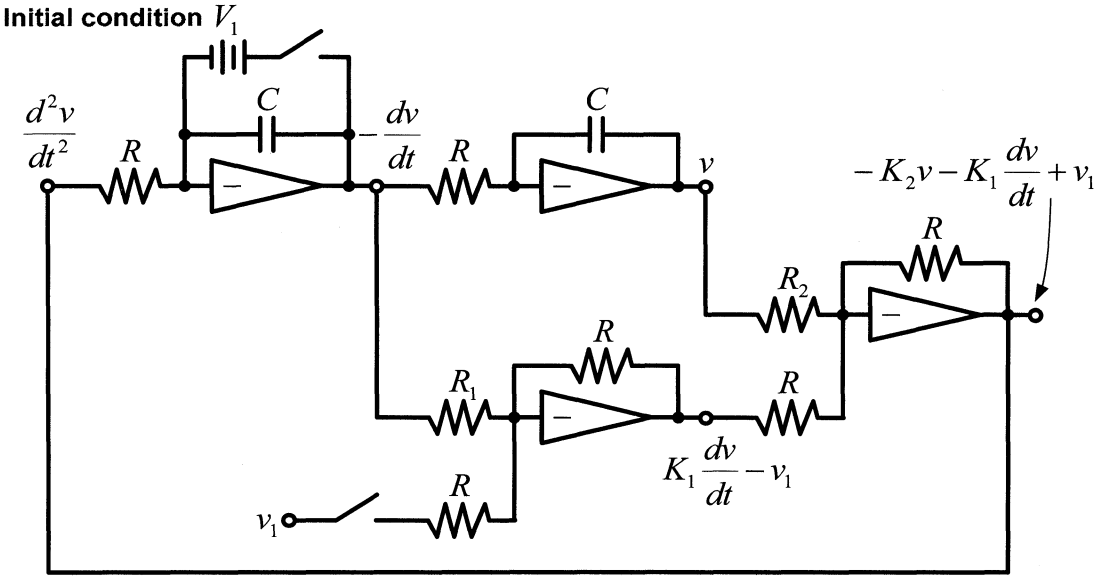
c. Solution



將高頻的增益降為 $-\frac{R}{R_1}$ (非理想的微分器)

3. Analog computation

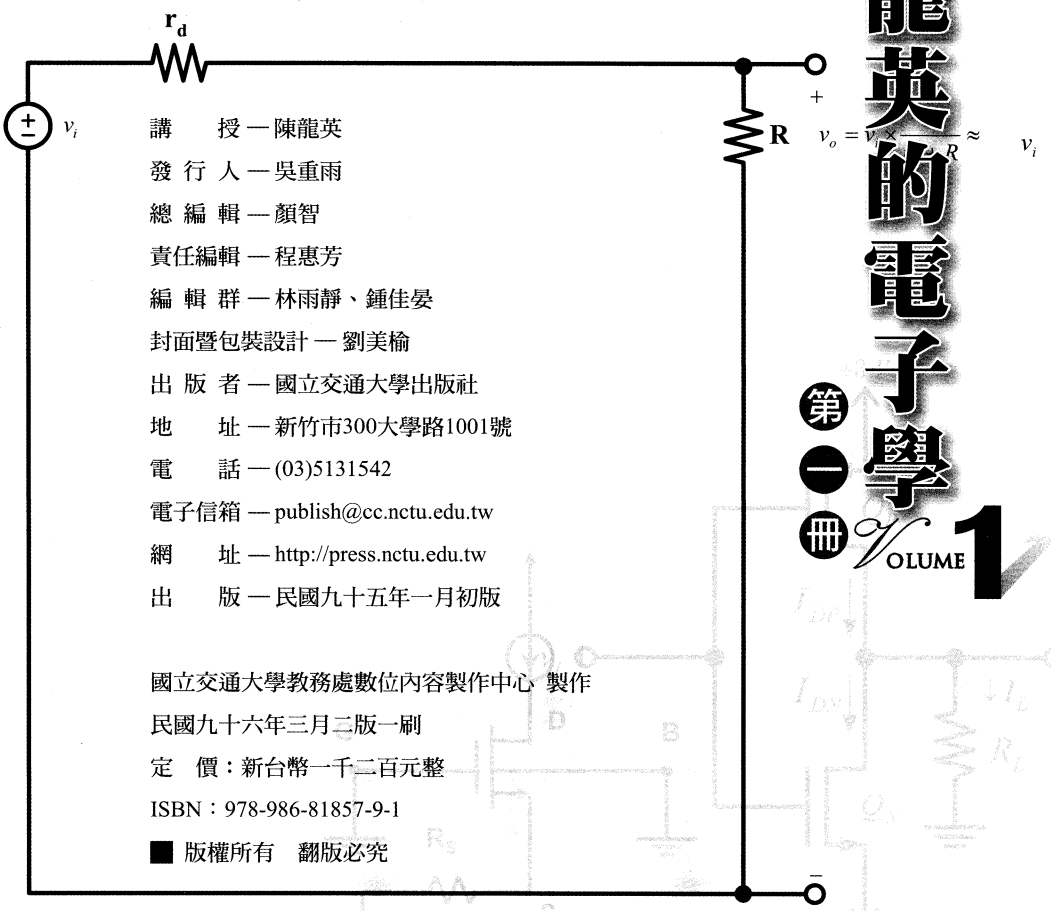
$$\frac{d^2v}{dt^2}+K_1\frac{dv}{dt}+K_2v-v_1=0$$



where $\frac{1}{RC}=1$, $\frac{R}{R_1}=K_1$, $\frac{R}{R_2}=K_2$

陳龍英的電子學

第一冊 VOLUME 1



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