Delta-Sigma Analog-to-Digital Conversion via Time-Mode Signal Processing

Christopher S. Taillefer, *Student Member, IEEE* and Gordon W. Roberts, *Fellow, IEEE*

***Abstract*—A signal processing methodology is proposed that performs delta-sigma (ΔΣ) analog-to-digital conversion on voltage signals while implementing all the circuits in a digital CMOS logic style. This methodology, called time-mode signal processing, uses time-difference variables as an intermediate signal between the input voltage and digital output. The resulting low cost silicon devices offer very compact, low power, high-speed, and robust analog-to-digital converter (ADC) alternatives. A first-order ΔΣ ADC is implemented using this methodology. Two integrated circuits were fabricated in a 0.18-µm CMOS technology to demonstrate the feasibility of the time-mode ΔΣ ADC approach. The first IC implements a single-ended input design while a differential design was fabricated in the second IC. Experimental results reveal that these devices can achieve 7 – 9-bit resolutions within 125 – 400 kHz bandwidths, while occupying areas smaller than 50 µm x 50 µm and consuming less than 800 µW.**

***Index Terms*—Analog-to-digital conversion, CMOS, delta-sigma modulation, low power, small area, time-mode signal processing.**

I. Introduction

Digital design is the driving force for the rapidly emerging deep submicron CMOS technologies. As such, CMOS processes are typically optimized for the needs of digital circuitry. In other words, CMOS technologies are being developed to improve digital switching speeds, lower the supply voltages, and reduce transistor geometries to increase the packing density of digital circuits. These pursuits have pushed the processing of digital information into the gigahertz frequency range. The need for digital, analog, and mixed-signal circuits to be integrated on a single die (i.e. System-on-Chip) is escalating as companies struggle to drive down cost, boost productivity, and create lower power and smaller devices.

There are many challenges in integrating analog and mixed-signal circuits in state-of-the-art digital CMOS technologies. As emerging CMOS technologies reduce feature size dimensions, transistor gate oxide thickness reduces forcing the system voltage to decrease. This negatively impacts analog and mixed-signal circuit performance by exercising transistors at non-optimal operating points and permitting currents to leak through transistor gates. This dilemma results in reduced input voltage swings and linearity problems for the processing of analog voltage signals. To upset the design challenge even further, area and power budgets are at best being preserved if not reducing. Additional implementation challenges are imposed when analog and mixed signal processing functions must coexist with digital circuits. The switching noise from the digital circuitry may couple into the analog blocks thus corrupting analog information.

In order to offset some of the analog-to-digital converter (ADC) design challenges imposed by digitally-driven deep submicron CMOS processes, a potential candidate to replace conventional voltage signal processing is being investigated, referred to as time-mode signal processing or TMSP. Although the concept of TMSP is fairly new, several works have begun to investigate its potential in many applications [1] – [13] including analog-to-digital (A/D) conversion. More recently, a continuous-time multi-bit sigma-delta converter has been proposed that makes use of time encoding in the feedback path [1]. This approach may simplify the requirements of the quantizer, especially in low-voltage technologies.

For instance, the basic operation of converting voltage into time is explored in [2]. A voltage comparator is implemented in [3] by converting voltage into a time difference via a voltage controlled delay circuit and is then compared using a time-to-digital converter. In [4] an analog voltage is used to control the propagation delay of a chain of inverters while modulating the period of an oscillator which is then converted into a digital representation. The work presented in [5] uses a voltage-tunable differential delay line to implement a time-to-digital converter together with the application of a time amplifier [6]. A single-slope ADC is implemented in [7] by integrating a voltage-controlled current onto a capacitor and quantizing its charging time. In [8] the time difference between two pulse edges is being integrated onto a capacitor which is then converted by a comparator into a new time difference whose value corresponds to a sum or difference of the two input signals. Another technique appearing in the literature is one that uses a voltage to control the oscillation period of a VCO which is then applied to a phase quantizer that produces a square wave output whose frequency is proportional to the input voltage. In [9] a counter is used to count the number of edges in a given time period resulting in a white quantization spectrum. In contrast [10], [11], and [12] use a differentiator which gives rise to a noise shaped quantization spectrum.

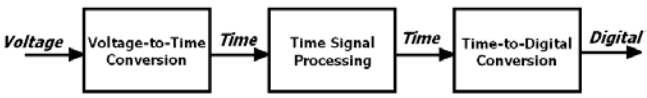


Fig. 1. Analog-to-digital conversion process via time-mode signal processing.

The A/D conversion process using the TMSP methodology is depicted in Fig. 1. Since most information begins in the form of a voltage, a voltage-to-time converter (VTC) is employed to convert the input signal into a time-difference signal. The time signal is then processed by various circuits resulting in an output time signal. Finally, the processed time signal is transformed into a digital representation using a time-to-digital converter (TDC).

Delta-sigma (ΔΣ) analog-to-digital conversion is a great candidate to be implemented with TMSP [13]. The circuits involved in the time-mode ΔΣ ADC (hereafter referred to as TMΔΣADC) are comprised of a digital CMOS construction. Therefore, this system offers all the benefits of the digital CMOS technology. Specifically, the TMΔΣADC will operate at high speeds, consume low power, and occupy small silicon area. Moreover, these performance specifications will improve with newer and smaller digitally-driven CMOS technologies.

This paper documents the new methodology with the following organization: in Section II the time-mode signal processing circuit blocks are described. The TMΔΣADC architecture is presented in Section III. Section IV demonstrates the mathematical modeling of the TMΔΣADC using MATLAB. The implementation and experimental results are discussed in Section V and VI. Finally, a comparison of the TMΔΣADC designs is presented in Section VII. Section VIII summarizes the work presented and discusses options to improve the TMΔΣADC performance.

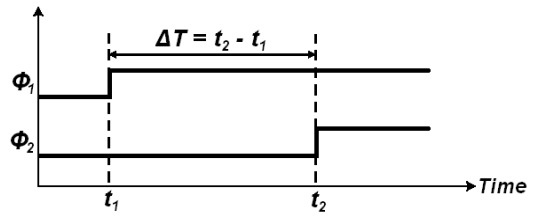


Fig. 2. Timing diagram example demonstrating a time-difference variable ΔT as the difference between two digital clock rising edge transition times.

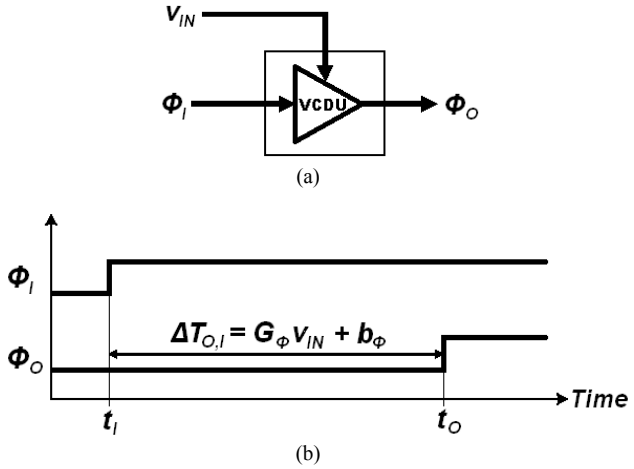


Fig. 3. Voltage-controlled delay unit (VCDU) (a) block diagram; (b) example timing diagram over linear operation.

II. Time-Mode Signal Processing Circuits

Time-mode signal processing (TMSP) may be defined as the detection, storage, and manipulation of sampled analog information using time-difference variables. Furthermore, we define a time-difference variable, ΔT, as the quantity of time between an event occurring with respect to a reference time or event. In the context of this work, a time-difference variable refers to the time interval between two digital clock edges. Fig. 2 demonstrates two digital clock signals, ϕ_1 and ϕ_2, and the time-difference variable, ΔT, represented as the time interval between the two clock-edge-transition times t_1 and t_2. Note that time-difference variables are discrete samples of analog information. Time-difference variables will be synonymously interchanged with time-mode signals. The circuit blocks used to implement the TMSP process, illustrated in Fig. 1, are described in the following subsections.

A. Voltage-Controlled Delay Unit

The process of voltage-to-time conversion is facilitated using a device called a voltage-controlled delay unit (VCDU). It is a circuit that proportionally delays an input time event (i.e. a clock edge) with respect to a sampled input voltage. The VCDU block diagram that will be used throughout this work is illustrated in Fig. 3(a). Regardless of its implementation, a VCDU has two inputs; an input event ϕ_I that has a low-to-high transition at time t_I and the sampled input voltage v_{IN} that controls the time of the low-to-high transition of the output event ϕ_O denoted by t_O. There are two ways to interpret the output of the VCDU: physically or conceptually. The physical output ϕ_O of the VCDU is a digital signal. The conceptual VCDU output is the time the output transition occurs with respect to the input transition time. Mathematically, we can write this relationship as follows

$$t_O = t_I + f(v_{IN}). \tag{1}$$

Assuming the VCDU operates within the linear region of the VCDU, the above functional relationship can be written as

$$t_O = t_I + G_\phi v_{IN} + b_\phi, \tag{2}$$

where G_ϕ and b_ϕ is the slope and y-intercept of a line drawn through the linear region of the VCDU transfer characteristic. Rearranging (2) we can express the VCDU input-output delay behavior or time-difference as

$$\Delta T_{O,I} = t_O - t_I = G_\phi v_{IN} + b_\phi. \tag{3}$$

Here we use $\Delta T_{O,I}$ to indicate the time-difference between the output signal relative to the input signal. Fig. 3(b) highlights the VCDU input-output delay as a linear function of the input signal.

VCDUs may be implemented in a variety of ways, some of which are described in [14] – [17]. A CMOS transistor

schematic of a current-starved inverter VCDU is shown in Fig. 4(a). When the input signal ϕ_I is low, capacitor C is set to the supply voltage forcing the output ϕ_O to reset to a logic low value. On the rising edge of the input signal capacitor C begins to discharge through the NMOS transistors M3 and M4 at a rate that is governed by the input voltage v_{IN}. The output inverter (M5 and M6) acts as the comparator and senses when the capacitor voltage has surpassed the inverter threshold voltage. Correspondingly, a low-to-high transition is created at the output of the VCDU whose transition time is controlled by v_{IN}. Conversely, when a high-to-low transition occurs at the input, the output will experience a high-to-low transition shortly afterwards which is ideally independent of the control voltage v_{IN}. We shall denote this delay as τ_{VCDU}.

A typical SPICE simulation of the input-output low-to-high transition transfer characteristic of a current-starved inverter VCDU is shown in Fig. 4(b). The circuit was simulated using HSPICE with BSIM3 models for a standard 1.8-V, 0.18-µm CMOS process proprietary to the Taiwan Semiconductor Manufacturing Corporation (TSMC). As is evident from the SPICE results, the linear region for this device lies between 0.8 V and 1.2 V with a maximum linearity error of ±0.15%. The voltage-to-time conversion factor G_ϕ and the y-intercept b_ϕ was determined to be -320 ps/V and 1125 ps, respectively. The average power consumption was extracted as 136 µW while operating at 150 MHz. A maximum conversion time of 900 ps is observed resulting in a maximum operating frequency of 1.1 GHz.

Control of the voltage-to-time gain factor, y-intercept, conversion time, and power is set by the value of capacitor C and the size of the voltage-controlled NMOS transistor M3. The VCDU designs used throughout this work were implemented without a capacitor thus operating with the transistor's parasitic capacitance. The W/L ratios for transistors M3 and M4 were respectively implemented as 0.5 µm / 4 µm and 1 µm / 0.5 µm.

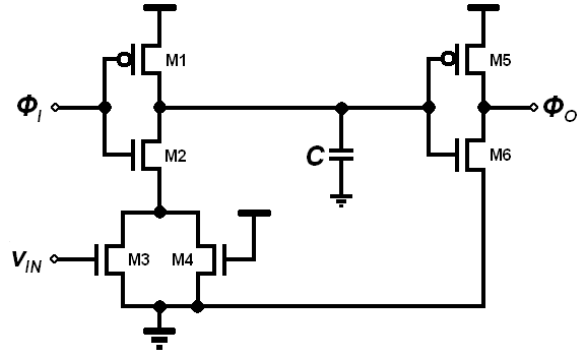
Sample-and-hold circuits are required in A/D conversion when the input voltage is a relatively high-frequency signal with respect to the ADC conversion process. Hence, a VCDU may act as a sampler provided its conversion time is sufficiently less than the period of the input signal. We can determine when a sample-and-hold circuit may be omitted by observing a sinusoidal input voltage signal expressed as

$$v_{IN}(t) = A\sin(2\pi f_{IN} t), \tag{4}$$

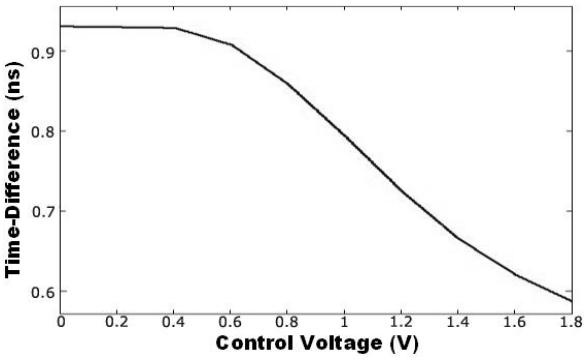
where A is the peak amplitude and f_{IN} is the maximum signal frequency. The maximum slope is calculated at the zero crossing and is given by

$$\left.\frac{dv_{IN}}{dt}\right|_{\max} = 2\pi A f_{IN}. \tag{5}$$

Let T_C represent the maximum conversion time of the VCDU. That is, T_C is the largest time difference between the input and output digital edges for any input voltage. In order to avoid



(a)



(b)

Fig. 4. Current-starved inverter VCDU (a) transistor schematic; (b) input-output low-to-high transition transfer characteristics obtained through a HSPICE simulation.

errors in the sampling, the input voltage cannot change more than one least significant bit (LSB) step V_{LSB} within the conversion time T_C. This imposes an upper limit on the maximum voltage change (i.e. maximum slope), such that

$$\left.\frac{dv_{IN}}{dt}\right|_{\max} = 2\pi A f_{IN} \le \frac{V_{LSB}}{T_C}. \tag{6}$$

The LSB voltage step that a converter is designed to detect may be expressed as

$$V_{LSB} = \frac{FS}{2^D - 1}, \tag{7}$$

where D is the number of bits the converter should resolve and FS is the full-scale voltage which is equal to two times the signal amplitude. Combining and rearranging (6) and (7) while assigning $FS = 2 \cdot A$ results in the expression

$$f_{IN} \le \frac{1}{\pi(2^D - 1)T_C}. \tag{8}$$

This inequality dictates whether or not a sample-and-hold circuit is required based on the desired resolution D, the maximum VCDU conversion time T_C, and input signal bandwidth f_{IN}. Note that harmonic distortion will result if the signal bandwidth violates this inequality.

The following example is offered to illustrate this limitation. Suppose that a 10-bit resolution is required. The previously described current-starved inverter VCDU design had a

maximum conversion time of 900 ps. Therefore, according to (5), if the signal bandwidth is smaller than 342 kHz, then the current-starved inverter can act as a sampler.

B. Voltage-to-Time Converter

A voltage-to-time converter (VTC) is required to transform voltage information into time-mode signals. In all signal processing circuitry voltage signals are measured with respect to an analog ground voltage reference V_{REF}. Moreover, in single-voltage power supply technologies the analog ground is usually a voltage greater than zero. In order to perform a similar approach in the time domain, we make use of two VCDU circuits as shown in Fig. 5(a). The top VCDU converts the input voltage v_{IN} into a time-transition variable which is then compared to the reference signal generated by the bottom VCDU driven by a voltage reference signal V_{REF}.

The VTC operation is illustrated in the timing diagram of Fig. 5(b) whereby the input clock event ϕ_I is delayed with respect to the input controlling voltages v_{IN} and V_{REF}, resulting in the respective VCDU output low-to-high transition times t_O and t_{REF}. Mathematically, we can write these two outputs as

$$t_O = t_I + G_\phi v_{IN} + b_\phi \tag{9}$$

and

$$t_{REF} = t_I + G_\phi V_{REF} + b_\phi . \tag{10}$$

Defining the output of the differential VTC as ΔT_O, that is, the time difference measured with respect to the reference time, we subtract (10) from (9) and write

$$\Delta T_O = t_O - t_{REF} = G_\phi (v_{IN} - V_{REF}) . \tag{11}$$

Finally, in much the same way voltage signals are compared to an analog ground reference, we can denote the input voltage difference as follows

$$v_{in} = v_{IN} - V_{REF} . \tag{12}$$

Subsequently, we can write (11) as

$$\Delta T_O = G_\phi v_{in} . \tag{13}$$

Mismatch between VCDUs in a VTC will cause offset delay errors, which manifest themselves as input-referred voltage offsets provided that the signals remain in the linear operating region of the VCDUs.

C. Voltage-to-Time Integrator

Voltage-to-time integration may be implemented by connecting the VCDU outputs to their respective inputs through an inverter. This circuit is equivalent to a voltage-controlled ring oscillator and is depicted in Fig. 6(a). Writing the low-to-high transition time equations for each VCDU as a function of the sampling instance n, we can write

$$t_O(n) = t_I(n-1) + G_\phi v_{IN}(n-1) + b_\phi \tag{14}$$

and

$$t_{REF}(n) = t'_I(n-1) + G_\phi V_{REF} + b_\phi . \tag{15}$$

Furthermore, the feedback path established by the inverter allows us to state

$$t_I(n-1) = t_O(n-1) + \tau_{VCDU} + 2\tau_{INV} \tag{16}$$

and

$$t'_I(n-1) = t_{REF}(n-1) + \tau_{VCDU} + 2\tau_{INV} , \tag{17}$$

where τ_{INV} is the average propagation delay through the inverters and $\tau_{VCDU}+2\tau_{INV}$ is the total propagation delay of a low-to-high transition at the VCDU output back to its input as a low-to-high transition. As is evident, this delay is independent of the VDCU control voltage. Combining (14) and (16) we can write

$$t_O(n) = t_O(n-1) + G_\phi v_{IN}(n-1) + b_\phi + \tau_{VCDU} + 2\tau_{INV} . \tag{18}$$

Likewise, combining (15) and (17) we can write

$$t_{REF}(n) = t_{REF}(n-1) + G_\phi V_{REF} + b_\phi + \tau_{VCDU} + 2\tau_{INV} . \tag{19}$$

Finally, subtracting (19) from (18), we obtain the difference equation of the voltage-to-time integrator with respect to the reference time $t_{REF}(n)$ and obtain

$$\Delta T_O(n) = \Delta T_O(n-1) + G_\phi [v_{IN}(n-1) - V_{REF}], \tag{20}$$

or, with $v_{in}(n) = v_{IN}(n) - V_{REF}$, we obtain

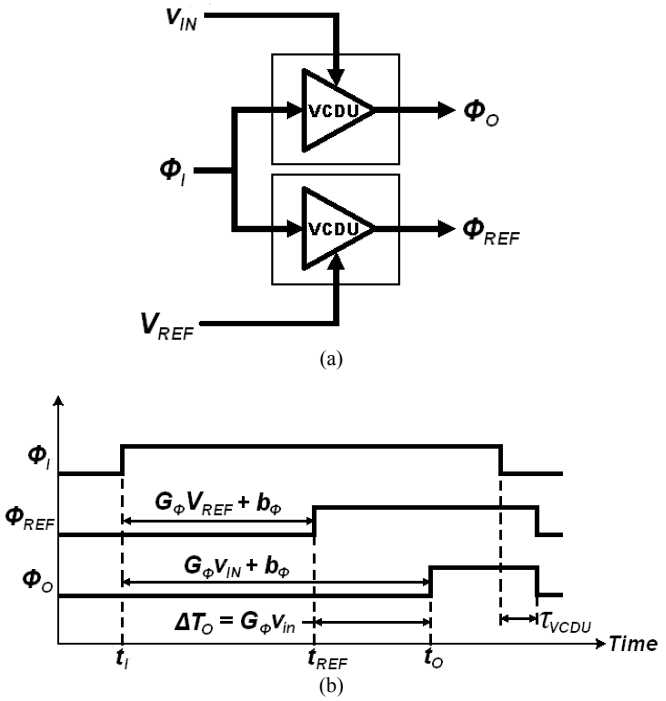


Fig. 5. Voltage-to-time converter (VTC) (a) block diagram; (b) timing diagram illustrating the VTC operation.

$$\Delta T_O(n) = \Delta T_O(n-1) + G_\phi v_{in}(n-1). \quad (21)$$

A timing diagram demonstrating three samples of the operation of the voltage-to-time integrator is presented in Fig. 6(b). The initial integrator output time-difference $\Delta T_O(0)$ is assumed equal to zero. The next output time-difference $\Delta T_O(1)$ is shown proportional to the input voltage at time instance $n=0$. The proceeding output $\Delta T_O(2)$ is the sum of the previous output $\Delta T_O(1)$ and the input voltage $v_{in}(1)$ scaled by G_ϕ.

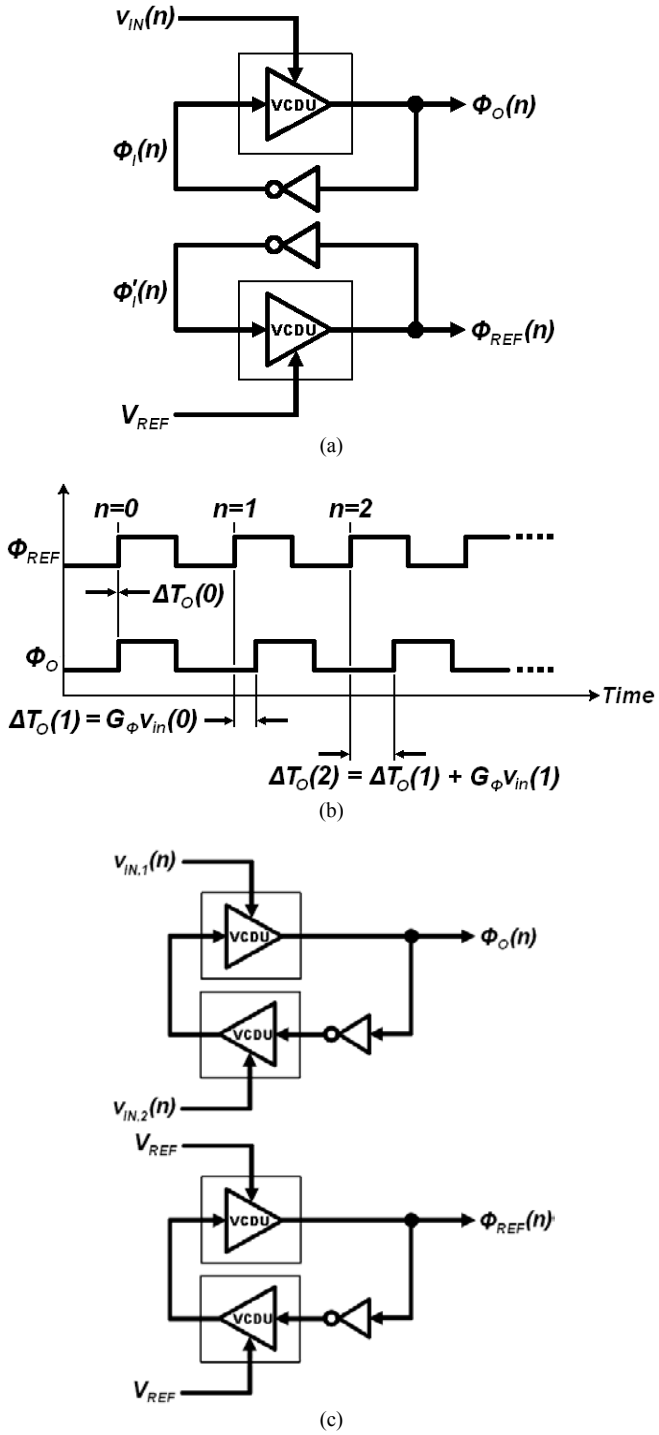


Fig. 6. Voltage-to-time integrator (a) block diagram; (b) timing diagram; (c) dual-input block diagram.

Note that there is no external clock signal in this design; it is a free-running or self-clocking system. Device sizing and input signal levels establish the oscillation frequency.

A dual-input or multi-input integrator may be created by including two or more VCDUs in the oscillating loop. Fig. 6(c) illustrates a dual-input integrator with controlling voltages $v_{IN,1}(n)$ and $v_{IN,2}(n)$. A second oscillator, controlled by reference voltages V_{REF}, is included to generate the reference time. Following along the same lines of reasoning for the single input integrator, we can write the difference equation for the dual-input integrator with respect to the reference time $t_{REF}(n)$ as

$$\Delta T_O(n) = \Delta T_O(n-1) + G_\phi v_{in,1}(n-1) + G_\phi v_{in,2}(n-1). \quad (22)$$

A very important VCDU design constraint must be adhered to when they are used in voltage-to-time integrators. When a rising edge passes through a VCDU, it will sample the input controlling voltage and delay the rising edge proportionally. However, the falling edge must not be affected by the controlling voltage, otherwise offsets or distortion may result. The VCDU design shown in Fig. 4(a) may be inadequate as the finite fall time of the input of ϕ_I may permit the input voltage to influence the charge time of capacitor C. Therefore, Fig. 7 illustrates the current-starved inverter VCDU outfitted with an AND gate. The AND gate is used to ensure that the input falling edge of ϕ_I is propagated to the output without being influenced by the input voltage v_{IN} through the VCDU.

It would be very desirable to cascade two integrators, however, this cannot be done easily. Because a time-difference variable is not a physical quantity the summation of two time-difference variables cannot be done without first transforming them into an intermediate medium such as charge [8], thus forfeiting some of the advantages of TMSP.

D. Time-to-Digital Conversion

The final step in the time-mode analog-to-digital process is to convert the time-difference variable into its digital representation. This may be accomplished with time comparators. Comparisons of two clock events may be performed by a D-type edge-triggered flip-flop, as demonstrated in Fig. 8. The input digital event $\phi_{IN}(n)$ is compared to a reference event signal $\phi_{REF}(n)$. If the edge of $\phi_{IN}(n)$ is leading $\phi_{REF}(n)$, then the output $D_{OUT}(n)$ results in a

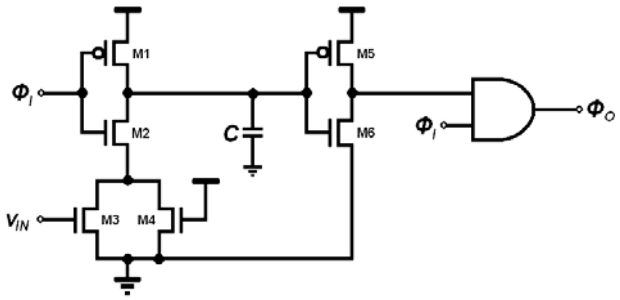


Fig. 7. Current-starved inverter VCDU with an output AND gate to bypass the clock's falling edge.

logic 1. Otherwise the output results in logic 0.

III. Time-Mode Delta-Sigma A/D Conversion

The TMΔΣADC system is designed based on the error-feedback structure for a ΔΣ modulator [18] shown in Fig. 9. The system model in this configuration may be implemented with a dual-input integrator, a comparator, and a digital-to-analog converter (DAC). The loop formed by the two summation blocks and the delay element is a two-input integrator with inputs $v_{in}(n)$ and $v_o(n)$. The dual-input time-mode integrator was described in the previous section and will be used as the core of the time-mode ΔΣ modulator design. The comparator block is implemented with the time comparator as previously described. If full scale voltages are being used then the DAC may be eliminated such that $v_o(n) = D_O(n)$. Otherwise, a single-bit DAC would be implemented consisting of a pair of analog switches. Recall that the summation block was implemented using a VCDU, which incorporates the sample-and-hold action under certain frequency and resolution conditions governed by (8). If this inequality is not satisfied based on design requirements then a sample-and-hold would need to be incorporated into the design.

The complete system of the TMΔΣADC is presented in Fig. 10 and consists of two dual-input integrators and a D-type edge-triggered flip-flop. The reference oscillator, i.e. the bottom dual-input integrator, provides the clock reference $\phi_{REF}(n)$ generating the analog time reference with the secondary function of clocking the data out of the D-type flip-flop. The signal oscillator, i.e. the top integrator, sums the input voltage with the inverse of the digital output voltage producing the difference equation

$$\Delta T_O(n) = \Delta T_O(n-1) + G_\phi\left[v_{in}(n-1) - v_o(n-1)\right], \tag{23}$$

where G_ϕ is the voltage-to-time conversion factor of the VCDUs, $v_{in}(n-1)$ and $v_o(n-1)$ are the input and output voltage levels relative to the reference voltage V_{REF}, and $\Delta T_O(n)$ is measured with respect to the time reference $t_{REF}(n)$. Note that this design is a discrete-time system since the analog input voltage is sampled by the VCDUs and converted into time-difference variables and processed at discrete time intervals.

The error signal $\Delta T_\varepsilon(n)$ made by the flip-flop comparison with respect to the analog time reference may be expressed as the difference between the input time difference $\Delta T_O(n)$ and the output $v_o(n)$ scaled by G_ϕ, i.e.

$$\Delta T_\varepsilon(n) = G_\phi v_o(n) - \Delta T_O(n). \tag{24}$$

Substituting the flip-flop error model from (24) into (23) reveals the first-order ΔΣ modulator difference equation

$$v_o(n) = v_{in}(n-1) + \frac{1}{G_\phi}\left[\Delta T_\varepsilon(n) - \Delta T_\varepsilon(n-1)\right]. \tag{25}$$

Fig. 11 presents an example illustrating the timing of four periods of the modulator's operation. The quantity T_{RESET} is defined as the propagation delay associated with a falling-edge transition through two VCDUs. It is the same for both oscillators. In terms of the parameters introduced earlier, we can write

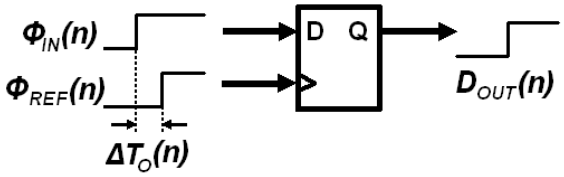


Fig. 8. Time comparator implemented using an edge-triggered D-type flip-flop.

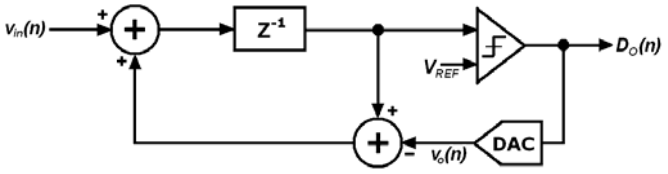


Fig. 9. First-order single-bit delta-sigma analog-to-digital converter error-feedback model.

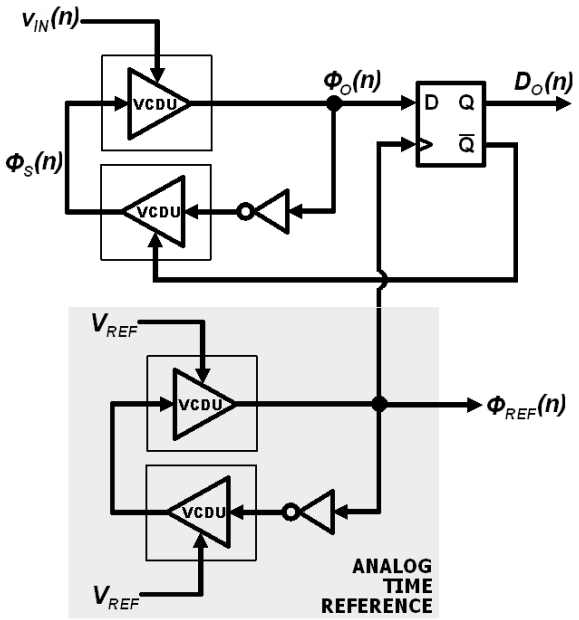


Fig. 10. First-order single-bit time-mode delta-sigma analog-to-digital converter (TMΔΣADC).

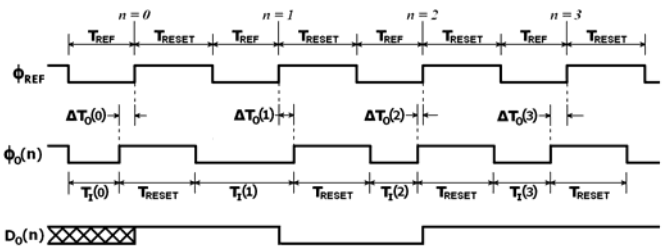


Fig. 11. Example timing diagram for the first-order single-bit TMΔΣADC.

$$T_{RESET} = 2\tau_{VCDU} + \tau_{INV} . \quad (26)$$

Likewise, T_{REF} is the delay through both VCDUs of the reference oscillator controlled by V_{REF} during a positive going edge, i.e.,

$$T_{REF} = 2G_\phi V_{REF} + 2b_\phi + \tau_{INV} . \quad (27)$$

As these two delays dictate the overall oscillation period, we can write the period of the reference oscillator as

$$T_{OSC,REF} = T_{REF} + T_{RESET} . \quad (28)$$

Subsequently, we can write the time of the rising-edge transition time for the reference oscillator output as

$$t_{REF}(n) = t_{REF}(n-1) + T_{REF} + T_{RESET} . \quad (29)$$

Conversely, the delay through the VCDUs controlled by $v_{IN}(n)$ and the flip-flop output $v_O(n)$ during a positive-going edge transition can be described as

$$T_I(n) = G_\phi v_{IN}(n-1) - G_\phi v_O(n-1) + 2b_\phi + \tau_{INV} . \quad (30)$$

Thus, the instantaneous period of the signal-dependent oscillator can be written as

$$T_{OSC,IN}(n) = T_I(n) + T_{RESET} . \quad (31)$$

As a result, the time of the rising-edge transition time for the signal-dependent oscillator becomes

$$t_o(n) = t_o(n-1) + T_I(n) + T_{RESET} . \quad (32)$$

Taking the difference between (32) and (29), allows us to write the time-difference at the input of the flip-flop as

$$\Delta T_O(n) = \Delta T_O(n-1) + T_I(n) - T_{REF} , \quad (33)$$

or when (27) and (30) are substituted in (33) we obtain the result shown in (23).

IV. MATLAB MODELING

A single-ended input first-order single-bit TMΔΣADC was modelled and simulated in MATLAB using the Simulink modeling environment. The block diagram of the model is shown in Fig. 12(a). VCDUs were implemented with transport delay blocks, a D flip-flop was used for the time comparator and the inverters were replaced with relay blocks. Some delay elements were incorporated to facilitate the processing time of the transport delay blocks. These delay were also implemented using transport delay blocks controlled by constant delays.

Simulations were conducted with the sampling frequency normalized to 8192 Hz. A simulation with 8192 points was collected and the power spectral density (PSD) of the output is presented in Fig. 12(b). At an oversampling ratio (OSR) of 390, the SNR is 79 dB. At an OSR of 195, the SNR is 70 dB. These data correspond to resolutions of approximately 13 and 11 bits, respectively. It may be seen from the PSD plot that the noise increases with frequency at a 20 dB/decade rate, as expected for a first-order modulator.

V. IMPLEMENTATION

A. Single-Ended Input TMΔΣADC

The TMΔΣADC was designed in a 0.18-μm CMOS technology and the complete transistor circuit is presented in Fig. 13. The VCDUs were implemented using the current-starved inverter design described in Fig. 4(a) without explicit capacitors in order to maximize the operation speed.

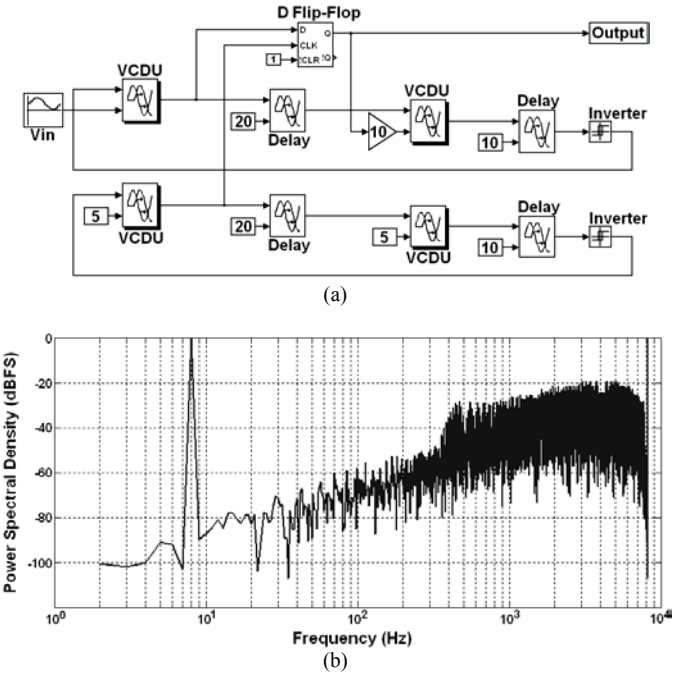


Fig. 12. Mathematical modeling of the TMΔΣADC: (a) MATLAB Simulink model diagram, (b) MATLAB simulation PSD results.

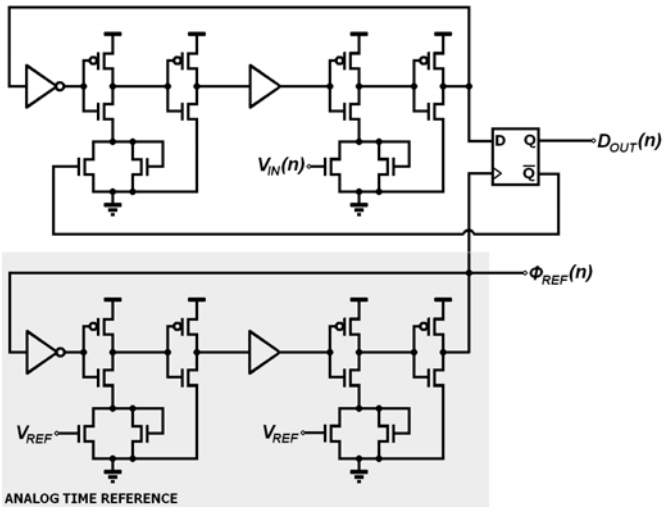


Fig. 13. Transistor schematic of a single-ended input first-order single-bit TMΔΣADC.

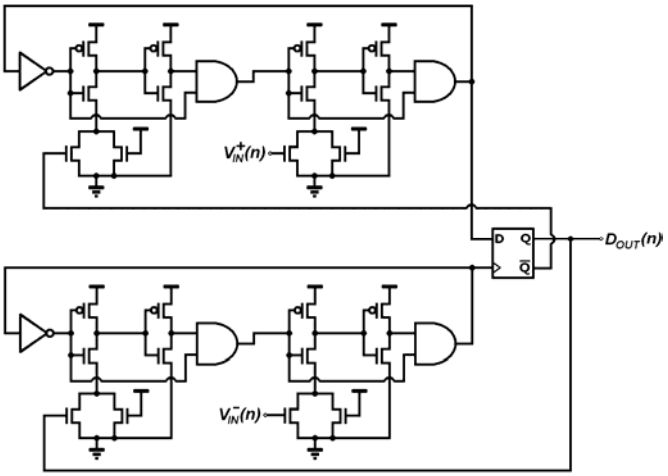


Fig. 14. Transistor schematic of a differential-input first-order single-bit TMΔΣADC.

The top oscillator is controlled by the input voltage $v_{IN}(n)$ and digital feedback voltage from the flip-flop. The bottom oscillator provides the analog time reference $\phi_{REF}(n)$ and is controlled by two reference voltages V_{REF}. Note that no sample-and-hold is being implemented thus relying on the VCDUs to perform the sampling action. The flip-flop was implemented with a library standard cell. The inverters and buffers are implemented in the complementary logic style and are sized to add appropriate delays to the oscillators to ensure that the flip-flop output reaches a stable state before it is sampled by the VCDU.

B. Differential-Input TMΔΣADC

The transistor level schematic for the differential-input TMΔΣADC is illustrated in Fig. 14. The VCDUs in this design have been outfitted with AND gates such that the negative-going edges bypass the VCDU, as presented in Fig. 7. In this design the top oscillator is controlled by the positive input voltage and the negative flip-flop output while the bottom oscillator is controlled by the negative input voltage and the positive flip-flop output.

C. Implementation Issues

There are several implementation issues which are inherently part of the TMΔΣADC architecture. They are described as follows.

Non-Uniform Sampling

The sample-and-hold action is being performed by the VCDU with respect to the sampling clock $\phi_S(n)$, as indicated in Fig. 10. The sampling clock edge measured with respect to the reference clock $\phi_{REF}(n)$ is also the error signal $\Delta T_\varepsilon(n)$ which is assumed to be uniformly distributed [19] with an RMS value of

$$T_{S-RMS} = \frac{2|G_\phi|A}{\sqrt{12}}, \tag{34}$$

where A is the maximum peak amplitude of the input voltage $v_{IN}(t)$. Hence, the input voltage is sampled non-uniformly which imposes a limitation on the performance of the overall TMΔΣADC design. This sampling mimics the effects of clock jitter. Using a formula from [20], the RMS noise $v_{n\text{-}RMS}$ that will result from this non-uniform sampling can be estimated by

$$v_{n-RMS} \approx \frac{2\pi A f_{IN}}{\sqrt{2}} T_{S-RMS} = \frac{2\pi |G_\phi| A^2 f_{IN}}{\sqrt{6}}, \tag{35}$$

where f_{IN} is the maximum frequency of the input signal. Although this noise is present, its magnitude is not predominant for low amplitudes or low frequencies. Furthermore, it may be controlled by the VCDU's voltage-to-time conversion factor G_ϕ. As an example, suppose the current-starved inverter VCDU described in the previous section was used, where its G_ϕ is -320 ps/V and the input amplitude is 200 mV. With an input bandwidth of 1 MHz, the resulting RMS voltage noise $v_{n\text{-}RMS}$ is 65.7 μV. Hence, this example TMΔΣADC will provide a best-case SNR of 72.7 dB which translates to an almost 12-bit resolution.

Synchronization

The TMΔΣADC is a synchronous ADC, however, the sampling clock must be generated on chip as it is implicitly part of the oscillating integrator operation. Moreover, the reference clock must also be generated on chip, which will oscillate at the same frequency as the sampling clock in order to provide the analog time reference $\phi_{REF}(n)$. An additional benefit of this design is that the reference clock $\phi_{REF}(n)$ and modulator clock $\phi_O(n)$ will automatically lock phases due to the system's negative feedback.

Mismatch

If the signal and reference oscillators are mismatched then their frequencies may differ. Consequently either the reference time T_{REF} will be skewed or the reset times T_{RESET} will differ between the oscillators. Consider, for example, that the VCDU reset times differ such that the reference and signal oscillator reset times are $T_{RESET,1}$ and $T_{RESET,2}$. Equation (33) would become

$$\Delta T_O(n) = \Delta T_O(n-1) + T_I(n) - T_{REF} + \left[T_{RESET\,2} - T_{RESET\,,1}\right]. \tag{36}$$

Substituting (27) and (30) into (36) produces the modulators difference equation

$$v_o(n) = v_{in}(n-1) + \frac{1}{G_\phi}\left[\Delta T_\varepsilon(n) - \Delta T_\varepsilon(n-1)\right] + \frac{1}{G_\phi}\left[T_{RESET\,,2} - T_{RESET\,,1}\right]. \tag{37}$$

Therefore, any mismatch which results from oscillator timing errors will manifest itself as a DC offset in the output.

Jitter Noise

Jitter noise on the sampling clock may arise from thermal noise, poor power and ground supplies, or EMI from external lines or devices. Consequently, jitter noise will manifest itself as an additive voltage noise source [20] with RMS value given by

$$v_{j-RMS} \approx \frac{2\pi A f_{IN}}{\sqrt{2}} T_{j-RMS}, \tag{38}$$

where $T_{j\text{-}RMS}$ is the RMS value of the jitter, f_{IN} is the input signal frequency, and A is the amplitude of the input signal. Note that (38) is based on the assumption that the input signal is sinusoidal.

Flip-Flop Metastability

Flip-flops have two stable states designated with logic 0 and logic 1. When the two input transitions edges are close together the flip-flop output may enter an unknown state, known as the metastable state. Given sufficient time the flip-flop output will reach one of the two stable states. However, noise may influence the flip-flop to make an incorrect comparison. Hence, metastability may result in the processing of an unknown logic state or an erroneous state. Although it was not used in this work, a technique to reduce the influence of flip-flop metastability is to pre-amplify the input time-difference using a time-amplifier [6].

VCDU Nonlinearity

It was demonstrated in the previous section that the VCDU circuits are linear within a limited input voltage range. Even within this range there remains some non-linearity in the order of ±0.1%. Therefore, the VCDUs may be the greatest factor in limiting the signal-to-noise and distortion ratio (SNDR) performance of the TMΔΣADC.

VI. Experimental Results

A. Single-Ended Input TMΔΣADC

The single-ended input TMΔΣADC was implemented in a 1.8-V, 0.18-µm, single-poly, six-metal CMOS process. A microphotograph of the test die is shown in Fig. 15. The single-ended input TMΔΣADC occupies a very small silicon area of 15 µm x 25 µm or 375 µm^2.

The analog time reference oscillator was determined to operate at approximately 140 MHz with a reference voltage V_{REF} set at 1 V. The total power dissipation was found to be approximately 475 µW. The modulator was exercised with a 400 $mV_{p\text{-}p}$ sinusoid at 100 kHz. 16384 points were collected and an example of the experimental results showing the power spectral density of the modulator's output is presented in Fig. 16(a). The SNR and SNDR measured from this example is 48.9 dB and 38.6 dB, respectively.

TABLE I
Design and Experimental Result Summary

Parameter	Single-Ended Input	Differential Input
Technology	0.18 µm CMOS, single-poly, 6 metal	0.18 µm CMOS, single-poly, 6 metal
Supply Voltage	1.8 V	1.8 V
Core Area	375 µm^2	2560 µm^2
Power Dissipation	475 µW	780 µW
Sampling Frequency	140 MHz	87 MHz
Output Nyquist Rate	400 kHz	125 kHz
OSR	175	348
Dynamic Range	55 dB	63 dB
Peak SNR	49 dB	60 dB
Peak SNDR	42 dB	54 dB

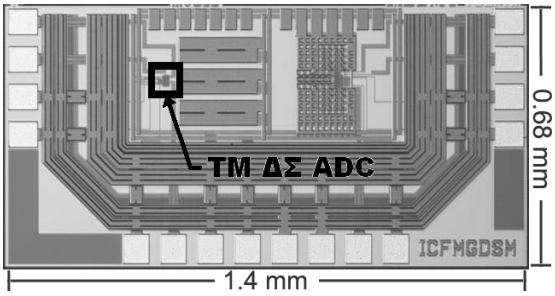
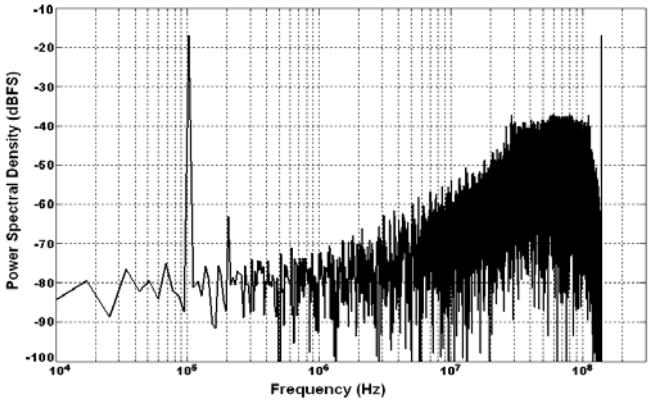
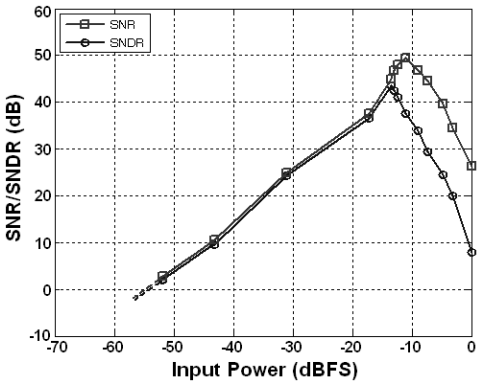


Fig. 15. Integrated circuit microphotograph of a test chip implementing the single-ended input time-mode delta-sigma ADC.



(a)



(b)

Fig. 16. Experimental results for the single-ended input first-order single-bit TMΔΣADC: (a) PSD of the ADC output. (b) SNR/SNDR versus input level.

The input voltage level was swept and the SNR and SNDR data was collected over a 400 kHz bandwidth, as presented in Fig. 16(b). The dynamic range of this design, as defined from the full-scale input amplitude of 0.8 V, is approximately 55 dB. A peak SNR of 48.9 dB and peak SNDR of 42.2 dB was achieved within a 400 kHz bandwidth (i.e. an OSR of 175). The specifications and experimental results for the single-ended input design are summarized in Table I.

B. *Differential-Input TMΔΣADC*

The differential-input TMΔΣADC, given in Fig. 14, was implemented in a 1.8-V, 0.18-µm CMOS process. A microphotograph of the test die is shown in Fig. 17. The complete ADC design occupies an area of 2560 µm^2. Each transistor in one time-mode integrator was matched with its equivalent transistor in the other integrator using an interdigitized finger layout technique [21].

The modulator was dynamically stimulated using a sine wave biased at 1 V with an amplitude of 400 mV. It was determined that the modulator was oscillating at 87.2 MHz. In order to maintain coherency the test signal frequency was set to 24 kHz. 65536 data samples were collected and an example PSD plot of the ADC output is presented in Fig. 18(a). Over a signal bandwidth of 125 kHz (i.e. OSR of 348) the SNR and SNDR was determined to be 56.8 dB and 54.3 dB, respectively. It may be seen from the ADC's output spectrum that the even-order harmonics have been suppressed, despite a significant presence of harmonic distortion. It is believed that the distortion is an artifact of the increased magnitude in the sampling non-uniformity.

The input dynamic range was determined by incrementing the input signal amplitude while capturing the resulting SNR and SNDR data. Fig. 18(b) presents the SNR/SNDR versus input signal level data revealing that the maximum achievable SNR and SNDR for this design is 60 dB and 54 dB, respectively. The input dynamic range for this design, within a 125 kHz bandwidth, is approximately 63 dB, where the full-scale input signal amplitude is 0.8 V. The design and experimental performance are summarized in Table I.

VII. Discussion

A. *Single-Ended versus differential-Input*

Comparison between the single-ended and differential-input designs presented in this work is difficult as these circuits have been implemented differently. That is, AND gates were added to the differential VCDUs to help reduce distortion. Nonetheless, we still believe that the differential design would have performed better than the single-ended counterpart, as a differential structure generally provides greater noise immunity and rejects even-order harmonics.

B. *TMΔΣADCs versus Other Designs*

Fig. 19 presents two graphs which compare the single-ended and differential-input TMΔΣADCs with many other low-pass delta-sigma ADC designs recorded in [11], [12], and [22] – [53]. Fig. 19(a) offers a comparison of silicon area usage plotted at various CMOS technology nodes. It may be observed that the area requirement of the TMΔΣADCs is between two and five orders of magnitude less that all other reported designs. Fig. 19(b) classifies the cited designs using the figure of merit (FoM) [54] given by

$$FoM = \frac{P}{2 \cdot BW \cdot 2^{ENOB}}, \tag{39}$$

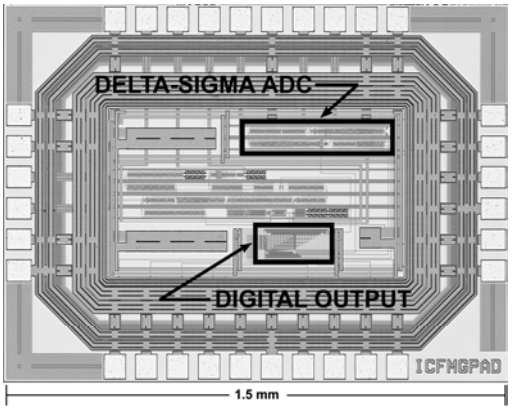
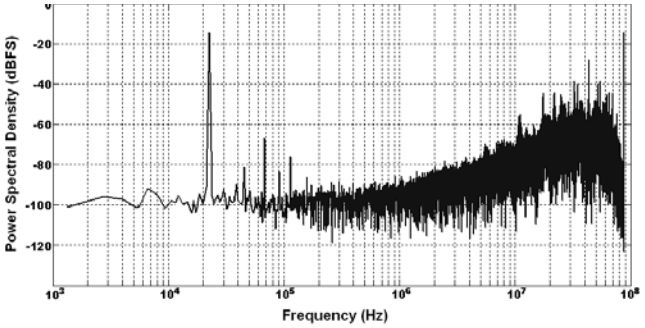
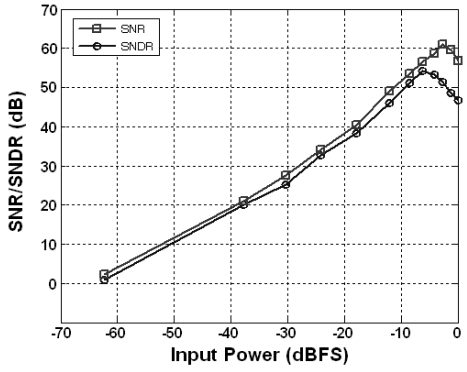


Fig. 17. Microphotograph of the test chip implementing the differential-input TMΔΣADC.



(a)



(b)

Fig. 18. Experimental results for the differential-input first-order single-bit TMΔΣADC: (a) PSD of the ADC output. (b) SNR/SNDR versus input level.

where P is the power dissipation, BW is the input signal bandwidth and $ENOB$ is the effective number of bits. ENOB may be defined as

$$ENOB = \frac{SNDR_{\max} - 1.76}{6.02}. \quad (40)$$

The FoMs for the single-ended and differential-input designs are respectively 5.6 pJ and 7.6 pJ. It should be noted that all of the published works with the exceptions of [11] and [12] are delta-sigma designs of higher-order (i.e. 2nd – 6th-order) and operate with multi-bit quantizers (i.e. 3 – 4-bit). As such, their performance is enhanced while sacrificing area and power. The TMΔΣADC experiences lower SNDR for several reasons. Primarily, the architecture is necessarily a first-order design which increases the quantization noise over all other designs. Moreover, the TMΔΣADCs were constructed with single-bit quantizers unlike most of the published works. Finally, the linearity of the front-end voltage-to-time converter is a large contributor to the distortion component of the SNDR. Therefore, improving the linearity of the VTC is crucial to increase the overall SNDR performance of the TMΔΣADC.

C. Higher-Order and Multi-Bit TMΔΣADC Designs

The construction of higher-order delta-sigma modulators using TMSP is not an easy task. The summation of two time-mode variables cannot be done directly without first converting them into physical intermediate variables. Since this opposes the advantages of TMSP, higher-order modulators were not explored further.

A multi-bit TMΔΣADC design may be implemented by replacing the time comparator with a TDC and adding a DAC in the feedback path of the single-bit design. For every additional bit SNR should improve by 6 dB. All the same implementation issues for the single-bit ADC described in Section III will apply to a multi-bit design, however, the linearity of the TDC and DAC may become an issue.

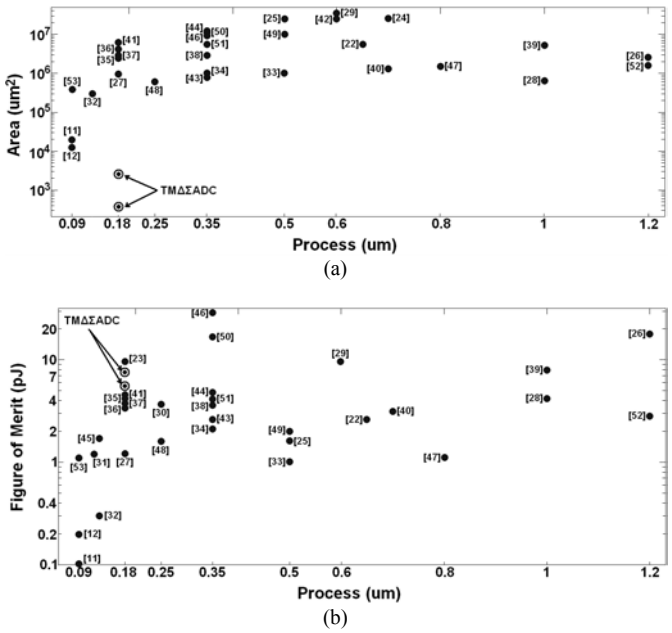


Fig. 19. Comparison between TMΔΣADC designs and state-of-the-art designs recorded in the literature: (a) Technology process node versus area, (b) Technology process node versus Figure of Merit.

VIII. Conclusion

This paper explored the design of ΔΣ ADCs utilizing the TMSP methodology. It was demonstrated that a first-order single-bit modulator could be designed from four VCDUs, a D-type flip-flop, and some digital inverters. Proof-of-concepts for a single-ended input design was offered through MATLAB modeling and simulations. Two ICs were fabricated incorporating two TMΔΣADC designs; a single-ended input and a differential-input design. The experimental results demonstrated that delta-sigma converters, offering 7 and 9-bits of effective resolution, may be constructed using the TMSP philosophy. These designs were shown to occupy very small silicon areas (375 μm^2 and 2560 μm^2) while consuming less than milliwatts of power.

Distortion was observed in both designs. This may be explained by the nonlinearity of the VTC's transfer characteristic and the nonlinear sampling mechanism of the VCDUs. A sample-and-hold circuit could be implemented to remove the latter distortion contribution.

The TMSP methodology proposes a low cost solution for integrating ΔΣ ADCs in state-of-the-art CMOS processes. Specifically, TMΔΣADCs offer the potential for ultra high speed (i.e. gigahertz range) data conversion which occupies incredibly small silicon areas while consuming very low power. The operating speeds of these designs were not pushed to their upper limits. In order to achieve maximum speed, the TMΔΣADC circuits may be modified by reducing the VCDU's voltage-to-time gain, minimizing nodal capacitance, and reducing inverter delays through transistor sizing.

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Christopher S. Taillefer (S'04) received the B.Eng. degree from Concordia University, Montreal, QC, Canada in 2000 and the M.Eng. and Ph.D. degrees from McGill University, Montreal, QC, Canada in 2003 and 2008, respectively.

He has been honored with the Teaching Excellence Award in 2006 from Concordia University where he has been a part-time faculty member since 2001. He is currently employed at DFT Microsystems Inc. in Montreal, Canada. His research interests include the design and test of mixed-mode integrated circuits and systems.

Dr. Taillefer has received several academic awards and scholarships including the undergraduate Phoivos Ziogas Medal for Electrical Engineering (Concordia University), and scholarships from the Natural Sciences and Engineering Research Council of Canada, le Fonds pour la formation de chercheurs et l'aide à larecherché du Quebec, le Groupe Interuniversitaire en Architecture des Ordinateurs et VLSI, and Walter C. Sumner Fellowships.

Gordon W. Roberts (S'85–M'89–F'04) received the B.A.Sc. degree from the University of Waterloo, Canada, in 1983 and the M.A.Sc. and Ph.D. degrees from the University of Toronto, Canada, in 1986 and 1989, respectively, all in electrical engineering. At McGill University he is a full professor and holds the James McGill Chair in Electrical and Computer Engineering.

He has co-written five textbooks related to analog IC design and mixed-signal test. He has published numerous papers in scientific journals and conferences, and he has contributed chapters to various industrially focused textbooks. Dr. Roberts has held many administration roles within various conference organizations, such as the International Test Conference, Custom Integrated Circuit Conference, Design Automation Conference and the International Symposium on Circuits and Systems.

Dr. Roberts has received numerous department, faculty and university awards for teaching test and electronics to undergraduates, and received several IEEE awards for his work on mixed-signal testing. Dr. Roberts has supervised over 40 graduate students at the Masters and PhD level. In 2003 he took leave from McGill to co-found DFT Microsystems, Inc, a company specializing in high-speed timing measurement. He returned to McGill 2005 where his current research includes analog IC design methods and built-in self-test techniques for analog and high-speed digital circuits.