High Dynamic Range CMOS Imager Technologies for Biomedical Applications

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***Abstract*—Apart from the ongoing debate about using CMOS active pixel sensors (APS) or CCD imagers for today's consumer and commercial applications the emerging biomedical market presents new opportunities to CMOS APS. Logarithmic response High-Dynamic Range CMOS (HDRC) cells are the preferred photosensitive circuits for building sensors with contrast and not with illumination dominated outputs. Prominent examples addressing distinct issues in life style and health care are the possibilities to restore vision through a sub-retinal CMOS imager implant and to fabricate a low-cost intracorporeal video probe through a miniature CMOS imager. The sub-retinal imager chip presented here is the first implanted into the eye of a blind human patient with partial restoring of vision.**

***Index Terms*—Endoscopes, high dynamic range, image sensors, retinal implants.**

I. Introduction

NEW developments in image sensors caused by the introduction of CMOS technology with improved possibilities for readout and signal conditioning prefer application specific image sensors for disposable, low-volume and high-sophisticated biomedical products. The CCDs performance criterion for this technology's selection has become less important compared to the stand-alone low power operation of CMOS image sensors by nearly comparable pixel size, sensitivity and noise [1]. The insufficient dynamic range, because of the charge storage capacity limited to about 60 dB, is the disadvantage of photo-generated charge integrating "linear" pixels in both technologies. The two sensor designs presented in this paper exploit the high-dynamic range CMOS (HDRC) pixel circuit providing a continuous linear-to-logarithmic transformation of the photo current into a voltage sense signal [2], [3]. This pixel inherent transformation expands the dynamic range to more than 120 dB with a slightly reduced color and contrast resolution (approx. 1%) in the high illuminated image areas. One sensor is used as a retinal implant for the human eye; the other sensor is used in endoscopic applications.

In Germany alone, about 17,000 people become blind every year, many of them due to degeneration of the photosensitive rod and cone cells by retinitis pigmentosa or macula degeneration. Restoring vision through a technical implant, similarly to the well established pace maker and cochlea implant technologies, is thus a very relevant social challenge [4]. In this paper we describe a slightly improved version of the original CMOS imager chip that was used in a clinical trial with successful partial vision restoration for the first time in October 2005 at the University Hospital Tübingen, Germany [5], [6]. Both the original and the improved retinal implant chips were designed and fabricated by the authors at IMS CHIPS. These chips have not been published before, apart from a brief presentation at the 2008 IEEE International Solid-State Circuits Conference [7]. The goal of this paper is to present the detailed circuit operation of the improved chip and to explain the slight change made from the original chip. Note, that, as the eye has a logarithmic response to illumination, the presented sensor with similar characteristics is well suited for a retinal implant.

Diagnosis and surgery in medical practice is today routinely involving endoscopic inspection aids, which operate under strongly varying light conditions. Low cost, or even disposable endoscopes with outstanding dynamic range are therefore highly desirable. The second image sensor we present and discuss is, to our knowledge, the first miniature APS imager chip based on thin-film-on-CMOS (TFC) photodiode technology targeted at low-cost and disposable diagnostic products.

II. Sub Retinal Implant

A. Retinal Implant Concepts and Biomedical Constraints

Additional to visual cortex [7]–[9] or optical nerve stimulations [10], [11] there are two competing approaches for a preferred retinal stimulation: With an epi-retinal implant, the information received by a camera is processed and transferred to a chip that supplies a stimulus signal to the ganglion cell/optical nerve interface [12]–[19] In contrast the sub-retinal implant directly replaces the malfunctioning rods and cones in the lower part of the retina by a CMOS imager chip having stimulus electrodes at its front-side surface [20], [21] (Fig. 1).

Charging and discharging the stimulus electrodes by monophased voltage pulses creates visual perception caused by an increased number of delayed spikes in the allocated ganglion cells [22] Sub-retinal stimulation of the residual nerve networks benefits from the natural perception assigned to the location of the lens image and the proposed use of eyes movements for the extension of the field of view [4].

Charging and discharging the very high capacitance stimulus electrodes by short monophased voltage pulses results in

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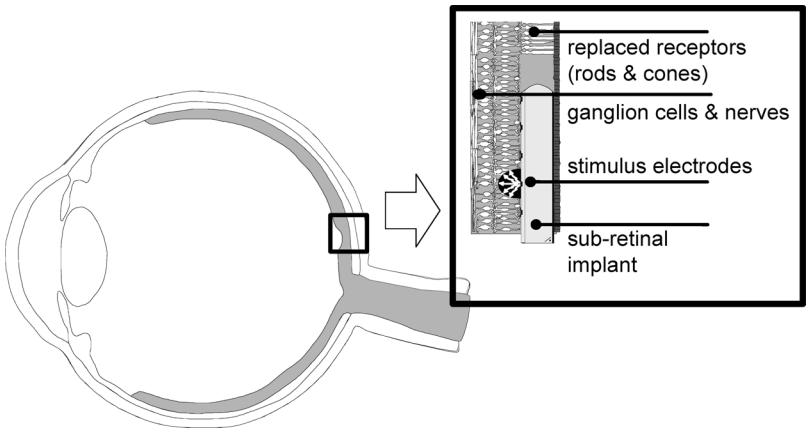

Fig. 1. Schematic illustration of the human eye with a part of the retinal tissue. The position of the sub-retinal chip within the macula is shown in the highlight.

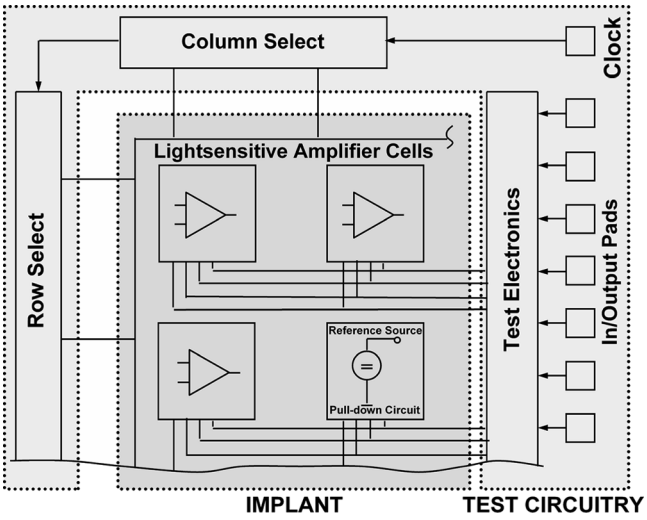

Fig. 2. Layout schematic of the chip, indicating the chip section to be implanted (dark grey) and the test circuit periphery to be removed after on-chip testing (light grey).

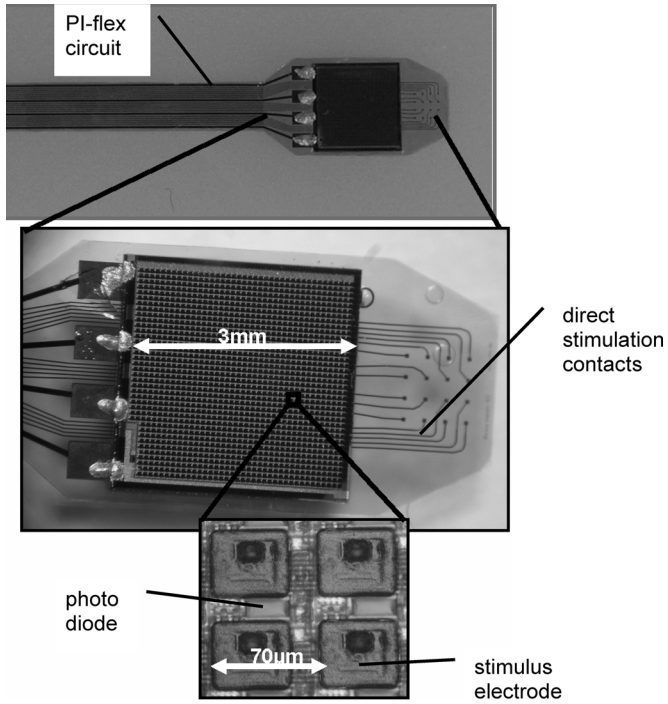

Fig. 3. Photographs of the tape with I/Os and mounted retina-implant chip (top) and magnified details in the highlighted areas. The middle inserted image shows the chip and a 4 × 4 point matrix for direct stimulation contacts. The large contacts (bottom) are the on-chip stimulation electrodes.

charge transfer by polarization changes of H_2O molecules on the electrode surface. No dissociation or tissue degradation occurs for polarization voltages below 2 V. Total discharging on the falling edge of the pulse results in charge-balance without any charge transfer and in two biphasic current pulses within the tissue resistance. To achieve proper stimulation and preventing cells from overcharging or damaging biophysically postulated constraints to charge modulation (1–40 nC), charging current (10–100 μA), safe voltage swing (<2 V), preferred pulse duration (500 μs) and a synchronous pulse on all pixels with a repetition frequency of 20 Hz need to be observed [22], [23]. The big variations of the threshold of the retina exclude the necessity of high accuracy for circuit components. Moreover, the chip size should be at least 3×3 mm^2 for a minimum viewing angle of 12°. The electrode spacing should be about 70 μm to ensure a properly resolved signal transfer to the ganglion cells and optical nerves, respectively [7].

B. Circuit Design

The complete chip shown in Fig. 2 consists of the actual implant and a test frame surrounding it. Within the implanted part, the pixel stimulation cells (pixel cells) are arranged in a 40 by 38 array with the "V_{global} cells" and the "V_{bias} cell" replacing some of the pixel cells. The implant is connected with four pads (VDD, VSS, Vbias, Vglobal) to the external control electronics by a metalized polyimide tape (Fig. 3). The terminals VDD, VSS and Vbias are for normal use.

Each of the more than 1450 pixel cells includes an HDRC circuit, consisting of a sub-threshold transistor in series with the photodiode. Whereas the illumination is increasing, the output voltage of the HDRC circuit is decreasing. This output (called the local diode) is connected to the inverting input of an operational amplifier (PMOS-gated low gain opamp) that drives the stimulus electrodes (Fig. 4).

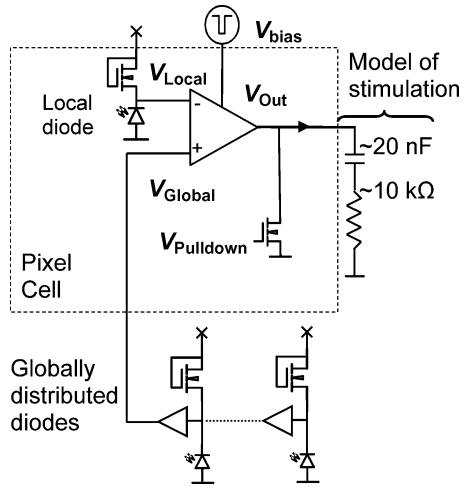

Fig. 4. Circuit schematic of the pixel cell of the sub-retinal implant.

The non-inverting input of the operational amplifier is connected to a reference signal (V_{global}) generated by 9 distributed "V_{global} cells" measuring the logarithmically averaged light intensity. For testing, characterization or adjustments for biological purposes, this V_{global} may be adjusted externally.

The "V_{bias} cell" is sourced with a mono-phased voltage pulse by the Vbias pad and reduces the internal low amplitude value of V_{bias} to the safe value of $V_{\mathrm{DD}}/2$ for the purpose of limiting the maximum power dissipation on the chip. This mechanism also covers broken wire connections in the carrier tape.

The signal V_{bias} serves three purposes in the pixel cell:

1) By setting V_{bias} to V_{dd}, the opamp is completely turned off, thus limiting the average power dissipation to about 1% of the steady-state value.
2) Setting V_{bias} at the opamps to a voltage in the range of $V_{\mathrm{dd}}/2$, the opamps are turned on to form an output pulse of defined length (500 μs/20 Hz). The exact value of V_{bias} determines the internal bias current (10–100 μA) and thus the driving strength of the stimulus electrodes (1–40 nC).
3) From V_{bias} the control signal pulldown is generated. It guarantees a defined termination of the stimulation pulse and a total discharge of the electrode.

Note, that in the original chip design the supply voltage was pulsed externally, thus leading to undesirable pulse distortion due to the parasitic RC delay of the metalized polyimide tape connection (see Fig. 3).

To ensure reliability, all relevant signals are distributed by a wire grid with at least two paths to each cell. The connections between test frame and implant chip are reduced to the minimum number required, with special precautions taken for the wider power lines, to reduce possible corrosion. To ensure safe operation on the implant side, the test control signals are actively pulled to safe values. The signals from the carrier tape to the implant chip are protected by ESD units.

C. Fabrication and Test Methodology

The circuit was fabricated by using an in-house 0.8 μm p-well CMOS technology with two metal levels supplemented by additional process steps for passivation seal and post process compatibility.

Prior to encapsulation the actual imager is functionally tested on wafer by the test frame [24]. Addressing all pixels by boundary scan circuits allows for sequential tests of bias voltages, local and averaged photosensitivity, amplifier-gain as well as open-circuit and capacitively loaded (22 nF) output signals. The sensor is also stimulated with different light levels and the different output voltage levels are measured. As described in the previous section, the output voltage at a capacitor of 22 nF (representing a model of the human eye) should be modulated between 0 V and 2 V applying the 500 μs stimulation pulse length and not exceed 2 V for all conditions and longer stimulation pulse length.

Subsequently the wafer is covered with biologically stable organic encapsulation layers and receives corrosion resistant nanocolumnar TiN or IrO electrodes (50×50 μm^2) with very high capacitance [24] (Fig. 3). The test frame is physically removed from the sensor by dicing, so none of the test circuitry remains. Selected good dies are thinned down to $\sim$ 50 μm thickness by a mechanical grinding process. The thinned imager chip is mounted onto a metalized polyimide tape-forming the medically proven flexible connection between the eye implant and the external power supply (Fig. 3). Corrosion safe materials and wiring constructions [25] are required for achieving long term stability of the connecting tape. Additional tests of the charge transfer of the implant are performed by probe connection prior to the implantation process in order to prevent the chip from from being damaged during the encapsulation process.

D. Results and Discussion

Fig. 5 shows the input voltages V_{local} (one cell) and V_{global} (average of 9 cells) of the HDRC circuit for a stimulation cell as a function of illumination. These input voltages follow the logarithmic value of illumination over more than four decades centered on retina's irradiance at normal room illumination. The difference of the two logarithmic voltages results in a 22 nF (adopted electrodes capacitance) loaded output signal controlled only by local image contrast without any effects of global illumination (Fig. 6).

The load dependent final voltage of the monophased output pulse on the pixel output is current-controlled by the external adjustable V_{bias} voltage to properly operate at variations in load capacitance of more than 400% [Fig. 7(a), (b)]. Caused by the current adjustment within the voltage range limitations the transferred charge is modulated only by the input voltage difference. The amount of charge is not sensitive to capacitance variations at the stimulation contacts. The pixel cell operational amplifier delivers up to 40 nC charge for the 500 μs pulse length according to biological test results.

The DC power supply concept with internal generation of pulsed amplifier outputs results in a stable operation without cross-coupling effects over the substrate to the photosensitive ultra-low current circuits even at a peak current consumption of more than 200 mA. With a duty cycle of 1% (500 μs on by 50 ms off) the average power consumption is less than 600 μW for the whole chips and no heating of the tissue is expected.

The chip described above is functionally the same as the original retinal implant chip but with the improvement in the on-chip voltage pulse generation. Although this improved version of the

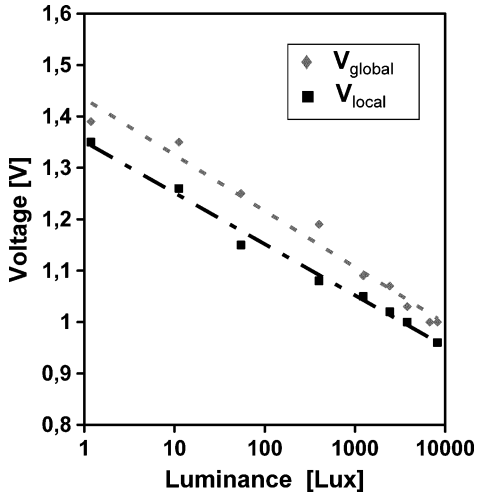

Fig. 5. Photosensitivity of $V_{\rm local}$ and $V_{\rm global}$ measured on the output of a differential amplifier in the test circuitry. $V_{\rm global}$ is an averaged signal of nine photodiodes. $V_{\rm local}$ is from a single photodiode. Offsets between $V_{\rm local}$ and $V_{\rm global}$ are from amplifier offset and from the noise of a single photodiode; these signal levels are adjustable by external controls.

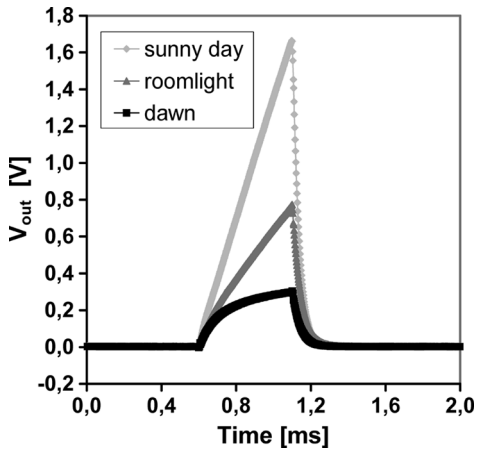

Fig. 6. Measured output signal of a stimulation electrode with different illumination as a spot of a 1/5 piece of the pixel array. $V_{\rm global}$ has no external adjustment. The load is simulated by a 22 nF capacitance. The amplitude is $<$2 V due to the biophysically postulated constraints (Sunny day $>$100,000 lux, room light $\sim$1000 lux, dawn $\sim$10 lux)

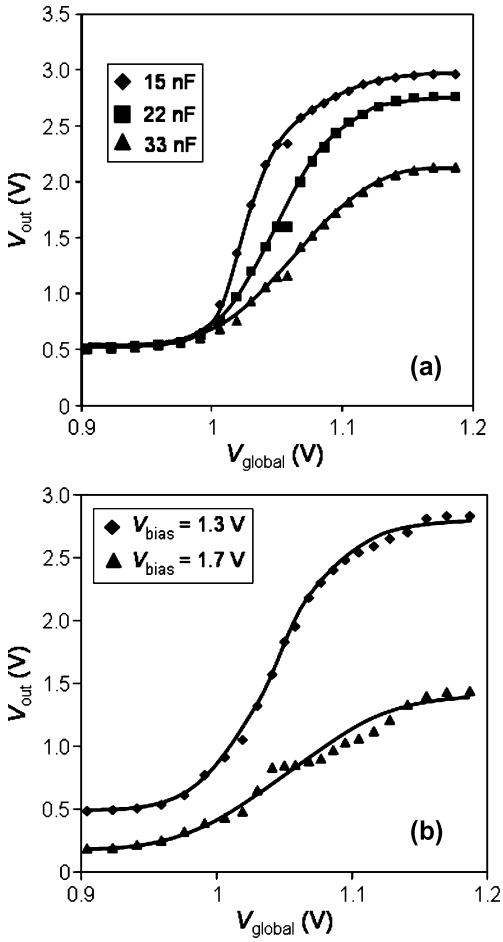

Fig. 7. Amplifier output voltage swing on different load capacitances. $V_{\rm bias}$ adjusted by 1.3 V (b, top curve) to 1.7 V (b, bottom curve); $V_{\rm global}$ is electrically modulated to simulate different illuminations levels. $V_{\rm local}$ is constant to represent constant illumination ($\gg$1000 lx). Pulswidth is 0.5 ms. Very high illumination and reduced current cause the saturation.

chip has not been implanted yet, we expect the implantation of the improved version into the human eye will be successful. This effort is currently under way.

III. Miniature Video Probe

Visual inspection by endoscopy is an important capability in clinical surgery and medical health care. Video inspection inside the human body also can be autonomous and lead to new products, such as the video pill [26]–[28]. Such diagnostic tools should have minimum size and be disposable thus making low-cost CMOS technology the preferred choice. The goal is to achieve a maximum fill factor and to tailor for an optimum trade-off between pixel size and sensitivity.

A. Bulk Silicon Versus TFC Pixel

An important requirement for miniature sensors is small pixel size with maximum sensitivity. The minimum detectable illumination of a CMOS image sensor pixel is particularly limited by the area available for the photodiode. This fill-factor amounts to typically 20–60%. Additionally, in state-of-the-art CMOS technologies the photo-sensing element is covered by dielectric layers having a thickness in the range of 3 to 7 μm [Fig. 8(a)]. Shadowing effects and undesired optical crosstalk caused by reflections of incident light within the metal and dielectric layers are the consequences.

Therefore, a vertical integration of the photodiode and the CMOS readout circuitry has been proposed and several approaches have been demonstrated [29]–[31]. The concept exploited here is based on low temperature deposition of amorphous silicon in order to implement photodiodes on top of CMOS image sensors [Fig. 8(b)]. A sandwich of p-i-n or n-i-p α-Si:H is deposited and patterned on top of the 0.25 μm CMOS foundry wafers. Due to the short diffusion length of charge carriers in α-Si:H based semiconductors no pixel separation is needed in the upper photodiode layers. A common top contact is formed by depositing a layer of ZnO. This layer needs to be sufficiently thin in order to be transparent for the incident light. The ZnO top layer is connected to the CMOS circuitry by an aluminum (Al) ring at the periphery of the imager field.

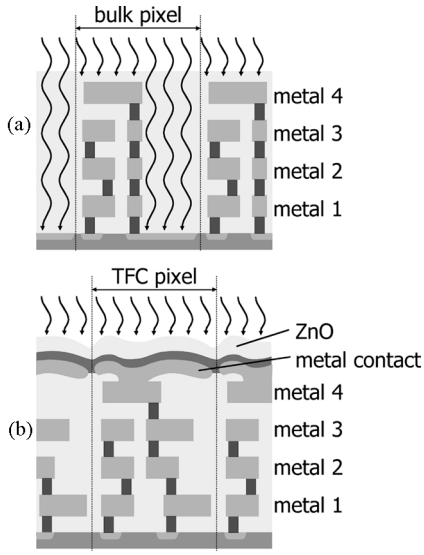

Fig. 8. (a), (b) Comparison of silicon and TFC photodiodes in the image sensor pixel. The TFC system consists of a stack of p-doped, intrinsic and n-doped a-Si:H layers with a transparent conducting top ZnO layer.

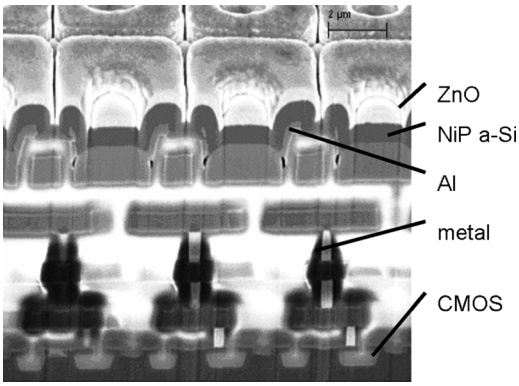

Fig. 9. Cross-sectional scanning electron micrograph (SEM) of a TFC pixel. The top layer is the transparent ZnO layer, underneath the TFC layers consisting of p-doped, intrinsic and n-doped a-Si:H layers.

Deposition of an anti-reflection coating and opening of the bond-pads completes the wafer-level processing. In Fig. 9 the cross section of a TFC sensor pixel is shown. One metal contact per pixel is required for the TFC diode that defines the photosensitive area of the pixel. As a result of the non-planarity of the TFC layer and the spacing of the base metal contacts between pixels the fill factor is $\sim$90% instead of the ideal value of 100%.

For comparison, miniature image sensors with both bulk and TFC pixels (pixel pitch was 4.6 μm in both cases) have been designed and processed.

B. Circuit and System Design

The main tasks for developing a CMOS imager for the use in special applications like endoscopes and seeing instruments for minimal invasive surgery are minimizing silicon area, reducing power consumption and minimizing the number of input/output (I/O) pads. The developed and tested HDRC image sensor is realized on 1.1×1.3 mm^2 silicon, has a pixel array of 208×186 pixels, a pixel pitch of 4.6 μm and needs only four I/O pads,

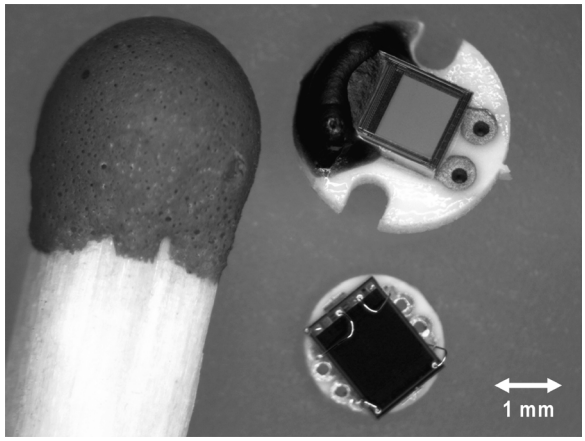

Fig. 10. Miniature image sensors with 180 by 200 pixels and four wire connections on different packages (compared to a match). The larger package (top) contains the TFC type sensor designed for a fiber optics illuminated endoscope. The design in the smaller package (bottom) is optimized for small diameter applications. By the centered image area and the edge positioned bonding pads the package diameter is reduced from 3 mm to 2 mm.

making the sensor very suitable for integration in such systems. It is possible to mount the image sensor directly onto the tip of the endoscope (Fig. 10) in comparison to other systems, this has the main advantage, that no fragile fiber optics are needed. The sensor has to be connected via four metal wires; cable lengths up to 3 m have been tested. For operation the required signal terminals are VDD (3.3 V power supply), VSS (ground), CLOCK (pixel clock 1.5 MHz) and VIDEO (analog video output signal). The straight forward operation control needs no external configuration signals. The imager is designed for a standard operation mode with a pixel rate of 1.5 MHz, which results in a frame rate of approx. 40 fps. Overall power consumption of the sensor is approximately 7 mW.

Fig. 11 shows the main building blocks and the I/O pads. The main building blocks are the address generator, including the operation control, the address decoder, decoder unit for the pixel array addressing and generating control signals for readout operation, the sample-and-hold stage with the analog multiplexer and the analog signal path including amplifier and level shifter for the analog video output signal. For a defined initiation of sensor operation a power-on-reset circuit (POR), which sets the address decoder in a defined state, is included. For on-chip separated power domains for switching activity and sensitive analog building blocks a power regulation circuit is also included. In the following the main building blocks of the imager are described in detail.

As described above the imager has a pixel array of 208 columns and 186 rows. The readout is realized by a rolling shutter. An on-chip address generator generates frames of 200×180 pixels. The readout frame is slightly smaller than the pixel array. This is done to reduce parasitic side effects from corner pixel cells like stray light and matching problems at the corner pixel cells. The resulting 200×186 frame is centered in the complete pixel array of 208×180. Output of the address generator is an 8-bit column address and an 8-bit row address. Both addresses are gray coded. The gray code is chosen to reduce the switching activity on chip. The address decoder

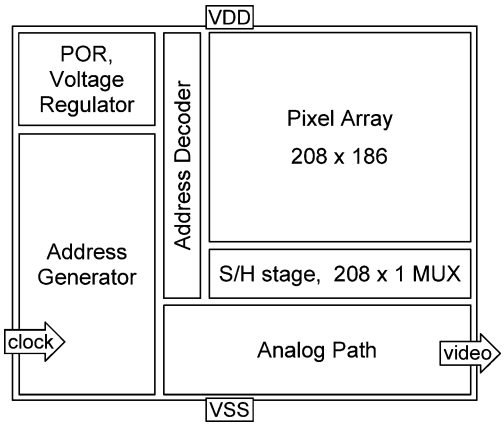

Fig. 11. Building blocks and architecture of the miniature image sensor.

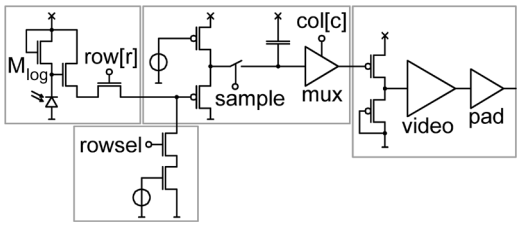

Fig. 12. Signal path of the miniature image sensor.

decodes the incoming gray coded address to a "1 of n code", which only activates one row for readout. Also the required control signals for the analog signal path are generated in the address decoder.

Fig. 12 shows the main building blocks of the analog signal path. The 4.6 μm HDRC pixel cell is designed as a three-transistor cell. Each pixel cell includes the input transistor of a NMOS source-follower. The current source is placed one time for all pixels in one row at the corner of the pixel array. This shared bias structure is possible due to the rolling shutter readout scheme. Only one of the 186 rows is active for readout. The source-follower is needed to drive the column line, which acts as a parasitic capacitance load for each pixel. The output of the pixel cell is connected via a row select transistor to the column line. The voltage level on each column line is stored in a sample-and-hold stage. This sample-and-hold stage is 208 times instantiated, which requires a small area and a smart power design. As shown in Fig. 12 the sample-and-hold stage consist of a source-follower at its input, the sample-and-hold capacitor and an amplifier at the output. The source-follower is needed to ensure, that the voltage level on the sample-and-hold amplifier settles to 99.9% in 600 ns when the sensor is used with a pixel rate of 1.5 MHz (external clock = 1.5 MHz) and to shift the voltage to about 1.65 V. An advantage of the source-follower is that it reduces the kickback noise to the sensitive column line. Each of the 208 PMOS source-followers is biased with a static current of 5 μA. Because of the rolling shutter readout, all source-followers were permanently switched on.

The sample-and-hold capacitor is realized as a parallel connection of a metal-insulator-metal (MIM) capacitor and the gate capacitance of a PMOS transistor. This parallel connection is caused by the capacitance value of the MIM cap (1 fF/μm^2). The needed sample-and-hold capacitor is approximately 600 fF. A PMOS transistor is chosen because the n-well in the p-substrate for the given CMOS process can be used as a shield against in coupling noise from the substrate. The output amplifier of the sample-and-hold stage is a one-stage amplifier with a NMOS input pair and a current source with a bias current of 20 μA. Because of the small given area to instantiate 208 buffer amplifiers and the low power consumption a second power output stage was not implemented. The amplifier has a low power to drive capacitive loads. It is designed to drive only the analog 208-to-1 analog multiplexer. The power amplification and level shift circuit is placed behind the multiplexer in the video amplifier. The multiplexer is controlled by the address decoder. At the output of the multiplexer an analog inverter shifts the light dependent output signal to the required voltage range (approximately 1 V for black level and 1.5 V for bright illumination; approx. 5000 lux). The analog inverter circuit is followed by a video amplifier to drive the input capacitance of the output pad buffer. This pad buffer is necessary to drive capacitive and resistive loads connected to the analog output pad, for example coaxial cable or an external circuits. In typical endoscope applications with a direct on-tip mounted imager cable lengths up to 3 m are feasible. The integrated pad amplifier is a two- stage voltage follower configuration with a folded cascode input stage and a Class-AB output stage, which is designed to drive capacitive and resistive loads up to 10 kΩ and 30 pF. Because of the small silicon area and the low power application a digital output was not implemented. The sensor has only an analog video output. To synchronize the application to the imager the information required for new line (line-enable) and new frame (frame-enable) are modulated on the analog video signal. For synchronization purposes the analog output level is clamped for a specified number of pixel clocks, 16 pixel clock cycles for line-enable and 1096 for frame-enable to a defined voltage level, which is out of the regular video signal levels for an easy detection in application. This circuit makes it possible to work without any additional I/O pads for integrating the sensor in an imager system.

The main operation control is implemented in the address generator and the address decoder. All control signals for pixel array readout and analog signal path control, like sample-and-hold and amplifier control are generated by the address decoder from the incoming gray coded addresses. To start readout operation in a defined state, the circuit includes a power-on-reset circuit (POR). Before the supply voltage reaches a threshold level of approximately 2 V the address decoder is in reset state. After reaching the threshold level the POR circuit starts the readout after a small time period by starting the address generator. The time interval is realized by a current source, which is connected to a capacitor. The value of the capacitor and the bias current defines the reset period after reaching a supply voltage level of approximately 2 V. After starting the address generator the POR circuit switches to a power down mode and will be active again after switching off the supply voltage.

The power regulation circuit is included because the logic parts of the imager, address generator and address decoder, are

realized with 2.5 V transistors. The chosen CMOS technology has two different kinds of transistors, i.e., 2.5 V transistors for digital circuits and 3.3 V transistors for the analog circuits. The advantage of the 2.5 V transistors is that smaller geometries are allowed than for the 3.3 V transistors. The digital circuits like address generator and address decoder are realized with 2.5 V transistors. This results in an area reduction of approximately 30% in comparison to a design using the 3.3 V devices. The sensor has only one external power connection pin. Therefore, an on-chip voltage regulation circuit in required. This is realized by a voltage divider with a buffer stage. For the layout this means that the chip has two power domains, i.e., a 2.5 V domain for digital switching and a 3.3 V domain for sensitive analog circuits. Control signals from the 2.5 V power domain to the 3.3 V power domain, like row addresses need a level shifter circuit to ensure correct operation. The main advantage of the two power domains is, that the in-coupled noise in the analog circuits caused by the switching activity in the digital parts is reduced. In the layout the power domain separation is achieved by an n-well and p-substrate guard ring surrounding all layout blocks.

C. Results and Discussion

Characteristics for bulk and TFC devices and test diodes for both sensor types have been compared experimentally:

TFC devices reveal values of dark current density as low as 10^{-10} A/cm^2. These results are similar to values for bulk silicon diodes fabricated in optimized CMOS processes. The higher band gap of α-Si:H (~ 1.8 eV) compared to that of silicon (1.12 eV) results in a potentially lower dark current ($< 10^{-10}$ A/cm^2) when compared to conventional silicon photodiodes. Experiments with different surface topography revealed that steep edges increase particularly the dark current of the amorphous diode system. The surface structure as shown in Fig. 9 indicates that surface topography is likely responsible for the observed dark current densities.

The spectral response was measured in the range of 400 nm to 750 nm as shown in Fig. 13. The thin film α-Si:H photodiodes have nearly two-fold higher spectral sensitivity compared to that of bulk silicon with a maximum at about 640 nm. The response is thus very similar to the sensitivity of the human eye. It is significantly higher in the green, yellow and red range of the visible spectrum than for the bulk diode.

Measurements of the minimum detectable illumination of the image sensors show a lower value of 0.1 lx for the TFC-device compared to 0.3 lx for the bulk sensor. Below the minimum detectable illumination an image signal might be obtained. The SNR is very poor, however, below the specified and measured minimum detectable illumination. The results agree with the larger fill factor of approximately 90% for the TFC device and about 30% for the silicon image sensor.

An image of a 100 W light bulb obtained by the image sensor (Fig. 14) as well as measurements demonstrate the high dynamic range of more than 120 dB for bulk Si and TFC Pixels, which is a result of the HDRC pixel cell used. Except of the known image lags in logarithmic pixels in the low illumination parts of the image no additional image lag is visible in video sequences.

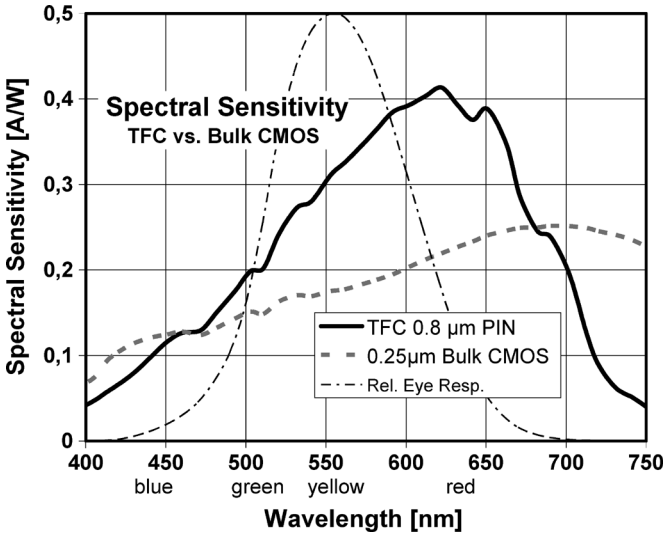

Fig. 13. Spectral response of a TFC diode in comparison to that of a bulk silicon diode.

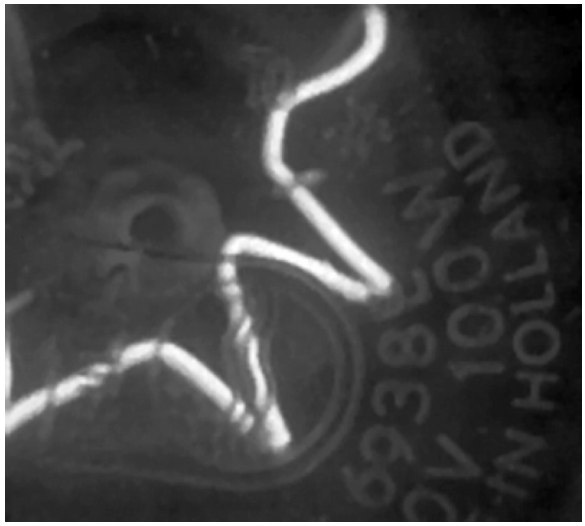

Fig. 14. A 180 by 200 pixel image grabbed from a video stream image, showing a light bulb, in which both the powered-on filament and the brand labels on the glass are visible.

IV. Conclusion

The two types of HDRC CMOS image sensors presented show the advantages of logarithmic response photosensitive cells for biological applications in an imperfect illumination-controlled environment.

In the retina implant application the chip delivers illumination-independent contrast signals to the biological tissue. This chip has recently been applied in a clinical trial (Fig. 15) at the Universitäts-Augenklink Tübingen (University Eye Clinic Tuebingen), Germany, with the result that partial vision could be restored to blind patients for the first time by a sub-retinal implanted photo sensitive device and electrically evoked perceptions by the retinal implant were reported by volunteers. The actual stimulation experiments result in a strong dependence of the stimulation thresholds on pulse mode, pulse duration and the actual conditions of the volunteers. Taking into account the

Fig. 15. Fundus photograph of a human eye with a sub-retinal implanted chip. The remaining retina on top of the chip is marked by its vessels. (Courtesy of Retina Implant AG).

concept dependent fixed pulse mode and the synchronous stimulation on all electrodes, the new modified implant circuit delivers adaptable electrical stimulation with matched power consumption. Furthermore a more stable operation to the effects of supply voltage modulations caused by the limited power line conductance was achieved.

For the second application, i.e., small and flexible endoscopes and surgery tools, a miniature image sensor was developed. An image sensor having a chip size of 1.1×1.5 mm^2 and only four terminals was fabricated. High fill factor pixels with a pixel pitch of 4.6 μm and a logarithmic response were obtained by deposition of amorphous silicon photodiodes above the HDRC CMOS sensor. In comparison to the state-of-the-art miniature CCD or CMOS imagers, the TFC sensor is the best choice if the focus is on low-cost products since it uses a common 0.25 μm CMOS foundry technology. Its only four terminals enable simple or even automated chip assembly and packaging processes, thus paving the way to the manufacturing of disposable endoscopes.

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