# High Dynamic Performance Current-Steering DAC Design With Nested-Segment Structure

Wei Mao, Yongfu Li, Chun-Huat Heng, and Yong Lian

***Abstract*— Dynamic performance of the current-steering digital-to-analog converter (DAC) is mainly affected by the mismatch-induced nonlinearity. Dynamic-element-matching (DEM) method has been widely employed to effectively improve the amplitude and timing mismatches. However, the maximum performance improvement is constrained by the conventional separate-segment structure for the current source array. In this brief, a DEM DAC with nested-segment structure is proposed to improve the mismatch performance. Compared with the best spurious-free dynamic range (SFDR) values obtained by the conventional DEM DACs, Monte Carlo simulations demonstrate that the proposed DAC achieves higher performance improvement with the same MSB bit width. The largest improvement occurs at MSB bit width of 3 with the 6.95- and 4.68-dB gain over two conventional designs, respectively. In terms of the digital complexity, the proposed architecture employs at least 2.7× fewer multiplexers compared with the reported DEM DACs, while achieving comparable dynamic performance. Fabricated in 130-nm CMOS process, the proposed 12-bit 100-MS/s DAC occupies 0.21 mm$^2$. Measurement results show that 1.9× integral nonlinearity reduction ratio and 15.5-dB SFDR improvement from 46.6 to 62.1 dB at near Nyquist frequency are achieved.**

***Index Terms*— Current-steering, digital-to-analog converter (DAC), dynamic-element-matching (DEM), mismatch-induced nonlinearity, nested segment, separate segment.**

## I. Introduction

The design of high dynamic performance current-steering digital-to-analog converter (DAC), especially with high spurious-free dynamic range (SFDR) value, requires significant effort in minimizing mismatch-induced nonlinearities [1]–[9]. The foreground calibration technique is one of the mismatch compensation methods [1]–[5]. By making use of the measured mismatch values, the linearity is improved by providing tuning current or rearranging the sequence of the current sources. However, this technique suffers from deteriorated dynamic performance at high frequency and large area penalty. Furthermore, the process voltage temperature (PVT) variation requires periodical recalibration. In contrast, the background calibration technique, especially the dynamic-element-matching (DEM) technique, effectively suppress the negative effects of mismatch-induced nonlinearities on the DAC's dynamic performance without the above-mentioned drawbacks [6]–[9].

In a DEM DAC, the units within the unary current source array are randomly selected. By adding the current from less-weighted binary current source array, the desired output current is generated. The harmonic distortions are reduced due to the averaging of mismatch error, which results in improved SFDR performance. Normally, the separate-segment structure is employed for the current source array. As shown in Fig. 1, the current sources of this structure are grouped into several separate segments, i.e., MSB segment, upper LSB (ULSB) segment, …, and LSB segment. The most weighted segments, such as the MSB and ULSB segments, are normally formed by unary current sources and controlled by individual DEM blocks. The remaining less-weighted segments are formed by the binary current sources and controlled by digital input directly. Although, the SFDR performance improves with the increasing bit width of the most weighted segments, especially the MSB bit width, the circuit complexity of DEM block increases exponentially with the increasing bit width. Besides, the digital blocks with larger stage number also results in time skew issue. Thus, the MSB bit width is usually fewer than 5 bits in the state-of-the-art DEM DAC designs [6]–[8]. This often limits the achievable SFDR performance. In this brief, we present a DEM DAC with nested-segment structure for better dynamic performance improvement.

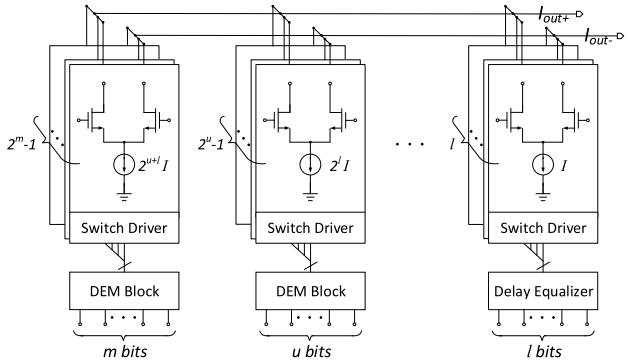


Fig. 1. Conventional DEM DAC with separate-segment structure.

This brief is organized as follows. In Section II, the structure of the proposed DEM DAC and the working principles are explained. In Section III, the dynamic performance improvement is verified by the Monte Carlo simulation and the multiplexer (MUX) count is benchmarked with other DEM-based DAC designs. The circuit implementation and the measurement results are presented in Section IV. Finally, the conclusion is given in Section V.

## II. Architecture

The DAC with the proposed nested-segment structure is segmented into three parts, i.e., MSB, ULSB, and LSB segments. The corresponding bit numbers are $m$, $u$, and $l$ bits, respectively. The $m$-bit MSB segment consists of $2^m$ MSB subarrays. Each MSB subarray will in turns contain $2^u$ ULSB subarrays, which can be chosen as an $u$-bit ULSB segment. Subsequently, each ULSB subarray will comprise of $2^l$ LSB unary current sources. Finally, $(2^l - 1)$ LSB unary current sources will constitute the $l$-bit binary-weighted LSB segment. The nested-segment structure is applied to MSB and ULSB segments only. The remaining LSB segment is controlled by the binary digital input directly.

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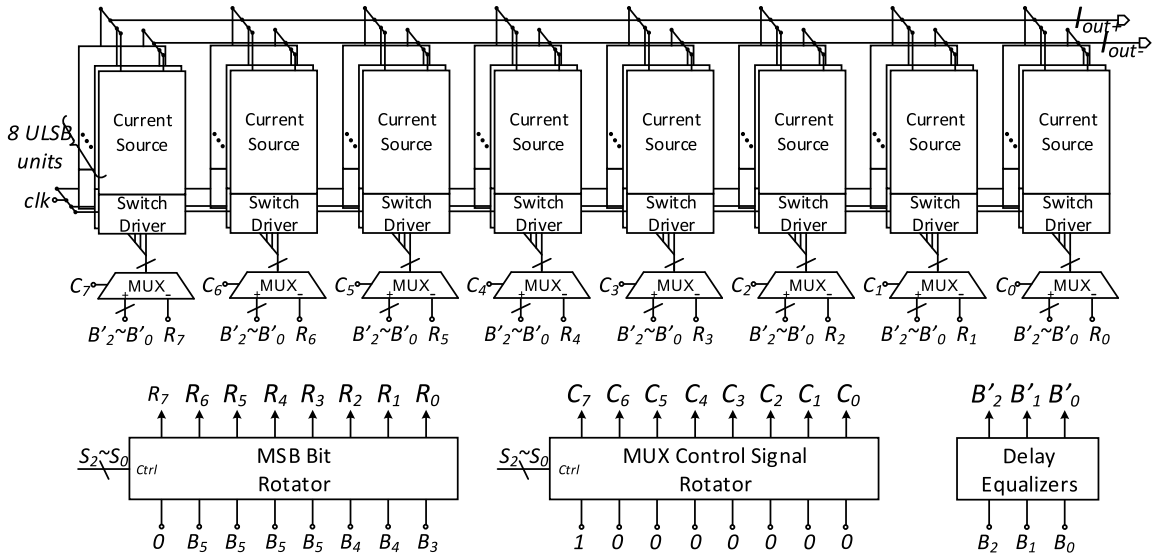



Fig. 2. Six-bit proposed DAC with nested-segment structure.

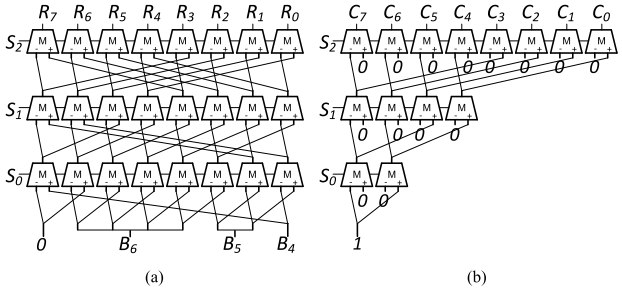



Fig. 3. Schematics of 3-bit MSB bit rotator and MUX control signal rotator. (a) MSB bit rotator. (b) MUX control signal rotator.

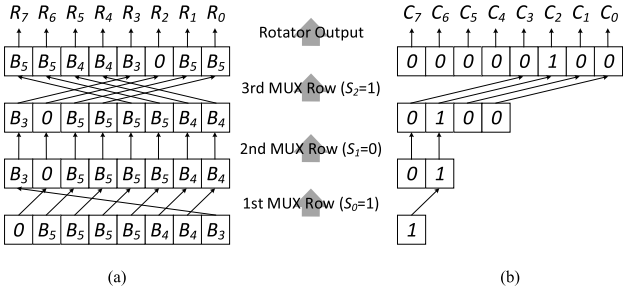



Fig. 4. Working principle of the rotators with $S_2$~$S_0$ equal to 101. (a) MSB bit rotator. (b) MUX control signal rotator.

In Fig. 2, a 6-bit DAC example is presented for illustrating the nested-segment structure and the corresponding DEM implementation. The total six bits $B_5$~$B_0$ are split into three MSB and three ULSB bits. Because the LSB part is controlled by digital input directly, the working principle of this part is the same as the conventional approach. The MSB segment consists of eight current source subarrays, with each subarray containing eight ULSB current source units. For each ULSB current source unit, the corresponding switch driver is provided. Thus, the ULSB segment is nested within the MSB segment, which means that any MSB unit can be selected as the ULSB segment. Besides, MUXs are added to each MSB unit for the control bit selection. The MSB bit rotator and MUX control signal rotator constitute the DEM block. The delay equalizer is employed for the ULSB control bits to compensate for the delay introduced by the rotator to the MSB control bits. The generated $B'_2$~$B'_0$ correspond to the delayed ULSB control bits.

The schematic of the 3-bit MSB bit rotator is shown in Fig. 3(a). The MSB bit rotator employs multilevel right-shifting barrel shifters to shift the digital input by 0~7 rotation steps from left to right. The amount of the total rotation steps is determined by the 3-bit shift input $S_2$~$S_0$ from pseudorandom number generator and changed each clock cycle. Thus, the initial MSB bits "$0B_5B_5B_5B_5B_4B_4B_3$" can be shifted with random rotation steps to generate the randomized MSB bits "$R_7R_6R_5R_4R_3R_2R_1R_0$." In Fig. 3(b), the 3-bit MUX control signal rotator is also controlled by $S_2$~$S_0$. Thanks to the predetermined control input, this rotator is a simplified version of the MSB bit rotator with fewer required MUXs while achieving the same shift functionality. After randomization, the generated MUX control bits "$C_7C_6C_5C_4C_3C_2C_1C_0$" determine which MSB subarray is chosen as the ULSB segment and which MSB subarrays are activated by the randomized MSB bits.

The working principles of the rotators are shown in Fig. 4. As shown, the shift input $S_2$~$S_0$ is randomly set to "101," which indicates a right-shifting amount of five. Hence, the original MSB bit sequence of "$0B_5B_5B_5B_5B_4B_4B_3$" has been randomly right-shifted by five resulting "$B_5B_5B_4B_4B_30B_5B_5$." Similarly, the initial MUX control bit sequence of "*10000000*" has also been right-shifted by five into "*00000100*." This implies that MSB subarray three from the right will be chosen as the ULSB segment, and the remaining subarrays will be activated by the randomized MSB bits shown in Fig. 4(a).

The proposed structure has several advantages over the conventional DEM structure. First, one more MSB subarray is available for DEM with no additional area penalty, which improves the overall dynamic performance. Second, although no DEM block is applied to the ULSB segment directly, the randomization effect for the ULSB segment is further achieved with our proposed technique. By randomly choosing one MSB subarray out of the eight as the desired ULSB segment, the current source units of the ULSB segment are randomized during each clock cycle. In Section III, the performance improvements over the conventional DEM DACs are analyzed in detail.

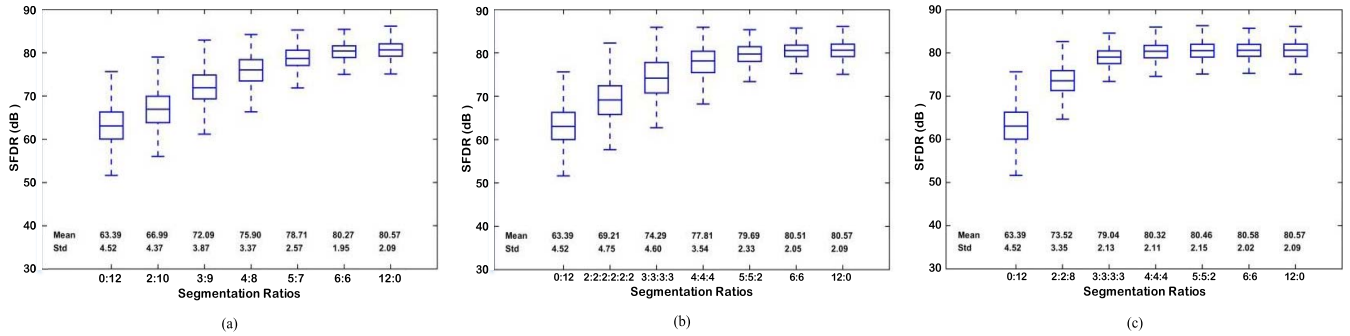



Fig. 5. Simulation results of three 12-bit DACs. Separate-segment DEM DAC with (a) single segmentation [8] and (b) multiple segmentations [6]. (c) Proposed nested-segment DEM DAC.

TABLE I
MUX COUNT COMPARISONS FOR DEM DACS WITH DIFFERENT STRUCTURES

| MSB Bits | Seg. Ratio | SFDR (dB) | MUX Count RRBS | MUX Count GRTC | Seg. Ratio | SFDR (dB) | MUX Count RRBS | MUX Count GRTC | Seg. Ratio | SFDR (dB) | MUX Count Proposed |
|---|---|---|---|---|---|---|---|---|---|---|---|
| 2 | 2T+10B | 66.99 | 6 | 6 | 2T+…+2T | 69.21 | 36 | 36 | 2T+2T+8B | 73.52 | 14 |
| 3 | 3T+9B | 72.09 | 21 | 14 | 3T+…+3T | 74.29 | 84 | 56 | 3T+3T+6B | 79.04 | 38 |
| 4 | 4T+8B | 75.90 | 60 | 45 | 4T+4T+4T | 77.81 | 180 | 135 | 4T+4T+4B | 80.32 | 94 |
| 5 | 5T+7B | 78.71 | 155 | 127 | 5T+5T+2T | 79.69 | 316 | 260 | 5T+5T+2B | 80.46 | 222 |
| 6 | 6T+6B | 80.27 | 378 | 255 | 6T+6T | 80.51 | 756 | 510 | 6T+6T | 80.58 | 510 |

## III. VERIFICATION AND COMPARISON

In this section, three behavioral models are constructed for comparison to verify the performance improvements. The first two models are the 12-bit conventional DEM DACs with the separate-segment structure based on single segmentation and multiple segmentations, respectively. The last model is the proposed 12-bit DEM DAC with nested-segment structure. For all the models, one sigma $\sigma$ of unit current source's static mismatch is set to 10%. The SFDR performance of three DACs are summarized based on 10 000 Monte Carlo simulations.

The single-segmentation separate-segment structure is often chosen to simplify the digital part and reduce the intersegment mismatch [8]. The DEM block is only implemented on the unary current sources of the MSB segment. For this structure, MSB to LSB segmentation ratio of 2:10, 3:9, 4:8, 5:7, and 6:6 are investigated. On the other hand, multiple-segmentation separate-segment structure is commonly adopted for better dynamic performance at the expense of more digital circuit [6], [7]. For this structure, the segmentation ratios of the multiple segments are set to 2:2:2:2:2:2, 3:3:3:3, 4:4:4, 5:5:2, and 6:6, respectively. This gives insight on the optimal segmentation ratio for achieving the best dynamic performance. The random rotation-based binary-weighted selection (RRBS) randomizer is employed as the DEM block, with which the best SFDR performance obtained by the DEM DAC has been reported [6]. For the proposed design, the segmentation ratios explored for the proposed DAC are 2:2:8, 3:3:6, 4:4:4, 5:5:2, and 6:6:0. Besides, the simulation results of DAC with "0:12" and "12:0" segmentation ratios are provided for comparison, which represent the "worst" and "best" SFDR performance of the 12-bit DAC with no randomization and full randomization, respectively. The SFDR values for each segmentation ratio are the average of the simulation results with normalized input frequencies ranging from (313/4096) to (1913/4096).

In Fig. 5, three box-whisker plots show the data distribution of the simulated SFDR results for the conventional and proposed DACs. The corresponding mean and $\sigma_{\text{SFDR}}$ values are also shown at the bottom of the plots. In these plots, increasing MSB bit width improves the SFDR performance with higher mean and smaller $\sigma_{\text{SFDR}}$ values. For the two conventional designs, the multiple-segmentation DACs outperform the single-segmentation ones with increasing MSB bit width from 2 to 6 by 2.22 to 0.24 dB. However, the $\sigma_{\text{SFDR}}$ values are worsened due to more dispersive combination of the current sources. For the proposed DAC with increasing MSB bit width from 2 to 6, the mean SFDR values are from 73.49 to 80.59 dB. The corresponding $\sigma_{\text{SFDR}}$ values decrease from 3.35 to 2.04 dB. Comparing with the conventional designs of the same MSB bit width, the proposed DAC achieved better performance with larger mean SFDR values. The largest improvement occurs at MSB bit width of 3 with the 6.95- and 4.68-dB gain, respectively. Meanwhile, the proposed DAC also observed smaller $\sigma_{\text{SFDR}}$.

To evaluate the DEM block complexity, the MUX counts for different structures are summarized in Table I. Given that the grouped random rotation thermometer code method can achieve comparable performance as RRBS method with the least DEM complexity [8], the MUX count is also listed in the table for comparison. As shown, the proposed DAC with MSB bit width of 3 and 4 can achieve comparable SFDR performance as the conventional designs with MSB bit width of 5 and 6. Hence, the required MUX count for the proposed design is about 2.7× and 5.4× fewer than the smallest MUX counts required by the conventional single-segmentation and multiple-segmentation architectures, respectively.

## IV. CHIP IMPLEMENTATION AND EXPERIMENTAL RESULTS

Fig. 6 presents the floorplan of the proposed 12-bit DEM DAC with nested-segment structure. "4T + 4T + 4B" segmentation type is implemented to verify the performance improvement. The DAC also incorporates the digital return-to-zero operation to remove the transient nonlinearity and obtain flat frequency response [7]. As DEM is not applied to the LSB segment, the hierarchical symmetrical sequence of LSB unit is adopted in the layout for gradient error compensation [10].

Fabricated in 130-nm 1P8M CMOS process, the DAC occupies a total area of 0.21 mm$^2$. The die photograph is shown in Fig. 7. The digital and analog supply voltages are 1.2 and 1.5 V, respectively.

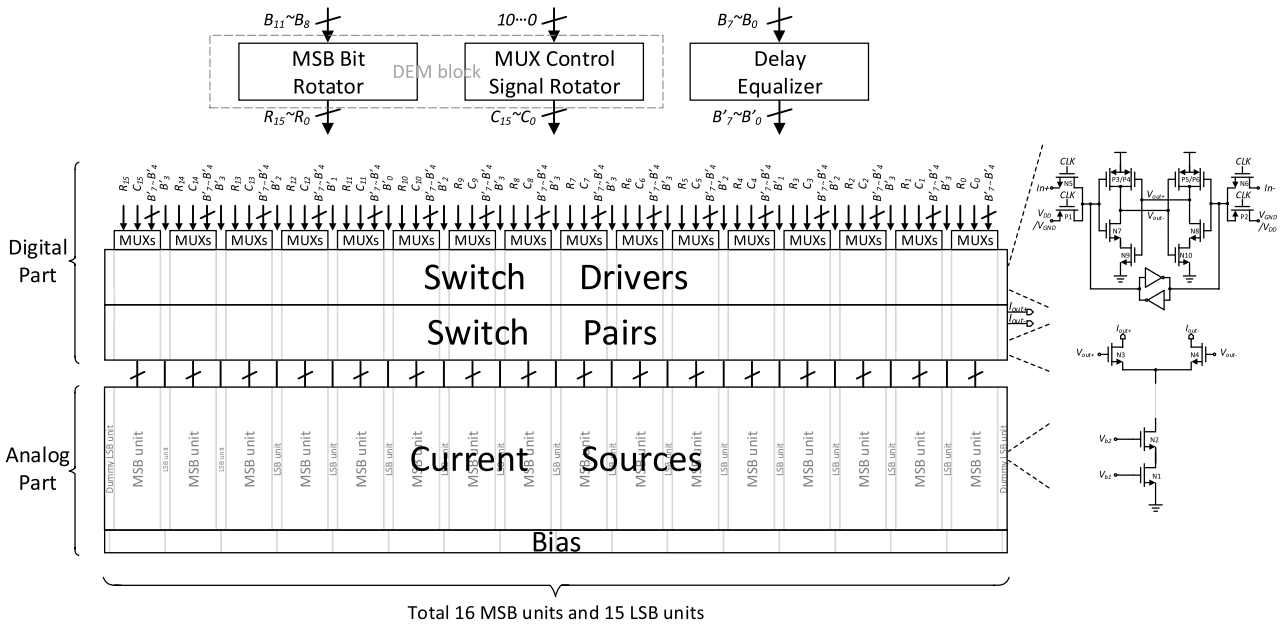



Fig. 6. Floorplan of the proposed DAC with circuit implementation.

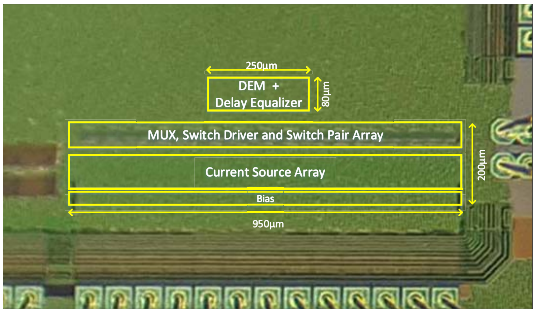



Fig. 7. Die photograph of the fabricated DAC.

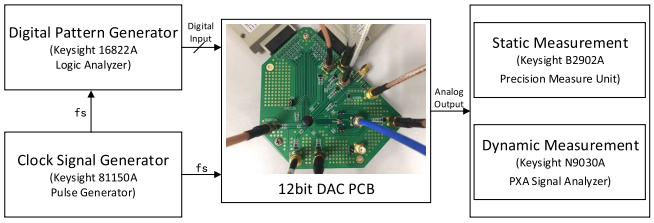



Fig. 8. Testbench for the DAC static and dynamic measurements.

The full-scale output current of the DAC is 16 mA. By driving off-chip 25-Ω differential load resistors, the peak-to-peak voltage swing $V_{\rm pp}$ is 800-mV.

Fig. 8 shows the measurement setup. All the instruments are from Keysight Technologies. The clock signals for the testbench are provided by the 81150A pulse generator. Based on the preloaded codes, the 16822A logic analyzer generates the digital patterns at the selected sampling frequency. For the static and dynamic performance analyses, the DAC output under the control of the ramp and sinusoidal digital patterns are measured by the B2902A precision measure unit and the N9030A spectrum analyzer, respectively.

The static linearity performance is tested under two conditions, without and with enabling the DEM block. Fig. 9(a) and (b) shows the corresponding measured integral nonlinearity (INL) values. For the segmented DAC with thermometer-coded units, the INL error is mainly affected by the intersegment mismatches. The proposed method randomizes the ULSB segment during each clock cycle,

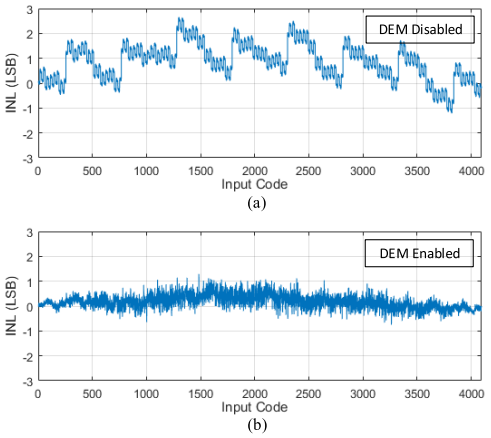



Fig. 9. Measured INL results of DACs with (a) disabling and (b) enabling the DEM block.

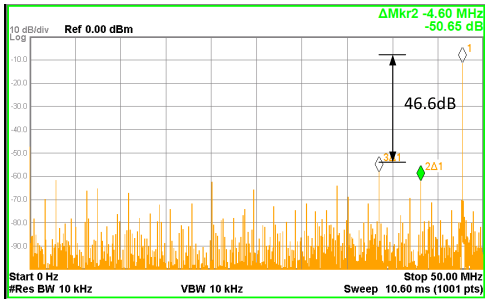
which averages the mismatches between ULSB and MSB/LSB segments with smaller values. As shown in the figure, it is supported from the measurement related to performance improvement. Thus, 1.9× INL performance improvement is observed with +2.7/−1.2 and +1.3/−0.7 LSB for the DEM-disabled and enabled DACs, respectively.

For the dynamic performance measurement, the proposed DAC is operating at 100 MS/s to generate a sinusoidal tone of 47.7 MHz. The measurement results are shown in Fig. 10. By comparing the results with disabling and enabling the DEM block, SFDR improvement of 15.5 dB from 46.6 to 62.1 dB is observed, which matches the performance improvement from simulation result shown in Section III.

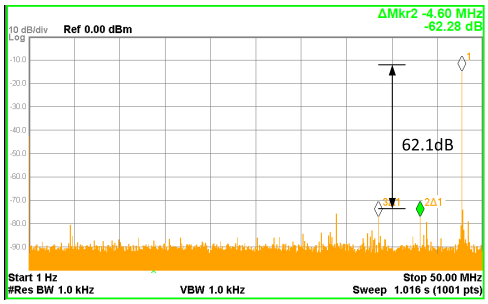
In Table II, the main performance of the state-of-the-art DACs [3], [7]–[9] and the proposed work are summarized. The figures-of-merit (FOM) value is calculated by [7]

$$\text{FOM} = \left( \frac{2^{\frac{\text{SFDR}_{\text{DC}} - 1.76}{6.02}} \times 2^{\frac{\text{SFDR}_{\text{Nyquist}} - 1.76}{6.02}} \times f_{\text{clk}}}{P_{\text{total}} - \frac{1}{2} I_{\text{load}}^2 \times R_{\text{load}}} \right). \quad (1)$$

This FOM evaluates the overall performance by considering energy efficiency, the SFDR variation and the sampling frequency.




(a)




(b)

Fig. 10. Measured SFDR performance of DACs with 47.7-MHz input signal at 100-MS/s with (a) disabling and (b) enabling the DEM block.

TABLE II

PERFORMANCE SUMMARY AND COMPARISONS

| Design | [3] | [7] | [8] | [9] | This Work |
|---|---|---|---|---|---|
| Resolution | 12 | 12 | 14 | 8 | 12 |
| Tech.(nm) | 90 | 40 | 180 | 90 | 130 |
| Supply (V) | 1.2/2.5 | 1.2 | 1 | 1.2/2.5 | 1.2/1.5 |
| $f_{clk}$ (MS/s) | 400 | 1600 | 500 | 1600 | 100 |
| $I_{load}$ (mA) | 26.7 | 16 | 10 | 20 | 16 |
| $P_{total}$ (mW) | 92 | 40 | 67.7 | 90 | 18 |
| Area ($mm^2$) | 0.18 | 0.016 | 0.55 | 0.16 | 0.21 |
| $SFDR_{DC}$ (dB) | 73.6 | 74 | 83.7 | 64.5 | 68.3 |
| $SFDR_{Nyq}$ (dB) | 59 (30MHz) | 70.3 | 68.9 | 57 | 62.1 |
| FOM [7] | 1.45e+7 | 4.43e+8 | 4.06e+8 | 1.49e+7 | 1.91e+7 |

## V. CONCLUSION

In this brief, the DEM DAC with nested-segment structure is proposed to improve the dynamic performance. From the Monte Carlo simulations, the largest SFDR performance improvements of 6.95 and 4.68 dB over two conventional DEM DACs are achieved at MSB bit width of 3. The proposed DAC can achieve comparable performance as the conventional ones with two fewer MSB bits used for DEM, which simplifies the DEM block significantly by reducing the MUX count more than 2.7×. The performance improvement also has been verified by the measurement results. 1.9× INL reduction ratio and 15.5-dB SFDR improvement at near Nyquist frequency are obtained.

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