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BD180 – a new 0.18 μm BCD (Bipolar-CMOS-DMOS) Technology from 7V to 60V

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***Abstract* — We present a new BCD technology in a 0.18 μm technology platforms with a capability of 7 to 60V high-voltage devices such as DEMOS and LDMOS. The developed 0.18 μm BCD process provides various kinds of high voltage LDMOS such as 7, 12, 20, 50, 60 V LDMOS transistors for variety of applications. The power LDMOS transistors in the process have very competitive specific on-resistance compared to previous results.**

I. INTRODUCTION

BCD (Bipolar-CMOS-DMOS) process [1-5] is widely used in a variety of areas such like large display (TV and monitor), small display (hand-held and mobile), POE (Power –On-Ethernet), and storage controller chip. Recently, many companies have made an effort to combine a power management, logic, audio and communication functions in a single chip. Therefore, more and more large logic contents has been integrated in a BCD technology [1-2]. This paper presents newly developed BCD process based on 0.18 μm logic platforms and the process has an operating voltage from 7 V to 60 V for high-voltage devices. The process involves high-voltage DE (drain-extended) CMOS, LDMOS (lateral double-diffused MOS), BJT (bipolar junction transistor), low TC (temperature coefficient) resistor, 1~2 fF/um^2 MIM (metal-insulator-metal) capacitor, and so on. Retrograded well structure, STI (shallow trench isolation), and other key technologies in a 0.18 μm standard process are used in the BD180 technology.

II. PROCESS SUMMARY OF BD180

Starting material is a p-epi wafer with resistivity of 7 ohm-cm on P$^+$ substrate. NBL (N$^+$ Buried Layer) is formed on it using Sb (antimony) implants. NBL is used for vertical NPN transistor (collector), high-side LDMOS, and isolated devices. Then, the p-type epitaxial layer, with an appropriate doping concentration and a thickness, is grown on NBL to achieve high breakdown voltage up to 60V n/pLDMOS. Deep N+ sinker is used for isolation and NPN collector as well. In the process, there are two HV wells, which are HVNWELL and HVPWELL, for high-voltage devices. HV wells are designed to achieve high breakdown voltage of 85V and 100V for NLDMOS and PLDMOS, respectively. There are two drift regions (NDT and PDT) for mid-voltage devices. The key process flow is shown in Fig. 1. The process offers up to six level metals and the top metal with a thickness of 2.7 μm.

Electrical parameters for 1.8V/5V CMOS, bipolar, diode, resistor, capacitor, and EEPROM are summarized in Table 1.

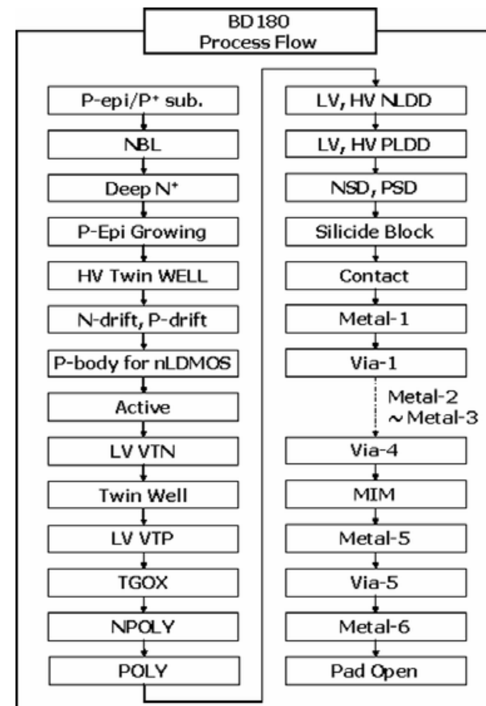


FIG. 1. KEY PROCESS FLOW OF BD180.

TABLE 2. ELECTRICAL PARAMETERS FOR 1.8V/5V CMOS, BIPOLAR, DIODE, POLY RESISTOR, CAPACITOR, AND EEPROM.

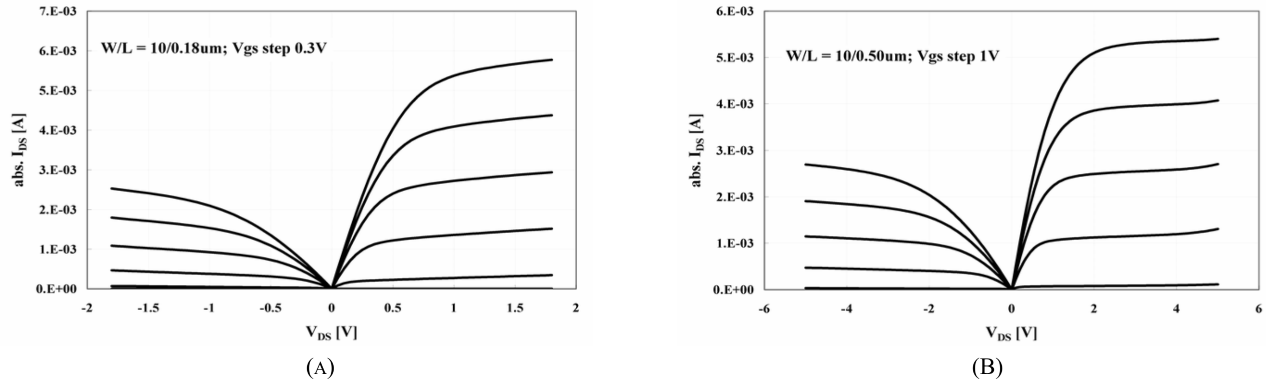
CMOS	V_T [V]	I_{DSAT} [µA/µm]	I_{off} [pA/µm]
1.8V NMOS	0.42	615	10
1.8V PMOS	-0.48	-260	6.5
5V NMOS	0.7	560	8.9
5V PMOS	-0.7	-290	9.2
Bipolar	**Hfe**	**BV_{CEO} [V]**	
Vertical NPN	84	27.4	
LPNP	118	28.2	
SPNP	37	33.4	
Diode	**V_F [V]**	**V_R [V]**	
Zener	0.7	5.6	
Bulk Zener	0.63	6.5	
Power Diode		60	
Resistor	**Res. [Ω/sq.]**		
Poly HSR	2000		
Low TCR	240		
Capacitor	**Density [fF/µm²]**	**BV [V]**	
MIM	1.0	34	
	2.0	21	
EEPROM	**VT_PGM[V]**	**ID_ERS [µA]**	
Single poly	5.4	47	

1.8V CMOS is fully compatible with the standard 0.18µm logic process allowing commercial library usages. We implemented 5V CMOS for I/O and core as well for analog circuits. Fig. 2 shows the 1.8V and 5V CMOS I_{DS}-V_{DS} characteristics.

Since BD180 has very modular fashion and various kinds of process differentiation is possible, e.g. 1.8V/5V/HV, 5V/HV, 1.8V/5V CMOS, and 5V power CMOS process. Fig. 3 shows the cross-sectional view of our BD180 process including 1.8V/5V CMOS, high-voltage DECMOS, N/PLDMOS and BJT. For analog design, bipolar transistor, 5V CMOS, MIM capacitor, resistor, and zero TC (temperature coefficient) resistors are available. In addition, a single poly EEPROM, OTP, Zener diode, and typical resistors, capacitors, and diodes are provided in the process.

III. HIGH-VOLTAGE DEVICE

In the BD180 process, LDMOS transistors are provided as a main switch device and high-voltage DECMOS are also provided for driving circuitry. As shown in Fig. 3, high voltage (30~60V) LDMOS has a field oxide between the gate and the drain while low voltage (12~20V) LDMOS doesn't. Both of n-ch and p-ch LDMOS for operating voltage from 7V to 60V are available in the BD180 process. Electrical



(A) (B)

FIG. 2. EXPERIMENTAL IDS-VDS CHARACTERISTICS FOR (A) 1.8V CMOS (B) 5V CMOS

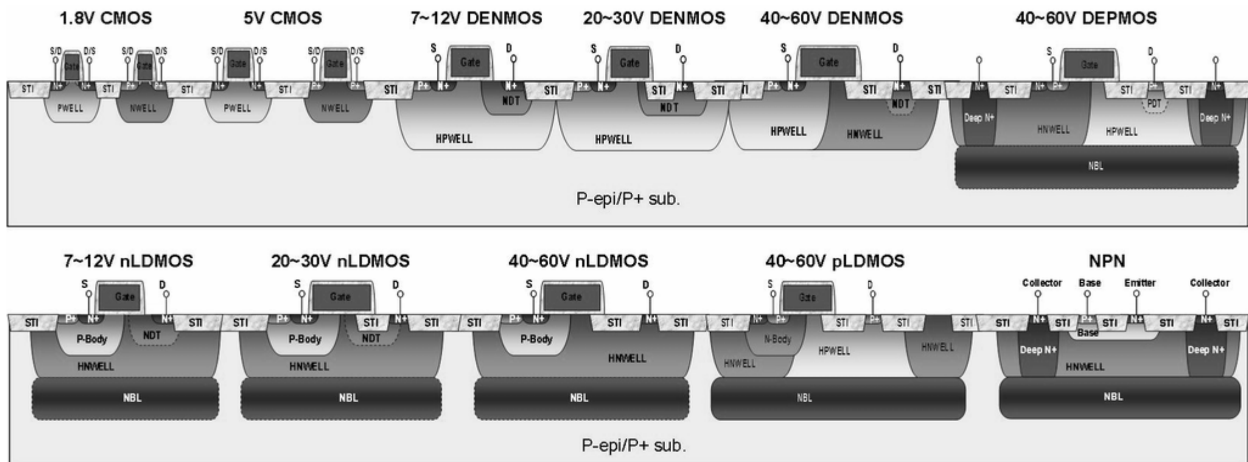


FIG. 3. CROSS-SECTION OF THE BCD TECHNOLOGY.

parameters for high voltage DECMOS and LDMOS are listed in Table 2. For the high-side operation, n-ch LDMOS with NBL layer is implemented to avoid the punch-through breakdown. In addition, p-ch LDMOS is also provided in the process, which can simplify the driving circuitry eliminating charge pump and external capacitor. Each device shows very competitive specific on-resistance at a given breakdown voltage.

TABLE 2. ELECTRICAL PARAMETERS FOR HIGH VOLTAGE DENMOS, DEPMOS, N-CH LDMOS, AND P-CH LDMOS.

DECMOS	BVdss [V]	R_{sp} [mΩ-mm²]	V_T [V]
7V DEN	13	4.9	0.97
7V DEP	16.1	36	-0.84
12V DEN	23	15.2	0.96
12V DEP	20	59.8	-0.83
25V DEN	55	74	0.88
25V DEP	52	250	-0.77
55V DEN	74	280	0.82
55V DEP	77	600	-0.73
65V DEN	>100	416	0.82
65V DEP	88	1300	-0.73
n-ch LDMOS	**BVdss [V]**	**R_{sp} [mΩ-mm²]**	**V_T [V]**
7V nLDMOS	15.3	5.7	0.9V
12V nLDMOS	17.5	9.1	0.9V
22V nLDMOS	34.0	21.5	0.9V
50V nLDMOS	73.5	72.8	0.9V
60V nLDMOS	80.0	87.9	0.9V
p-ch LDMOS	**BVdss [V]**	**R_{sp} [mΩ-mm²]**	**V_T [V]**
12V pLDMOS	17.5	37.2	-1.05V
22V pLDMOS	29.0	65.3	-1.05V
50V pLDMOS	71.5	212.8	-1.05V
60V pLDMOS	83.0	246.3	-1.05V

Fig. 4 shows the I_{DS}-V_{DS} characteristics for 50V n-ch and p-ch LDMOS transistors. For the high voltage ranges (40~60V), HVNWELL and HVPWELL are used as a drift region. HVWELL, however, is not suitable for low and medium voltage (7~30V) LDMOS transistors. Thus, we employed additional layers (NDT and PDT) with a dose around 1e13 cm^{-3} to optimize the low and medium voltage devices. Using the NDT, the 22V LDMOS shows the breakdown voltage of 34V and the specific on-resistance of 21.5 mΩ·mm².

Fig. 5 shows the micrograph of the cross-sections for 50V LDMOS structure. The simulated 50V LDMOS structure with a doping profile and a potential distribution at breakdown are illustrated in Fig. 6. The simulated breakdown voltage and the specific on-resistance are 72 V and 79 mΩ·mm², respectively. The simulation results show very good agreement with the experimental results. Fig. 7 shows the trade-off performance between the breakdown voltage and the specific on-resistance for n-ch and p-ch LDMOS, respectively. The n-ch LDMOS shows good performance compared to previous 0.18 µm BCD technology [1]. Especially, at high voltage ranges, the devices show better BV vs. $R_{ON,sp}$ performance than previous ones. For the p-ch LDMOS, our work shows higher on-resistance than that in [1], which is due to the fact that the doping concentration of the HVPWELL is low enough to achieve a high breakdown voltage up to 80V while the previous result shows maximum breakdown voltage of 60 V.

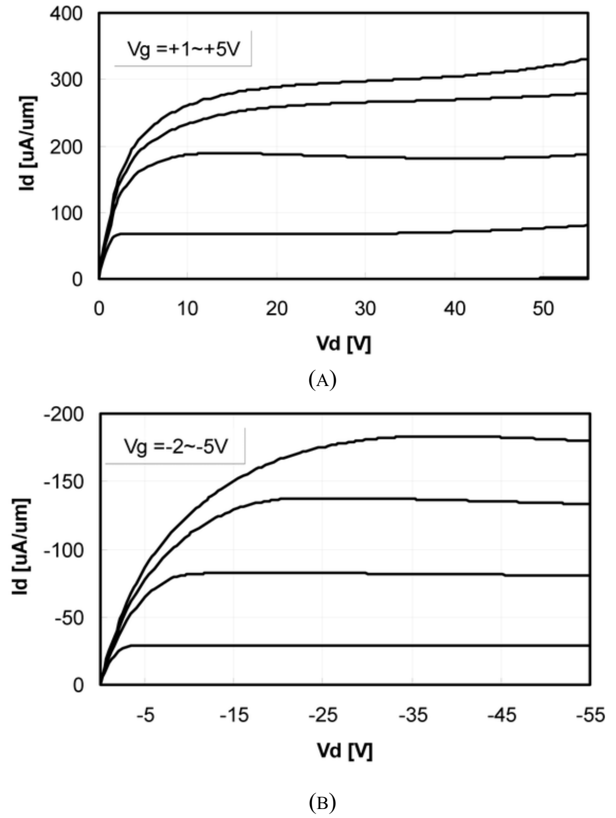


FIG. 4. EXPERIMENTAL IDS-VDS CHARACTERISTICS FOR 50V (A) N-CH AND (B) P-CH LDMOS.

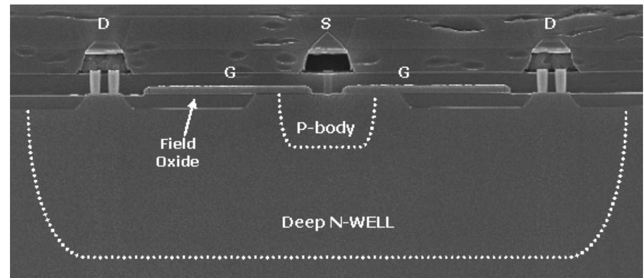


FIG. 5. SEM CROSS-SECTIONAL VIEW OF A HIGH-VOLTAGE LDMOS STRUCTURE.

IV. CONCLUSION

BD180 – a new 0.18 µm BCD process – was developed by integrating standard 0.18 µm CMOS with 5V CMOS, high-voltage devices, BJT and analog components. High-voltage devices such as DECMOS and LDMOS have been

materialized in the wide range of operating voltage from 7V to 60V with very competitive on-resistance. MIM capacitor with 1~2 fF/um2, high poly resistor with 2 KΩ/sq., and zero TC resistors are available using an optional mask layers for each components. P-ch LDMOS will be further optimized by using PDT layer in the drift region. Developed BD180 technology can be a very useful backbone process for applications in large and small display area, audio amplifier, and motor driver ICs for storage and automotive.

ACKNOWLEDGMENT

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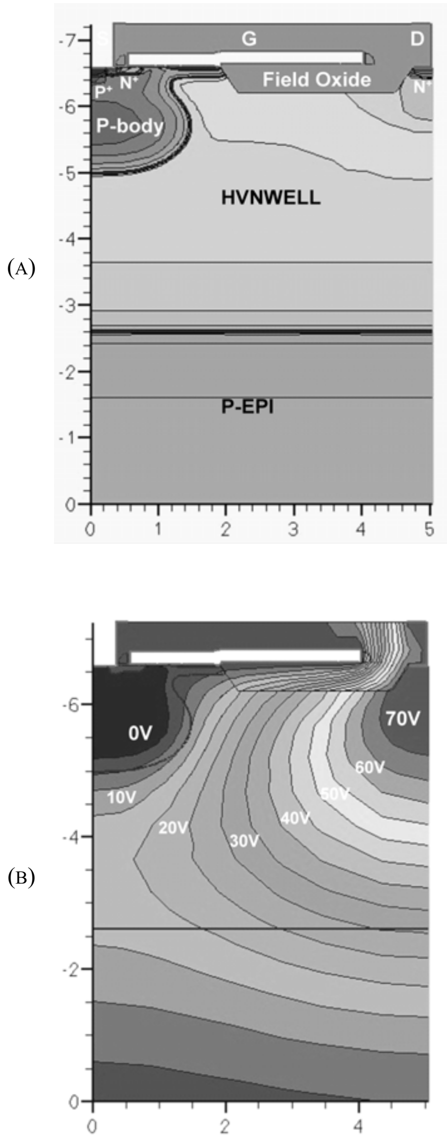
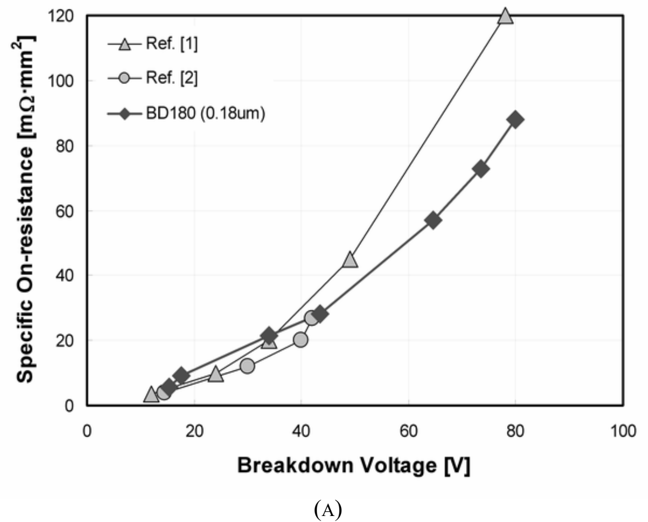


FIG. 6. SIMULATED LDMOS STRUCTURE. (A) 50V LDMOS STRUCTURE WITH A DOPING PROFILE, (B) POTENTIAL DISTRIBUTION AT BREAKDOWN (BV=72V) WITH 5V SPACING BETWEEN THE LINES



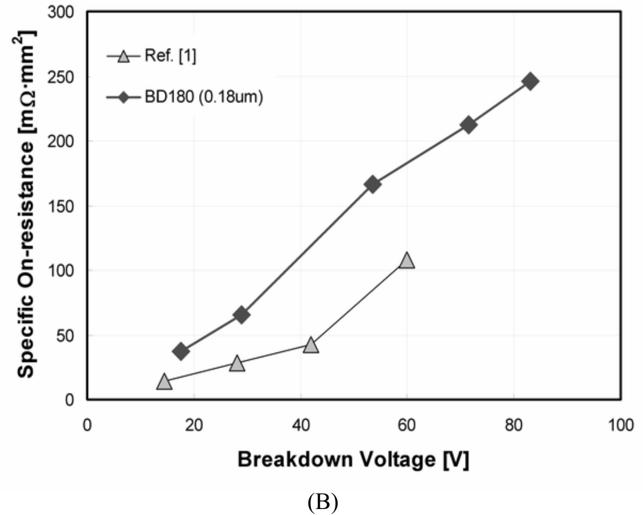


FIG. 7. TRADE-OFF CHARACTERISTICS BETWEEN THE BREAKDOWN VOLTAGE AND THE SPECIFIC ON-RESISTANCE FOR THE (A) N-CH AND (B) P-CH LDMOS.