Dynamic-Offset Cancellation Techniques in CMOS

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Motivation

- Many analog circuits e.g. opamps, integrators, comparators, ADC and DAC stages etc. require amplifiers with offsets in the **microvolt** range

- Also, many sensors (e.g. thermopiles, bridges, hall-effect sensors etc.) output DC signals that need to be processed with **microvolt** precision

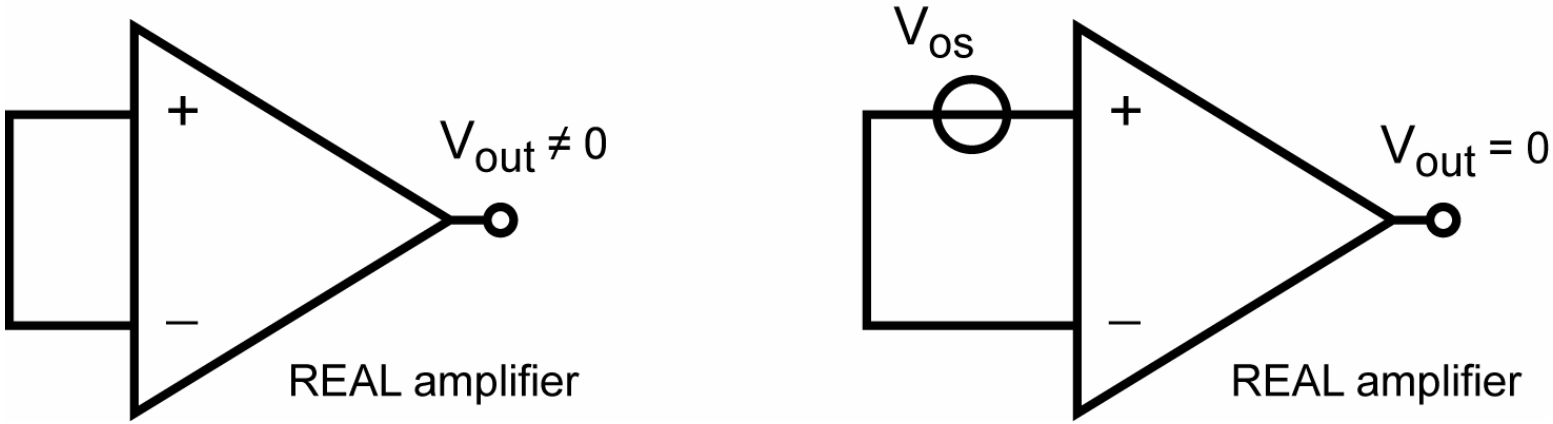
- However, the offset of native CMOS amplifiers is typically in the **millivolt** range

- This tutorial will focus on **dynamic** offset-cancellation (DOC) techniques, with which offset can be reduced to the **microvolt** level.

Outline

- Differential amplifiers
  - Offset and 1/*f* noise
- Trimming
- Dynamic Offset Cancellation
  - Auto-zeroing
  - Chopping
- Design of a CMOS temperature sensor
- Summary
- References

What is Offset?



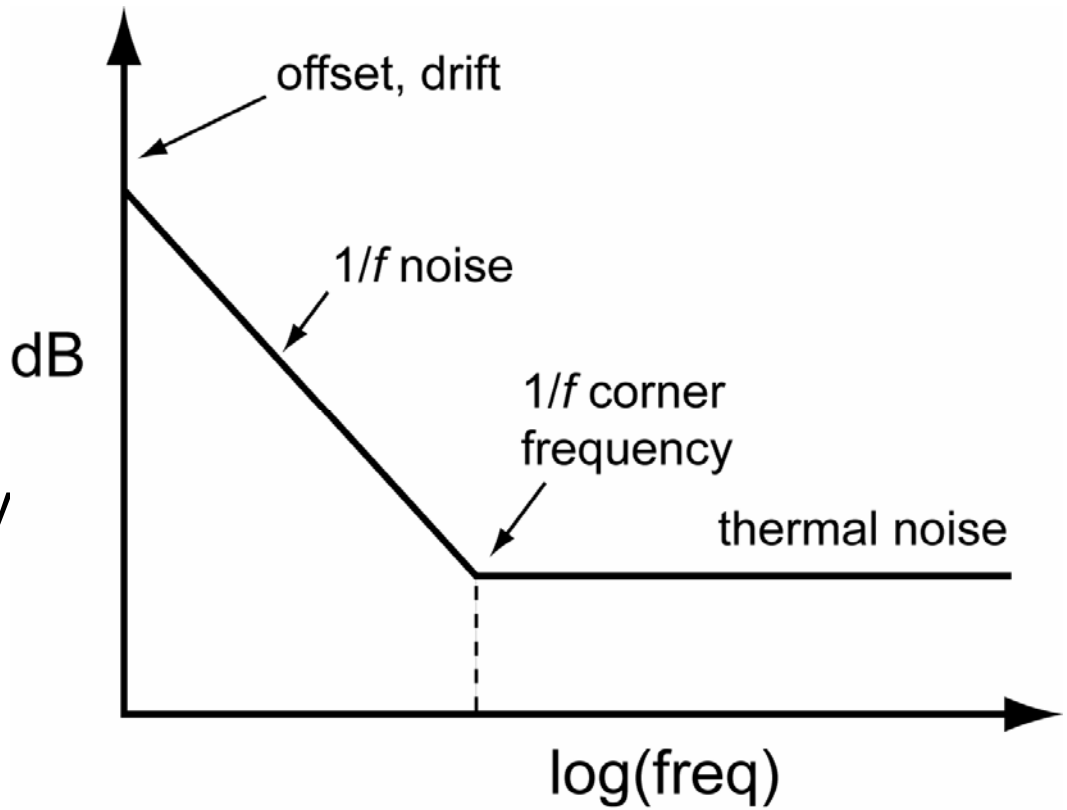
- When the input of a REAL amplifier is shorted, $V_{out} \neq 0$!
- The **offset** V_{os} is the input voltage required to make $V_{out} = 0$. It is typically in the range 100μV to 10mV.

- Note: In CMOS, input currents are usually negligible.

Amplifier Behaviour Near DC

Characterized by

- Offset
- Drift
- 1/*f* (flicker) noise
- Thermal noise
- 1/*f* corner frequency
- Errors due to finite CMRR and PSRR

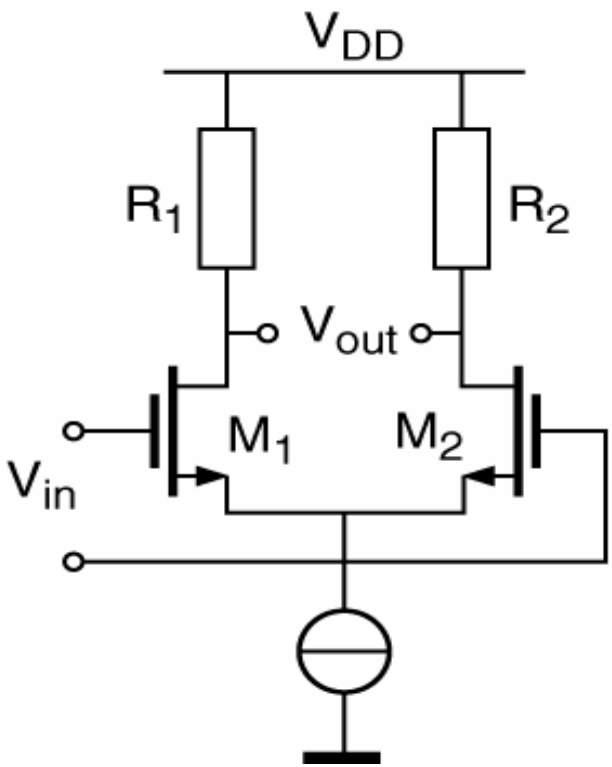


Differential Amplifiers

Differential amplifiers are often used to amplify DC signals.

Their balanced structure is

- Nominally offset free
- Rejects common-mode and power supply interference
- Easily realized in both CMOS and bipolar technologies

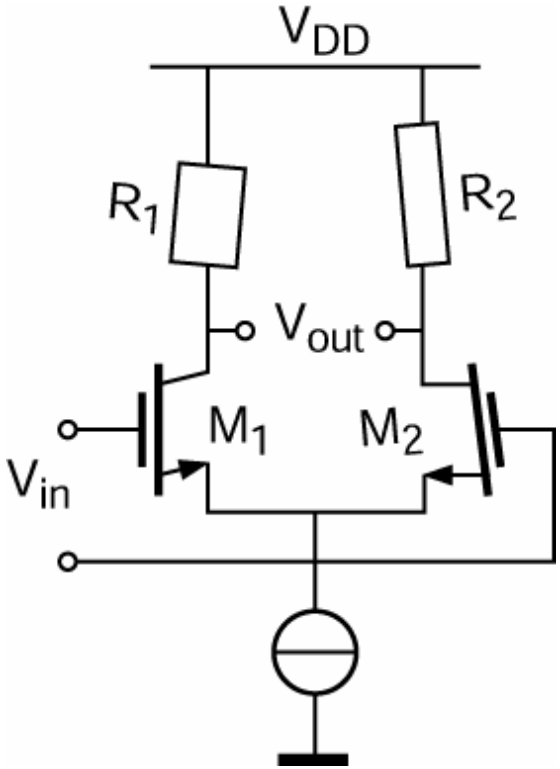


Offset in Differential Amplifiers

Component mismatch
e.g. $R_1 \neq R_2$, $M_1 \neq M_2 \Rightarrow$ **offset**

Mismatch is mainly due to
- Doping variations
- Lithographic errors
- Packaging & local stress

All things being equal
- Bipolar $\Rightarrow V_{os} \sim 0.1mV$
- CMOS $\Rightarrow V_{os}$ is 10 -100x worse!



What to Do?

Offset and 1/*f* noise are part of life!

But we can reduce offset “enough” by

1. Using “large” devices and good layout[1] $\Rightarrow$ 1mV
2. Trimming $\Rightarrow$ 100μV
3. Dynamic offset-cancellation (DOC) techniques $\Rightarrow$ 1μV

DOC techniques also

- Reduce drift and 1/*f* noise
- Improve PSRR and CMRR

Trimming

- Low circuit complexity
- Minimal effect on circuit bandwidth
- Requires a memory element, e.g.
  - Fusible links (Zener diodes)
  - Laser-trimmed resistors
  - Floating gate MOSFETs
  - PROM
- Requires test infrastructure
- Does not reduce drift or 1/*f* noise
- Poorly defined temp. dependence of MOSFETs
  $\Rightarrow$ offset after trimming > 100µV over temp.

Dynamic Offset Cancellation (DOC)

Two basic ideas[2]

1. Measure the offset somehow and then subtract it from the input signal $\Rightarrow$ Auto-zeroing

2. Modulate the offset away from DC and then filter it out $\Rightarrow$ Chopping

DOC Techniques

Auto-zeroing

Discrete time

Sample offset, then subtract.

Chopping

Continuous time

Modulate offset away from DC, then filter.

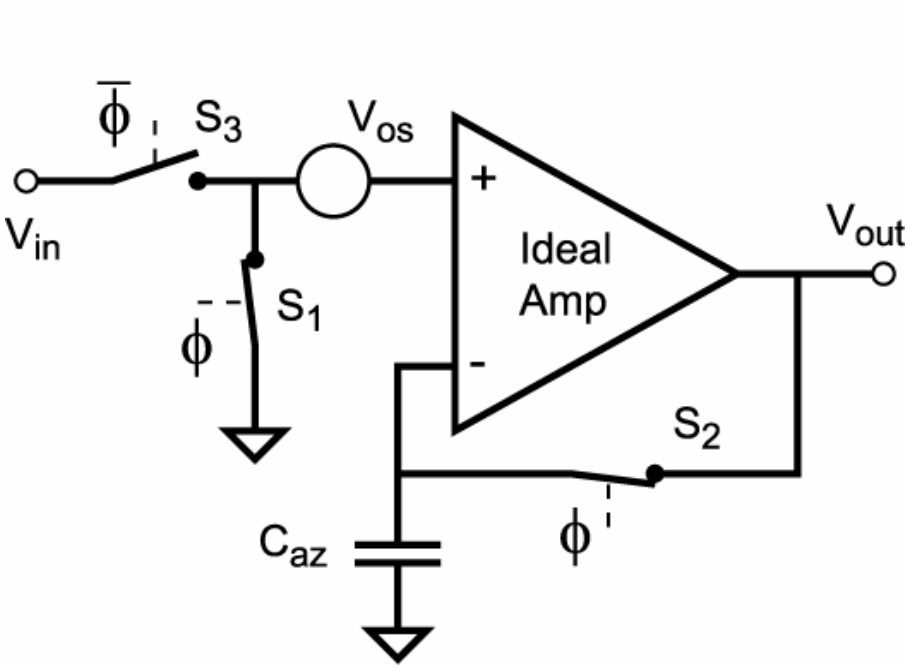
Switches required $\Rightarrow$ CMOS or BiCMOS

DOC Techniques vs. Trimming

+ reduction of offset and 1/*f* noise
+ excellent stability (over temperature, time, supply and common-mode voltages)
+ no additional costs for testing

- possible bandwidth reduction
- increased circuit complexity
- aliasing & intermodulation issues

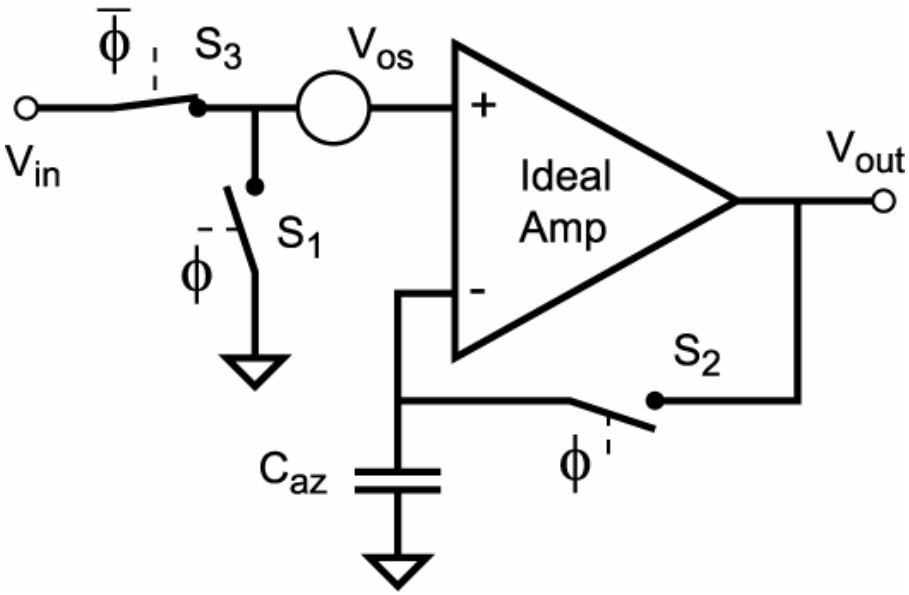
Auto-zero Principle (1)



Auto-zero phase

- S_1, S_2 closed, S_3 open $\Rightarrow V_{out} = V_{os}$
  $\Rightarrow$ offset stored on C_{az}
- Amplifier is unavailable

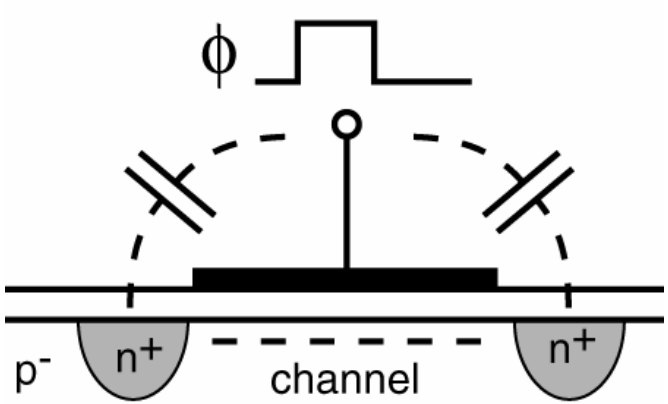
Auto-zero Principle (2)



Amplification phase:

- S_1, S_2 open, S_3 closed $\Rightarrow$ V_{in} is amplified
- *Finite* voltage gain A $\Rightarrow$ error in sampled offset
  $\Rightarrow$ input-referred residual offset $V_{res} = V_{os}/(A+1)$
- Charge injection is also a problem …

Charge Injection (1)

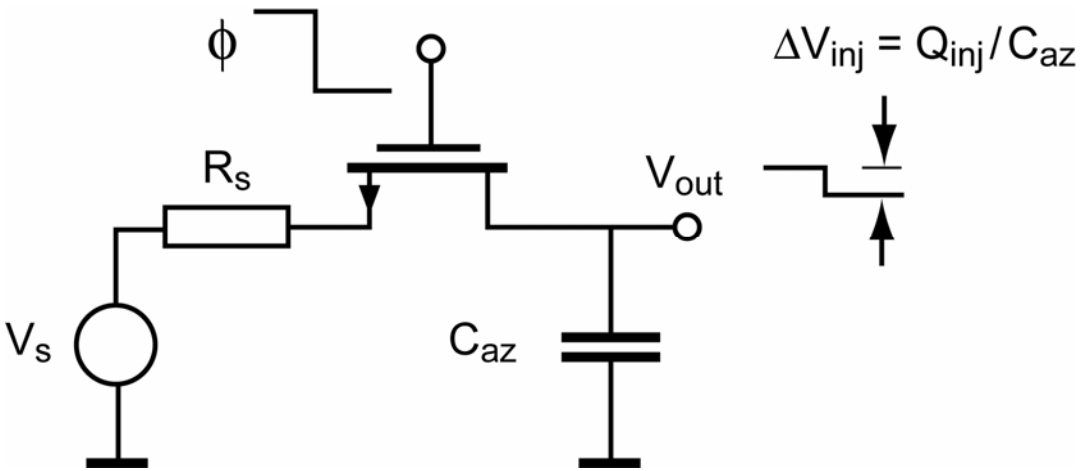


Consists of two components

1. Channel charge, $Q_{ch} = WLC_{ox}(V_{GS}-V_t)$
2. Charge in the overlap capacitance between the gate and the source/drain $\Rightarrow$ clock feed-through

Problematic when a MOSFET switches **OFF**.

Charge Injection (2)

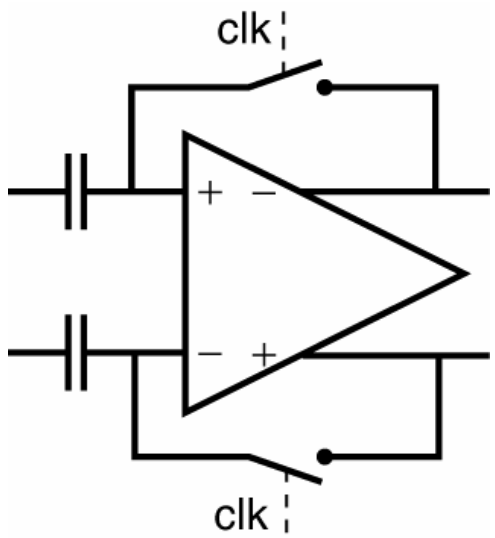


Error voltage ΔV_{inj} depends on many factors[3,4]

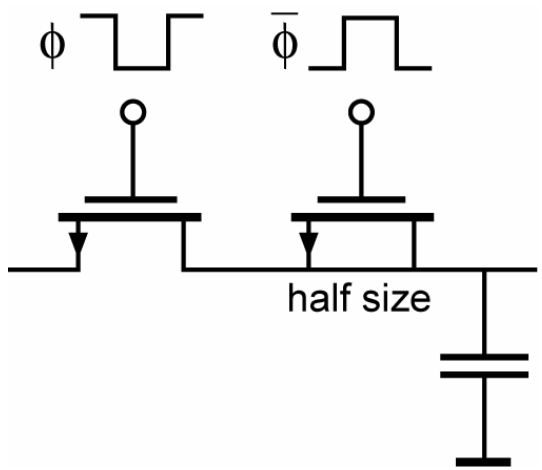
- Source voltage and impedance
- Transistor area (WL)
- Clock amplitude & slew rate
- Value of C_{az} (larger values $\Rightarrow$ smaller errors)
- In a 0.7µm process, minimum size NMOS switch, 2.5V step & 10pF $\Rightarrow \Delta V_{inj}$ ~ 250µV

Mitigating Charge Injection (CI)

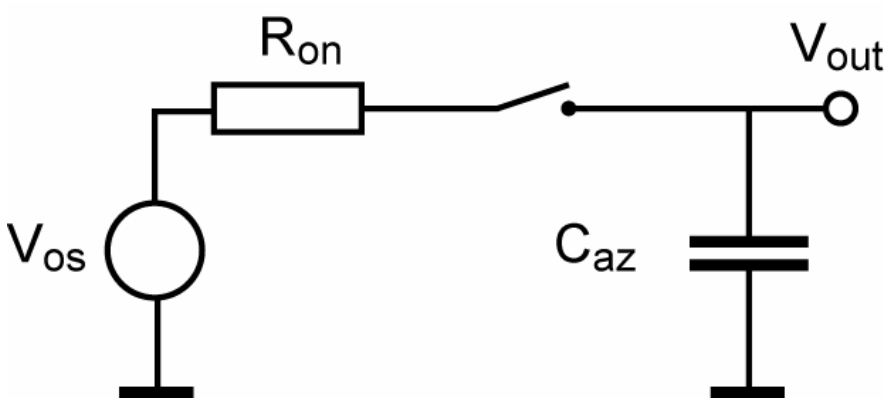
- Use differential topologies
  $\Rightarrow$ common-mode CI
  $\Rightarrow$ 1st order cancellation
- Use minimum size switches
  (subject to noise & BW requirements)



- For single-ended topologies
  dummy switches help[3,4]
- **But** area of main switch will be
  ~2x minimum size $\Rightarrow$ more CI
  $\Rightarrow$ limited benefit

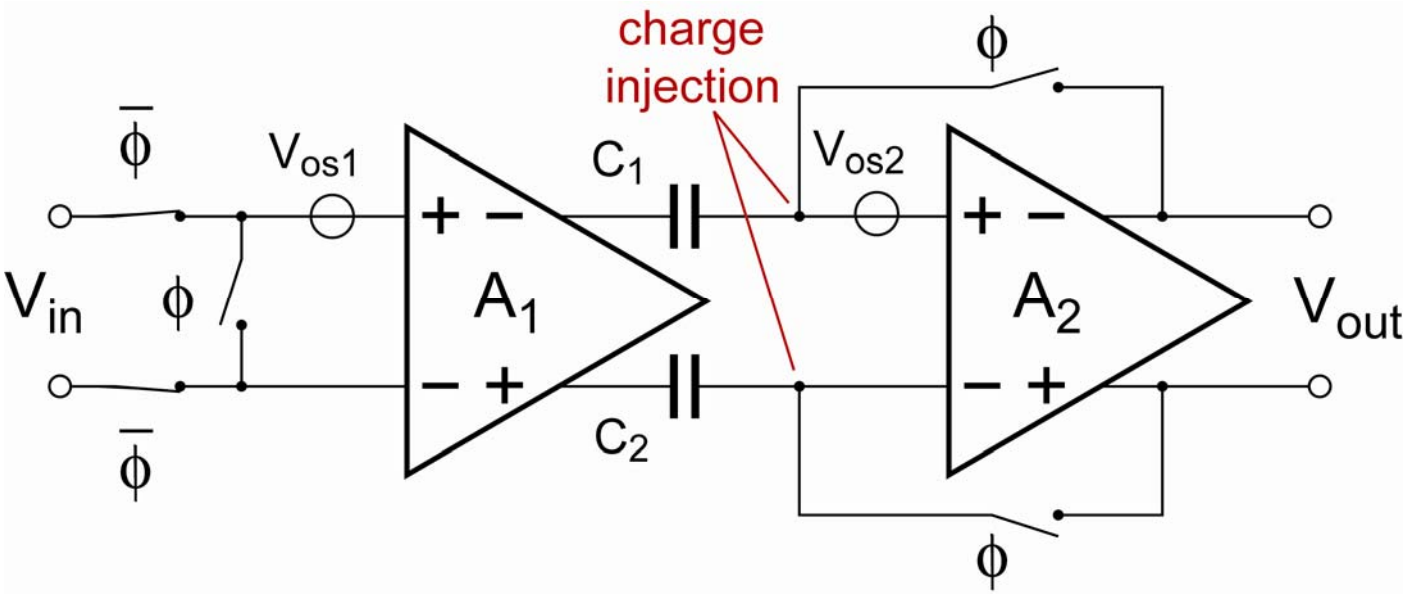


Sampling the offset: kT/C noise



- Thermal noise of R_{on} is filtered by C_{az}
- When the switch is opened the instantaneous noise voltage is held on C_{az}
- Total noise power = kT/C_{az} (10pF @ 300K $\Rightarrow$ 20.3μV)
- Large capacitance $\Rightarrow$ accurate sampling of V_{os}

Reducing Capacitor Size (1)

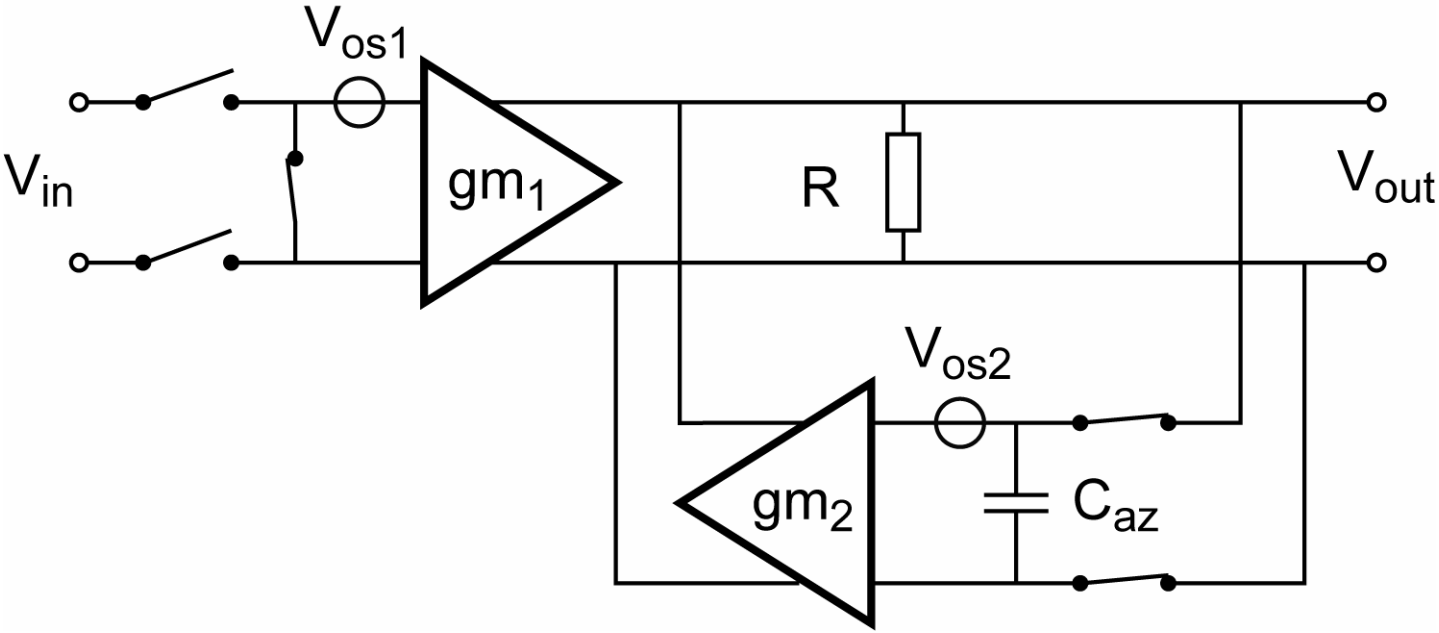


$V_{res} = V_{os2}/(A_1A_2) + \Delta V_{inj}/A_1$

- Offset of 1st amplifier is cancelled[5,6]
- Gain of 1st amplifier reduces offset of 2nd amplifier
- **But** too much gain $\Rightarrow$ clipping!
- Also reduces kT/C noise and charge injection errors

$\Rightarrow$ Sampling capacitors can be smaller

Reducing Capacitor Size (2)



Amplifier with an auxiliary input[7,8]

- $V_{res} \sim V_{os1}/(gm_2R) + V_{os2}/(gm_1R) + \Delta V_{inj}(gm_2/gm_1)$
- Large R and $gm_2 << gm_1 \Rightarrow$ low-offset and reduced kT/C noise and charge injection errors

$\Rightarrow$ Sampling capacitors can be smaller

Residual Offset of Auto-zeroing

Determined by

- Charge injection
- Leakage on C_{az}
- Finite amplifier gain

In practice

- Minimum size switches
- C_{az} as large as possible (sometimes external)
- Multi-stage amplifier topologies

Results in residual offsets of 1-10μV

Residual Noise of Auto-zeroing (1)

$V_{n,az}(f) = V_n(f)*(1 - H(f))$

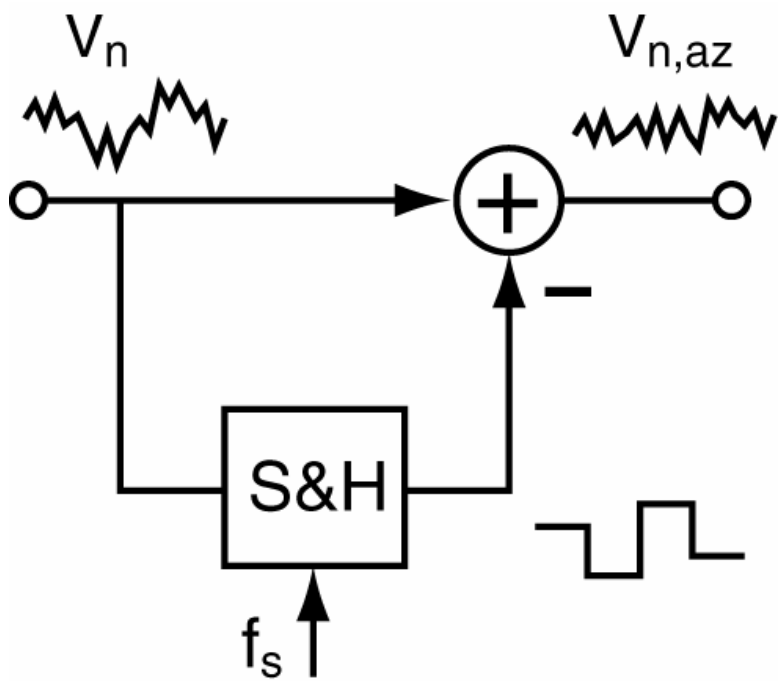
H(f) is the frequency response of the S&H

$H(f) = \text{sinc}(\pi f/f_s) \Rightarrow$ LPF

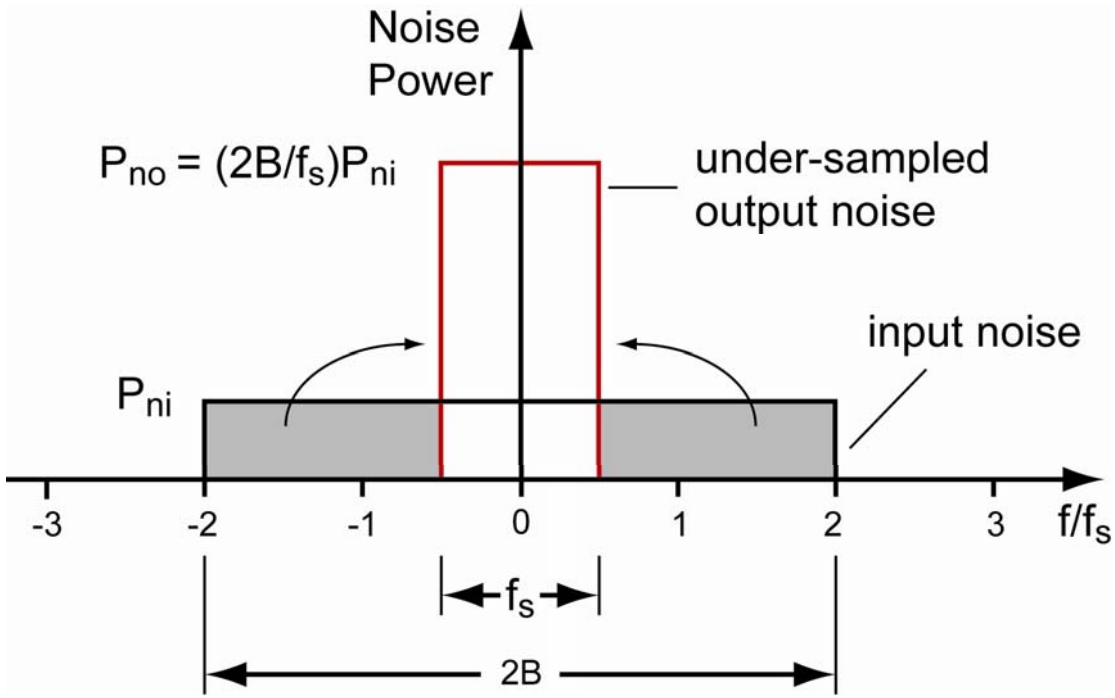
$\Rightarrow$ 1 - H(f) is a HPF

$\Rightarrow$ reduction of both offset and 1/*f* noise

$\Rightarrow$ but thermal noise will be (under) sampled

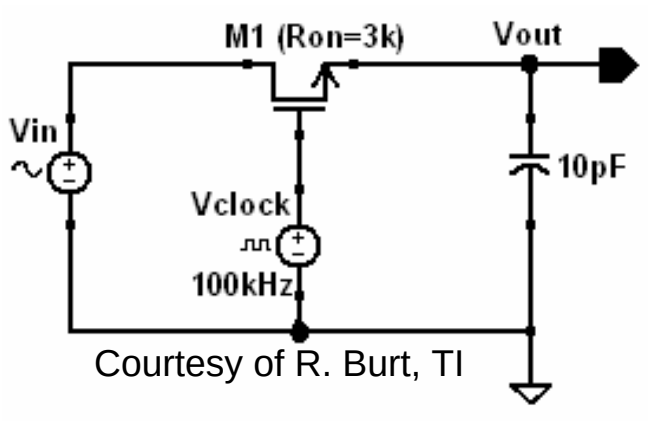


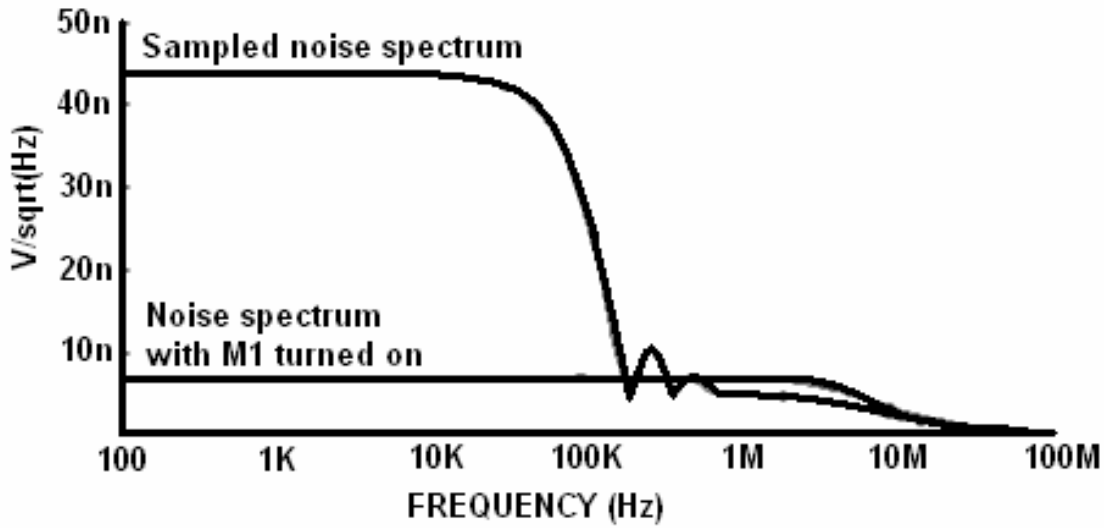
Residual Noise of Auto-zeroing (2)



- **Noise** bandwidth $B > f_s$ (due to settling considerations)
  $\Rightarrow$ input noise will be folded back (aliased) to DC
- The result is then LP filtered by the $\text{sinc}(\pi f/f_s)$ function

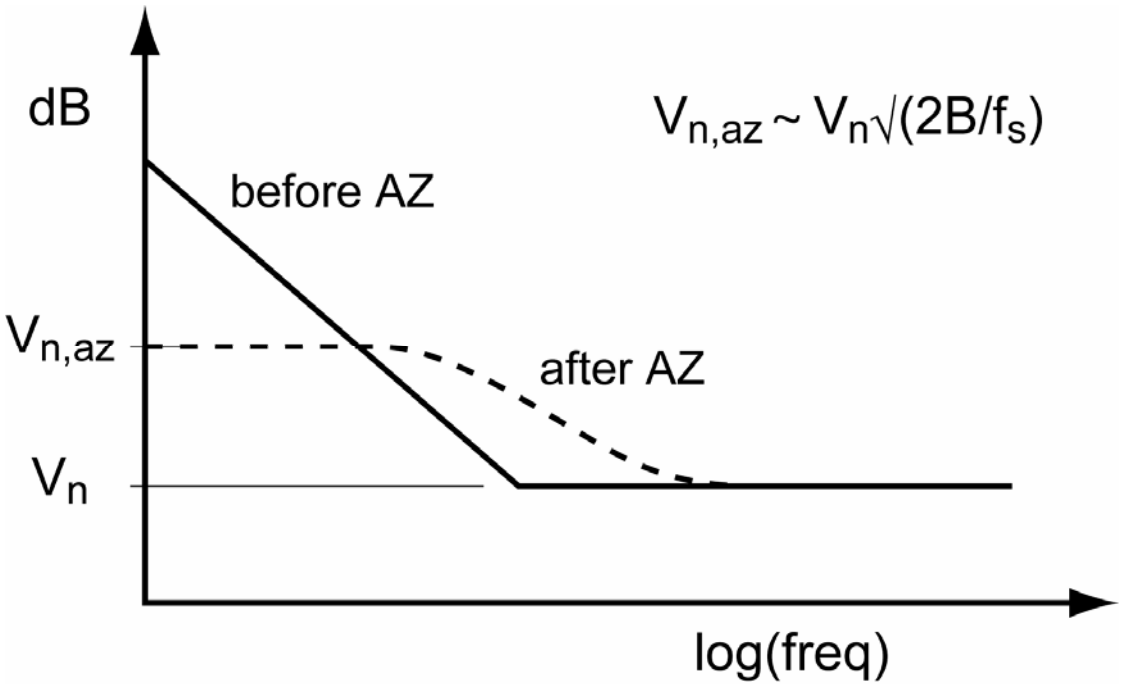
Residual Noise of Auto-zeroing (3)





- S&H with 100kHz clock & 50% duty-cycle
- Noise aliasing $\Rightarrow$ factor of 6 increase in LF noise!
- Notches at multiples of **2**fclock due to 50% duty cycle[2]
- Sampled noise spectrum obtained with Spectre RF[9,10]

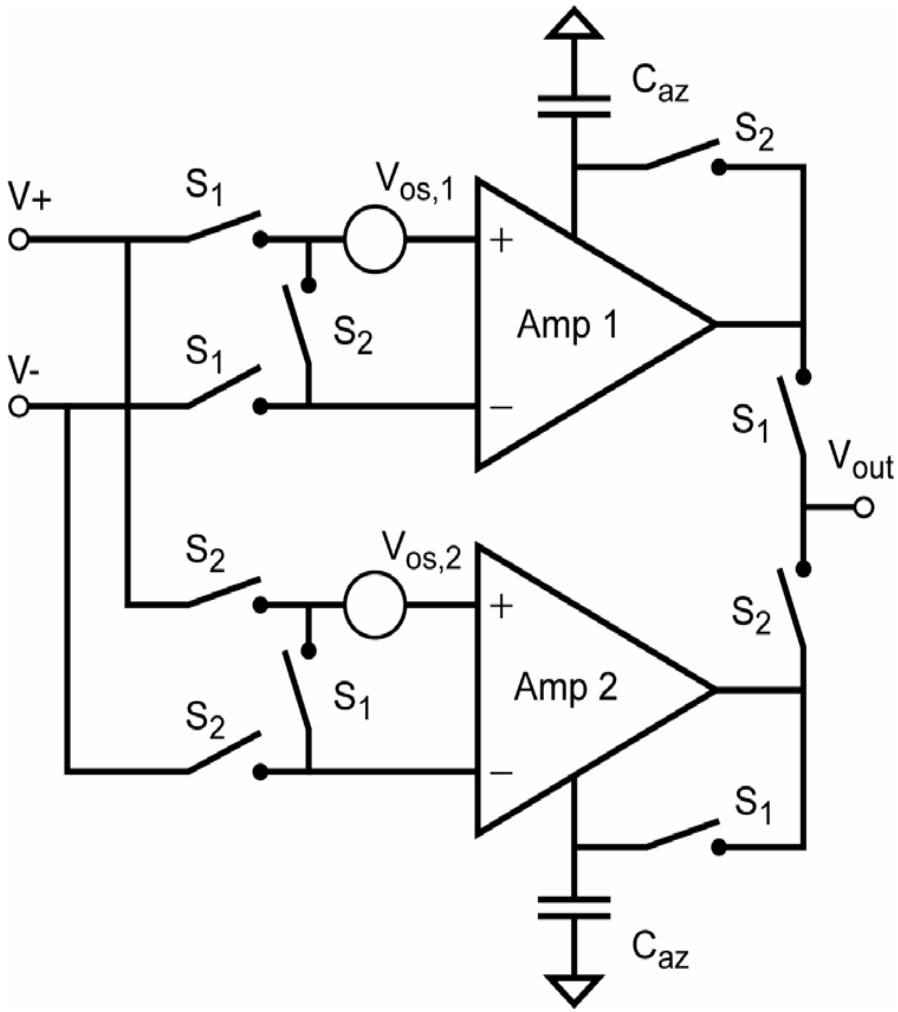
Residual Noise of Auto-zeroing (4)



- Detailed analysis[2] $\Rightarrow$ significant reduction of 1/*f* noise **IF** f_s >> 1/*f* corner frequency
- Noise aliasing $\Rightarrow$ LF power increased by the under-sampling factor (USF) = $2B/f_s$ $\Rightarrow$ factor 3 to 6 in volts

Ping-Pong Amplifier

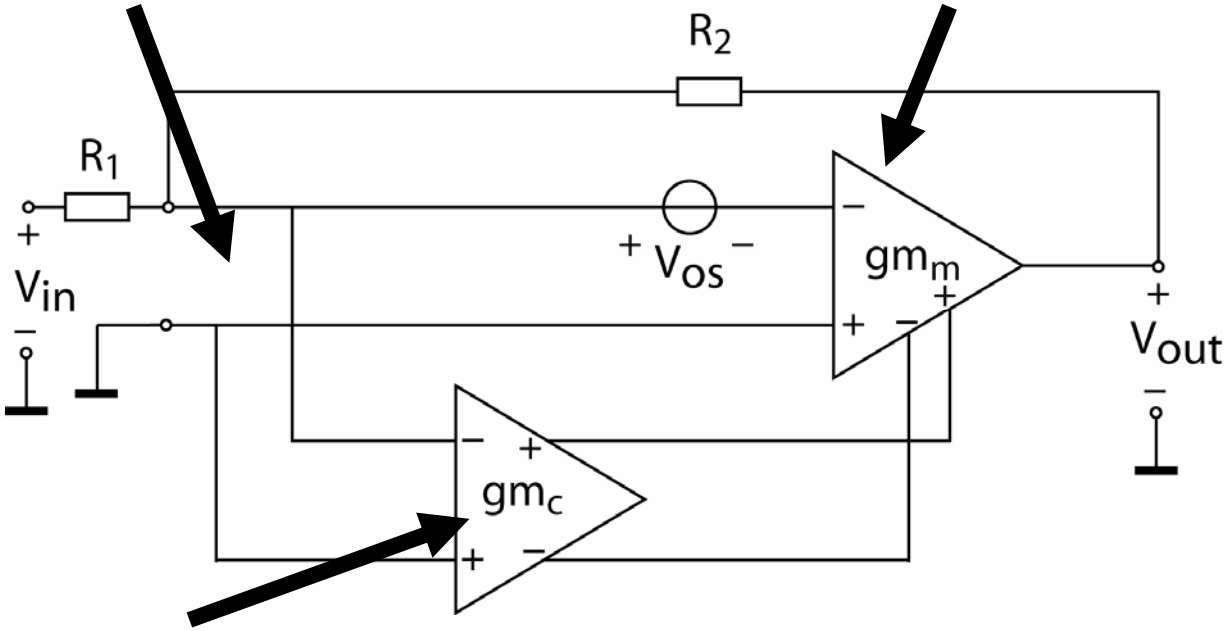
- Input signal “bounced” between two auto-zeroed amplifiers[11,12]
- Output V_{out} is then a quasi-continuous signal
- But switching spikes limit performance
- Randomized switching reduces spikes[13]



Offset Stabilization (OS)

Negative feedback
$\Rightarrow$ offset visible at input

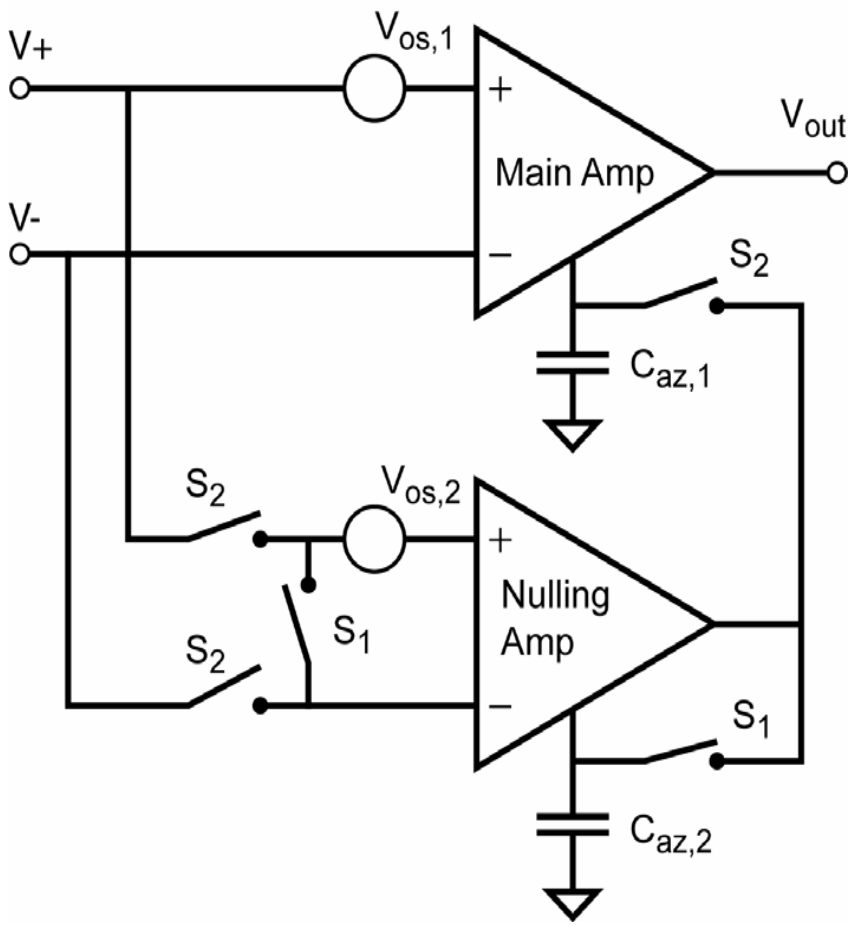
High bandwidth
main amplifier



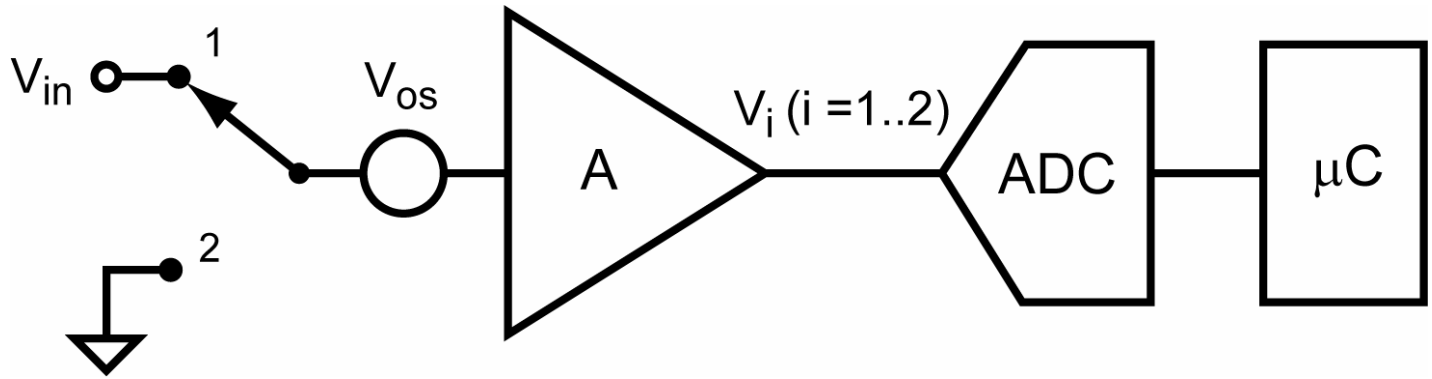
Low bandwidth, low offset compensating amplifier
$\Rightarrow$ Auto-zeroed or chopped

AZ Offset-Stabilized Amplifier

- Auto-zeroed nulling amp cancels the offset of main amplifier[14,15]
- Continuous output and less spikes
- But poor overload performance, i.e. when $V_+ - V_- > V_{os}$
- Amplifier cannot be used as a comparator



System-level Auto-zeroing

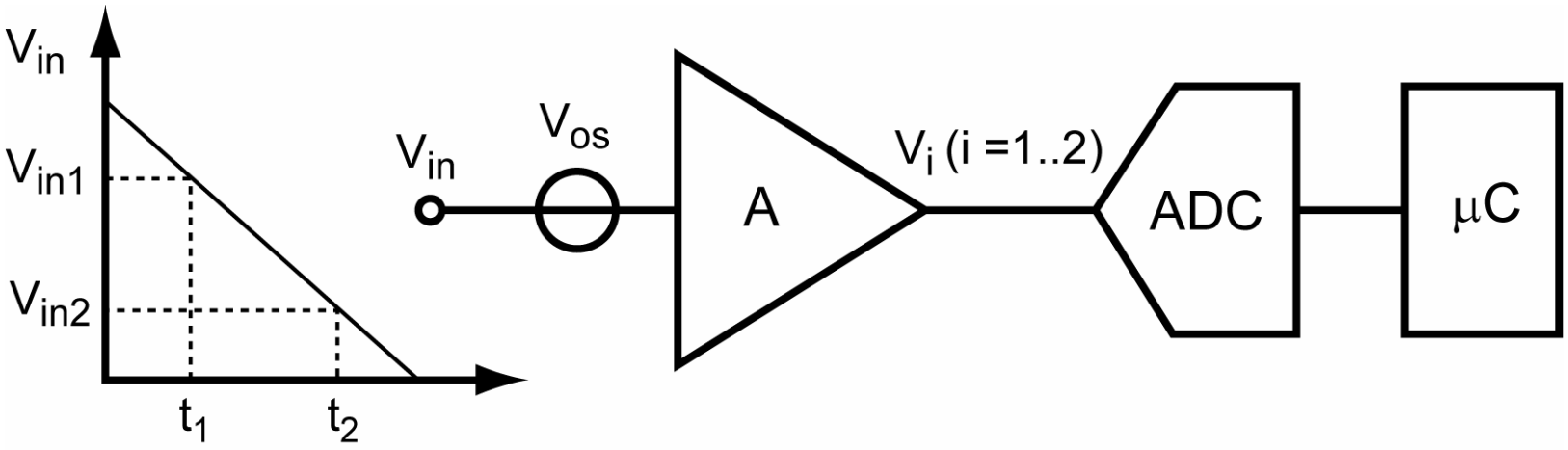


- Phase 1: $V_1 = A(V_{os} + V_{in})$
- Phase 2: $V_2 = AV_{os}$

$\Rightarrow (V_1 - V_2) = AV_{in}$

- Offset stored in the digital domain
- Widely used in instrumentation & measurement systems

Correlated Double Sampling (CDS)

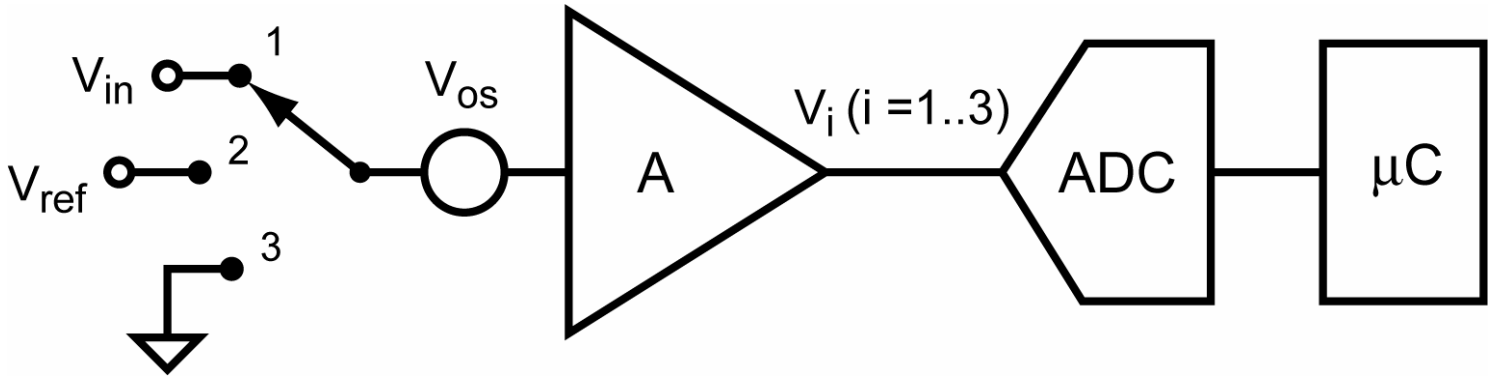


- Sometimes only a signal **difference** is required
  e.g. in image sensors
- Phase 1: $V_1 = A(V_{in1} + V_{os})$
- Phase 2: $V_2 = A(V_{in2} + V_{os})$

$\Rightarrow (V_1 - V_2) = A(V_{in1} – V_{in2})$

- To maximize suppression of 1/*f* noise, the interval $t_1 - t_2$, should be as short as possible

The 3 Signal Method



- Phase 1: $V_1 = A(V_{os} + V_{in})$
- Phase 2: $V_2 = A(V_{os} + V_{ref})$
- Phase 3: $V_3 = AV_{os}$

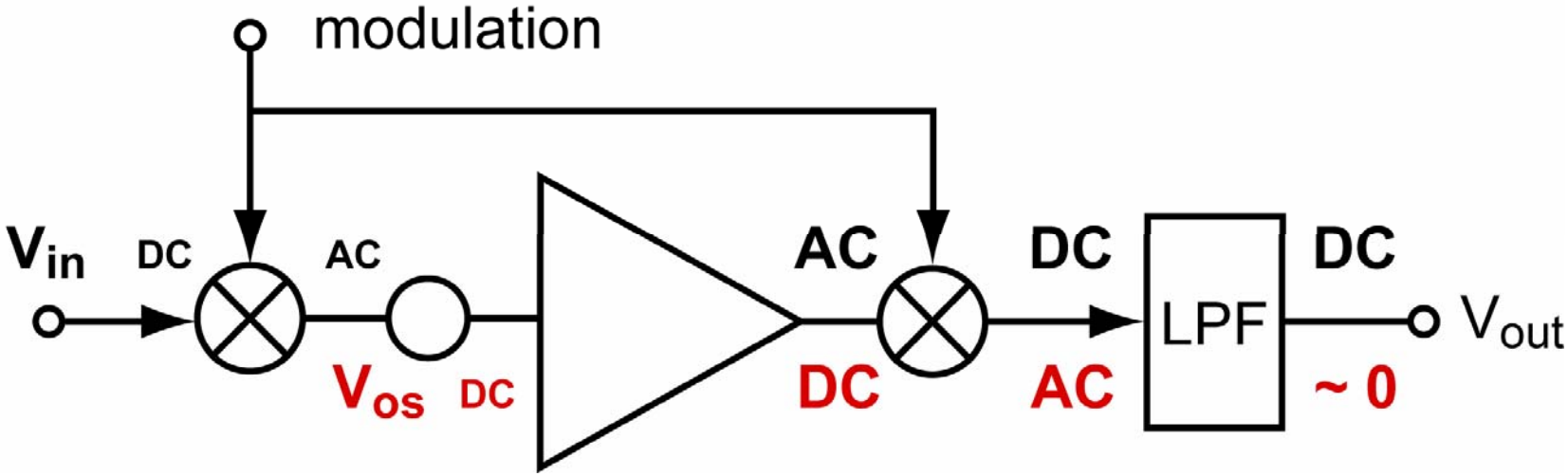
$\Rightarrow V_{in} = V_{ref}(V_1 - V_3)/(V_2 - V_3)$

Requires a known reference voltage
and a microprocessor to perform the division

Auto-Zeroing: Summary

- Offsets in the range of 1-10μV can be achieved
- No loss of bandwidth with appropriate amplifier topologies (ping-pong, offset-stabilization)
- Sampled data technique $\Rightarrow$ kT/C noise is an issue
- Noise aliasing will occur $\Rightarrow$ increased LF noise
- DOC technique of choice in sampled-data systems e.g. switched-capacitor filters, ADCs etc.

Chopping Principle

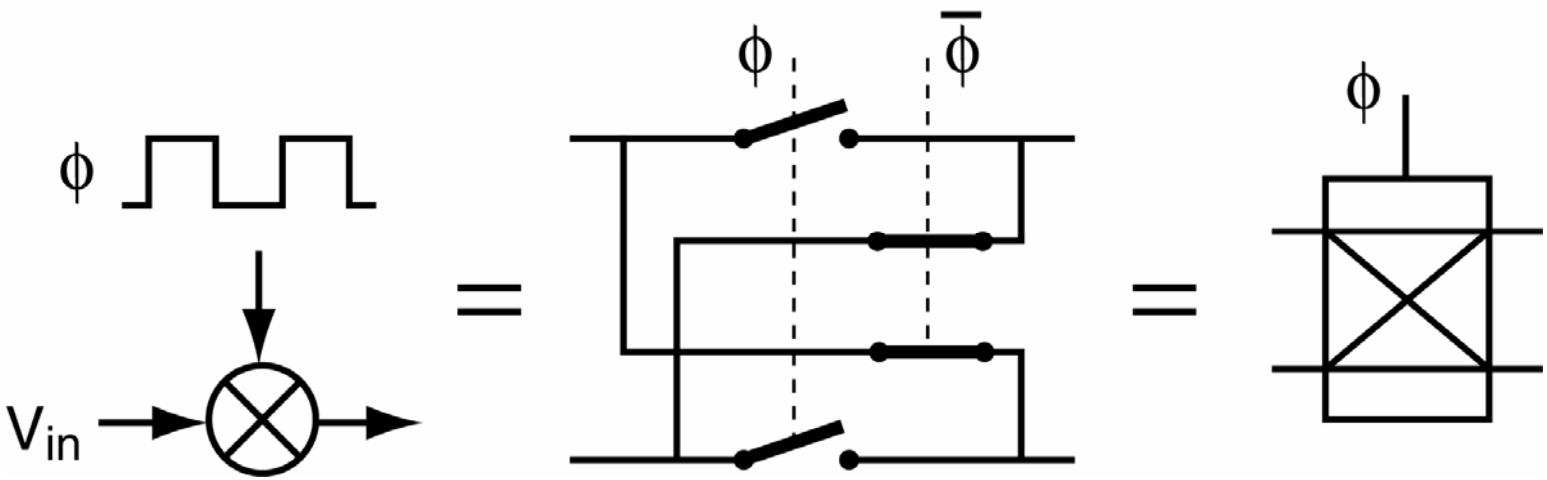


Signal is modulated, amplified and then demodulated[16]

+ Output signal is continuously available

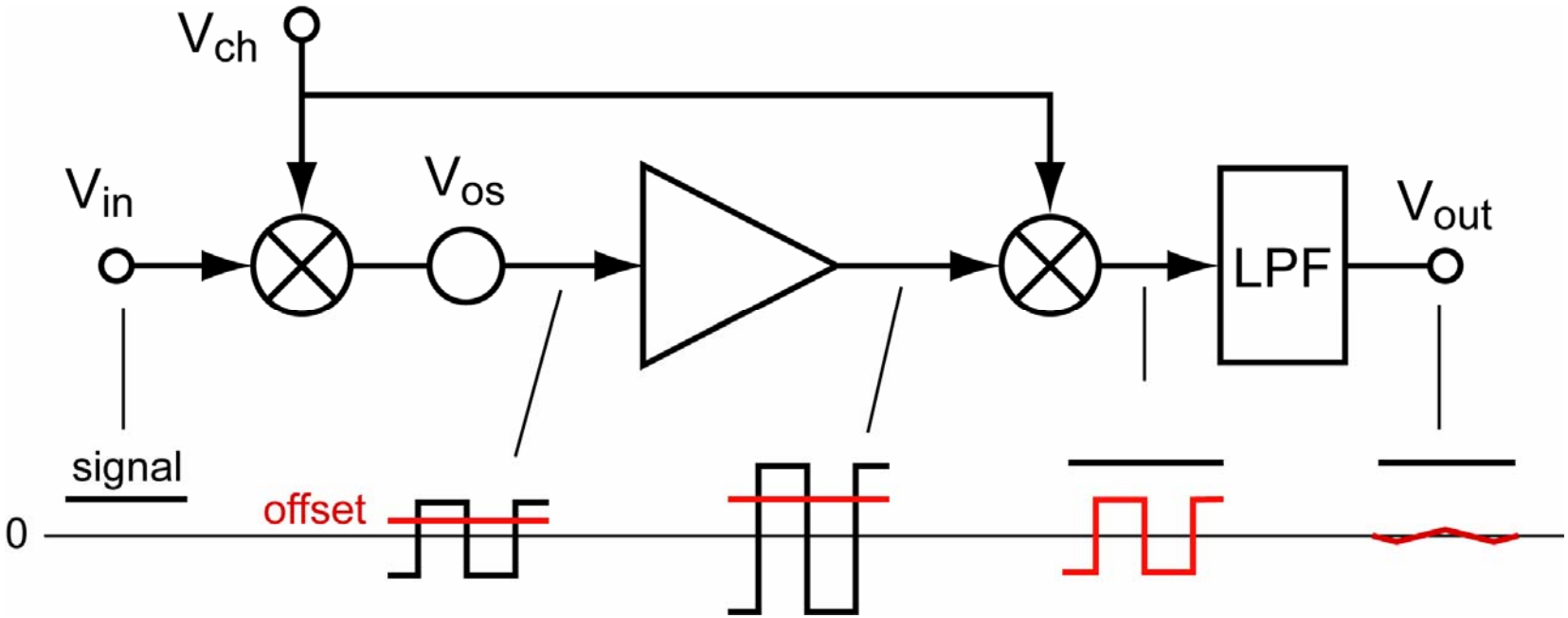
- Low-pass filter required

Square-wave Modulation



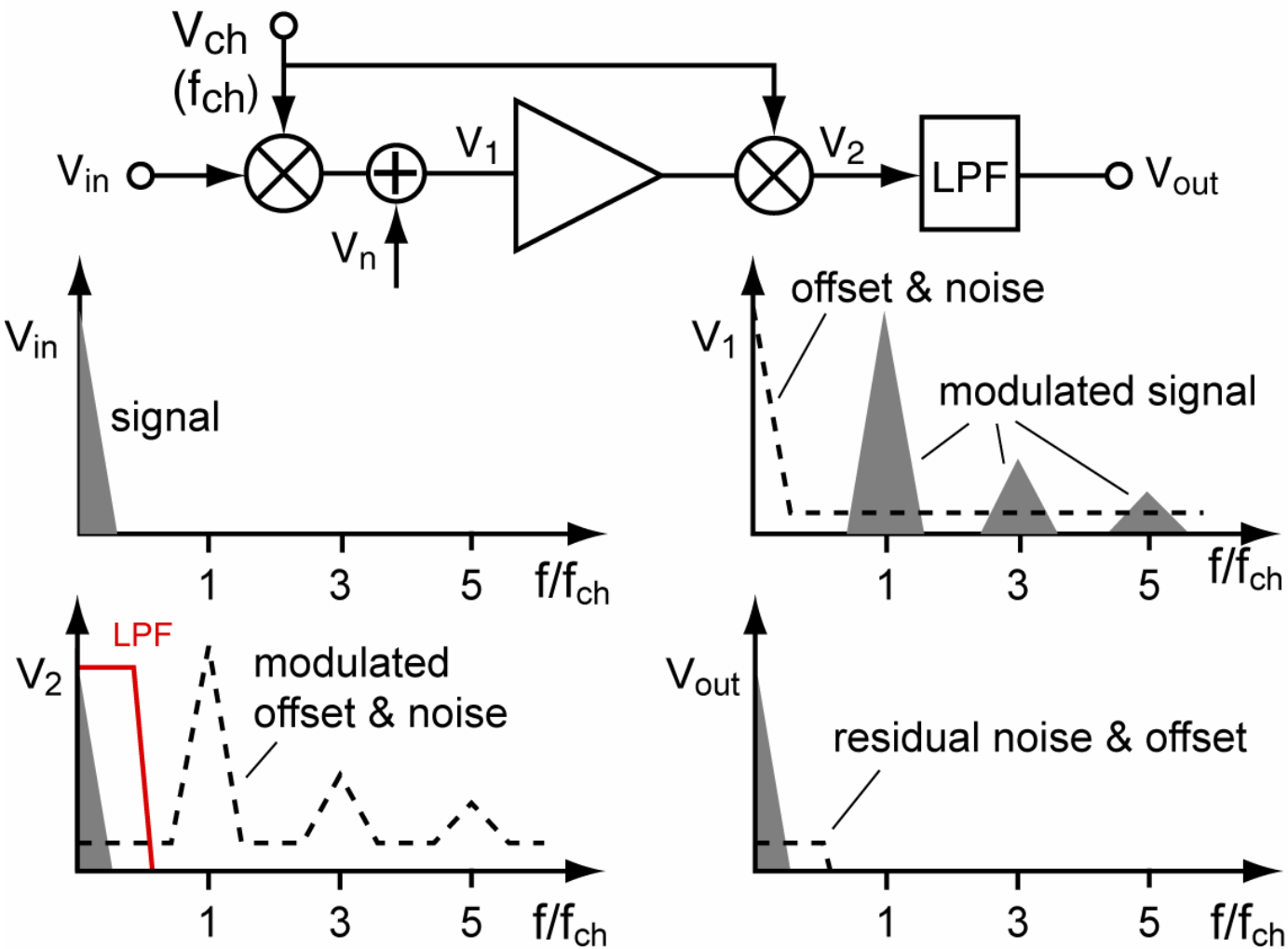
- Easily generated modulating signal
- Modulator is a simple polarity-reversing switch
- Switches are easily realized in CMOS

Chopping in the Time Domain

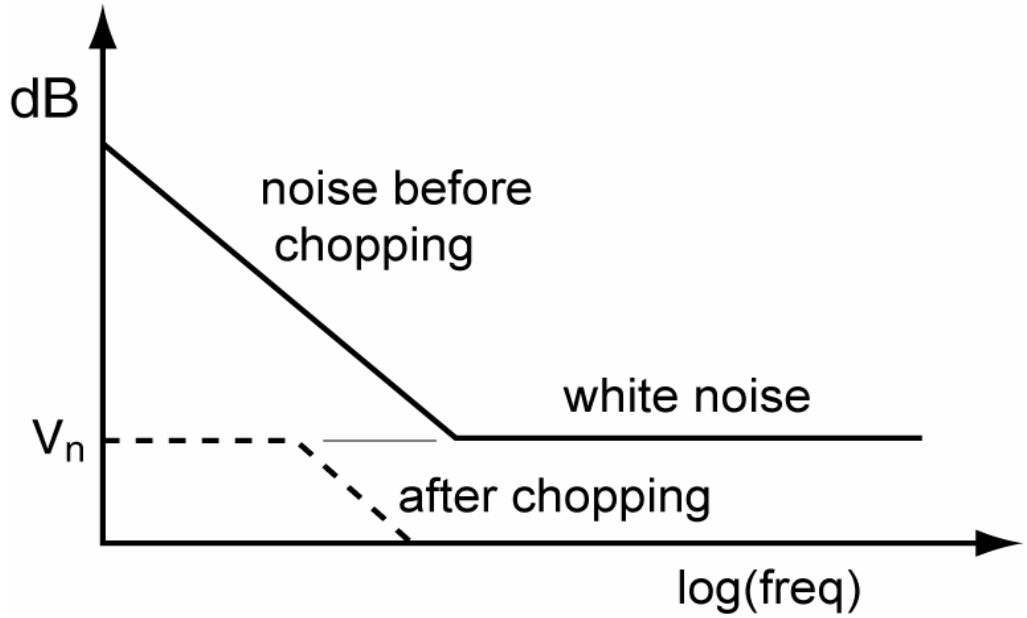


- V_{res} = 0 **IF** duty-cycle of V_{ch} is exactly 50% $\Rightarrow$ flip-flop
- If V_{os} = 10mV & f_{ch} = 50kHz, then 1ns skew $\Rightarrow$ V_{res} = 1µV

Chopping in the Frequency Domain

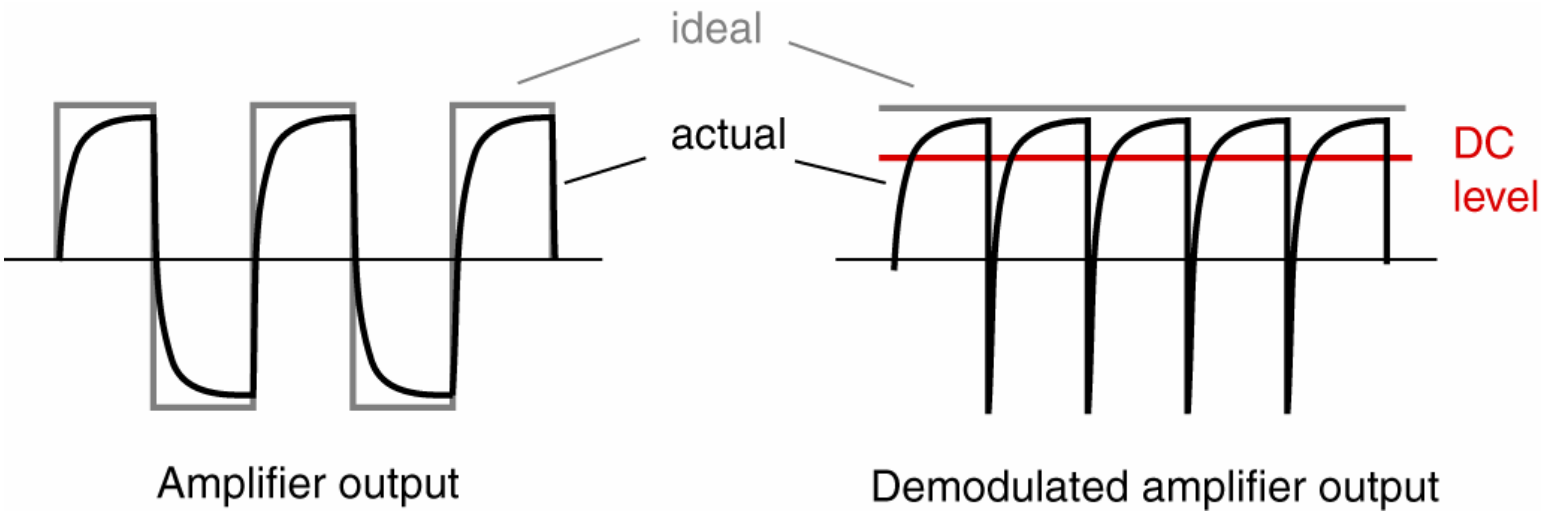


Residual Noise of Chopping



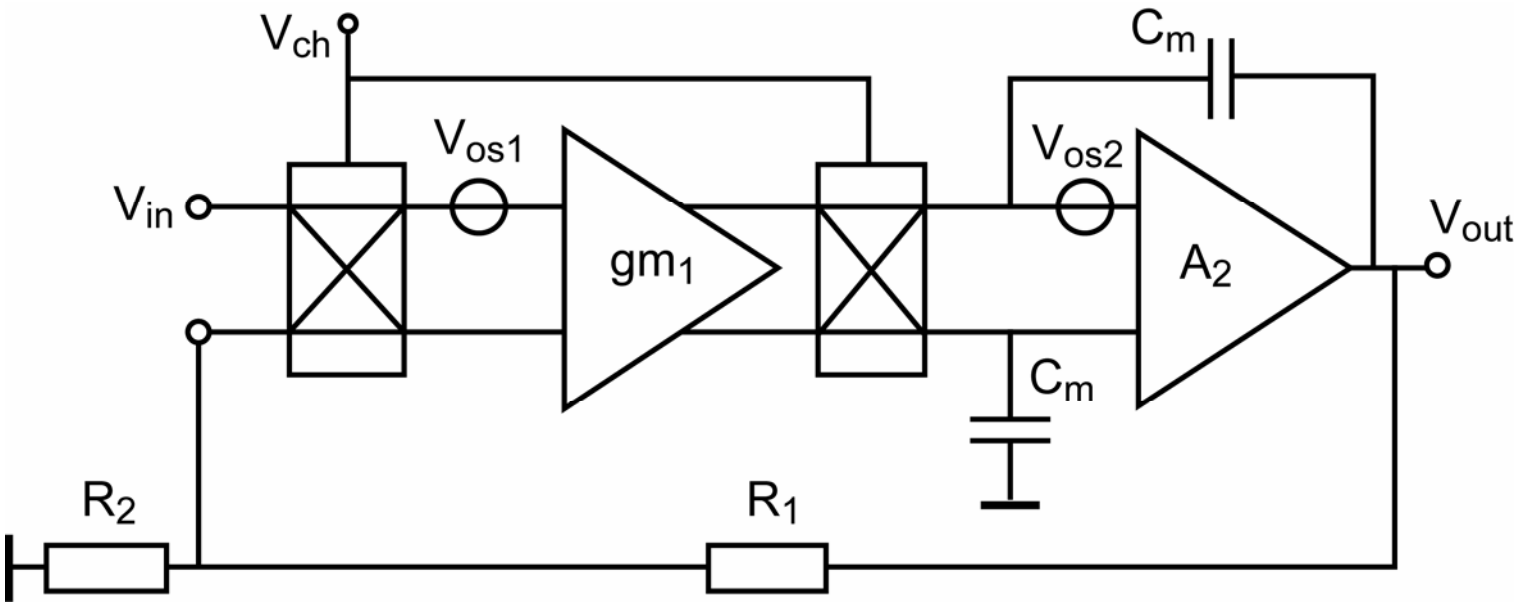
- 1/*f* noise is **completely** removed
  IF f_{ch} > 1/*f* corner frequency
- Significantly better than auto-zeroing!

Bandwidth & Gain Accuracy



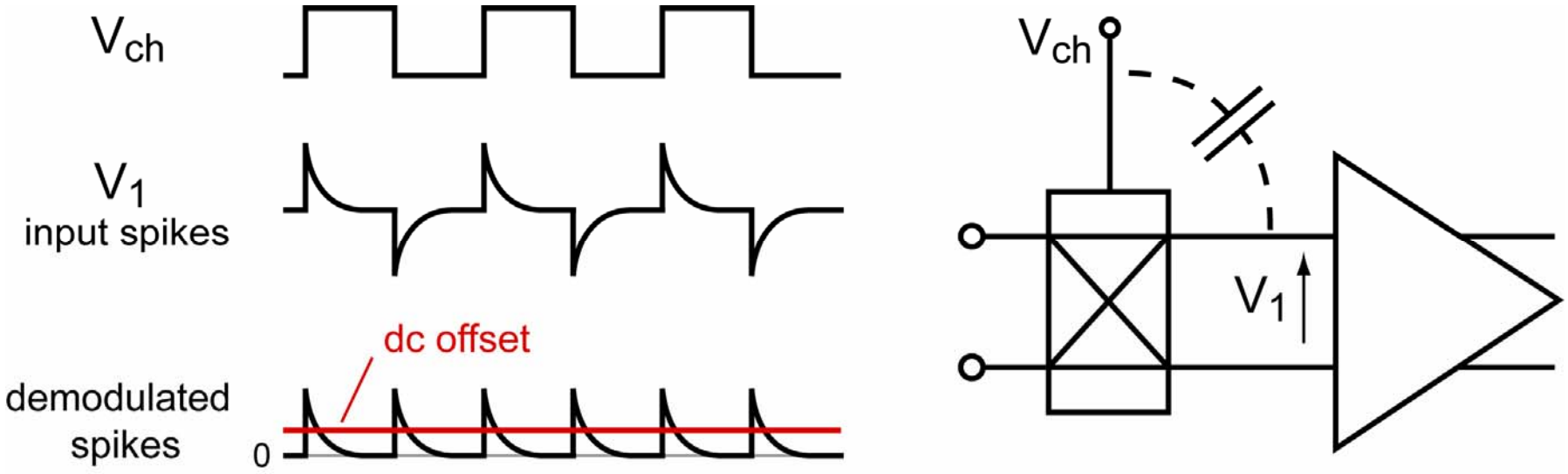
- Limited BW $\Rightarrow$ lower effective gain A_{eff}
  and chopping artifacts at even harmonics of f_{ch}
- $A_{eff} = A\,(1\text{-}4\tau/T_{ch})$ for a 1st order LP filter,
  where $BW = 1/2\pi\tau$ and $\tau << T_{ch}$
- $T_{ch}/\tau = 40 \Rightarrow BW = 6.4f_{ch} \Rightarrow$ 10% gain error!

Chopper Opamp with Feedback



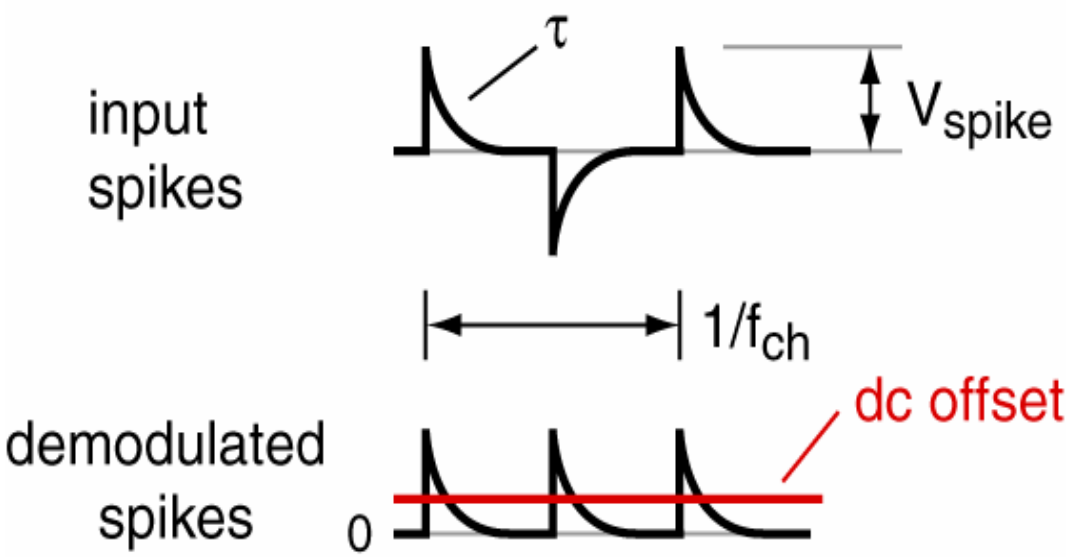
- Feedback resistors $\Rightarrow$ Accurate gain[17,18]
- To suppress V_{os2}, A_1 should have high gain
- Miller capacitors C_m also suppress ripple
- Minimum ripple $\Rightarrow$ high chopping frequencies

Residual Offset of Chopping (1)



- Due to mismatched charge injection and clock feed-through at the input chopper[19,20]
- Causes a typical offset of 1-10μV
- Input spikes ⇒ bias current (typically 50pA)

Residual Offset of Chopping (2)



- Residual offset^2 = $2f_{ch}\, V_{spike}\tau$
- Spike shape (τ) depends on source impedance e.g. feedback resistors around an opamp

Design Considerations

Input chopper

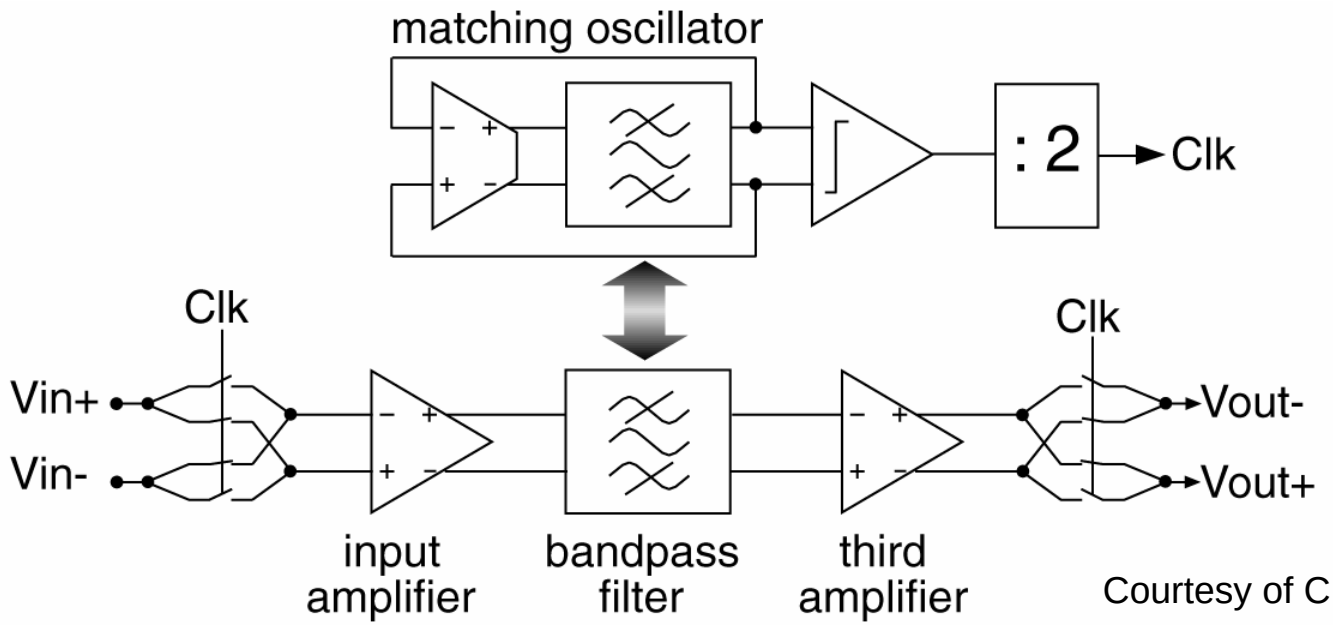
- Use minimum size switches
- Good layout $\Rightarrow$ symmetric, balanced clock coupling
- Ensure that switches “see” equal impedances
- Use a flip-flop to ensure an exact 50% duty-cycle

Chopping frequency f_{ch}

- Higher than 1/*f* noise corner frequency
- Not **too** high, as the residual offset increases with f_{ch}

Amplifier BW >> f_{ch} to minimize gain errors

Band-Pass Filtering

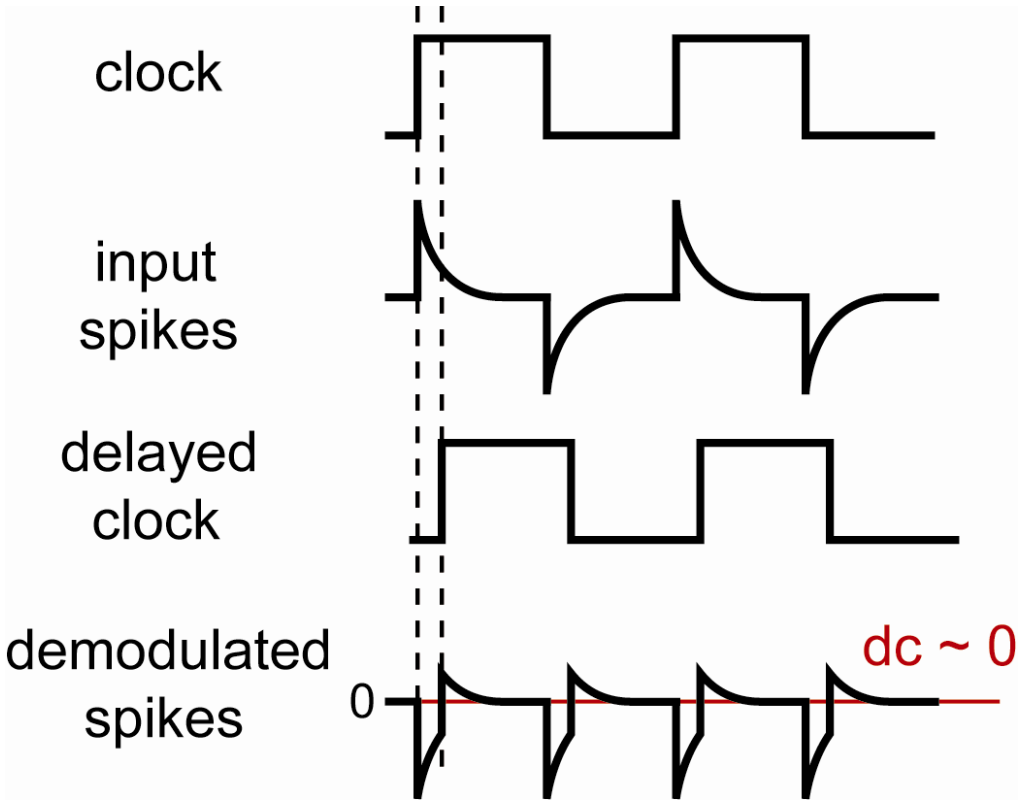


Courtesy of C. Hagleitner, IBM

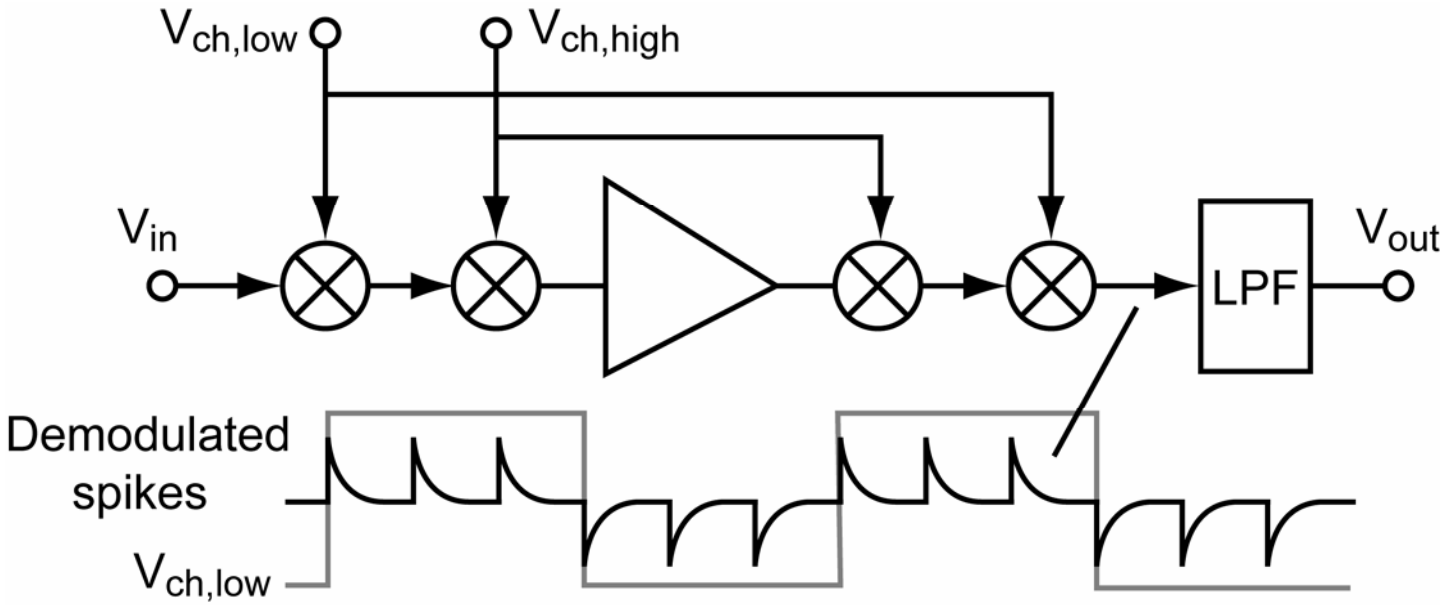
- Spike spectrum is “whiter” than that of modulated signal
  $\Rightarrow$ BP filter will reduce **relative** spike amplitude[19,21,22]
- Clock frequency tracks BP filter's center frequency
  $\Rightarrow$ low Q filter, Q ~ 5
- Residual offset ~ 0.5μV!

Delayed Demodulation

- Optimal delay ~ $0.7\tau_{spike}$
- Tricky timing!
- Solution: clock and spikes delayed by identical amplifiers[23]
- Residual offset ~ 1μV

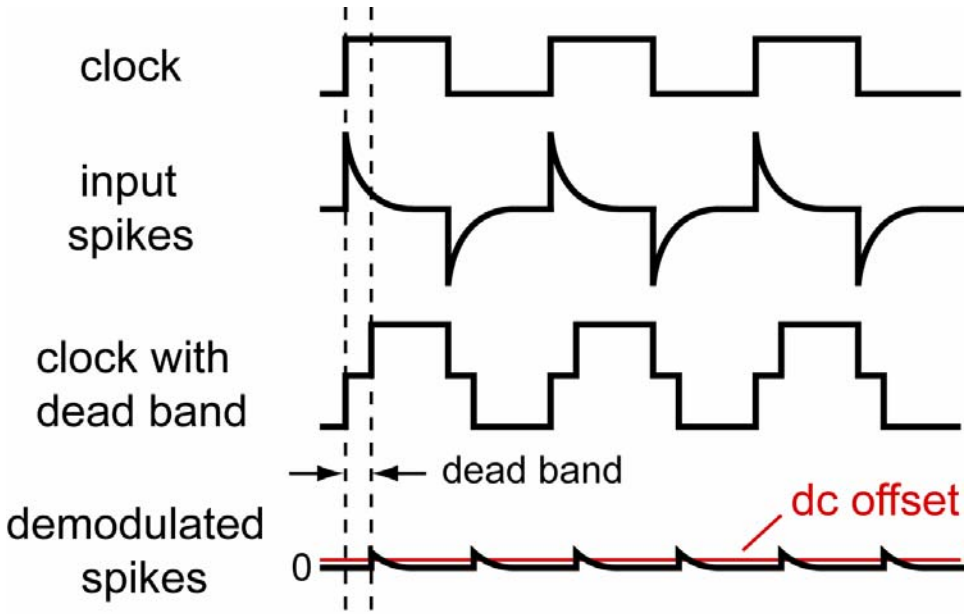


Nested Chopping



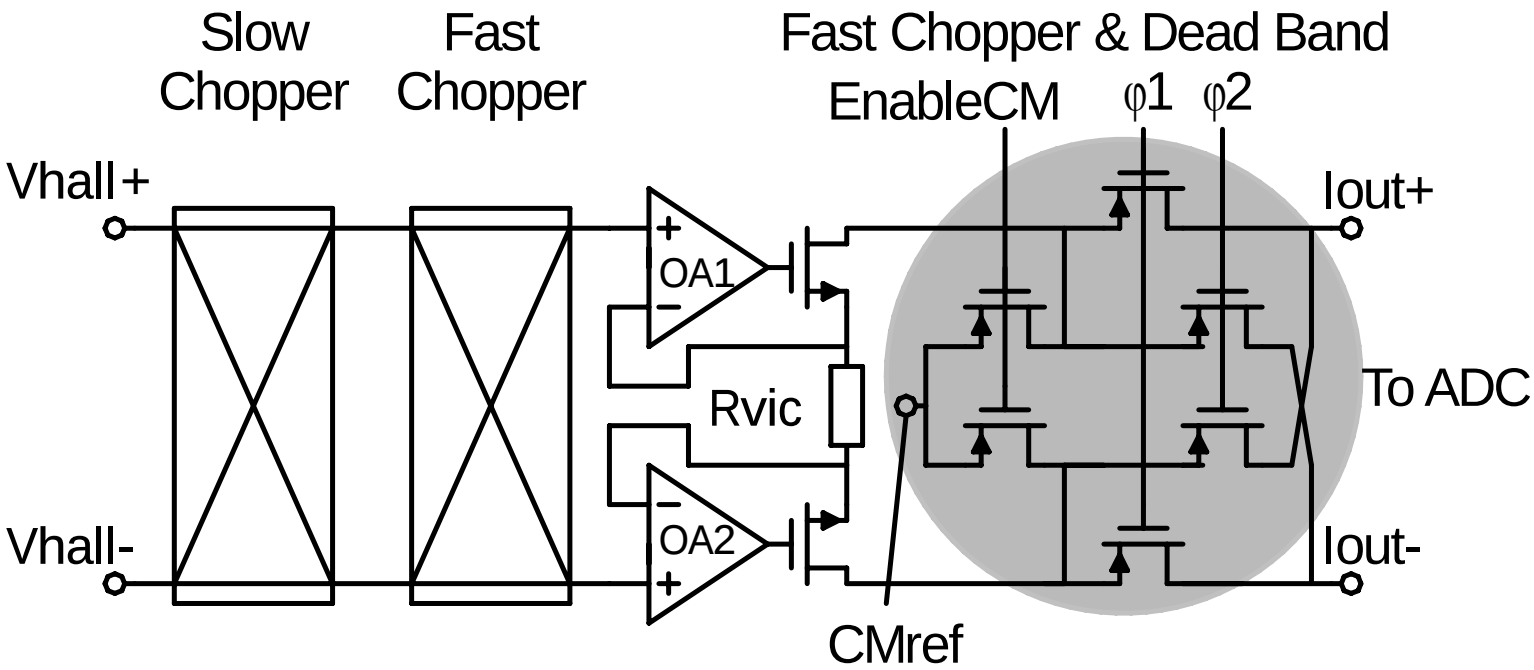
- Inner HF chopper removes 1/*f* noise
- Outer LF chopper removes residual offset[24,25]
- Residual offset ~ 100nV, but reduced bandwidth
- Note: input choppers should not be merged!

Dead-Banding



- During dead-band amplifiers output is tri-stated[26,27,28]
- Residual offset ~ 200nV!
- BUT loss of gain and aliasing due to S&H action
  $\Rightarrow$ slightly worse noise performance

Precision V-I Converter



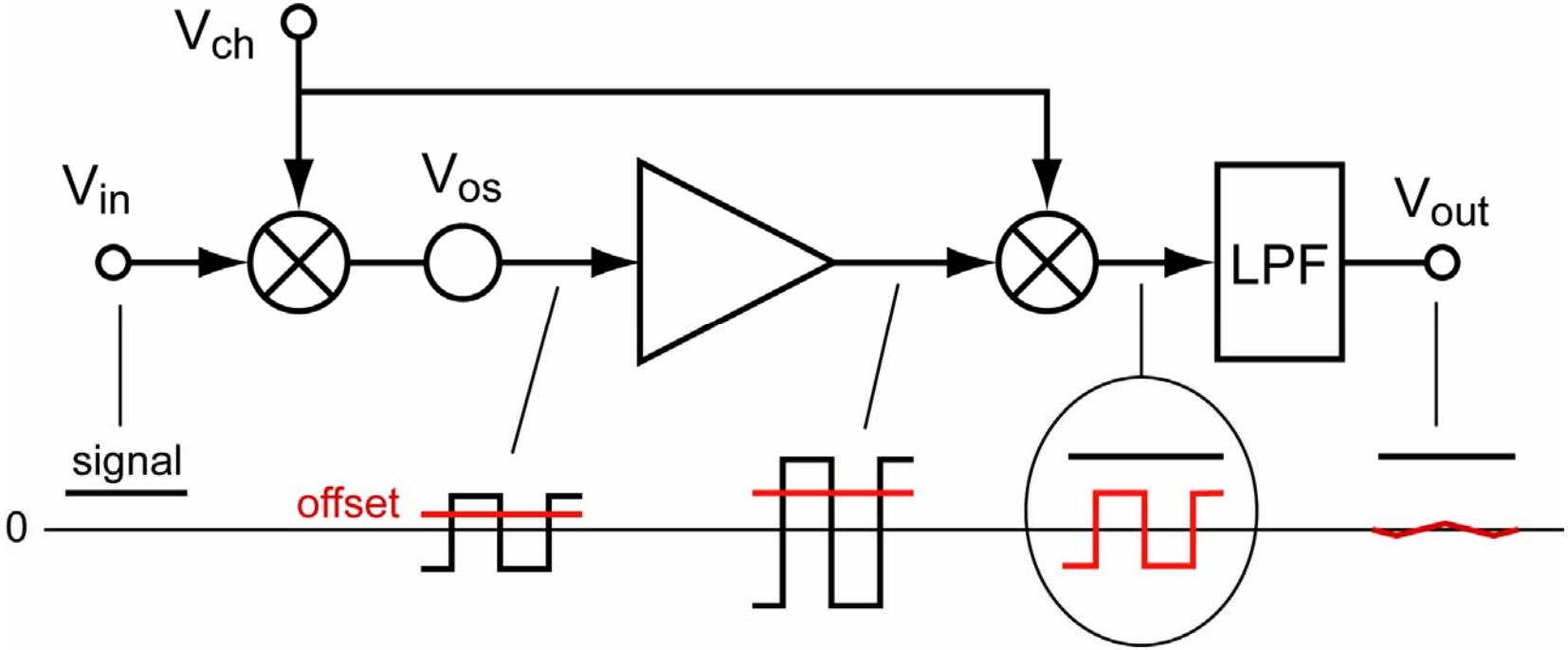
- Front-end of a magnetic field sensor[29] with < 50nV offset!
- Fast output chopper implements dead-bands
- During dead-bands, output current flows into a CM node
- Slow output chopper implemented in ADC

Dealing with Spikes: Overview

- BP Filtering: ~ 0.5μV offset, complex clock timing
- Delayed demodulation: ~ 1 μV offset, complex clock timing
- Dead-banding: ~ 200nV offset, wide BW
- Nested chopping: ~ 100nV offset, but limited BW

Last two techniques represent best compromise between offset magnitude and circuit complexity

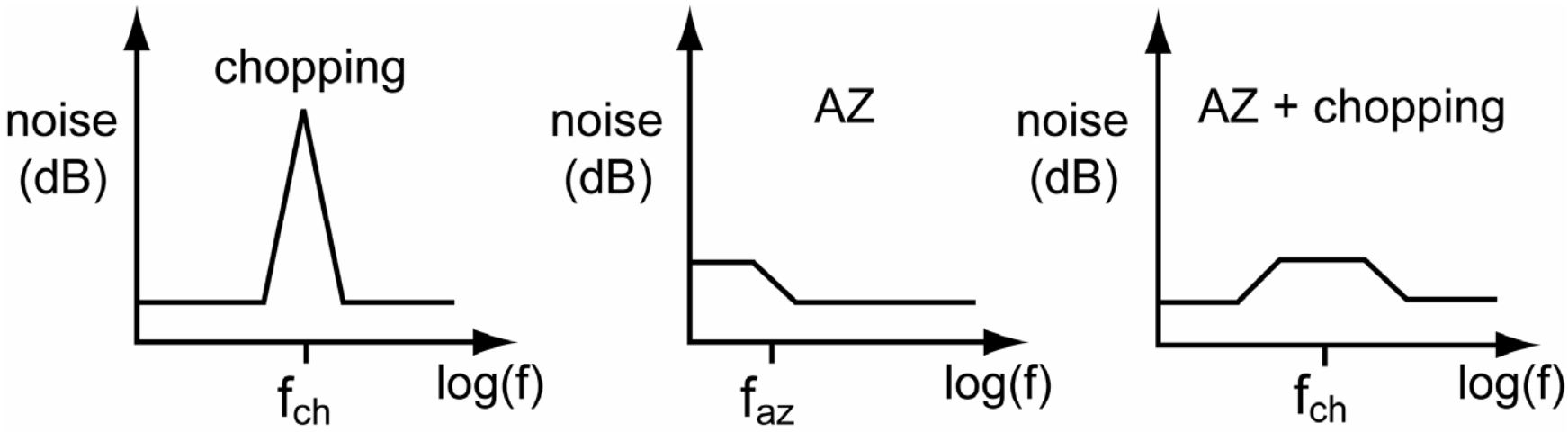
Chopping Artifacts



Modulated offset $\Rightarrow$ chopping artifacts

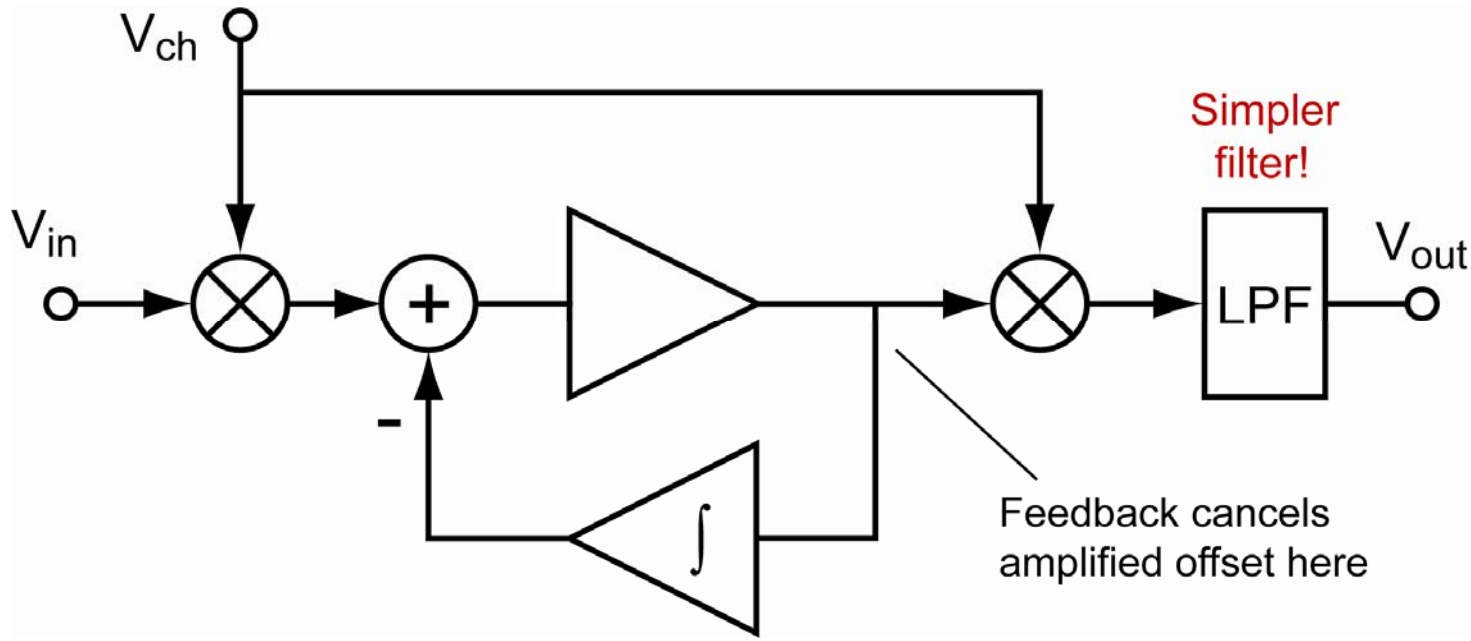
- Can be removed by a low-pass filter
- BUT analog filters with low cut-off frequencies are difficult to realize on chip

Auto-zeroing and Chopping



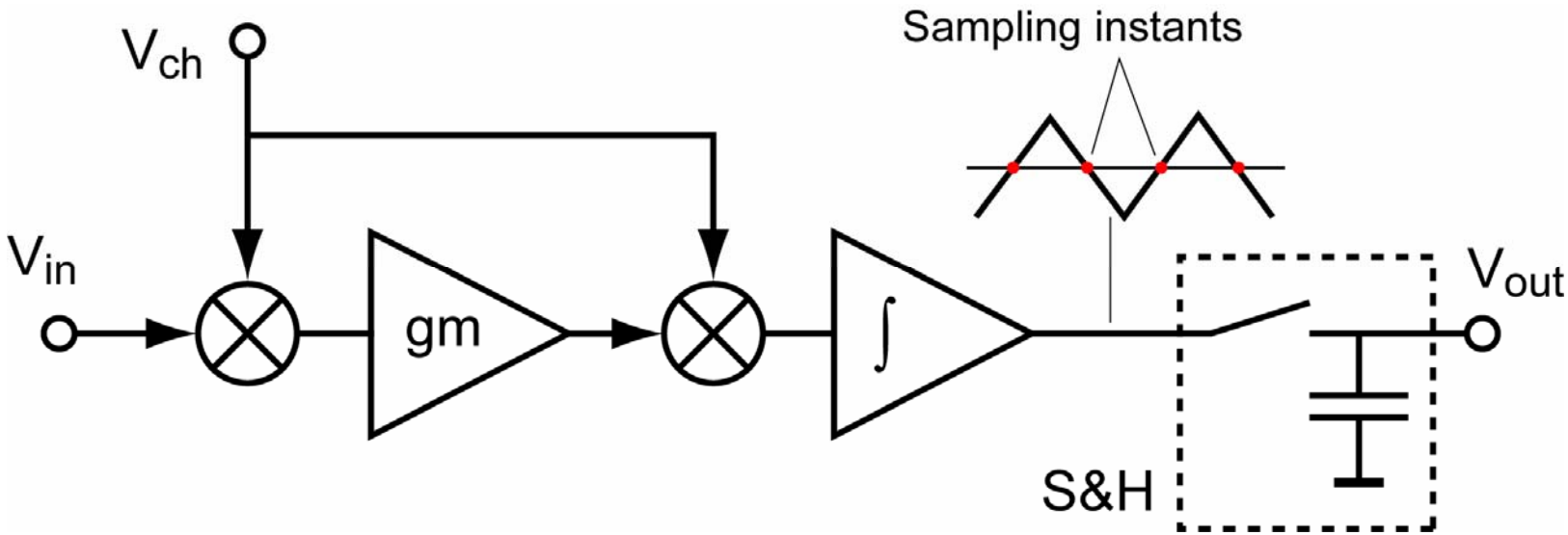
- Significantly improves LF noise performance[30,31,42]
- Much less artifacts than with chopping alone
- 3 μV offset & 20nV/√Hz demonstrated in a ping-pong amplifier[30]
- Choosing $f_{ch} = 2f_{az} \Rightarrow$ aliased noise has notch at DC

AC Coupling



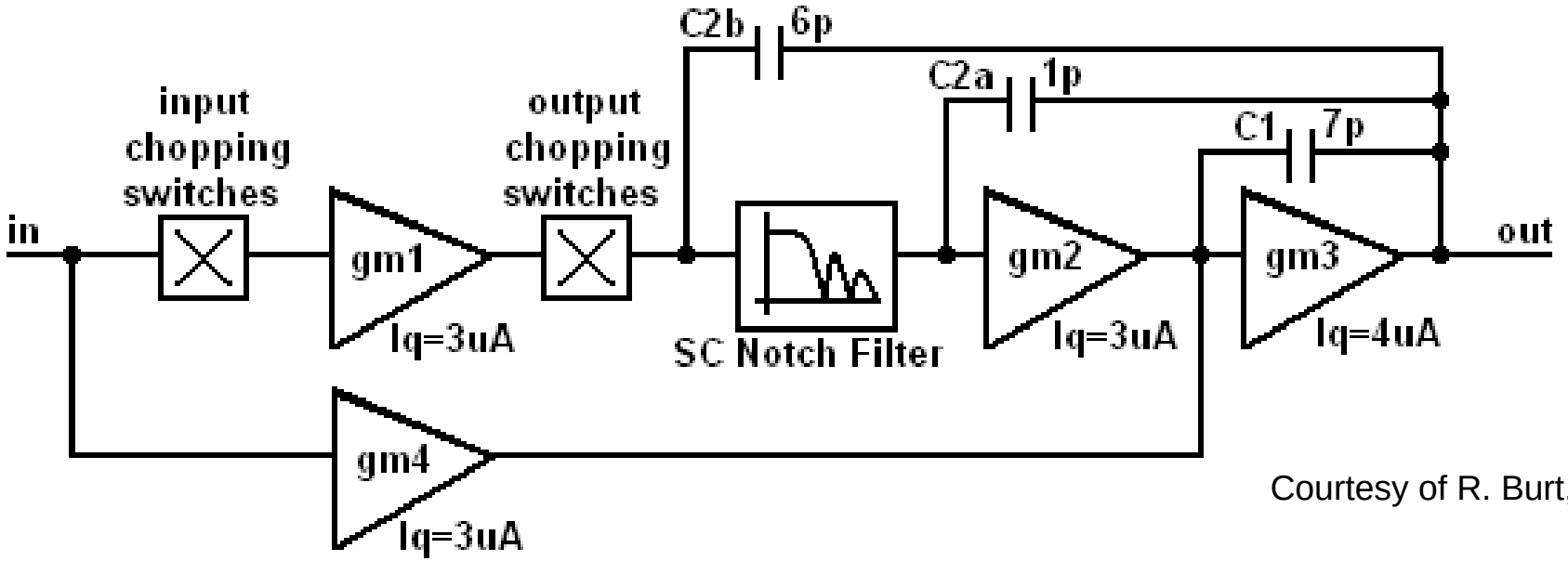
- AC coupling will block the amplifier's offset
- Alternatively, DC "servo" loop (shown) *inside* the choppers will also suppress the amplifier's offset[32,33]
- Note: DC servo loop *outside* the choppers results in a low-noise amplifier with a HPF characteristic[33,34]

Switched Capacitor Filter (1)



- Chopped offset is integrated & the triangular ripple is then sampled at the zero-crossings[35]
- SC filter essentially eliminates residual ripple
- Filter introduces delay and a (small) noise penalty

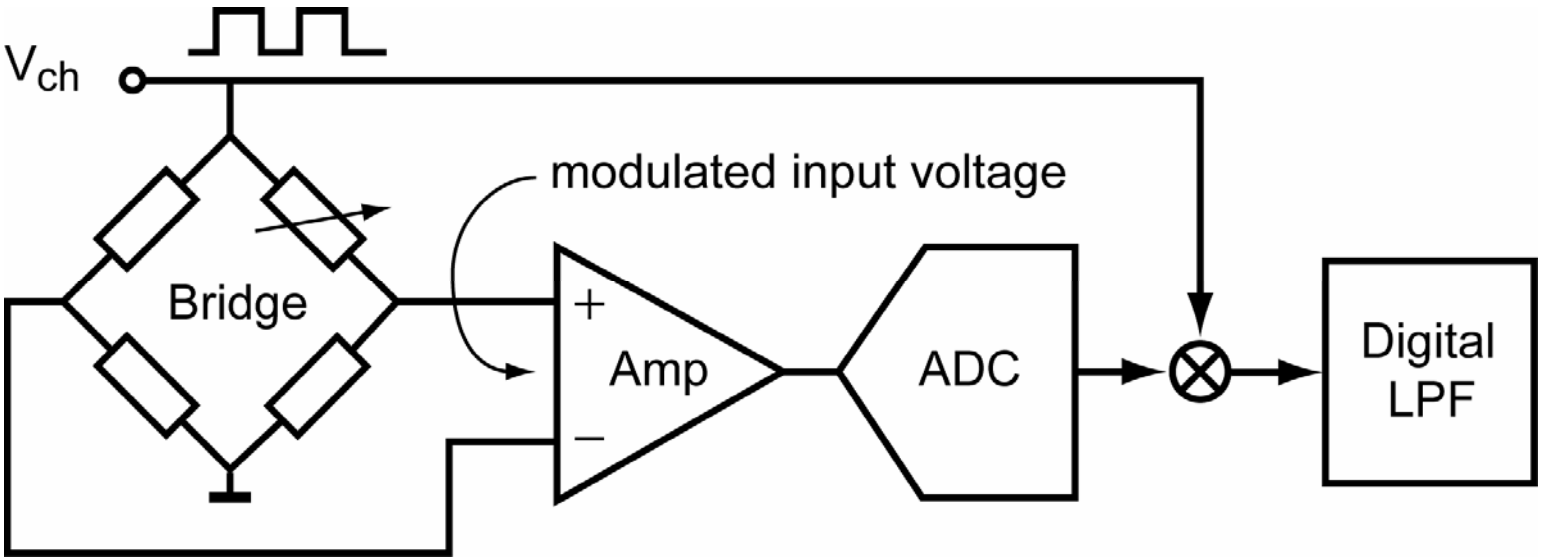
Switched Capacitor Filter (2)



Courtesy of R. Burt, TI

- SC filters have been used in **true** chopper-stabilized opamps[9,36]
- Note: gm4 is not chopped $\Rightarrow V_{res} > V_{os4}A_{gm4}/(A_{gm1}A_{gm2})$
- Filter delay incorporated into a multi-path nested Miller compensation scheme

Digital Filtering



- Chopped signal is digitized
- Demodulation is done digitally[25,37]
- Chopper artifacts are removed by a digital LPF
  e.g. a sinc filter with notches at f_{ch}

Dealing with Artifacts: Overview

Reduce the amplifier's initial offset

- Auto-zeroing and chopping: increased noise
- DC servo: still requires some analog filtering
- Switched capacitor filtering

Digital Filtering

- Very low cut-off frequencies can be realized
- Decimation filter of a $\Sigma\Delta$ ADC can be used to remove chopper artifacts $\Rightarrow$ no extra overhead

Chopping: Summary

- Offsets in the range of 50nV-10μV can be achieved
- Fundamental loss of bandwidth (unless offset-stabilized topologies can be used)
- Eliminates 1/*f* noise, noise floor set by thermal noise
- DOC technique of choice when noise or offset performance is paramount e.g. in biomedical amplifiers, low-power opamps, smart sensors etc.

State-of-the-Art Opamps

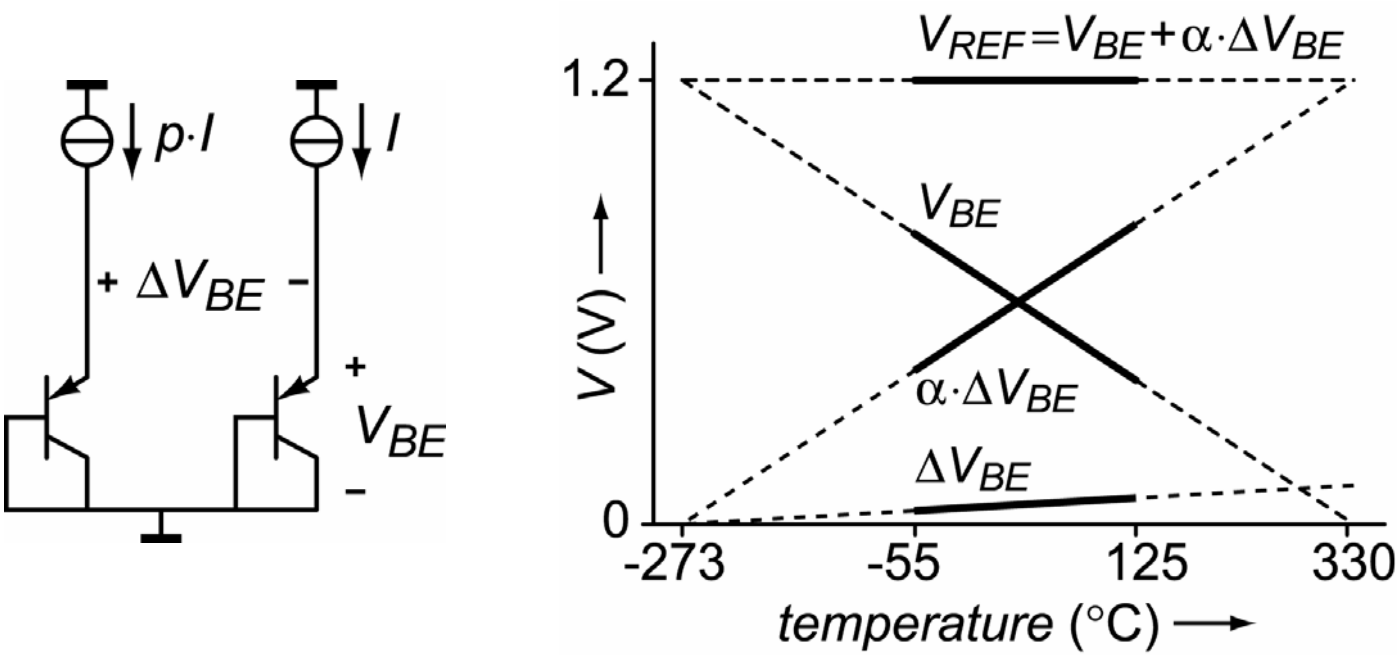
Type	Offset (max)	Noise (0 - 10Hz)	DOC Freq. (kHz)	Isy (max, µA)	Typ. GBW (MHz)	Technique
LTC2050	3µV	1.5µV	7.5	1200	3.0	AZ-OS
AD8571[13]	10µV	1.0µV	2 – 4	1075	1.0	Randomized AZ-PP
AD8628[30]	10µV	0.6µV	7.5/15	1000	2.5	CH & AZ-PP
MAX4238[39]	3.5µV	1.5µV	10 – 15	850	1.0	Randomized CH-OS
OPA333[9]	10µV	1.1µV	100	28	0.35	CH-OS
CS3001[38]	10µV	0.125µV	200	2800	5.0*	CH-OS

*Conditionally stable

Design of a CMOS Temp. Sensor[40,41]

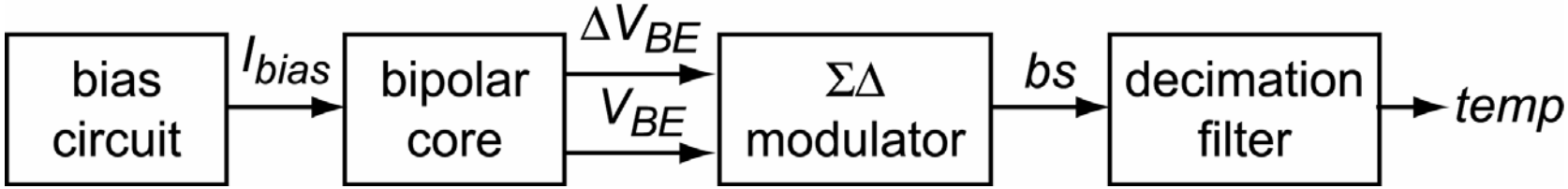
- Why CMOS ‘smart’ temperature sensors?
  + digital interface
  + low cost
- But accuracy is a problem!
  Only ±2.0°C from –55°C to 125°C
- By comparison: class-A Pt100
  achieves ±0.5°C in the same temp. range
- Goal: ±0.1°C from –55°C to 125°C
  with single temperature calibration only

Operating Principle



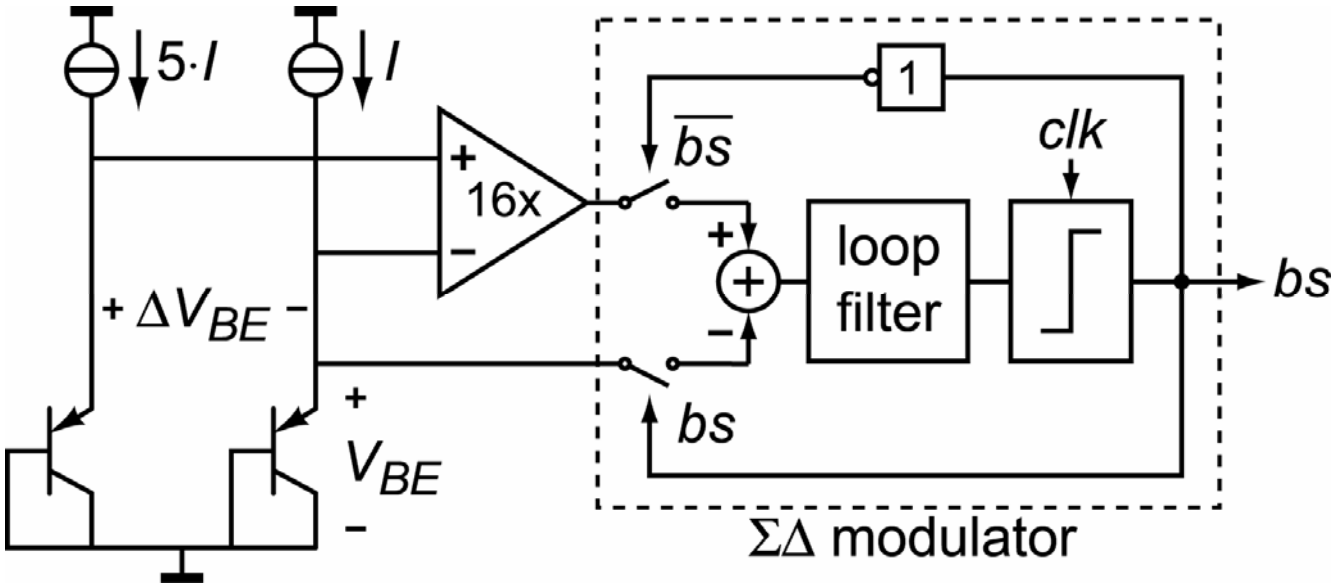
- Substrate PNPs generate:
  - ΔV_{BE} proportional to absolute temp. (PTAT)
  - V_{BE} complementary to absolute temp. (CTAT)
- Ratiometric measurement: $\mu = \frac{V_{TEMP}}{V_{REF}} = \frac{\alpha \cdot \Delta V_{BE}}{V_{BE} + \alpha \cdot \Delta V_{BE}}$

Block Diagram



- ΣΔ modulator produces bitstream *bs* whose average is representation of temperature
- Offset in ΔV_{BE} read-out results in errors of ~10°C/mV
  $\Rightarrow$ offset << 10μV required for error << 0.1°C
- Spread of V_{BE} and bias-current ratio are mitigated by trimming and DEM respectively[40,41]
- Bitstream is filtered and scaled by decimation filter to produce binary reading in °C

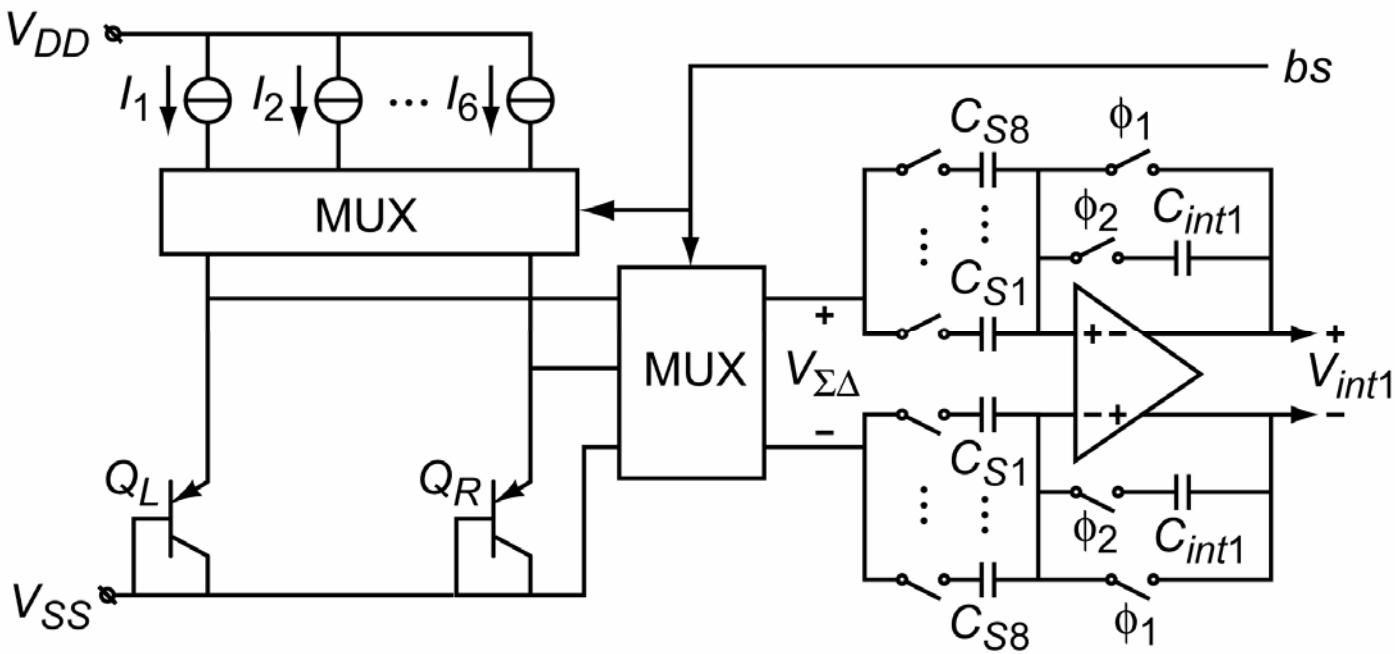
Charge Balancing in ΣΔ



- Every clock cycle, either $16 \cdot \Delta V_{BE}$ (bs=0) or $-V_{BE}$ (bs=1) is input to the loopfilter
- Resulting bitstream average μ:

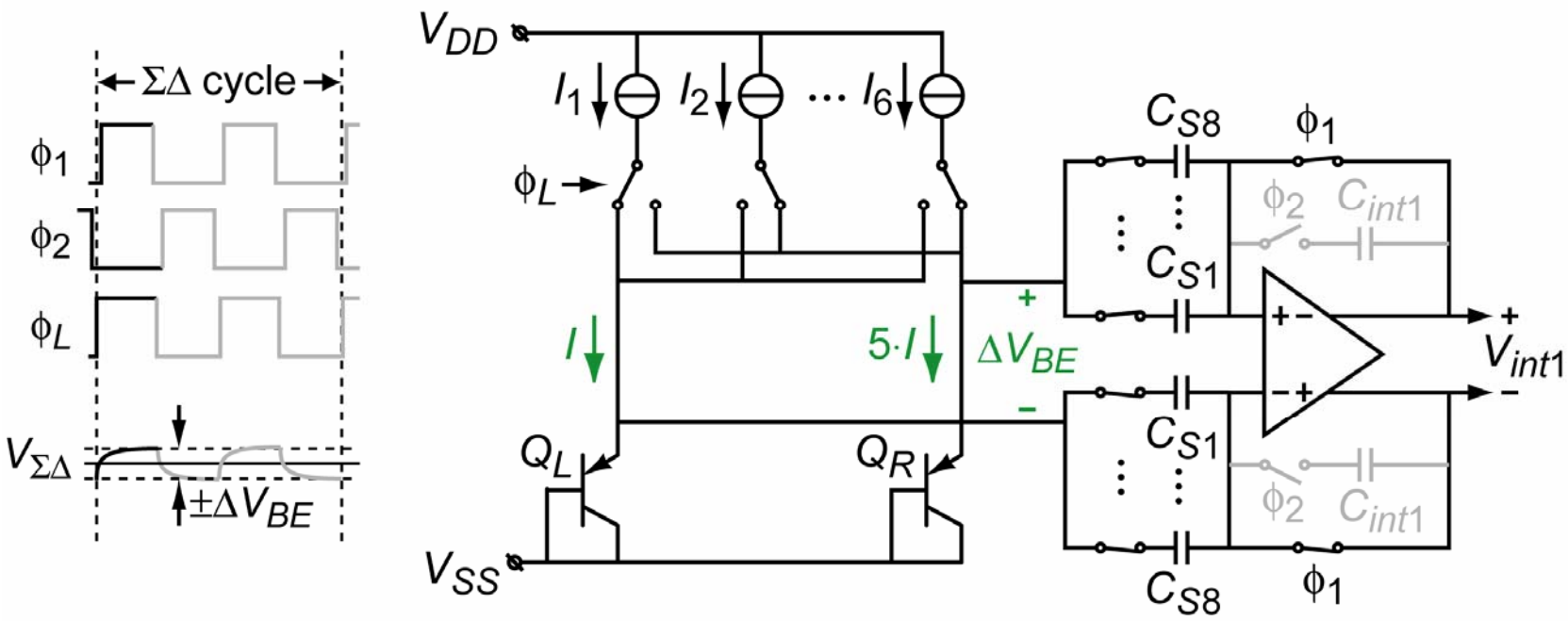
$$\mu \cdot V_{BE} = (1-\mu) \cdot 16 \cdot \Delta V_{BE} \Rightarrow \mu = \frac{16 \cdot \Delta V_{BE}}{V_{BE} + 16 \cdot \Delta V_{BE}} = \frac{16 \cdot \Delta V_{BE}}{V_{REF}}$$

Switched-Capacitor 1st Integrator



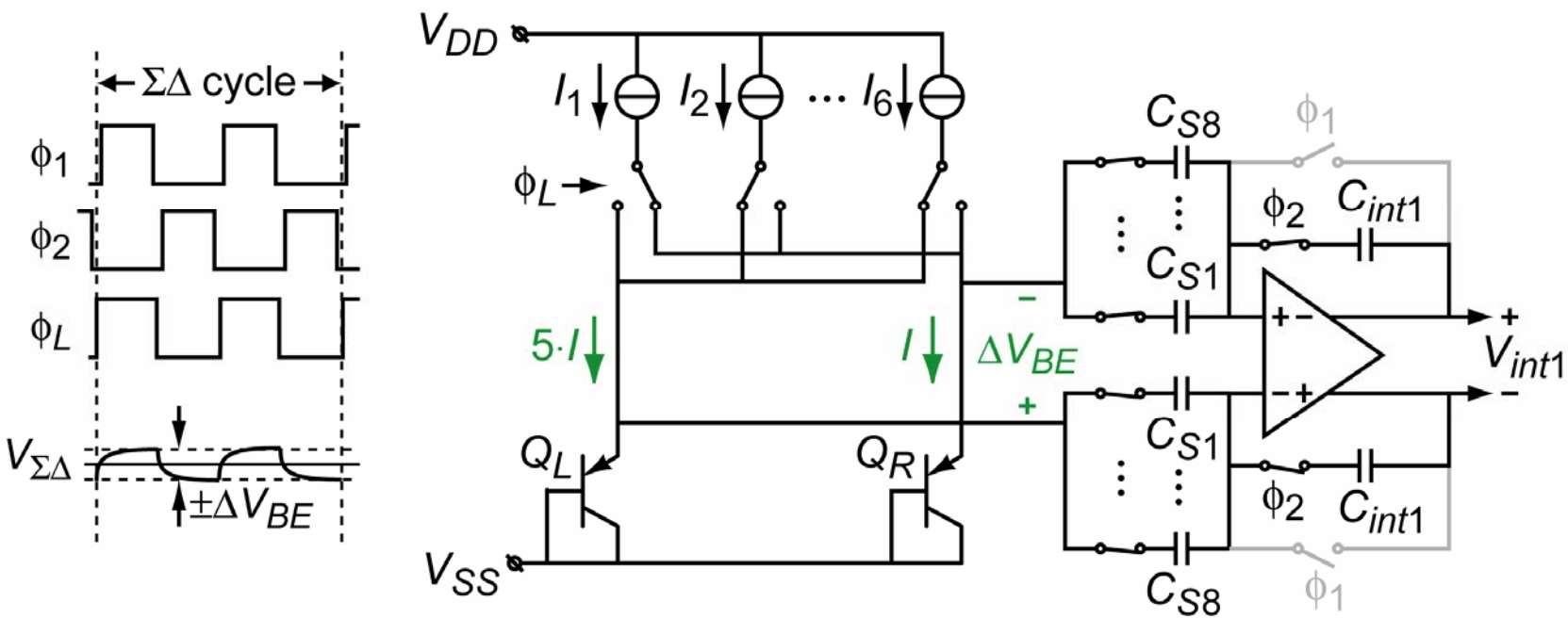
- PNPs Q_L and Q_R generate ΔV_{BE} (bs=0) or V_{BE} (bs=1)
- C_{S1}-$C_{S8} \Rightarrow$ gain of 1 or 16 (with 2 integration cycles)
- Correlated double-sampling (CDS) used to sample ΔV_{BE} *or* V_{BE} **and** cancel opamp's offset and 1/*f* noise

ΔV_{BE} Sampling (*bs*=0)



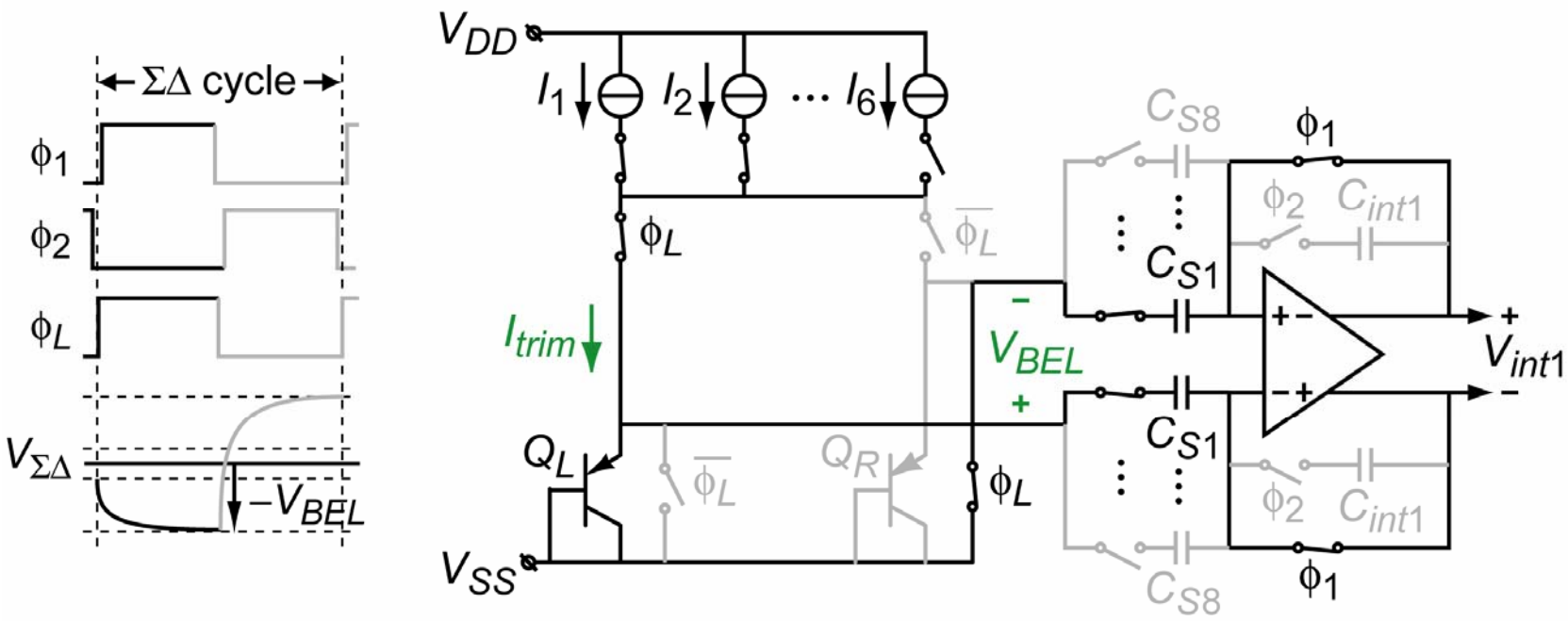
- PNPs biased at 1:5 current ratio
- $\Delta V_{BE,RL}$ **and** offset sampled on 8 sampling capacitors
- Minimum size NMOS switches + 5pF caps
  $\Rightarrow$ residual offset ~ 10μV $\Rightarrow$ too high

ΔV_{BE} Integration (*bs*=0)



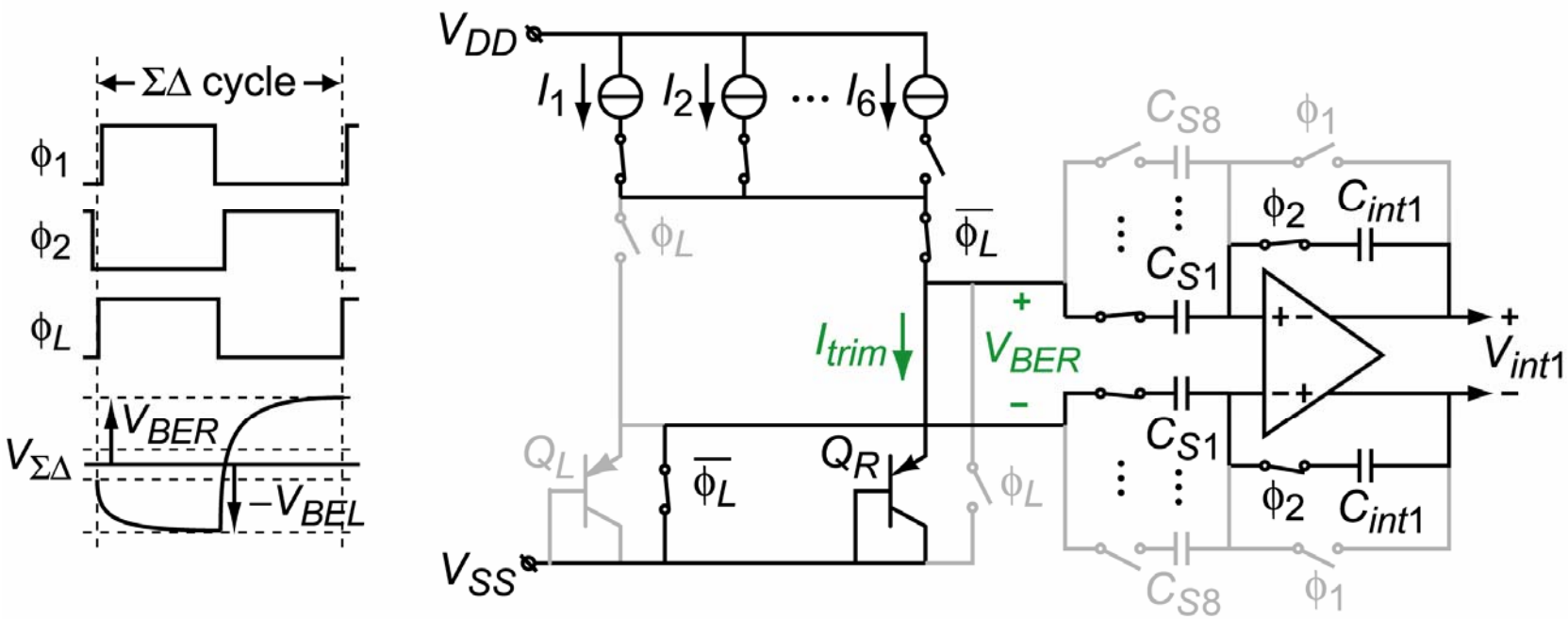
- Bias currents are swapped
  $\Rightarrow$ integrated charge: $8 \cdot C_S \cdot (\Delta V_{BE,RL} + \Delta V_{BE,LR})$
- 2 integration cycles in 1 ΣΔ cycle
  $\Rightarrow$ total charge: $16 \cdot C_S \cdot (\Delta V_{BE,RL} + \Delta V_{BE,LR})$

V_{BE} Sampling (bs=1)



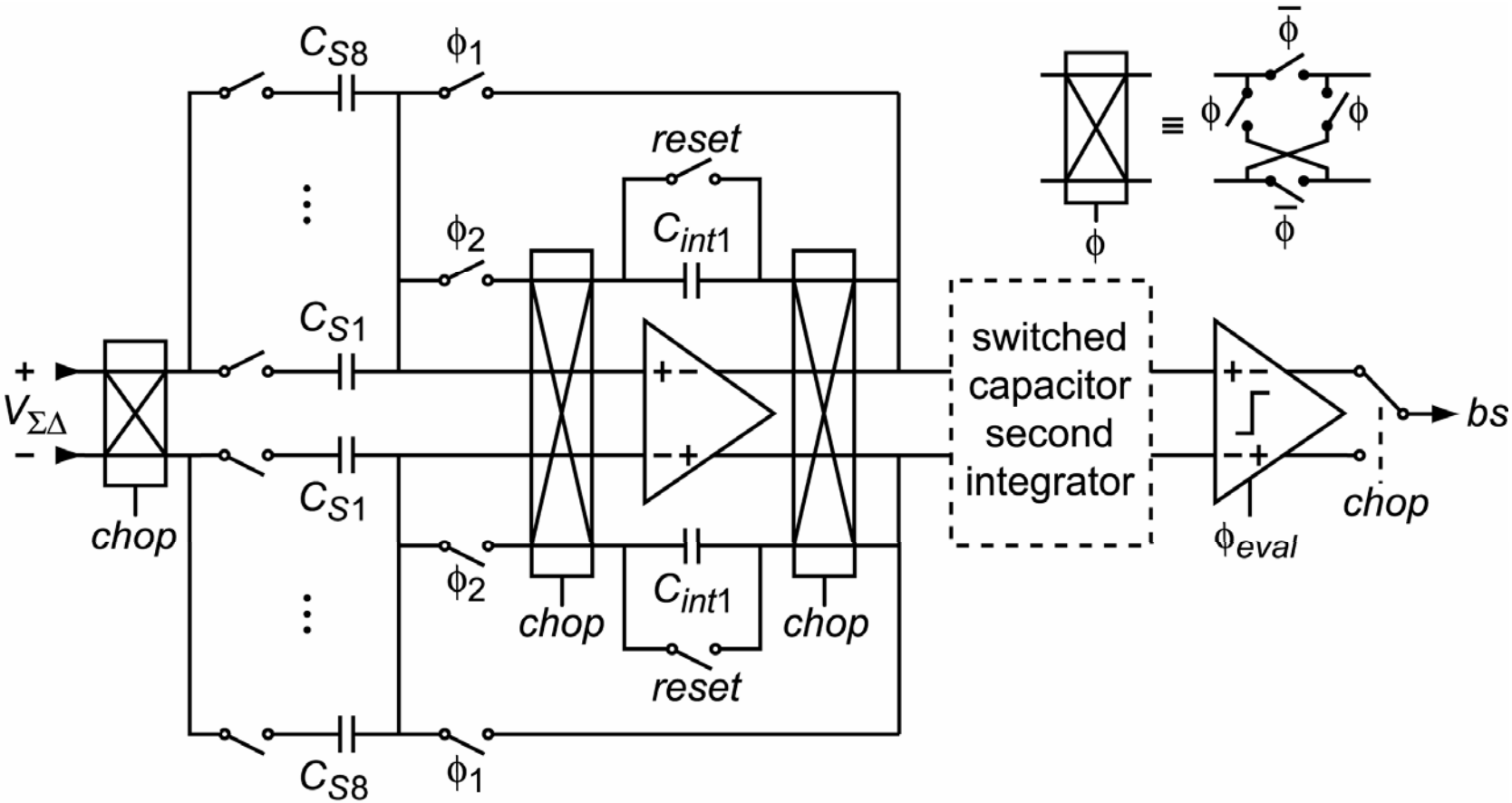
- Q_L biased at programmable current I_{trim}
- $-V_{BEL}$ and offset sampled on 1 sampling capacitor

V_{BE} Integration (bs=1)



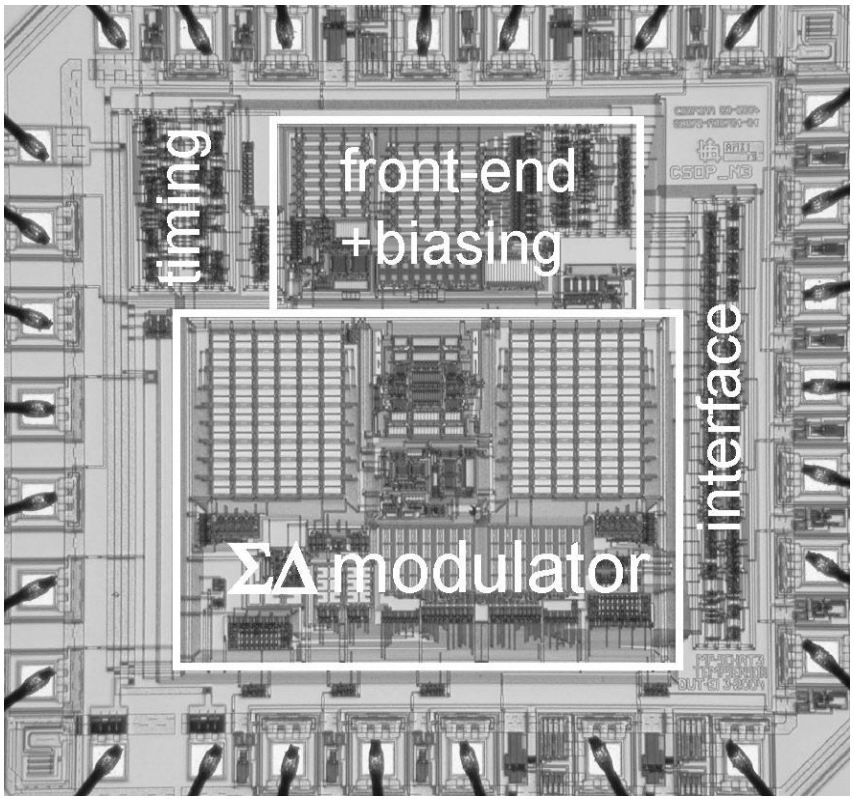
- I_{trim} swapped to Q_R
  $\Rightarrow$ total charge: $C_S \cdot (V_{BEL} + V_{BER})$
- compare with $16 \cdot C_S \cdot (\Delta V_{BE,RL} + \Delta V_{BE,LR})$
  $\Rightarrow$ effective 16x gain for ΔV_{BE}

Chopped ΣΔ Modulator



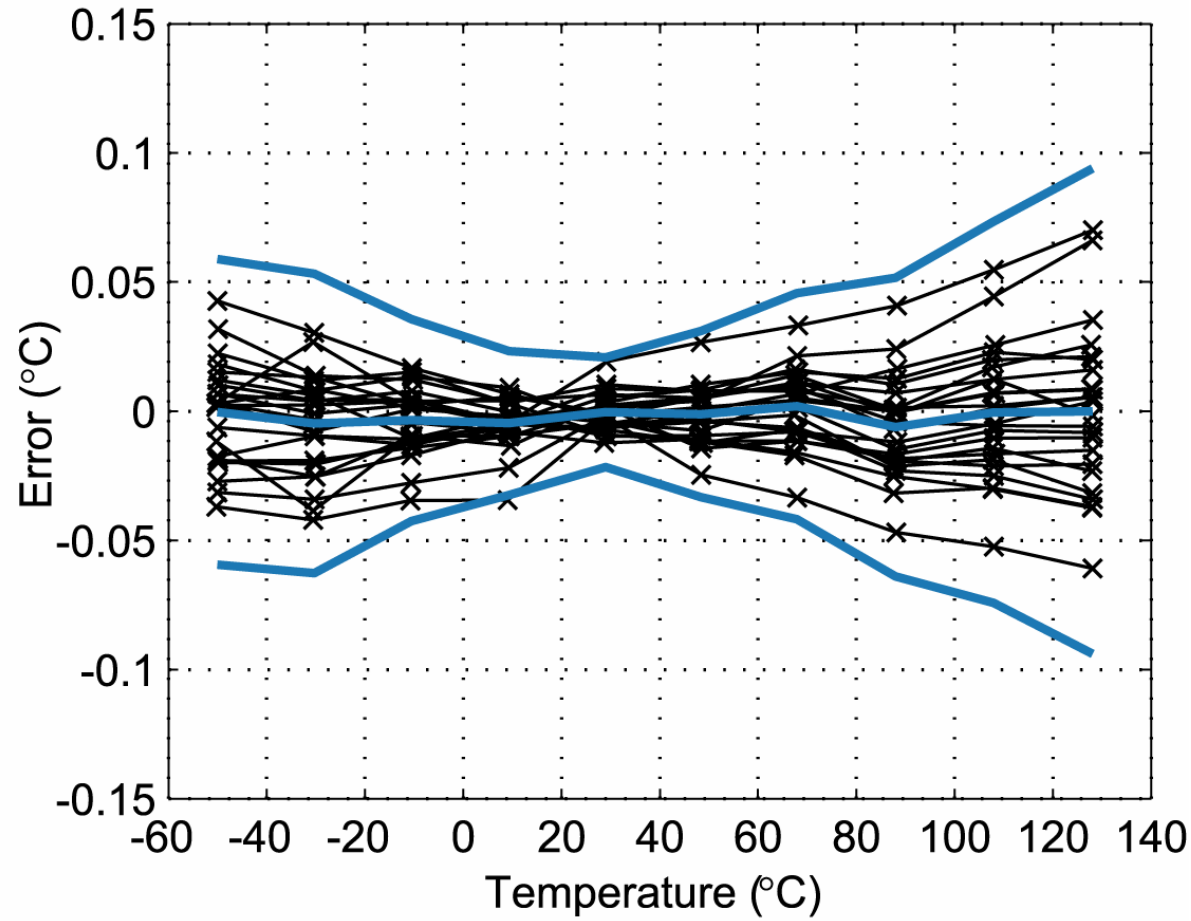
Offset after CDS >10μV ⇒ input, output **and** modulator state are chopped 2x per conversion ⇒ sub-μV offset

Chip Micrograph



- 4.5mm^2 in 0.7μm CMOS
- Off-chip decimation filter removes chopper residuals
- Supply voltage: 2.5..5.5V
- Supply current: 75μA

Measurement Results



24 samples
from 1 batch

Inaccuracy ($\pm 3\sigma$)
after trimming
at 30°C:

±0.03°C 30°C
±0.1°C –55..125°C

World's most
accurate CMOS
temp sensor!

Summary

- Offset and 1/*f* are part of life!
- Trimming
  - reduces offset but not 1/*f* noise
  - no loss of bandwidth
- Auto-zeroing
  - Reduces 1/*f* noise, but sampling $\Rightarrow$ noise aliasing
  - Indirect loss of bandwidth
- Chopping
  - eliminates 1/*f* noise
  - Direct loss of bandwidth
- Nested DOC techniques $\Rightarrow$ sub-microvolt offset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