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LC-VCO Design Methodology Based on Evolutionary Algorithms

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Abstract—**In his paper the design of LC-VCOs is addressed. Due to the high-density integration needs as well as to low cost fabrication, RF applications are usually implemented in CMOS technology. However, this technology development brought up several issues such as the degradation of on-chip LC tank quality factor, yielding VCO's phase noise limitation. To overcome phase-noise limitations, optimization design methodologies are usually used. Since electromagnetic simulations are timely expensive, model based approaches are needed. In this work the characterization of the oscillator behaviour is guaranteed by a set of analytical models describing each circuit element performance. A set of working examples for UMC130 technology, aiming the VCO phase noise and power consumption optimization, is addressed. The results presented, spotlight the potential of the proposed design methodology, combined with a GA optimization procedure, for an accurate and timely efficient oscillator design. The accuracy of the results is checked against HSPICE/RF simulator.**

Keywords—LC-VCO; Design methodology; Discrete-Variable Optimization; Evolutionary Algorithms

I. INTRODUCTION

The progressive scaling of CMOS technology towards nanometre sizes has made the implementation of highly integrated systems for the wireless communication systems possible. Additionally, higher speed, lower power consumption and area reduction has been reached. Due to the high-density integration needs, as well as to low cost fabrication, RF applications are usually implemented in CMOS technology. However, this technology development brought up several issues, such as the degradation of the phase noise or the increase in the power consumption due to low on-chip *LC* tank quality factor (*Q*). As a matter of fact the inductor *Q* in the GHz range of operation is in the order of 5 to 15, due to the thin metal thickness and to the substrate losses [1]. Yet, as the process technology improves and the number of metal layers increases, the passive elements *Q* is improving [2]. Furthermore, the technology scaling has lead to a decrease in the supply voltage, thus making the analog design more challenging, since neither a wide range of linearity nor full output voltage swing are easily guaranteed [3].

In the literature several methodologies for the design of *LC* tank voltage controlled oscillators (*VCO*) have been proposed. In [4] a methodology for reducing the phase noise of a cross-coupled *LC* tank *VCO* is proposed, where a 2 GHz LC-VCO is designed and fabricated in 0.18 μm CMOS technology. However, this methodology suffers from being based in fundamental relationships between the phase noise and the channel length, without exploring other optimization opportunities. A design approach where a graphic design space regarding design constraints, allowing a deeper insight into the LC tank behaviour, is offered to the designer is proposed in [5]. Though, the previous work presents a very straight design methodology, based on bifurcation analysis, which is difficult to adapt to new design strategies. In [6] a heuristic algorithm that seeks to determine optimal designs for inductors, bias current and transistors channel widths, aiming to minimize the VCO phase noise is considered. However, the analytical models that characterize the elements behaviour, do not account for parasitics, which are subsequently obtained through simulations. A very low-voltage *LC-VCO*, where bias controllability is introduced, is presented in [7]. Yet, the analytical models used are very simple, being functional just for the proof of concept. More recently, the design of an *LC*-VCO based on the g_m/I_D technique, exploring all inversion regions of CMOS transistors, is proposed in [8]. Yet, the g_m/I_D technique is not easily extended for the characterization of the varactor. Regarding the optimization procedure, a complete description of an integrated LC-VCO design is presented in [9], where the complexity of the optimization design, regarding the number of variables involved, is focused. A graphical optimization methodology using nonlinear programming is proposed, providing essential intuitions in finding the optimum solution.

The main advantage of the methodology proposed in this work is twofold. In one hand the use of accurate device models, makes the determination of design parameters very rapid. On the other hand as the model parameters are exclusively based on technological parameters, the adaptability of the design process to new technologies is extremely easy.

Besides the Introduction, this paper comprises four additional sections. Section II presents the *LC-VCO* optimization approach used in the proposed work. Then, in Section III, a brief description concerning the oscillator performance characteristics is presented. A set of *LC-VCO* design examples is presented in Section IV, where the solutions obtained with the proposed methodology are compared against

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HSPICE/HSPICE RF simulation results. Finally, conclusions are offered.

II. LC-VCO Optimization Approach

When designers have in hands the task of designing a *VCO*, one of the main challenges is to obtain results between simulation and on-chip measurement as close as possible. For this propose, accurate models are essential for each of the circuit blocks, where parasitics must be accounted for. For the dimensioning of *LC-VCOs*, the design methodologies usually adopted, rely on the accuracy of models of each element. Even though designers may use very accurate models, for predicting the *VCO* performance, there will always be a certain error due to some parasitic effects that appear in the manufacturing process [10]. For that reason a *VCO* is always tunable. In Fig. 1 a cross coupled *LC-VCO* with two main blocks is represented; the *LC* thank responsible for the oscillation frequency, and the active circuit which accounts for reducing the circuit losses by introducing a negative resistance. Most *LC-VCO* designs aim at achieving both minimum phase noise and power consumption for a certain oscillation frequency. In Fig. 2 the typical design trade-offs for an *LC-VCO* are depicted. For instance, if low power consumption is desired, a low bias current must be delivered to the circuit. Yet, parasitic effects will have a major role in circuit behaviour, yielding to the degradation of phase noise. On the other hand, if low phase noise is required, high output voltage swing is desired. To achieve this goal, either the power consumption increases or the *VCO* tuning range shrinks, due to a higher inductance. The necessity for coping with correlated design parameters makes the *VCO* design a candidate for optimization based design methodologies.

In this work an optimization-based *LC-VCO* design methodology is proposed. The design flow for the proposed methodology is represented in Fig. 3.

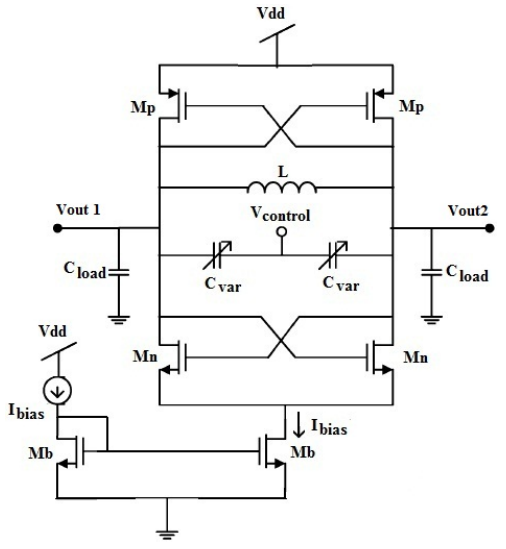

Figure 1. Cross coupled LC-VCO topology

Considering the *LC-VCO* topology illustrated in Fig. 1, the design process starts with the design of the active elements, since the drain current in each transistor is the dominant contributor to the phase noise. The following step addresses the optimization of the *LC* tank, by maximizing both the corresponding quality factor, and tank tuning range. Therefore, the overall optimization procedure main goals will consist on the minimization of the circuit power consumption and phase noise. To deal with both criteria, a figure of merit (FoM), described in the next Section, will be adopted.

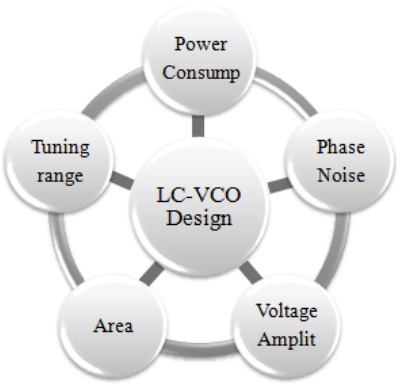

Figure 2. LC-VCO design trade-offs

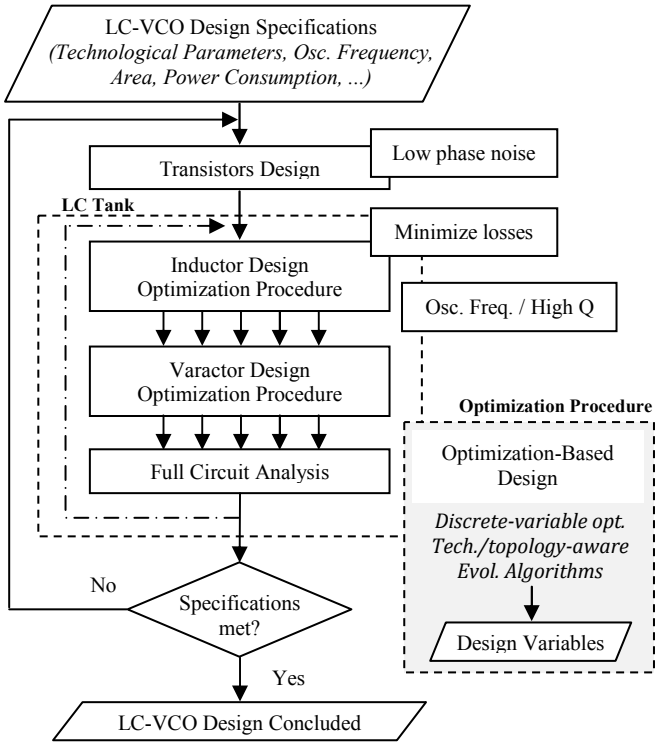

Figure 3. LC-VCO optimization design flowchart

III. Circuit Modelling

The efficiency of the optimization process is guaranteed through the use of its elements analytical models. For the clarity of exposure, and due to space constraints, just a brief description of the analytical models used will be done. The characterization of the CMOS transistors is based on the well know EKV MOS [11]-[12], guaranteeing the accuracy of the results for low-voltage circuit design. In the EKV model the drain current is given by a single expression for linear and

saturation regimes of operation and valid from weak to strong inversion. The characterization of the varactor behaviour is also supported by EKV MOS model equations, which are based on process and technological parameters, avoiding the undesired empirical/fitting factors granting the accuracy of the results [14]. With respect to the inductor, the double pi-model is adopted [13], where the model element values are obtained though analytical expressions based on both technology parameters and device geometric characteristics.

Concerning the full *LC-VCO* characterization, the fundamental equations for the oscillation frequency and oscillation condition are given by

$$f_0 = \frac{1}{2\pi\sqrt{\mathrm{L_{tank}\,C_{tank}}}}, \tag{1}$$

$$\alpha \cdot g_{\mathrm{tank,max}} \le g_{\mathrm{active}}, \tag{2}$$

where α in the range of 2-3 assures the start-up condition. The tank and active conductances, g_{tank} and g_{active} ,respectively, are obtained through

$$g_{\mathrm{tank}} = g_{\mathrm{ind}} + g_{\mathrm{var}} + \frac{g_{\mathrm{ds,p}}}{2} + \frac{g_{\mathrm{ds,n}}}{2}, \tag{3}$$

$$g_{\mathrm{active}} = \frac{g_{\mathrm{m,p}}}{2} + \frac{g_{\mathrm{m,n}}}{2}. \tag{4}$$

The differential output voltage, $2\cdot V_{tank}$, is determined as in

$$\mathrm{V_{tank}} = \frac{4}{\pi}\frac{\mathrm{I_{bias}}}{g_{\mathrm{tank}}}. \tag{5}$$

In order to supply enough voltage swing to the following circuit, V_{tank} can be limited to $V_{tank,min}$

The oscillation tuning range is given by

$$\frac{1}{\sqrt{\mathrm{L\,C_{tank,\,max}}}} \le \omega \le \frac{1}{\sqrt{\mathrm{L\,C_{tank,\,min}}}} \tag{6}$$

where the C_{tank} takes into account the both the varactor capacitance, and the active elements output capacitance.

Phase-noise is an elementary characteristic of a VCO that depicts the purity of the oscillation signal in the vicinity of the oscillation frequency f_0. In this work, the VCO phase-noise is obtained through [15]

$$L\{\Delta_f\} = 10\log\left[\frac{1}{16\pi^2\Delta_f^2}\cdot\frac{\mathrm{L_{tank}^2}(2\pi f_0)^4}{\mathrm{V_{tank}^2}}\cdot 2K_{\mathrm{B}}T\left[g_{\mathrm{L}} + g_{\mathrm{var}} + \gamma\left(g_{\mathrm{d0,p}} + g_{\mathrm{d0,n}}\right)\right]\right] \tag{7}$$

where g_{d0} is the drain conductance when V_{DS}=0, and γ is the excess noise factor. Finally, a figure of merit is used to compare circuits' performance, given by

$$\mathrm{FoM} = L\{\Delta_f\} - 20\log\left(\frac{f_0}{\Delta_f}\right) + 10\log\left(\mathrm{P_{dc(mW)}}\right) \tag{8}$$

IV. LC-VCO Optimization and Simulation Results

The present work proposes an *LC-VCO* design methodology that was implemented in Matlab and uses the Genetic Algorithms (GA) toolbox. In this section the design of three *LC-VCO*s for operating frequencies of 1.0, 2.4 and 2.8 GHz in UMC130 technology are addressed. The design objective functions are the minimization of both the phase noise and the power consumption The VCO characteristics and parameters range are given in Table I. The results obtained with the proposed methodology as well as those obtained through HSPICE and HSPICE RF simulations, are presented in Table II. The average computational time is approximately 20 seconds. In all the VCO characteristics the error is always less than 10%, showing a quite good agreement between predicted and simulations results. Yet, the use of a tunable capacitor provides the VCO with the possibility of reducing this error.

Table III presents a comparison between results obtained with the present design methodology, and results published in related work. Despite identical results for phase noise and FoM, the proposed design has lower implementation area, due to a smaller I_{bias} that corresponds to smaller active elements.

TABLE I. LC-VCO Characteristics & Parameters Limits

Center frequency - f_0 & Δ_f	1.0, 2.4, 2.8 GHz / 1 MHz
Bias current	0.5 mA – 5 mA
Output voltage swing	$V_{DD}/8$ – $V_{DD}/2$
Transistor width	$3\cdot L_{min}$ – 100 µm
Tank inductance - L	1 nH – 15 nH
Tank capacitance - C_{var}	1 pF – 20 pF
C_{Load}	1 pF

TABLE II. Optimization Design Results vs Simulation

	1.0 GHz		**2.4 GHz**		**2.8 GHz**	
	Optim	**Hspice**	**Optim**	**Hspice**	**Optim**	**Hspice**
I_{bias} (mA)	1.00	1.05	1.50	1.58	1.25	1.31
W_p (µm)	217.8	- -	326.8	- -	272.3	- -
W_n (µm)	88.6	- -	132.9	- -	110.8	- -
W_b (µm)	78.6	- -	117.9	- -	98.3	- -
L_{tank} (nH)	7.0	- -	2.0	- -	1.5	- -
C_{var} (pF)	4.40	4.44	1.28	1.32	1.36	1.39
V_{outAmp}(V)	0.16	0.18	0.23	0.27	0.18	0.21
P_{dc} (mW)	1.20	1.25	1.80	1.86	1.50	1.56
f_0 (GHz)	1.01	0.95	2.40	2.20	2.81	2.60
L{1MHz} (dBc/Hz)	-115.5	-116.2	-109.4	-121.5	-105.8	-122.6
FoM (dBc/Hz)	174.7	174.8	174.4	185.6	173.0	188.9

In Fig. 4 the VCO output signals for an oscillation frequency of 1.0 GHz are presented. With the proposed design, after 10 ns the VCO reaches to oscillation stability. The output signal oscillates between 0.66 and 1.04 V, which represents a

tank output swing of 0.38 V, as shown in Fig. 5. Also, at the centre frequency, 1.0 GHz, the oscillator phase noise reaches to -116.2 dBc/Hz.

TABLE III. COMPARISON OF PUBLISHED VCO PERFORMANCES

Ref	Tech	*f*o (GHz)	Pdc (mW)	L{1MHz} (dBc/Hz)	FoM (dBc/Hz)
Prop. work	CMOS 0.13 µm	2.4	1.80	-109.4	174.7
[6]	CMOS 0.35 µm	2.6	8.20	-124.9	184.1
[16]	SiGE-BJT process	2.4	41.2	-128.0	179.5
[17]	CMOS 0.18 µm	2.2	5.17	-119.0	179.0

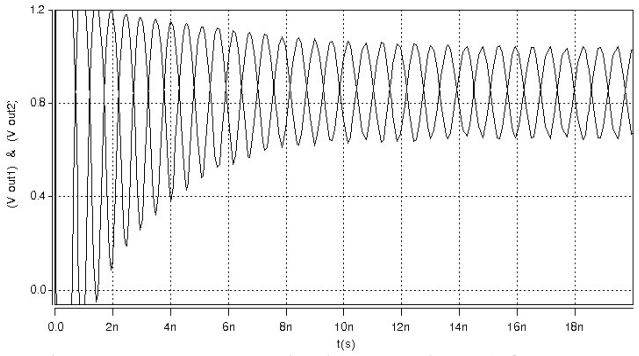

Figure 4. LC-VCO output signal (Vout1 and Vout2) @ 1.0GHz

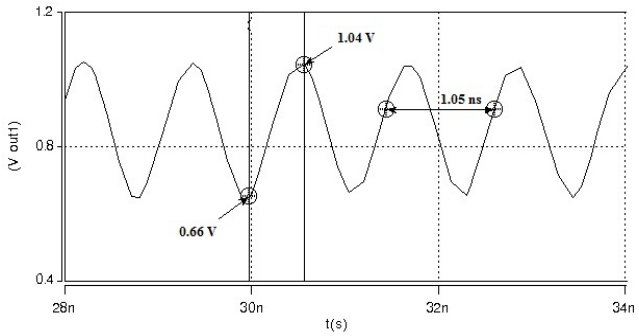

Figure 5. Vout1@1.0GHz with indication of signal period and output swing

V. CONCLUSIONS

This paper introduces an *LC-VCO* Design Methodology based on Evolutionary Algorithms. The oscillator analytical model is supported by a set of equations based exclusively in technology parameters. The optimization design tool presented in this work has two main advantages: i) as the VCO model is based in technological parameters, it may be straightforwardly adapted to new technologies; ii) reduced computation time, if compared with electromagnetic simulator –based optimization procedure.

Furthermore, in this work the design of *LC-VCO* is supported by a GA optimization methodology, which is able to deal with both continuous and discrete variables, making possible to satisfy both technological and layout constraints. A set of design examples showing the design of three *VCOs* for different oscillation frequencies is shown. The results presented, duly validated against HSPICE/RF simulations, point out the potential of proposed work, when integrated in a top-level design tool.

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