Fast & Energy Efficient Start-Up of Crystal Oscillators by Self-Timed Energy Injection

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Abstract—Crystal oscillators take a long time and, more importantly, a significant amount of energy to start-up. This article presents a self-timed energy injection technique to quickly start-up a crystal oscillator, for very low energy consumption. This is achieved without a power-hungry oscillator to provide the injection signal. The design considerations are discussed, and a prototype crystal oscillator using the proposed technique is integrated into a 22-nm fully depleted silicon-on-insulator (FD-SOI) technology. Connected to a 50-MHz crystal, the manufactured IC achieves a start-up time of 6 µs, for an energy consumption of just 3.7 nJ.

Index Terms—Crystal oscillators, duty cycling, energy injection, Internet of Things (IoT), low power, start-up energy, start-up time.

I. INTRODUCTION

LOW-POWER wireless systems are on the rise, with applications in the Internet of Things (IoT), such as Bluetooth low energy (BLE). Supply energy is usually scarce in these applications as power is often delivered by batteries or energy harvesting, necessitating techniques to achieve low power consumption. Duty cycling is one way to achieve low (average) power consumption. A duty-cycled system spends most of the time in a low-power sleep mode, only briefly waking up to transmit or receive packets in the active mode [1]. The transition from sleep mode to active mode requires starting up the radio circuit blocks, which take some time for settling. Most circuit blocks, such as the low-dropout regulator (LDO) and phase-locked loop (PLL), settle quickly (tens of microsecond range) [2]. However, the crystal oscillator that serves as frequency reference conventionally starts up relatively slowly (millisecond range) [3]–[7] due to the high-quality factor of the crystal resonator. The start-up of this crystal oscillator not only dominates overall start-up time but—more importantly—comes with large energy consumption, gravely compromising battery life. This article presents a technique to quickly start-up crystal oscillators with very low energy consumption.

A typical crystal oscillator is shown in Fig. 1. The RLC model of the crystal models the fundamental resonance mode by a series (motional) branch consisting of \(L_m\), \(C_m\), and \(R_m\), in parallel with the package parasitic capacitance \(C_p\). During start-up, the amplitude \(I_m\) of the sinusoidal series branch current \(I_m(t)\) grows from its initial value \(I_m(0)\) to its steady-state amplitude \(I_{m,SS}\) [8]. Conventionally, the oscillation is started and sustained by an active circuit, as shown in Fig. 1. This circuit provides a complex impedance, consisting of an imaginary part, formed by \(C_{load}\) as specified by the crystal manufacturer, and a negative real part, usually called as the negative resistance \(R_N\), which compensates the crystal losses. Since the initial condition is typically very small (noise), and the magnitude of the negative resistance is quite small, the start-up is typically a lengthy and inefficient process. Recent literature has presented solutions that improve the start-up time and/or energy consumption by injecting energy into the crystal before settling to the steady-state [8]–[15] and/or increasing the magnitude of the negative resistance during start-up [3], [10], [13], [16], [17].

The magnitude of the negative resistance can be boosted by increasing \(g_m\) [10], [13], [16]–[19] and/or altering the load capacitance \(C_{load}\) [16], [20]. However, the maximum negative resistance, and hence minimum start-up time, is limited by \(C_p\) [10], [13], [17]–[19]. This can be overcome by making the active circuit appear slightly inductive to (partially) cancel \(C_p\) [13], [17]. Although this solution is among the most energy-efficient in the literature, the start-up time is still relatively long, as perfect cancellation of \(C_p\) over process, voltage, and temperature (PVT) variations is difficult.

Another way to reduce the startup time is energy injection [8]–[15]. During start-up, an injection oscillator is connected to the crystal, as shown in Fig. 2. The injection oscillator injects energy at the frequency of the crystal. Fig. 3 shows an example of a square-wave injection waveform and the resulting growing amplitude of \(I_m\). Provided that the crystal quality factor is high \((R_m\) is small), the amplitude \(I_m\) can
be calculated to (initially) increase linearly over time with a slope of $\frac{A}{2L_m}$ [21], where $A$ is the amplitude of the fundamental of the injection waveform [8], [10]. Although the repetitive (dis)charging of $C_p$ introduces significant $CV^2$ losses, the start-up slope is not dependent on $C_p$, as opposed to negative-resistance based circuits.

However, a major challenge in energy injection techniques is the accuracy of the injection oscillator. To be effective, the injection signal should be in phase with the current waveform over the entire injection time. Since the start-up takes at least hundred(s) of periods, this puts tough requirements on the frequency accuracy of the injection oscillator, i.e., better than 0.5%, over PVT variations [9]. To achieve the required accuracy, the prior art has resorted to measures, such as calibration or trimming [8], [11], [12], chirping [10], [13], dithering [9], or injecting in multiple steps [14], [15]. Calibration attempts to exactly track the crystal frequency, which is power consuming and difficult to ensure over PVT. Chirping and dithering spread the energy over a frequency band, such that there is always a certain amount of energy injected in the crystal, even with frequency uncertainty due to PVT variations. However, this also reduces the amount of energy into the crystal, such that it takes a longer time to reach the steady-state amplitude. Injecting over multiple steps in time reduces the frequency accuracy requirements on the injection oscillator since the injection signal only needs to be in phase with the crystal oscillation for a short time. On the other hand, additional time and circuitry are necessary to synchronize the injection signal with the crystal oscillation. The lowest startup time with energy injection can be obtained if the injection duration $t_{\text{injection}}$ is precisely timed as to inject the exact amount of energy into the crystal that is required to reach

the steady state amplitude [8]. However, the generation of the injection signal requires frequency tuning to the specific crystal.

This article proposes a self-timed energy injection technique that allows quick and energy-efficient start-up of crystal oscillators, without the use of an injection oscillator. This is achieved by realizing that the injection waveform, as shown in Fig. 3, ideally switches polarity at each zero-crossing of the current. Instead of relying on an injection oscillator to generate the timing, the zero crossings can be directly detected to generate a self-timed injection signal.

Section II further elaborates on the concept of self-timed energy injection. Section III covers the circuit implementation and Section IV shows simulation results. Measurement results on a prototype are described in Section V, followed by a conclusion in Section VI.

II. SELF-TIMED ENERGY INJECTION

A. Concept

The proposed self-timed energy injection relies on the measurement of the motional current $I_m$. To minimize $CV^2$ losses, there are no load capacitors connected during start-up. It is impossible to directly measure $I_m(t)$ since the motional branch is in parallel with $C_p$, so any current measured at the crystal terminals could flow in either the motional branch or $C_p$. This can be overcome by ensuring that no current flows in $C_p$, such that the current measured at the crystal terminals could flow in either the motional branch or $C_p$. This is achieved by applying (quasi-) constant voltages to the crystal by connecting it in an H-bridge, as shown in Fig. 4. For a zero-switch resistance, the voltage over the crystal settles immediately to $+V_{DD}$ or $-V_{DD}$, respectively. This means that $dV_{C_p}/dt = 0$ (except at the switching instants), meaning that $I_{C_p} = 0$, and hence all current $I_m$ flows through the low-impedance path to the supply. The switch current, therefore, accurately indicates the zero-crossing of $I_m$.

The current measurement can be performed by exploiting the non-zero on-resistance of practical switches. The voltage over a switch in "ON" state is a measure of the current flowing through it. The use of non-zero switch resistances has some implications that will be further discussed in Section II-B.

A block diagram of the proposed architecture is shown in Fig. 5. The switches to the ground have a low impedance, while the switches to the supply have a relatively high resistance to increase the current detection sensitivity. As $I_m(t)$ is normally very small before start-up, it is maximized by applying a single voltage step, leading to an initial oscillation which is large enough to be detected. Comparators are used...
to determine the direction of the current through the switches. Only the comparator that is connected to the switch in “ON” state is active. If the output of that comparator toggles, its input voltage has changed sign, meaning that $I_{m}$ has reversed direction. The switch control block then toggles the switches, and waits until the next zero crossing is detected, resulting in current and voltage waveforms similar to Fig. 3.

B. Switch Resistance

The current sensing sensitivity is critical at the beginning of start-up, where $I_{m}(t)$ is the smallest. A high switch resistance $R_{sw}$ is desired to maximize this sensitivity, resulting in a voltage drop of $I_{m}(t) \cdot R_{sw}$. However, a non-zero switch impedance has two side effects. First, the voltage over the crystal does not immediately settle to $+V_{DD}$ or $-V_{DD}$ due to the RC-time constant of $C_{p}$ being charged through $R_{sw}$. Second, part of the current $I_{m}(t)$ flows through $C_{p}$ and part of it through the switch, such that there is a phase shift between $I_{m}$ and $I_{sw}$.

To analyze these effects during a single switch cycle, the circuit can be modeled, as shown in Fig. 6. The motional branch has a high Q-factor, such that it can be approximated as a sinusoidal current source with amplitude $I_{m}(t)$, which increases with each switching cycle. The model includes a parasitic capacitance $C_{par}$, consisting of parasitics like comparator input capacitance, bond pad capacitance, and PCB trace capacitance. The current through $R_{sw}$ can be separated in the individual contributions due to the charging of $C_{tot} = C_{p} + C_{par}$ and the motional current $I_{m}(t)$.

1) Charging Current: The current through $R_{sw}$ due to charging $C_{p}$ and $C_{par}$ can be calculated as follows:

$$I_{sw, charge}(t) = \frac{V_{DD} - V_{X}(0)}{R_{sw}} e^{-\frac{t}{R_{sw}C_{tot}}}.$$  

2) Motional Branch Current: $R_{sw}$ and $C_{tot}$ form an RC-filter, which affects the phase and amplitude of the current $I_{sw}$ to $I_{m}$. The current through $R_{sw}$ due to the motional current $I_{m}$ can be calculated as follows:

$$I_{sw, m}(t) = A \hat{I}_{m}(t) \sin(\omega t - \varphi)$$  

where

$$\varphi = \tan^{-1} \frac{1}{\omega R_{sw}C_{tot}}$$

$$A = \frac{1}{\sqrt{1 + (\omega R_{sw}C_{tot})^2}}$$

3) Total Switch Current: By superposition, (1) and (3) can be added to yield the total switch current

$$I_{sw}(t) = A \hat{I}_{m}(t) \sin(\omega t - \varphi) + \frac{V_{DD} - V_{X}(0)}{R_{sw}} e^{-\frac{t}{R_{sw}C_{tot}}}. \quad (4)$$

Fig. 7 shows the individual contributions, as well as the total switch current $I_{sw}(t)$, over an oscillation period $T$.

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In this expression $C_{tot} = C_{p} + C_{par}$, and $V_{X}(0)$ is the initial voltage at the crystal terminal. The voltage over $C_{par}$ starts at 0 V, while $C_{p}$ is initialized to $-V_{DD}$ as a result of charging to $V_{DD}$ in the previous switch state. After switching, $C_{p}$ and $C_{par}$ share charge, such that the initial voltage $V_{X}(0)$ can be calculated as follows:

$$V_{X}(0) = -V_{DD} \frac{C_{p}}{C_{p} + C_{par}}. \quad (2)$$

Fig. 7. Modeled crystal voltage and switch current for a single switching event and (large) non-zero switch resistance. In actual operation, the circuit would switch again just after $t = T/2$.

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is taken when $I_{sw} = 0$, which is later than $t = 0.5T/2$ and depending on the switch resistance, as shown in Fig. 8. Furthermore, the delay from, for example, the comparator or D flip-flop, increases the time between the ideal switching time and the actual switch time. The latest point in time at which the injection waveform may switch is 90° ($T/4$) out of phase with $I_m$, as otherwise the oscillation would be damped instead of amplified. For a comparator delay $T_{D,comp}$, this means that $I_{sw}(0.75T - T_{D,comp}) < 0$, as shown in Fig. 8. Substitution in (4) yields
\[
\frac{1}{\sqrt{1 + (\omega R_{sw} C_{tot})^2}} I_m(t) \sin \left(\frac{3}{2} \pi - \tan^{-1} \frac{1}{\omega R_{sw} C_{tot}}\right) + \frac{V_{DD}}{R_{sw}} e^{2 \frac{T - T_{D,comp}}{R_{sw} C_{tot}}} < 0. \tag{5}
\]
This equation can be solved (numerically) for $R$ to find the maximum switch resistance $R_{max}$.

Note that $T_{D,comp}$ is in practice amplitude-dependent, and $I_m(t)$ is time-dependent. However, the first cycle is most critical since the motional current is at its smallest. In each cycle, the amplitude $I_m$ grows and the specifications on comparator and switch resistance become more relaxed. To maximize the initial current, a “single kick” is given to the crystal by applying a voltage step equal to the supply. The initial current amplitude after this “single kick” can be found by calculating the step response of an LC circuit to a step with amplitude $V_{DD}$, resulting in $I_m(0) = V_{DD} \sqrt{C_m / L_m}$, which is in the range of 150 nA–2 μA for typical crystals ranging between 16 and 50 MHz. Substituting in the equation for $R_{max}$ and assuming that the comparator delay is the negligible results in a maximum switch resistance that is typically in the order of 1 kΩ, depending on the crystal and the parasitics.

C. Comparator Specifications

Comparator offset results in decisions taken early or late, as shown in Fig. 9. If the offset is positive, the comparator decision is slightly late, while for a negative offset, the decision is taken slightly early. As discussed in Section II-B, the decision is delayed with respect to the ideal decision moment due to the charging of (parasitic) capacitances and comparator delay. Too much delay slows down the start-up process or can even dampen the oscillation. Therefore, in the circuit implementation, we make sure that the decision threshold is always below $V_{DD}$.

With this decision threshold always below the supply, comparator offset will cause a current-referred offset $|V_{offset}| / R_{sw}$, causing early comparator decision. The earliest allowable decision moment is at $t = (T/4)$. Hence,
\[
I_{sw} \left(\frac{T}{4}\right) < \frac{|V_{offset}|}{R_{sw}}. \tag{6}
\]
Using (4), this equation can be solved (numerically) for the maximum allowable offset for a given switch resistance. Fig. 10 shows the allowable offset for different values of comparator delay, for a 50-MHz crystal with $L_m = 1.18mH$ and $C_{tot} = 7pF$. Furthermore, the allowable switch resistance range is indicated, as calculated from (5), showing the design space of offset versus switch resistance that permits the oscillation to start at a frequency that will inject energy into the crystal.

Note that the current-referred offset may be larger than $I_m(0)$, but the start-up is still achieved as long as the decision moment is after $T/4$. In this case, the circuit can be regarded as a relaxation oscillator. This behavior, due to the $RC$-charging of $C_p$, is taken into account in the previous analysis. This means that, as long as the requirements set on offset and switch resistance are fulfilled, energy is injected into the crystal in each cycle, such as $I_m(t)$ grows.
III. CIRCUIT IMPLEMENTATION

A block diagram of the implemented circuit is shown in Fig. 11. The enable logic block enables the appropriate circuit blocks for start-up or steady-state. During start-up, the offset detection is briefly enabled, after which the start-up circuitry starts injecting energy into the crystal. The 15-pF load capacitor bank consists of 1-pF unit elements to allow various load capacitances, and is disconnected during start-up to minimize $CV^2$ losses.

After a pre-determined (externally controlled) start-up time, the start-up control block disables the start-up circuitry. The steady-state oscillator, as well as the load capacitor bank, is then enabled by closing the appropriate switches.

A. Start-Up Circuit

Fig. 12 shows the block diagram of the start-up circuitry. Since only one comparator is active at any instant in time, a single comparator is used, with a switch matrix that is controlled by the switch control logic, to connect the appropriate comparator inputs. The switch control logic block consists of static combinational logic. When the start-up circuit is enabled, the D flip-flop toggles every time the comparator detects a zero-crossing. This, in turn, toggles the H-bridge switches, as well as the comparator inputs, repeating the process until the start-up circuitry is disabled.

During the first 80 ns of each start-up cycle, the comparator offset sign detection is enabled by the enable logic. During this phase, both comparator inputs are connected to $V_{DD}$. The comparator output, which indicates the sign of the offset, is stored in an SR-latch. This serves as an input for the switch control logic, which swaps the comparator inputs and output when necessary to make sure that the decision threshold is always below $V_{DD}$.

The comparator is implemented as a continuous-time (limiting) amplifier, as shown in Fig. 13. The first differential pair is large to minimize offset and is connected to a symmetric active load. A second differential stage increases the gain and converts to a single-ended output, which is amplified by cascaded inverters generating rail-to-rail outputs.

The schematic of the H-bridge is shown in Fig. 14. A low-impedance path to ground is provided by large NMOS switches. The PMOS switches to the supply act as measurement resistors. Their impedance is binary scalable over a range of approximately 40 $\Omega$ to 1.3 k$\Omega$ to accommodate various crystals having different requirements on settling time and detection sensitivity. Self-quenching NMOS switches are connected in parallel to the PMOS switches to quickly pull-up the respective crystal nodes to $V_{DD} - V_{TH,N}$ after a switch event. In our current implementation, this allows a reduction in settling time by approximately one third, while retaining the PMOS switch resistance for current detection sensitivity.
55 pF of decoupling capacitance is integrated on-chip. Simulations show that any ringing due to switching of the H-bridge has damped before the next zero-crossing of \( I_m(t) \).

### B. Steady-State Oscillator

To demonstrate the transition from start-up to steady-state, a self-biased NMOS oscillator is integrated, as shown in Fig. 15. There is no amplitude control loop for simplicity. The bias current, however, is externally tunable to accommodate various crystals, as well as, enabling manual amplitude control. Binary switches allow coarse tuning while analog fine-tuning is possible through an external pin. Self-quenched NMOS transistors, triggered by a delay-line as one-shot, pull the load capacitor voltages to \( V_{DD} - V_{TH} \) to reduce the settling time of the steady-state oscillator during the transition from start-up to steady-state. The \( CV^2 \) energy consumption associated with charging the load capacitors is negligible.

#### IV. Simulation Results

The proposed circuit is implemented in a 22-nm FD-SOI technology with 0.8-V supply voltage. Fig. 16 shows waveforms for full-chip simulations with a 50-MHz crystal. At \( t = 0 \), the start-up circuit is activated, linearly increasing \( I_m \) after a brief offset sign detection phase. Although the initial injection frequency error is large, energy is injected in the crystal during the first few cycles, causing a linear growth of \( I_m(t) \). If the injection frequency was to be constant, \( I_m(t) \) would quickly saturate because the injection phase drifts away from the crystal phase. However, using the proposed technique, the injection phase aligns itself with the crystal oscillation as \( I_m(t) \) grows. The injection frequency, therefore, converges to the crystal (series) frequency, allowing \( I_m(t) \) to keep growing (approximately) linearly. At \( t = 3.4 \mu s \), the start-up circuit is disabled and the steady-state oscillator and load capacitors are enabled. The resonance frequency immediately switches to the parallel resonance frequency as evident from the frequency of \( I_m(t) \), while the frequency of the output voltage requires some settling time (approximately 6–7 \( \mu s \)). The simulated time required for the output frequency to settle within 20 ppm is 6.9 \( \mu s \), mainly due to dc settling of the steady-state oscillator. The steady-state oscillator has a differential swing of 320 mVpp. The switches that (dis)connect the crystal to the steady-state oscillator and load capacitors have a negligible effect on phase noise performance.

#### Table I

<table>
<thead>
<tr>
<th>Component</th>
<th>Energy (nJ)</th>
<th>% of total energy</th>
</tr>
</thead>
<tbody>
<tr>
<td>H-bridge</td>
<td>2.32</td>
<td>73%</td>
</tr>
<tr>
<td>Comparator</td>
<td>0.49</td>
<td>15%</td>
</tr>
<tr>
<td>Logic etc.</td>
<td>0.03</td>
<td>1%</td>
</tr>
<tr>
<td>Steady-state oscillator settling</td>
<td>0.33</td>
<td>10%</td>
</tr>
<tr>
<td><strong>Total start-up energy</strong></td>
<td><strong>3.19</strong></td>
<td><strong>100%</strong></td>
</tr>
</tbody>
</table>

#### A. PVT Variations & Mismatch

As discussed in Section II-C, comparator offset is an important factor in start-up time. The simulated comparator 1-\( \sigma \) offset is 0.8 mV. Fig. 17 shows Monte-Carlo simulation...
TABLE II
SIMULATED VARIATION OVER EXTREME PROCESS CORNERS AT 20°C

<table>
<thead>
<tr>
<th>Corner</th>
<th>Im(T_{inj}) (μA)</th>
<th>T_{inj} (μs) (untrimmed)</th>
<th>ΔT_{inj} (μs)</th>
<th>T_{start} (μs) (trimmed)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Nominal</td>
<td>908</td>
<td>6.9</td>
<td>0</td>
<td>6.9</td>
</tr>
<tr>
<td>SS</td>
<td>679</td>
<td>12.0</td>
<td>+1.07</td>
<td>10.2</td>
</tr>
<tr>
<td>FF</td>
<td>1048</td>
<td>6.3</td>
<td>-0.46</td>
<td>4.6</td>
</tr>
<tr>
<td>FS</td>
<td>916</td>
<td>7.3</td>
<td>-0.03</td>
<td>7.3</td>
</tr>
<tr>
<td>SF</td>
<td>899</td>
<td>9</td>
<td>0.03</td>
<td>8.8</td>
</tr>
</tbody>
</table>

results for local mismatch in the typical process corner, showing the spread in start-up time and energy after injecting energy for 3.4 μs to a 50-MHz crystal, without any calibration or tuning.

As the steady-state oscillator in the prototype is unregulated, the steady-state amplitude varies greatly over process corners. However, in a practical implementation, the steady-state oscillator would be compensated to have a constant swing over PVT variations. To achieve this swing in the shortest possible time, the injection time could be corrected as to yield the nominal steady-state current. Since \( \dot{I}_m \) is approximately a linear function of \( T_{inj} \), this could be achieved with a single trim. The additional start-up time due to variation in \( T_{inj} \) is listed in Table II. Simulations over extreme process corners confirm that start-up is achieved over process variations, as shown in Table II. \( \dot{I}_m(T_{inj}) \) is within \(+/-25%\) of its nominal value after a fixed injection time of 3.4 μs, without any tuning or calibration. The third and fourth column lists the required adjustment in \( T_{inj} \) to result in the same steady-state swing and the resulting settling time, respectively. Note that the variation in start-up time is mostly due to dc settling of the steady-state oscillator.

Simulations show minimal variation over circuit temperature, with \( \dot{I}_m(T_{inj}) \) varying less than 3% over \(-40 C \) to \(+85 C \). The settling time, however, varies between 6 and 9.6 μs due to the variation in steady-state oscillator settling. Simulations over supply voltages between 750 and 850 mV show a variation in \( \dot{I}_m(T_{inj}) \) ranging from 763 to 1041 μA, and start-up times between 6.9 and 9.4 μs.

Variation of the crystal \( L_m \), just like other injection techniques, has a direct influence on the growth of \( \dot{I}_m(t) \) since its slope varies with \( A/2L_m \). Simulations show a successful start-up for \( C_p \) varying over ±50%, as well as robustness over crystal quality factor, with only 3% variation in \( \dot{I}_m(T_{inj}) \) for a five times lower quality factor. These large variations in crystal parameters are unlikely to be encountered in practice.

V. MEASUREMENT RESULTS AND DISCUSSION

The proposed circuit was fabricated in Global Foundries’ 22-nm FD-SOI CMOS process. A photograph of the fabricated test-chip is shown in Fig. 18. The area breakdown is listed in Table III. The output voltages are buffered by off-the-shelf amplifiers (LTC6268) in the unity-gain configuration. Fig. 19 shows the conventional start-up sequence (without the proposed start-up technique) for a 5 × 3.2 mm² 50-MHz crystal from the Abracon ABM3 series. The start-up time is more than 16 ms, for an energy consumption exceeding 0.8 μJ. This long time is the result of the oscillator bias current being fixed for the final steady-state swing. The start-up would have been faster with an amplitude control loop.

The optimum injection time depends on the crystal frequency, as well as the desired output swing, which depends on \( \dot{I}_m \) and motional inductance, as well as the load capacitance. The injection time is controlled by an external microcontroller, but could easily be integrated on-chip by, e.g., counting comparator decisions. The optimum injection time is manually (iteratively) determined once to reach the desired steady-state swing, as in the prototype it is not possible to detect if the steady-state amplitude has been reached during the injection. The switch resistance is also determined manually, depending on the crystal’s motional inductance and parallel capacitance. The injection time and switch resistance are kept constant in the measurements over voltage and temperature variations. Fig. 20 shows the start-up transient with the proposed energy injection technique. After the injection time of 3.4 μs, the steady-state oscillator quickly settles to its steady-state amplitude, with a total start-up time of 6 μs.
Fig. 20. (a) Measured output voltages for a 50-MHz crystal in a 5 × 3.2 mm² package, with energy injection, for $T_{\text{inj}} = 3.4 \, \mu\text{s}$, at $T = 20^\circ$. (b) Zoomed-in view.

Fig. 21. Measured frequency error at 20 °C.

Fig. 22. Measured frequency settling at 20 °C.

Fig. 23. Measured start-up time and energy over temperature for $T_{\text{inj}} = 3.4 \, \mu\text{s}$.

As with any energy injection technique, driving the crystal not only excites the crystal fundamental tone but also other spurious tones as well. These become visible as slight frequency deviations after energy injection, until these spurs have damped after 1–2 ms. To show the frequency settling of the fundamental, the center frequency and IF bandwidth in measurement can be chosen such that the spurious tones fall out of band, assuming that a PLL would normally filter out these spurs. Fig. 22 shows the frequency settling measurement, showing that the frequency has settled within 20 ppm after only 6 μs.

The settling time after $T_{\text{inj}}$ is mainly due to dc settling of the steady-state circuit, and could be improved by reducing $R_{\text{fb}}$ (now 190 kΩ) in the steady-state oscillator, at the cost of increased power consumption. This is confirmed by simulation, showing that halving $R_{\text{fb}}$ results in 45% reduction of the settling time. The measured start-up energy is 3.7 nJ, more than two orders of magnitude lower than without the proposed injection technique.

Note that for measurement flexibility, the injection duration is externally controlled in the proposed prototype. However, an (initially inaccurate) clock signal is immediately available at the comparator output, which could be used to self-time the start-up circuit, e.g., by counting the number of cycles. An additional oscillator to generate this timing is therefore
not necessary. Additionally, this clock could be used for, e.g., coarse settling of a PLL or clocking digital circuitry.

Figs. 23 and 24 show the measured start-up time and energy over temperature and voltage, respectively. For both measurements, the injection time is kept constant. The steady-state oscillator bias current is manually adjusted to keep the amplitude constant.

Fig. 25 shows the measured and simulated amplitude just after disabling the start-up circuitry, as a function of $T_{inj}$. The measured amplitude for long injection times is significantly lower than those of the extracted simulations. Inclusion of

Table IV

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<td>CMOS process (nm)</td>
<td>180</td>
<td>90</td>
<td>65</td>
<td>65</td>
<td>65</td>
<td>65</td>
<td>55</td>
<td>65</td>
<td>22 FD-SOI</td>
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<tr>
<td>Supply voltage (V)</td>
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<td>1.0</td>
<td>1.2</td>
<td>0.35</td>
<td>1.68</td>
<td>1.0</td>
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<td>54</td>
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</tr>
<tr>
<td>Load capacitance (pF)</td>
<td>8</td>
<td>10</td>
<td>9</td>
<td>6</td>
<td>6</td>
<td>6</td>
<td>6</td>
<td>9</td>
<td>7</td>
</tr>
<tr>
<td>Steady-state amplitude (Vpp)</td>
<td>1.5</td>
<td>N/A</td>
<td>N/A</td>
<td>0.3</td>
<td>N/A</td>
<td>0.7</td>
<td>0.75</td>
<td>0.25</td>
<td>0.32</td>
</tr>
<tr>
<td>Steady-state power consumption (µW)</td>
<td>181</td>
<td>95</td>
<td>141</td>
<td>32</td>
<td>393</td>
<td>198</td>
<td>N/A</td>
<td>195</td>
<td>10</td>
</tr>
<tr>
<td>Start-up time (µs)</td>
<td>158</td>
<td>200</td>
<td>64</td>
<td>400</td>
<td>64</td>
<td>400</td>
<td>23</td>
<td>195</td>
<td>15</td>
</tr>
<tr>
<td>Temperature range (°C)</td>
<td>-30 to 125</td>
<td>-40 to 90</td>
<td>-20 to 55</td>
<td>-40 to 90</td>
<td>-40 to 85</td>
<td>-40 to 85</td>
<td>-40 to 140</td>
<td>-40 to 85</td>
<td>-40 to 85</td>
</tr>
<tr>
<td>Start-up time variation over temperature (°C)</td>
<td>±7%</td>
<td>28%</td>
<td>±10%</td>
<td>8%</td>
<td>±35%</td>
<td>±1%</td>
<td>±11%</td>
<td>N/A</td>
<td>23%</td>
</tr>
<tr>
<td>Start-up time (cycles)</td>
<td>6202</td>
<td>4800</td>
<td>2560</td>
<td>9600</td>
<td>1536</td>
<td>1026</td>
<td>736</td>
<td>98</td>
<td>360</td>
</tr>
<tr>
<td>Start-up Energy (nJ)</td>
<td>349</td>
<td>37†</td>
<td>37†</td>
<td>14†</td>
<td>25†*</td>
<td>35†</td>
<td>20†</td>
<td>9†</td>
<td>4.4</td>
</tr>
</tbody>
</table>

* ESTIMATED BY MULTIPLYING STEADY-STATE POWER CONSUMPTION AND START-UP TIME
† INCLUDING CLOCK BUFFER POWER
additional board parasitics and comparator offset in the simulation did not improve the match, leaving the exact reason for the deviation unknown. Fig. 26 shows the measured start-up time over switch resistance variation.

The measured phase noise is $-123 \text{ dBc/Hz}$ at 1-kHz offset. The phase noise can be lowered by increasing the injection time and steady-state bias current, increasing the output swing at the expense of increased (start-up) energy consumption.

Table IV lists the measured performance, for both a 24- and 50-MHz crystal, and compares it to the state-of-the-art. The startup time and startup energy comparison are also graphically shown in Fig. 27. Compared to the work with the lowest $E_{\text{start}}$ in the literature, which uses energy injection, the start-up time is longer due to a lower injection amplitude caused by a lower supply voltage, as well as comparator delay. However, the energy consumption, using identical crystal part numbers, is 2.6 times lower.

VI. CONCLUSION

In this article, a self-timed energy injection technique is proposed, enabling quick and energy-efficient start-up of crystal oscillators. This is achieved by detecting the zero crossings of the motional branch current of the crystal and using this information to switch the voltage over the crystal. Since the injection waveform is self-timed, the injection frequency automatically matches the crystal frequency. This allows accurate energy injection, without the need for power-hungry frequency injection oscillators or calibration steps. The manufactured prototype achieves the start-up energy of 3.7 nJ.

To the authors' best knowledge, this is the lowest start-up energy reported in the literature so far.

ACKNOWLEDGMENT

The authors would like to thank Global Foundries, Dresden, Germany, for silicon donation, NXP, Eindhoven, The Netherlands, for wire-bonding, and G. Wienk and H. de Vries from the University of Twente, Enschede, The Netherlands, for their valuable CAD and measurement support.

REFERENCES

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