Time-Interleaved ADCs

Theory and Design

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Who am I?

- Received B.E. from A.U.B. in 2004
- Received Ph.D. from Stanford University in 2010
  - Thesis: "Background calibration of timing-skew in time-interleaved ADCs"
  - Ph.D. Advisor: Boris Murmann
  - Research interests: Integrated circuits, background calibration, low power design
- Currently working at Texas Instruments (Dallas, TX) on high-speed data converters

Tutorial objectives

- To understand the theory and operation of time-interleaved ADCs and how to design them
- At the end of this tutorial, you **will** have a toolbox to analyze time-interleaved ADCs with and a **starting point** from which to design one

Stop me whenever you have questions

A broad-stroke outline

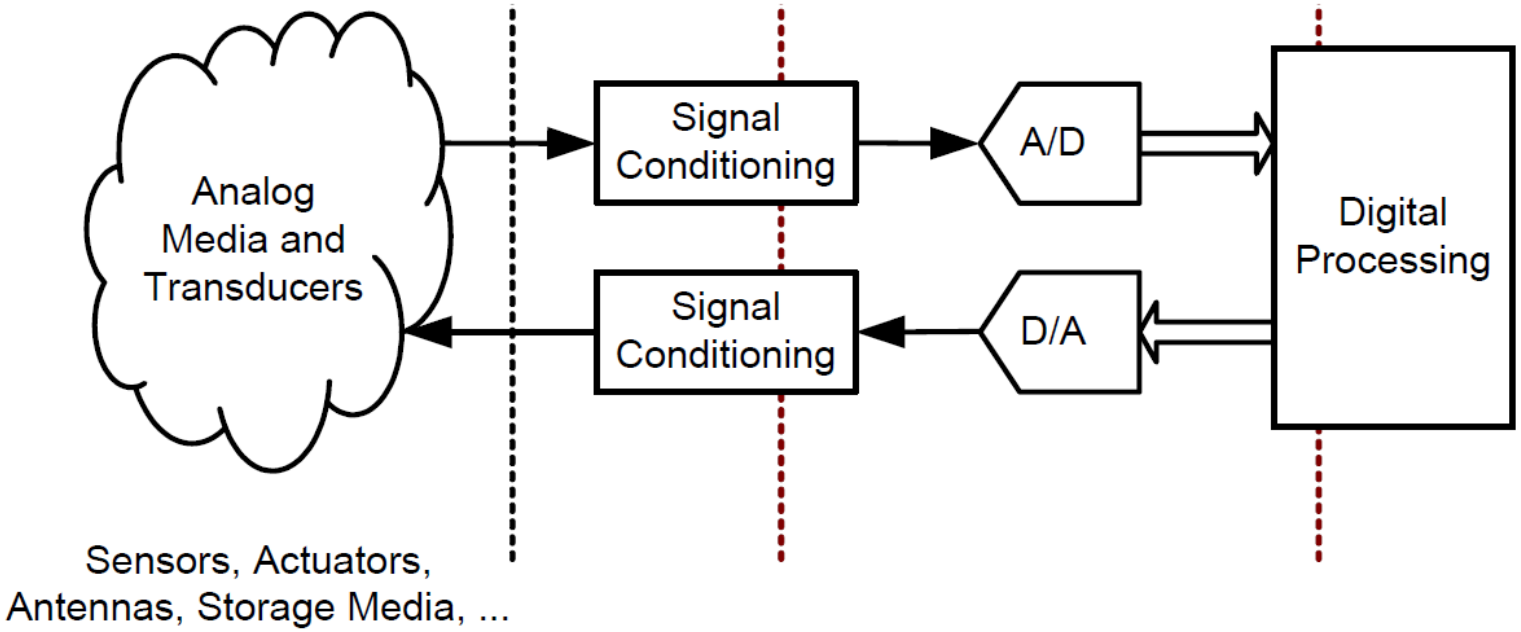
- Overview of data converters
- The time-interleaved ADC
- Quantitative analysis of time-varying errors
- Design of time-interleaved ADCs
- Calibration

Part I

Overview of Data Converters

Introduction

- Data converters important part of signal chain

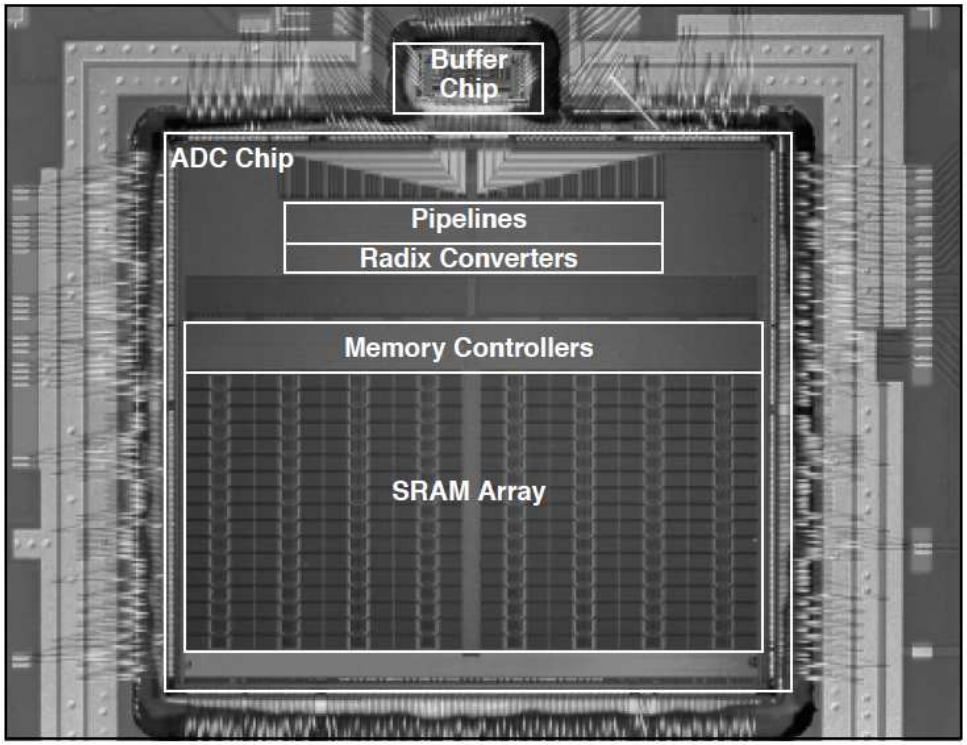


[Slide taken from B. Murmann notes]

Data converter applications

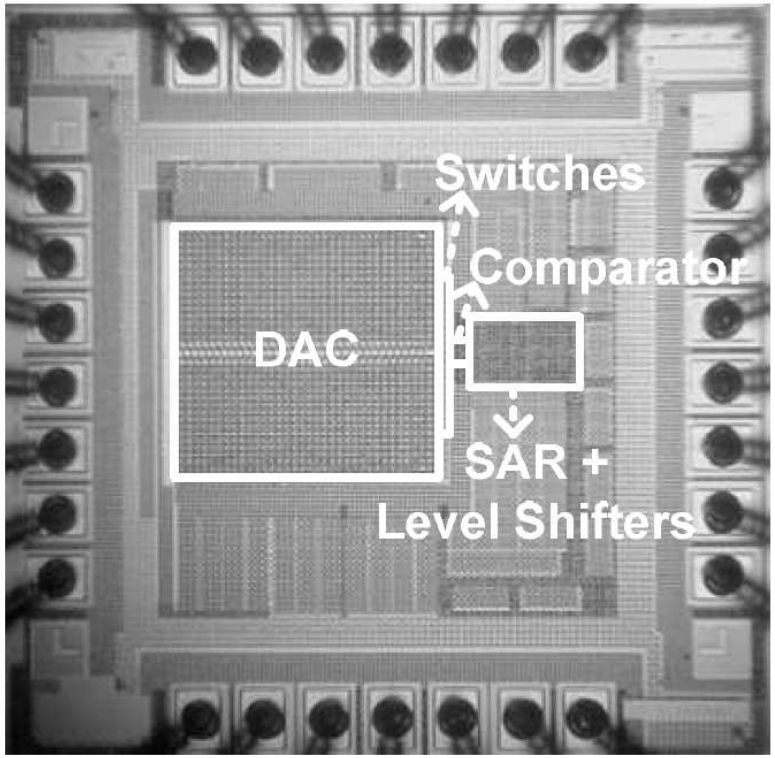
- Consumer electronics
  - Video and audio
  - Digital cameras
  - Automotive systems
- Communication systems
  - Wireless infrastructure
  - Ethernet
- Computing and control
  - Storage media
  - Feedback systems
- Instrumentation
  - Medical equipment
  - Oscilloscopes

Examples



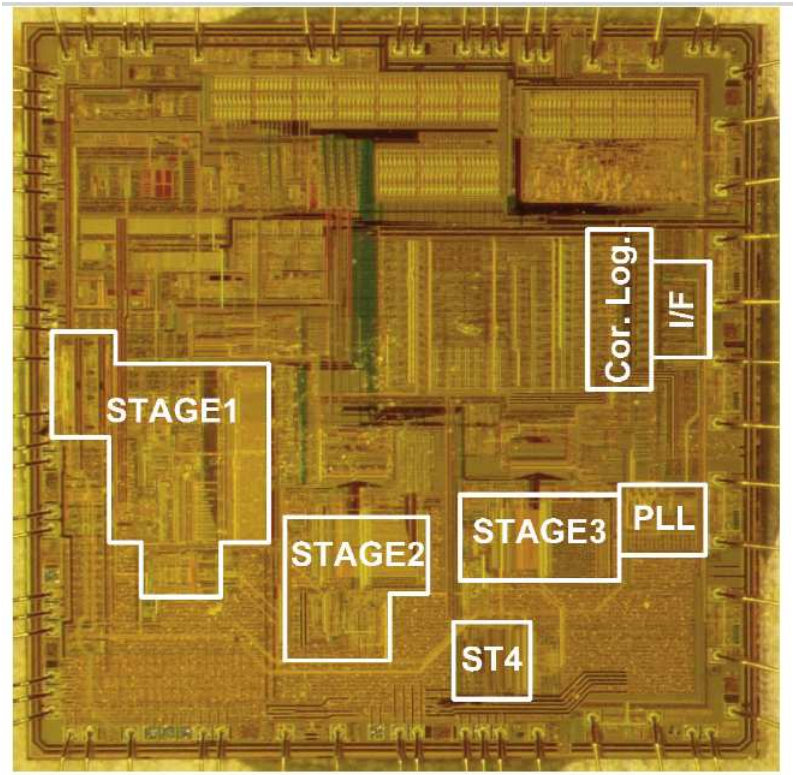
- Agilent oscilloscope
- Published in ISSCC 2003

Examples



- 1 kS/s ADC for medical implants
- Published in ESSCIRC 2010

Examples



- TI ADC used in wireless infrastructure
- Published in ISSCC 2010

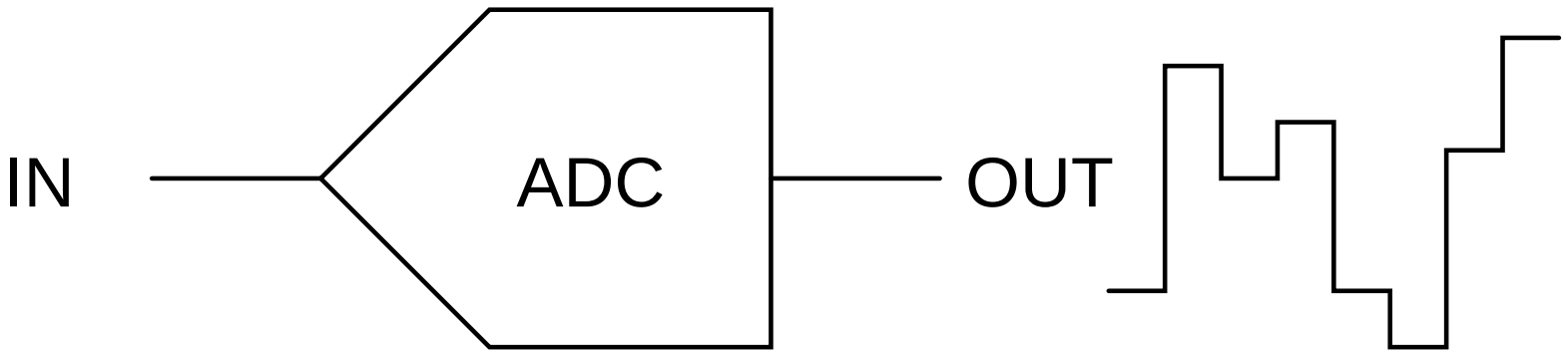
Reference books

- *Principles of Data Conversion System Design*, Behzad Razavi
- *Data Converters*, F. Maloberti
- *CMOS Data Converters for Communications*, Mikael Gustavsson et al.
- *Understanding Delta-Sigma Data Converters*, Richard Schreier et al.
- *Data Conversion Handbook*, Analog Devices Inc.

Analog-to-digital conversion

Definition

The conversion from a **continuous-time** signal to a **discrete-time** representation



Analog-to-digital conversion

Analog-to-digital conversion consists of two operations ...

- Sampling
- Quantization

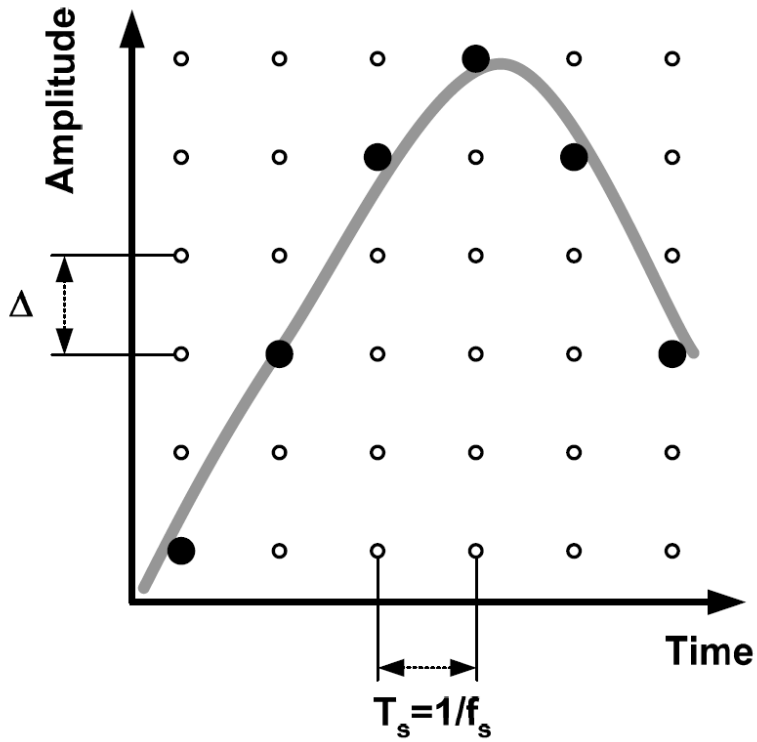
Sampling and quantization

- Sampling

  (Discretizing in time)

- Quantization

  (Discretizing in amplitude)



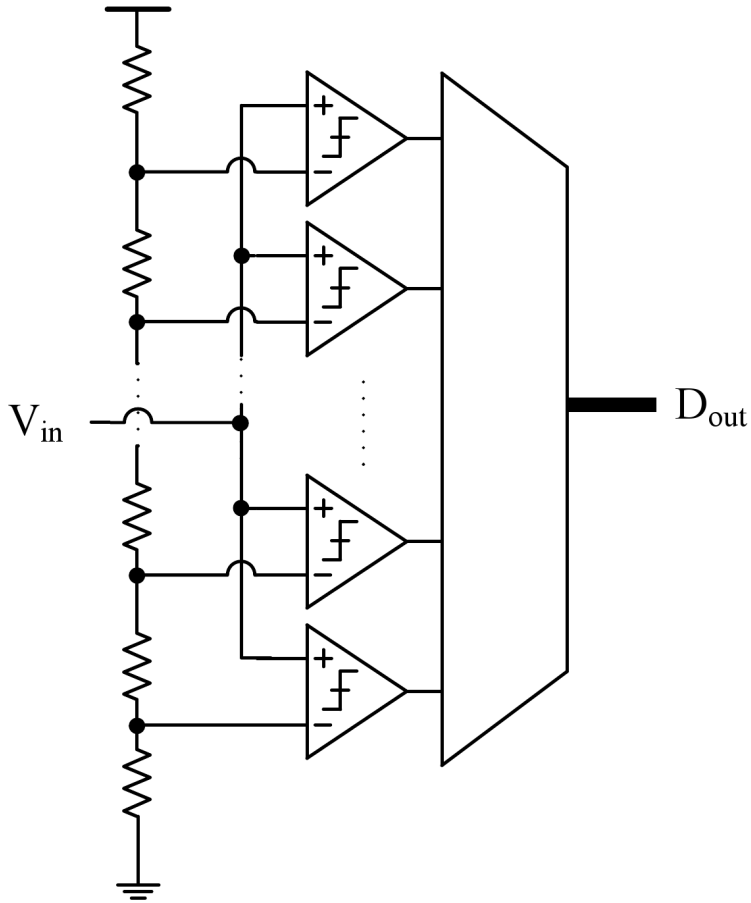
[Murmann notes]

Sampling and quantization

- Most common approach is to discretize **uniformly** in both time and amplitude
- These two concepts alone can fill an entire semester ...
- For more on these, see reference books

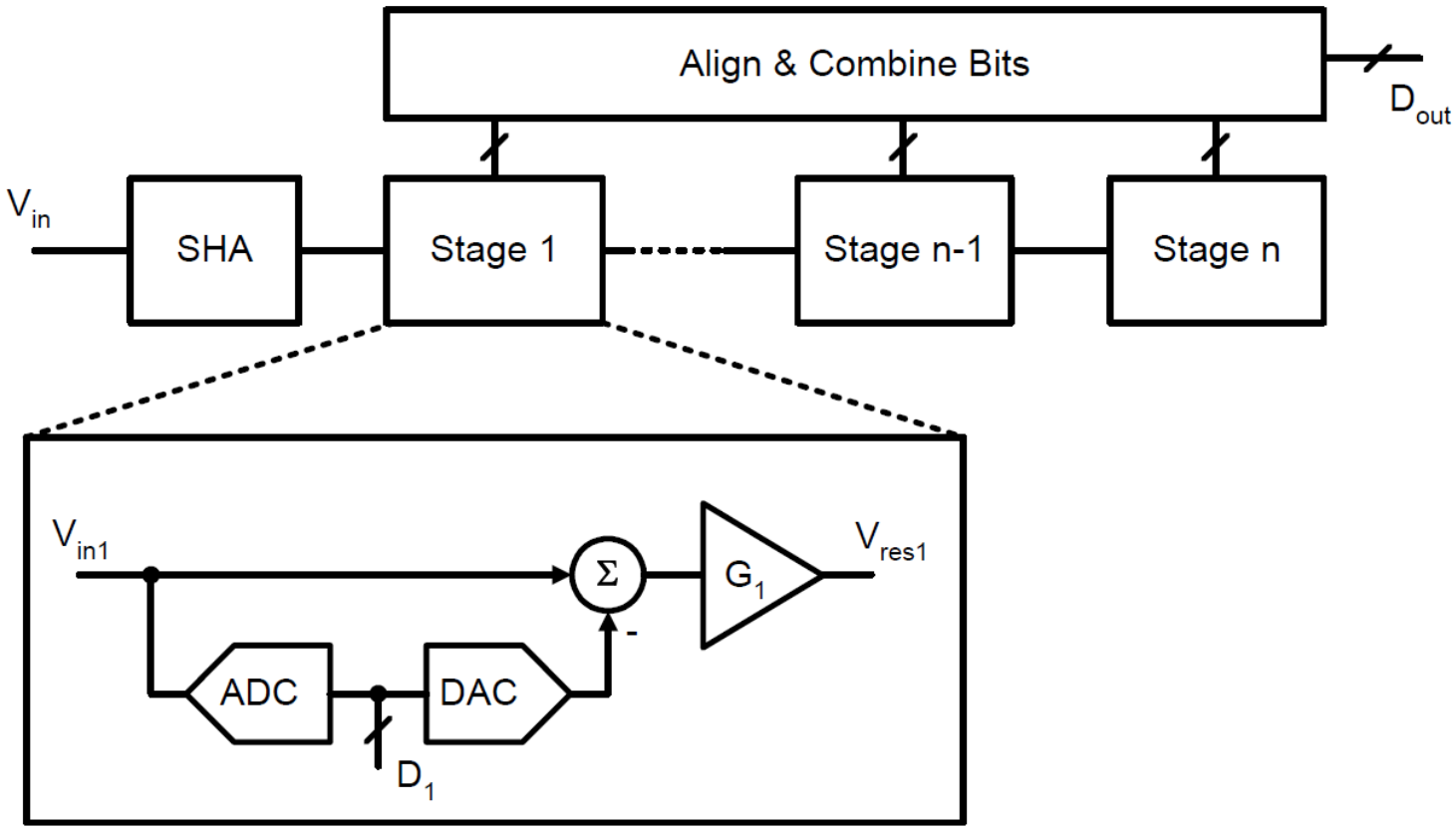
Types of ADCs: the flash ADC

- Flash ADC has $2^B - 1$ comparators
- Extremely fast with limited resolution



Types of ADCs: the pipeline ADC

- Pipeline ADCs have moderate speed and high resolution



[Image from B. Murmann notes]

Types of ADCs

- SAR
- Sigma-delta
- Algorithmic
- Single-slope
- Time-to-digital

- ... references previously mentioned discuss most of these

Part II

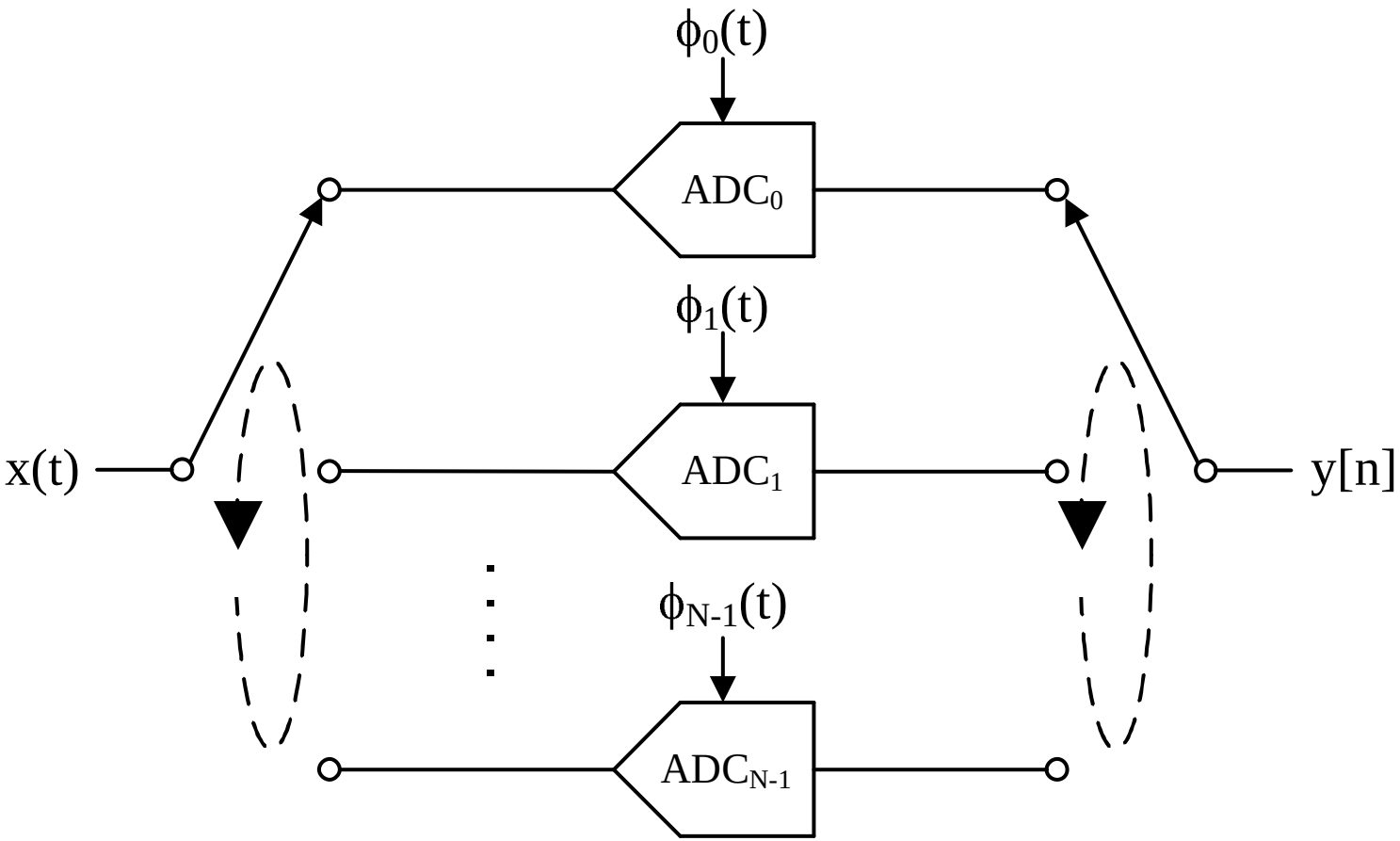
The Time-Interleaved ADC

Introduction to time-interleaved ADCs

Definition

An ADC that cycles through a set of N sub-ADCs, such that the aggregate sample-rate is N times the sample-rate of the individual sub-ADCs

Introduction to time-interleaved ADCs



- Sub-ADCs tend to be identical

Back in 1980 ...

- William Black, Ph.D. thesis "High Speed CMOS A/D conversion techniques"
- Published "Time-Interleaved Converter Arrays"

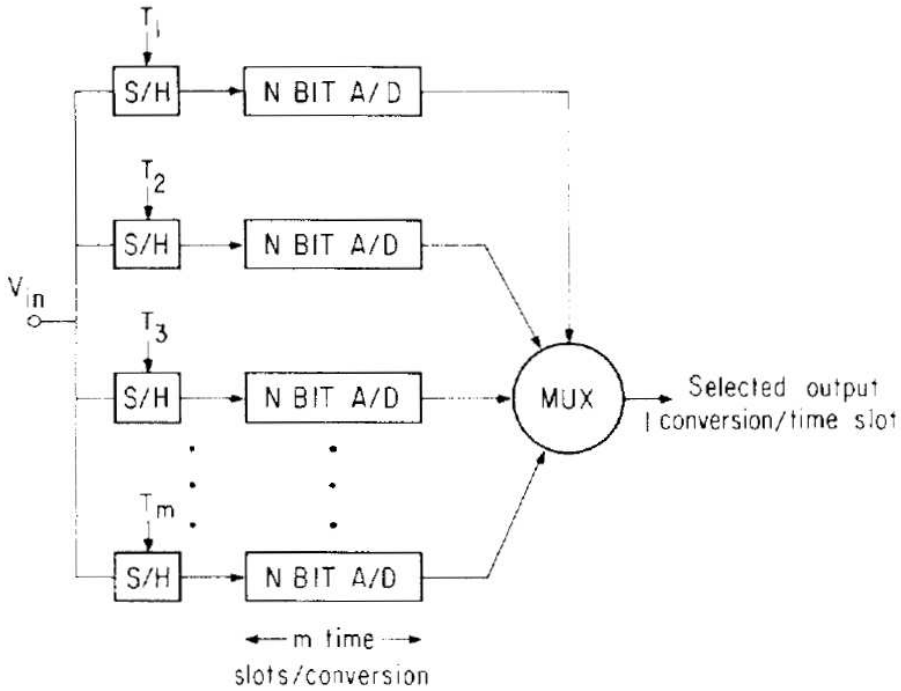


FIGURE 1—Converter array technique where a number of time-interleaved converters are used to achieve a fast effective sampling rate.

[Black 1980]

This "high speed" technique was for a **7-bit 2.5 MHz** ADC

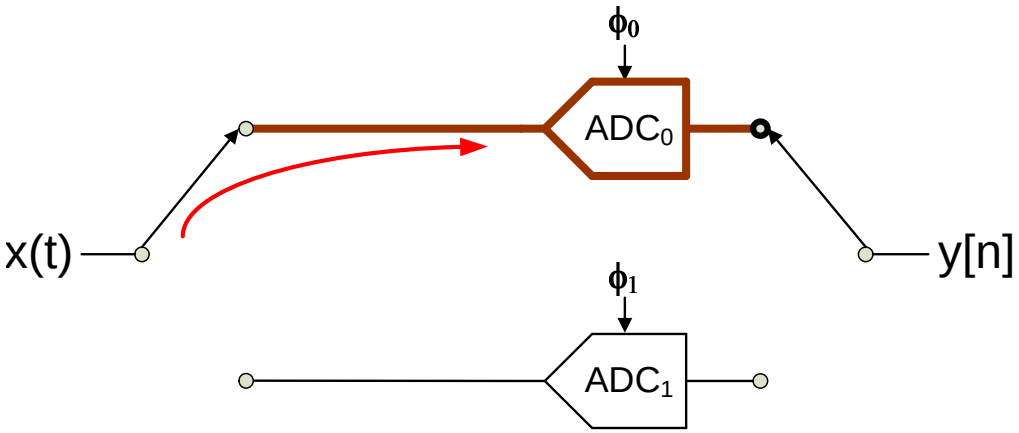
... 30 years later

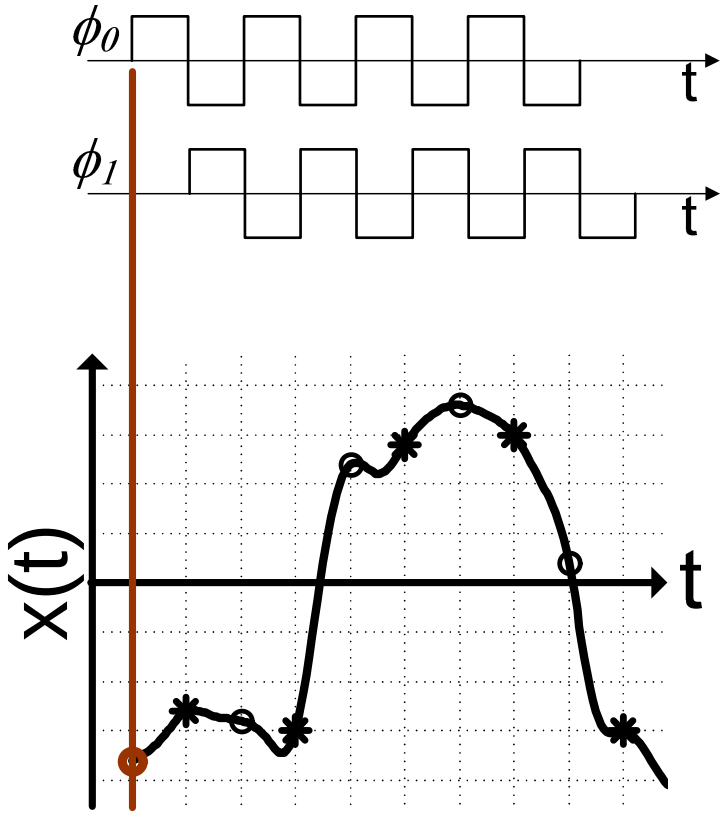
- Time-interleaved ADCs are still a serious research area
- Multi-GHZ ADCs are the **norm**
  - Agilent, 2003: 80-way interleaved 20 GS/s
  - Fujitsu, 2009: 4-way interleaved 56 GS/s
  - Nortel, 2010: 16-way interleaved 40 GS/s

How exactly does it work?

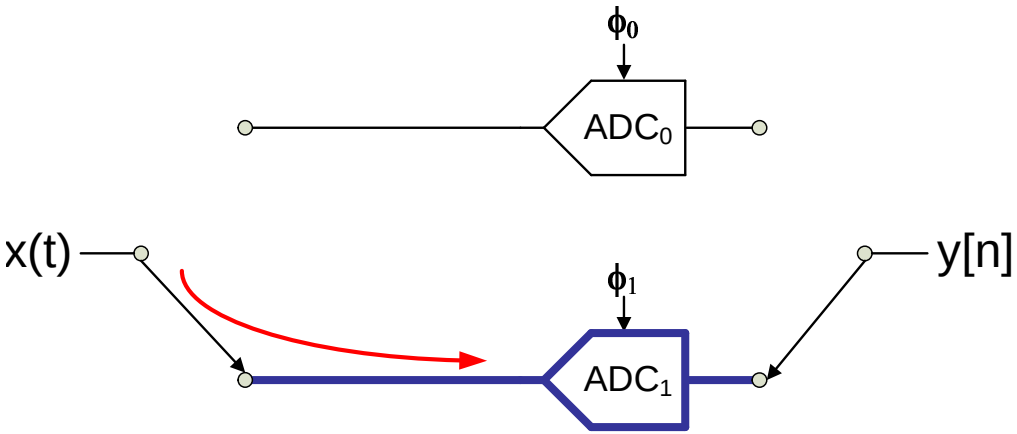
- Intuitive in the time-domain

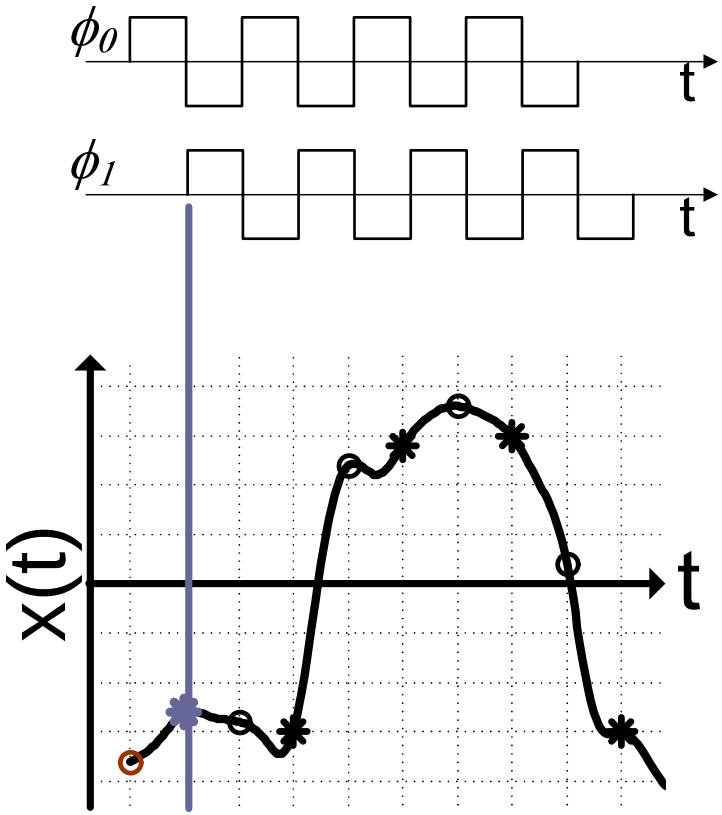
First ADC samples the signal ...



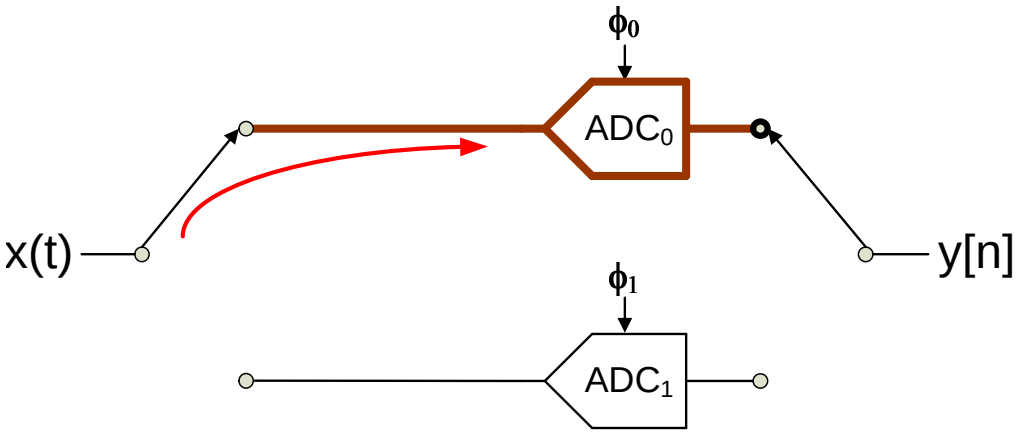


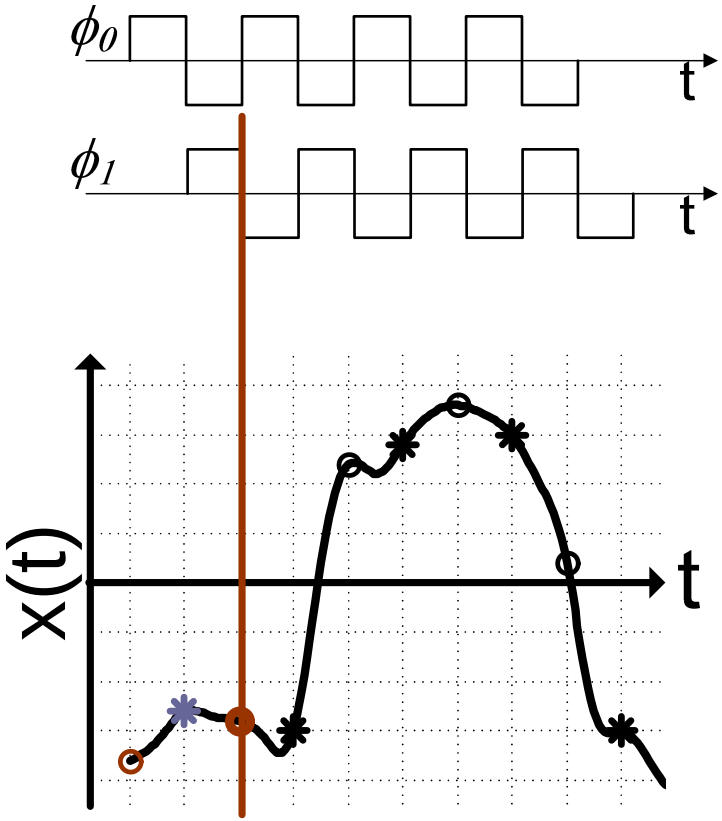
Second ADC samples the signal ...





And again, first ADC samples the signal ...





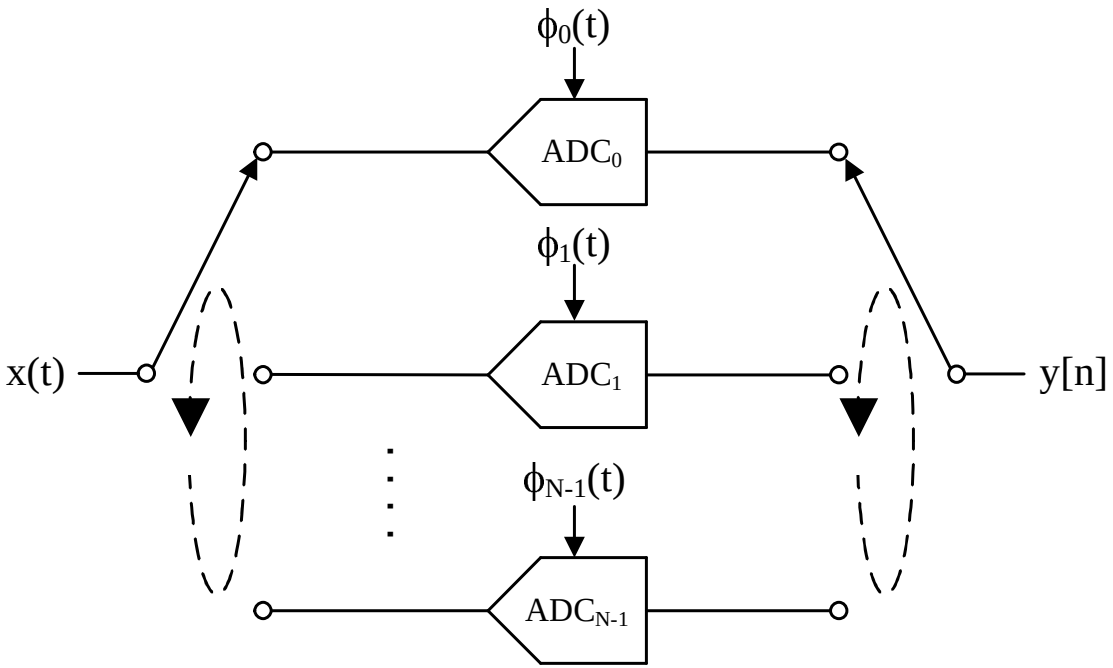
Time-domain analysis

- Each sub-ADC output is (ignoring quantization)

$$y_i[n] = x\left((nN + i)\,T_s\right) \tag{1}$$

- where T_s is sampling period, N is interleaving factor, and $i = 0, ..., N-1$

Time-domain analysis



- Output multiplexer combines these streams such that

$$y[n] = y_i\left[\frac{n-i}{N}\right] \text{ where } i = n \bmod N \tag{2}$$

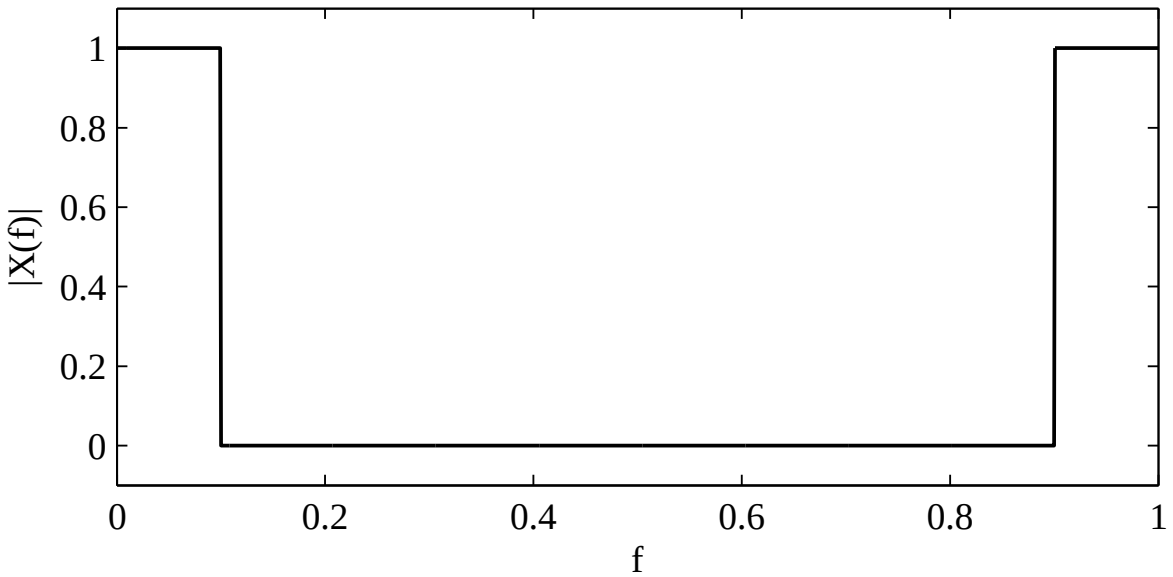
Frequency-domain analysis

- This is less intuitive ...
- Can take the discrete-time Fourier transform (DTFT) of the (upsampled) sub-ADC outputs and the time-interleaved ADC output
- In theory, ...

$$Y(f) = \sum_{i=0}^{N-1} Y_i(f) \tag{3}$$

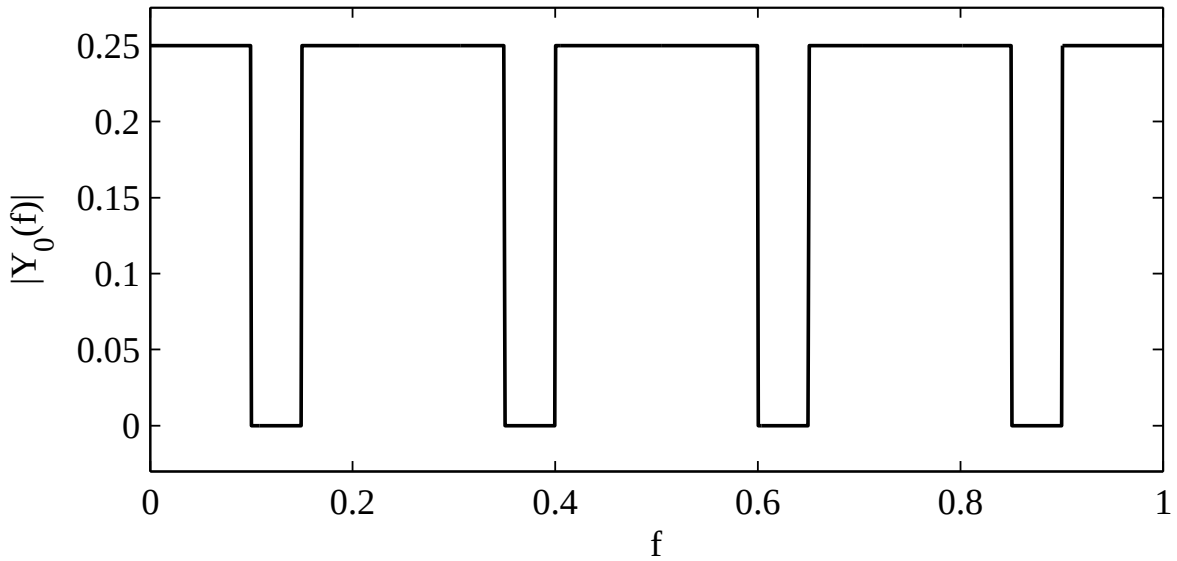
Frequency-domain analysis

- Assume you have an input signal with the following DTFT



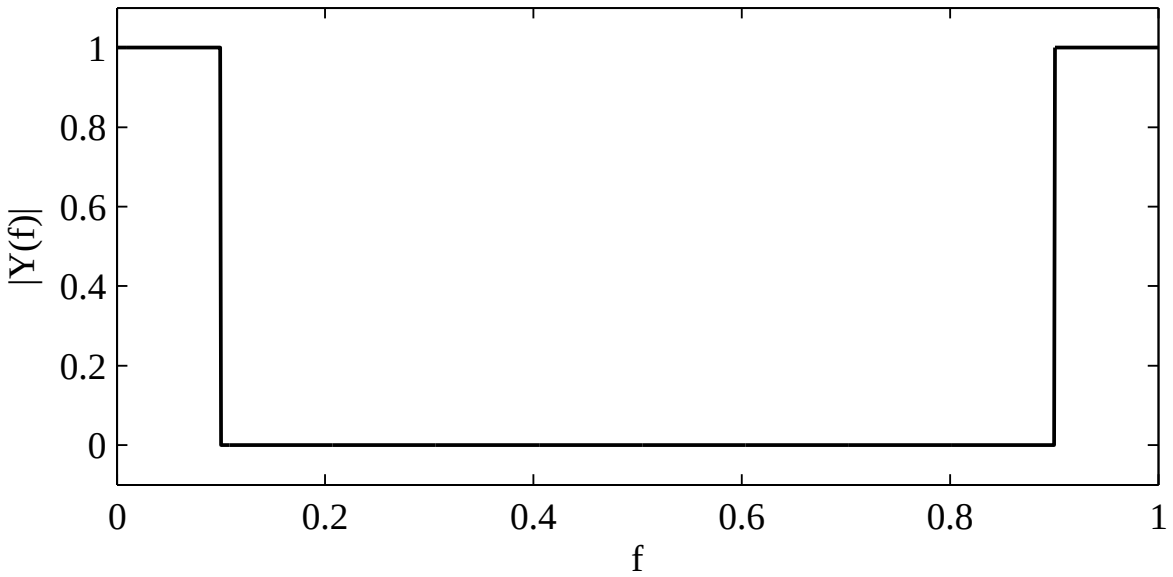
Frequency-domain analysis

- The resulting (upsampled) sub-ADC output DTFT will be



Frequency-domain analysis

- Replicas have different phases for each of the sub-ADCs
- When summed, the phases cancel each other out
- You **will** get the same spectrum as the input



Time-varying errors

In theory, theory and practice are the same.

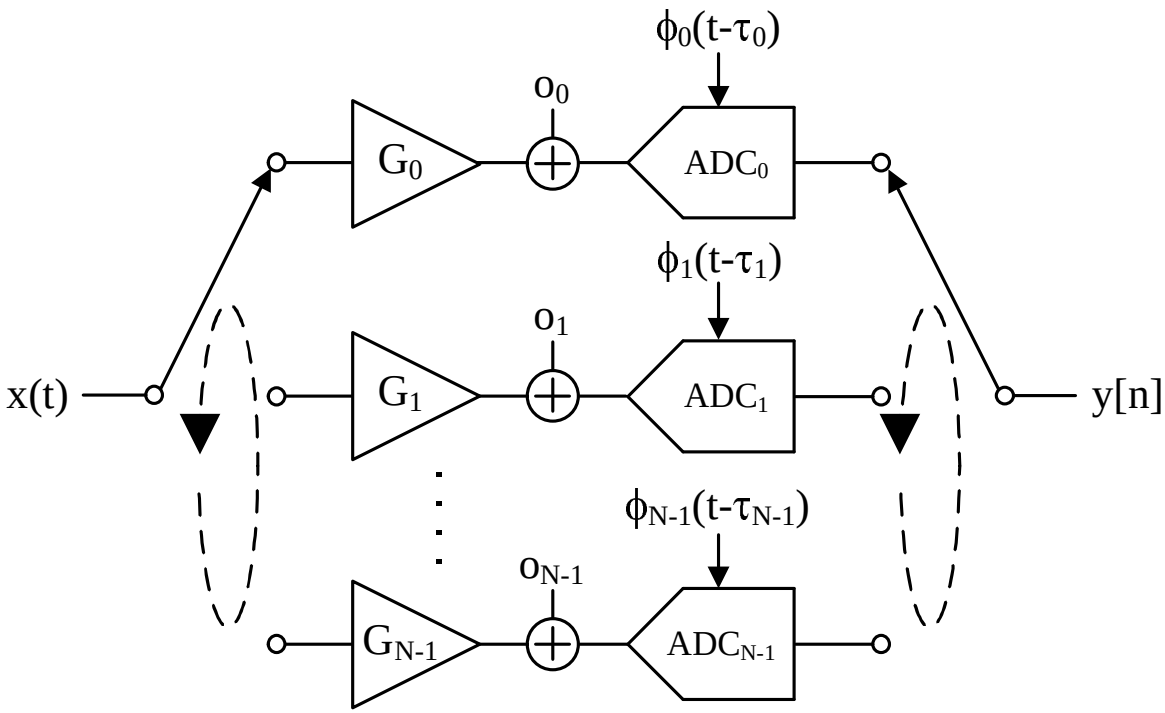
In practice, they are not.

Time-varying errors

- Ideally, a time-interleaved ADC can be blackboxed into a single monolithic ADC

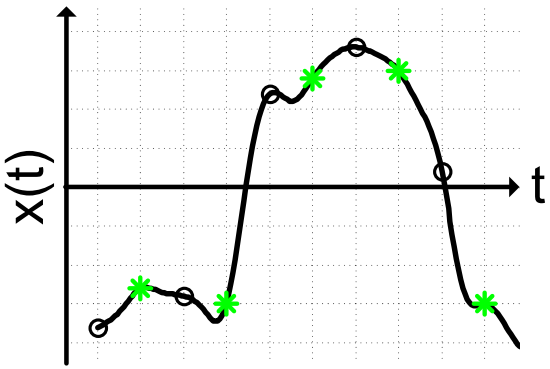
Time-varying errors

- Offset
- Gain
- Timing skew
- (Bandwidth)

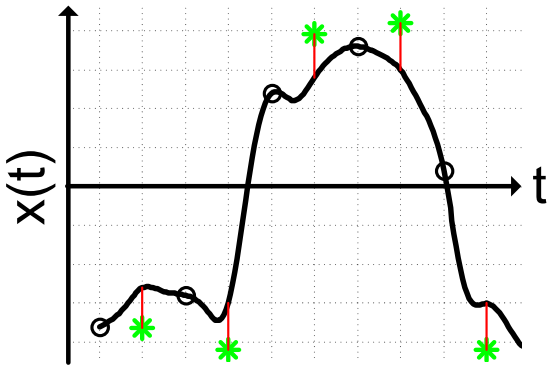


Time-varying errors

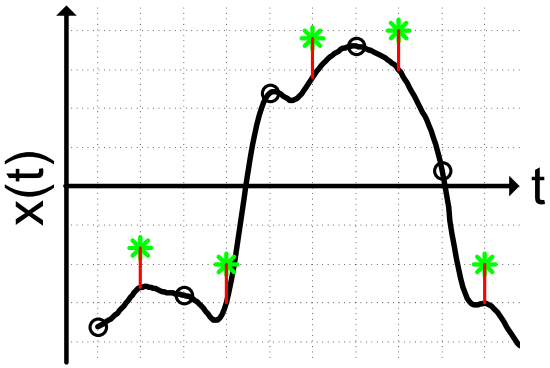
Ideal



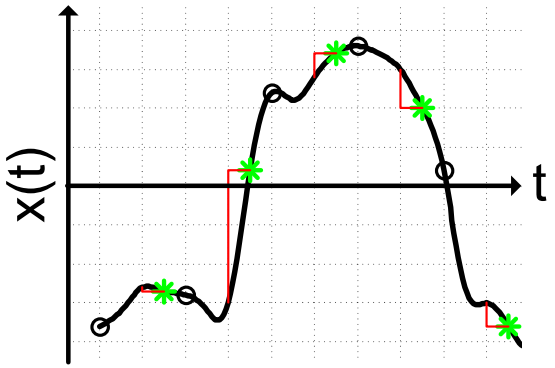
Gain



Offset



Timing Skew



Sources of errors

- PVT (Process, voltage, temperature) variations
- Current flow, layout nonidealities, mismatch in stray capacitance, etc.

All of these will limit your ADC performance

Offset mismatch

- Each sub-ADC **ideally** digitizes $x(t)$

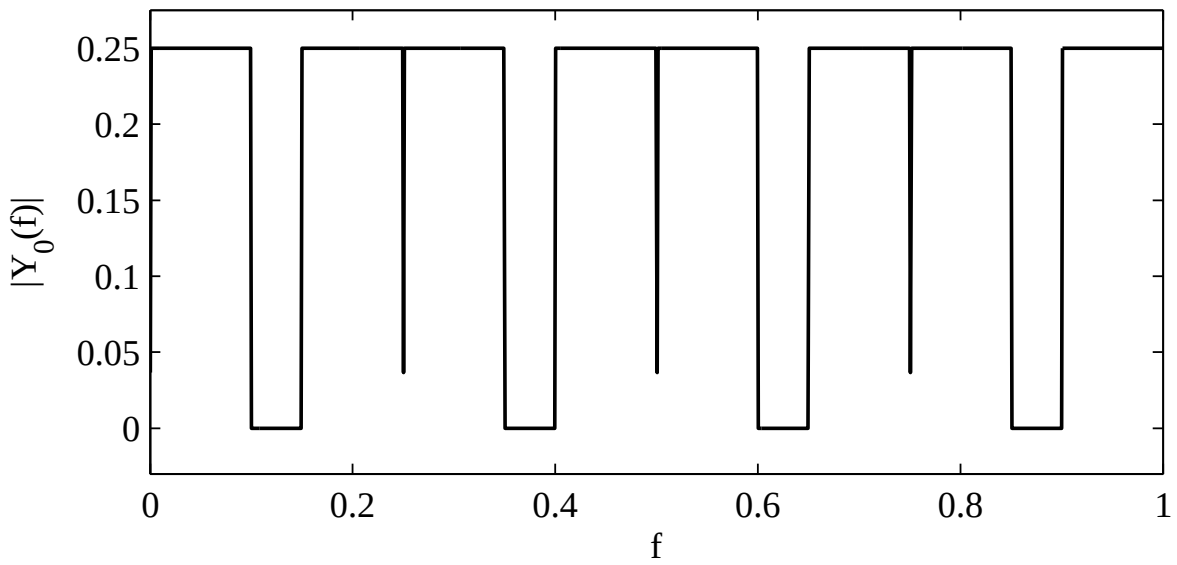
$$y_i[n] = x\left((nN + i)\,T_s\right) \tag{4}$$

- Each sub-ADC **actually** digitizes $x(t) + o_i$

$$y_i[n] = x\left((nN + i)\,T_s\right) + o_i \tag{5}$$

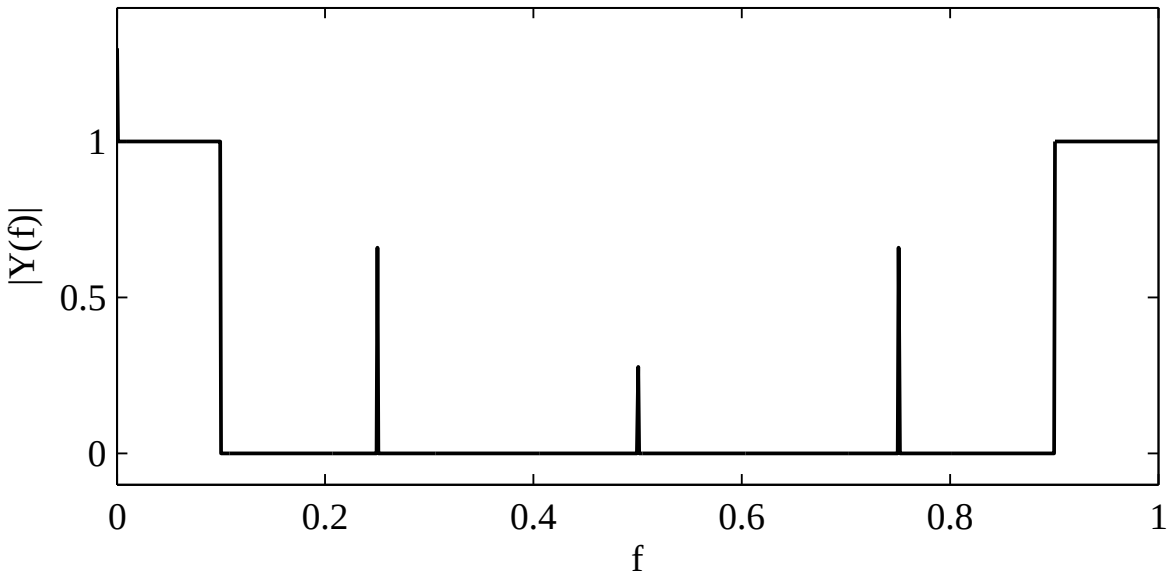
- o_i is different for each sub-ADC

Frequency-domain effects



- The DTFT of the sub-ADC changes because of these offsets

Frequency-domain effects



- The DTFT of the ADC has spurs at frequencies $i \cdot f_s/N$

Gain mismatch

- Each sub-ADC **ideally** digitizes $x(t)$

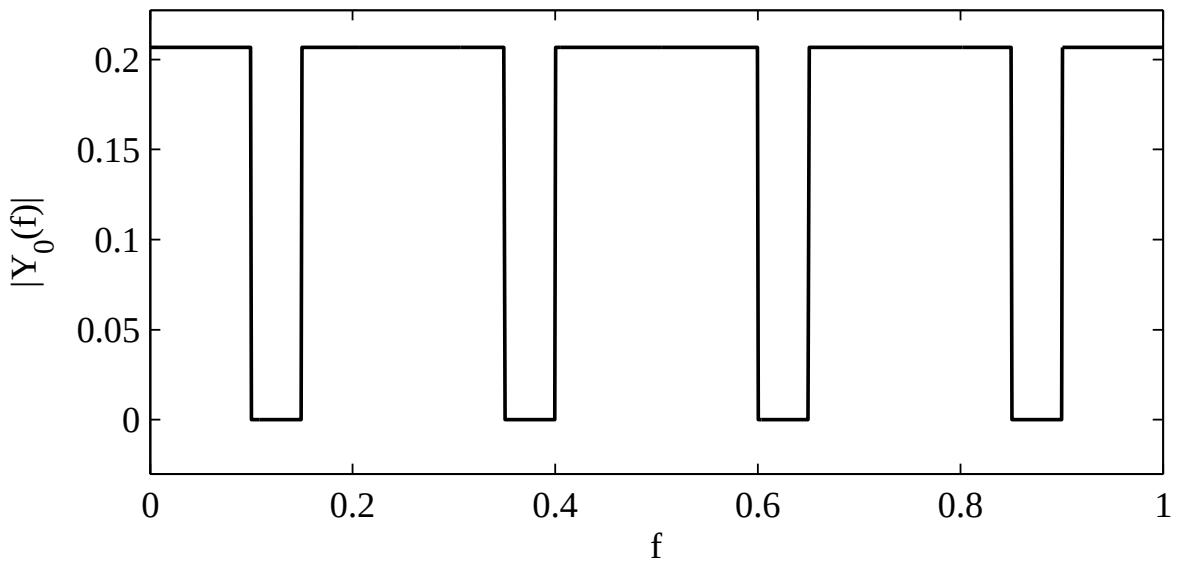
$$y_i[n] = x\left((nN + i)T_s\right) \tag{6}$$

- Each sub-ADC **actually** digitizes $G_i x(t)$

$$y_i[n] = G_i x\left((nN + i)T_s\right) \tag{7}$$

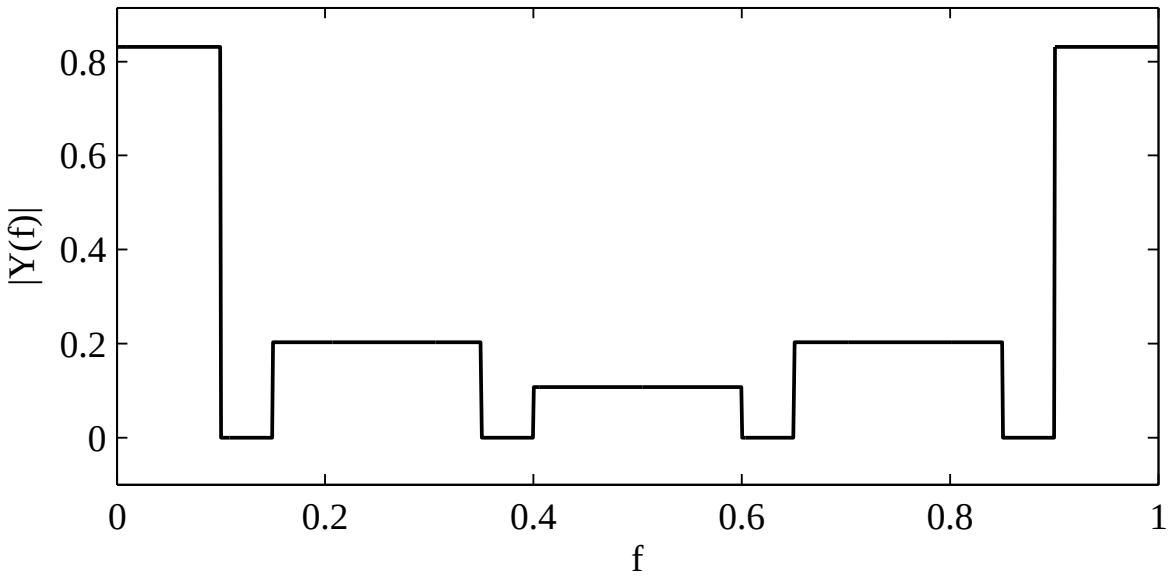
- G_i is different for each sub-ADC

Frequency-domain effects



- The DTFT of the sub-ADC changes because of these gain differences

Frequency-domain effects



- The DTFT of the ADC has replicas at frequencies $f_{in} - i \cdot f_s/N$

Timing skew

- Each sub-ADC **ideally** digitizes $x(t)$

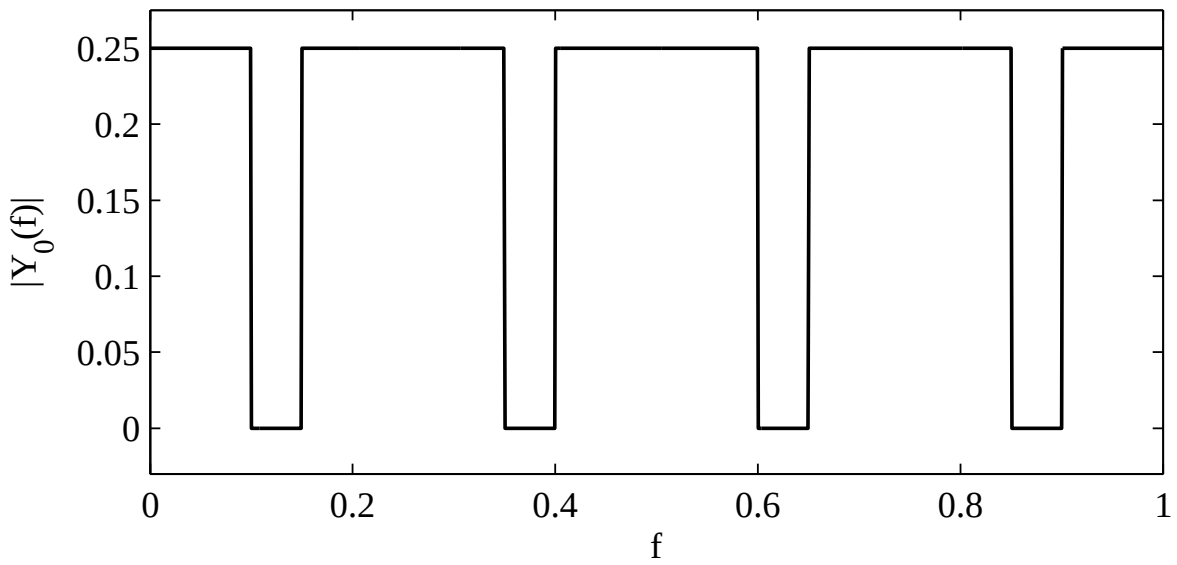
$$y_i[n] = x\left((nN + i)\,T_s\right) \tag{8}$$

- Each sub-ADC **actually** digitizes $x(t - \tau_i)$

$$y_i[n] = x\left((nN + i)\,T_s - \tau_i\right) \tag{9}$$

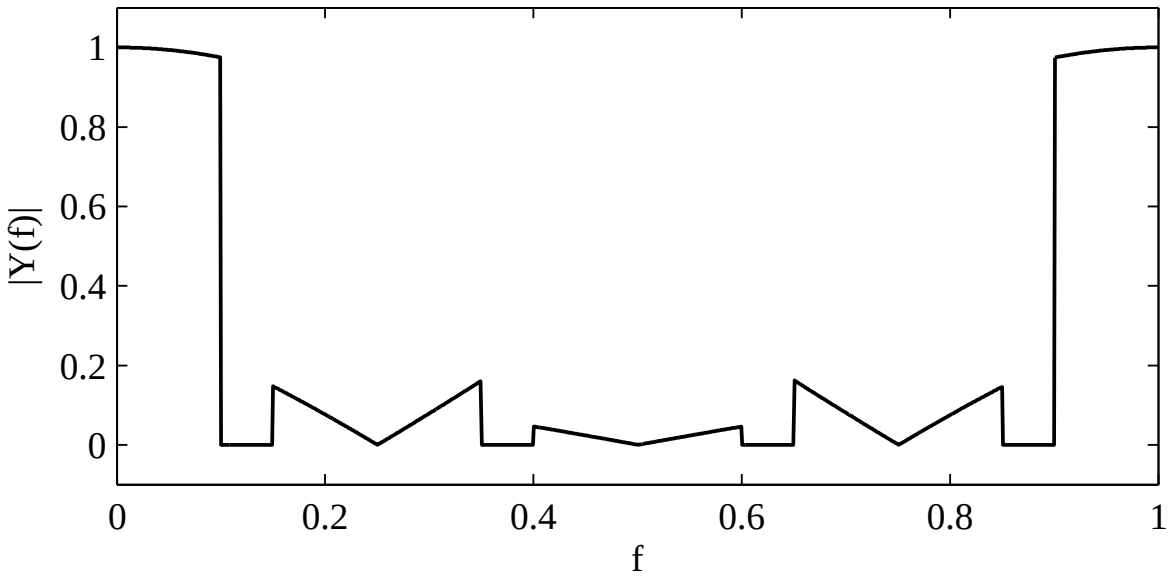
- τ_i is different for each sub-ADC

Frequency-domain effects



- The DTFT of the sub-ADC changes because of timing skew

Frequency-domain effects



- The DTFT of the ADC has replicas at frequencies $f_{in} - i \cdot f_s/N$

Some notes

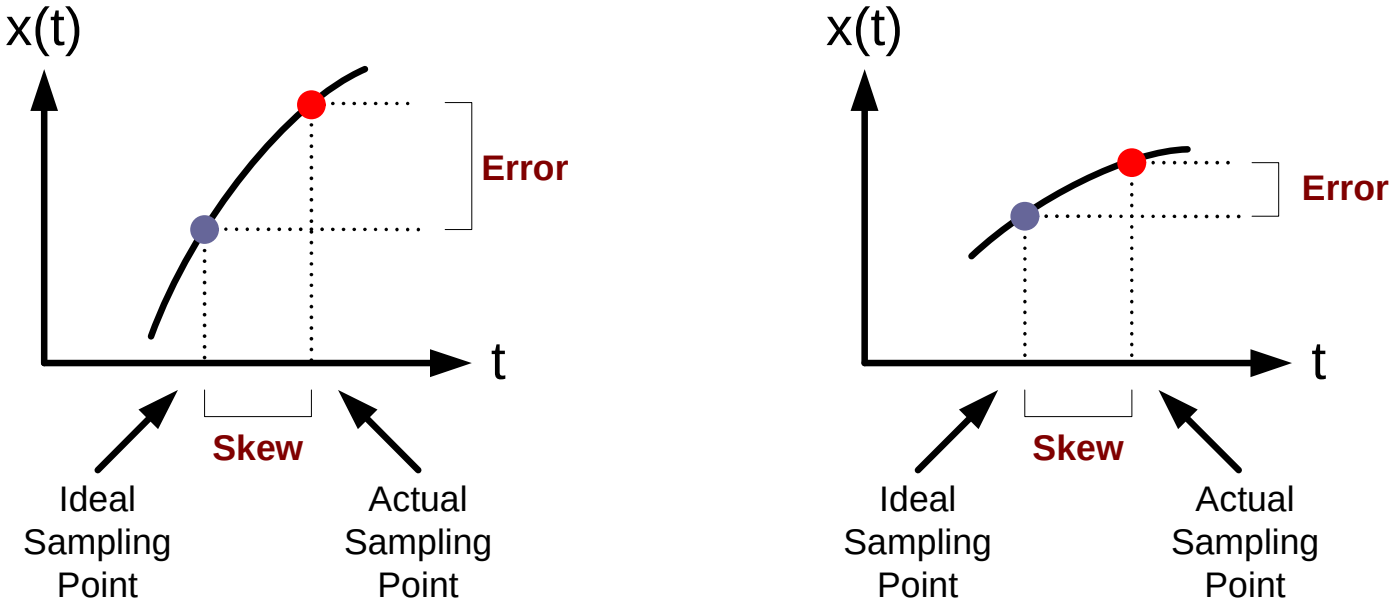
- Gain and offset mismatch are "static" errors
- Impact independent of input frequency

- But ... what if gain is a function of frequency? **(which it is)**
- And ... what if the gain transfer function varies? **(which it will)**

- You have bandwidth mismatch ...

Some notes ... continued

- Timing skew is not a "static" error



"Fast" signals suffer more sampling error due to timing skew than "slow" signals

Why is timing skew such a problem?

- ADCs are **generally** uniform sampling systems
- What if two consecutive samples aren't at times nT_s and $(n+1)T_s$?
  - If the deviation is random, you have jitter
  - If the deviation is deterministically time-varying because you are interleaving, you have timing skew
  - Timing skew becomes jitter as $N \to \infty$

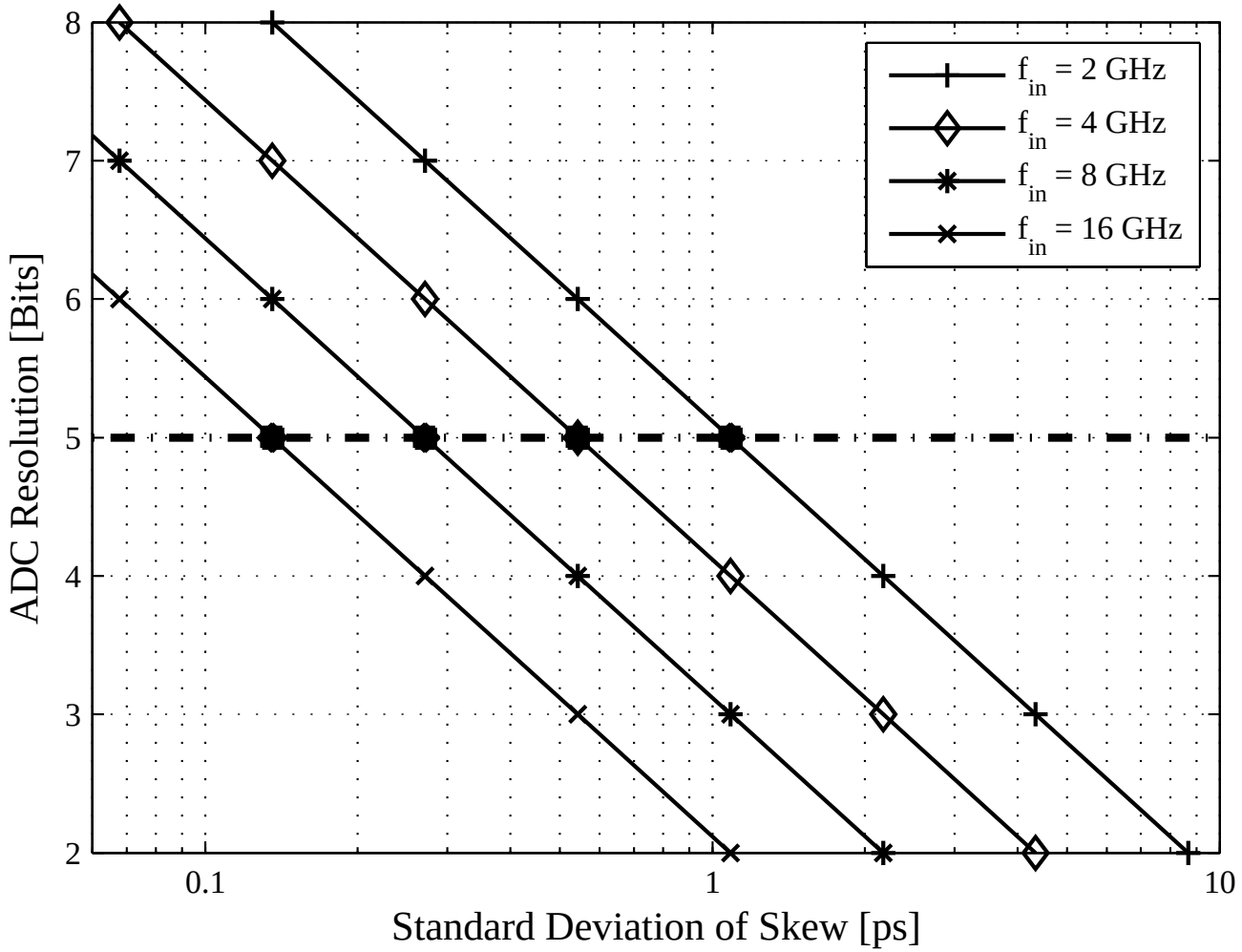
How much of a problem is timing skew?

- Interleave N B-bit sub-ADCs
- Input signal is sinusoid with frequency f_{in}

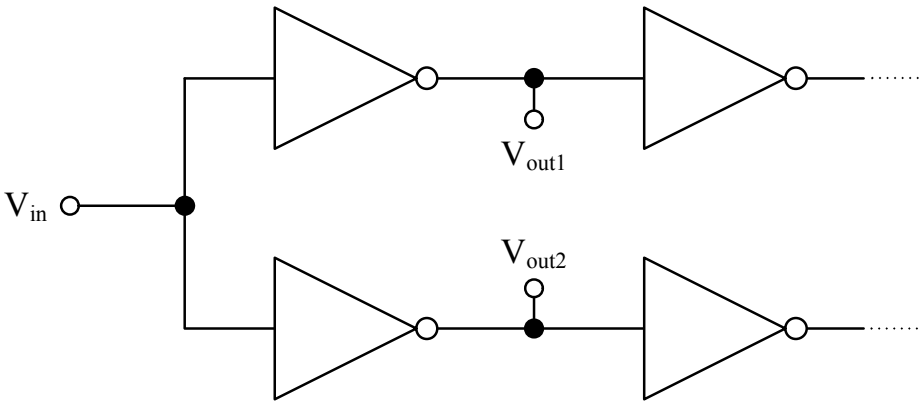
$$\sigma_\tau = \sqrt{\left(\frac{N}{N-1}\right) \cdot \left(\frac{1}{2^{2B}}\right) \cdot \left(\frac{2}{3(2\pi f_{in})^2}\right)} \tag{10}$$

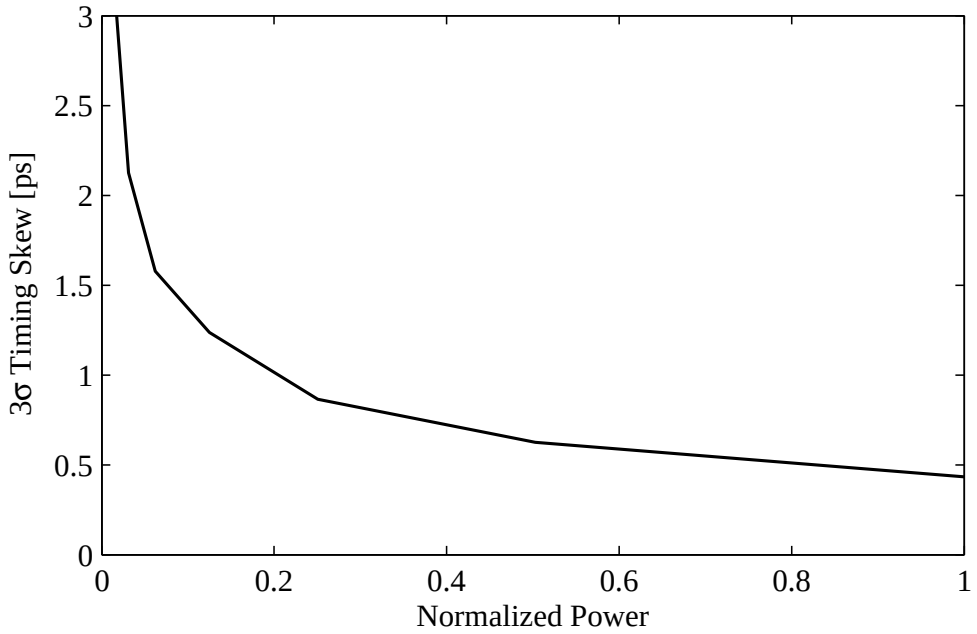
[Jenq 1988]

How much of a problem is timing skew?



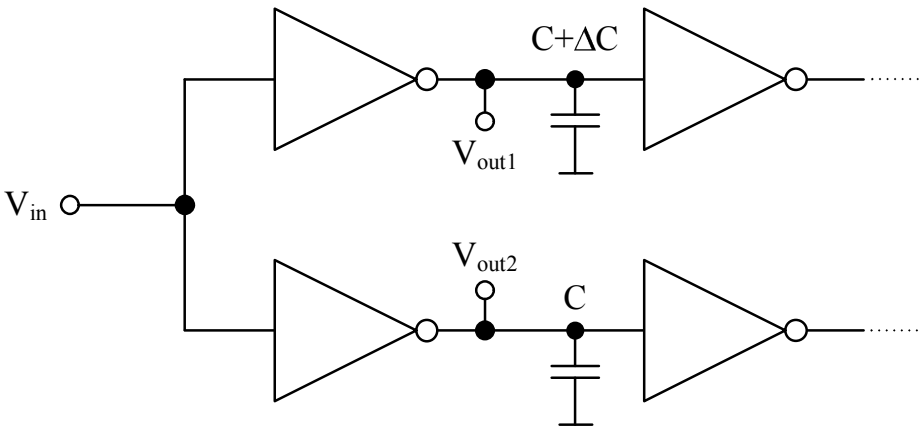
Sources of timing skew

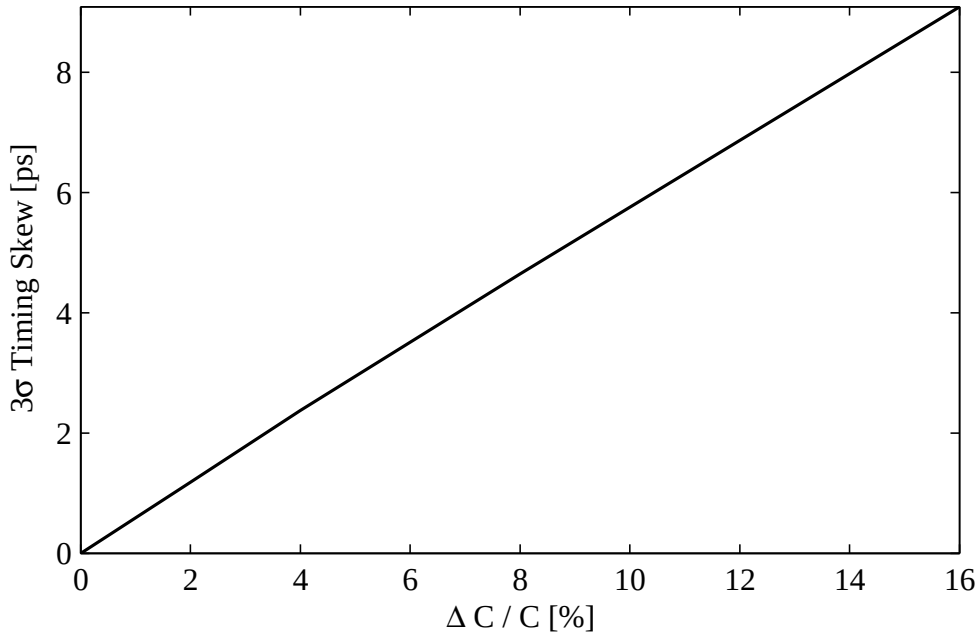




- Threshold mismatch causes delay change
- Rule: Halve deviation with four-fold increase in power (Pelgrom's equation)

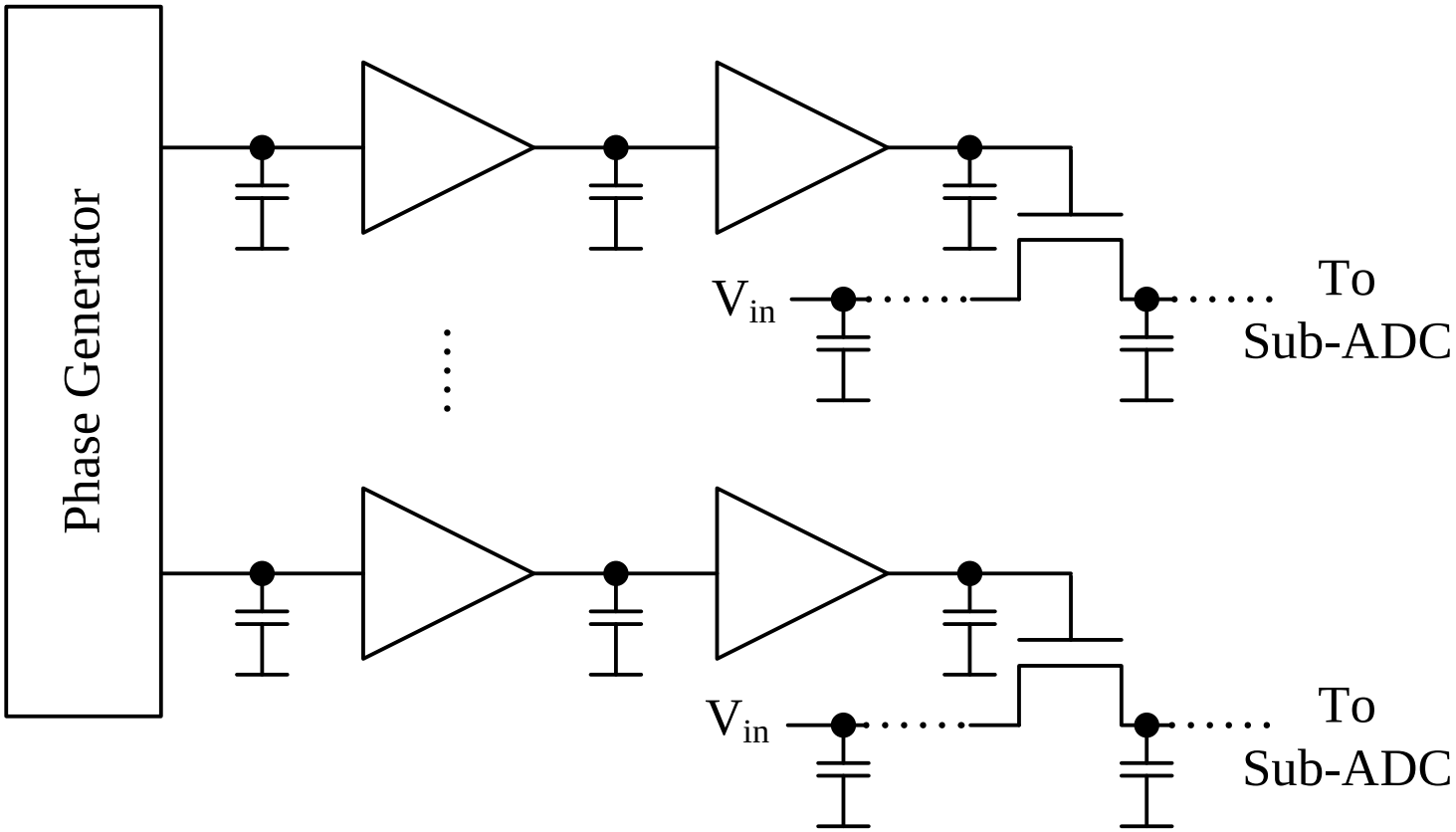
Sources of timing skew





- Trace *RC* differences cause delay change

Sources of timing skew



- Can easily have over 10 ps skew [Agrawal 2008]

Part III

Quantitative Analysis of Time-Varying Errors

Errors exist. What can we do?

- **Step 1**: Quantify error you can tolerate
- **Step 2**: Define your design space

The sinusoidal approach

- Most ADC simulated with a sine wave input
- Allows you to define dynamic performance metrics
  - Fundamental tone and harmonics
  - SFDR: Spurious free dynamic range
  - SNR: Signal to noise ratio
  - SNDR: Signal to noise and distortion ratio
- Can do the same for time-varying errors

Bounds on time-varying errors (part 1)

- Bound on offset

$$\sigma_o = \sqrt{\left(\frac{N}{N-1}\right) \cdot \left(\frac{A^2}{3 \cdot 2^{2B}}\right)} \tag{11}$$

- Bound on gain

$$\sigma_g = \sqrt{\left(\frac{N}{N-1}\right) \cdot \left(\frac{2}{3 \cdot 2^{2B}}\right)} \tag{12}$$

- Bound on timing skew

$$\sigma_\tau = \sqrt{\left(\frac{N}{N-1}\right) \cdot \left(\frac{2}{3 \cdot 2^{2B} \cdot (2\pi f_{in})^2}\right)} \tag{13}$$

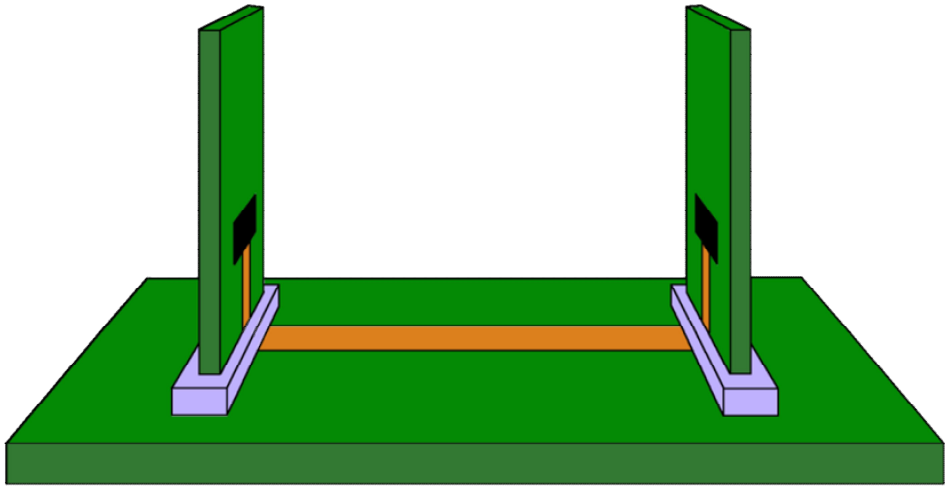
[Jamal 2001]

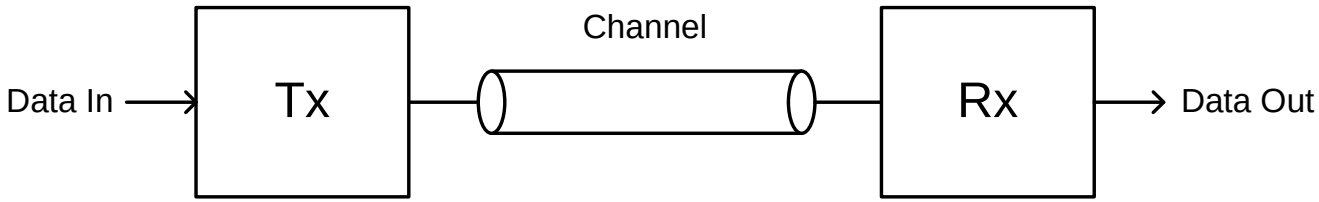
Examples

- 5-bit ADC with input amplitude $A = 1$ and $N = 2$
  - $\sigma_o = 25$ mV
  - $\sigma_g = 3.6$ %
  - $\sigma_\tau = \frac{1}{175 \cdot f_{in}}$ (e.g. $f_{in} = 100$ MHz, $\sigma_\tau \approx 57$ ps)
- 12-bit ADC with input amplitude $A = 1$ and $N = 2$
  - $\sigma_o = 0.2$ mV
  - $\sigma_g = 0.028$ %
  - $\sigma_\tau = \frac{1}{22{,}000 \cdot f_{in}}$ (e.g. $f_{in} = 100$ MHz, $\sigma_\tau \approx 0.5$ ps)

Bounds on time-varying errors (part 2)

- In real-world applications, ADCs don't sample sine waves
- Many systems are broadband





Using a sine wave at Nyquist will **overdesign** your system

Cost of overdesign

- More chip area
- More power
- Longer design cycle

- More $$$

- Use minimum-mean square error to derive more realistic bounds

"Best-fit" approach

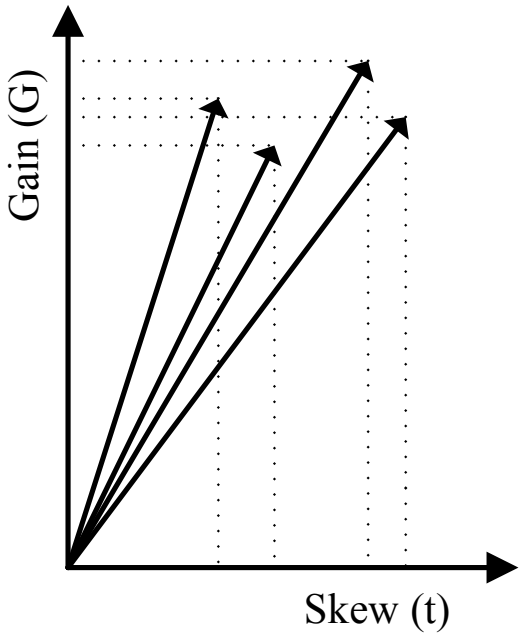
$$y[n] = x_o[n] + e[n] \tag{14}$$

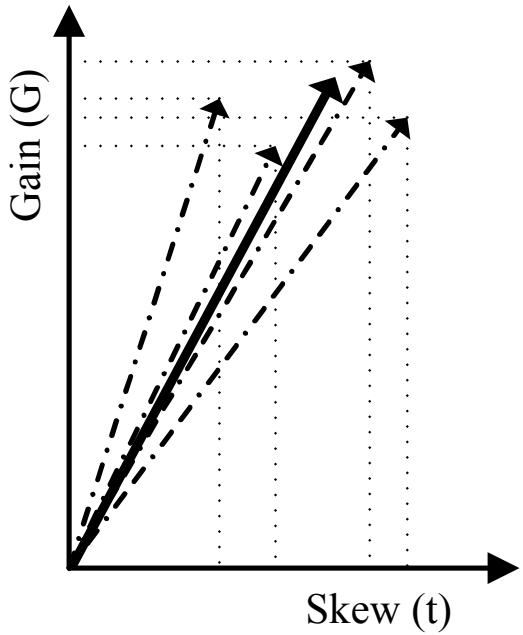
- $x_o[n]$ is the "best-fit"

$$x_o[n] = \hat{G}x\left(nT_s - \hat{\tau}\right) \tag{15}$$

- Nontrivial to solve in the general sense
- Solvable for WSS and WSCS signals [El-Chammas 2009]

Intuition





Find vector that minimizes distance to sub-ADC vectors

Wide-sense stationary

Definition

A signal is wide-sense stationary (WSS) if its mean and autocorrelation are not a function of time

$$m(t_1) = m(t_2) = m \tag{16}$$

$$R(t_1, t_1 + \tau) = R(t_2, t_2 + \tau) = R(\tau) \tag{17}$$

Calculate the MSE

$$f(\hat{G}, \hat{\tau}) = E\left[e[n]^2\right] - E\left[e[n]\right]^2 \tag{18}$$

Remember:

$$e[n] = y[n] - x_o[n] \tag{19}$$

Calculate the MSE

$$f(\hat{G},\hat{\tau}) = \left(\hat{G}^2 P + \frac{P}{N}\sum_{i=0}^{N-1} G_i^2 - 2\frac{\hat{G}}{N}\sum_{i=0}^{N-1} G_i R(\tau_i - \hat{\tau}) + \frac{1}{N}\sum_{i=0}^{N-1} o_i^2\right) - \frac{1}{N^2}\left(\sum_{i=0}^{N-1} o_i\right)^2 \quad (20)$$

(work your "write" arm muscles and derive this)

Calculate the "best-fit" parameters

$$\boxed{\text{Minimize } f(\hat{G}, \hat{\tau})}$$

- Differentiate with respect to $\hat{G}$ and $\hat{\tau}$ and set to zero

$$\hat{G} = \frac{1}{NP} \sum_{i=0}^{N-1} G_i R(\hat{\tau} - \tau_i) \tag{21}$$

$$\hat{\tau} = \arg\max_{\tau} \sum_{i=0}^{N-1} G_i R(\tau - \tau_i) \tag{22}$$

Mismatch or quantization limited?

$$SNR_f = \frac{P}{f(\hat{G}, \hat{\tau})} \gtrless \frac{3}{2} \cdot 2^{2B} = SNR_Q \tag{23}$$

$$f(\hat{G}, \hat{\tau}) \lessgtr \frac{2 \cdot P}{3 \cdot 2^{2B}} \tag{24}$$

Effect of timing skew

- Impact on timing skew **is** different than previously shown
- Assume $o_i = 0$ and $G_i = 1$

$$\frac{1}{P}\sum_{i=0}^{N-1} R(\hat{\tau} - \tau_i) \geq N\sqrt{\frac{SNR_Q - 1}{SNR_Q}} \tag{25}$$

- Let's make one more assumption: the autocorrelation is second order differentiable

$$R(\tau) \approx R(0) + \cancel{R'(0)\tau} + \frac{R''(0)}{2}\tau^2 \tag{26}$$

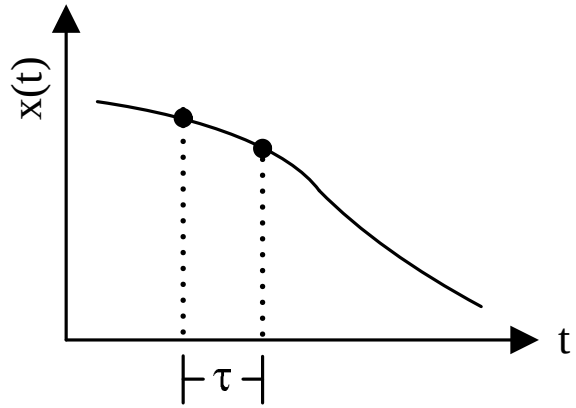
Effect of timing skew

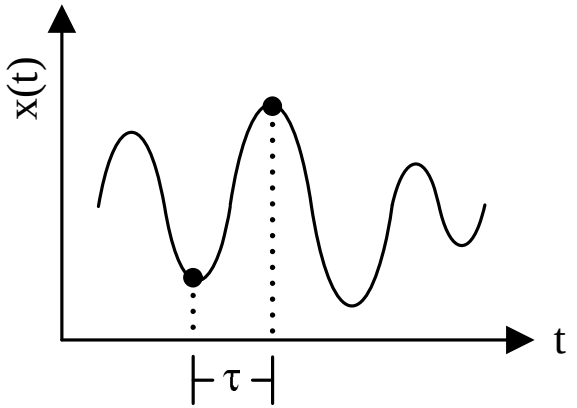
$$\sigma_\tau \leq \sqrt{\left(\frac{N}{N-1}\right) \cdot \left(\frac{2}{3 \cdot 2^{2B}}\right) \cdot \left(\frac{1}{|R''(0)|}\right)} \tag{27}$$

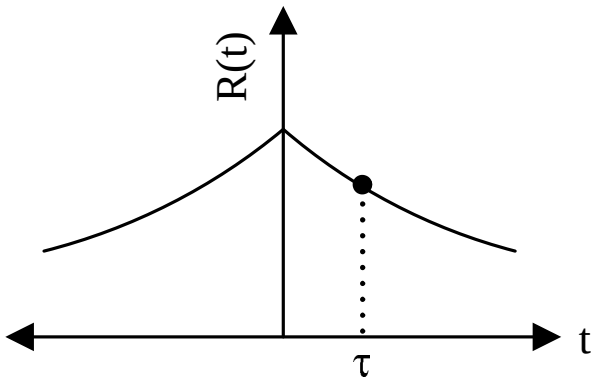
Function of three parameters (N, B, and $R''(0)$)

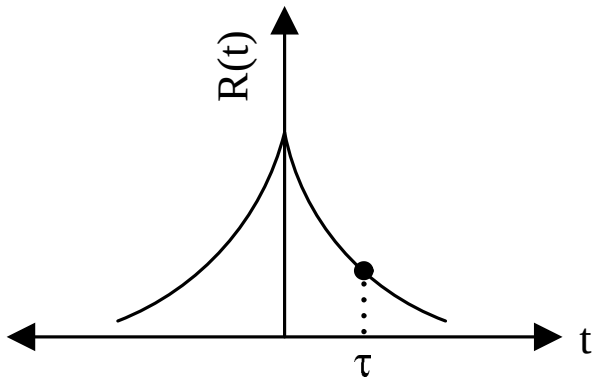
More on autocorrelation intuition

- Autocorrelation related to speed of signal

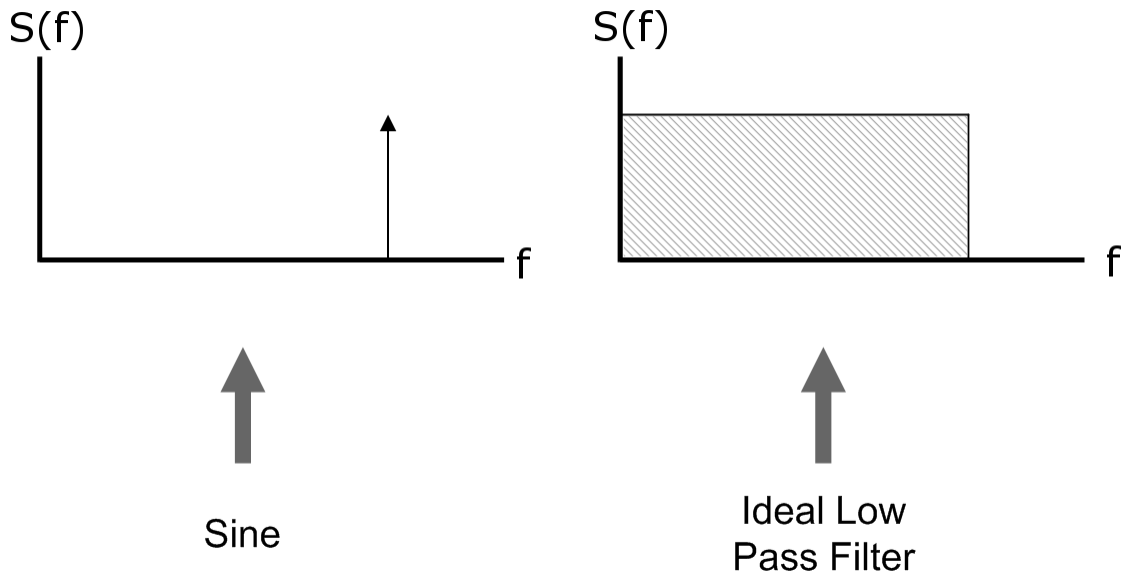








Importance of signal statistics



$$R(\tau) = \mathrm{sinc}(2\mathrm{f_c}\tau) \tag{28}$$

$$R''(0) = -\frac{1}{3}(2\pi f_c)^2 \tag{29}$$

- If you had used sine wave analysis, you would **overconstrain the variance of τ by 3**

Importance of signal statistics

- Same applies to more realistic signals (e.g. WSCS)
- If timing skew is a problem, then improve your design space by knowing your system
- Sidenote: this viewpoint also extends to nonlinearities and jitter (See e.g. [Gupta 2006] and [Da Dalt 2002])

Questions?

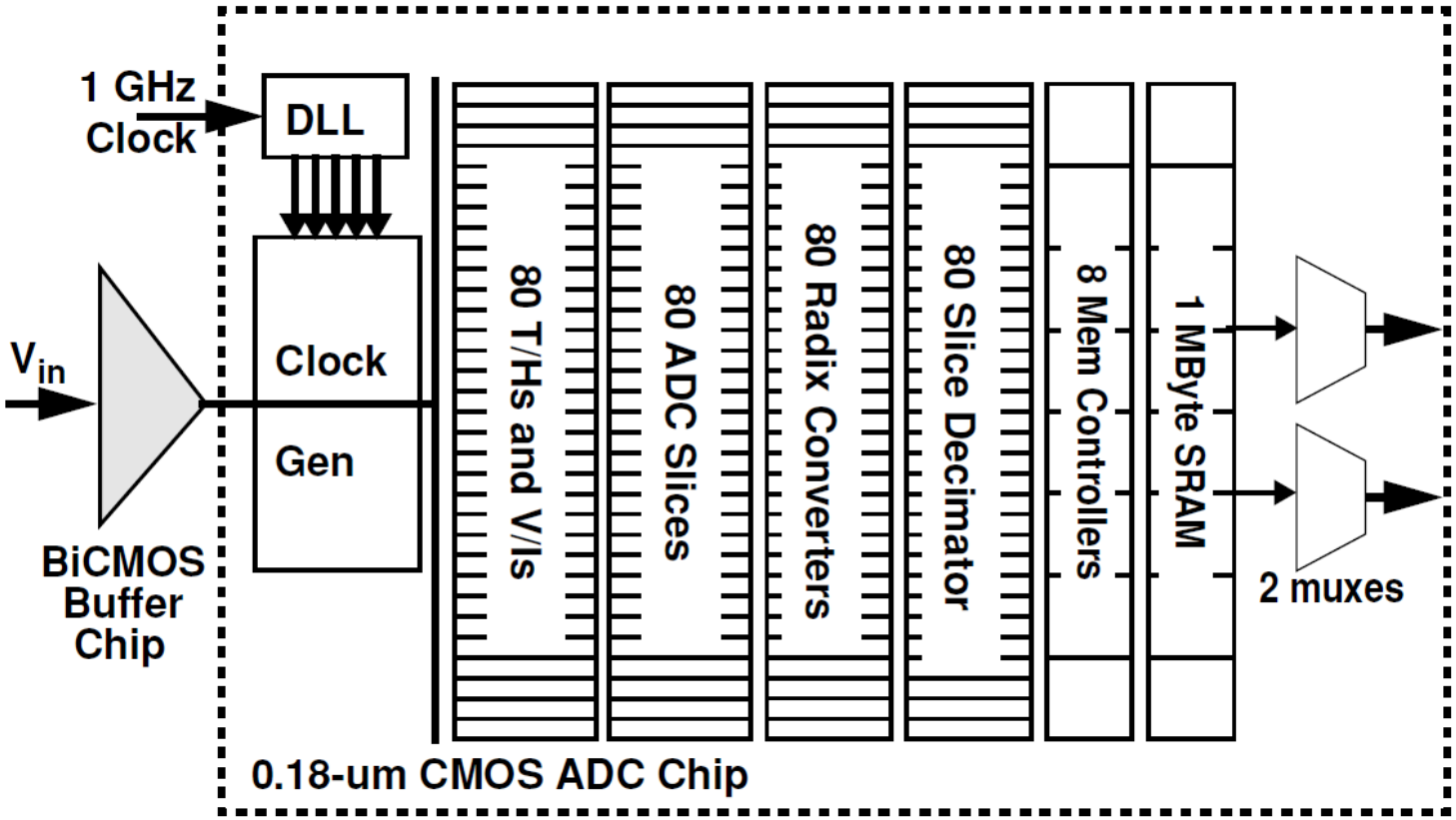
Part IV

Design of Time-Interleaved ADCs

The coolest ADCs from the past 10 years

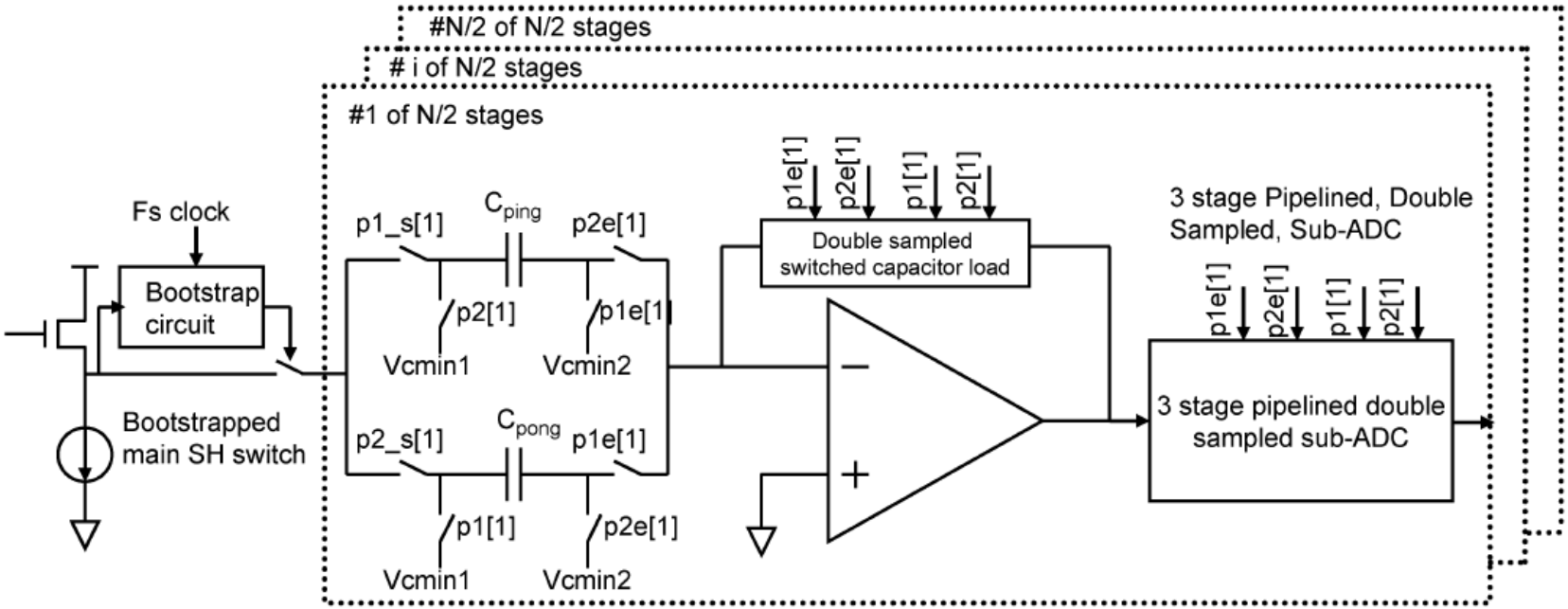
- Agilent, 2003, ISSCC
- Terranetics, JSSC 2006
- Nortel, ISSCC 2010
- Fujitsu, OFC 2010

Interleaving 80 pipeline ADCs



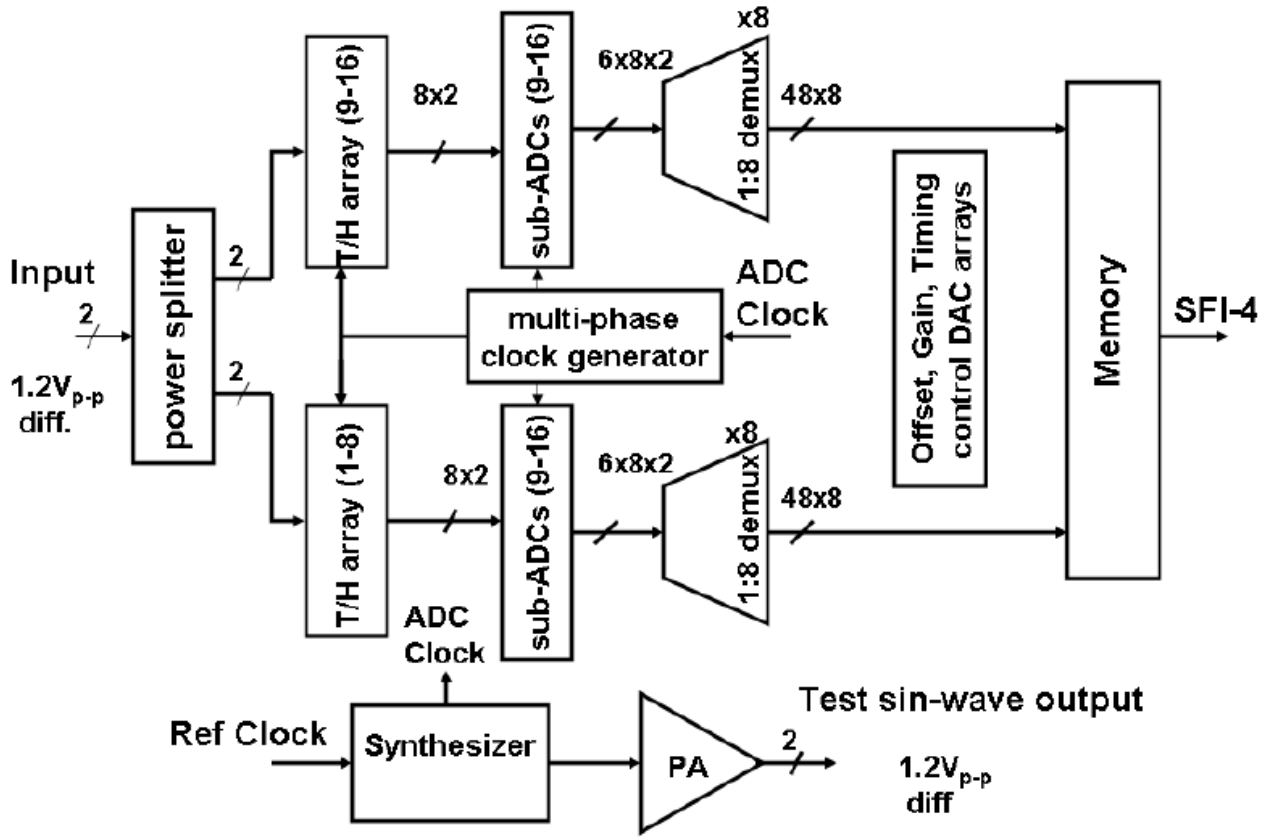
- 20 GS/s 8 bit ADC
- Correct for gain, offset, and timing skew [Poulton 2003]

Interleaving 4 pipeline ADCs



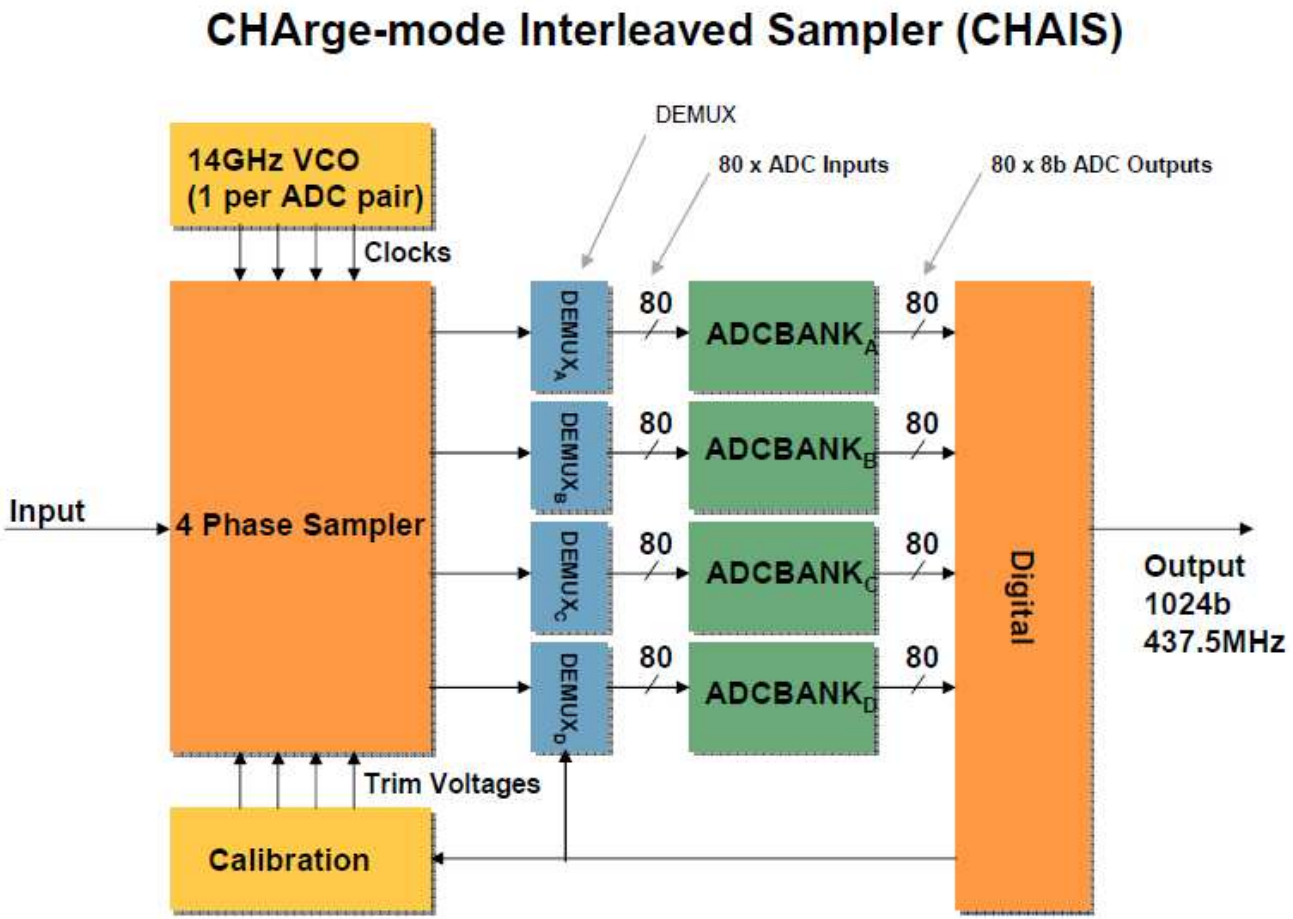
- 1 GS/s 11 bit ADC
- Correct for gain and offset [Gupta 2006]

Interleaving 16(0) SAR ADCs



- 40 GS/s 6 bit ADC
- Correct for gain, offset, and timing skew [Greshishchev 2010]

A 56 GS/s ADC



- 56 GS/s 8 bit ADC and interleaved 4x80 ADCs [Dedic 2010]

Choosing the design space

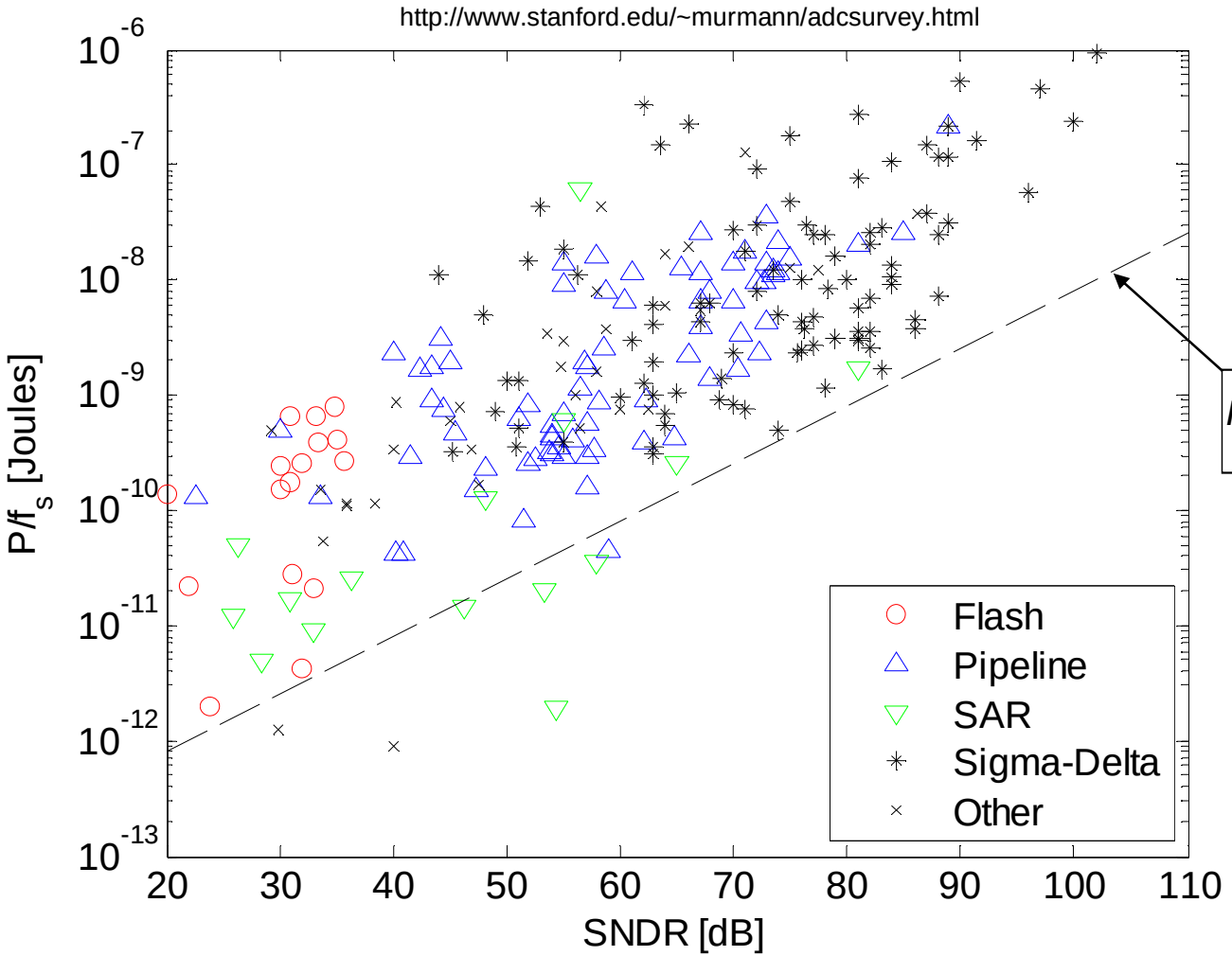
- You have: input signal statistics + bit resolution + application space
- Calculate acceptable bounds on time-varying errors
- Choose sub-ADC architecture (beyond scope of tutorial)
- Choose interleaving factor
- Design clocking network
- Deal with time-varying errors

Looks simpler than it is

Sub-ADC architecture

- Extremely low end resolution and high end resolution choice is easy
  - Flash ADCs for 3 bits
  - Sigma-Delta for 24 bits
- SAR, pipeline, ...

Sub-ADC architecture



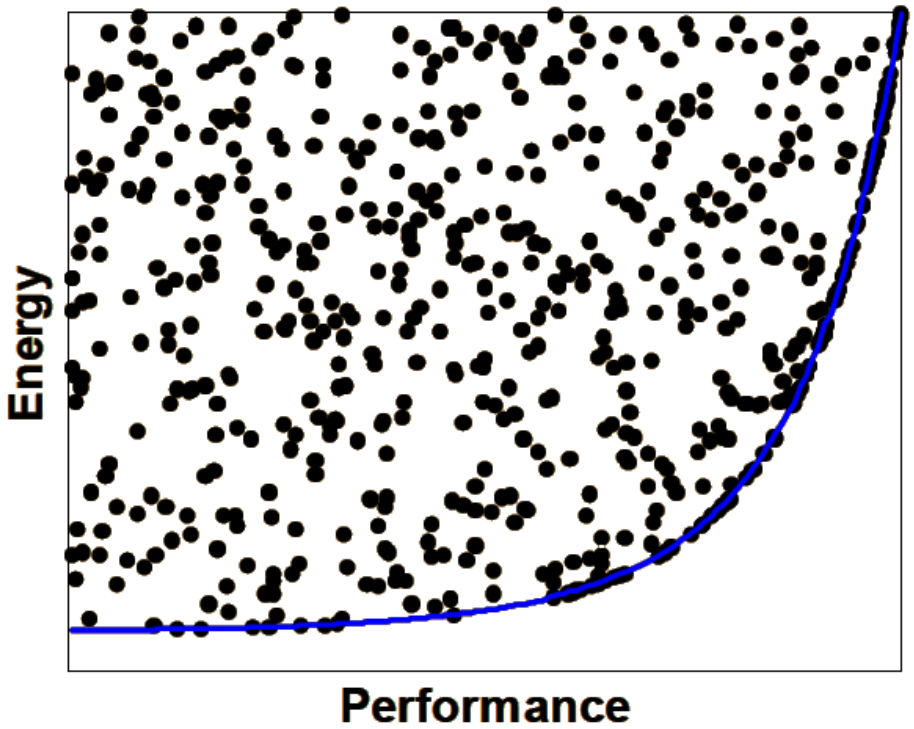
$$FOM = \frac{P}{f_s \cdot 2^{ENOB}} = 100 \frac{\text{fJ}}{\text{conv-step}}$$

$$ENOB = \frac{SNDR[dB] - 1.76}{6.02}$$

[Image from Murmann class notes]

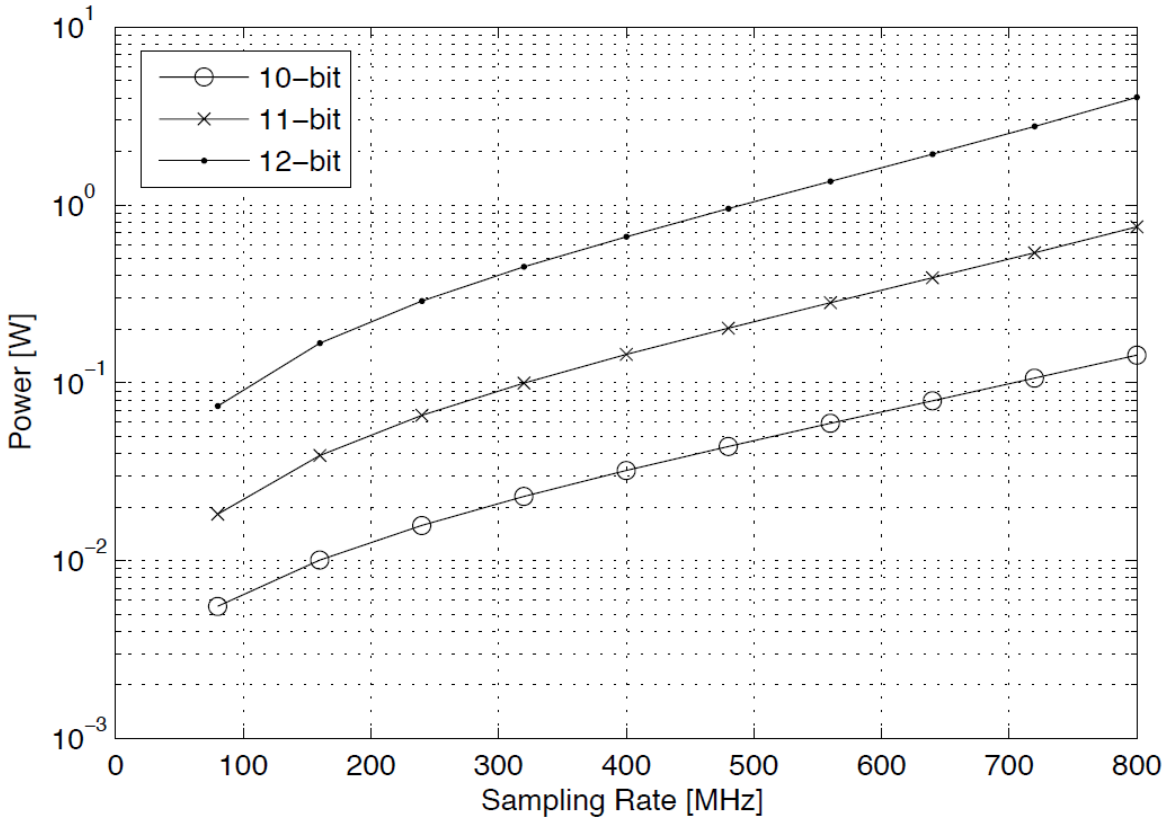
Interleaving can lower power*

- Lessons from parallel processing [Horowitz 2006]



* at the expense of complexity, area, and headache

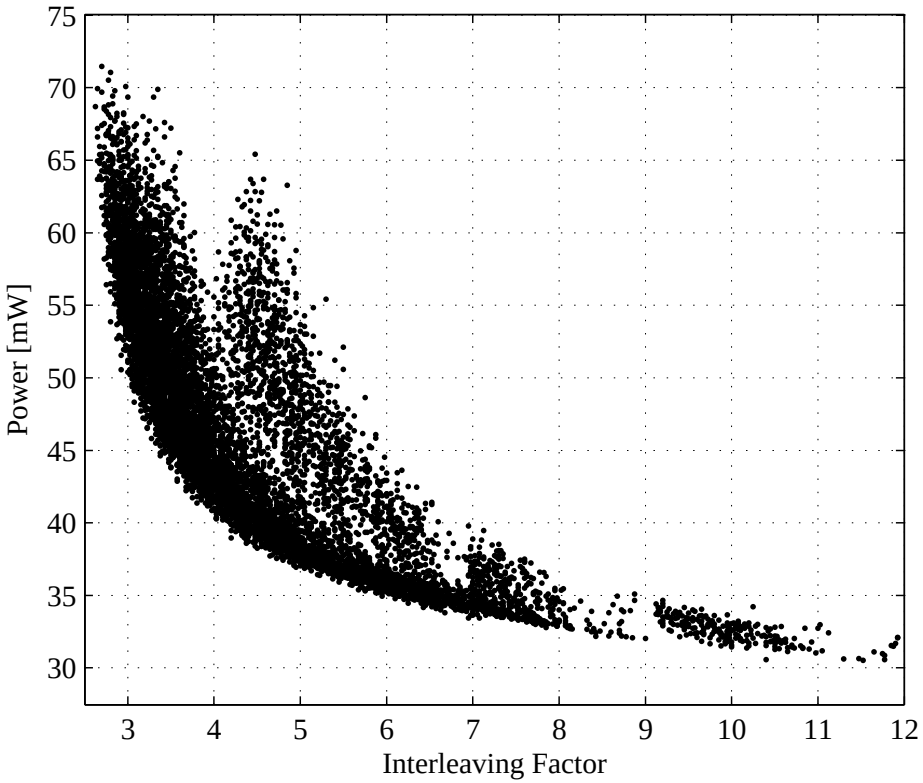
Interleaving can lower power



[Maloberti 2008]

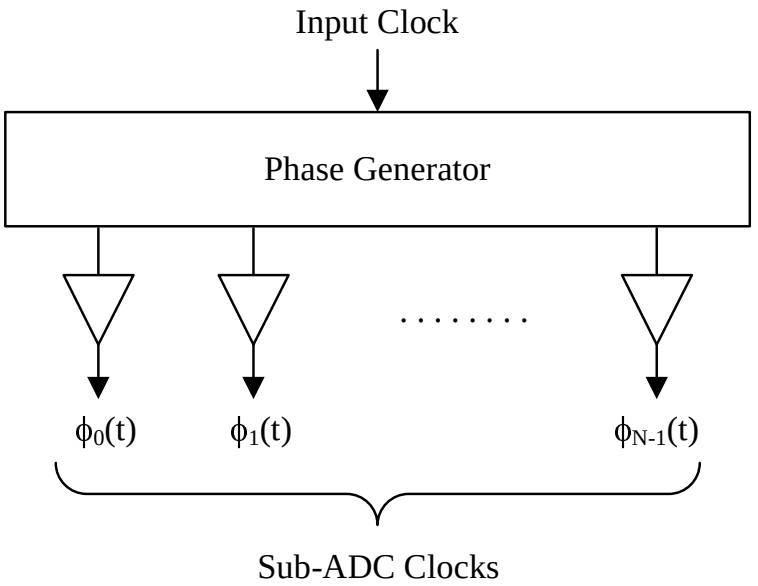
- 11-bit ADC at 100 MS/s needs $\sim$ 15 mW
- At 800 MS/s needs $\sim$ 700 mW

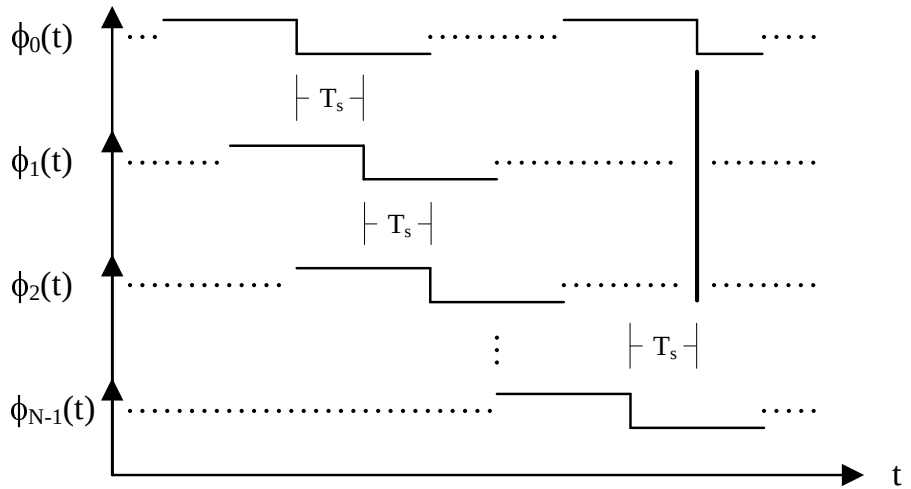
Interleaving can lower power



- Increasing f_s will force you to hit a technological wall
- True even in the smallest ADC element - the comparator

Clocking network





- Need to provide N clocks to sub-ADCs
- Ideally offset by T_s

Clocking network

- Phase locked loops and delay locked loops
- Can use frequencies lower than sub-ADC sample rates

Clocking network

- Clock-gating
- Use full-rate clocks and control sub-ADC clock with digital logic (e.g. [Louwsma 2008])

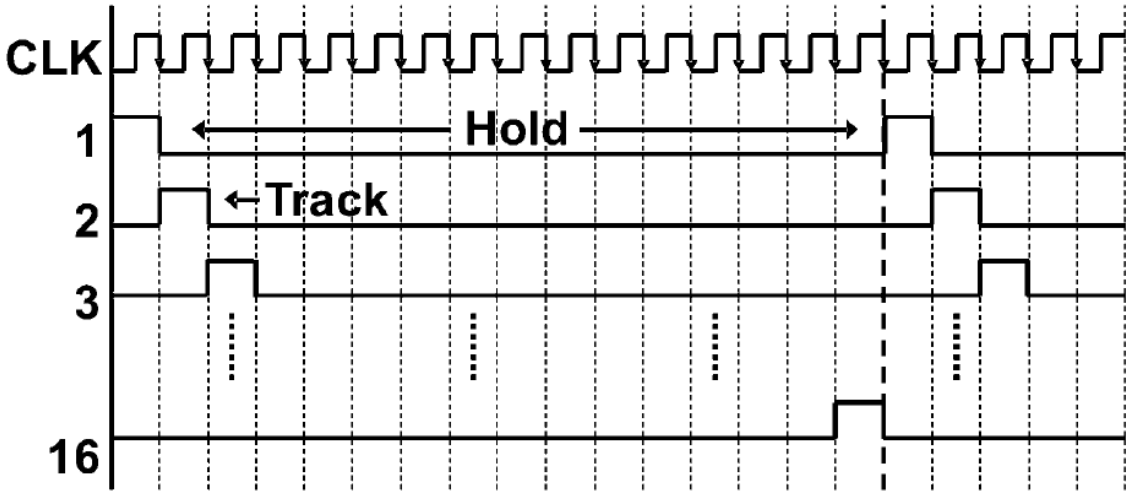
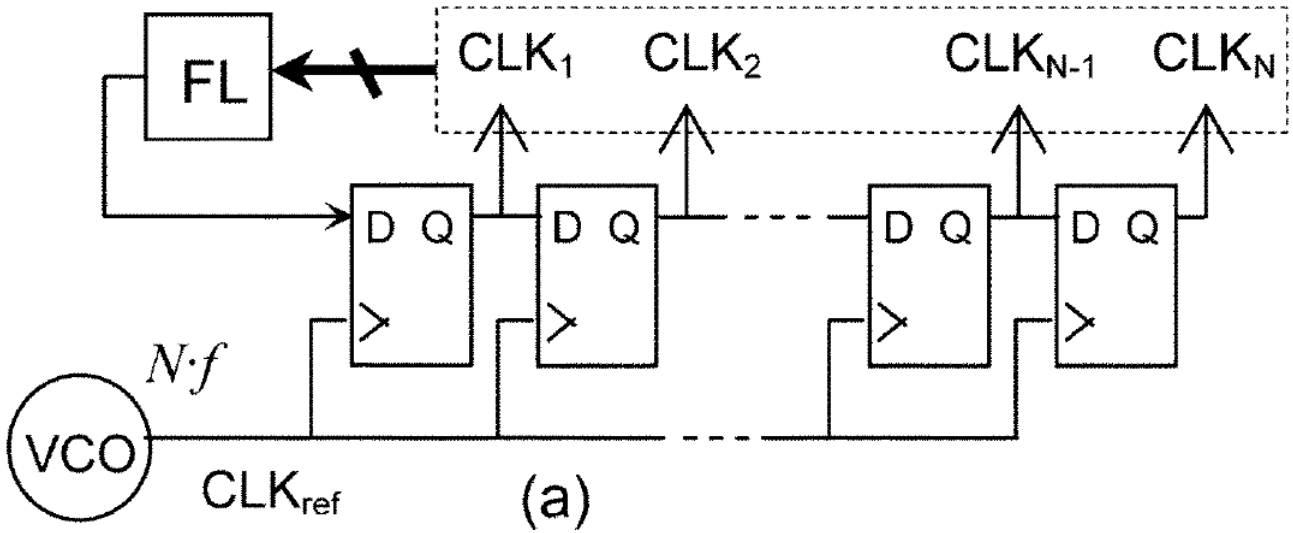


Fig. 2. Timing diagram of the time-interleaved T&H.

Clocking network

- Shift registers (e.g. [Gao 2008])



Time-varying errors?

- You've chosen your sub-ADC architecture
- and your interleaving factor
- and designed your clocking network

- How do you deal with time-varying errors?

- Two approaches: **correct by design** or **correct with calibration**

Approach 1: by design

$$v_{offset} \approx \frac{3}{\sqrt{WL}} mV/\mu m \tag{30}$$

- Pelgrom's Model

- 12-bit ADC, 1 V_{p-p} requires less than 0.3 mV offset
- $WL > 100\mu m^2$
- In 65 nm CMOS, $W > 1.5$ mm ...

Approach 1: by design

- There exist analog offset-minimization techniques for amplifiers and comparators

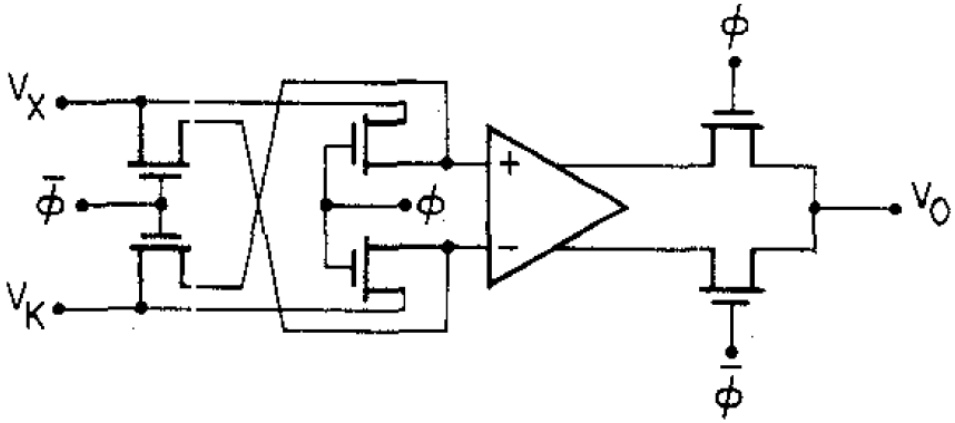


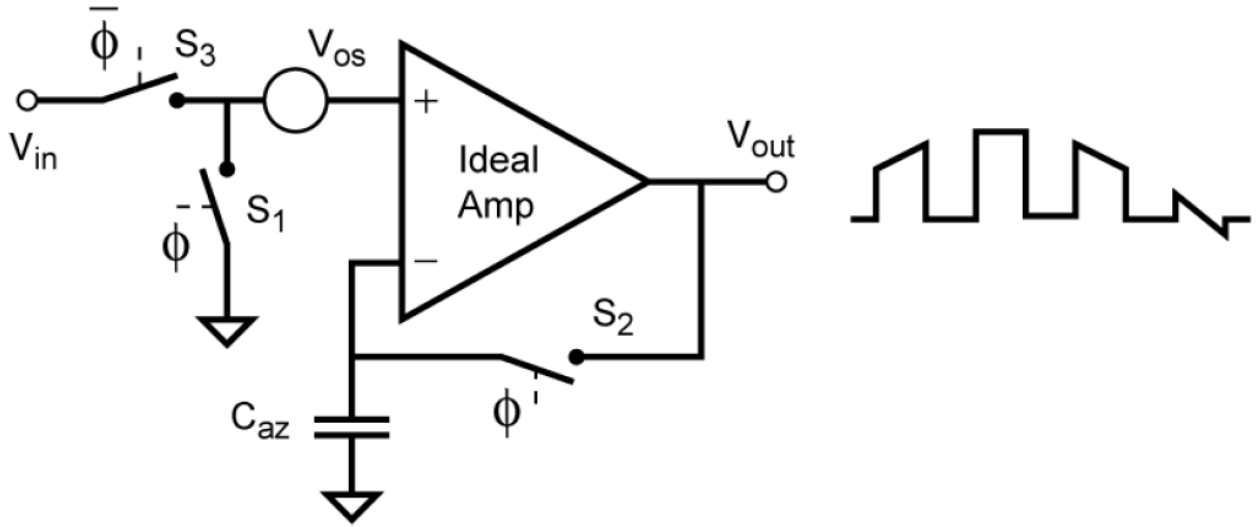
Fig. 8. Circuit for offset cancellation by subtraction.

[Suarez 1975]

- Most of these are extremely old

Approach 1: by design

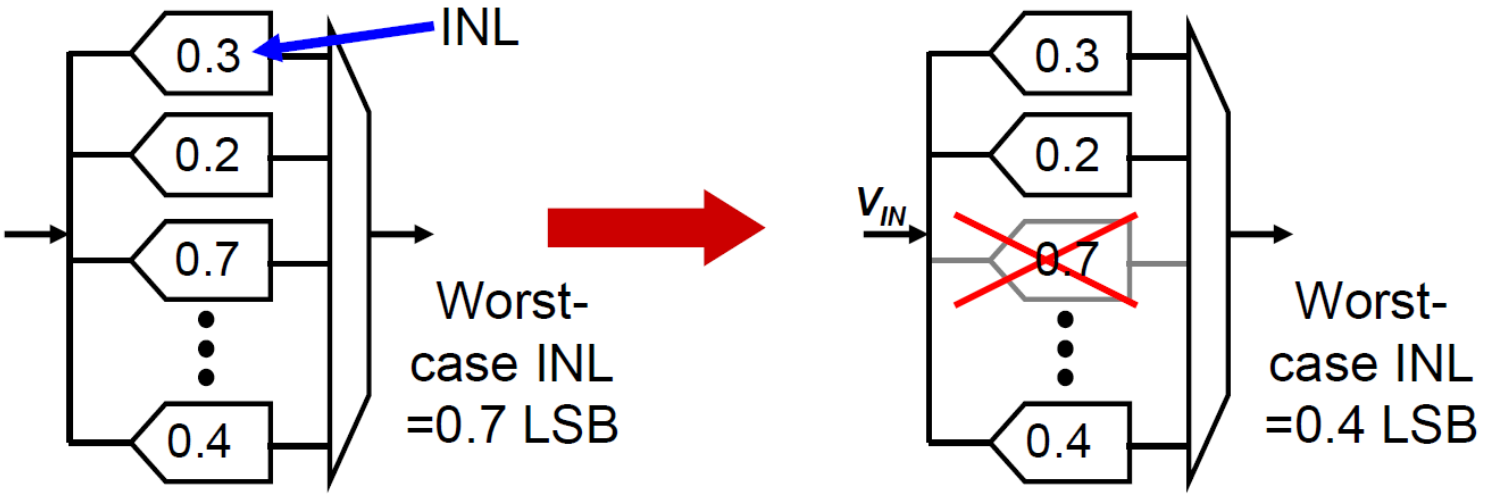
- Trimming
- Dynamic techniques: auto-zeroing or chopping



[Makinwa 2002]

Approach 1: by design

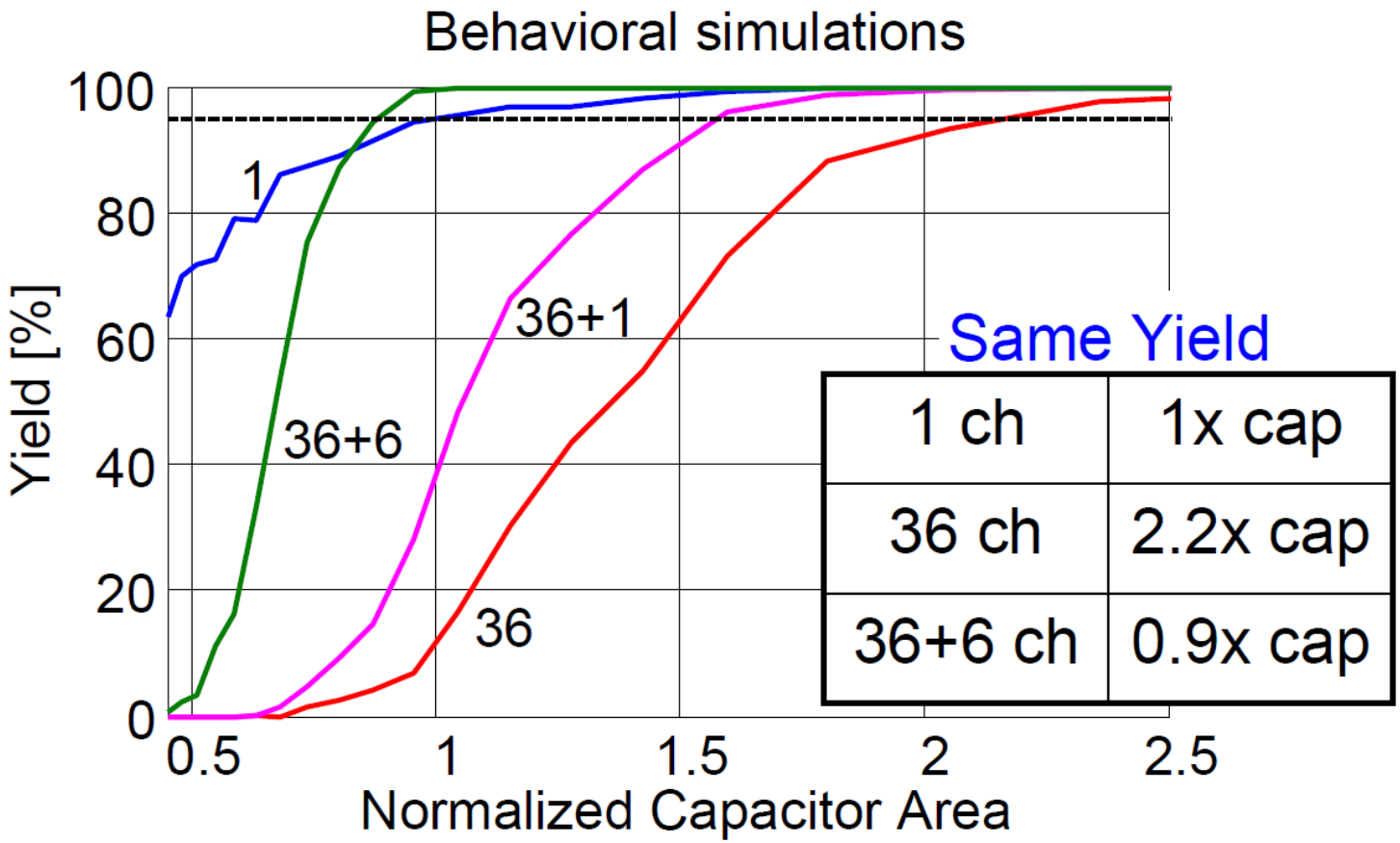
- Introduce redundancy



[Ginsburg 2008]

Approach 1: by design

- Introduce redundancy



[Ginsburg 2008]

Alternative approach for offset and gain

- Correct with calibration

Some design techniques for timing skew

- Timing skew problem exists between track-and-holds
- Use a front-end sampler

Front-end sampler

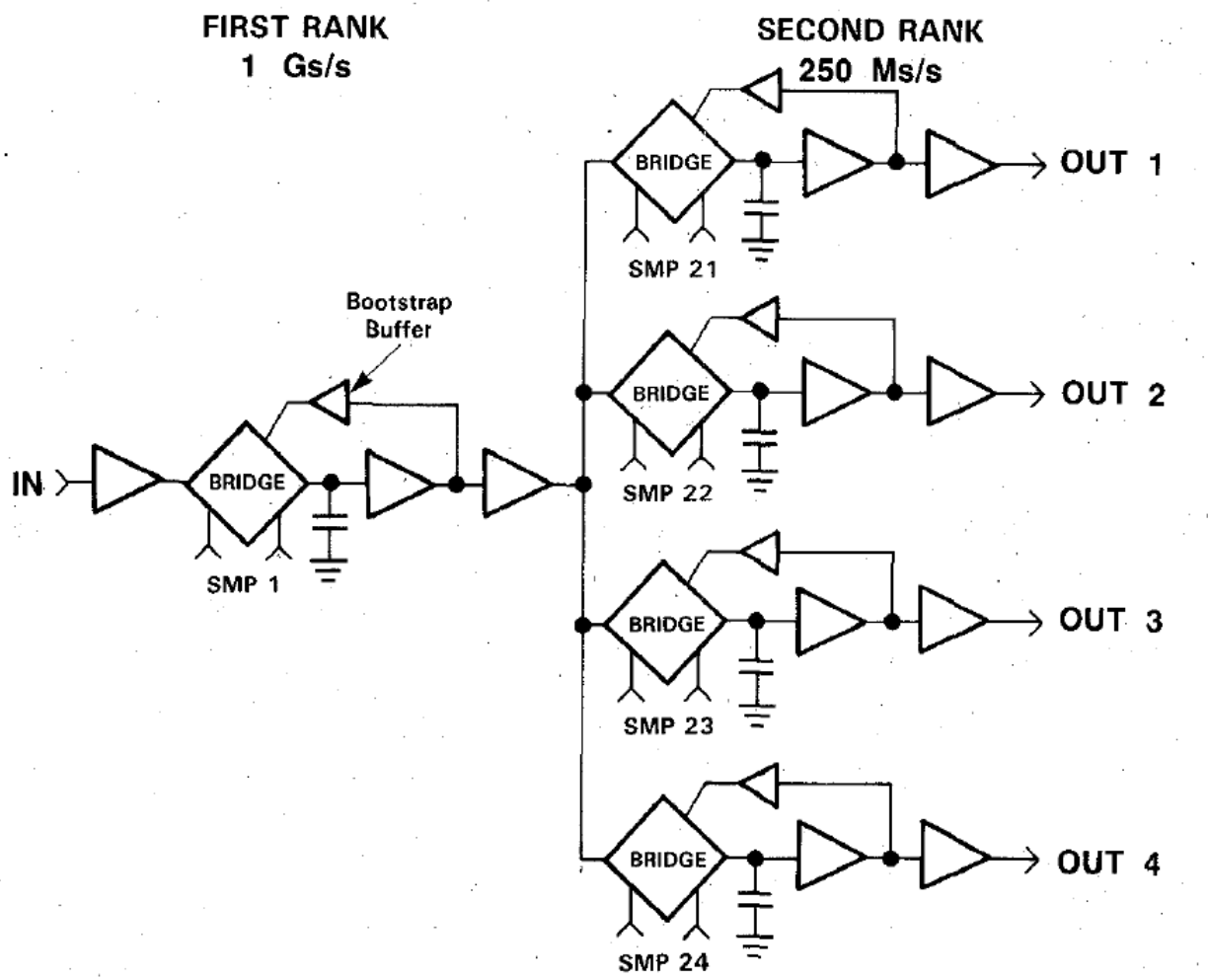
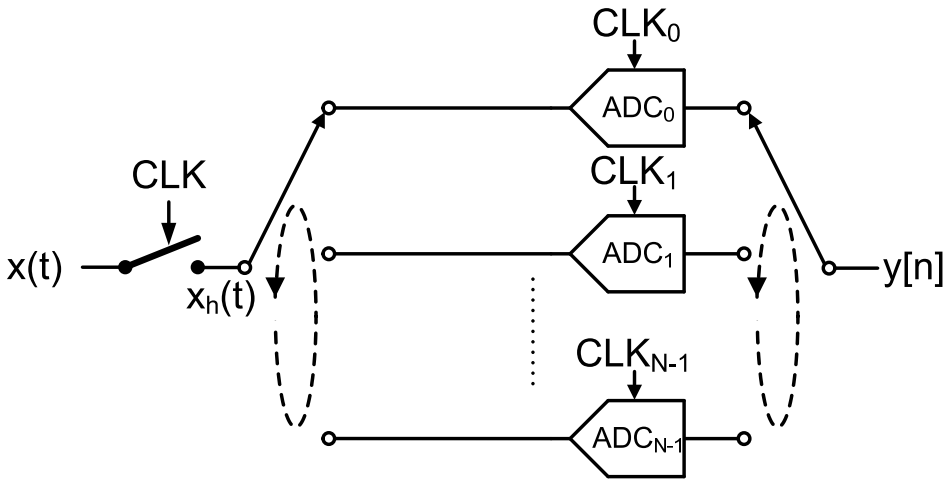
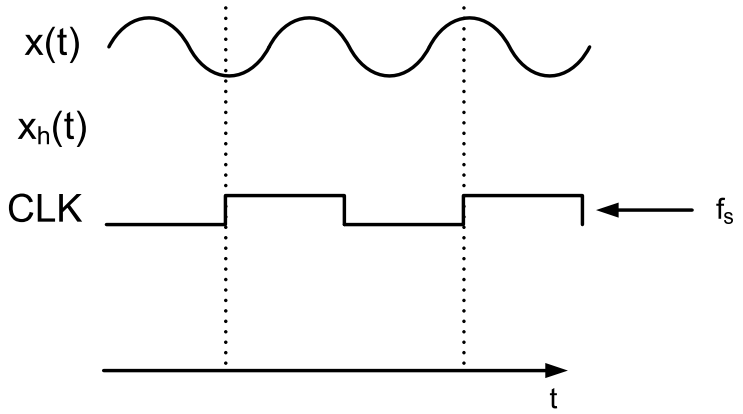


Fig. 3. S/H chip block diagram. All buffers are unity-gain source followers.

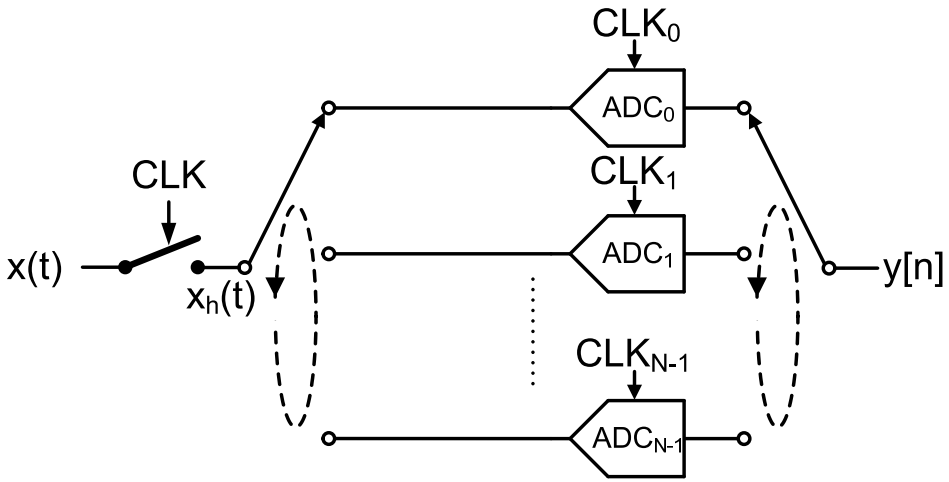
[Poulton 1987]

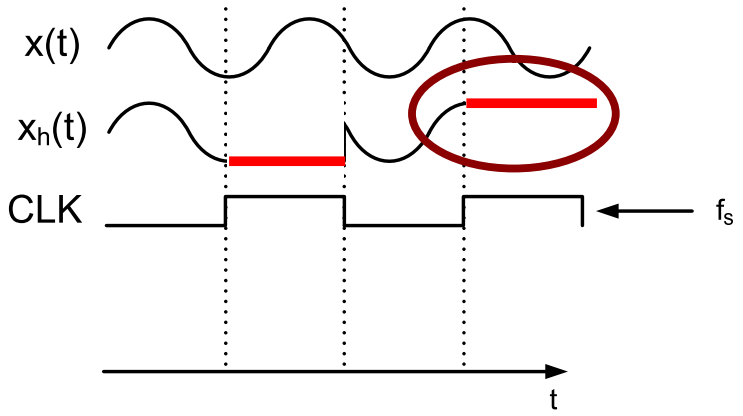
Front-end sampler



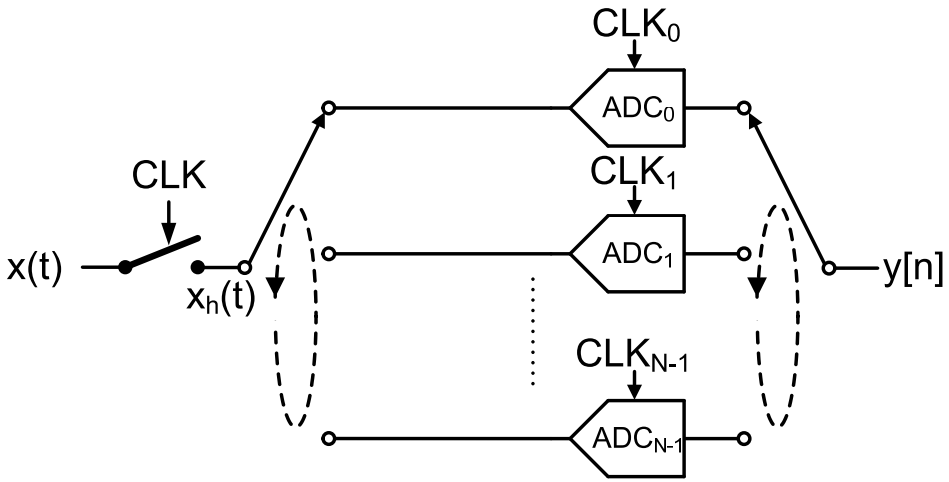


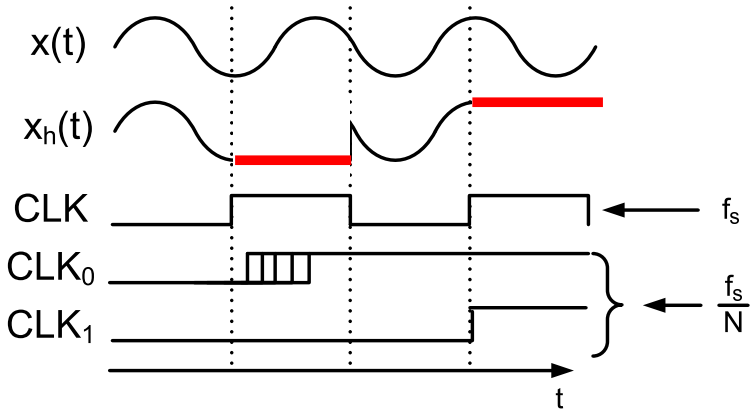
Front-end sampler



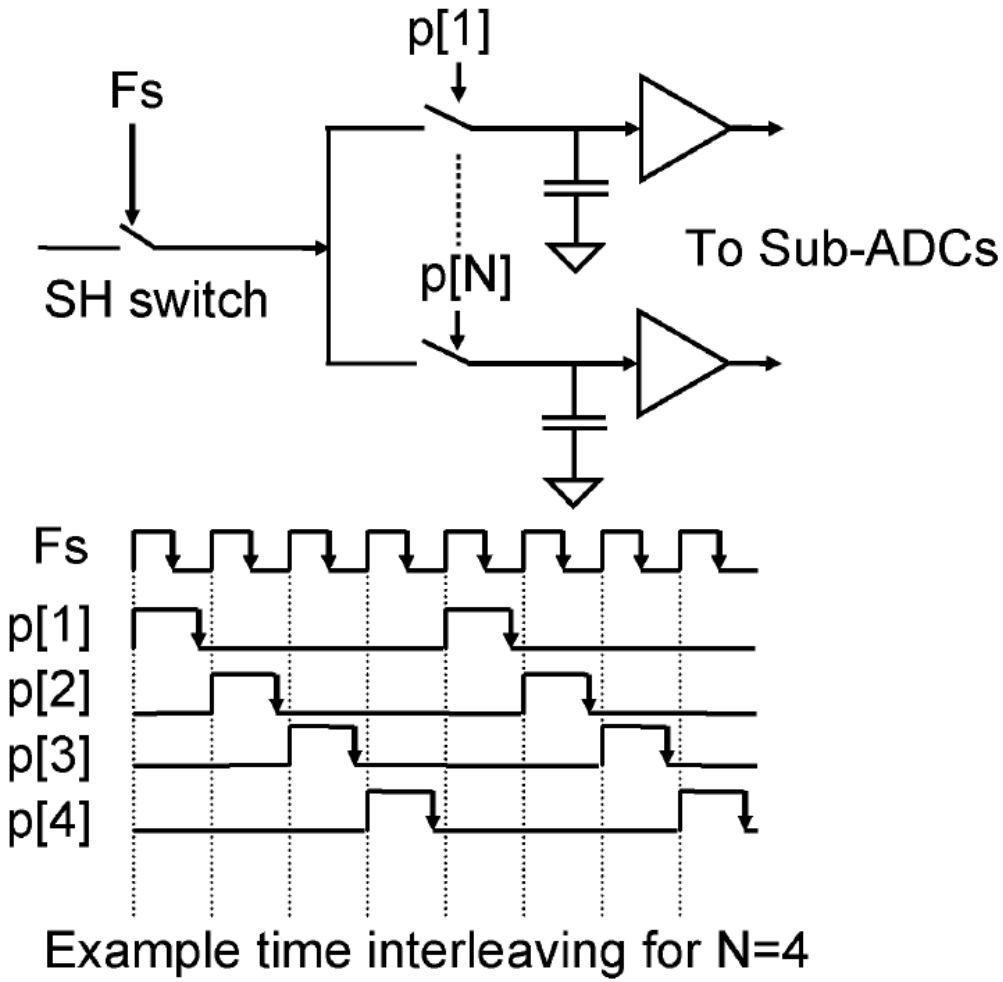


Front-end sampler





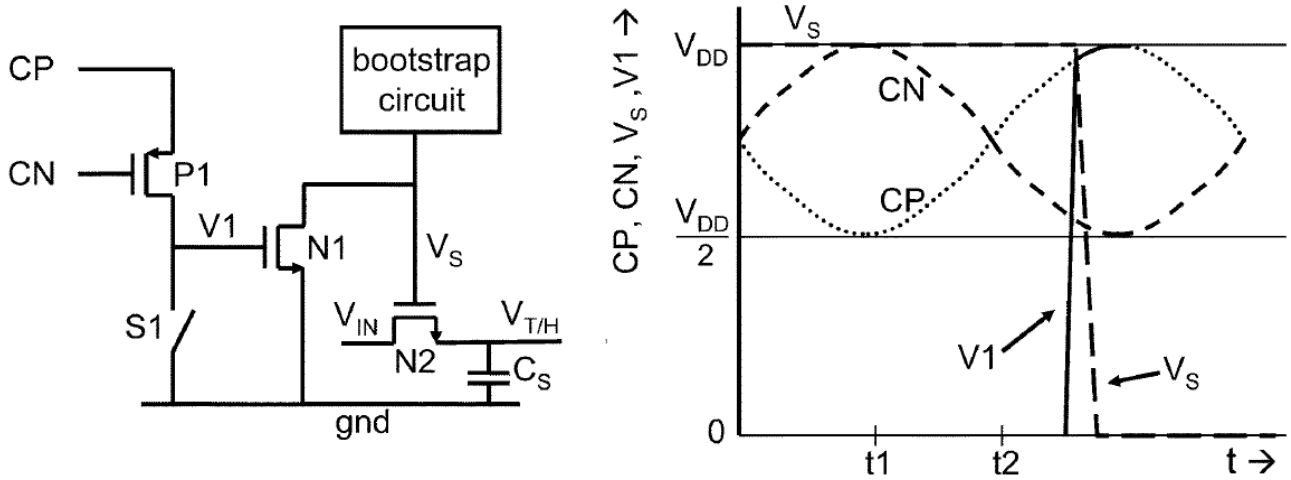
Front-end sampler



[Gupta 2006]

Use a better clocking scheme

- Front-end samplers have limited application



[Louwsma 2008]

- 10 b, 1.35 GS/s
- Transistor threshold limitation

Part V

Calibration

Approach 2: use calibration

- Straightforward for offset and gain
- Not as trivial for timing skew

Calibration = estimation + correction

Definition

Estimation: An approximation of the value or extent of something

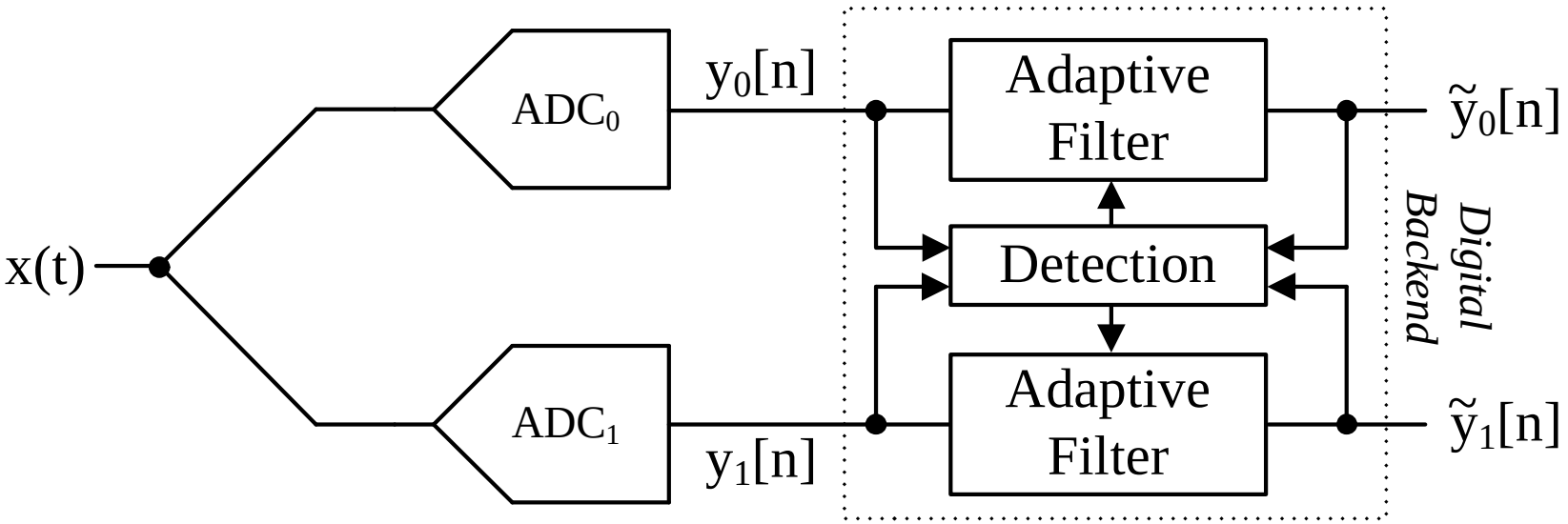
Definition

Correction: The action or process of correcting something

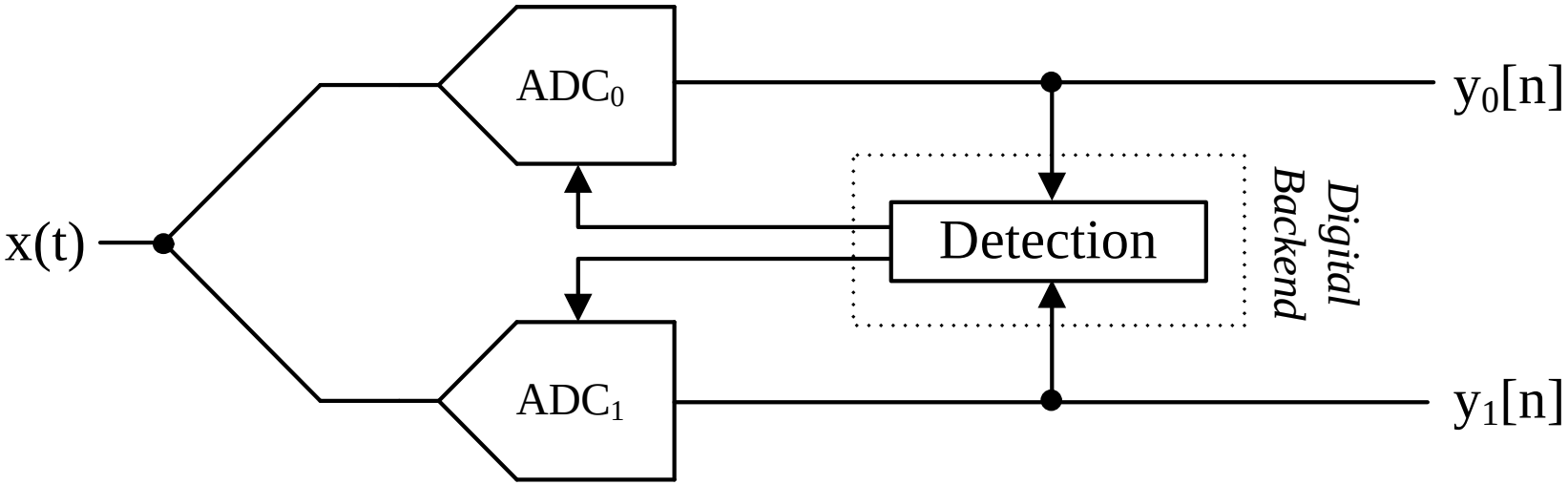
Types of calibration

- Digital vs. mixed-signal
- Foreground vs. background

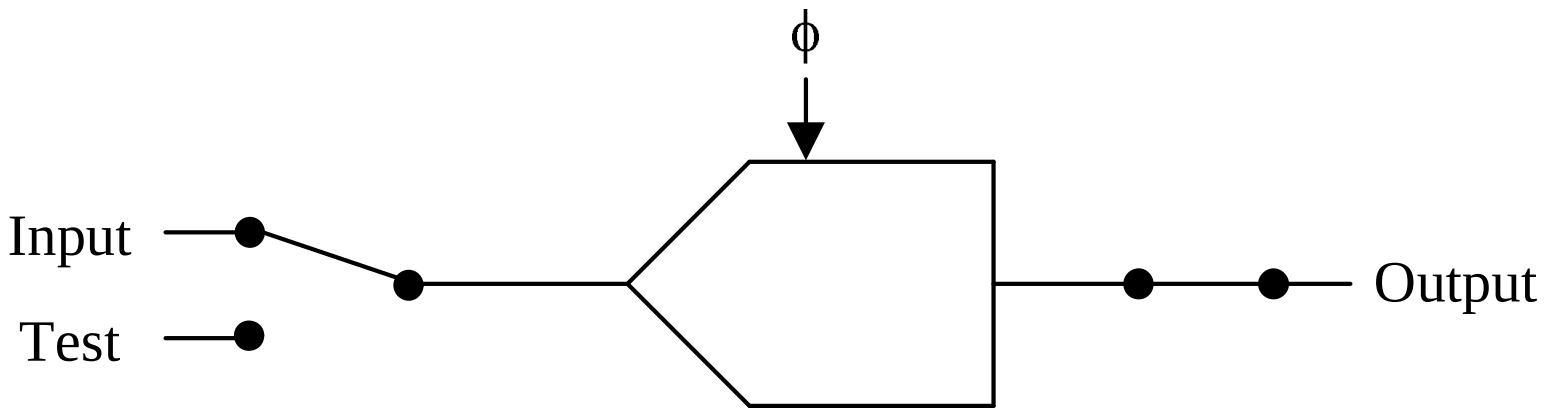
Digital calibration



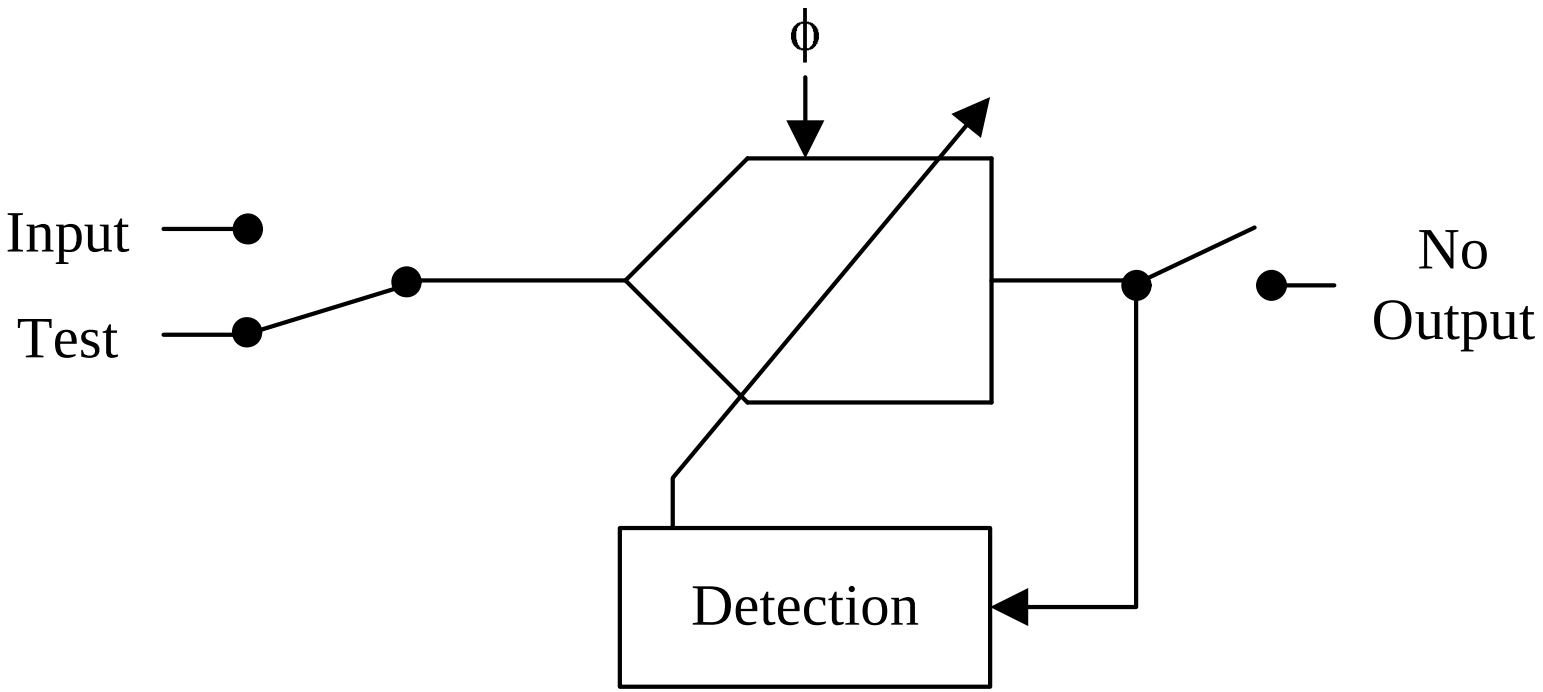
Mixed-signal calibration



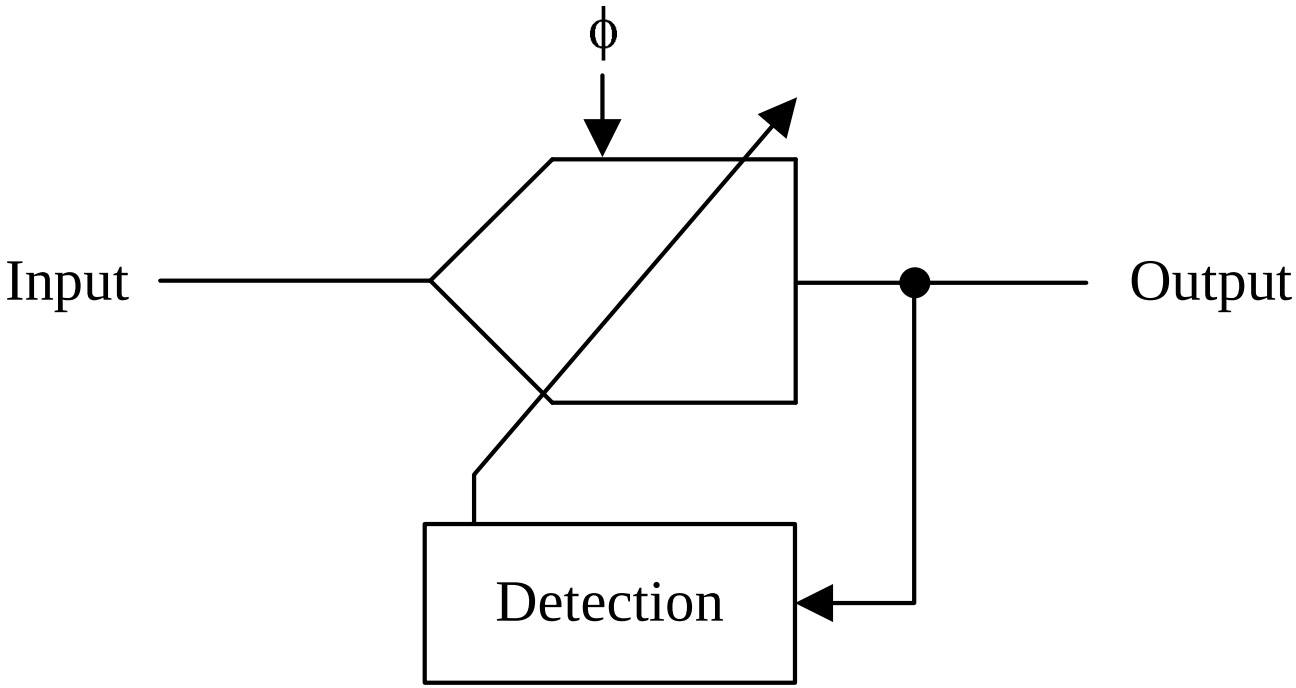
Foreground calibration



Foreground calibration



Background calibration



Offset and gain "almost" solved problem

- Still a research topic
- But ... there is a popular solution

Correcting offset

- Estimation ...

$$o_i \propto \sum_j D_{i,j} \tag{31}$$

- Correction ...

$$\hat{D}_{i,j} = D_{i,j} - o_i \tag{32}$$

Correcting gain

- Estimation ...

$$G_i \propto \sum_j (D_{i,j})^2 \tag{33}$$

- Correction ...

$$\hat{D}_{i,j} = D_{i,j}/G_i \tag{34}$$

Example 1 (1998)

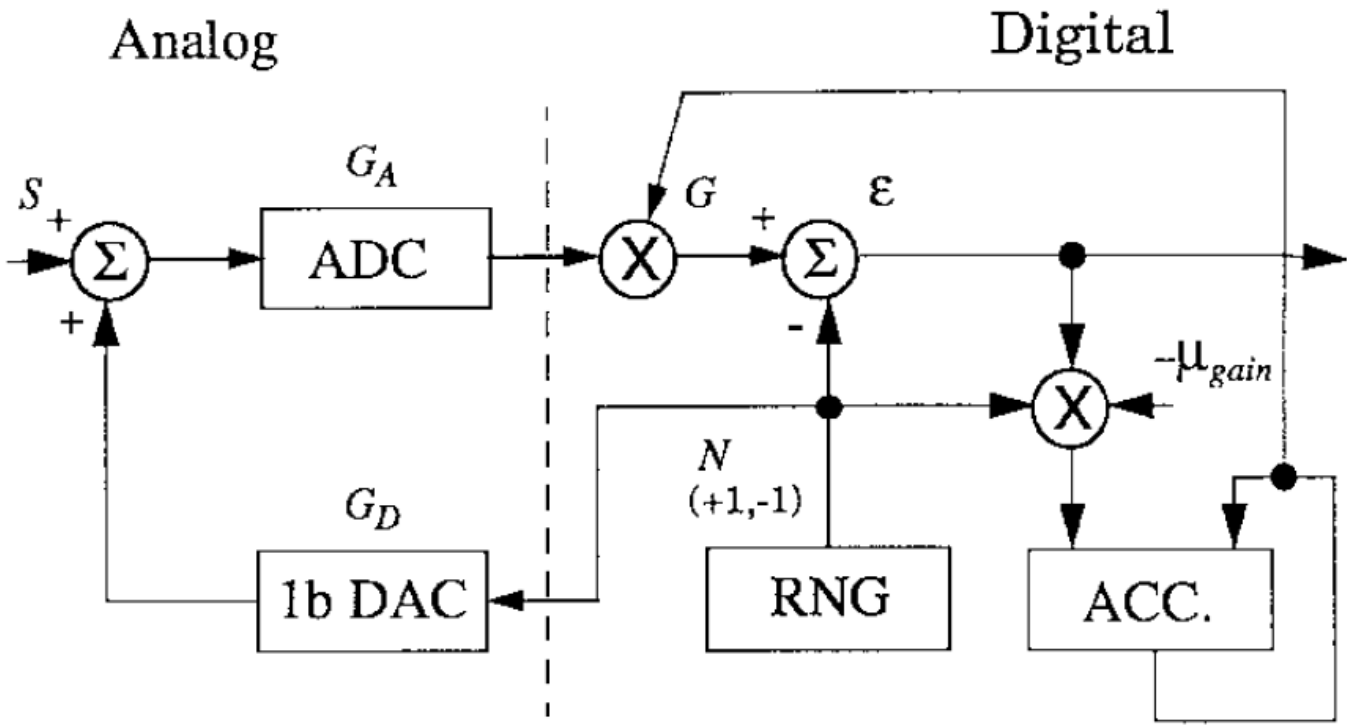


Fig. 2. The gain calibration loop.

[Fu 1998]

Example 1 (1998)

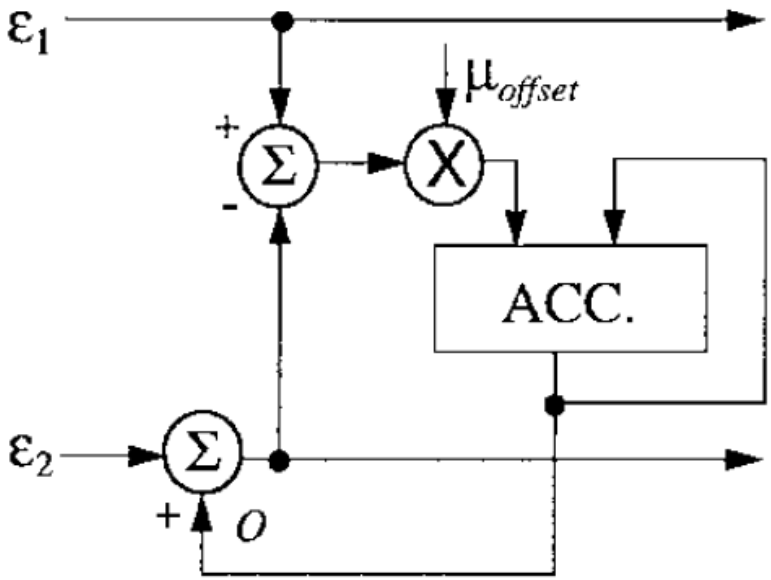


Fig. 5. Offset calibration system for two time-interleaved ADC's.

[Fu 1998]

Example 1 (1998)

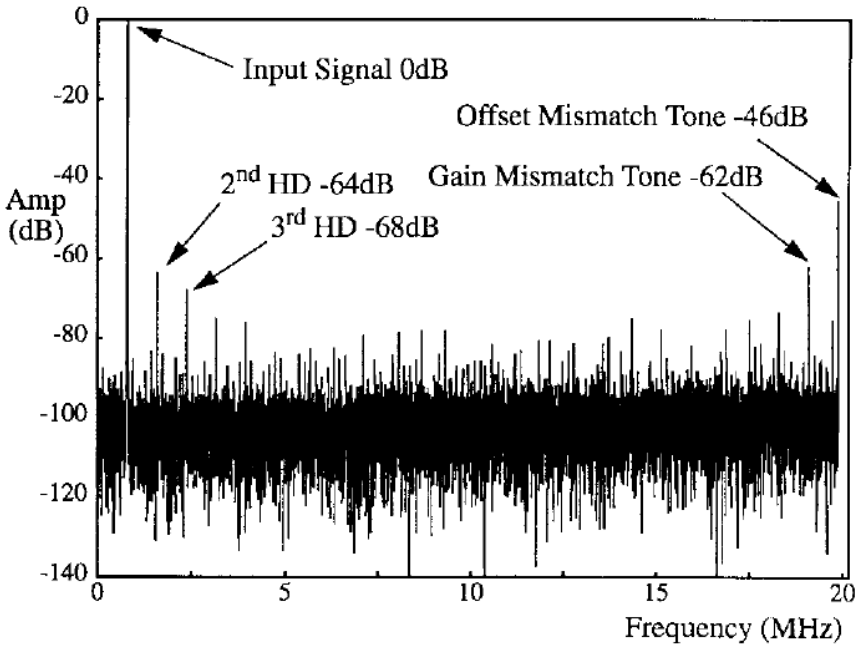


Fig. 11. ADC output spectrum without calibration.

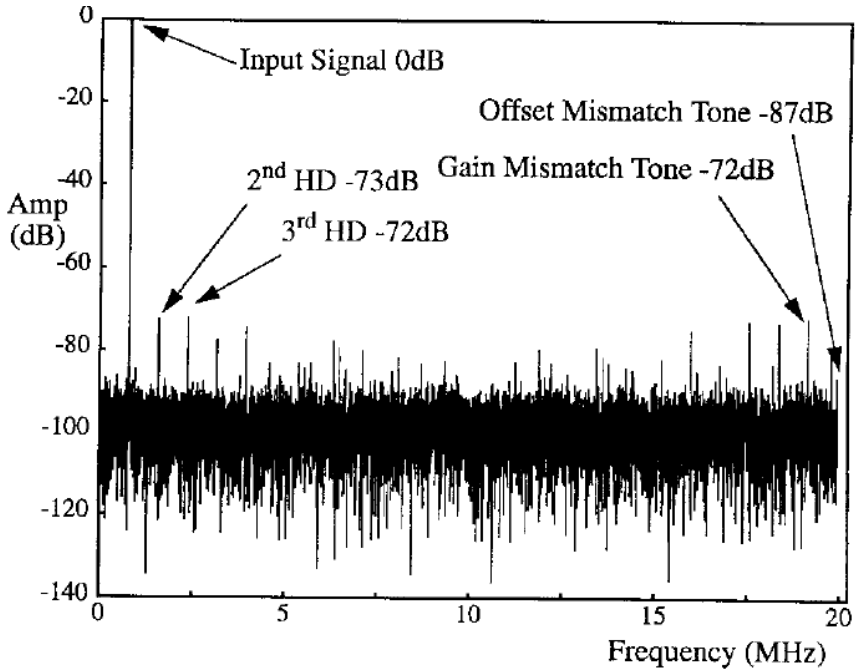


Fig. 12. ADC output spectrum with calibration.

- 10-bit, 40 MS/s, two-way interleaved ADC [Fu 1998]

Example 2 (2001)

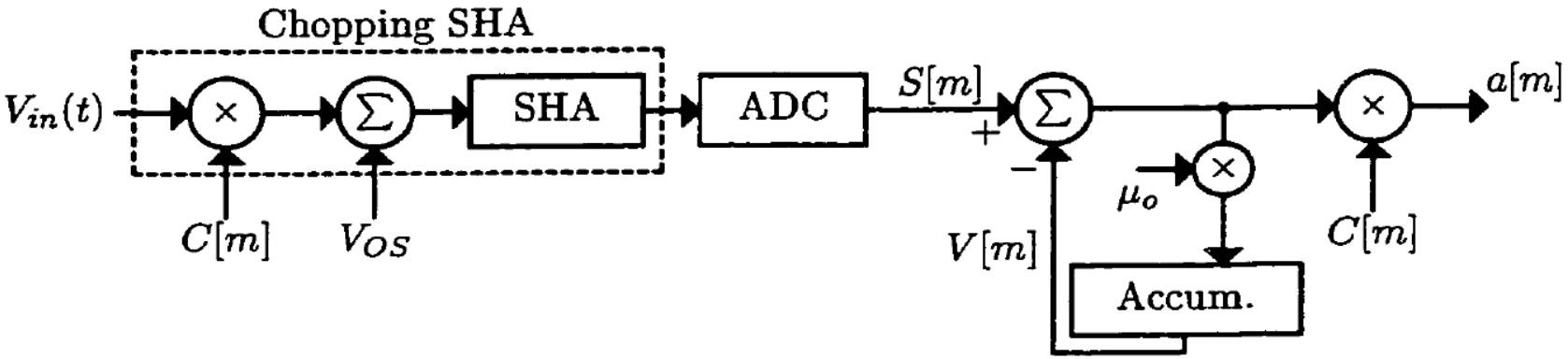


Figure 3.2: Chopper-based offset calibration for single channel.

[Jamal 2001]

Example 2 (2001)

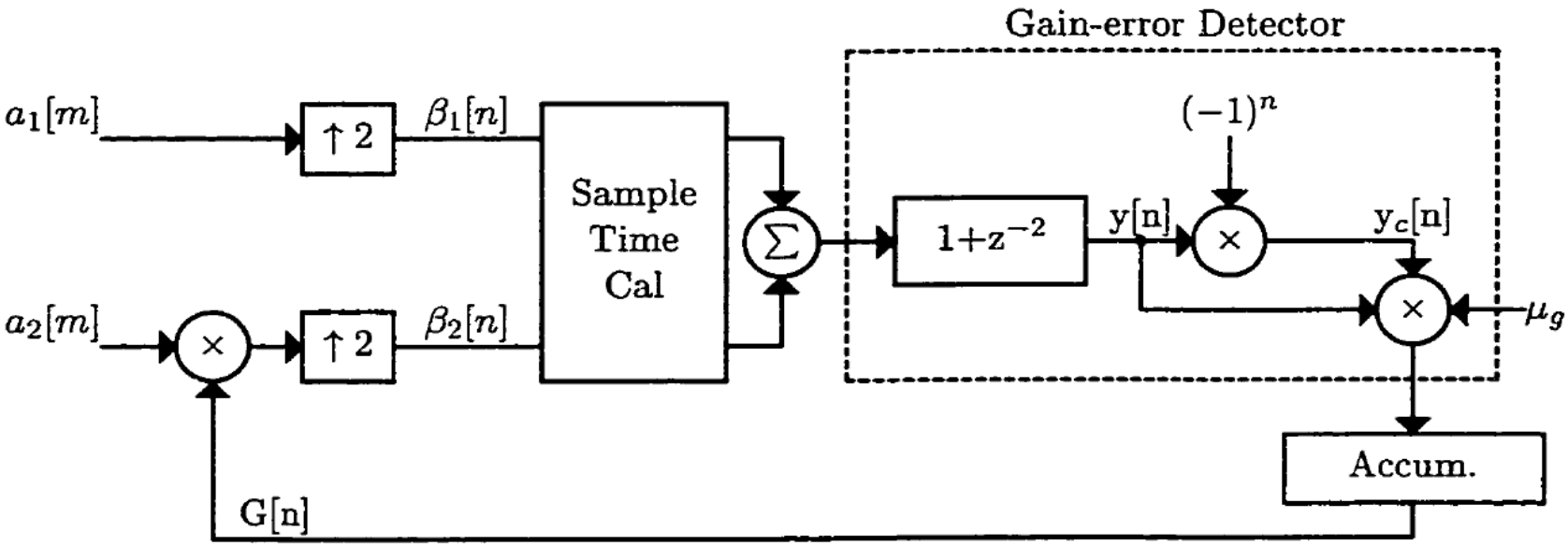


Figure 3.7: Block diagram of the gain calibration scheme

[Jamal 2001]

Example 3 (2007)

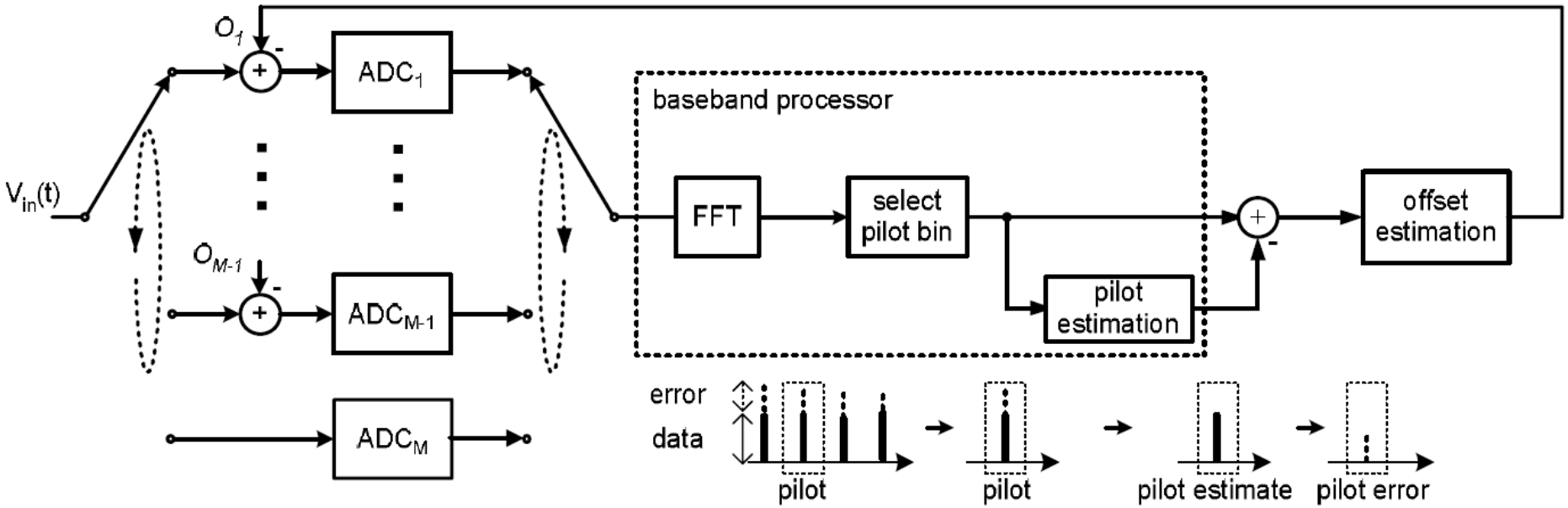


Fig. 2. Block diagram of the proposed calibration technique.

[Oh 2007]

- Makes use of pilot tones in OFDM systems

Example 3 (2007)

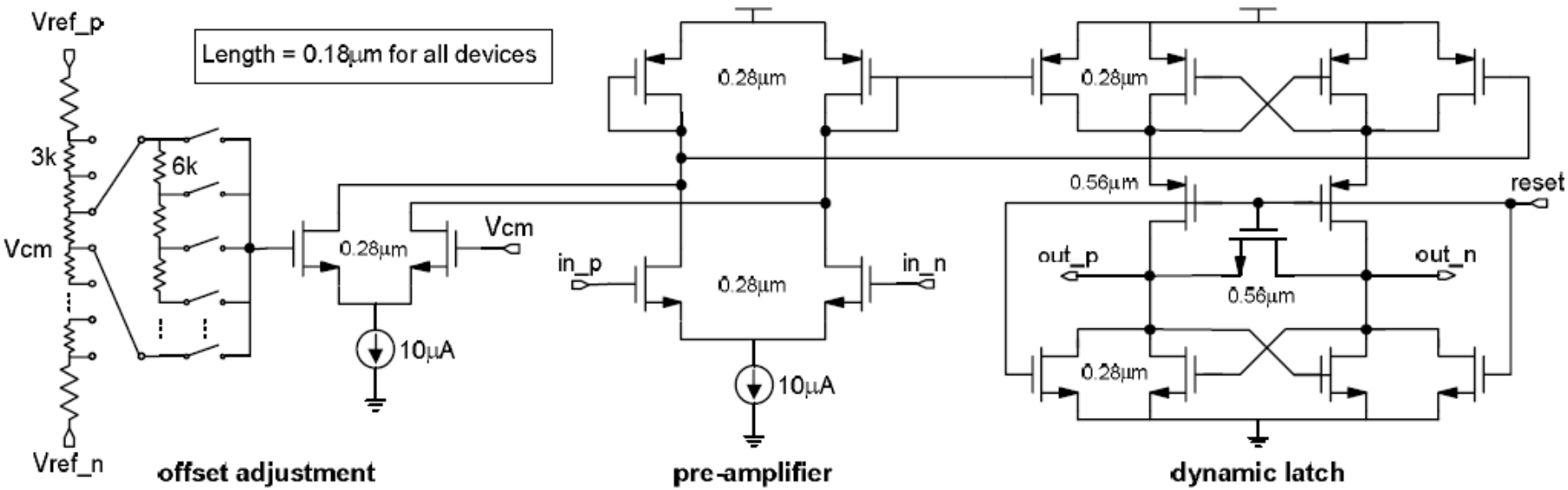


Fig. 3. Comparator circuit with offset adjustment DAC.

[Oh 2007]

Example 3 (2007)

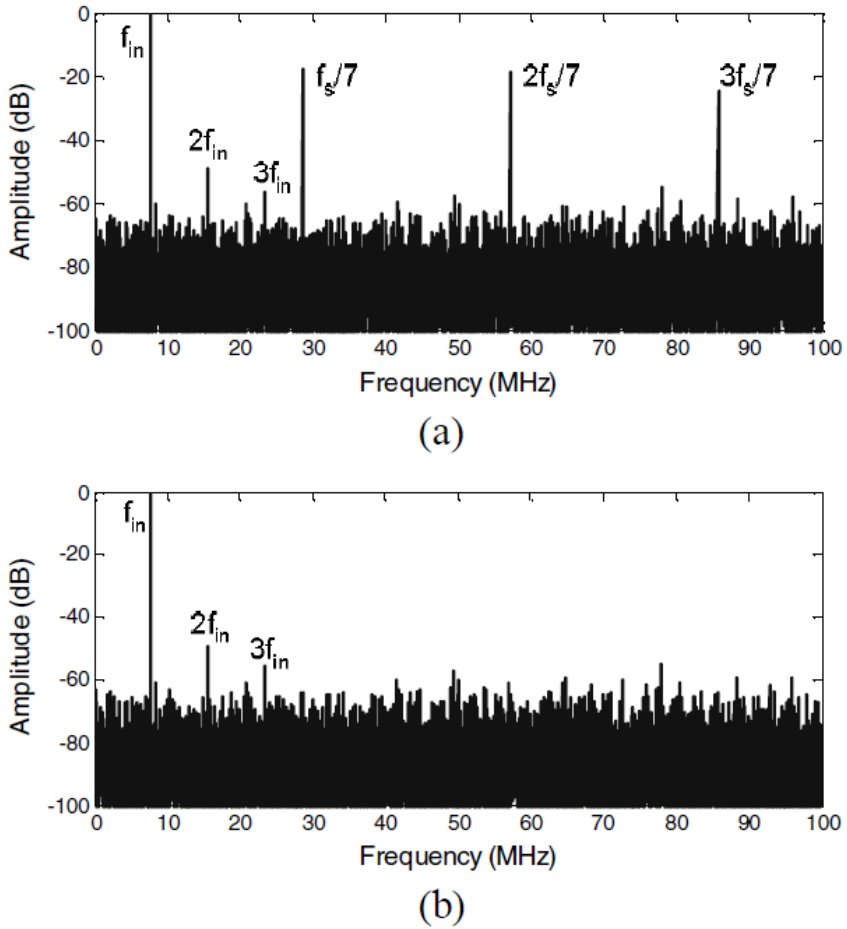


Fig. 7. Single tone FFT of the time-interleaved ADC array (f_{in}=8MHz, f_s=200MHz). (a) Before offset adjustment. (b) With ideal offset adjustments.

[Oh 2007]

- 6-bit, 200 MS/s

And timing skew?

- Still ongoing research
- No single winner

Example 1 (2001)

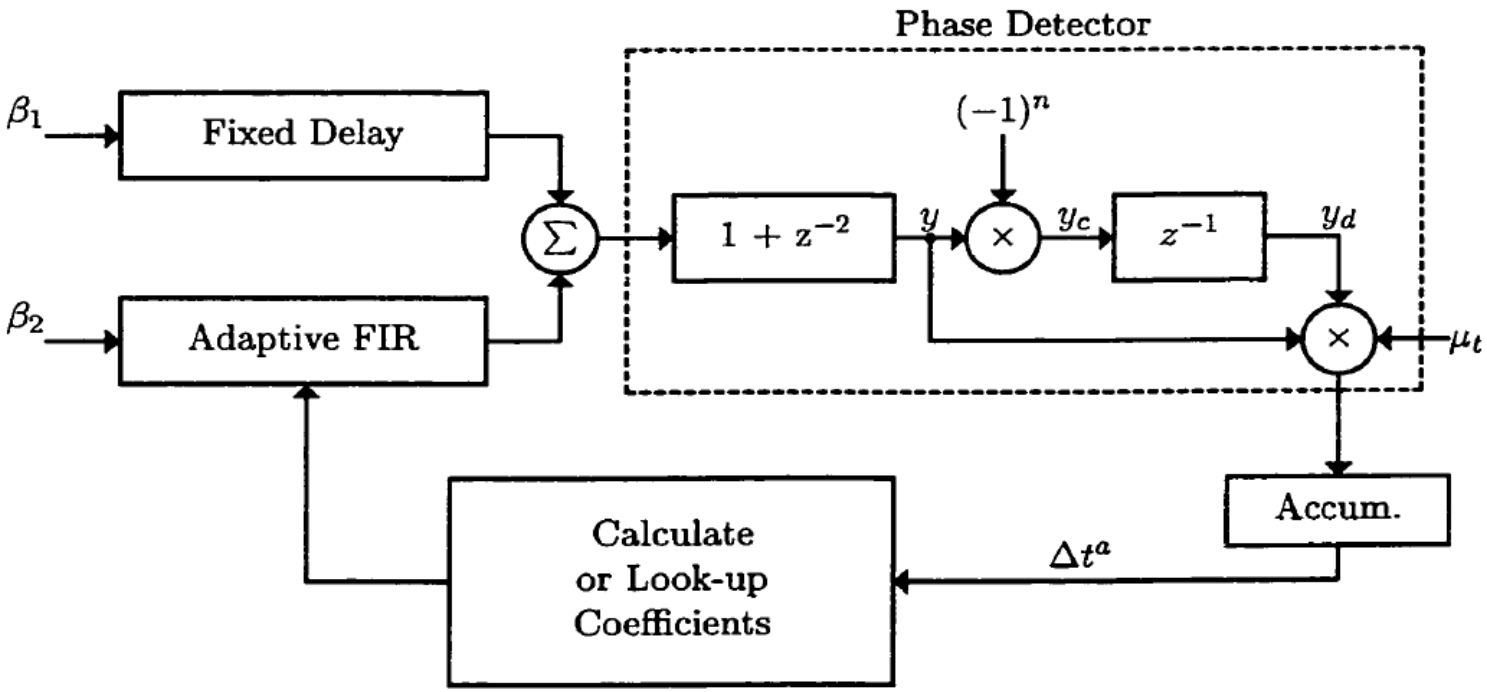


Figure 3.14: Block diagram of the adaptive sample-time calibration system.

[Jamal 2001]

- Requires fractional delay filter

Example 1 (2001)

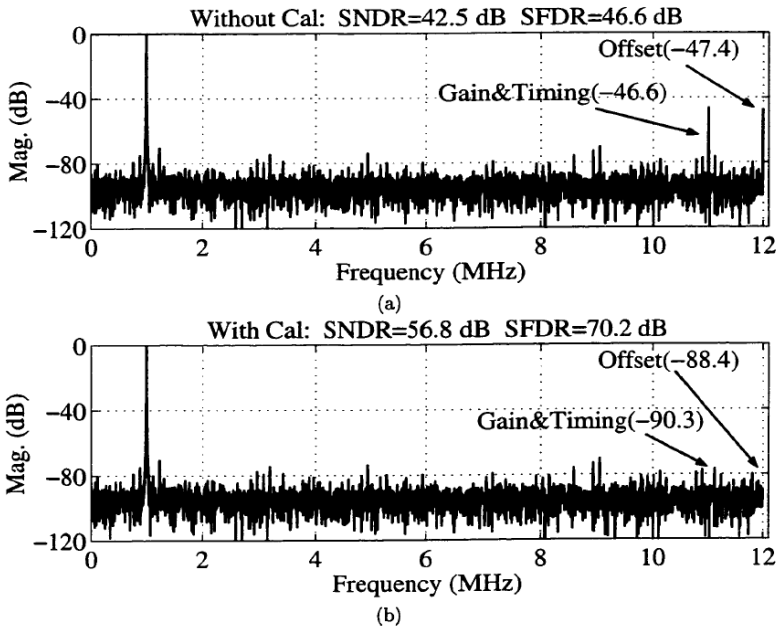


Figure 5.2: ADC output spectrum without calibration (a) and with calibration (b). (f_s = 120 MS/s, $V_{in} = 3$ V_{p-p}, $f_o = 0.99$ MHz)

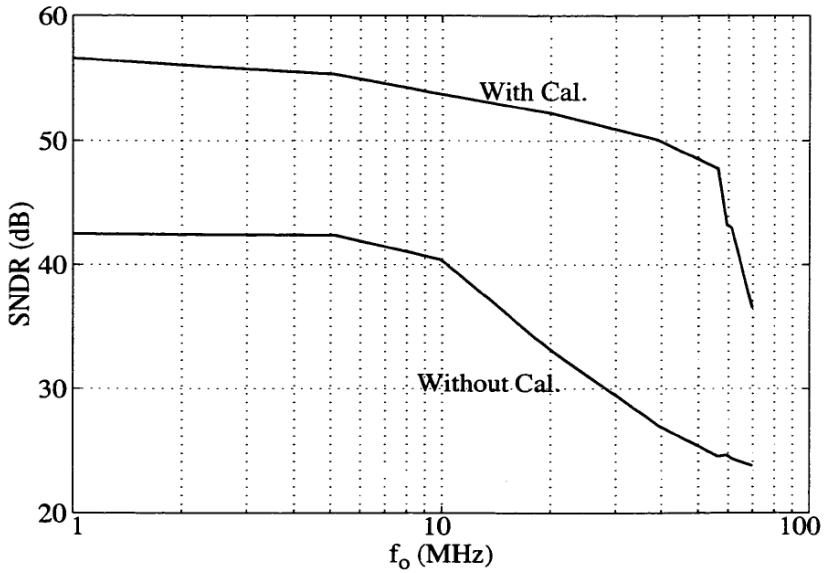
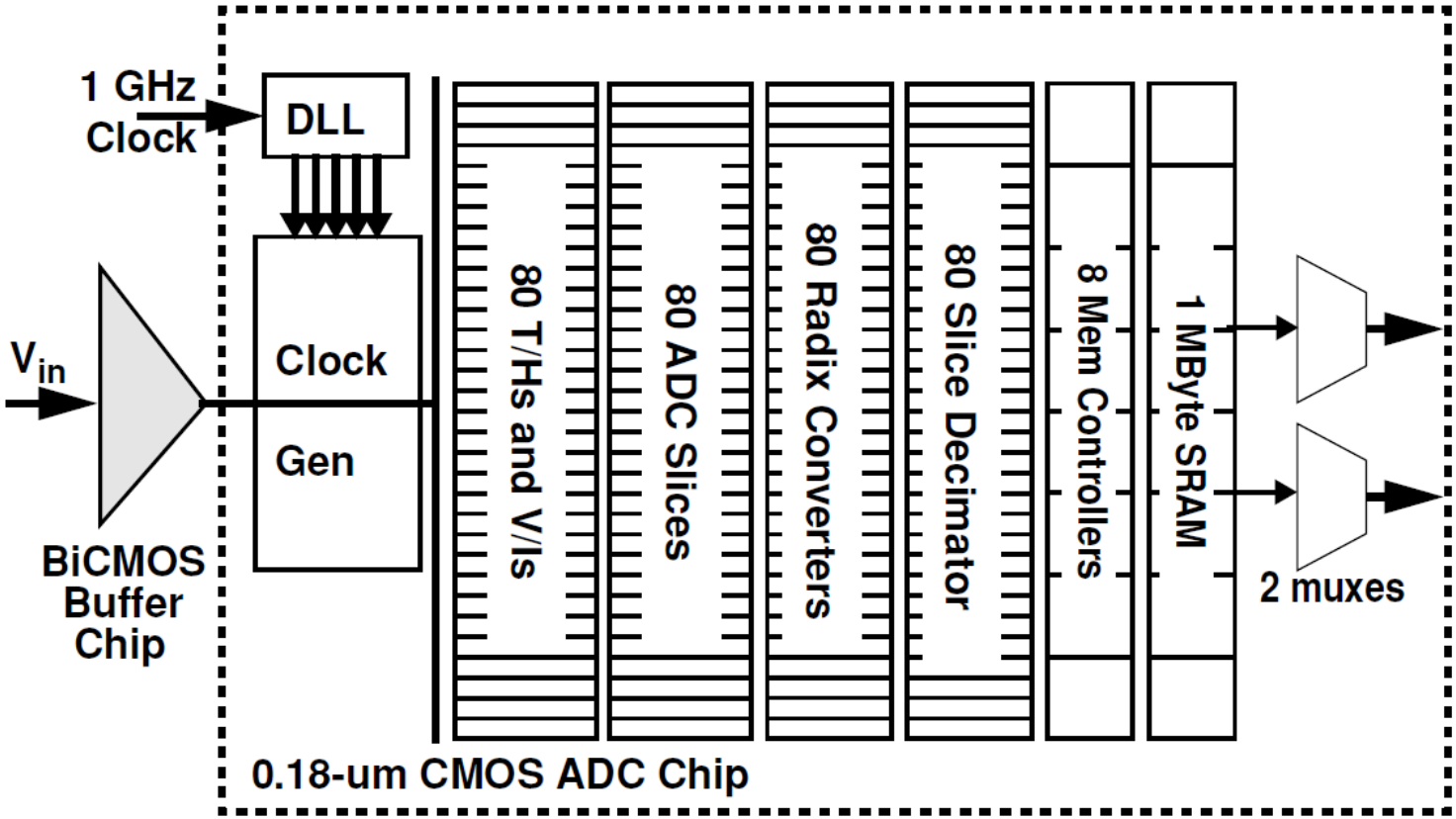


Figure 5.7: SNDR versus Input Frequency

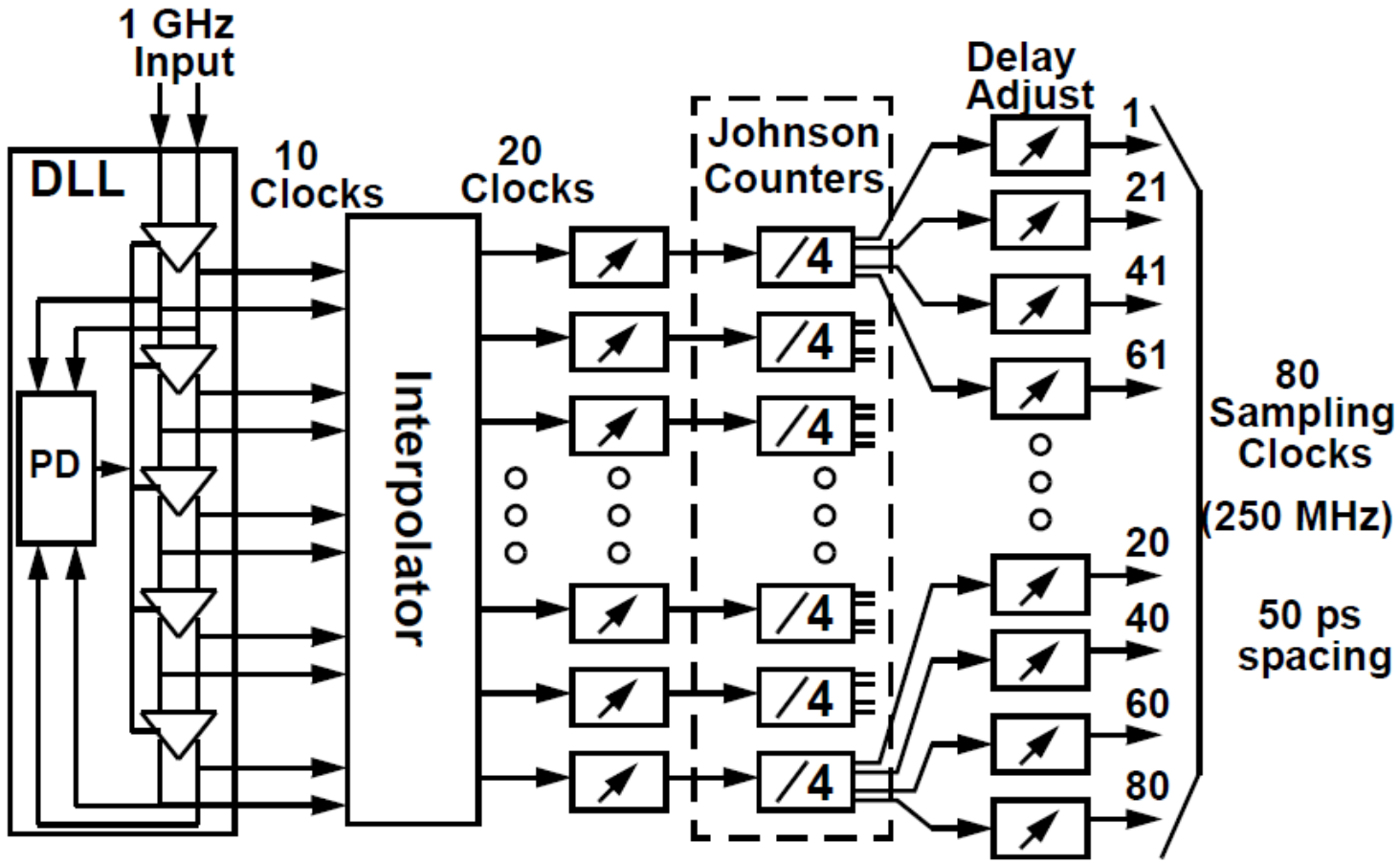
[Jamal 2001]

Example 2 (2003)



[Poulton 2003]

Example 2 (2003)



[Poulton 2003]

Example 2 (2003)

- Foreground calibration
- Apply pulse train with fast edges
- Use FFT to measure phase delay of T/H
- Adjust time delay
- Rinse and repeat

[Poulton 2003]

Example 3 (2005)

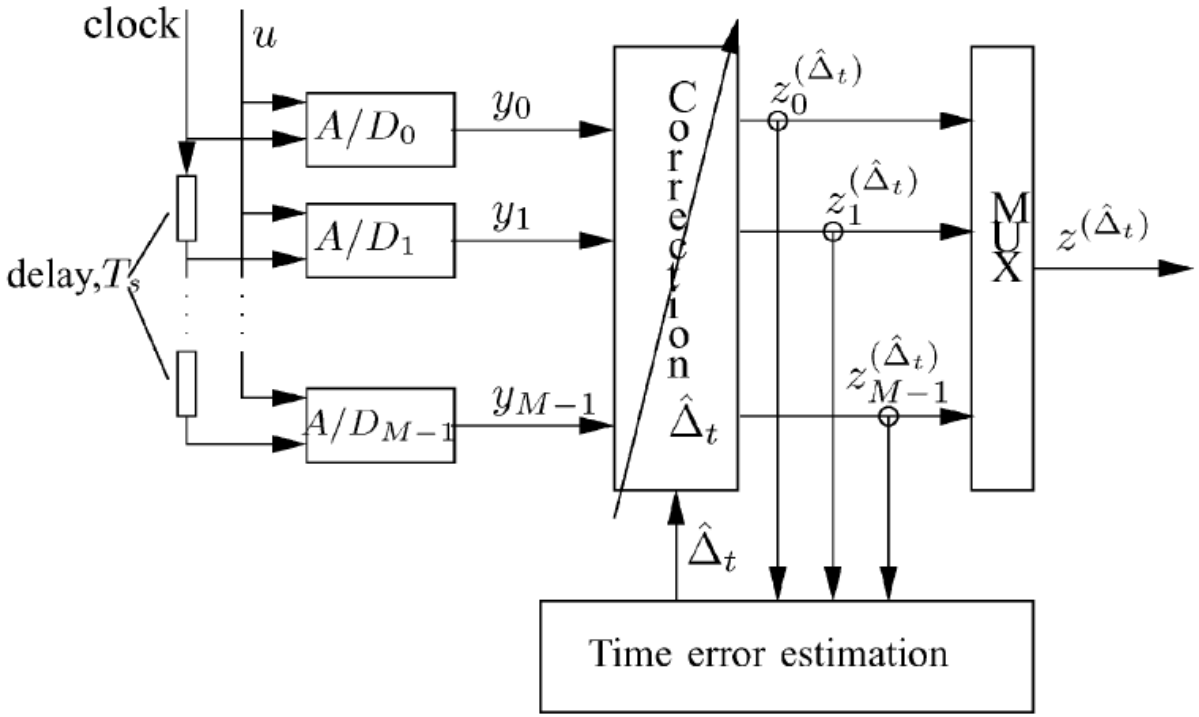


Fig. 6. Time-interleaved ADC system with time errors. The time errors $\hat{\Delta}_t$ are estimated by a blind adaptive algorithm and the signal is corrected by a filter.

[Elbornsson 2005]

- Digital and background calibration
- Uses cost function based on input statistics

Example 3 (2005)

$$\hat{\Delta}_t^{(i+1)} = \hat{\Delta}_t^{(i)} - \mu \frac{\nabla V\left(\hat{\Delta}_t^{(i)}\right)}{\max\left|\nabla V\left(\hat{\Delta}_t^{(i)}\right)\right|},$$

$$V(\Delta_t) = \sum_{l=0}^{\infty} \sum_{m=0}^{M-1} \sum_{i,j} \left(\left(R_z^{\Delta_t}\right)_{i,i-m}[l] - \left(R_z^{\Delta_t}\right)_{j,j-m}[l] \right)^2$$

[Elbornsson 2005]

- Use inverse DTFT to reconstruct signal using timing estimation
- Update timing estimation with cost function (i.e. has cost function decreased or increased?)
- Requires bandlimited signal (common limitation to many blind calibration algorithms)

Example 4 (2008)

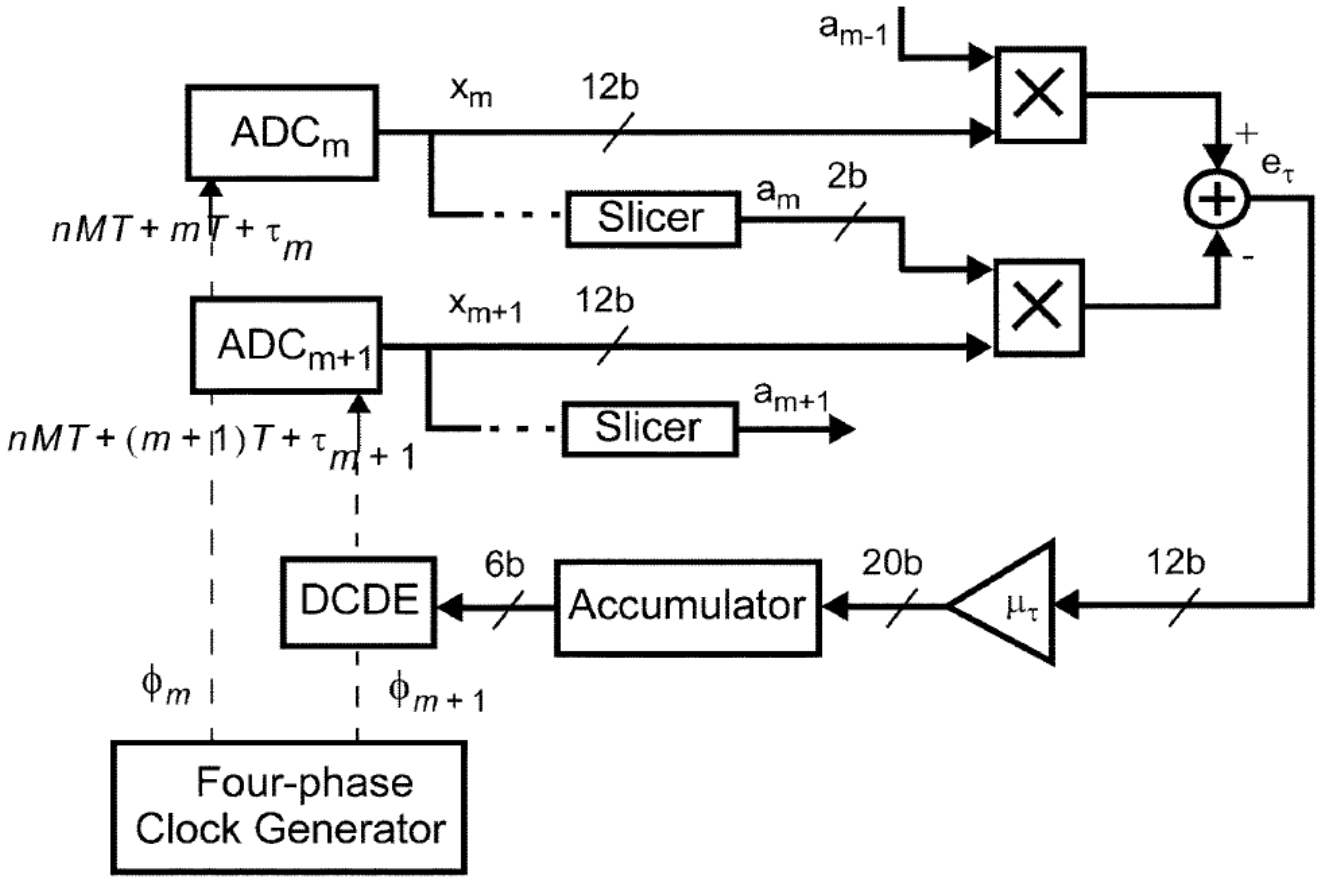


Fig. 3. Sample-time error calibration between two adjacent channels.

[Haftbaradaran 2008]

Example 4 (2008)

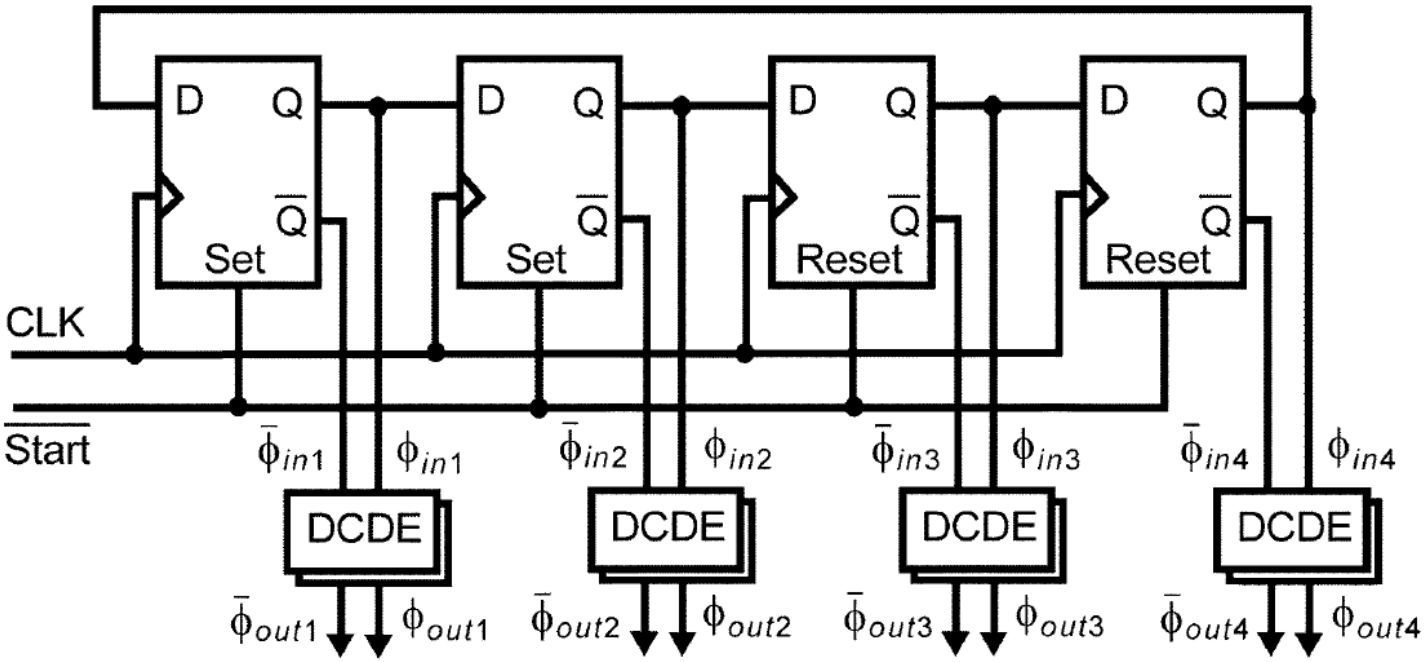


Fig. 5. Four-phase clock generator and DCDEs.

[Haftbaradaran 2008]

Example 4 (2008)

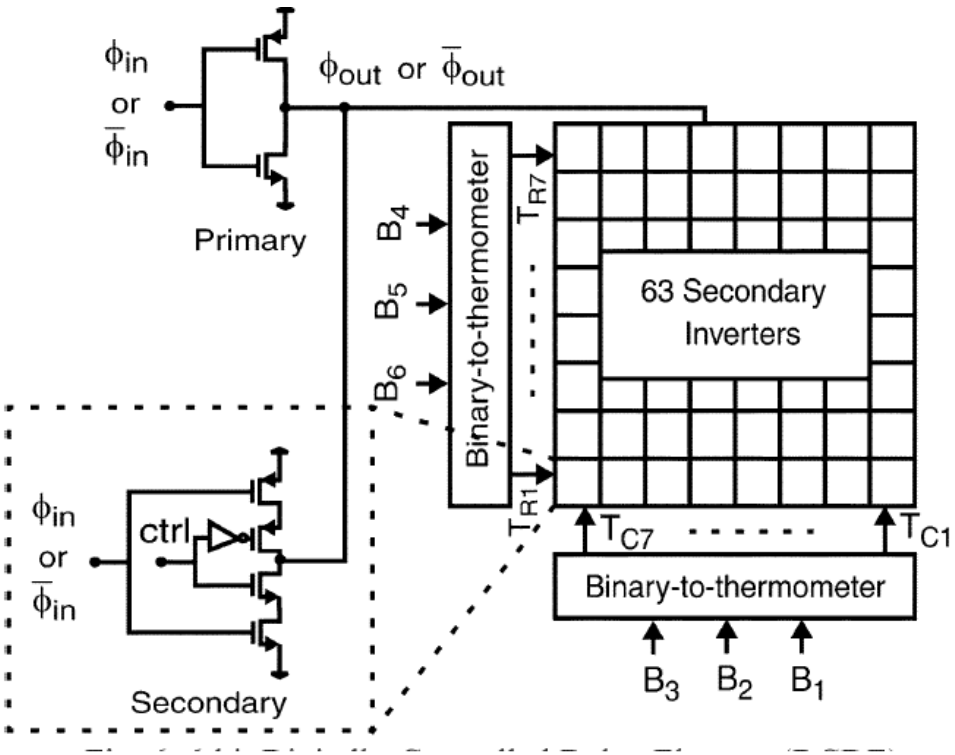


Fig. 6. 6-bit DCDE.

[Haftbaradaran 2008]

- Has 0.86 ps delay change (on average)

Example 4 (2008)

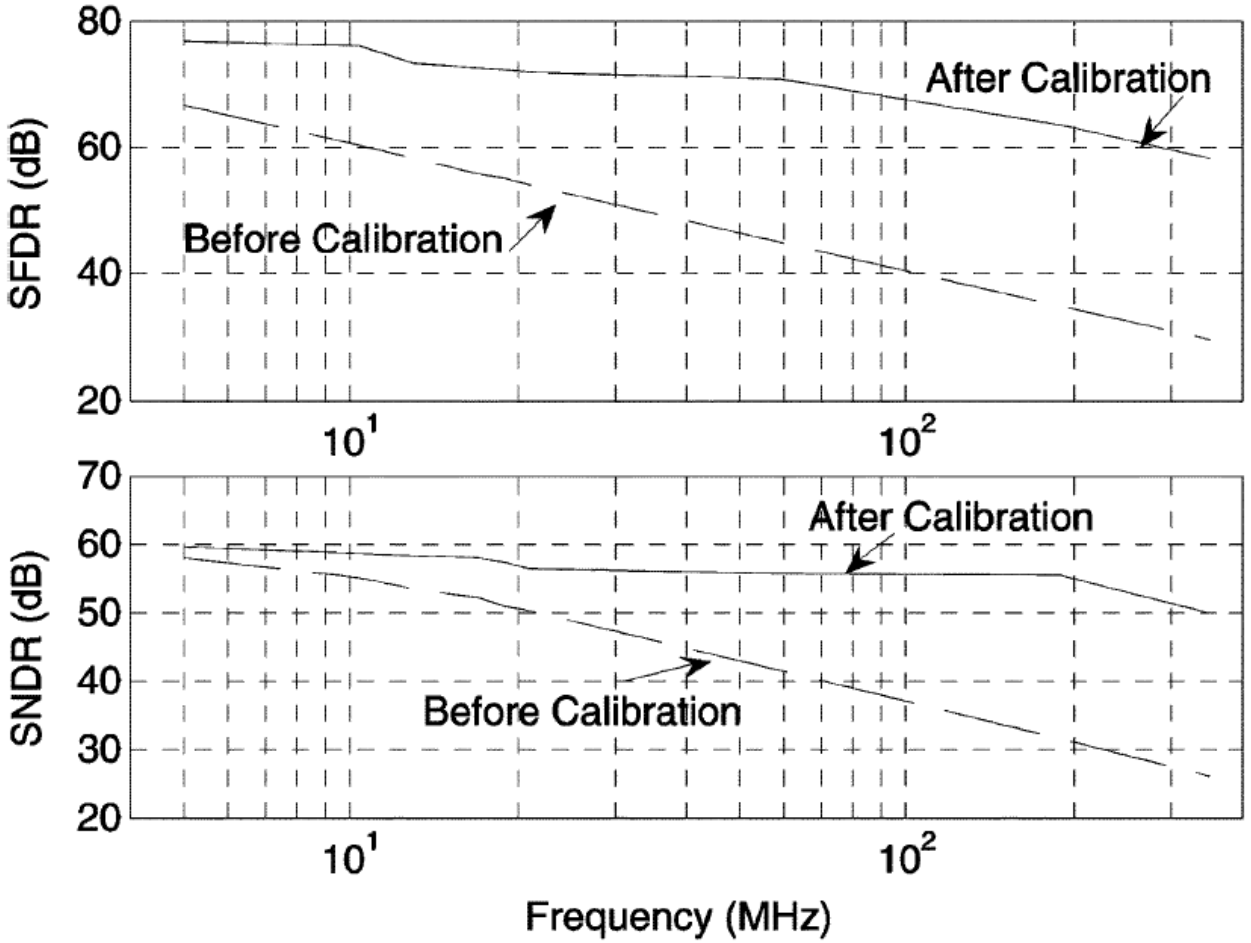
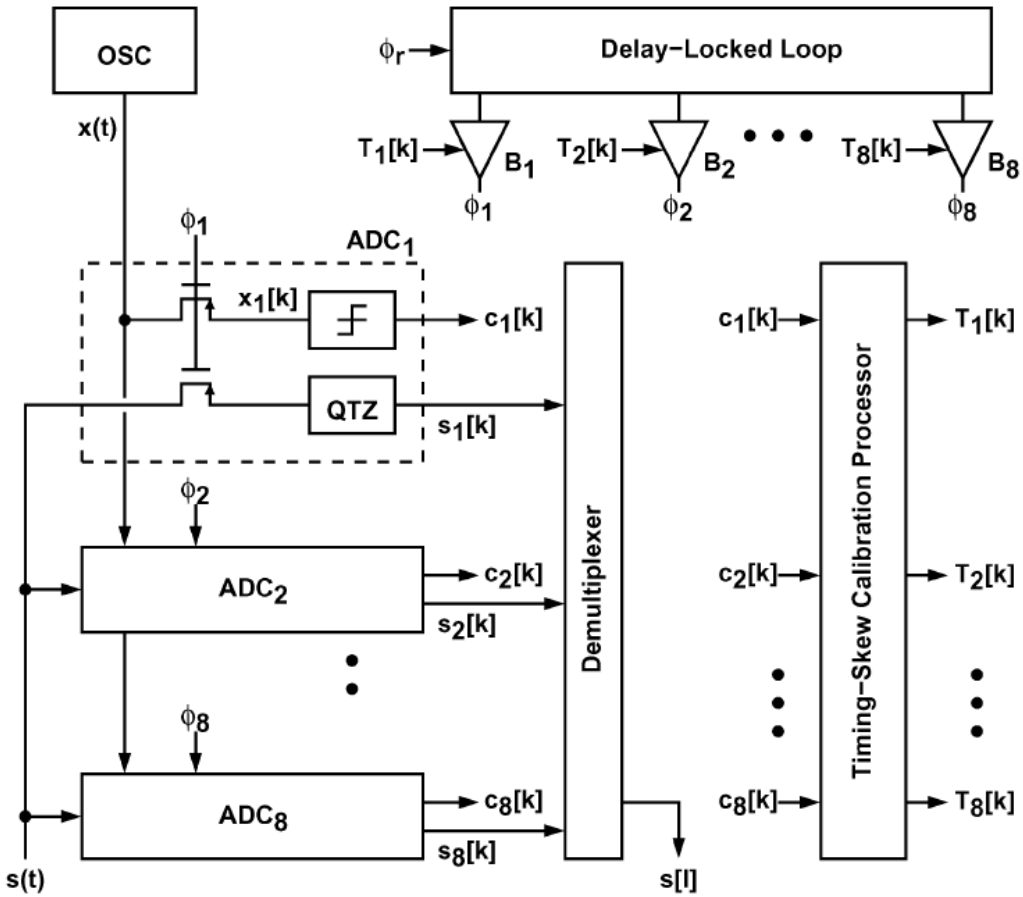


Fig. 10. SFDR and SNDR of the ADC versus the frequency of the input signal, before and after sample-time error calibration.

[Haftbaradaran 2008]

Example 5 (2010)



[Huang 2010]

- 6-bit 16 GS/s flash ADC

Example 5 (2010)

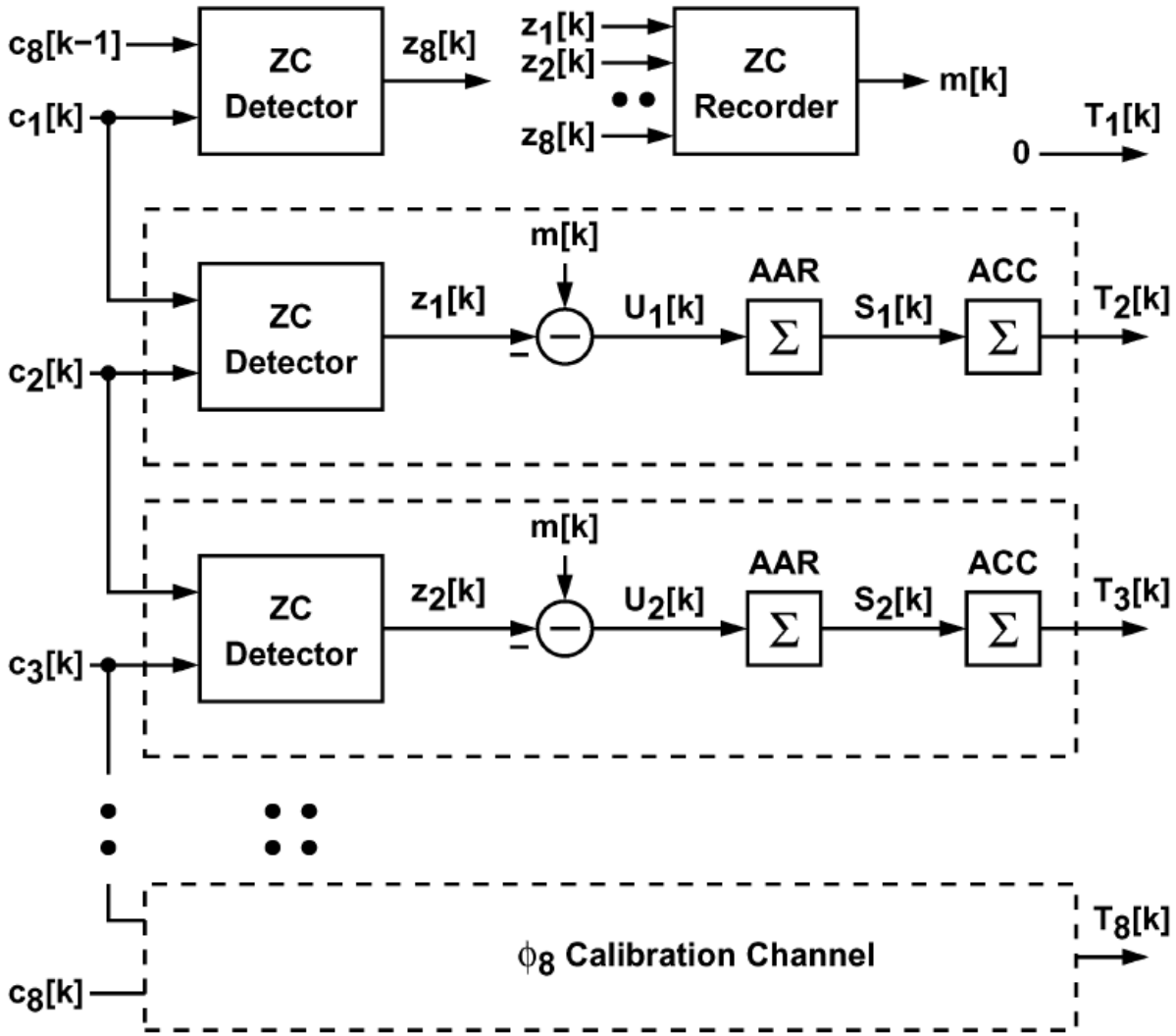


Fig. 10. Timing-skew calibration processor (TSCP).

[Huang 2010]

Example 5 (2010)

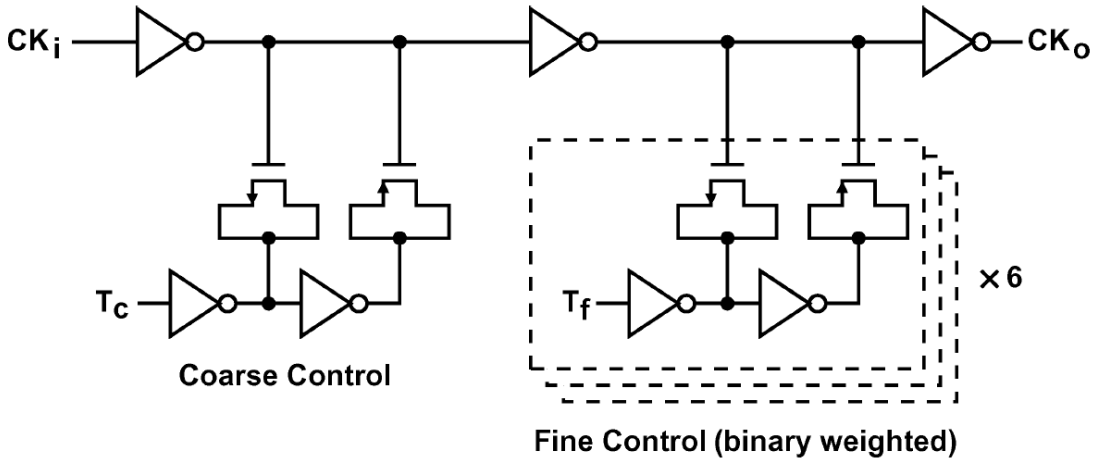
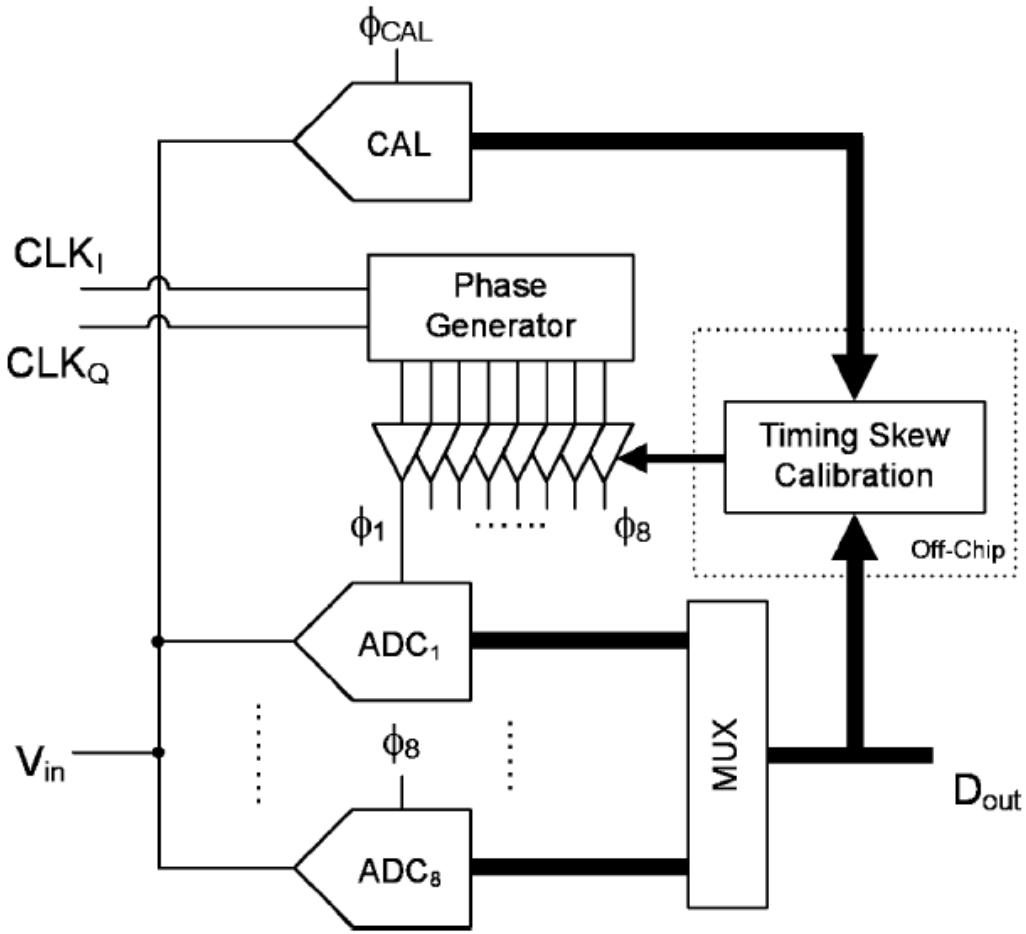


Fig. 15. Digitally-controlled variable-delay clock buffer.

[Huang 2010]

- Change capacitive load on delay cells (similar to [Poulton 2003])

Example 6 (2010)



[El-Chammas 2010]

- 5-bit 12 GS/s
- Add extra channel (used 1-bit ADC in implementation)

Example 6 (2010)

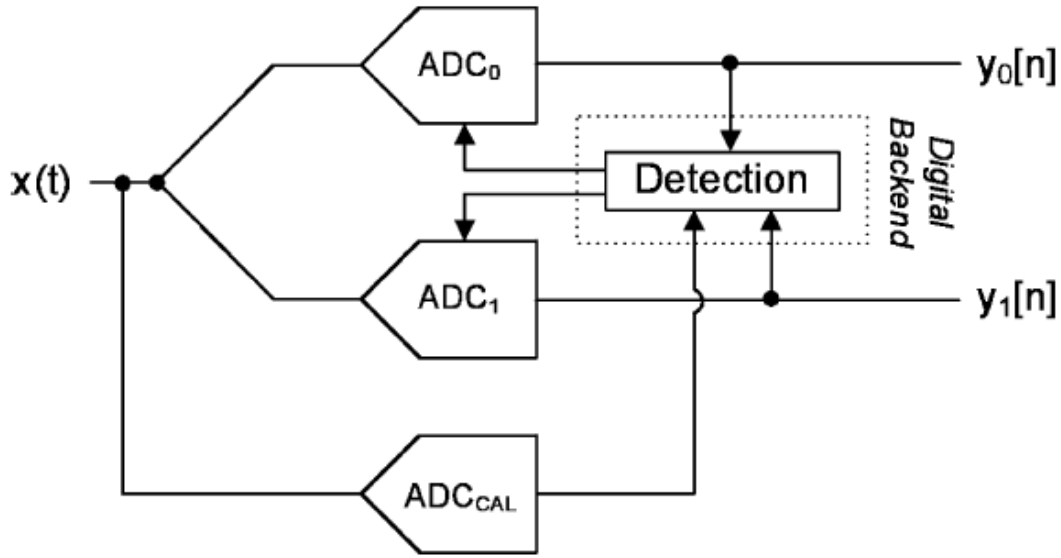


Fig. 8. Adding an auxiliary ADC to a 2-channel time-interleaved ADC.

Example 6 (2010)

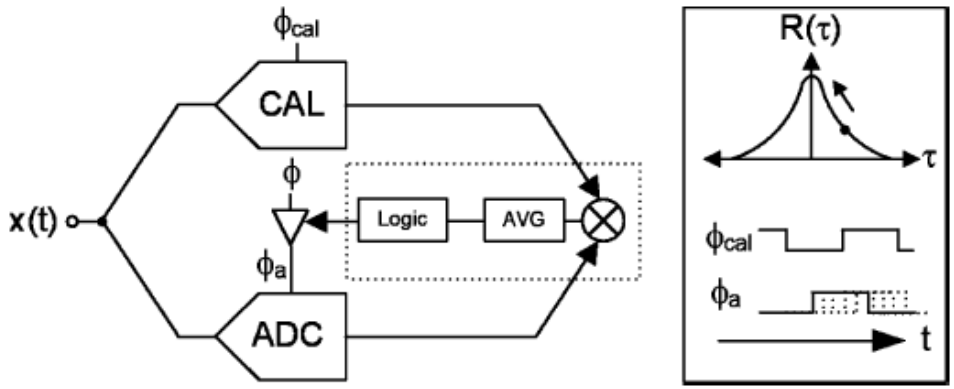


Fig. 9. Timing adjustment to maximize the correlation between a sub-ADC and the auxiliary ADC.

- Maximize correlation between extra ADC and each sub-ADC by adjusting delay cell

Example 6 (2010)

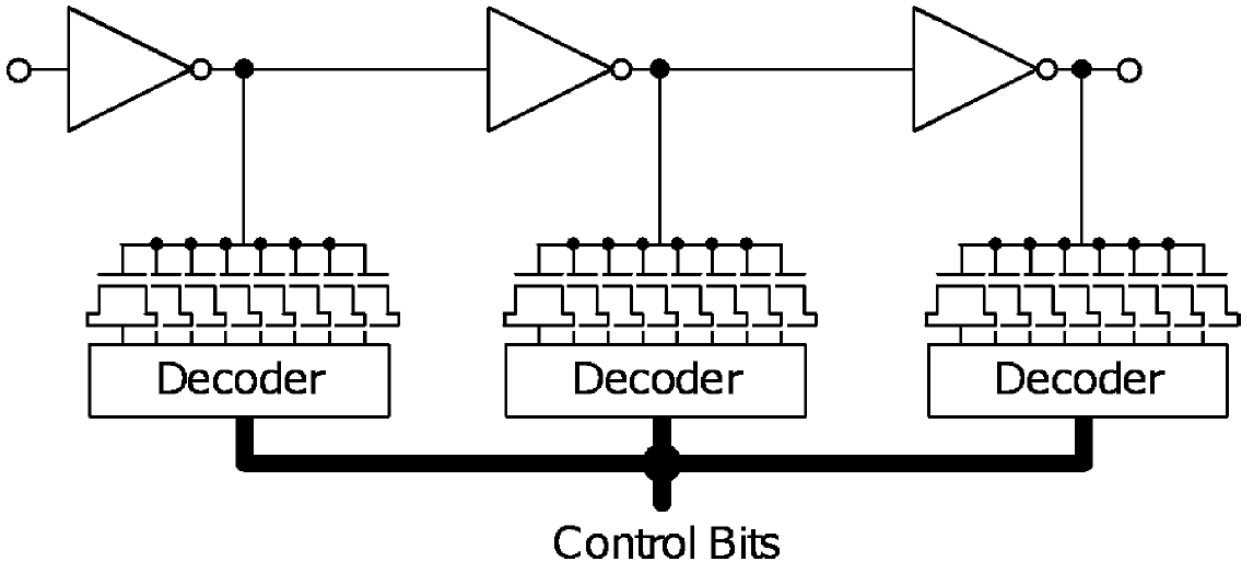


Fig. 18. Complete delay line.

- Adjust delay cell load (around 0.3 ps resolution)

Example 6 (2010)

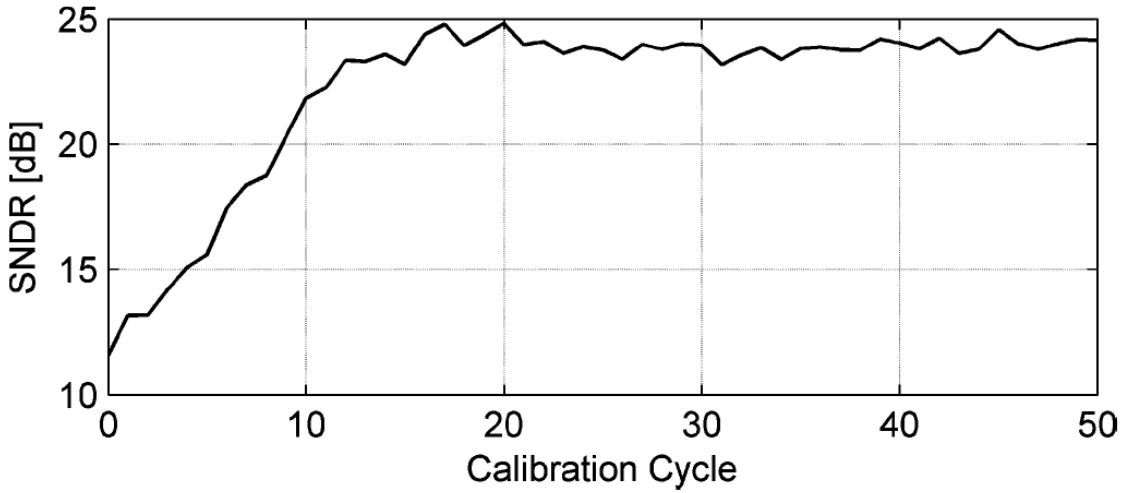


Fig. 25. SNDR during convergence of the timing skew calibration algorithm with 500,000 samples per calibration cycle.

- Several hundred milliseconds for initial convergence

Example 7 (2011)

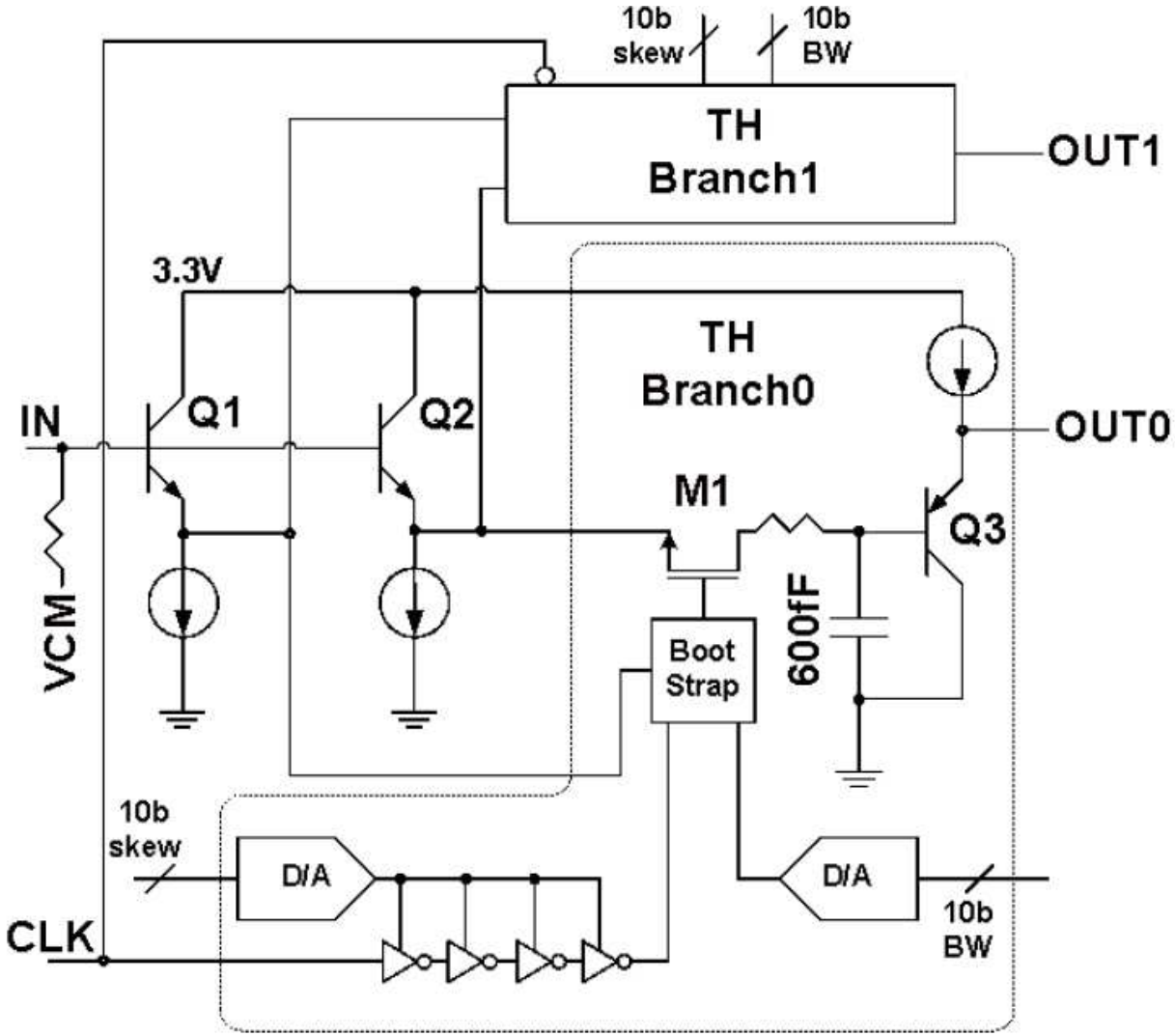


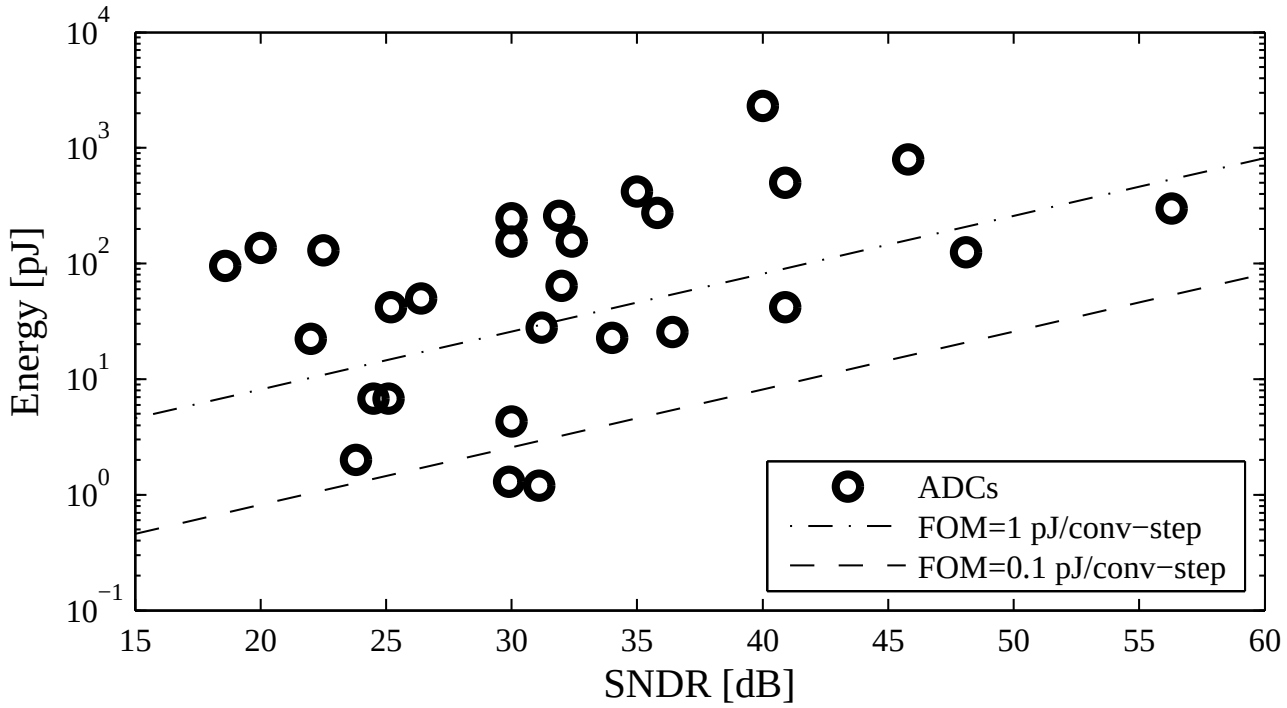
Figure 10.2.2: Input buffers, and track and hold.

[Payne 2011]

And many more ...

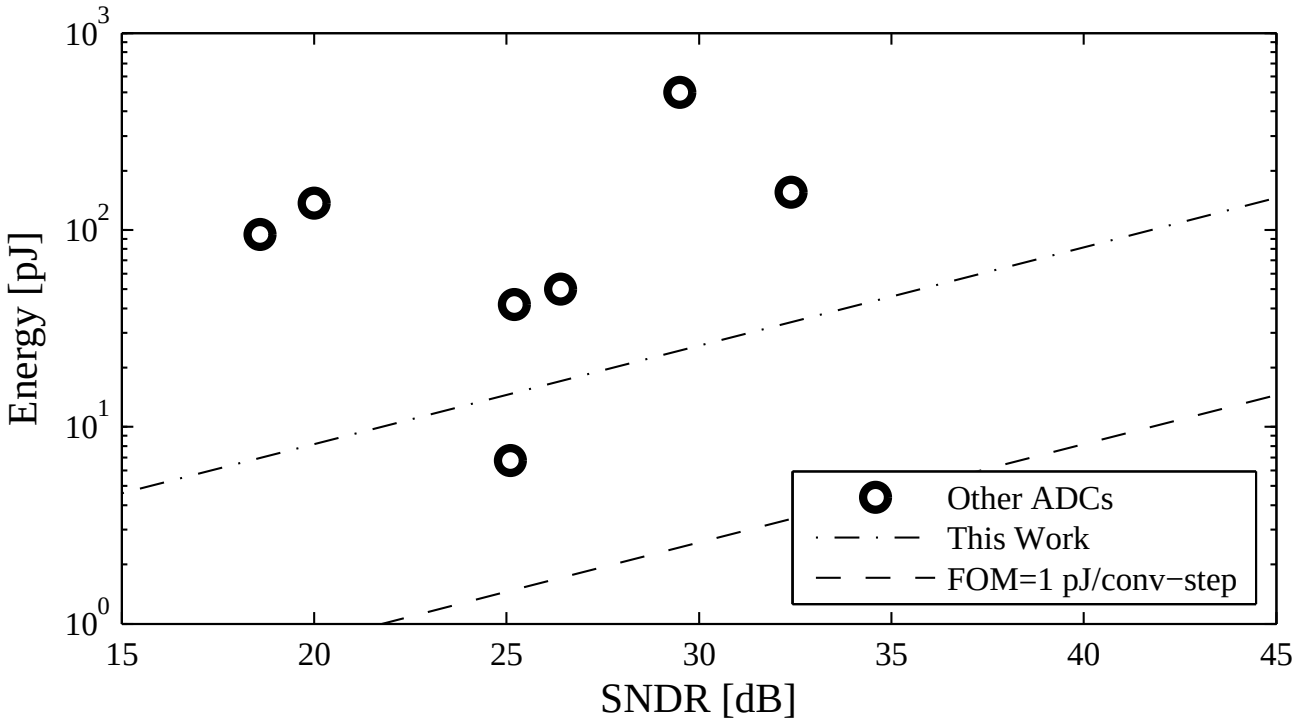
- There are many more approaches for timing skew calibration
- Some require energy free bands, and others don't
- Some use fractional delay filters, and others tune delay with delay cells
- There is much research in both the estimation and correction blocks

Current time-interleaved ADCs



- ADCs faster than 1 GS/s (published in ISSCC and VLSI)

Current time-interleaved ADCs



- ADCs faster than 10 GS/s

Making sense of the noise

- Can either minimize mismatch through careful design and layout
- Or can use calibration
- "Optimal" type of calibration is application and system dependent
- Be careful of throwing everything at the digital backend
- A lot of room for future research

Making sense of the noise

- What are some common themes?
- Some operations are better done in digital
- Others are better in analog
- Co-optimization of calibration and circuit design

Summary

- Time-interleaved ADCs important in pushing performance
- Time-varying errors set performance limitations
- System-level analysis improves design space specifications (e.g. mismatch constraints and ADC architecture)
- Calibration techniques extremely useful in compensating for errors

Questions

- **Email**: manar@ti.com, manar.chammas@gmail.com

Thank you

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