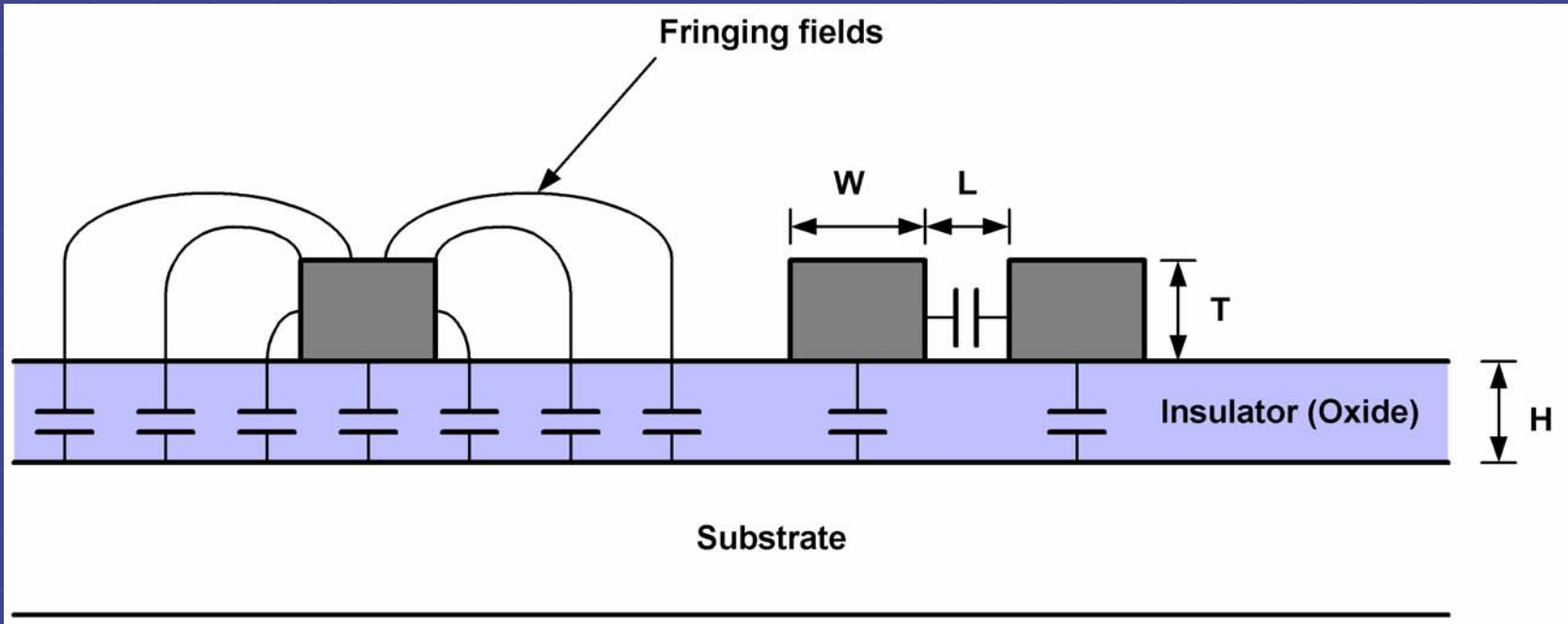
Chapter 7 Layout of Capacitor

- Routing Capacitance
- Capacitance
- Capacitor Variability
- Capacitor Parasitics
- Comparison of Available Capacitors
- Layout of Capacitors
- Varactors

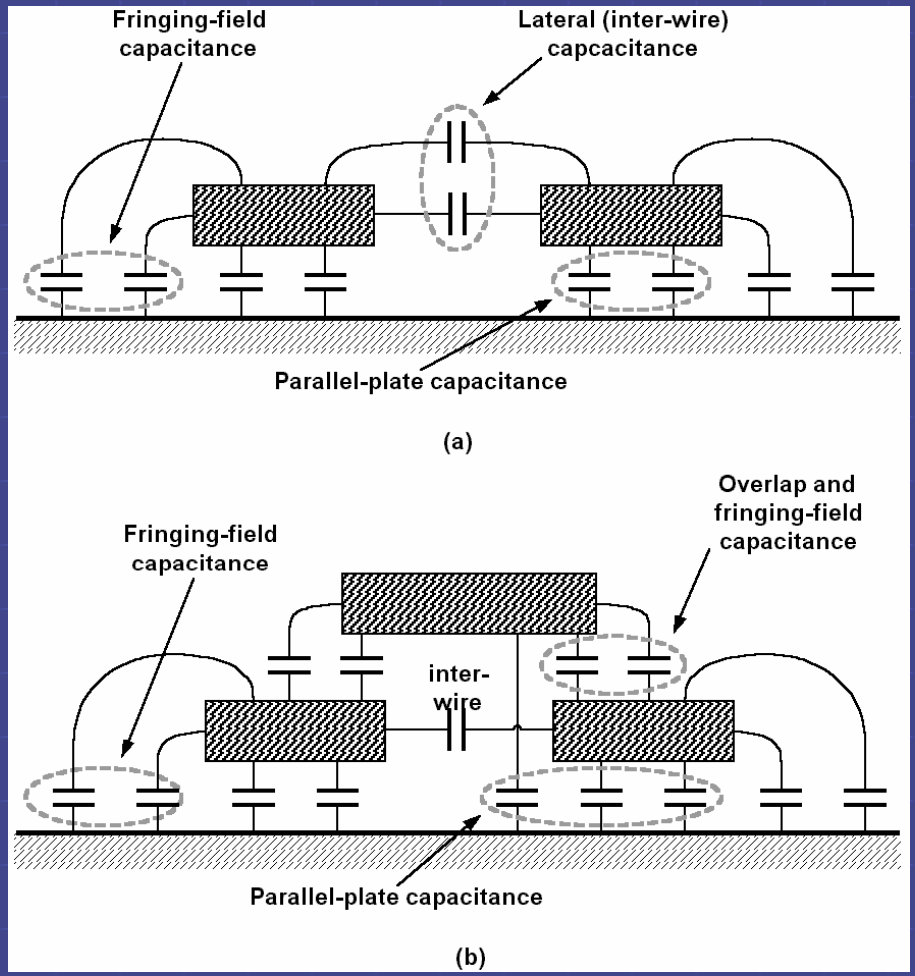
Routing Capacitance

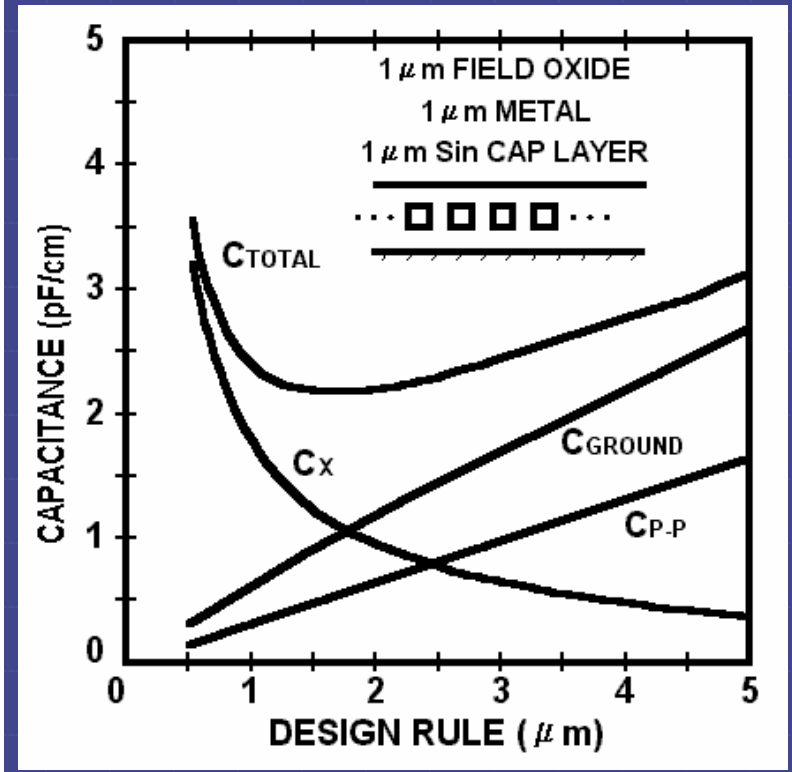


two components

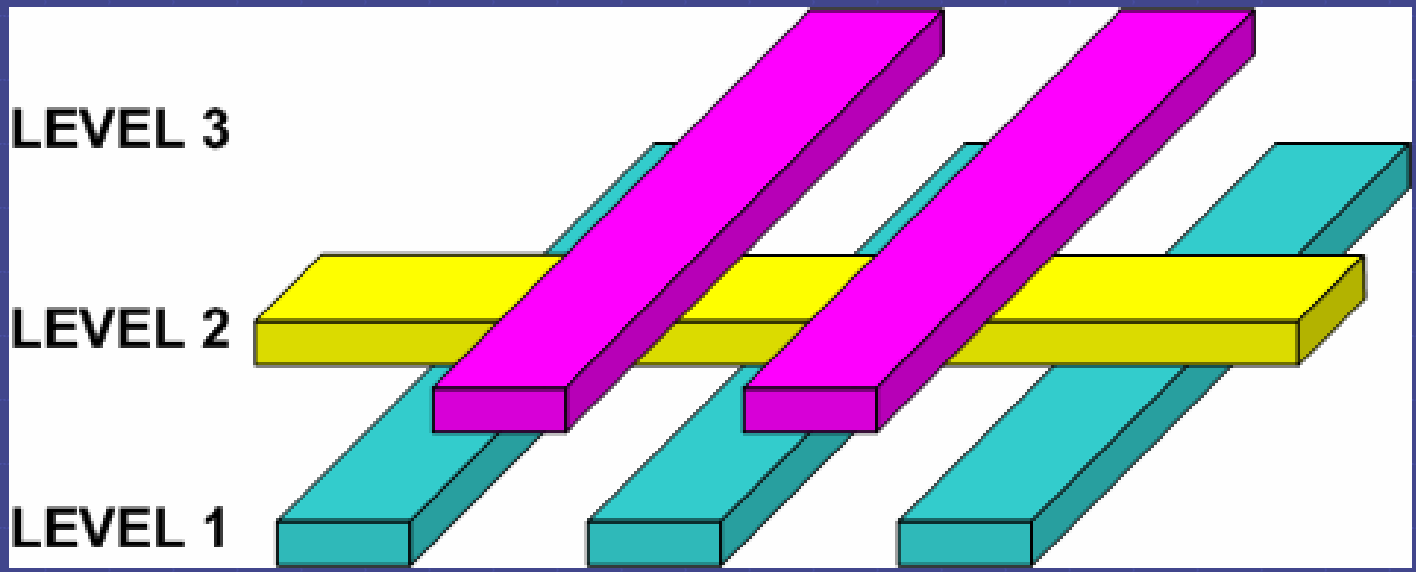
- parallel-plate capacitance
- fringing field

Capacitive Coupling Components



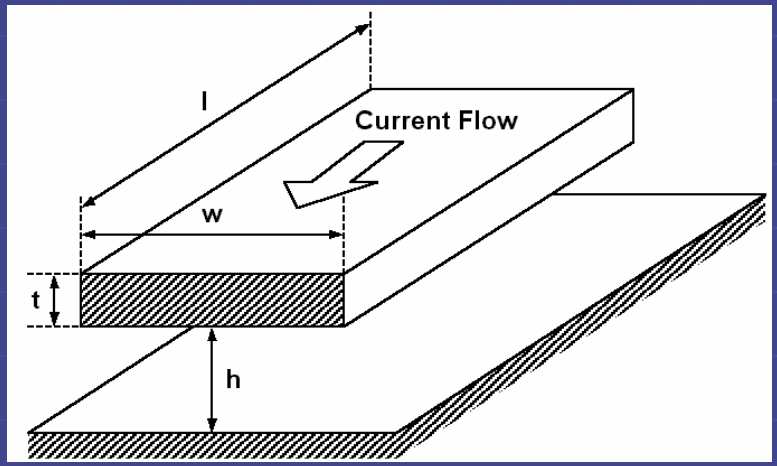


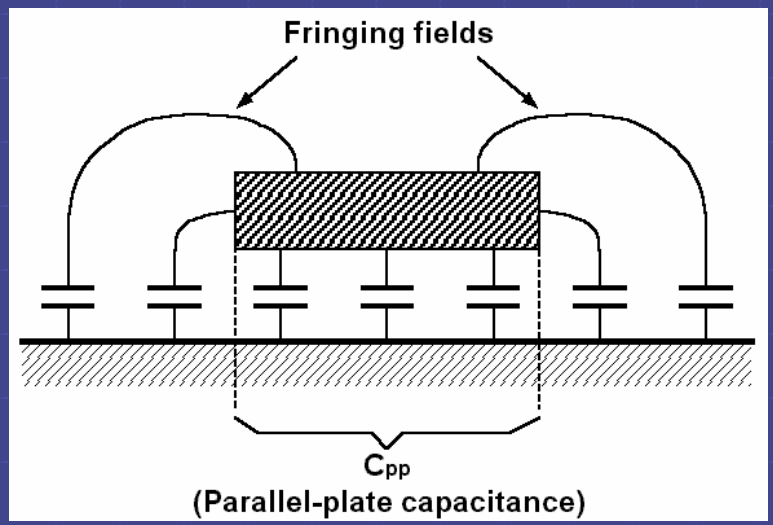
Interconnects Routing

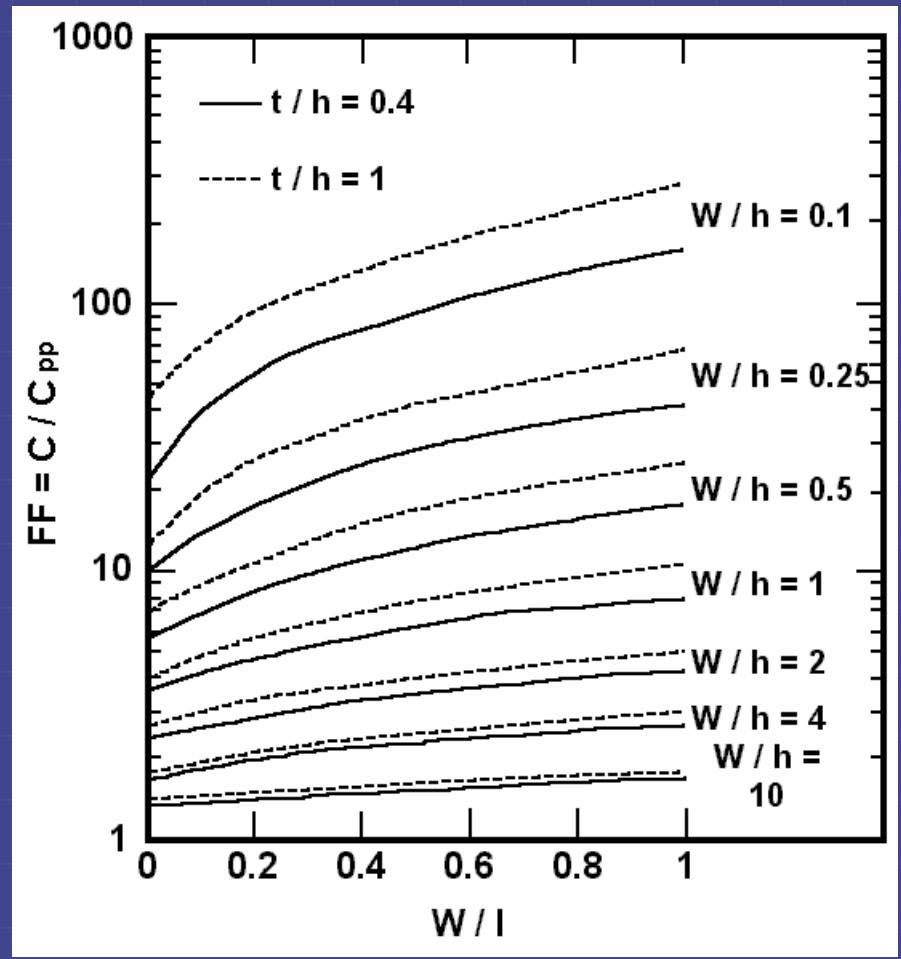


Each layer is perpendicular to its bottom and top layer to reduced overlapped capacitance and increase complexity of wire routing.

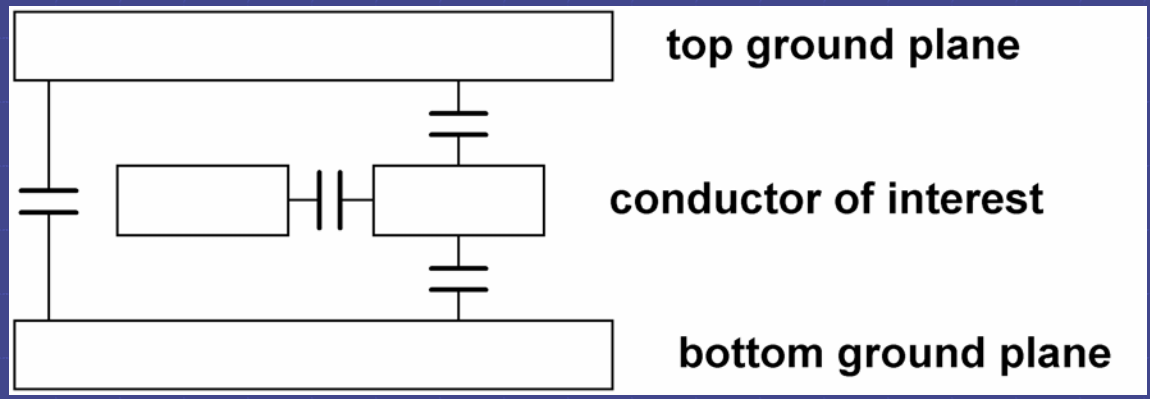
Variation of Fringing-Field Factor



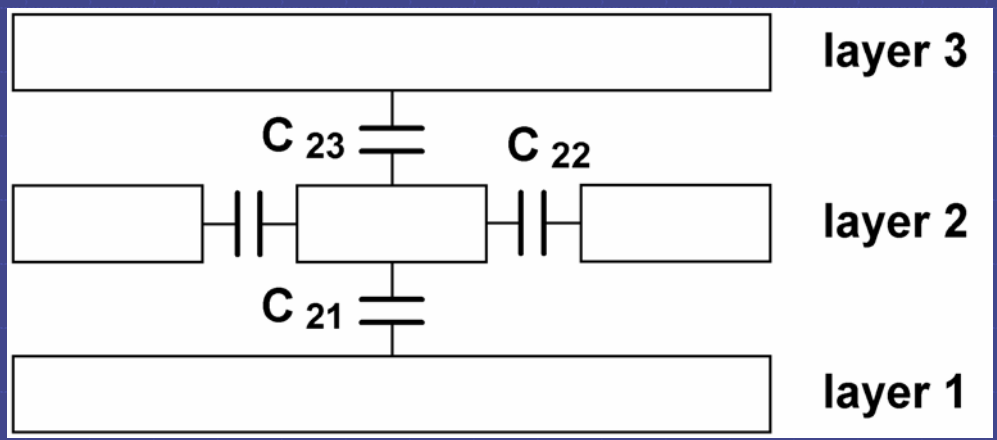




Multiple Conductor Capacitance



three conductor layer
- top ground plane
- conductor of interest
- bottom ground layer



$C_2 = C_{21} + C_{23} + C_{22}$

where

C_2: middle layer 2 to ground

C_{21}: middle layer 2 to layer I

C_{23}: middle layer 2 to layer 3

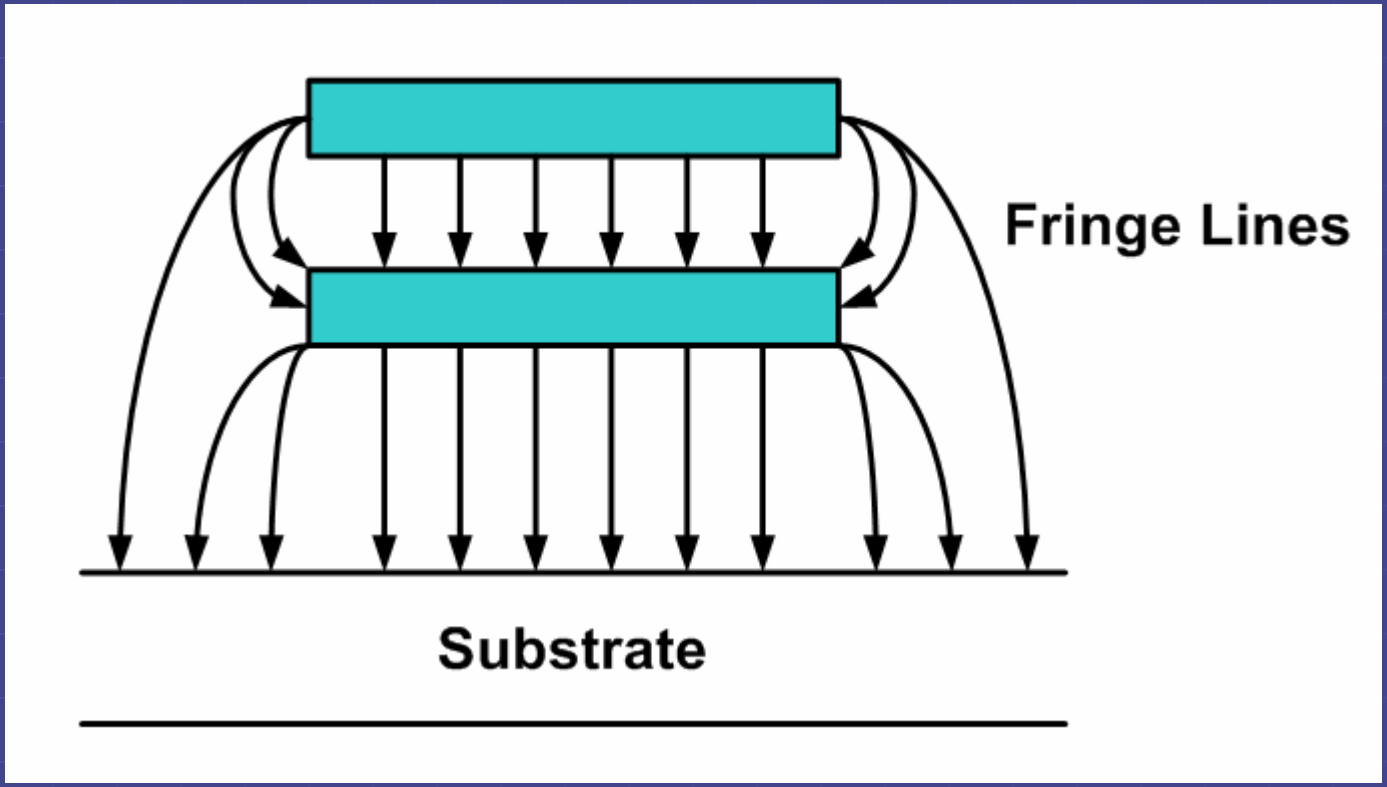
C_{22}: capacitance between other parallel conductor on layer 2

C_{21} and C_{23} given by formula for crossover capacitance

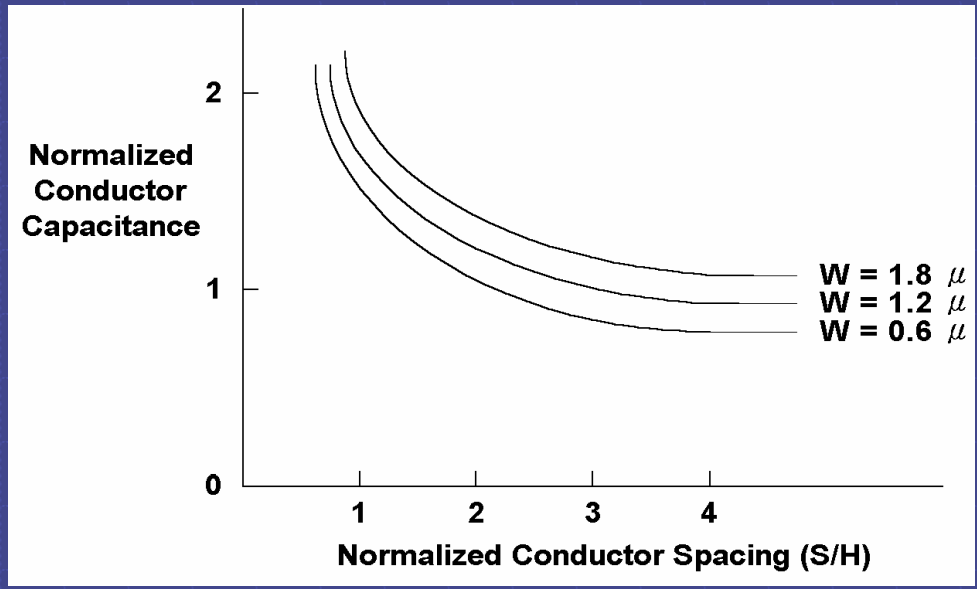
C_{22} affected by the presence or absence of layer-1 and layer-3

C_{22} total capacitance of layer-2 to layer-2 capacitance

Fringe Component of Capacitance



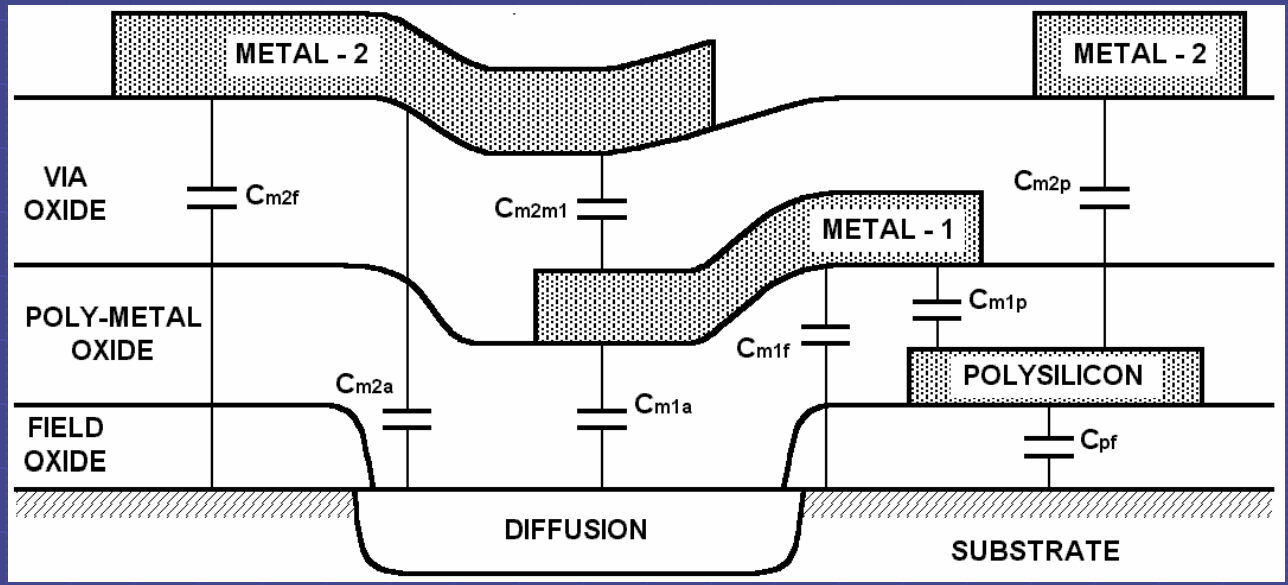
Conductor Capacitance vs. Spacing



- Calculated directly from parameters, complicated for large circuits
- weight factor model, depends on thickness and separation
- missing neighbor model, look-up table, detect the presence or absence of adjacent conductor segments,
- drawn dimension, actual dimension after process, dielectric thickness variation

★ maximum width and minimum thickness for delay and power calculation
★ minimum width and maximum thickness dielectric for race calculation
★ minimum width of conductors for RC delay calculation

Parasitic Capacitance Values in 0.8um Process



Poly over field oxide	C_{pf}	Area	0.066	fF / μm^2
		Perimeter	0.046	fF / μm
Metal - 1 over field oxide	C_{m1f}	Area	0.030	fF / μm^2
		Perimeter	0.044	fF / μm
Metal - 2 over field oxide	C_{m2f}	Area	0.016	fF / μm^2
		Perimeter	0.042	fF / μm
Metal - 1 over poly	C_{m1p}	Area	0.053	fF / μm^2
		Perimeter	0.051	fF / μm
Metal - 2 over poly	C_{m2p}	Area	0.021	fF / μm^2
		Perimeter	0.045	fF / μm
Metal - 2 over Metal - 1	C_{m2m1}	Area	0.035	fF / μm^2
		Perimeter	0.051	fF / μm

Process Parameters

Field oxide thinckness	0.52	μm	
Gate oxide thinckness	16.0	μm	(= 0.016 μm)
Polysilicon thinckness	0.35	μm	(minimum width 0.8 μm)
Poly - metal oxide thinckness	0.65	μm	
Metal - 1 thinckness	0.60	μm	(minimum width 1.4 μm)
Via oxide thinckness	1.00	μm	
Metal - 2 thinckness	1.00	μm	(minimum width 1.4 μm)
n+ junction depth	0.40	μm	
p+ junction depth	0.40	μm	
n - well junction depth	3.50	μm	

Poly over field oxide	C_{pf}	Area	0.066	fF / μm^2
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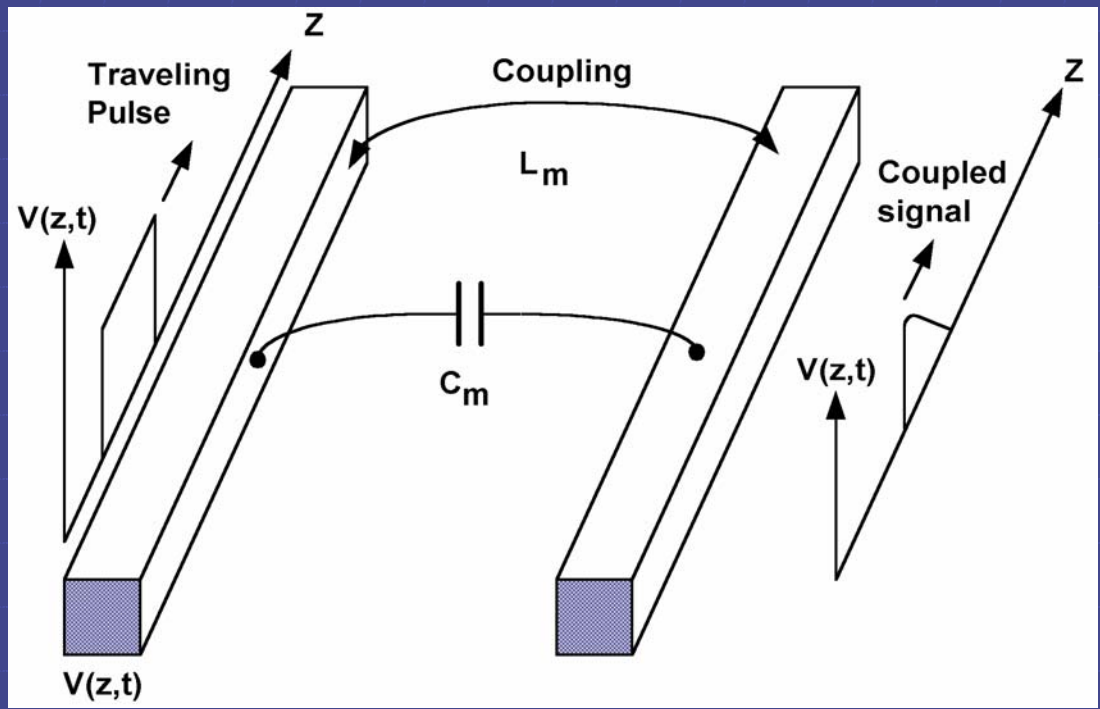
Cross Talk

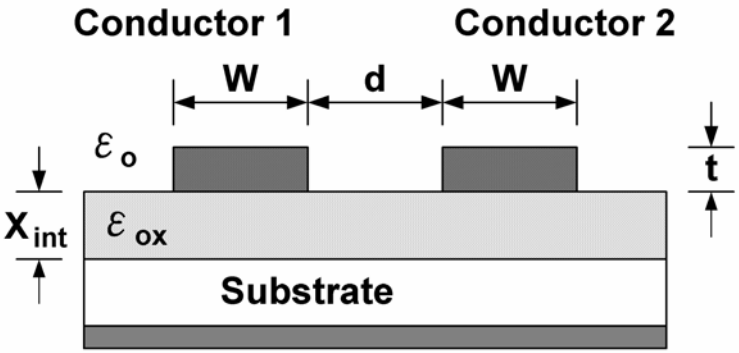


line-to-line parasitic capacitance C_m

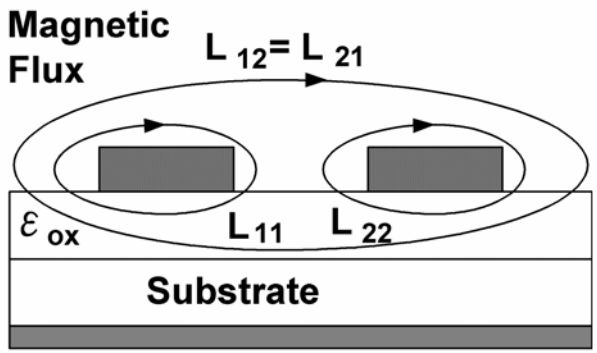
mutual inductance L_m

- Troublesome problem in high-density layout
- Incorrect or false transition may occur.

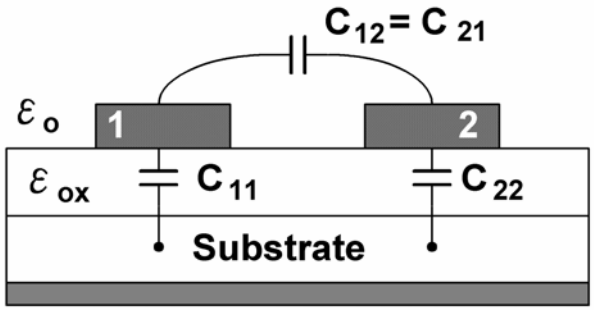
Cross Talk



(a) Cross-Section



(c) Inductive Coupling



(c) Capactive Coupling

$$Q_1 = C_{11}V_1 + C_{12}(V_1 - V_2)$$
$$Q_2 = C_{21}(V_2 - V_1) + C_{22}V_2$$

$$\Phi_1 = L_{11}I_1 + L_{12}I_2$$
$$\Phi_2 = L_{21}I_1 + L_{22}I_2$$

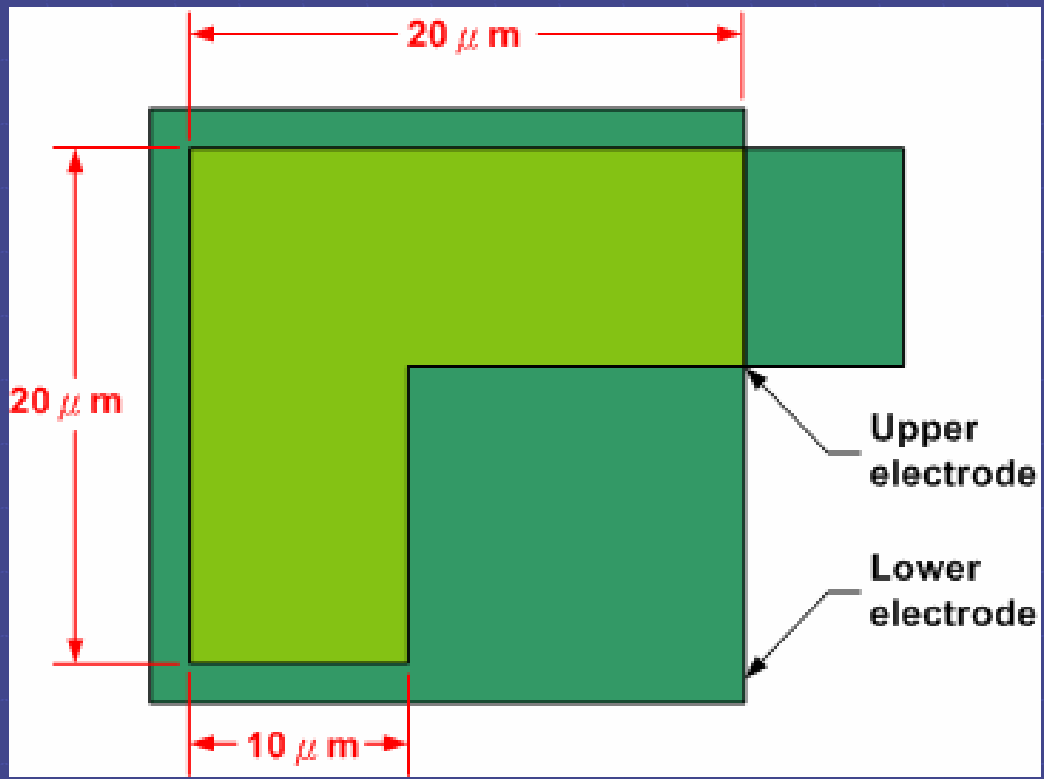
$I = dQ/dt$ $\quad C_m = C_{12} = C_{21}$ $\quad V = d\Phi/dt$ $\quad L_m = L_{12} = L_{21}$

$$I_1 = C_{11}\, dV_1/dt + C_m\, d(V_1 - V_2)/dt \qquad V_1 = L_{11}\, dI_1/dt + L_m\, dI_2/dt$$
$$I_2 = C_m\, d(V_2 - V_1) + C_{22}\, dV_2/dt \qquad V_2 = L_m\, dI_1/dt + L_{22}\, dI_2/dt$$

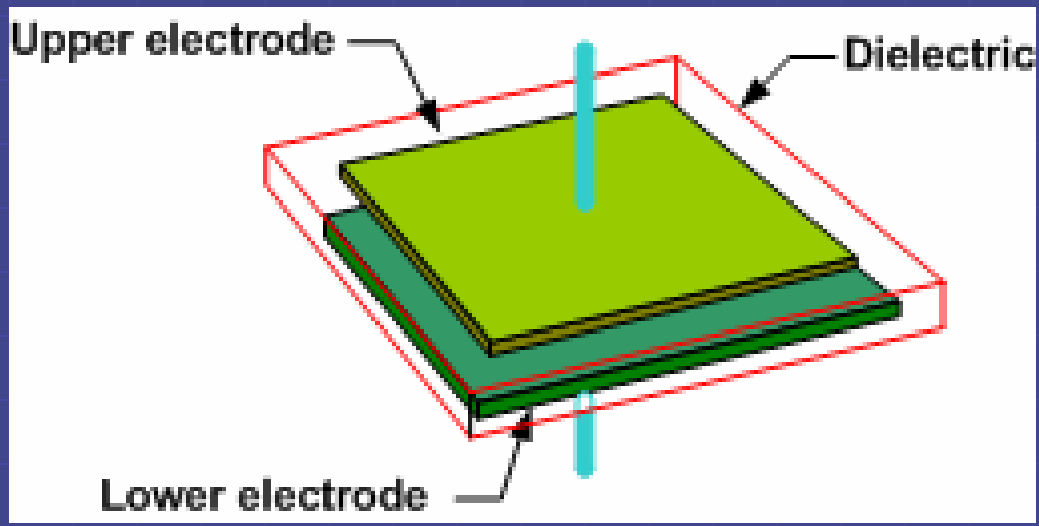
Relative permittivities and dielectric strengths of selected materials

Material		Relative Permittivity (Vacuum=1)	Dielectric Strength (MV/cm)
Silicon		11.8	30
Silicon dioxide (SiO_2)	Dry oxide	3.9	11
	Plasma	4.9	3~6
	TEOS	4.0	10
Silicon nitride (Si_3N_4)	LPVCD	6~7	10
	Plasma	6~9	5

Hypothetical example of a thin – film capacitor. The crosshatched region where the two plates intersect forms the effective area of the capacitor plates, or in this case 300um^2.

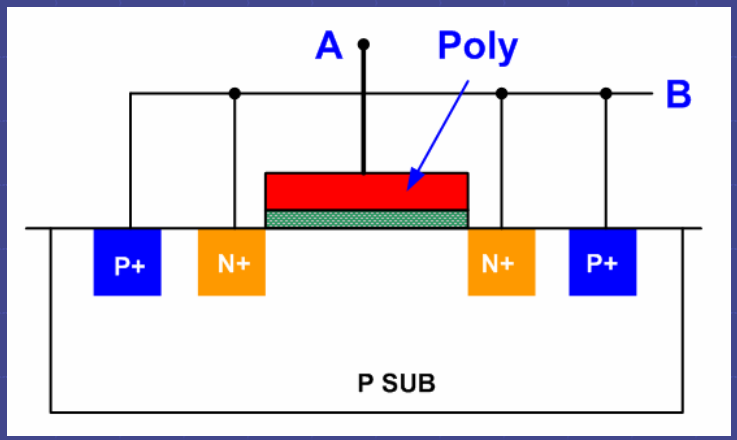


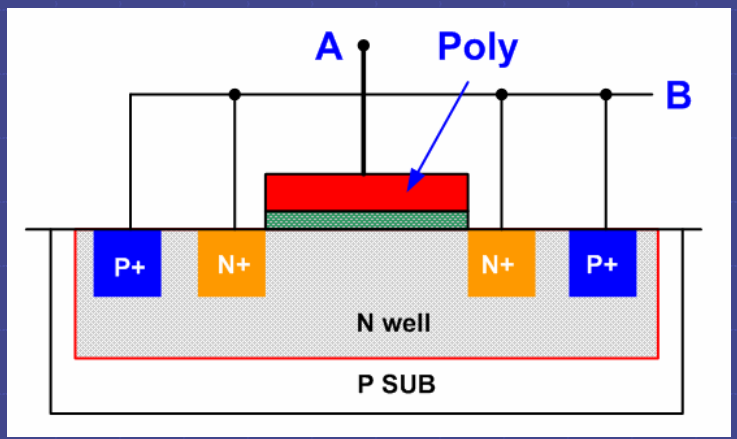
Construction of a simple parallel – plate capacitor

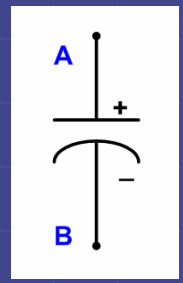


Capacitor Types

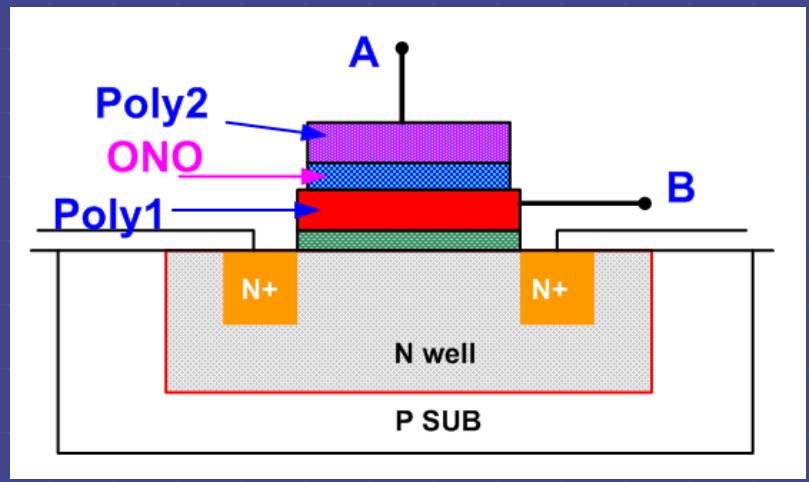
MOS

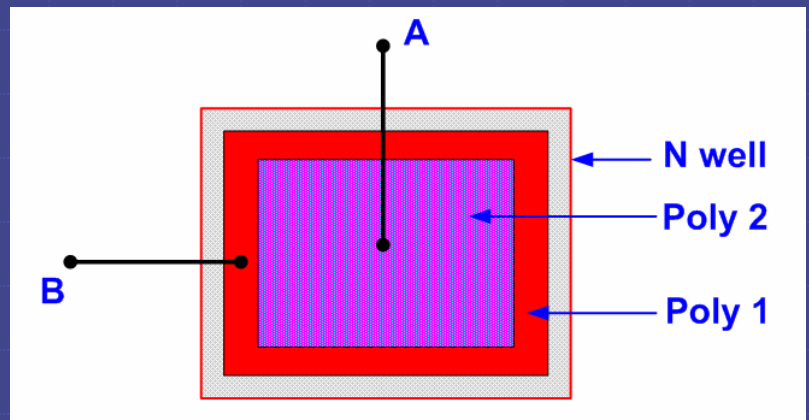






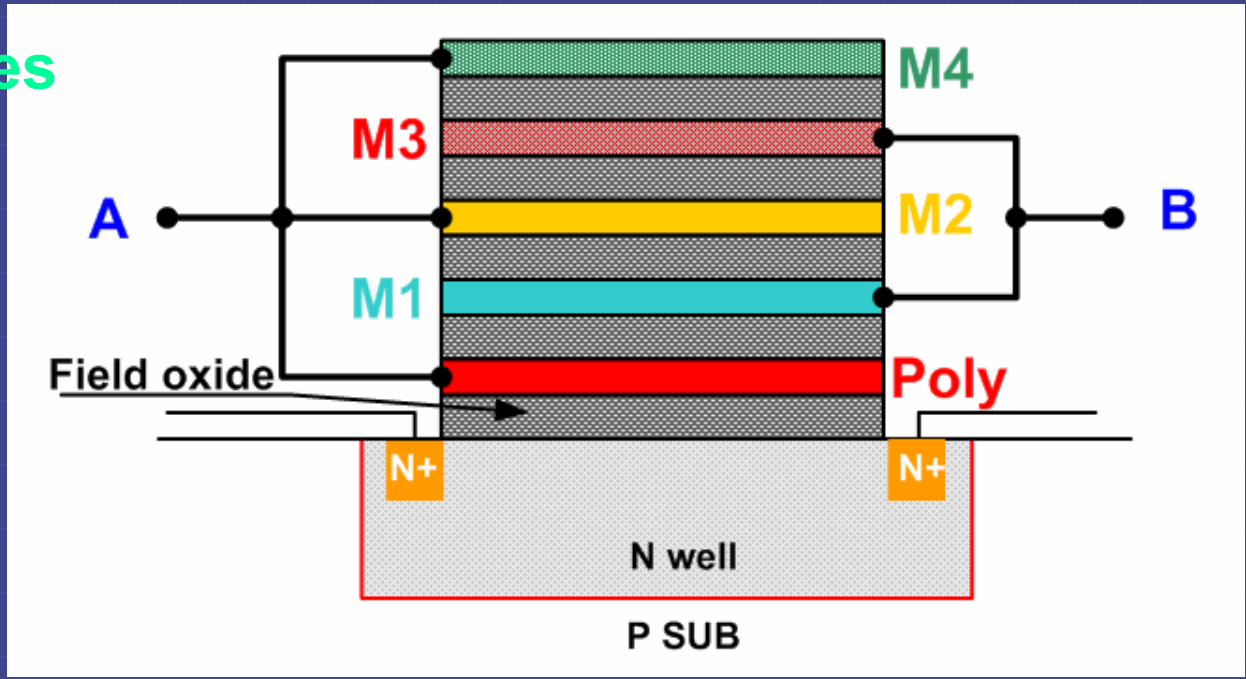
Double poly

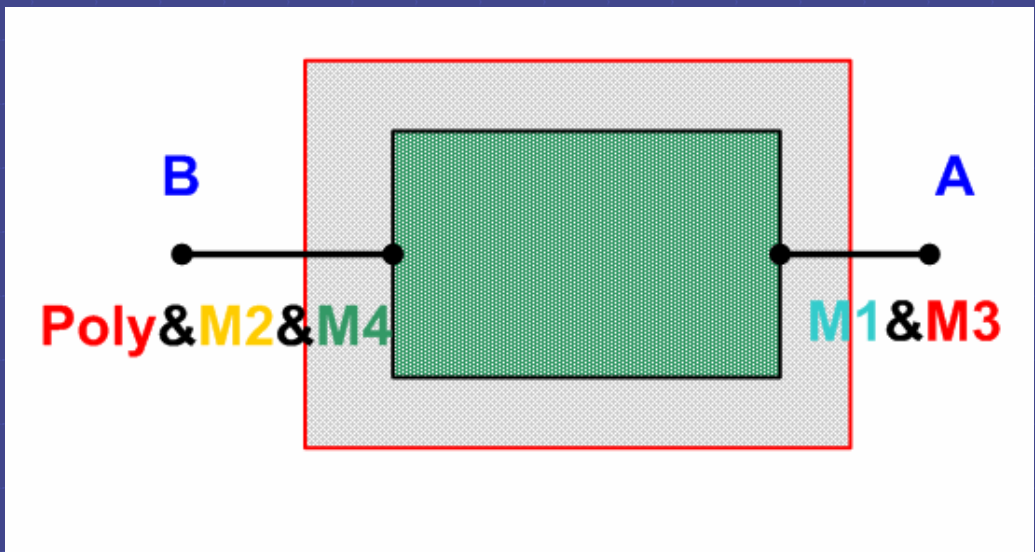


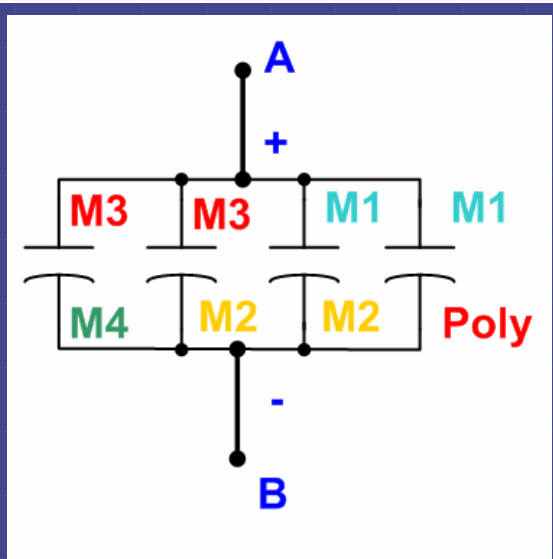


Capacitor Types

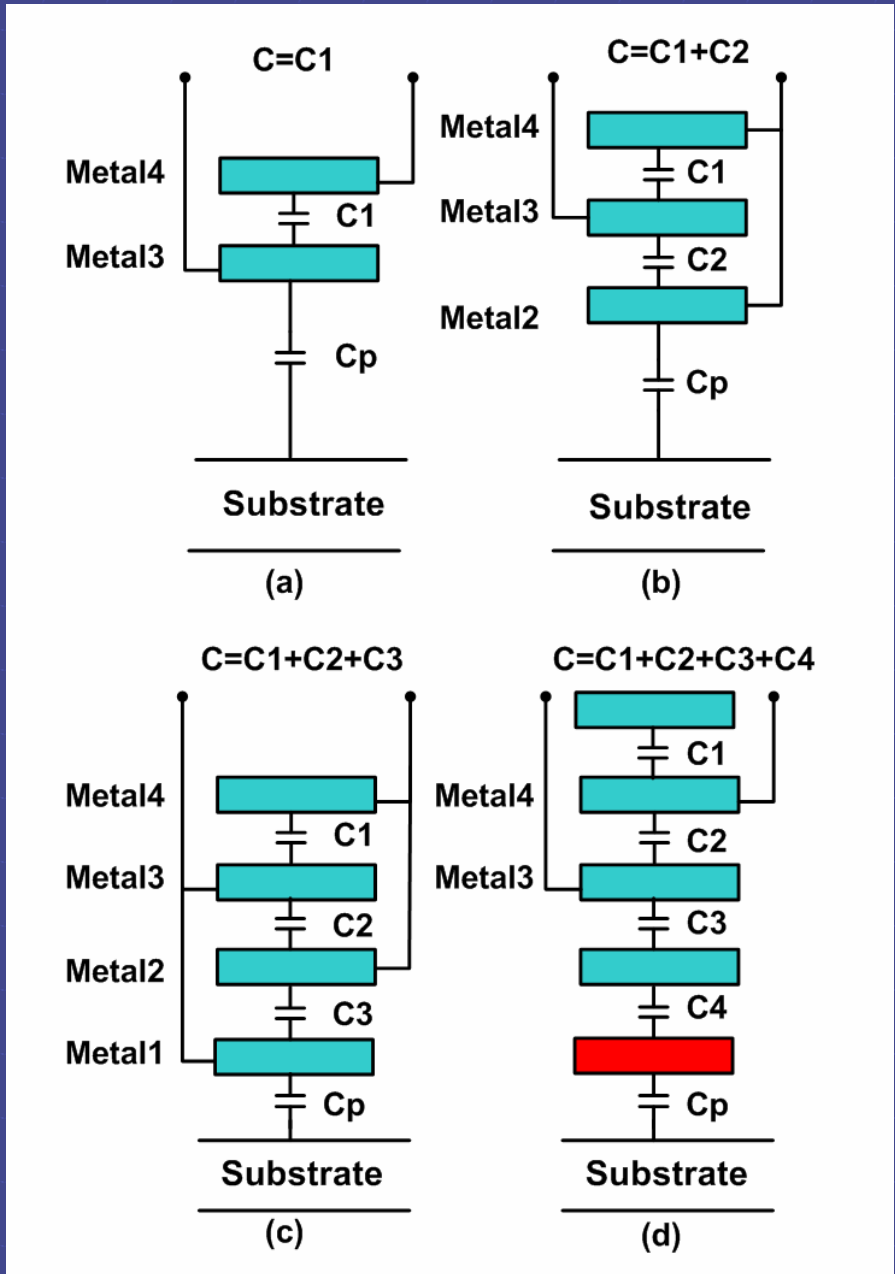
Sandwich



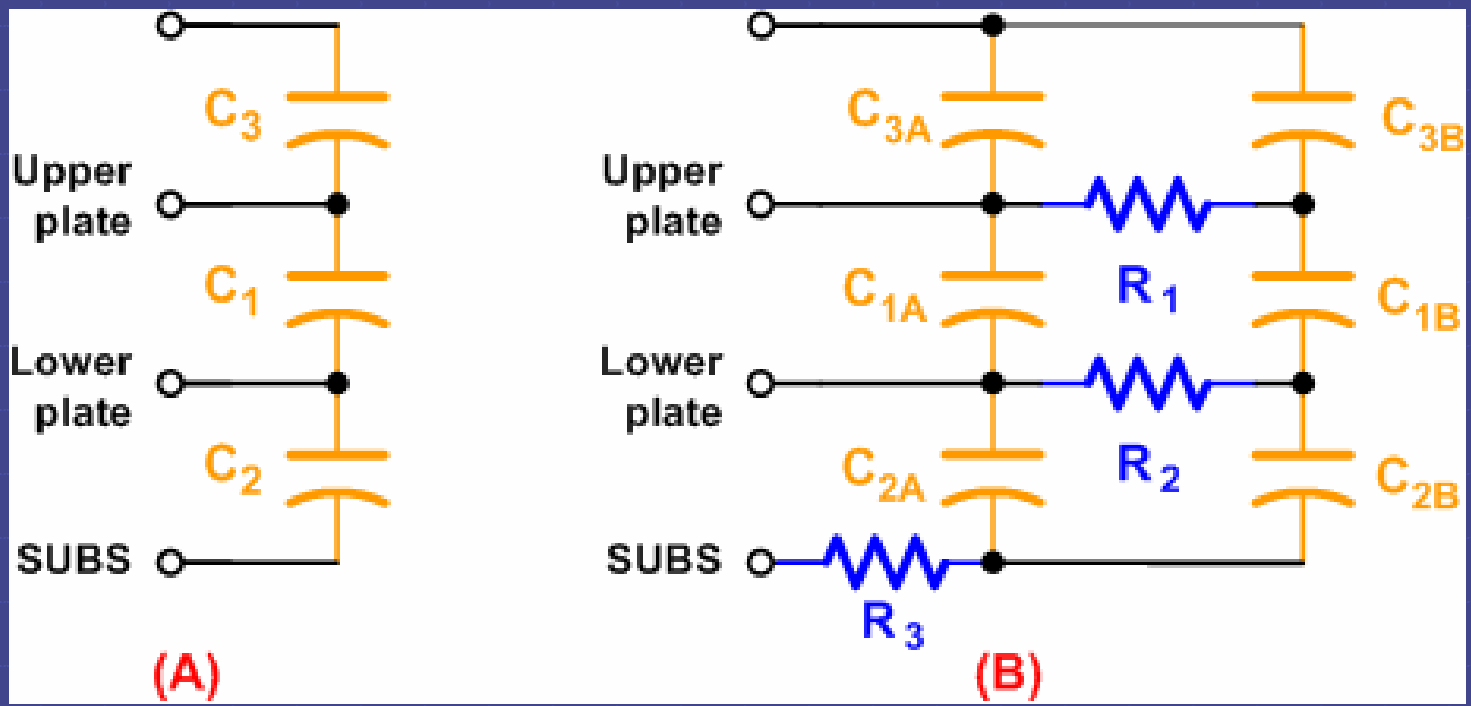




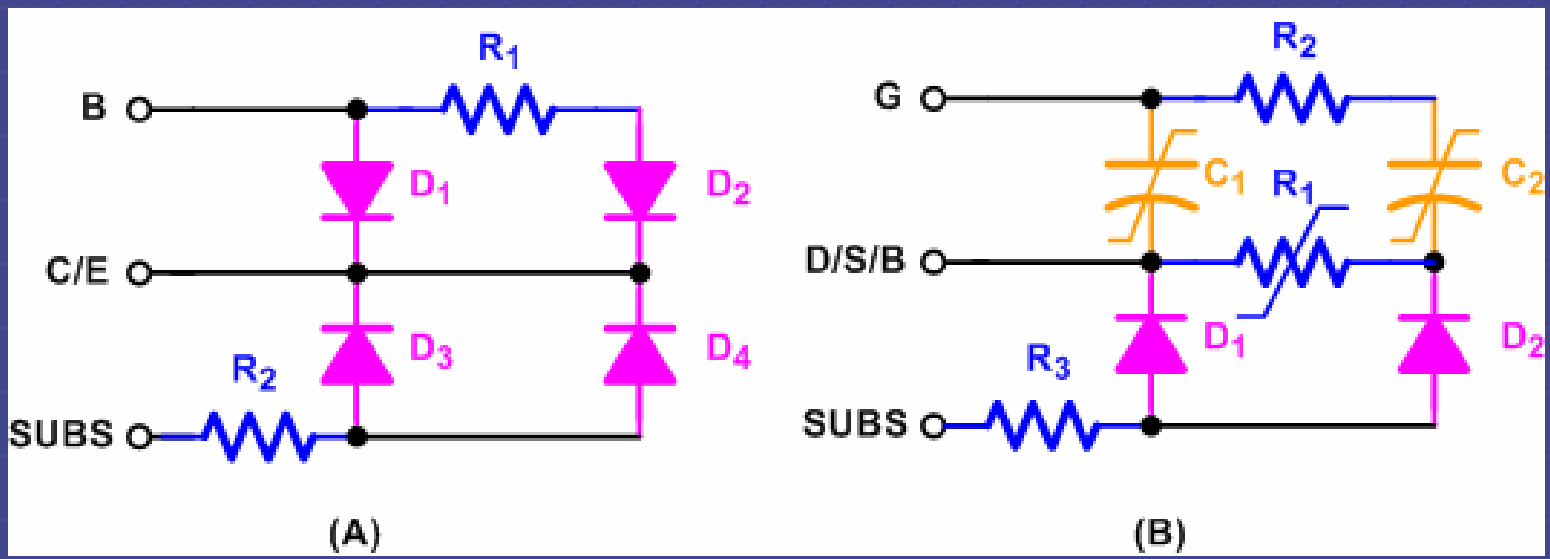
Capacitor Structure Using Various Conductive Layers



Subcircuit models for poly-poly capacitors: (a) a simple model without series resistance, and (b) a model incorporating series resistance using single π-sections.

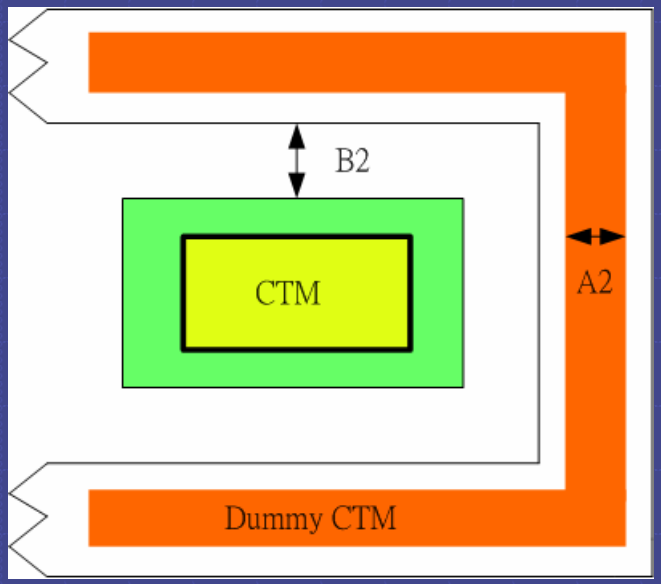


Subcircuit models for (a) a junction capacitor where C/E denotes the collector.emitter electrode and B denotes the base electrode; and (b) an MOS or gate oxide capacitor where G denotes the deposited gate electrode and D/S/B denotes the drain/source backgate electrode.

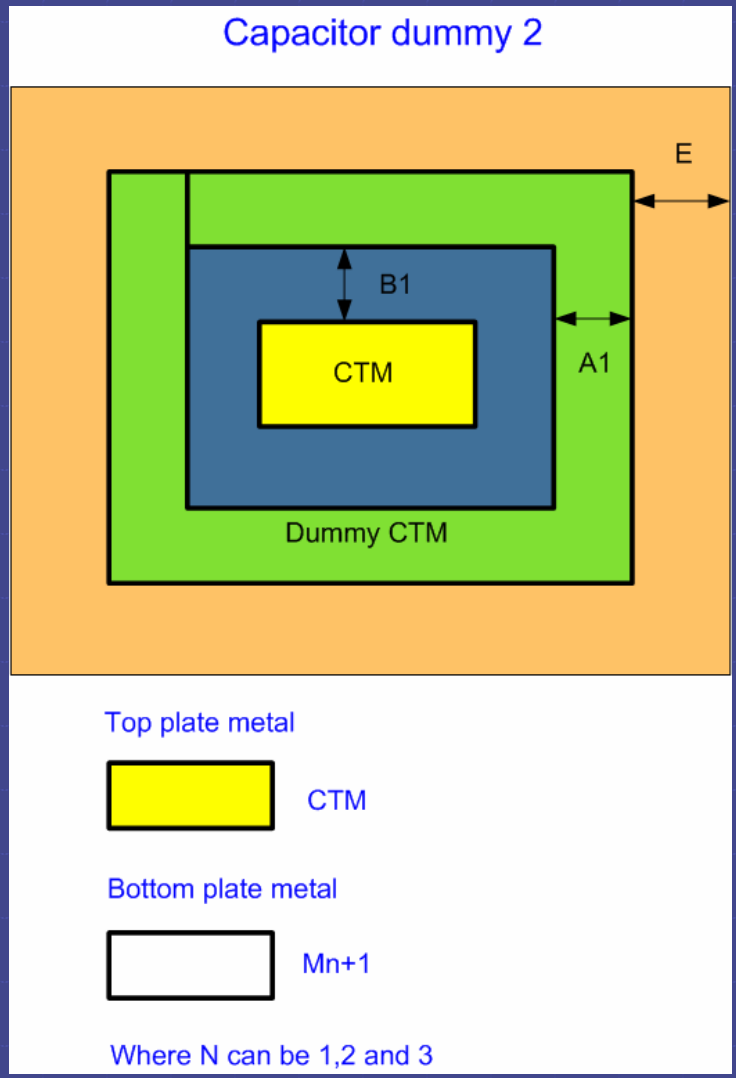


CTM

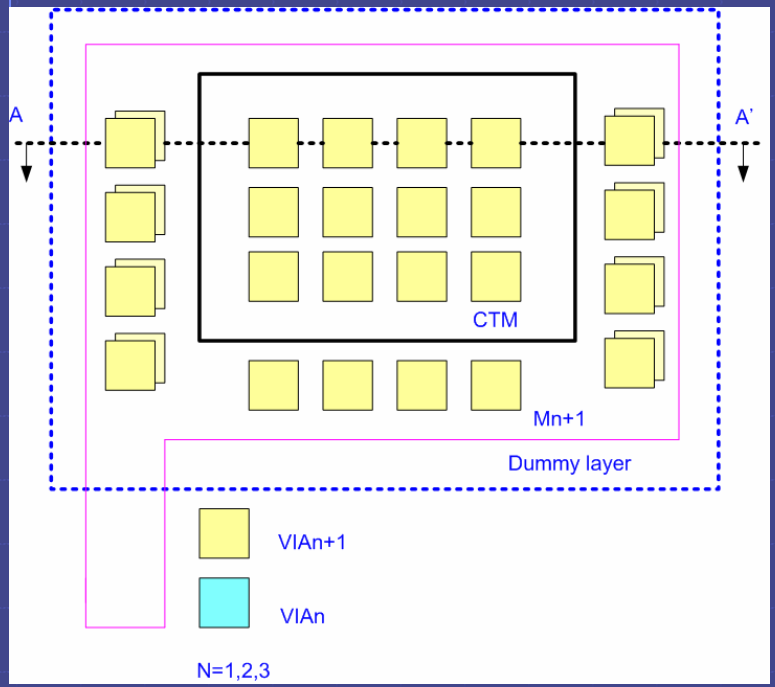
Capacitor dummy 1

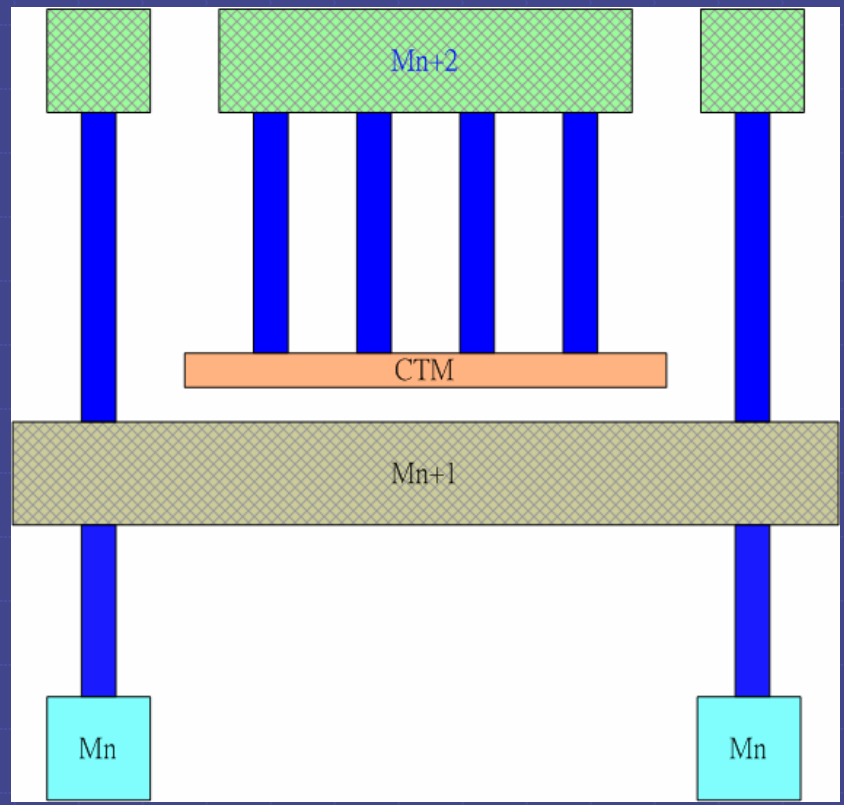


Capacitor dummy 2



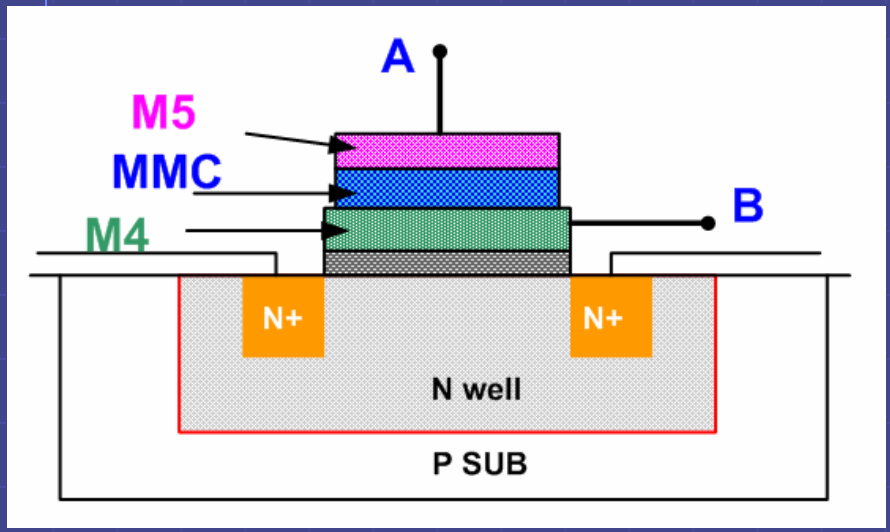
Metal-Insulator-Metal (MIM) Capacitor

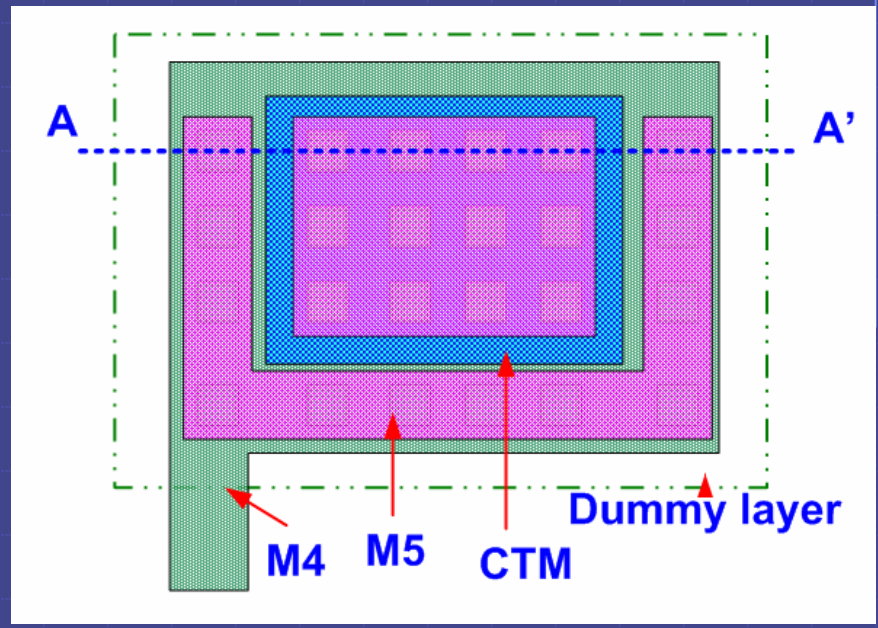


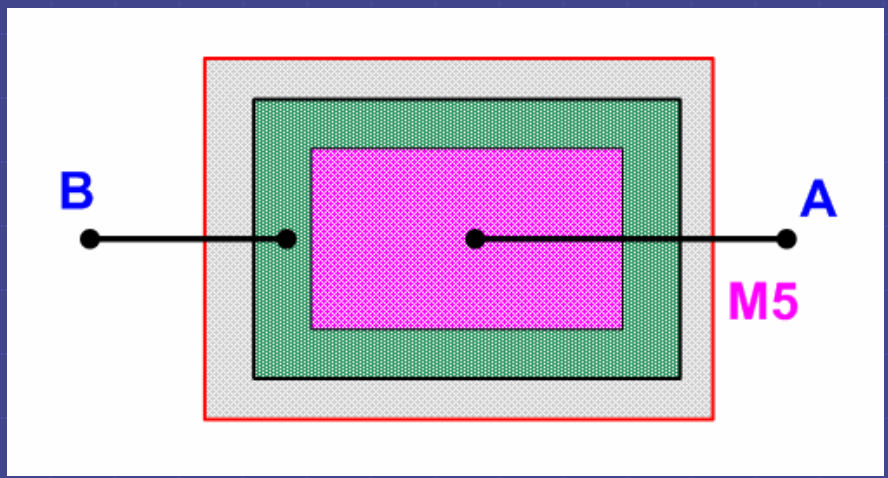


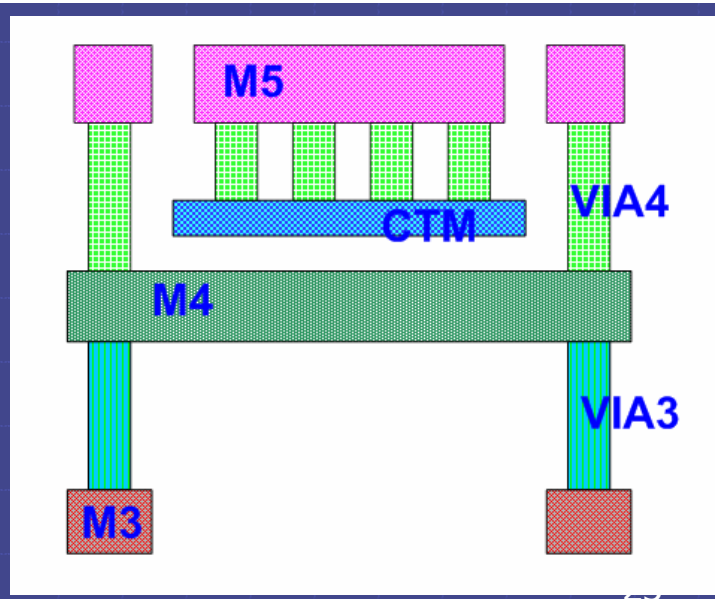
Capacitor Types

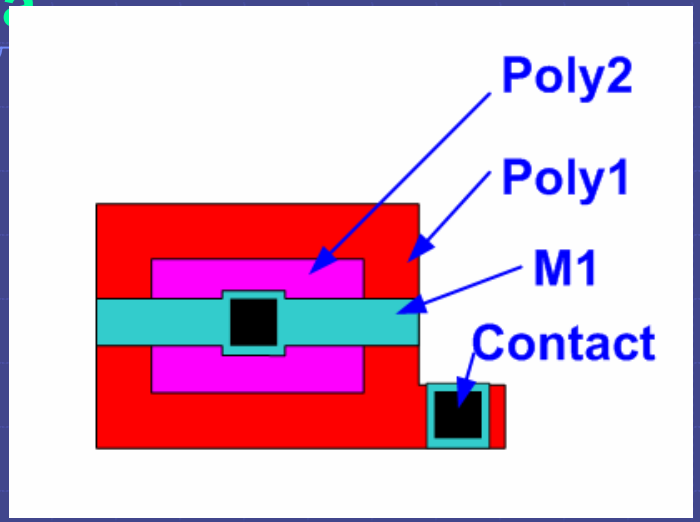
MMC

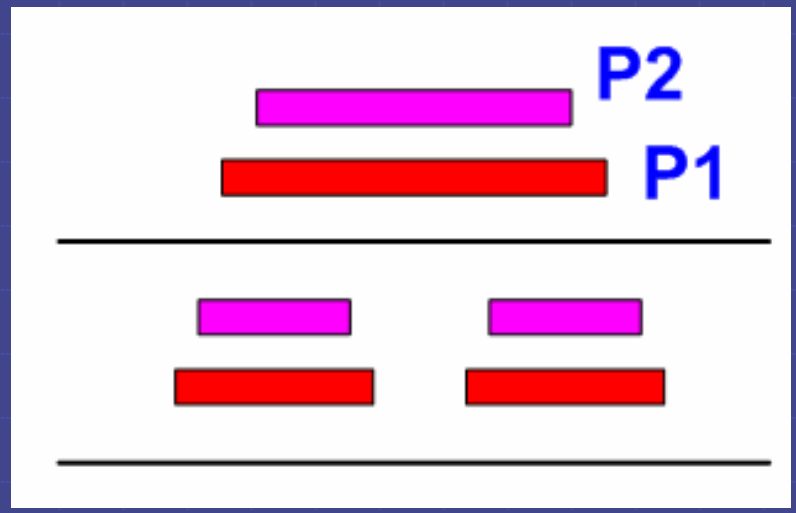


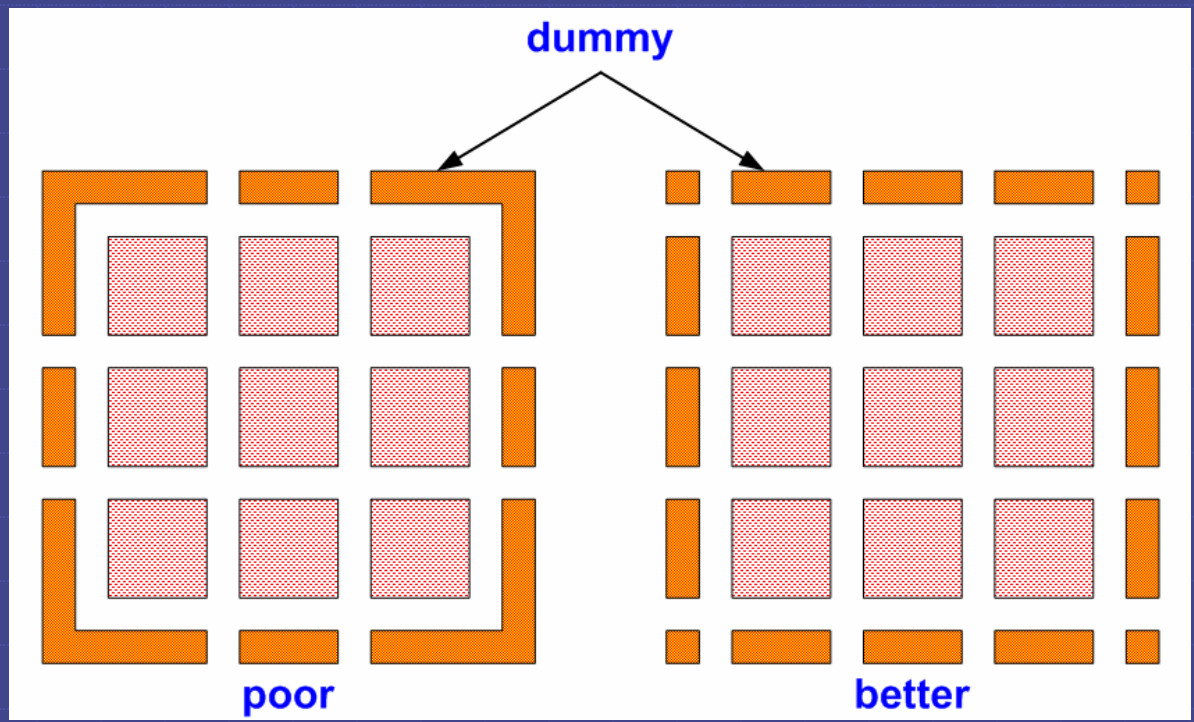




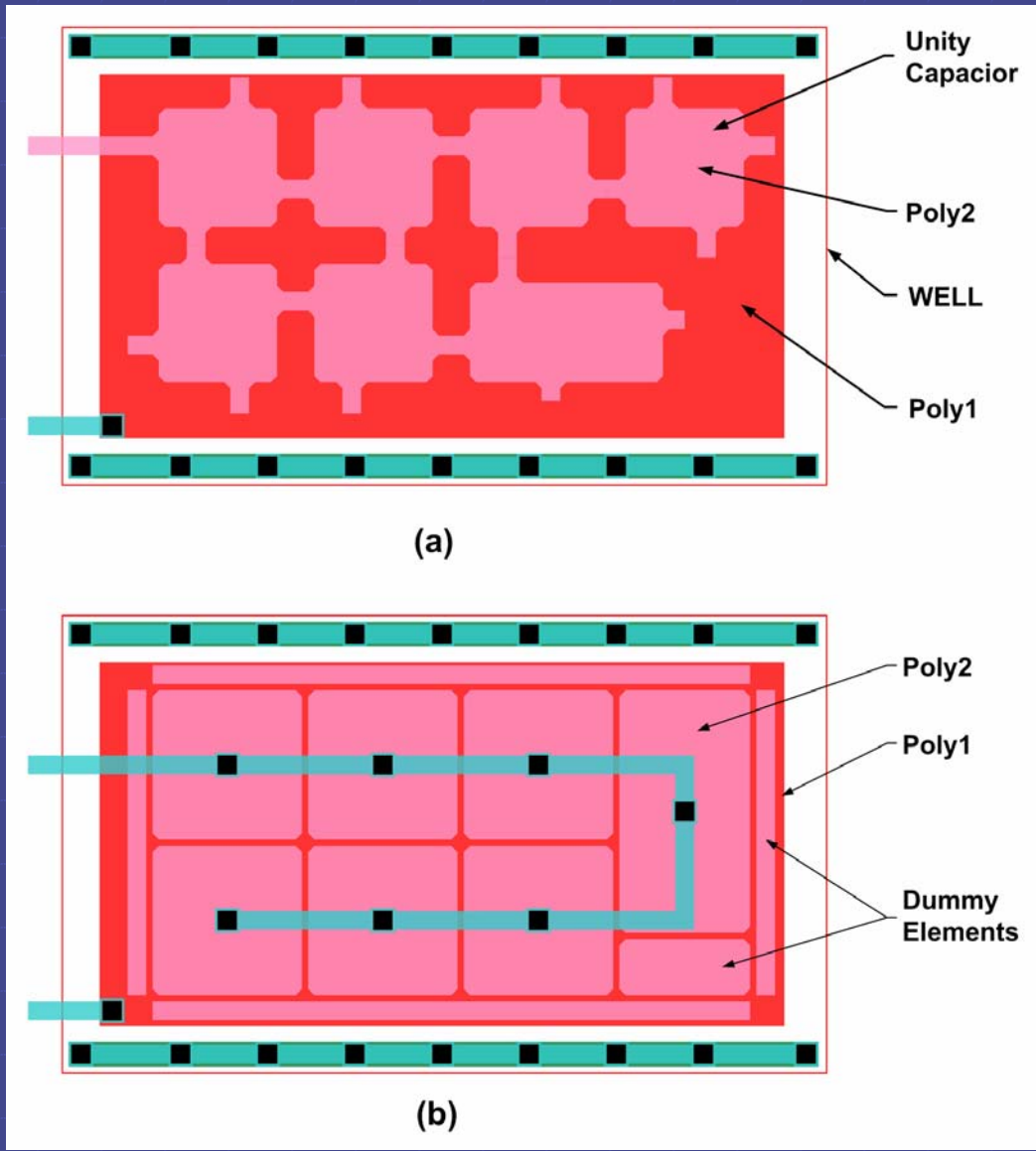


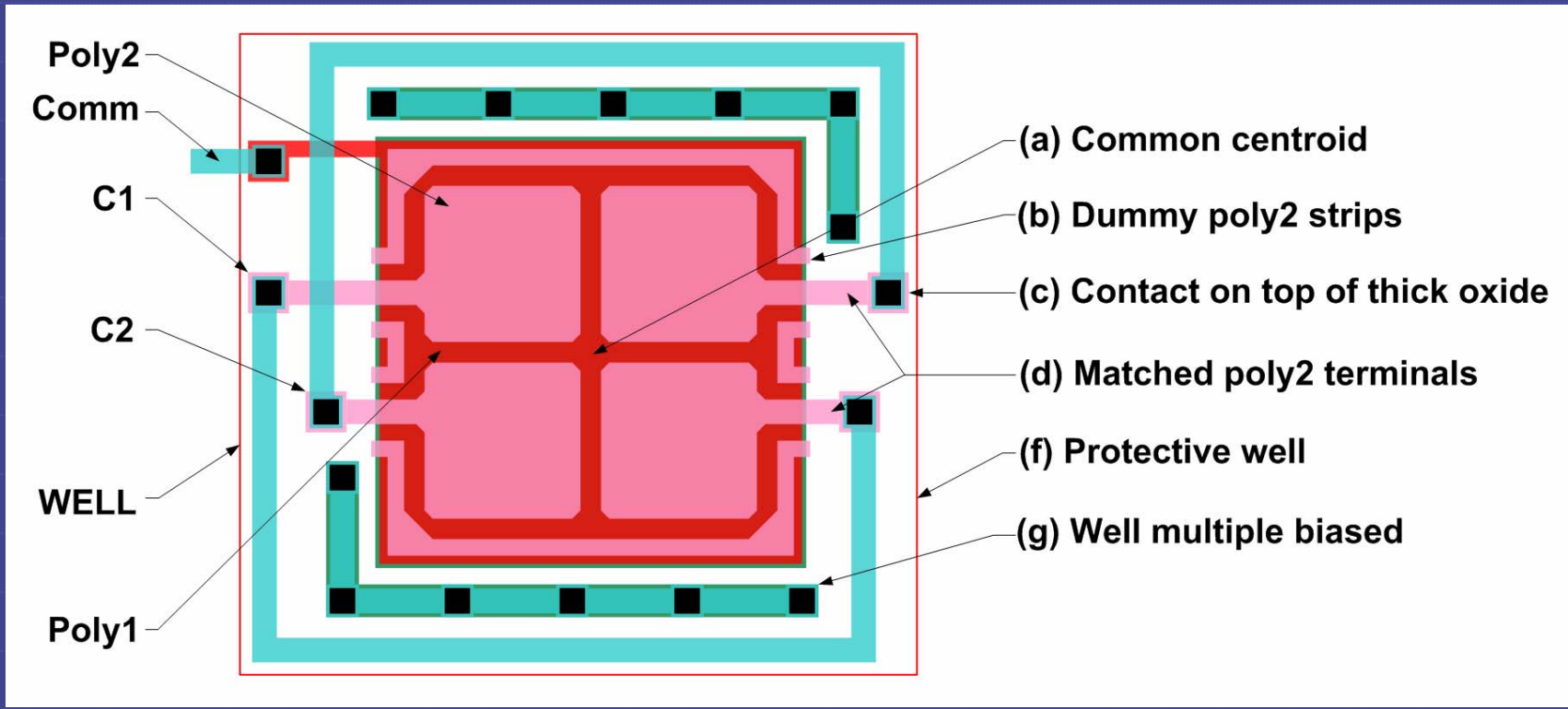

Poly2
Poly1
M1
Contact

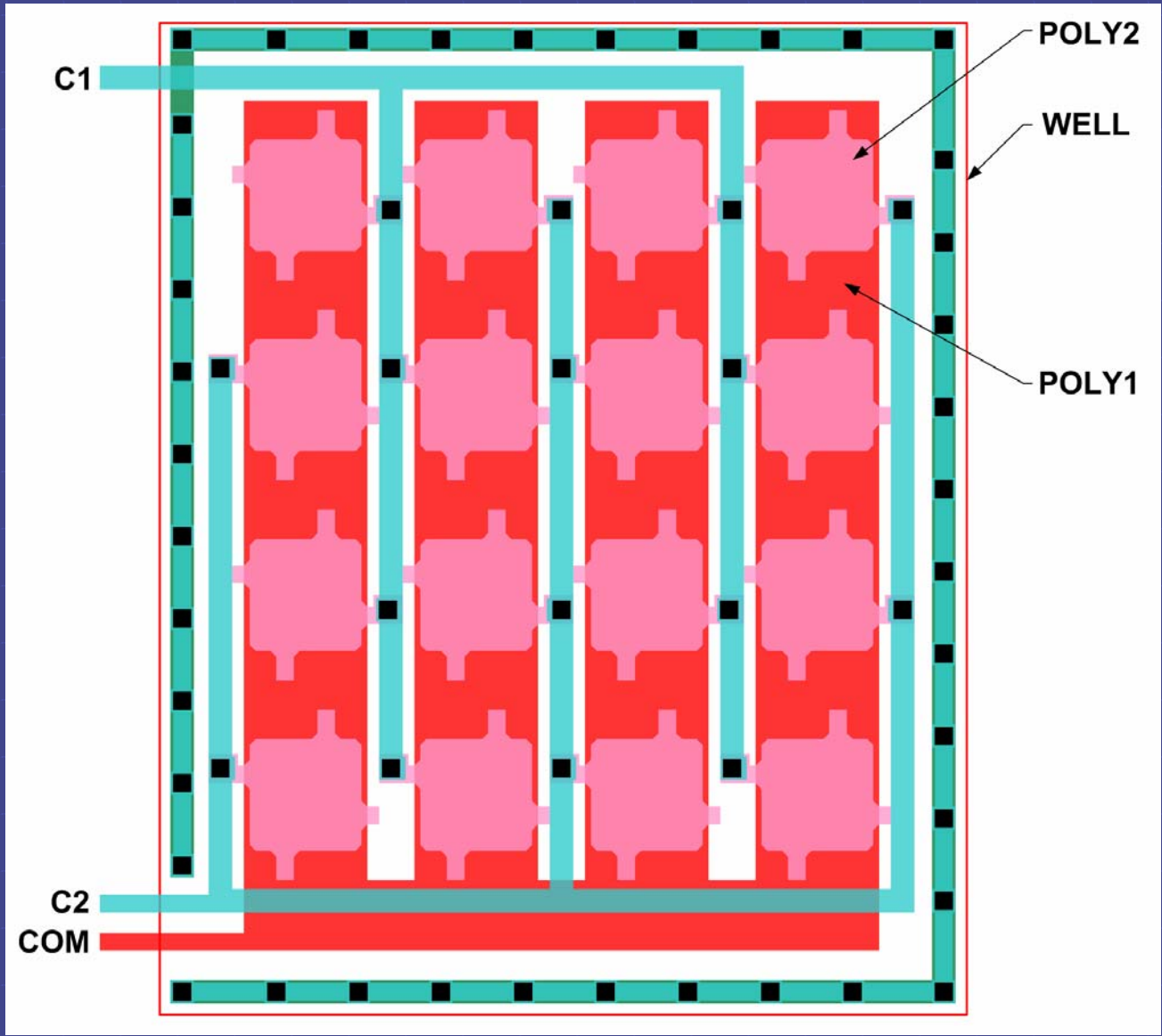

P2
P1

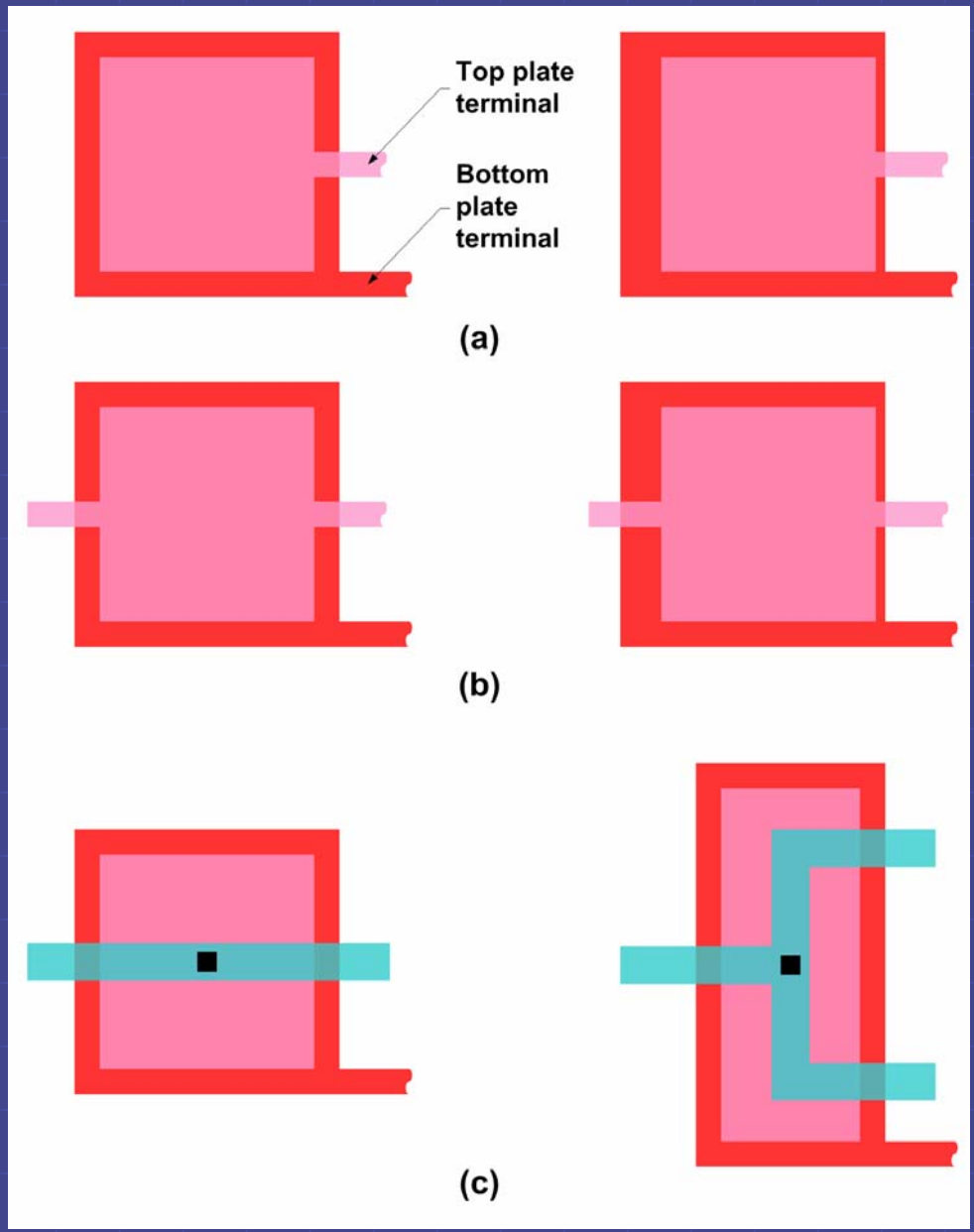

dummy
poor
better

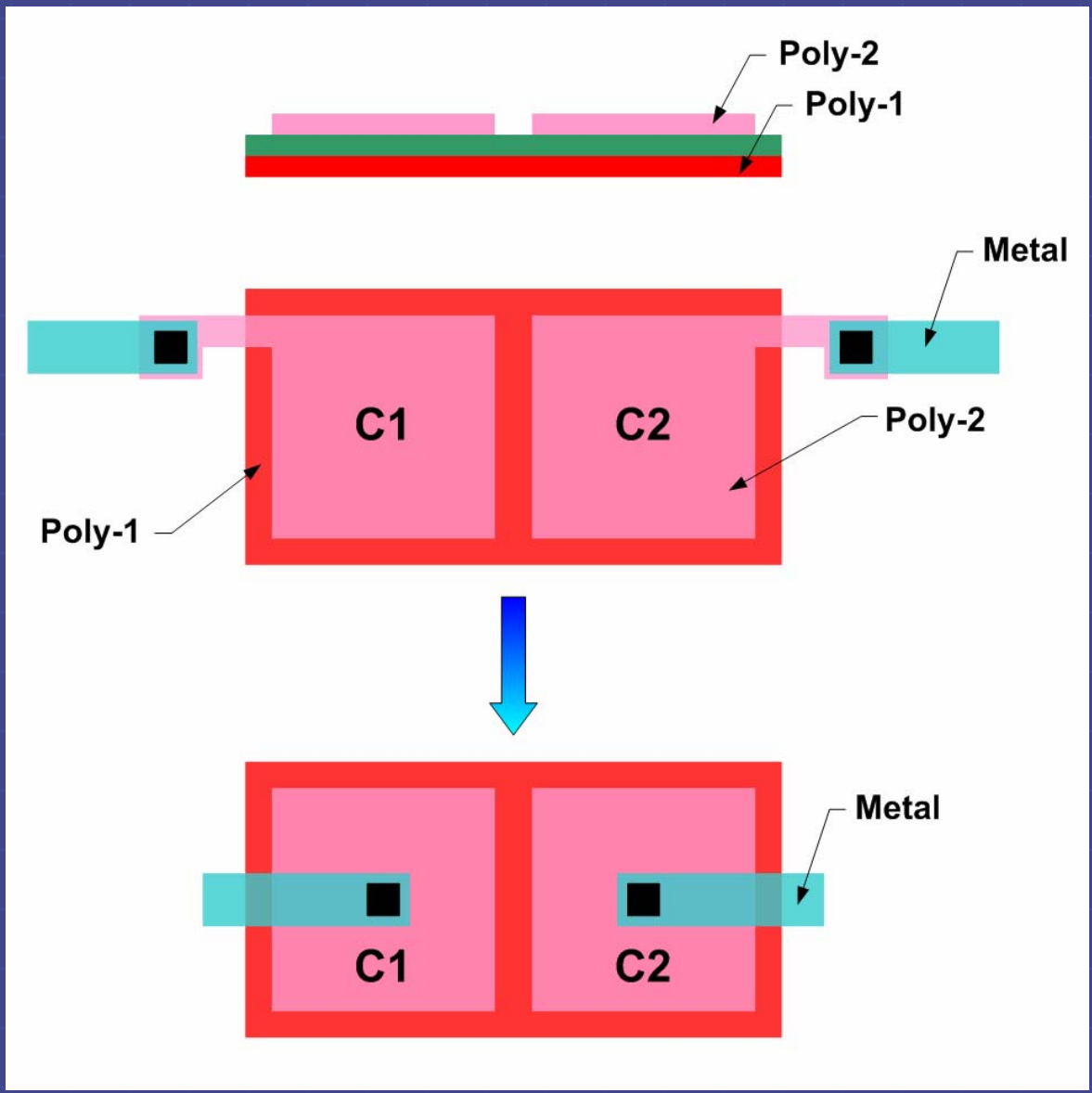
Non-Integer Multiple of Unity Capacitor

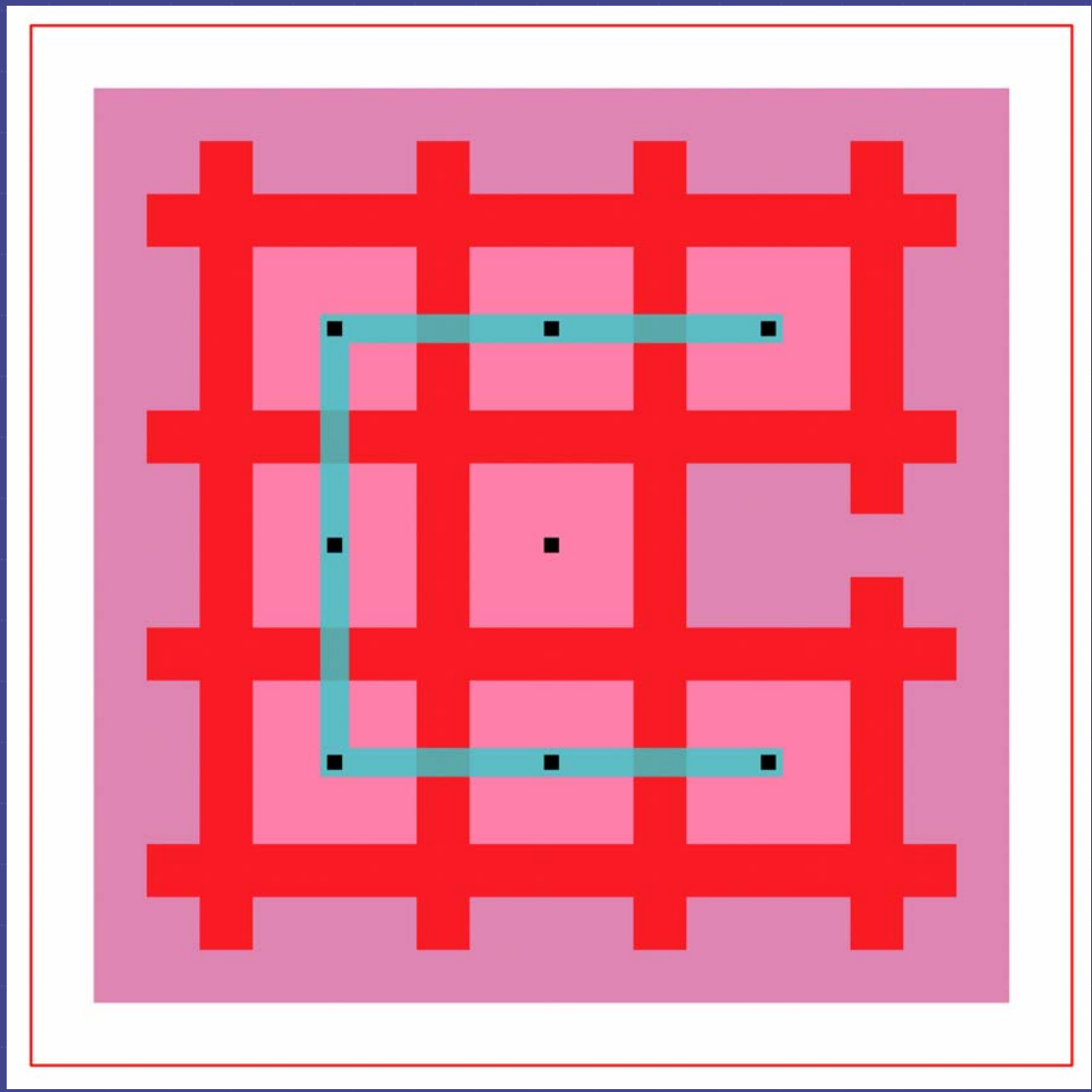


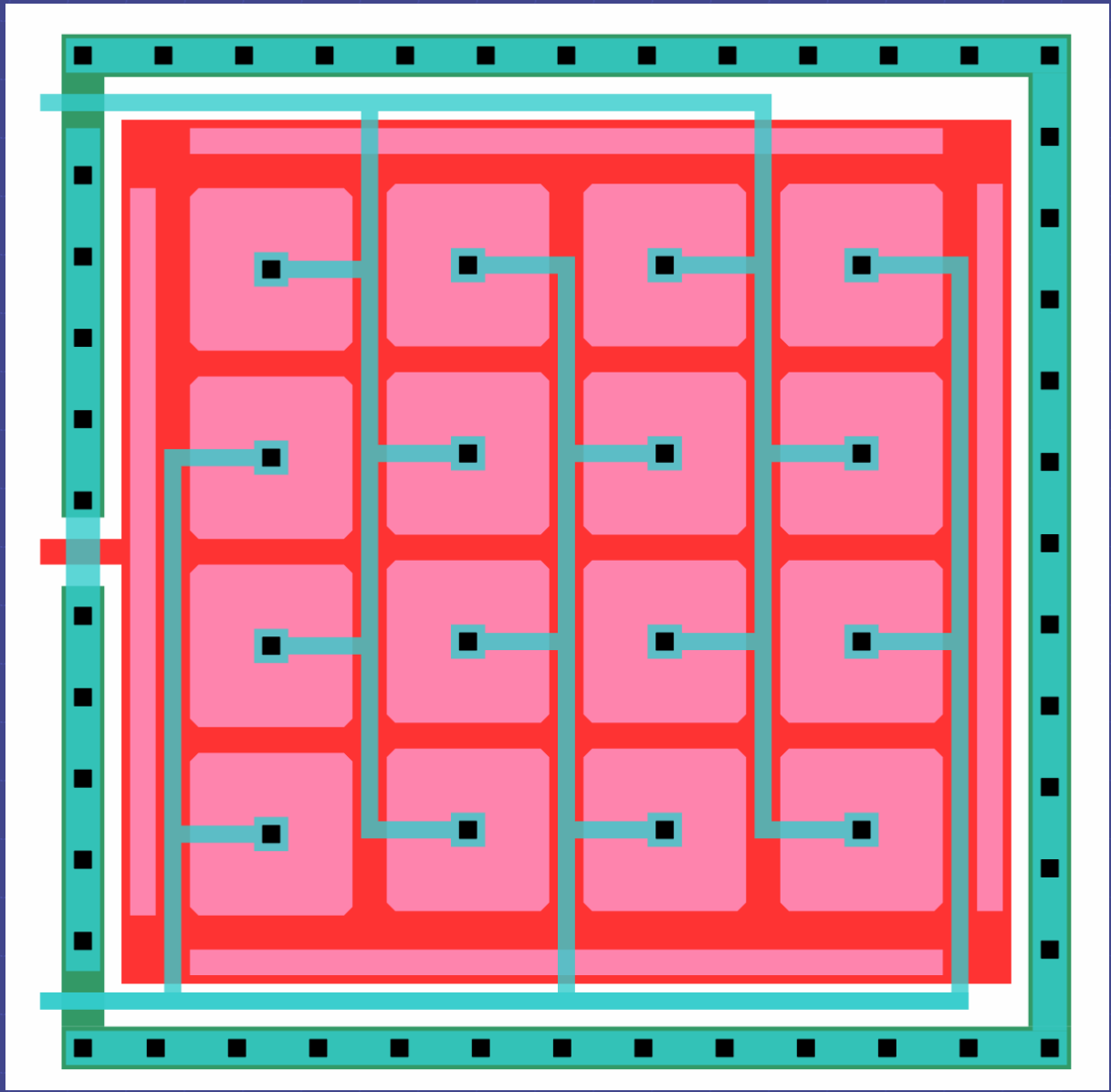

Poly2
Comm
C1
C2
WELL
Poly1
(a) Common centroid
(b) Dummy poly2 strips
(c) Contact on top of thick oxide
(d) Matched poly2 terminals
(f) Protective well
(g) Well multiple biased


C1
POLY2
WELL
POLY1
C2
COM

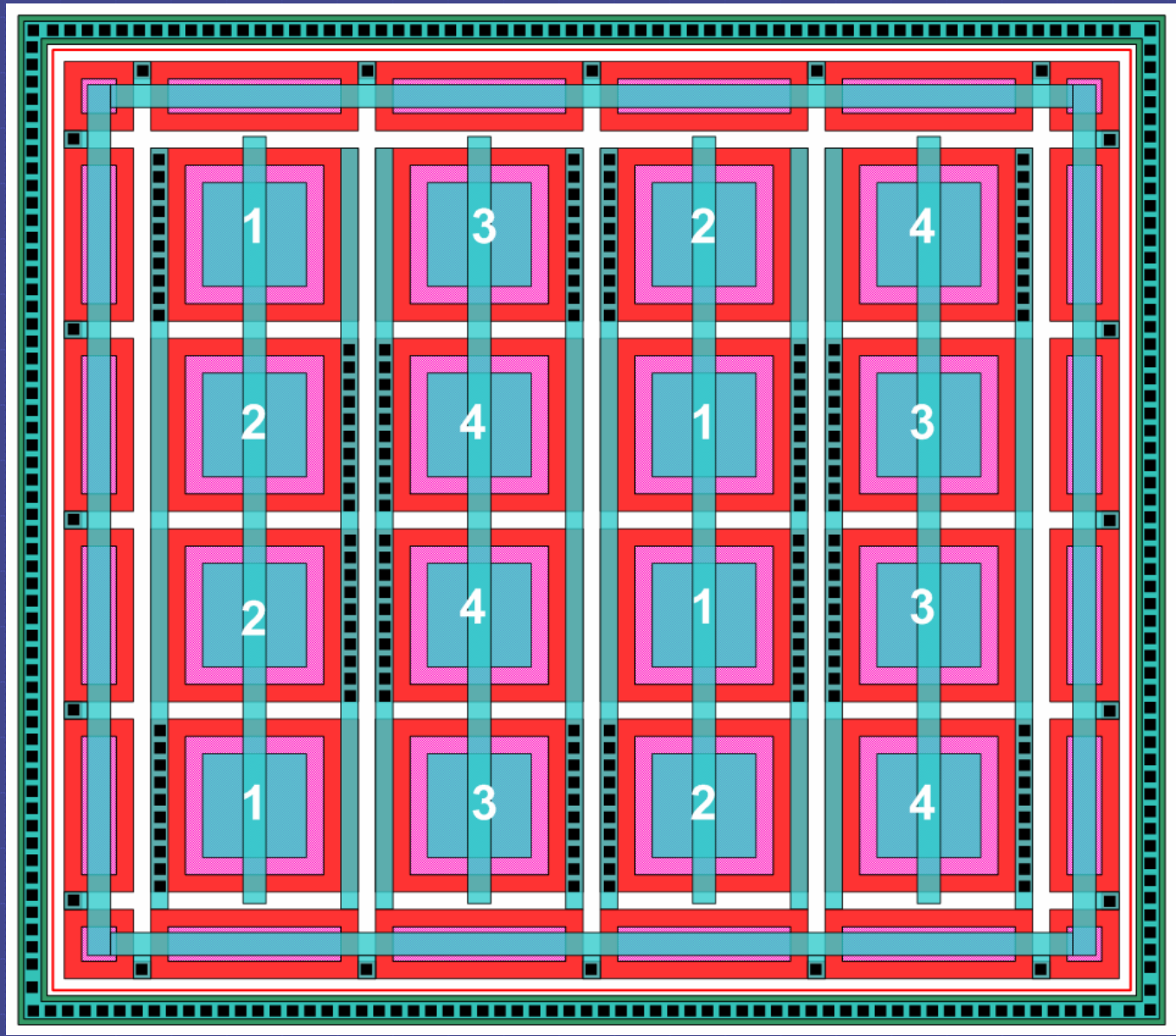

Top plate terminal
Bottom plate terminal
(a)
(b)
(c)


Poly-2
Poly-1
Metal
C1
C2
Poly-2
Poly-1
Metal
C1
C2

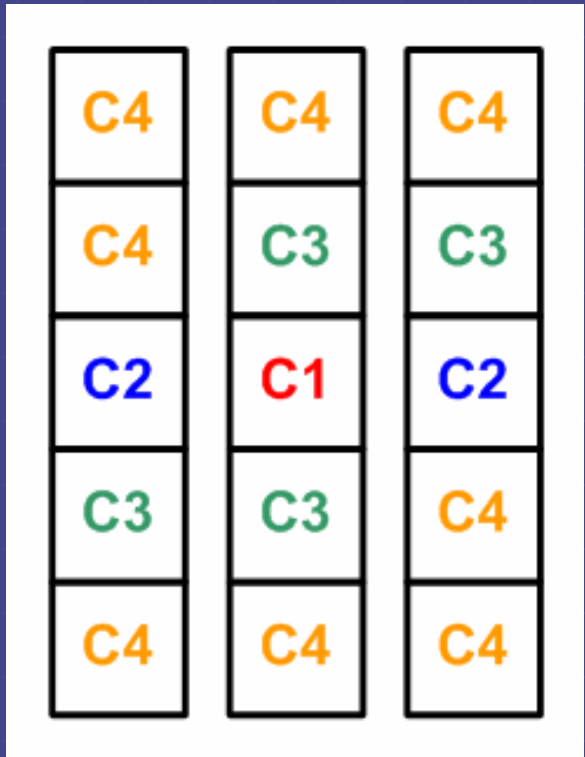


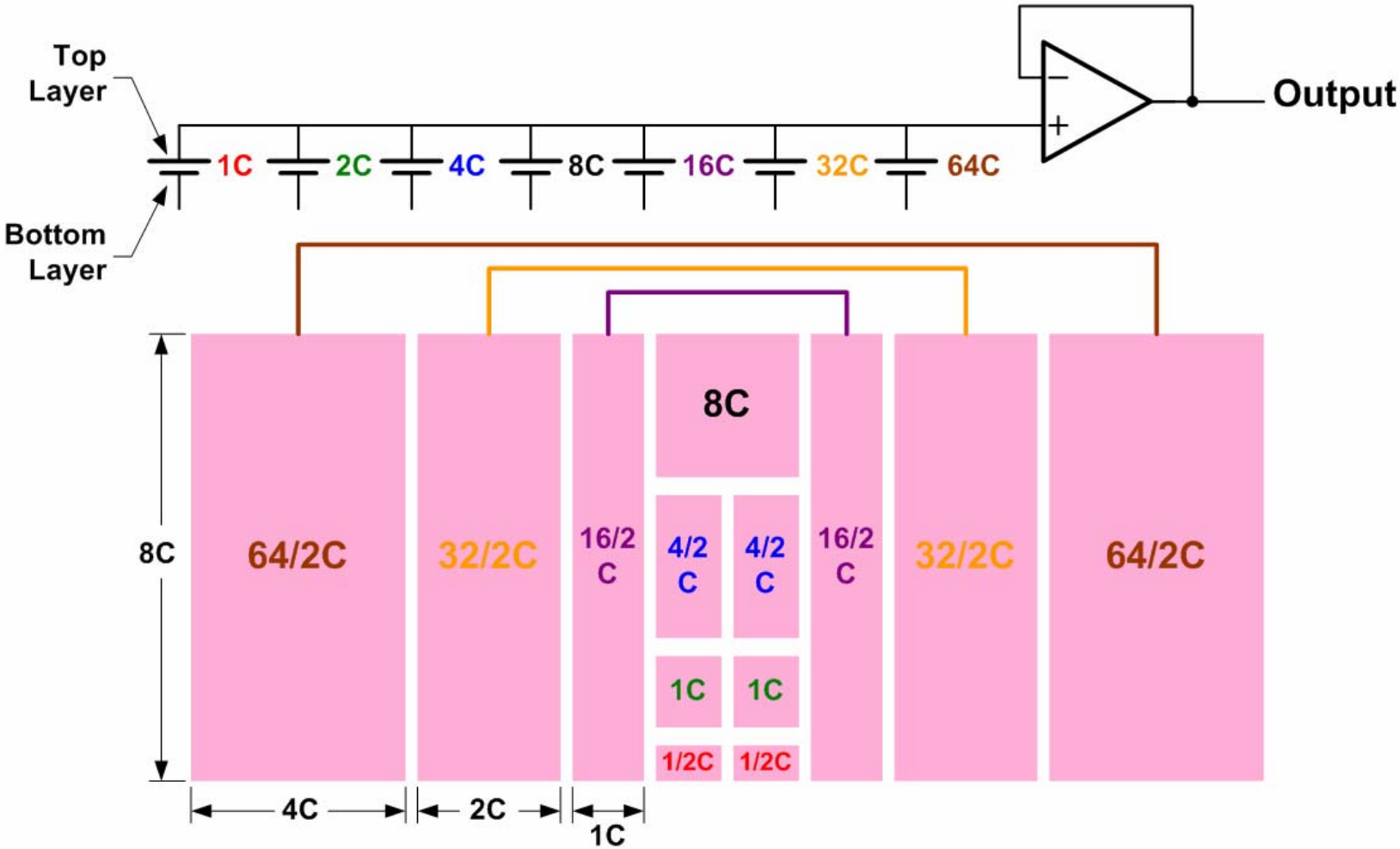


Unit Capacitor

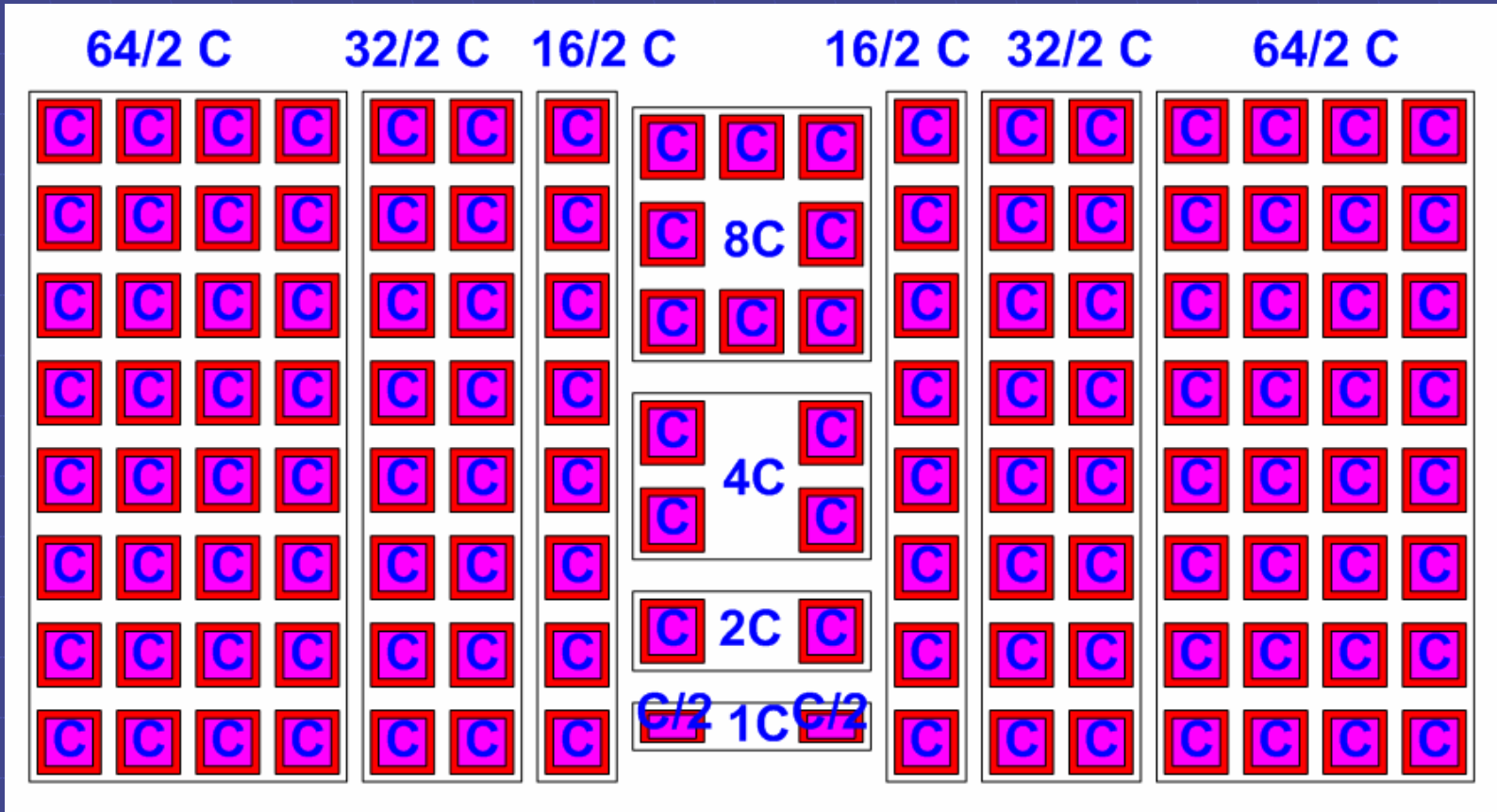


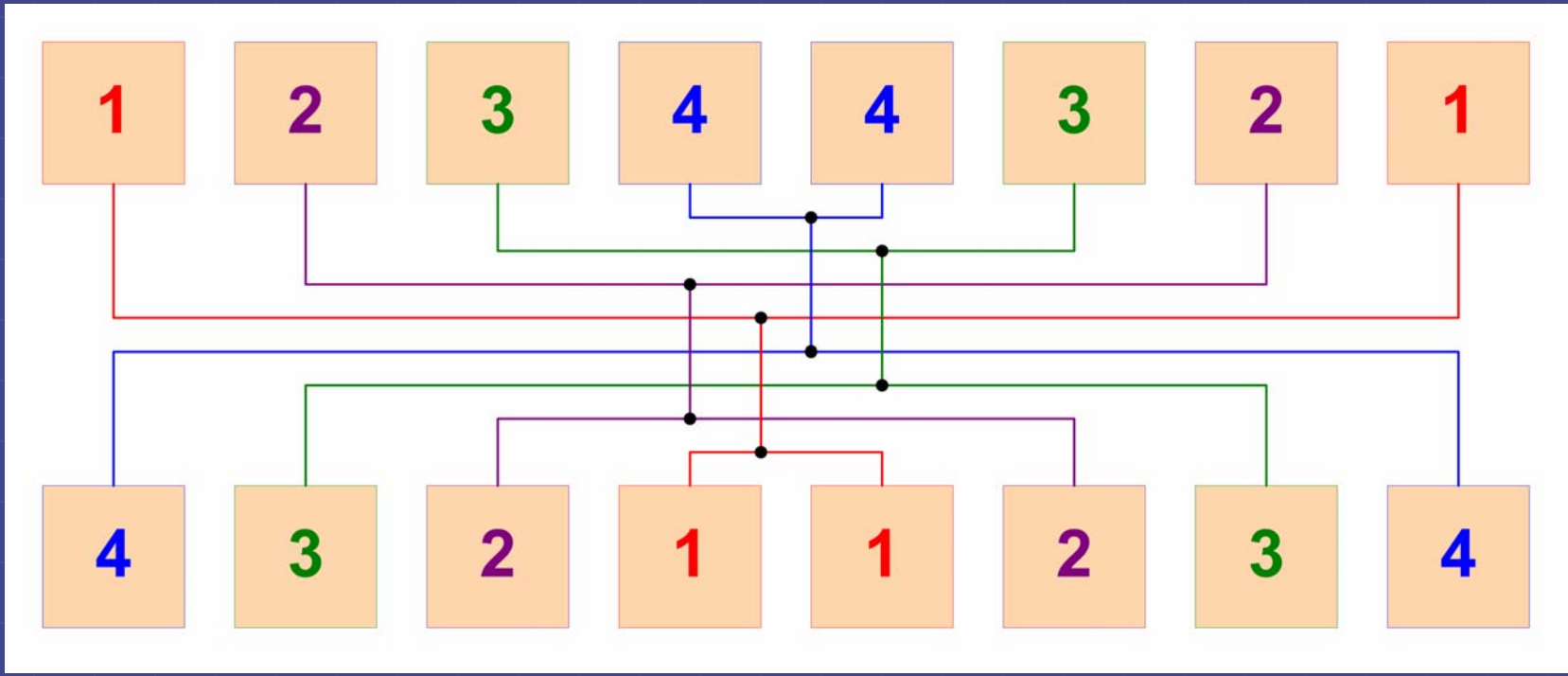
Common-Centroid Layout of Capacitor



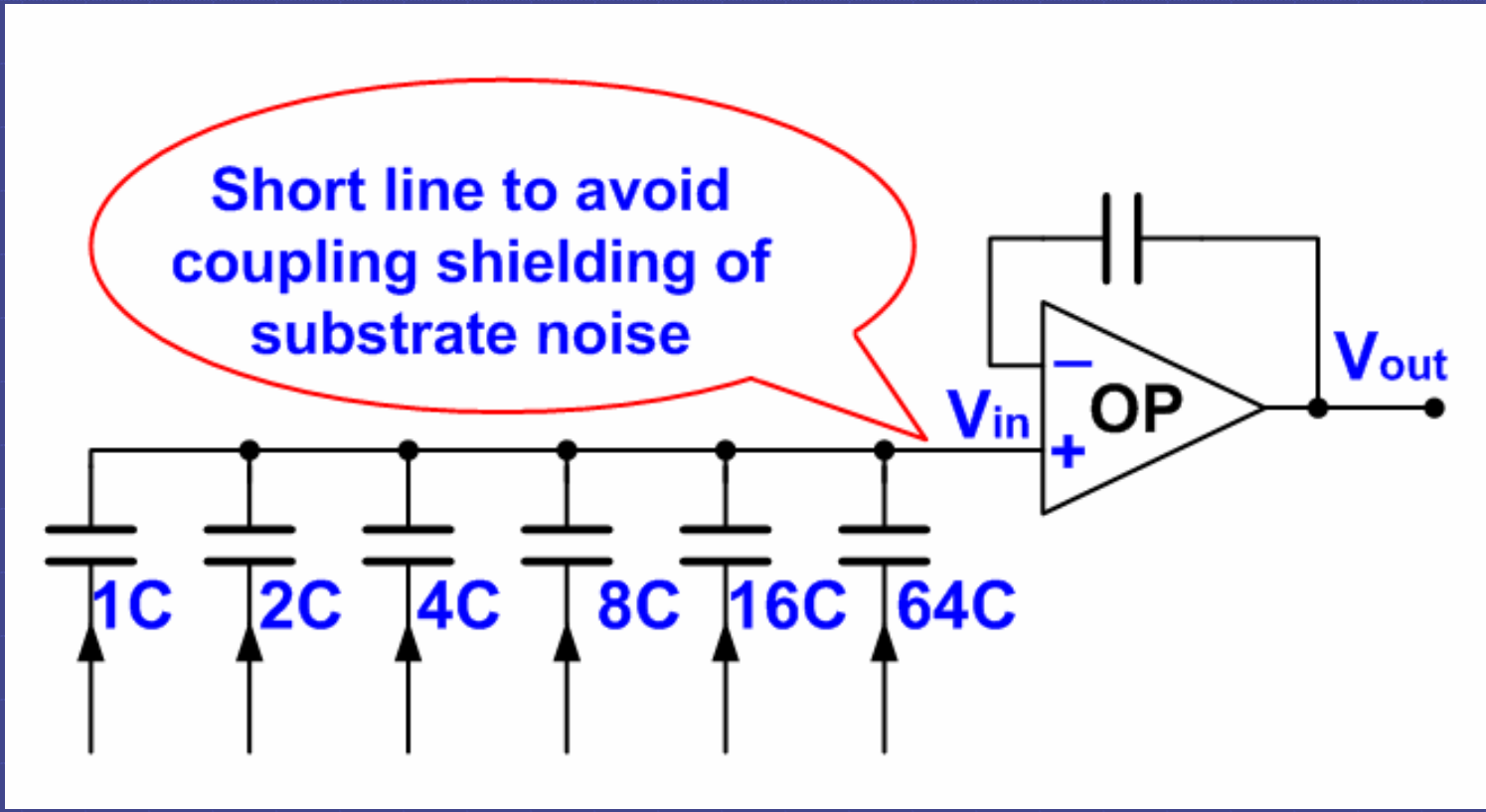

Top Layer
Bottom Layer
1C
2C
4C
8C
16C
32C
64C
Output
8C
64/2C
32/2C
16/2 C
8C
4/2 C
4/2 C
1C
1C
1/2C
1/2C
16/2 C
32/2C
64/2C
4C
2C
1C

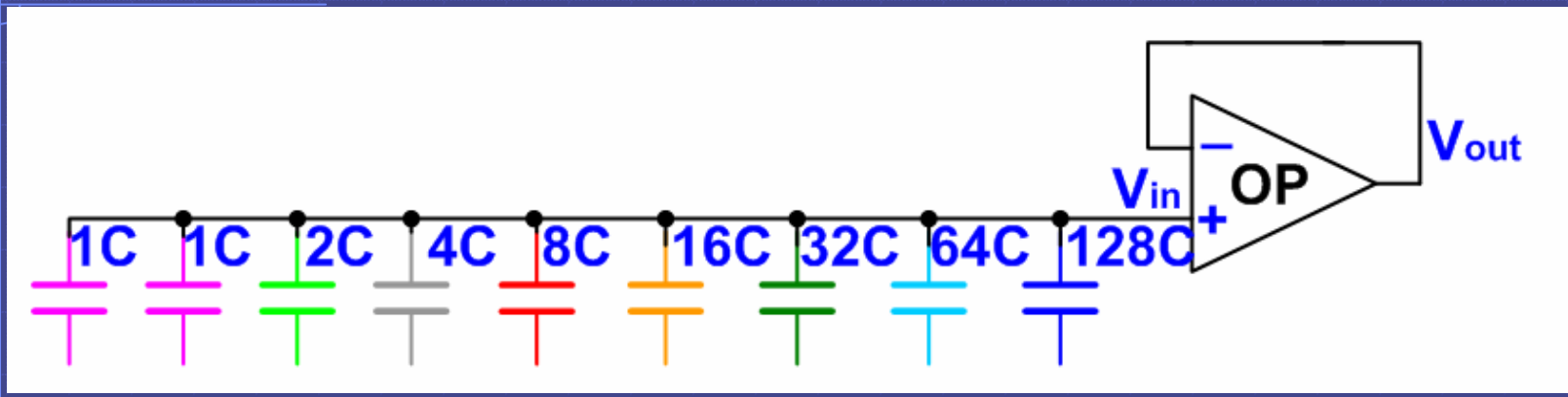
Capacitor Array

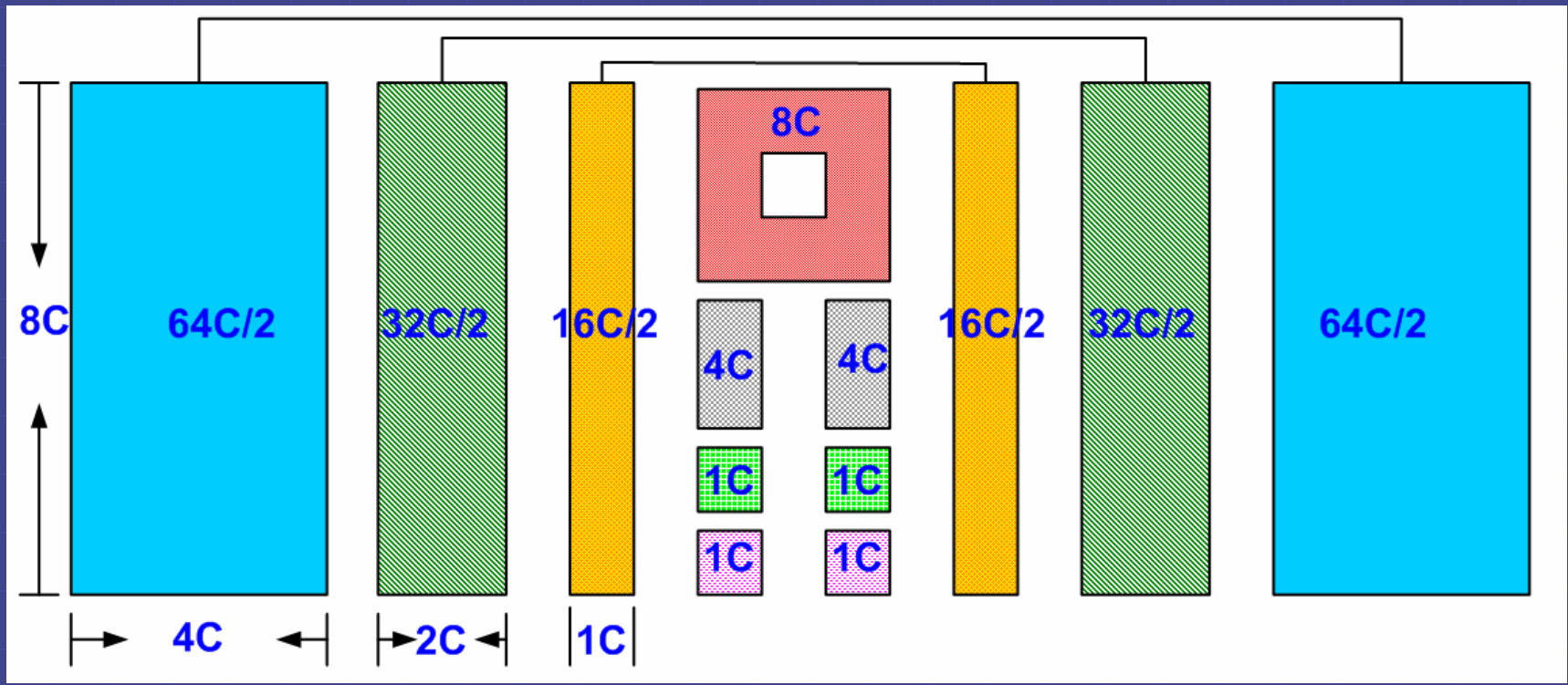


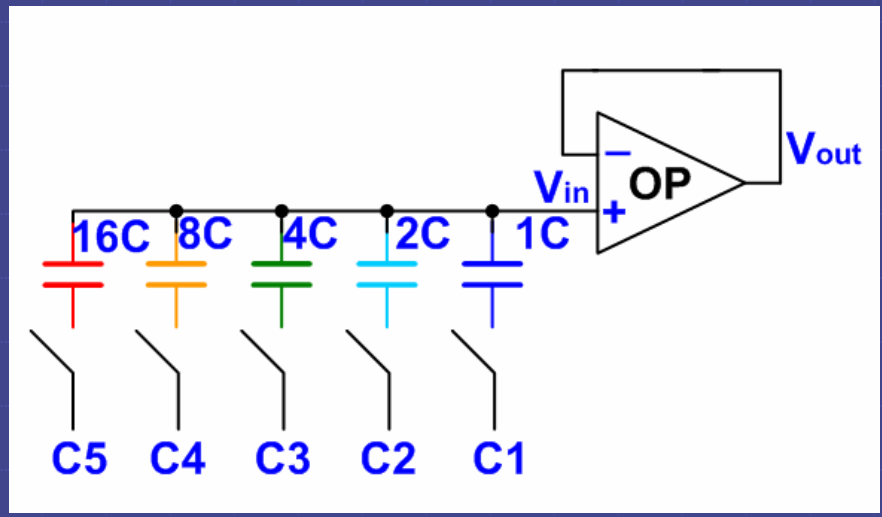

1
2
3
4
4
3
2
1
4
3
2
1
1
2
3
4

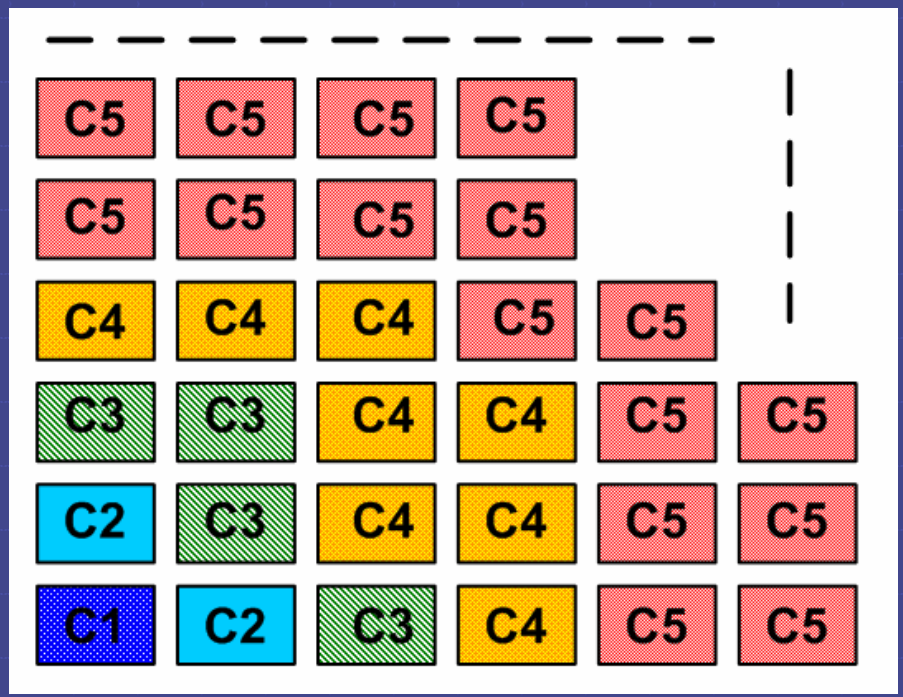
Capacitors Array in ADC/DAC




1C
1C
2C
4C
8C
16C
32C
64C
128C
Vin
OP
Vout


8C
64C/2
32C/2
16C/2
8C
4C
4C
1C
1C
1C
1C
16C/2
32C/2
64C/2
4C
2C
1C


Vout
OP
Vin
16C
8C
4C
2C
1C
C5
C4
C3
C2
C1


C5 C5 C5 C5
C5 C5 C5 C5
C4 C4 C4 C5 C5
C3 C3 C4 C4 C5 C5
C2 C3 C4 C4 C5 C5
C1 C2 C3 C4 C5 C5

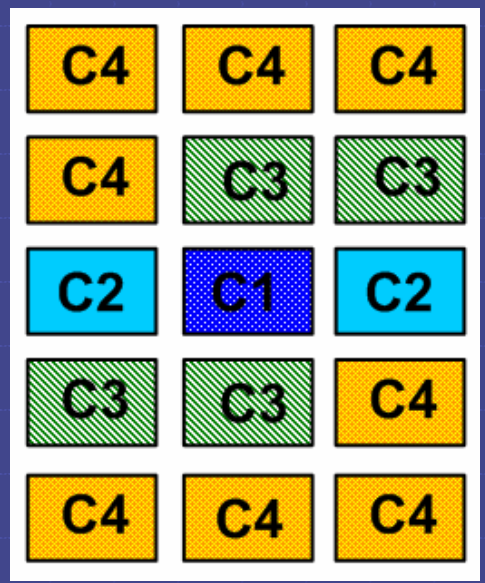
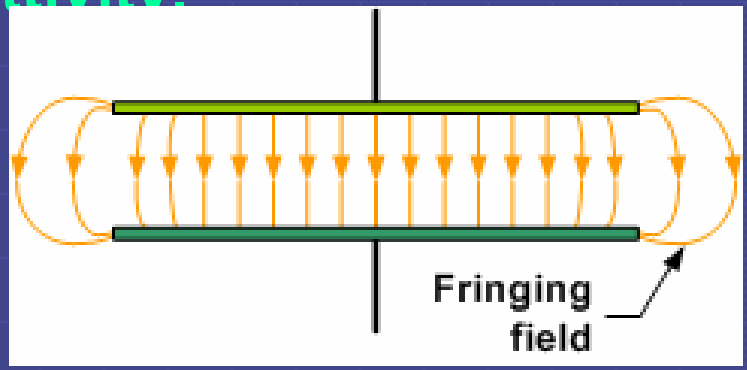
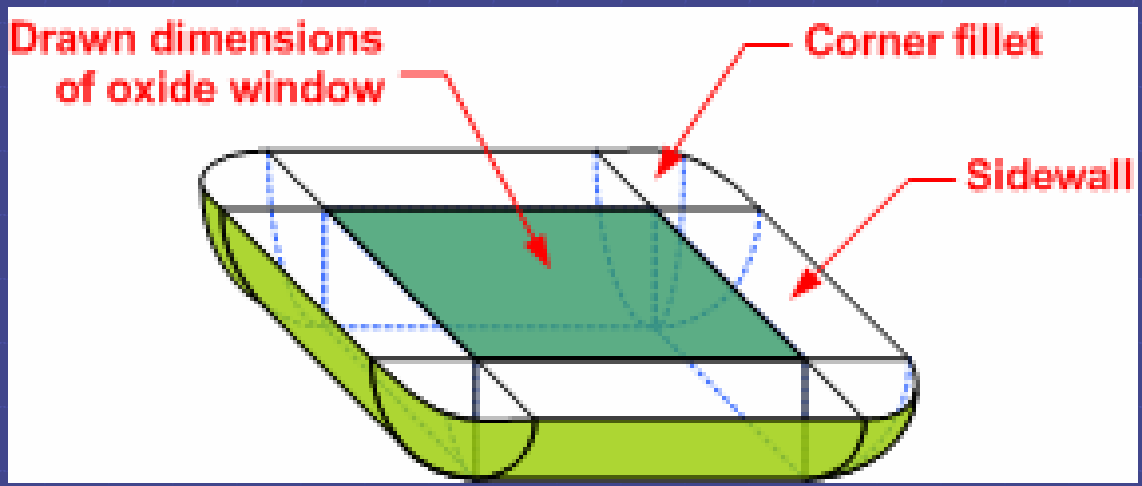

C4 C4 C4
C4 C3 C3
C2 C1 C2
C3 C3 C4
C4 C4 C4

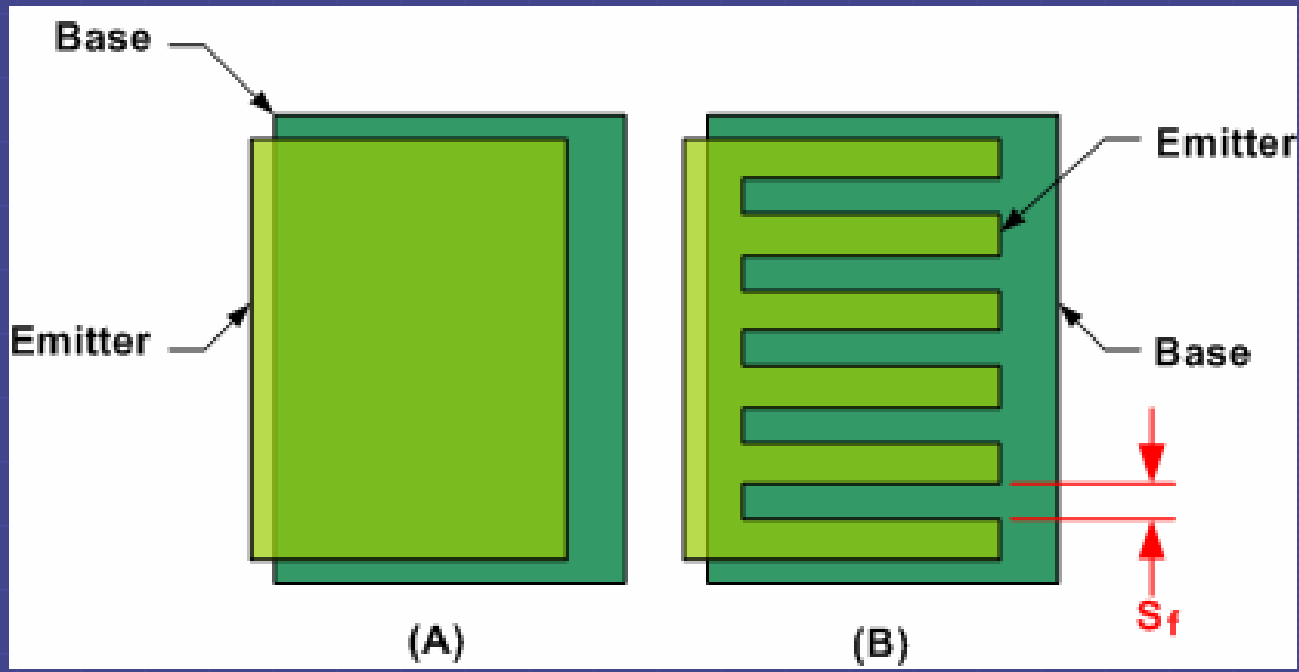
Illustration of the fringing field surrounding a parallel –plate capacitor embedded in a dielectric of constant permittivity.



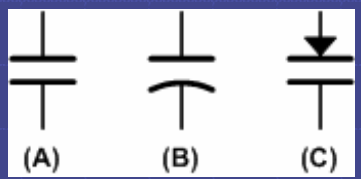
Three – dimensional view of a diffused junction, showing the sidewalls and filleted corners produced by outdiffusion beyond the drawn dimensions of the oxide window.



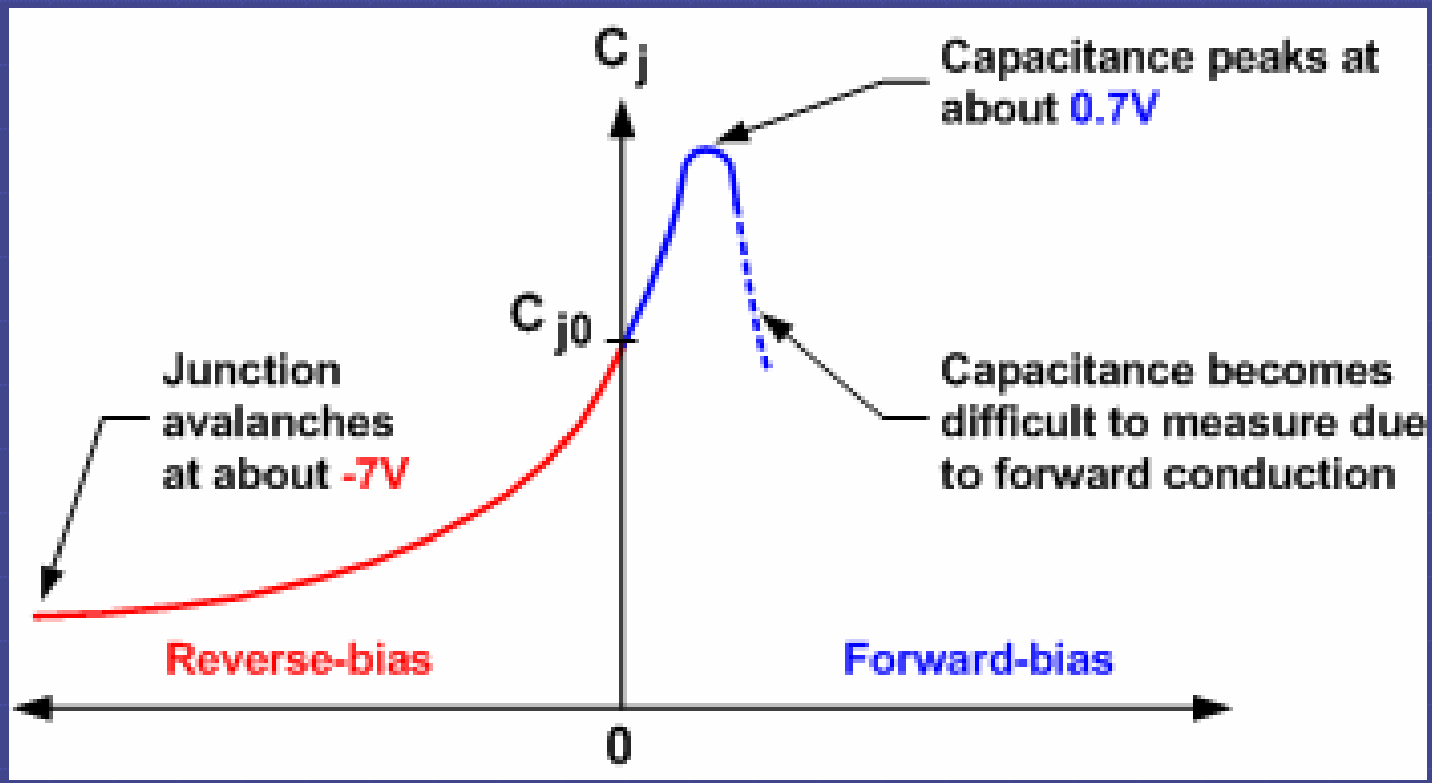
Two different styles of diffusion capacitor: (a) plate and (b) comb. The tank, NBL, contact, and metal layers are omitted for clarity.



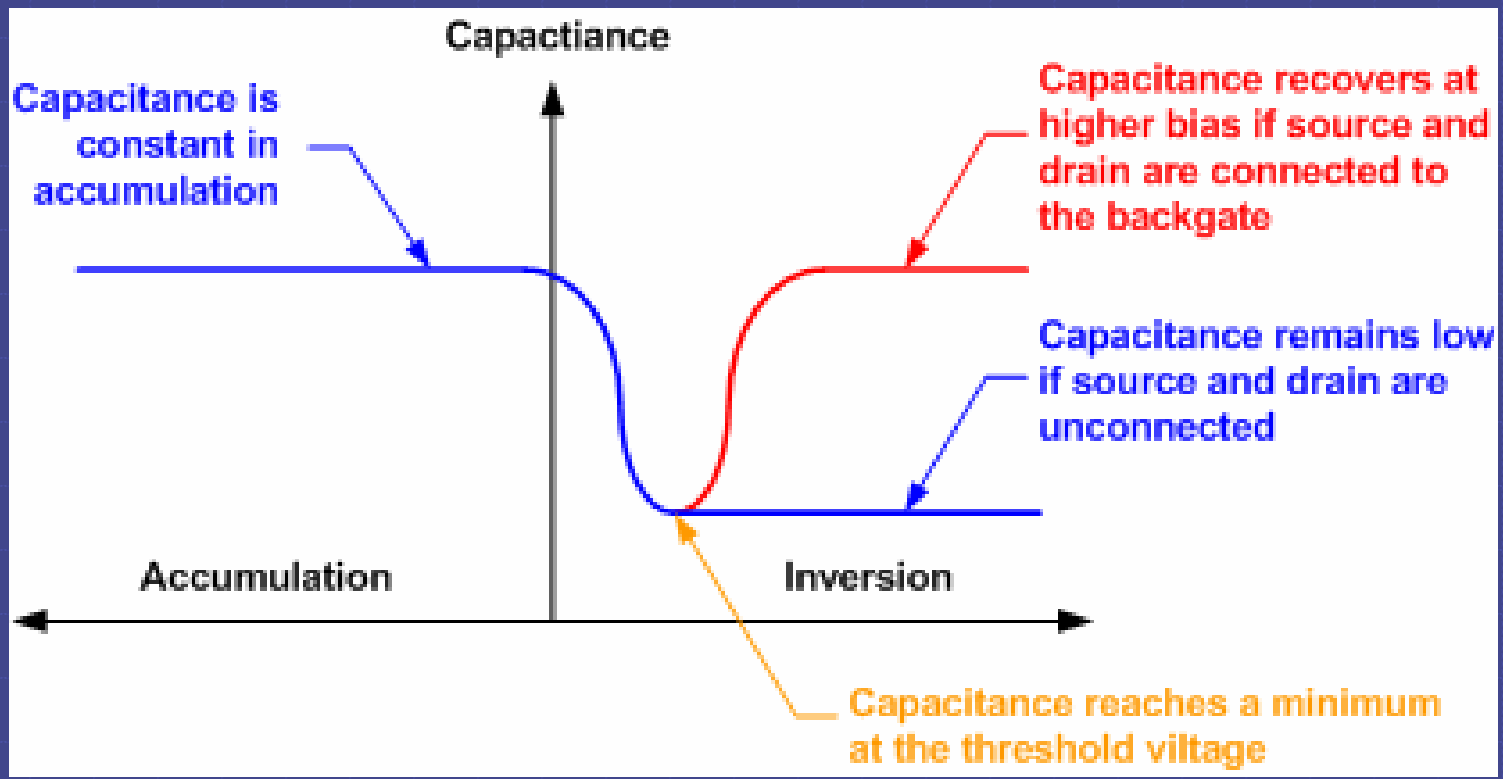
Typical schematic symbols for capacitors.



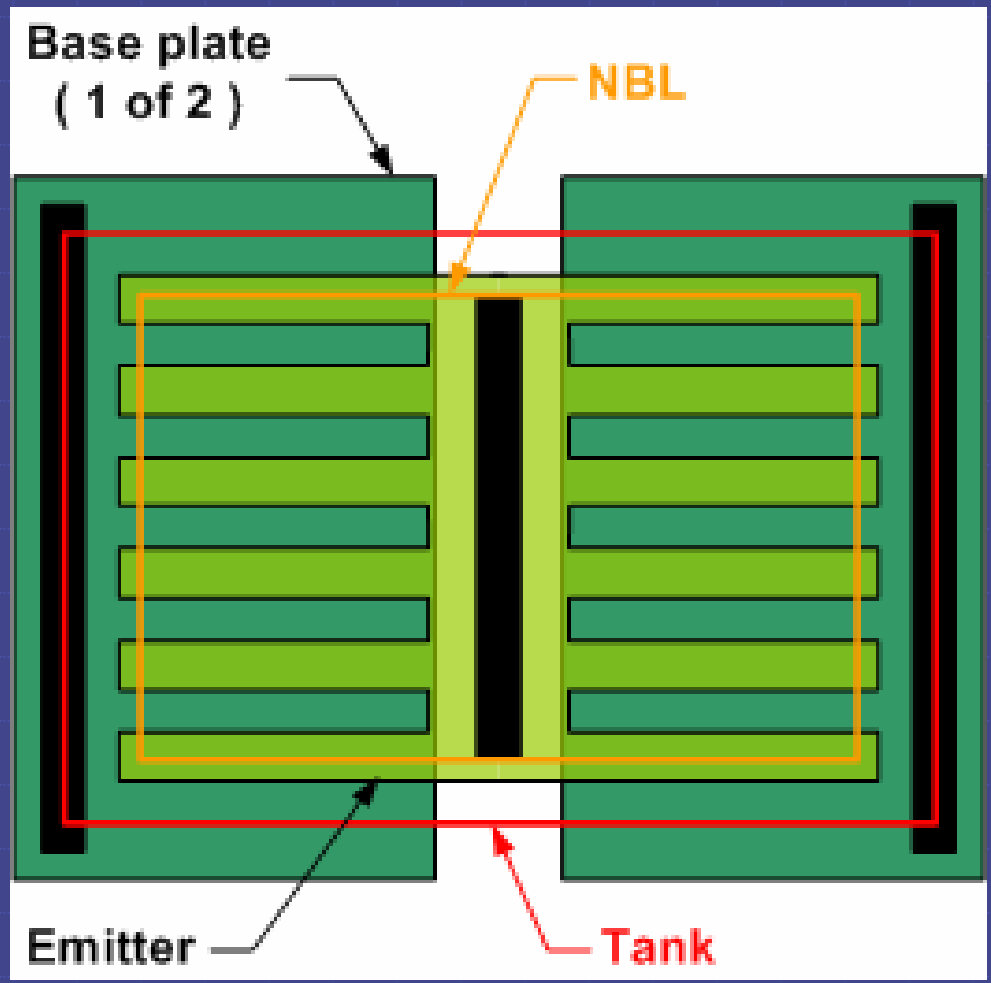
General behavior of base- emitter junction capacitance under bias. The minimum capacitance just prior to avalanche equals about 40 to 50% of the zero- bias value $C_{j\theta}$.



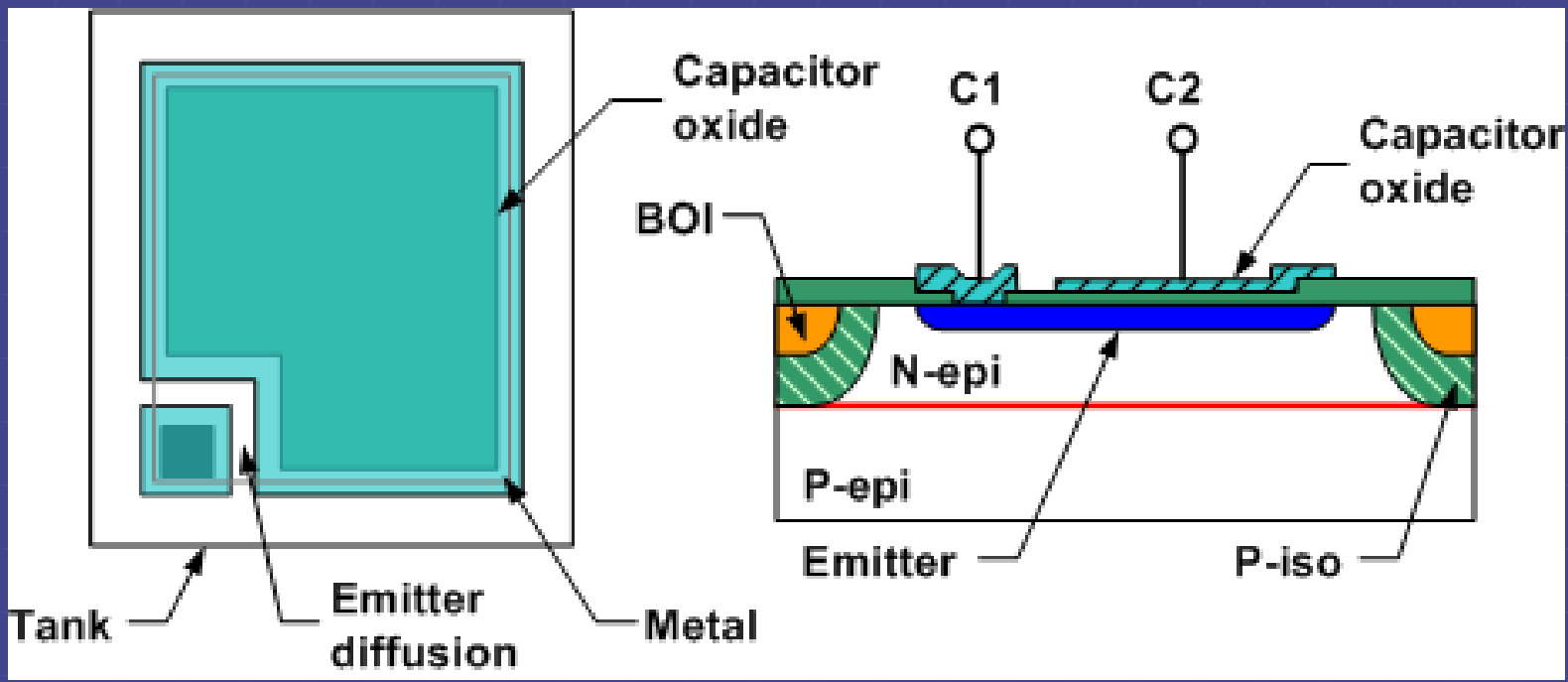
General behavior of a MOS transistor employed as a capacitor. Different curves are obtained depending on the connection of the source and the drain.



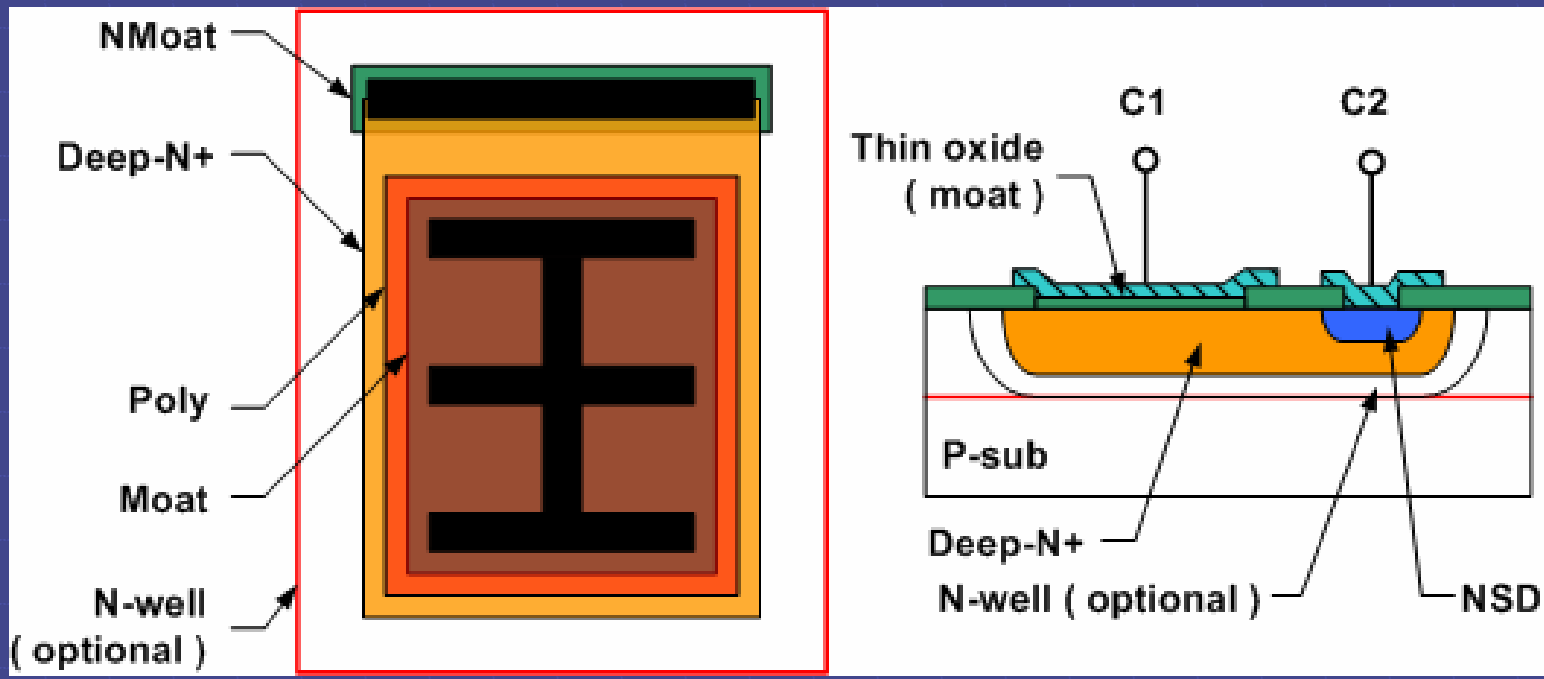
A junction capacitor with base plates extending into isolation.



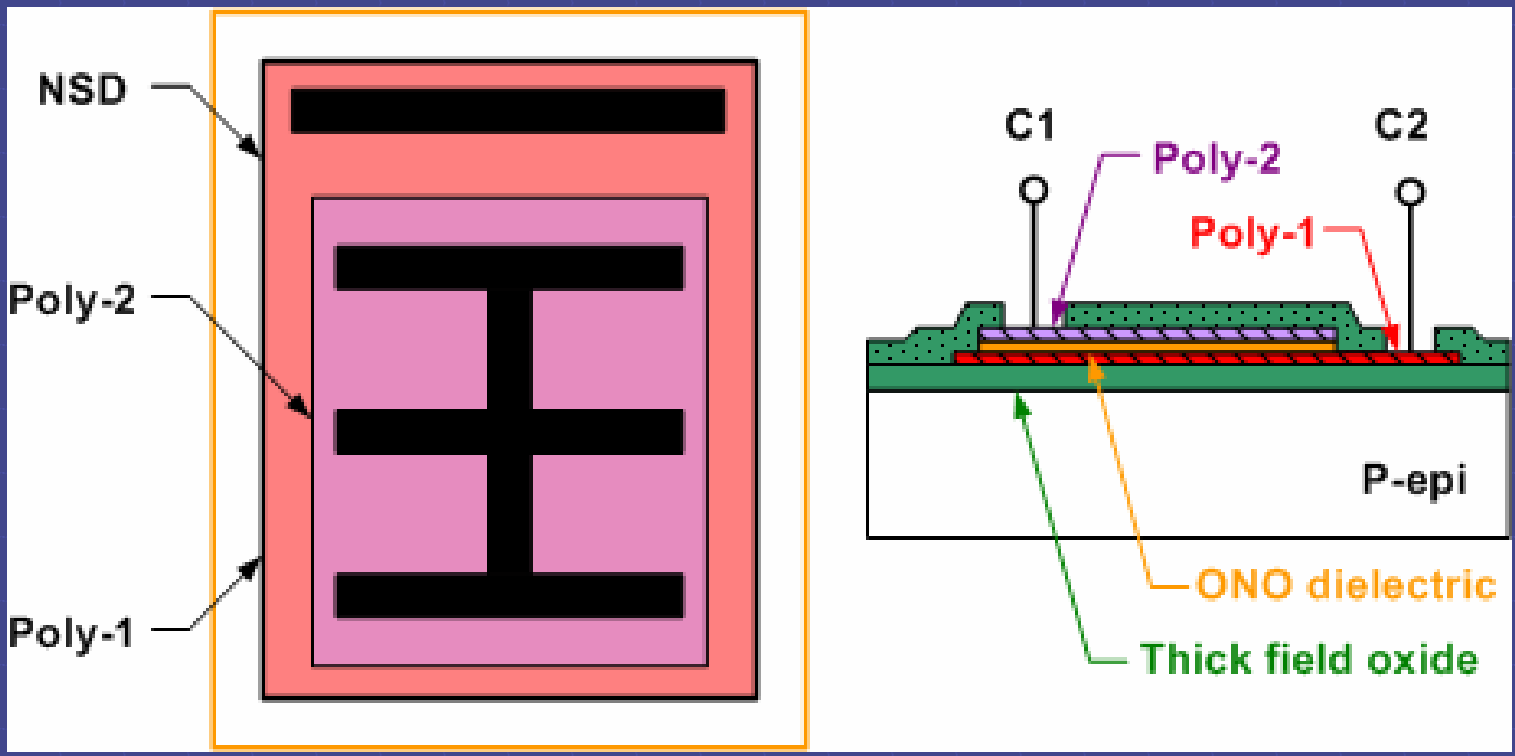
Layout and cross section of an MOS capacitor constructed in a standard bipolar process using a capacitor oxide mask.



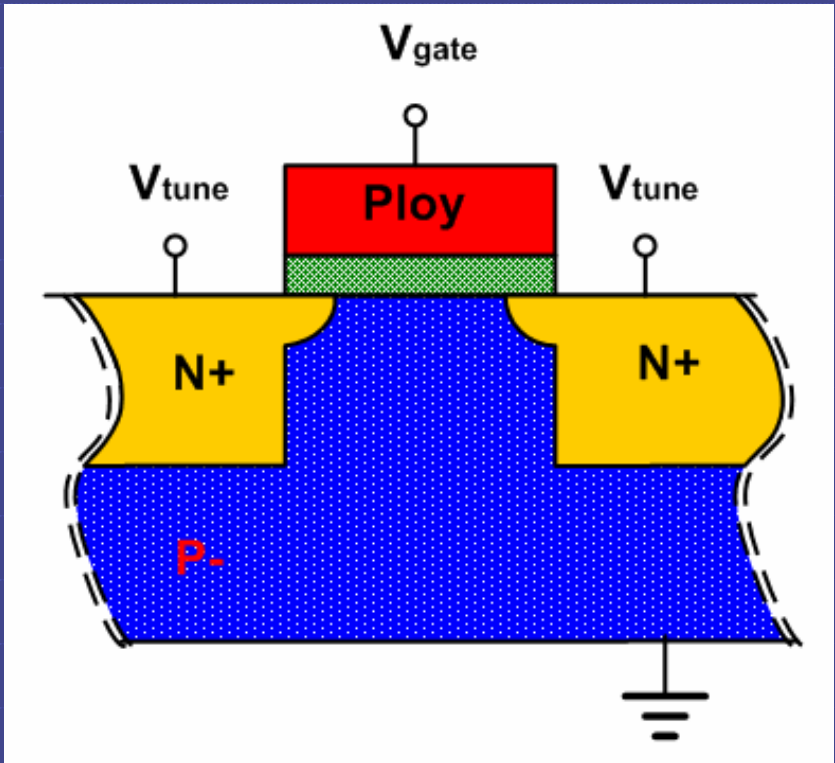
Layout and cross section of a deep-N+ MOS capacitor constructed in an analog BiCMOS process.

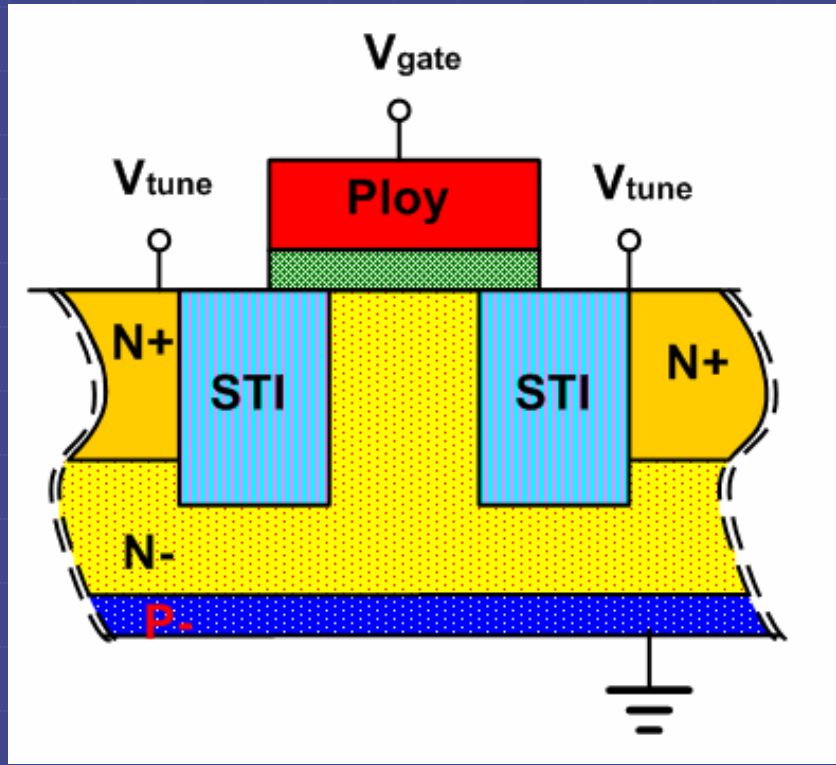


Layout and cross section of a poly-poly ONO capacitor. The entire capacitor has been enclosed in NSD because the gate poly is also N-type and the additional dopant only further reduces its sheet resistance .

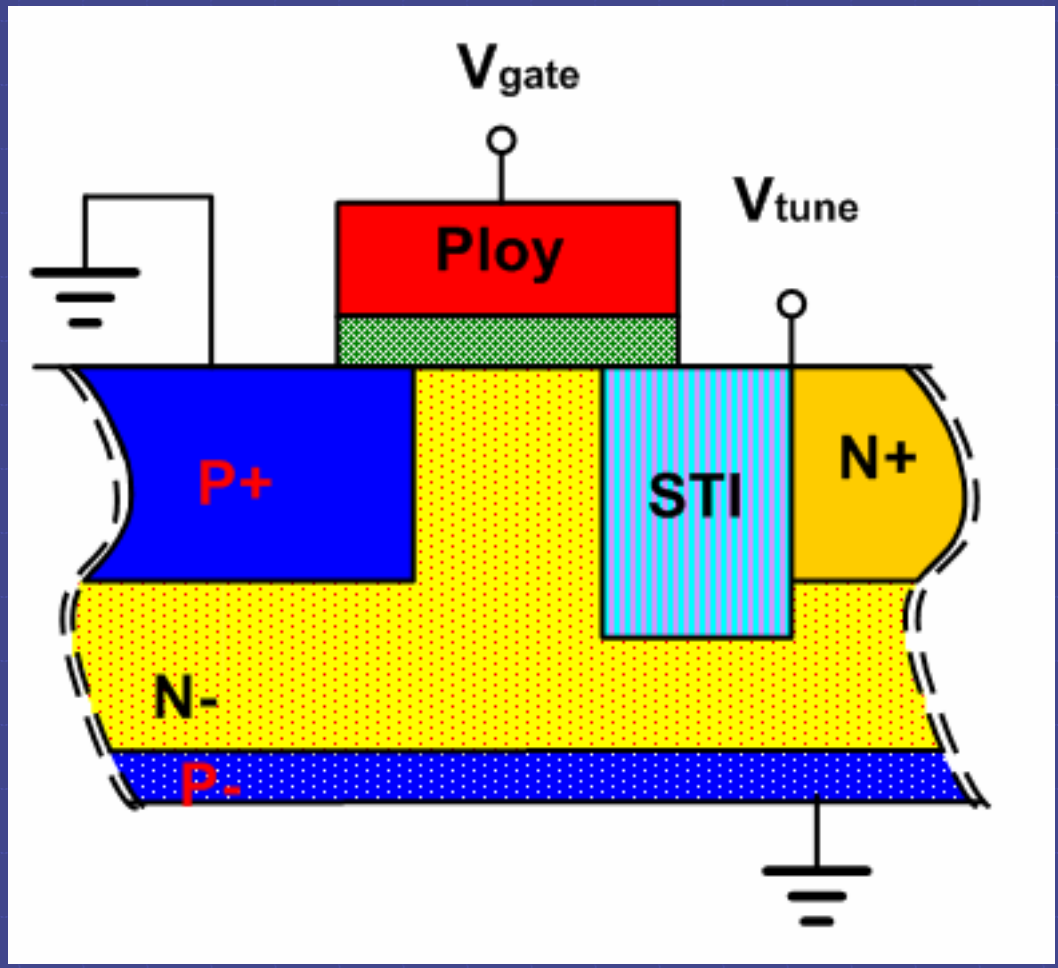


Varactor

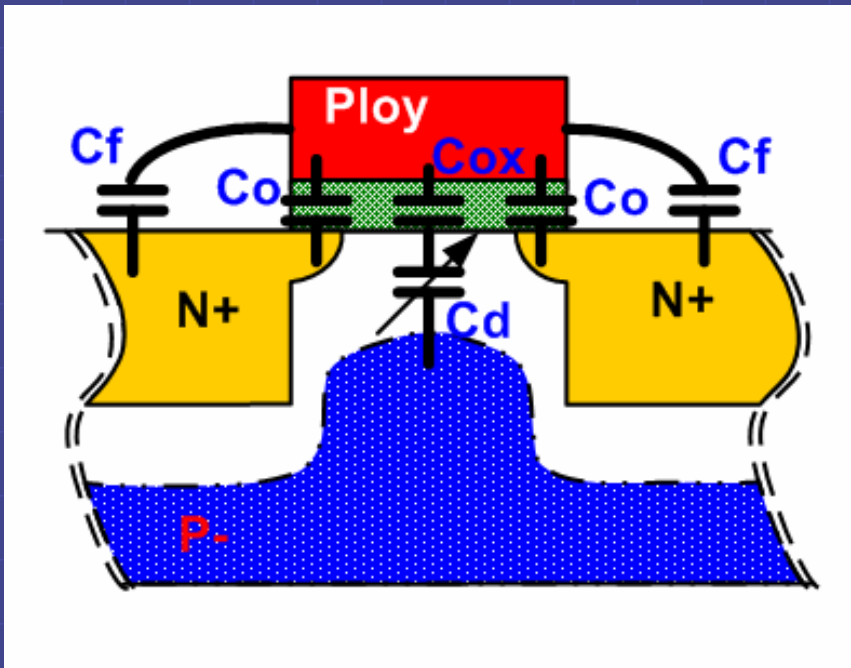

Vgate
Vtune
Ploy
Vtune
N+
N+
P-

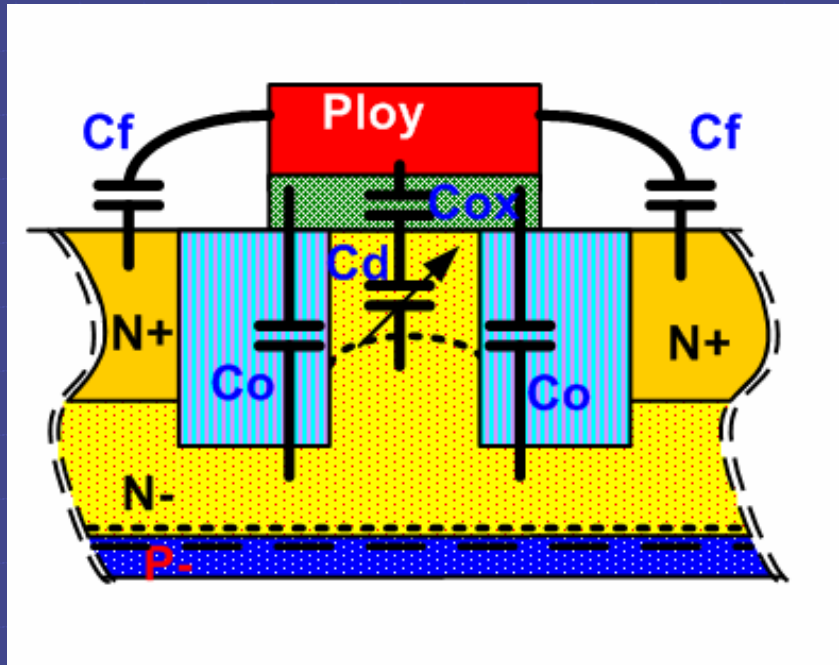

Vgate
Vtune
Ploy
Vtune
N+
STI
STI
N+
N-
P-

Varactor



Varactor





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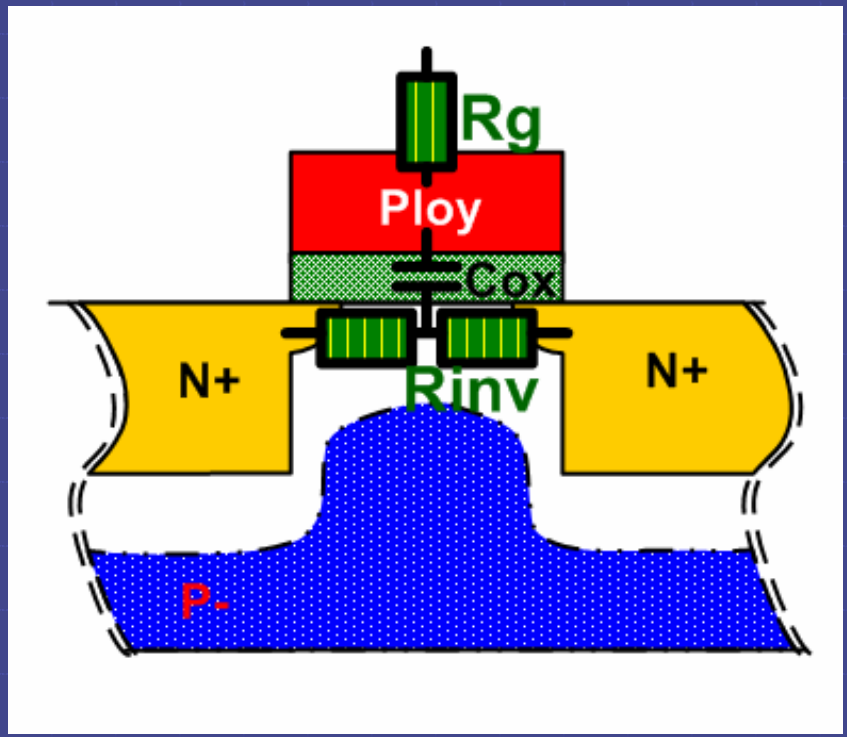
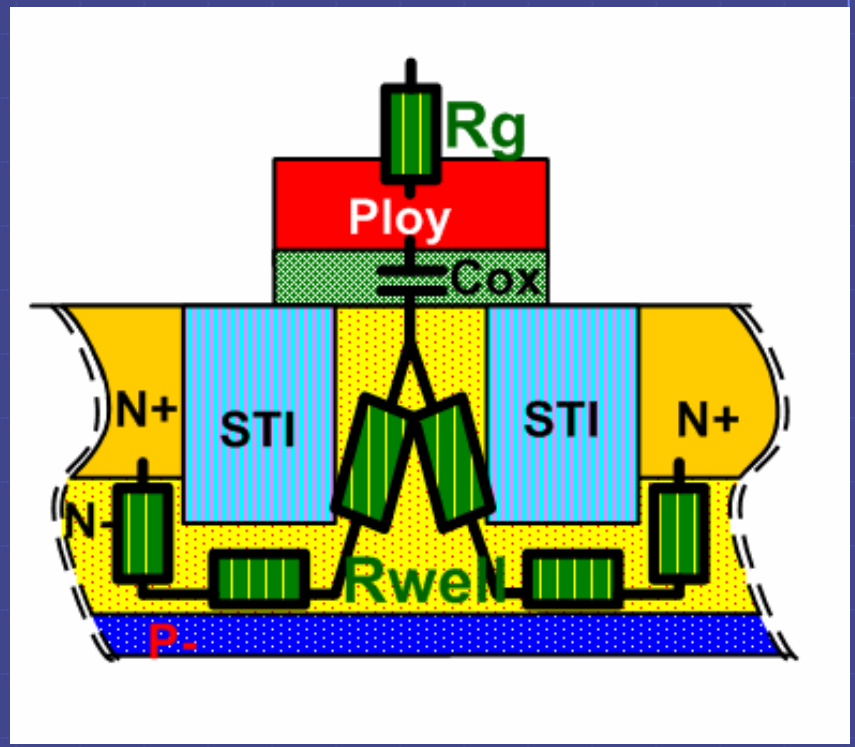
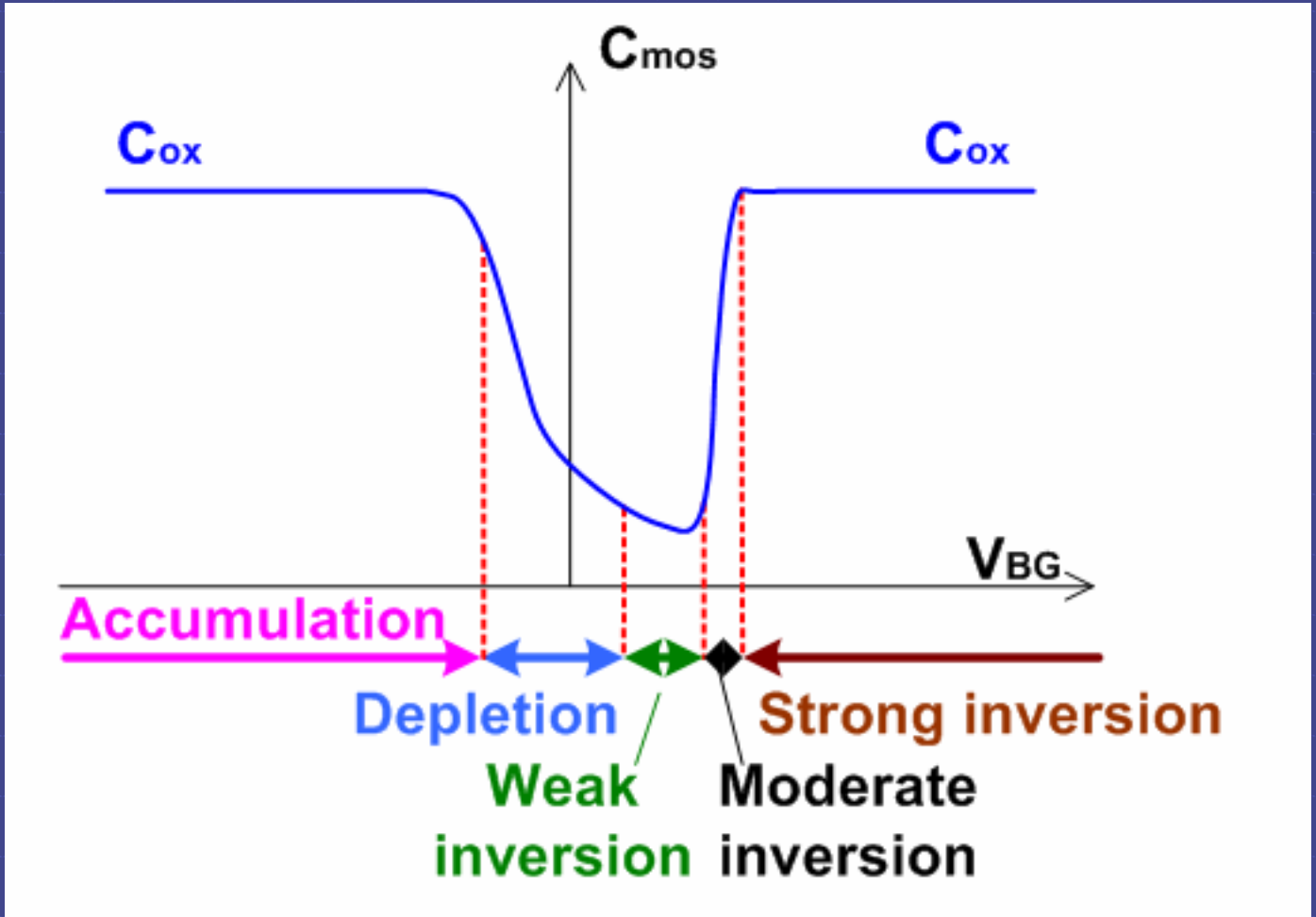
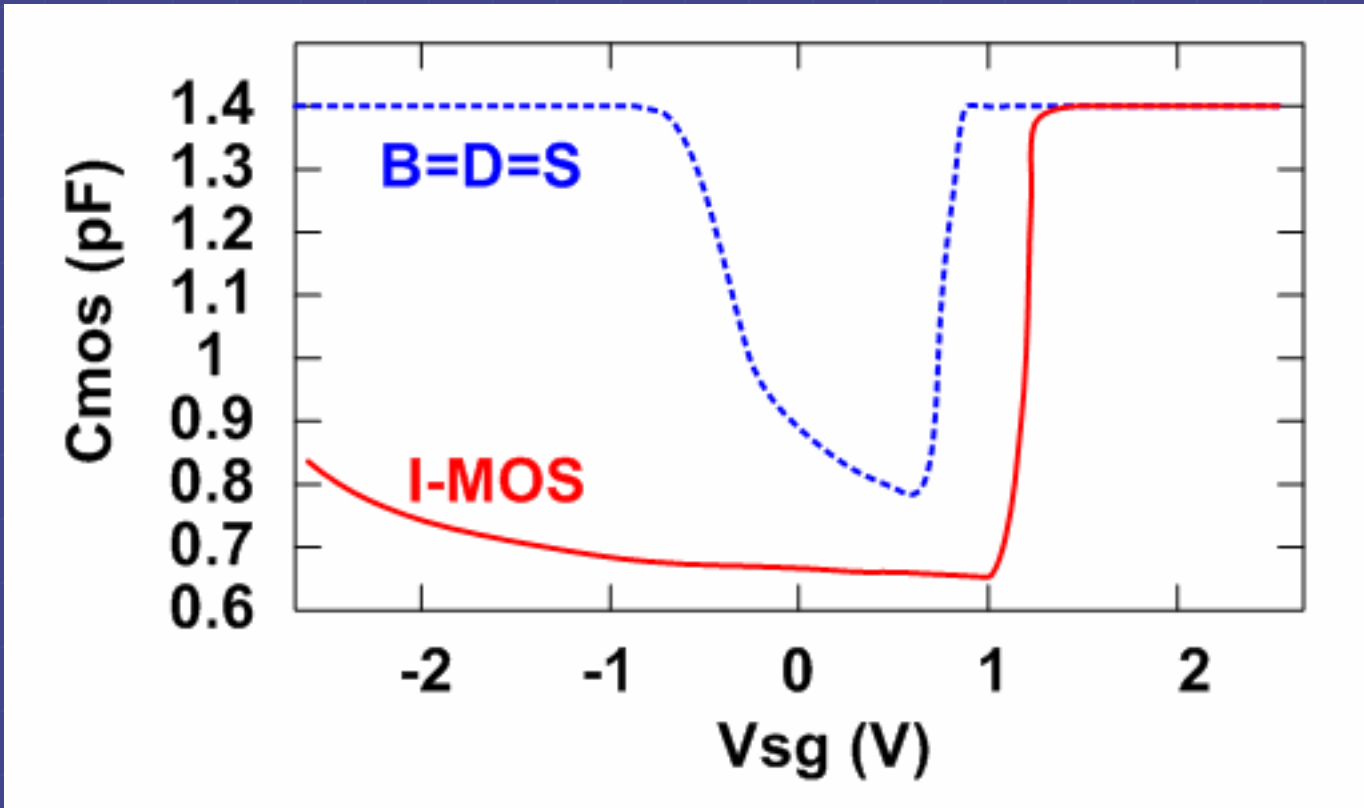




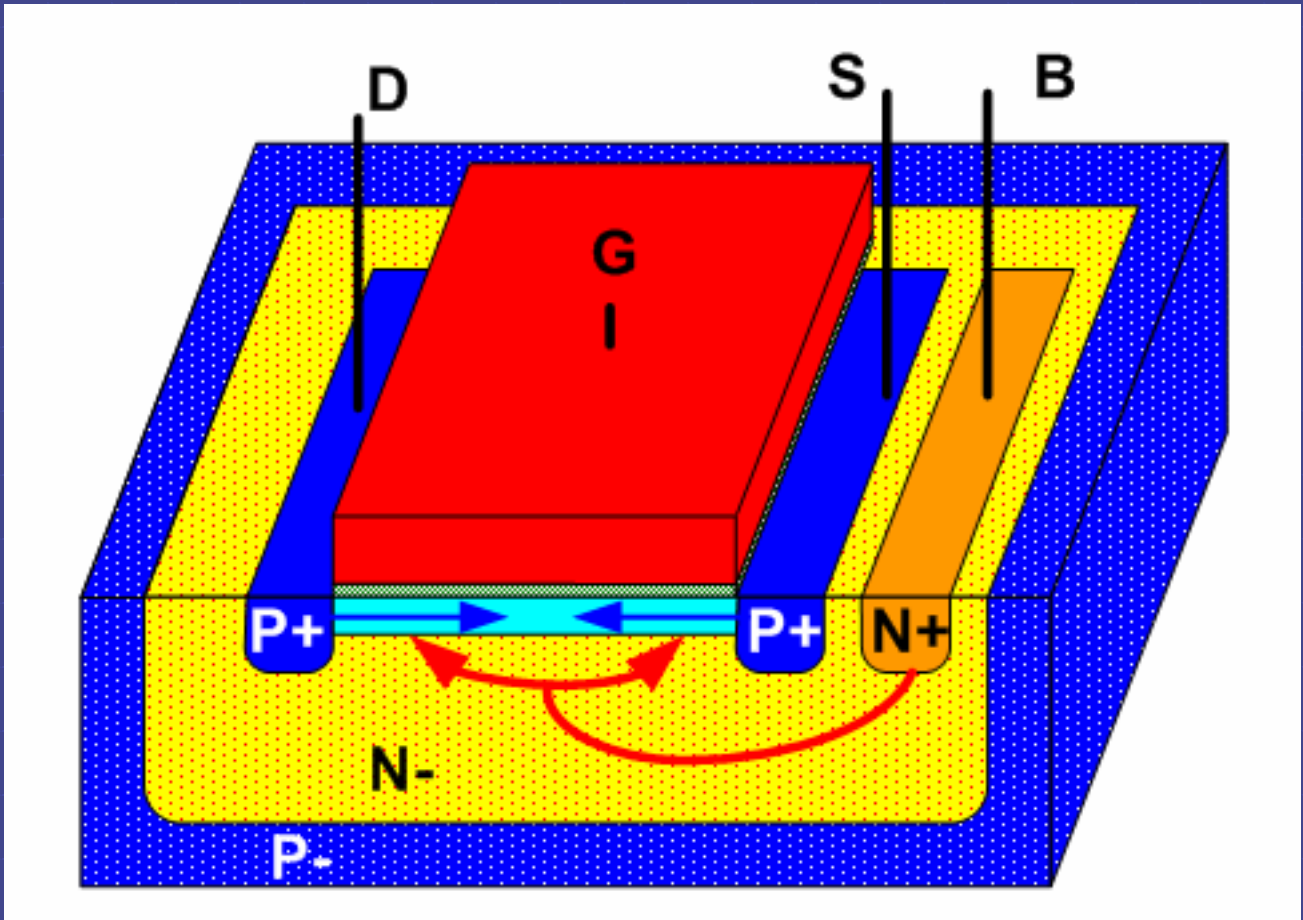
Varactor


Cmos
Cox
Cox
VBG
Accumulation
Depletion
Weak inversion
Moderate inversion
Strong inversion

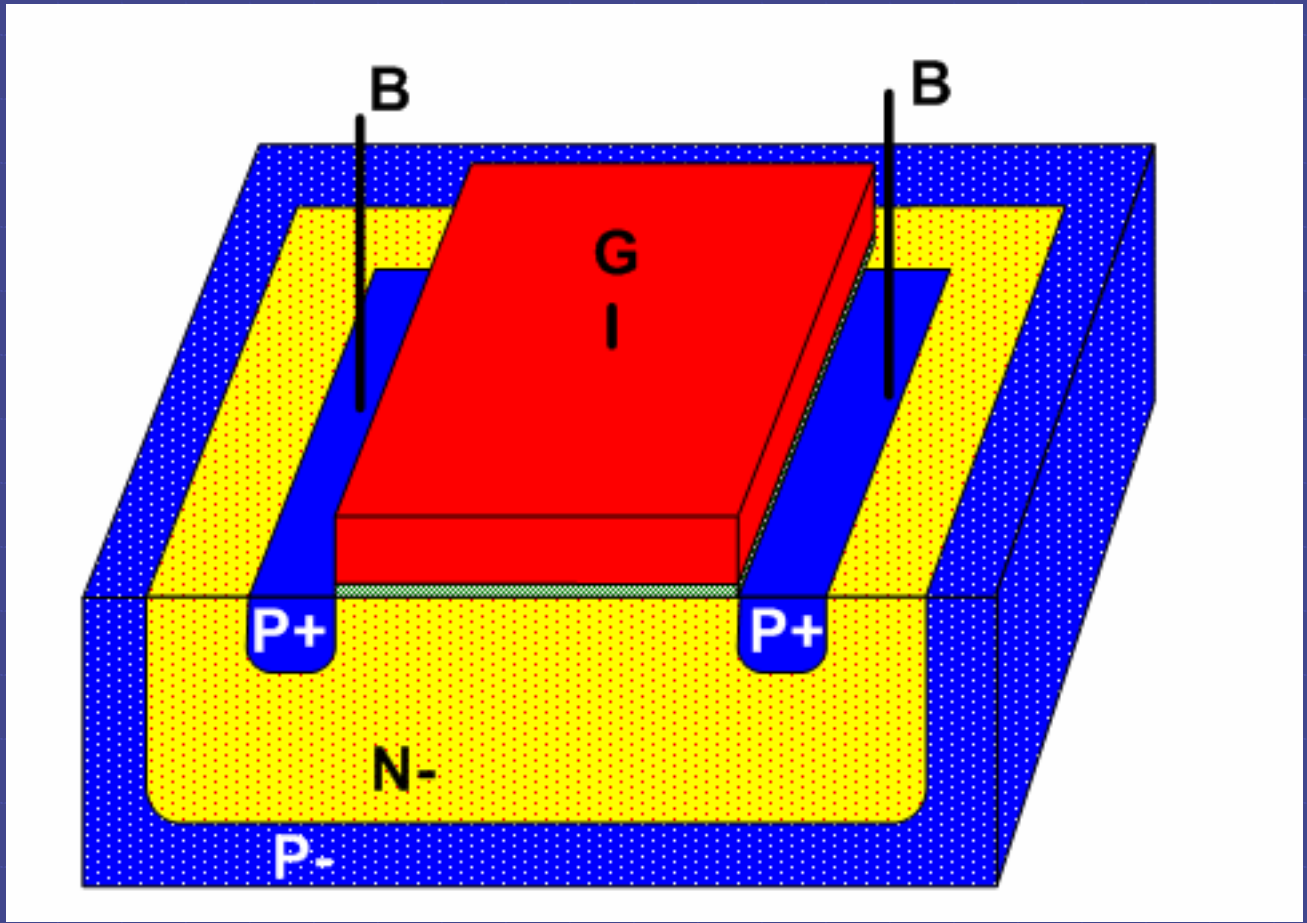
Varactor



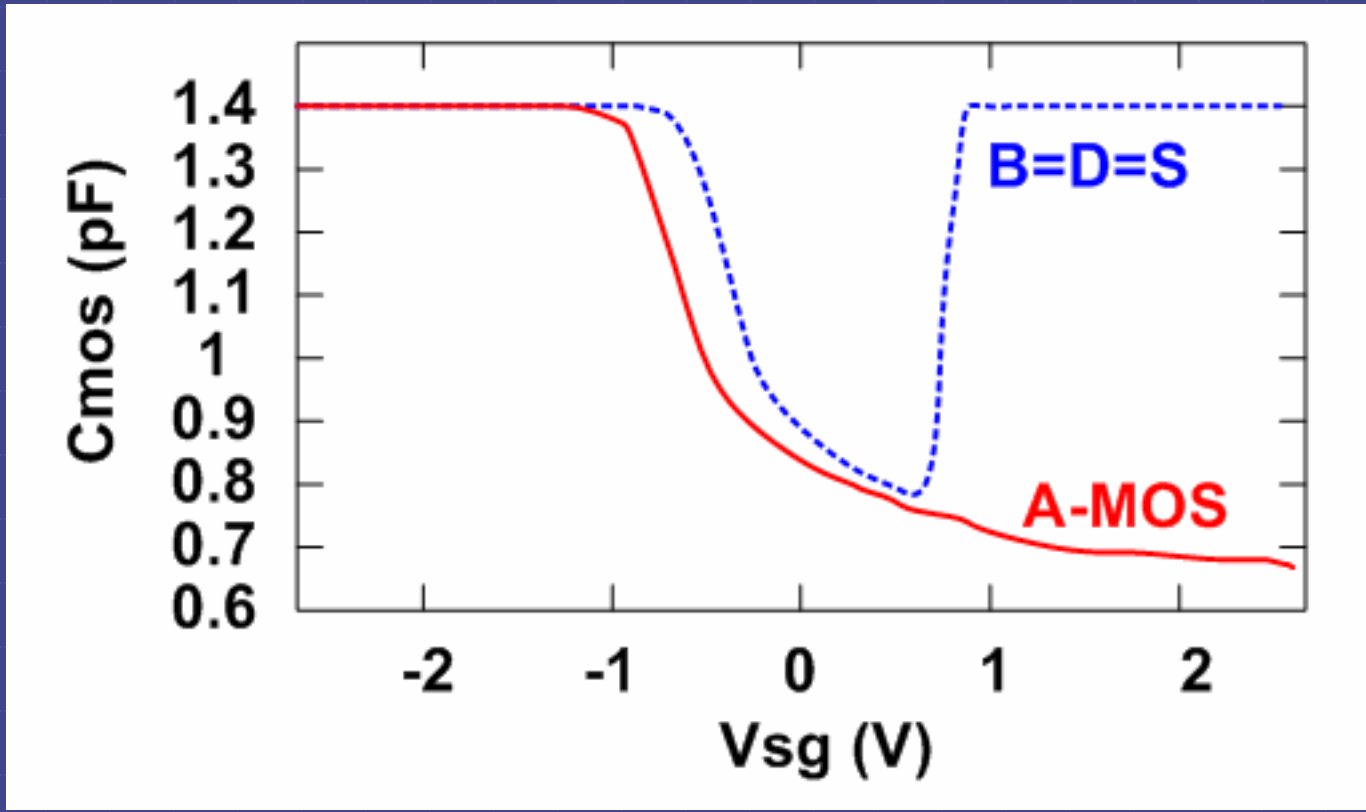
Varactor



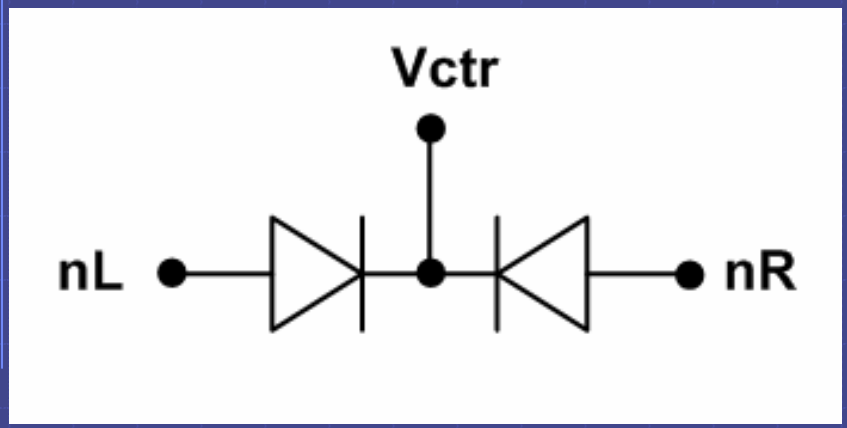
Varactor

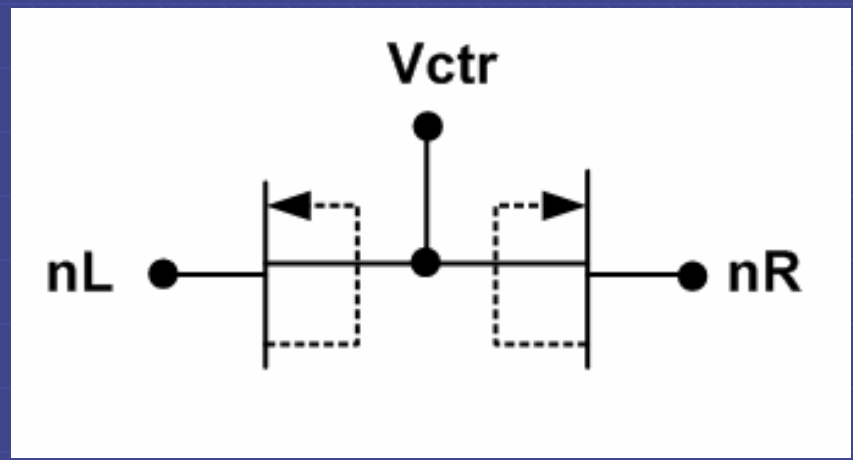


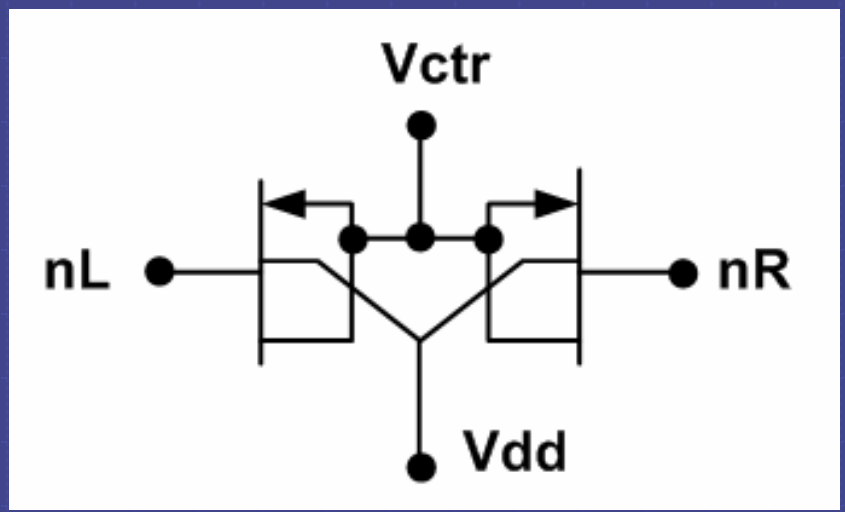
Varactor



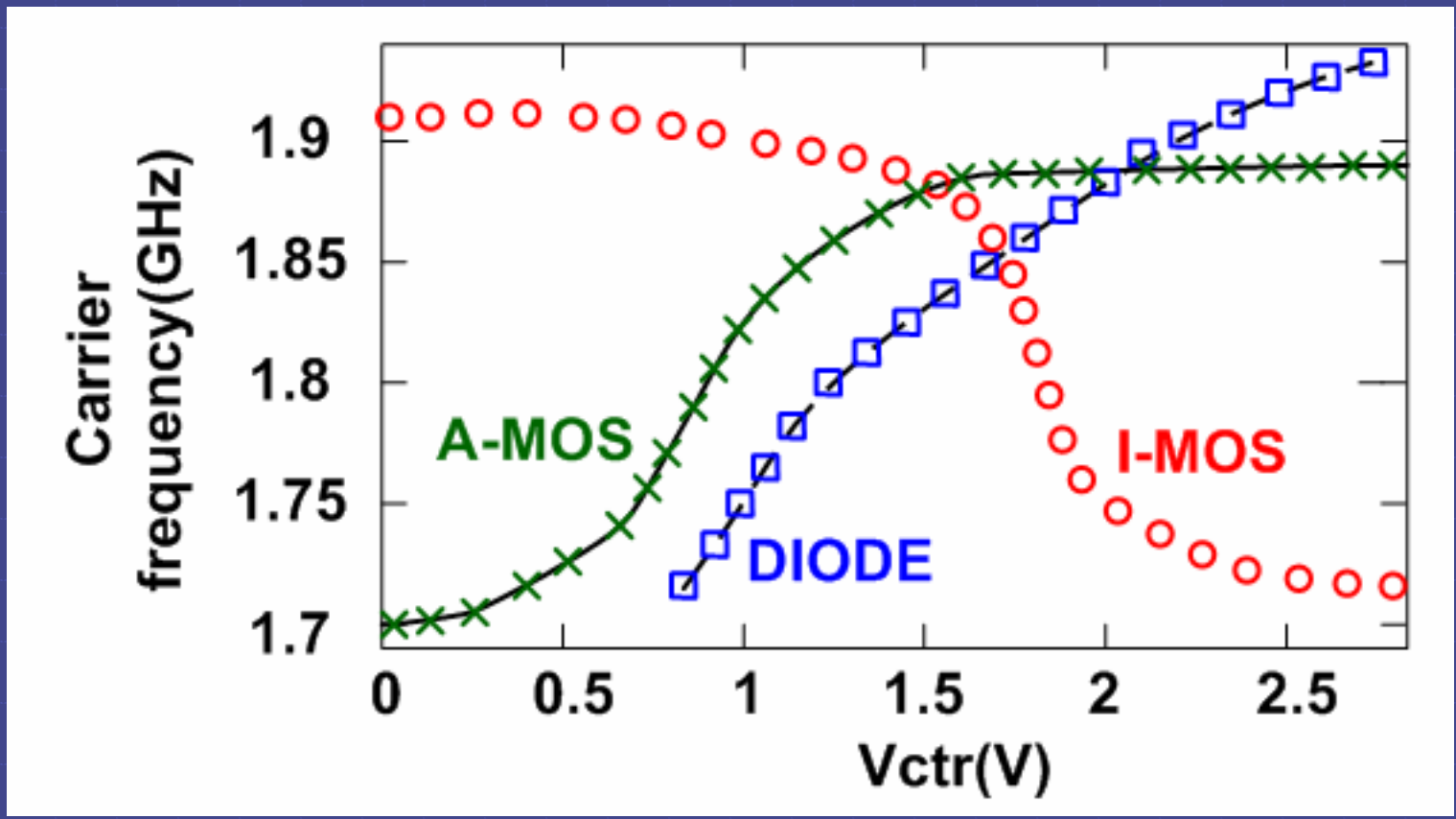
Varactor







Varactor


Carrier frequency(GHz)
1.9
1.85
1.8
1.75
1.7
0
0.5
1
1.5
2
2.5
Vctr(V)
A-MOS
DIODE
I-MOS

Varactor

Varactor	f_L-f_H (GHz)	f_C(GHz)	Tuning range
Diode	1.73-1.93	1.83	10.9%
I-MOS	1.71-1.91	1.81	11.0%
A-MOS	1.70-1.89	1.80	10.6%